Betriebssysteme

6. Tutorium - Paging

Peter Bohner

6. Dezember 2023

ITEC - Operating Systems Group

Feedback 2. Übungsblatt

- Danke an die 2, die regelmäßig abgeben :)
- Niemand hat die Fadenschwimmbecken-Aufgabe[1] gelöst

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- No external fragmentation, little internal

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Segment and Page tables

Segment Number	Base	Limit
0	0xdead	0x00ef
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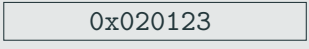

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0x020123

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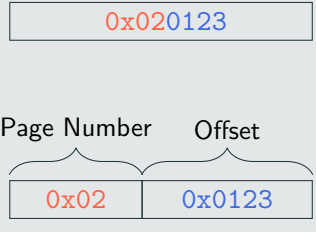

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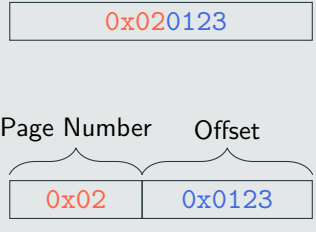

pfn	flags
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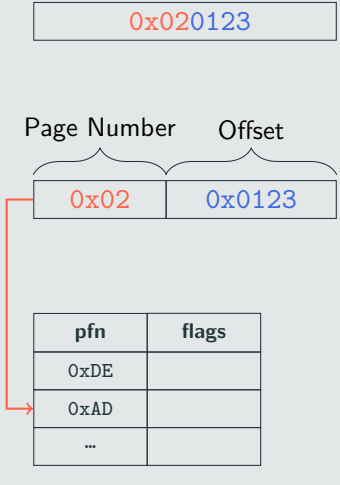

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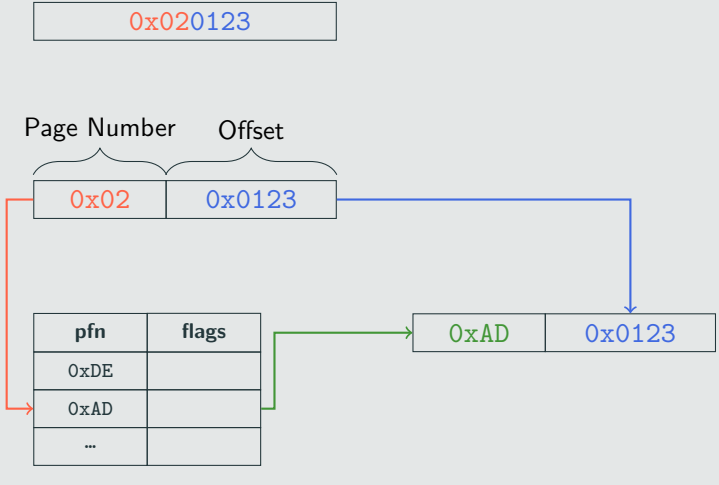

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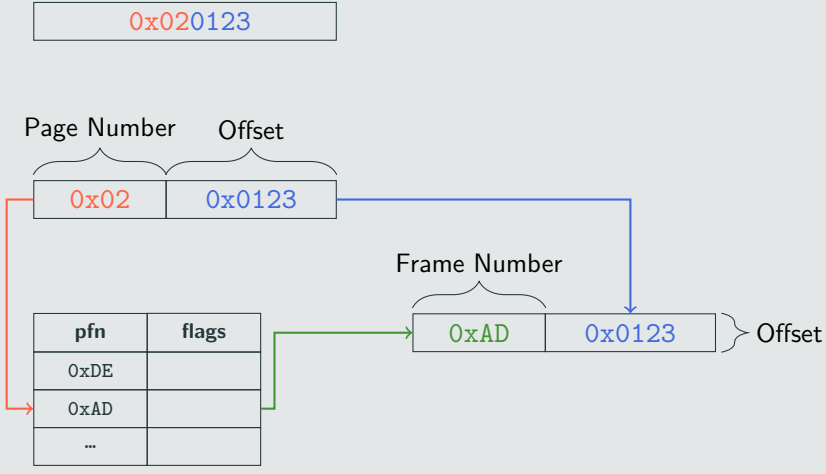

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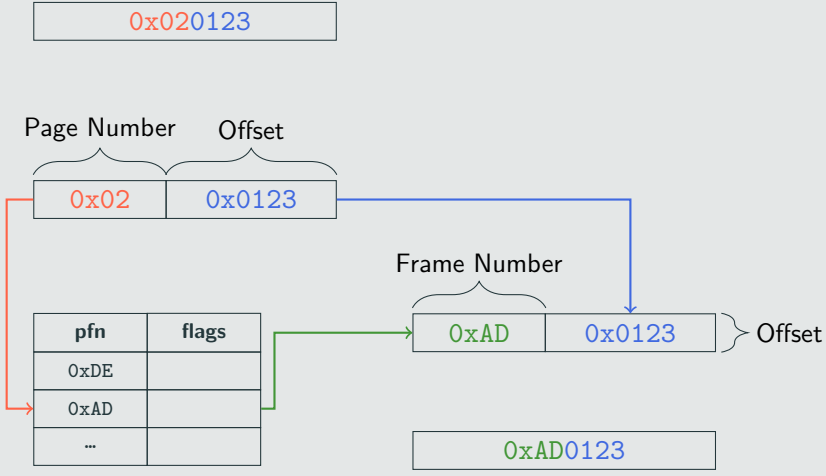

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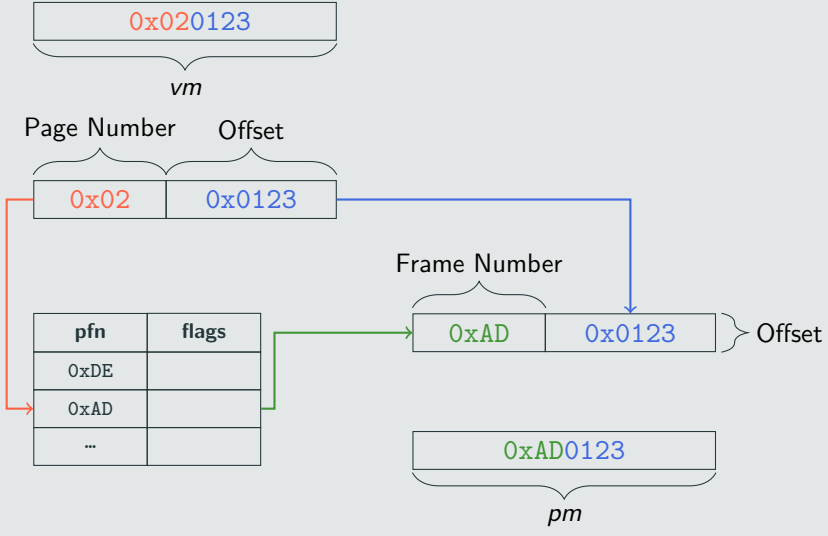

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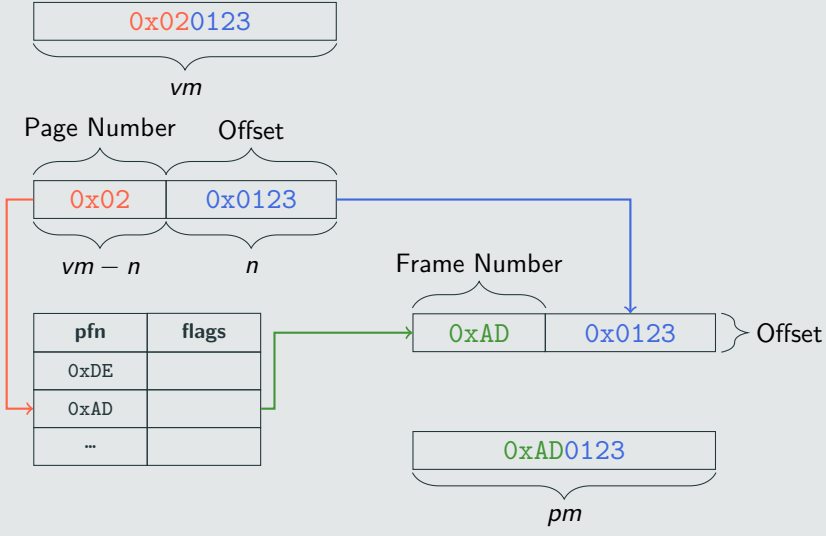

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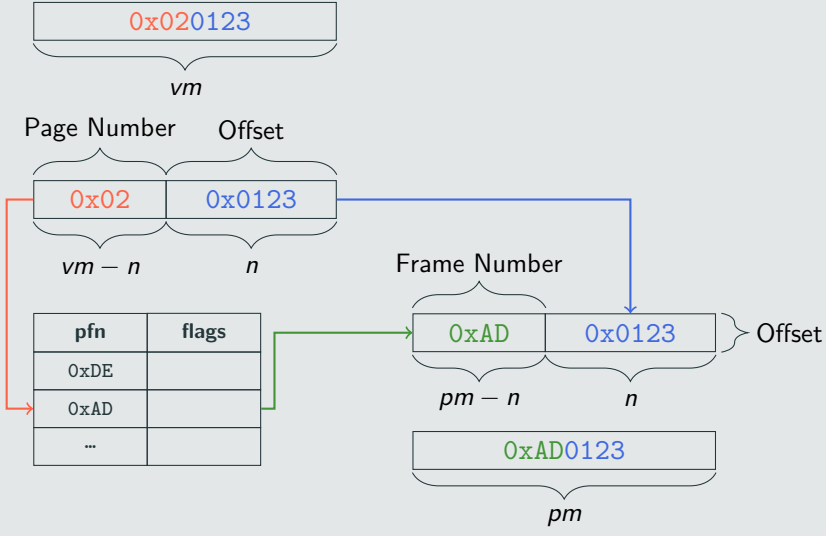

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$\Rightarrow$ If every entry was 1 Bit we'd need (asking `units`...)

```
You have: 2^52 bit
You want: tebibyte
        * 512
        / 0.001953125
```

- You might *not* have that much memory to spare :)

Single Level Page Table - Disadvantages

Math is fun, let's do some math

Calculate the space requirements for a single level page table with

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- vm $= 48$, 4Kib $= 2^{12} \Rightarrow$ n $= 12$
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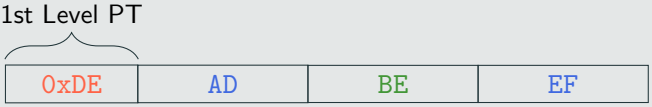

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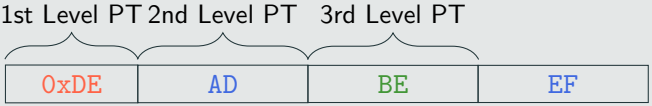

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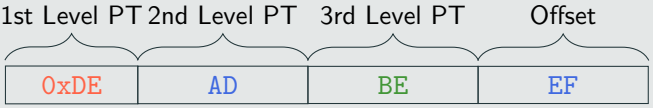

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- \- Pointer chasing down each level ⇒ More memory accesses
- \+ Address spaces are *sparse* ⇒ Only instantiate page tables you need

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- That requires iteration :(

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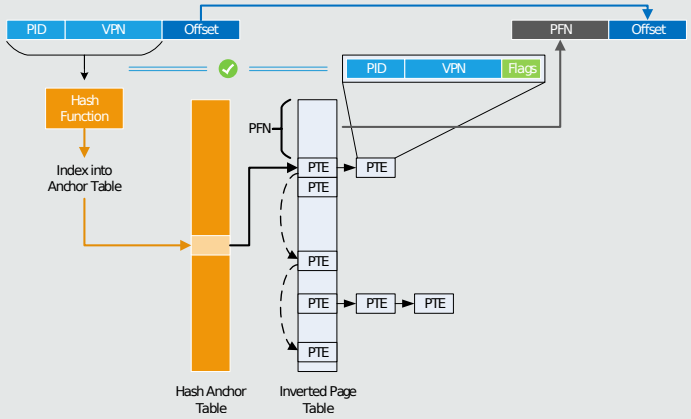

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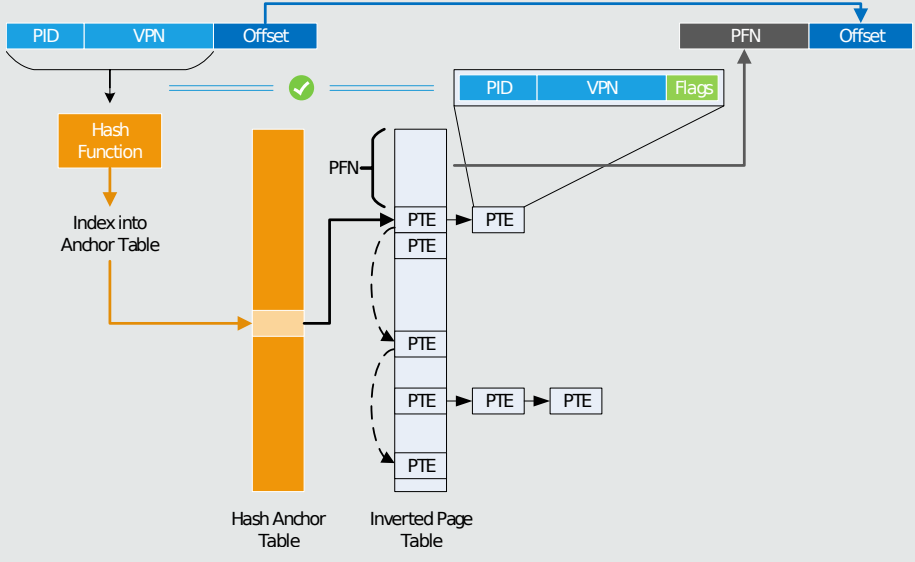

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- Page fault!
- Handle it and do sth. sensible (or crash the process...)

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$\Rightarrow$ There is no problem you can't solve with another caching layer (except having too many caching layers) Nearly the Fundamental theorem of software engineering

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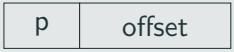

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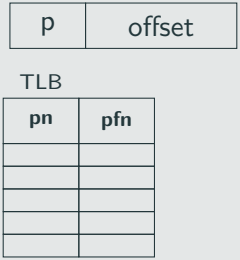

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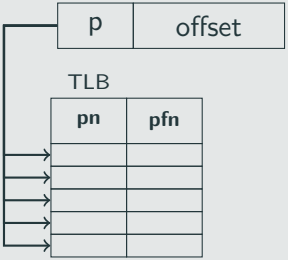

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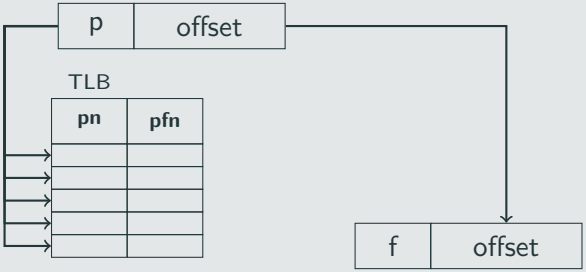

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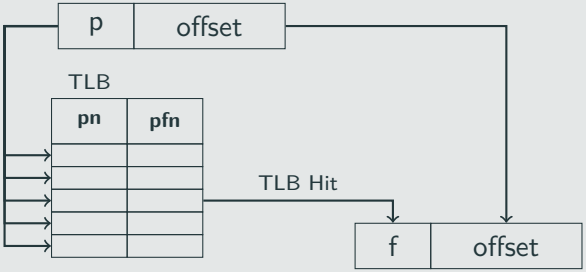

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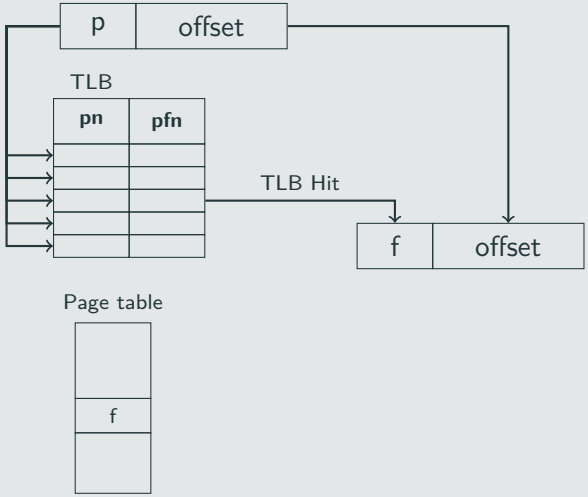

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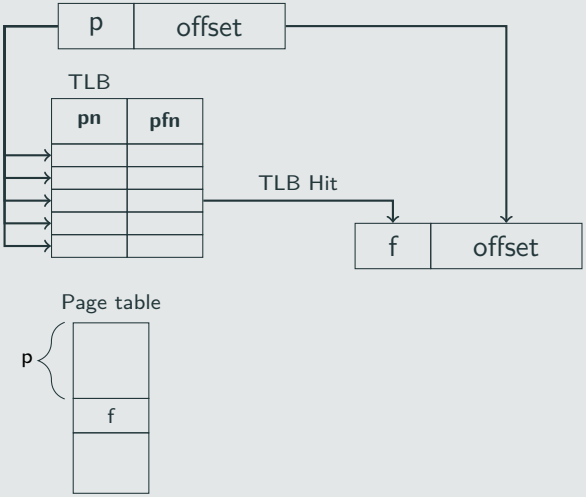

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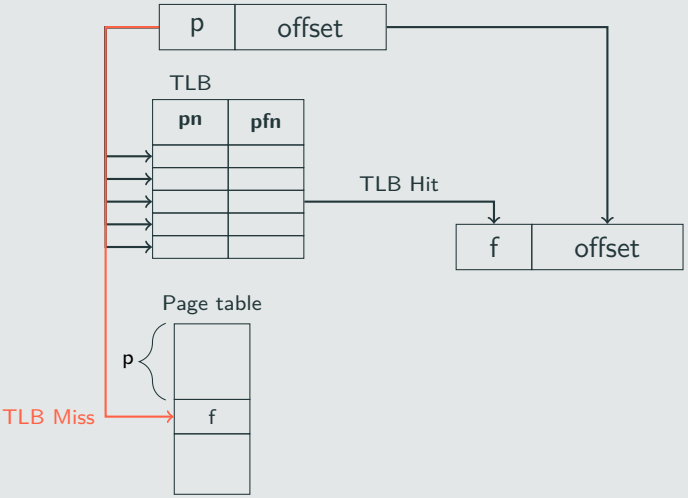

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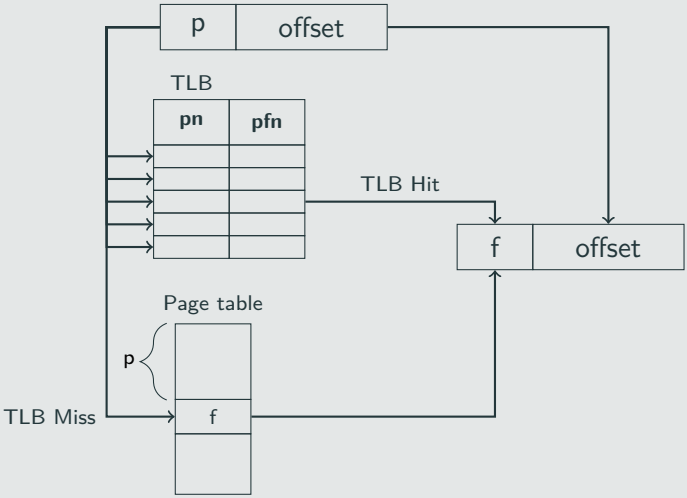

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- Hardware looks at your page table
- Hardware *resolves* the physical address using it
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$\Rightarrow$ What does that imply? Page table layout is fixed

Software walked

- Transfers control to TLB miss handler
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TLB - Misses

What is the difference between software and hardware walked TLBs?

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- Kernel routine walks the page table and tries to find a mapping
- Loads that mapping into the TLB and can choose which entry to evict!
- If there is none $\Rightarrow$ Jump to page fault handler

TLB - Software or hardware walked

What are benefits / drawbacks of software walked TLBs?

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+ Free to choose which TLB entries to evict $\Rightarrow$ Use optimized strategy
- Greater overhead

TLB - Contents

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- Valid / Present Bit
- Modified bit, permissions, ...

TLB - Page faults

When is a TLB miss or page fault raised?

Due to the TLB:

- Software walked: No entry found in TLB $\Rightarrow$ TLB miss exception

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- Software walked: Raise some kind of TLB fault if the page is e.g. read-only
- Hardware walked: Page fault raised, page fault handler has to find out what happend

Page Fault Handling

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Page Fault Handling

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Why would you (not?) use Demand-Paging?

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- Generates lots of page faults before working set is in memory

Page Fault Handling

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+ Might reduce number of page faults
- Loads more than needed $\Rightarrow$ Wasteful
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+ HDDs a lot faster when reading chunks

On-Demand Paging

Different kind of page faults

Not all pages are created equal. Do you have any idea what types of page faults typically exist?

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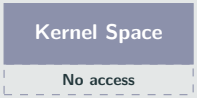

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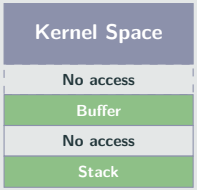

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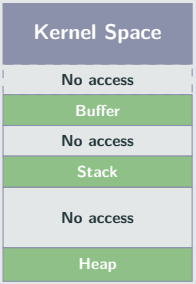

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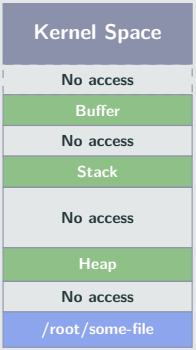

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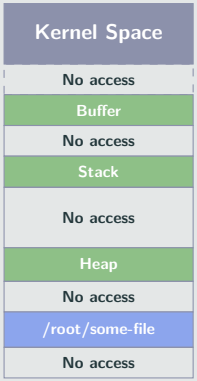

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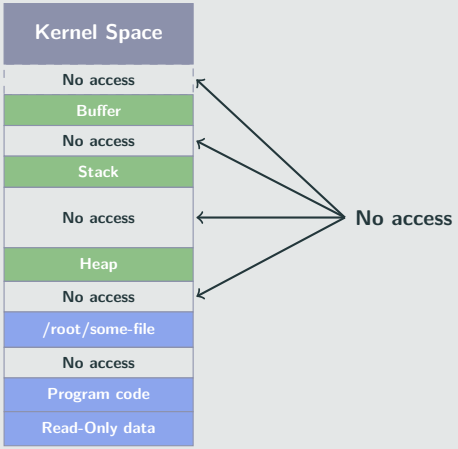

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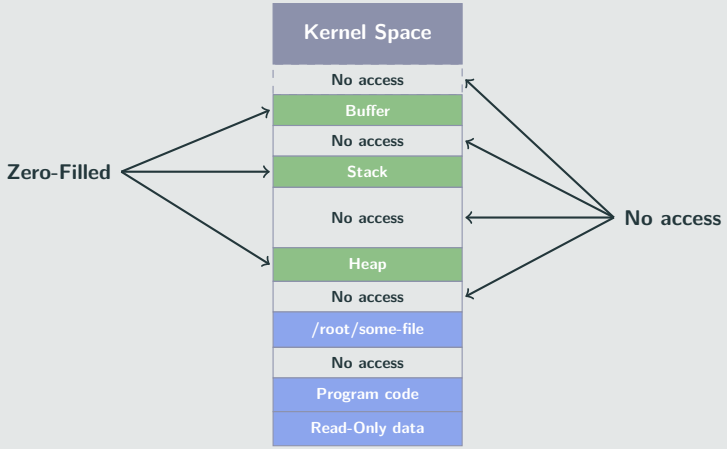

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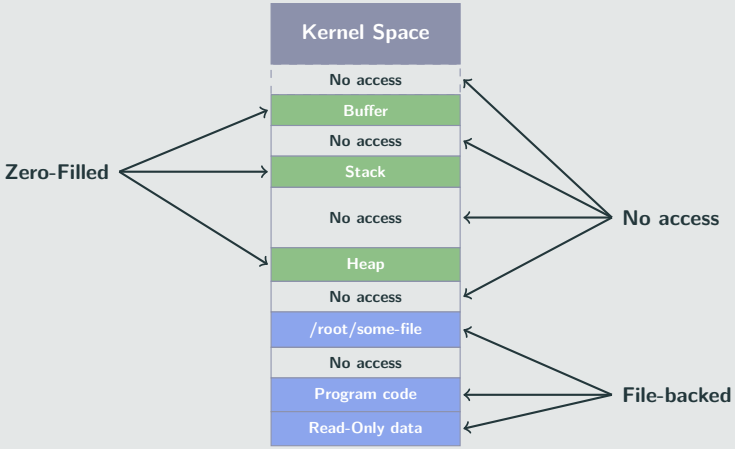

On Demand Paging

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And there is one other kind of page fault...

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Also supported on some systems: *Purgable memory*. Stolen from Apple and also implemented in SerenityOS in this video.

Page faults

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- Access flags: Can the user perform the operation on this page?
- Where to find the most recent version (different for zero filled, file backed, etc.)

CoW

How could you implement Copy-on-Write memory?

CoW

How could you implement Copy-on-Write memory?

- Mark memory as read-only on fork
- Add an additional `CoW` flag: When a page fault is raised check it, copy the page and clear the `CoW` and `ro` flag

Ende

XKCD 912 - Manual Override

F R A G E N?

https://forms.gle/9CwJSKidKibubran9

Bis nächste Woche :)