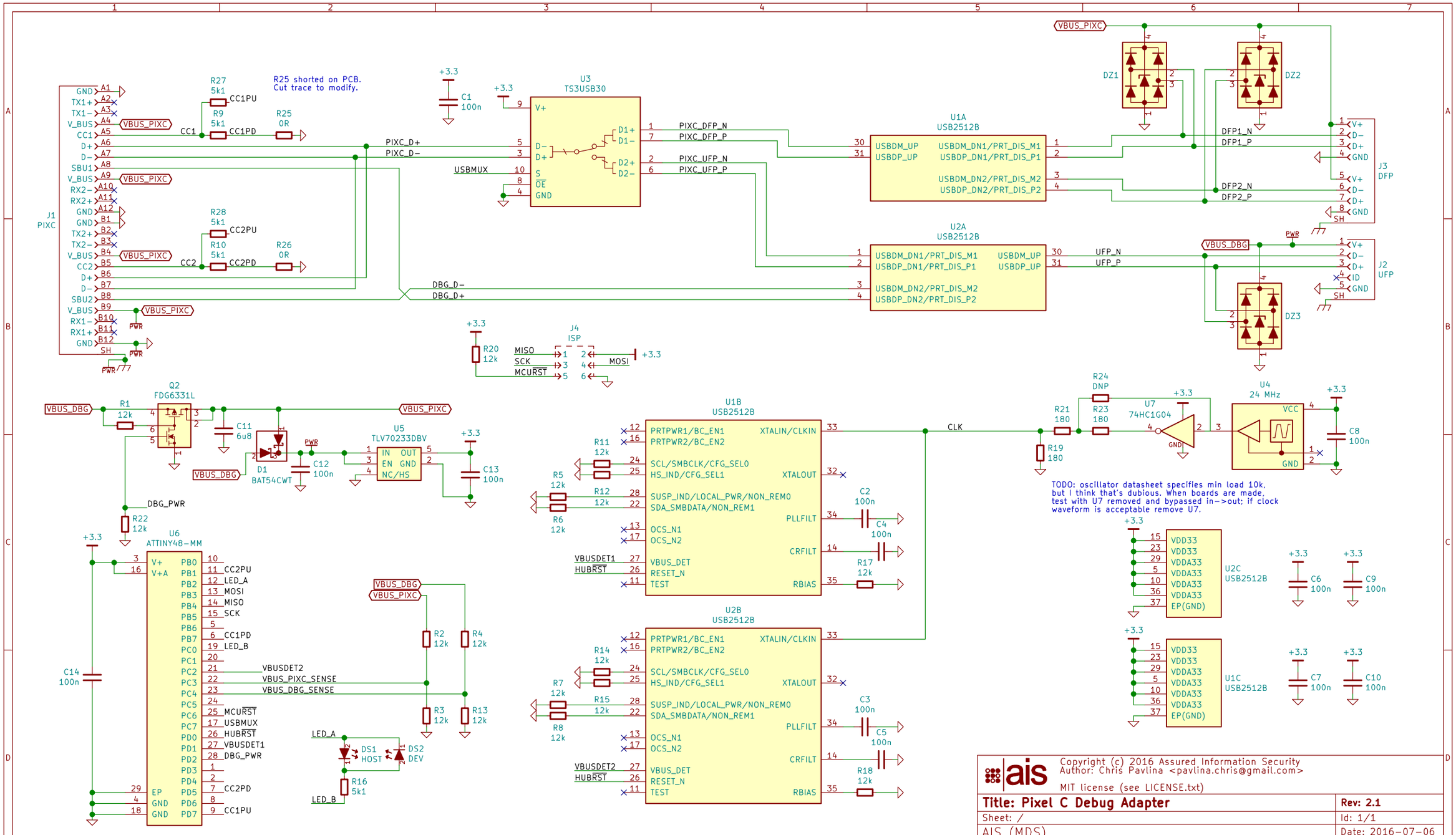
J1
PIXC
GND
TX1+
TX1−
V_BUS
CC1
D+
D−
SBU1
RX2−
RX2+
TX2+
TX2−
CC2
SBU2
RX1−
RX1+
SH
VBUS_PIXC
R27
5k1
CC1PU
R9
5k1
CC1PD
R25
0R
R25 shorted on PCB.
Cut trace to modify.
R28
5k1
CC2PU
R10
5k1
CC2PD
R26
0R
PIXC_D+
PIXC_D−
DBG_D−
DBG_D+
+3.3
C1
100n
U3
TS3USB30
V+
D−
D+
S
OE
GND
USBMUX
D1+
D1−
D2+
D2−
PIXC_DFP_N
PIXC_DFP_P
PIXC_UFP_N
PIXC_UFP_P
U1A
USB2512B
USBDM_UP
USBDP_UP
USBDM_DN1/PRT_DIS_M1
USBDP_DN1/PRT_DIS_P1
USBDM_DN2/PRT_DIS_M2
USBDP_DN2/PRT_DIS_P2
U2A
USB2512B
DZ1
DZ2
DZ3
DFP1_N
DFP1_P
DFP2_N
DFP2_P
J3
DFP
J2
UFP
VBUS_DBG
PWR
UFP_N
UFP_P
ID
J4
ISP
MISO
SCK
MCURST
MOSI
R20
12k
Q2
FDG6331L
R1
12k
C11
6u8
D1
BAT54CWT
C12
100n
U5
TLV70233DBV
IN
OUT
EN
GND
NC/HS
C13
100n
DBG_PWR
R22
12k
U6
ATTINY48−MM
V+
V+A
EP
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
LED_A
MOSI
LED_B
SCK
CC1PD
VBUSDET2
VBUS_PIXC_SENSE
VBUS_DBG_SENSE
MCURST
USBMUX
HUBRST
VBUSDET1
DBG_PWR
CC2PD
CC1PU
C14
100n
R2
12k
R4
12k
R3
12k
R13
12k
DS1
HOST
DS2
DEV
R16
5k1
U1B
USB2512B
PRTPWR1/BC_EN1
PRTPWR2/BC_EN2
SCL/SMBCLK/CFG_SEL0
HS_IND/CFG_SEL1
SUSP_IND/LOCAL_PWR/NON_REM0
SDA_SMBDATA/NON_REM1
OCS_N1
OCS_N2
VBUS_DET
RESET_N
TEST
XTALIN/CLKIN
XTALOUT
PLLFILT
CRFILT
RBIAS
R11
12k
R5
12k
R12
12k
R6
12k
C2
100n
C4
100n
R17
12k
VBUSDET1
HUBRST
U2B
USB2512B
R14
12k
R7
12k
R15
12k
R8
12k
C3
100n
C5
100n
R18
12k
VBUSDET2
CLK
R24
DNP
R21
180
R23
180
R19
180
U7
74HC1G04
GND
U4
24 MHz
VCC
C8
100n
TODO: oscillator datasheet specifies min load 10k,
but I think that's dubious. When boards are made,
test with U7 removed and bypassed in−>out; if clock
waveform is acceptable remove U7.
U2C
USB2512B
VDD33
VDDA33
EP(GND)
C6
100n
C9
100n
U1C
USB2512B
C7
100n
C10
100n
ais
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Author: Chris Pavlina <pavlina.chris@gmail.com>
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Title: Pixel C Debug Adapter
Rev: 2.1
Sheet: /
Id: 1/1
AIS (MDS)
Date: 2016−07−06