UNIT-4 BOOLEAN LOGIC

Boolean algebra is an algebra that deals with Boolean values((TRUE and FALSE) . Everyday we have to make logic decisions: “Should I carry the book or not?” , “Should I watch TV or not?” etc.

Each question will have two answers yes or no, true or false. In Boolean Algebra we use 1 for true and 0 for false which are known as truth values.

Truth table:

A truth table is composed of one column for each input variable (for example, A and B), and one final column for all of the possible results of the logical operation that the table is meant to represent (for example, A XOR B). Each row of the truth table therefore contains one possible configuration of the input variables (for instance, A = true B = false), and the result of the operation for those values.

Logical Operators:

In Algebraic function e use +,-,*,/ operator but in case of Logical Function or Compound statement we use AND,OR & NOT operator.

Example: He prefers Computer Science NOT IP.

There are three Basic Logical Operator:

1. NOT
2. OR
3. AND

- **NOT Operator**—Operates on single variable. It gives the complement value of variable.

X	$\overline{\mathbf{X}}$
0	1
1	0

- **OR Operator** -It is a binary operator and denotes logical Addition operation and is represented by ”+” symbol

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 1

X	Y	X+Y
0	0	0
0	1	1
1	0	1
1	1	1

- **AND Operator** – AND Operator performs logical multiplications and symbol is (.) dot.

0.0=0
0.1=0
1.0=0
1.1=1

Truth table:

X	Y	X.Y
0	0	0
0	1	0
1	0	0
1	1	1

Basic Logic Gates

A logic gate is an physical device implementing a Boolean function, that is, it performs a logical operation on one or more logic inputs and produces a single logic output. Gates also called logic circuits.

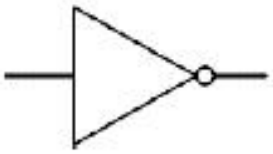
Or

A gate is simply an electronic circuit which operates on one or more signals to produce an output signal.

NOT gate (inverter): The output Q is true when the input A is NOT true, the output is the inverse of the input:

Q = NOT A

A NOT gate can only have one input. A NOT gate is also called an inverter.



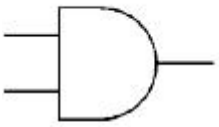
Traditional symbol

Input A	Output Q
0	1
1	0

Truth Table

AND gate

The output Q is true if input A AND input B are both true: **Q = A AND B** An AND gate can have two or more inputs, its output is true if all inputs are true.



Traditional symbol

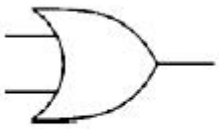
Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table

OR gate

The output Q is true if input A OR input B is true (or both of them are true): **Q = A OR B**

An OR gate can have two or more inputs, its output is true if at least one input is true.



Traditional symbol

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table

Basic postulates of Boolean Algebra:

Boolean algebra consists of fundamental laws that are based on theorem of Boolean algebra. These fundamental laws are known as basic postulates of Boolean algebra. These postulates states basic relations in boolean algebra, that follow:

I If X != 0 then x=1 and If X!=1 then x=0

II OR relations(logical addition)

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 1

III AND relations (logical multiplication)

0.0 = 0
0.1 = 0
1.0 = 0
1.1 = 1

IV Complement Rules $\bar{0} = 1, \bar{1} = 0$

Principal of Duality

This principal states that we can derive a Boolean relation from another Boolean relation by performing simple steps. The steps are:-

1. Change each AND(.) with an OR(+) sign
2. Change each OR(+) with an AND(.) sign
3. Replace each 0 with 1 and each 1 with 0

e.g

0+0=0	then dual is	1.1=1
1+0=1	then dual is	0.1=0

Basic theorem of Boolean algebra

Basic postulates of Boolean algebra are used to define basic theorems of Boolean algebra that provides all the tools necessary for manipulating Boolean expression.

1. Properties of 0 and 1
   (a) 0+X=X
   (b) 1+X=1
   (c) 0.X=0
   (d) 1.X=X
2. Indempotence Law
   (a) X+X=X
   (b) X.X=X
3. Involution Law

   $\overline{\overline{(X)}} = X$
4. Complementarity Law

   (a) $X + \bar{X}=1$

   (b) $X. \bar{X}=0$
5. Commutative Law
   (a) X+Y=Y+X
   (b) X.Y=Y.X
6. Associative Law
   (a) X+(Y+Z)=(X+Y)+Z
   (b) X(YZ)=(XY)Z
7. Distributive Law
   (a) X(Y+Z)=XY_XZ
   (b) X=YZ=(X+Y)(X+Z)
8. Absorption Law
   (a) X+XY= X
   (b) X(X+Y)=X

Some other rules of Boolean algebra

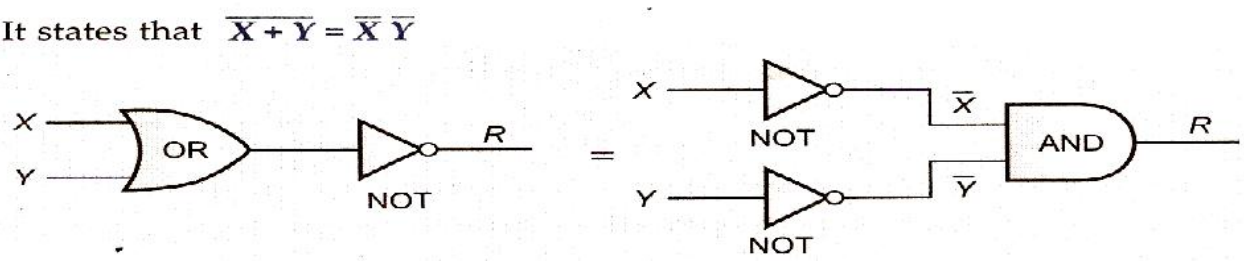
$X+\overline{X}Y=X+Y$

Demorgan's Theorem

A mathematician named DeMorgan developed a pair of important rules regarding group complementation in Boolean algebra.

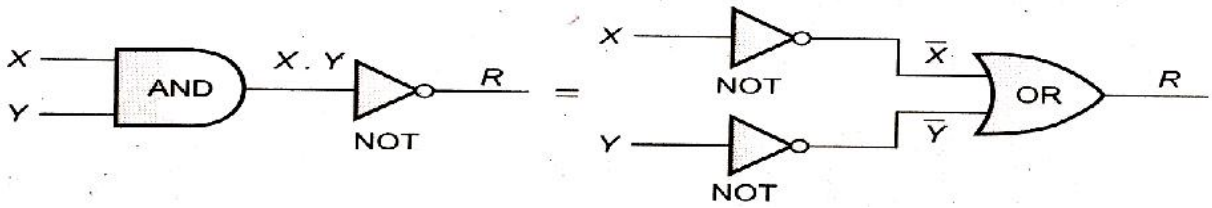
Demorgan's First Theorem

It states that $\overline{X+Y}=\overline{X}\,\overline{Y}$



Demorgan's Second Theorem

This theorem states that : $X.Y=\overline{X}+\overline{Y}$



Derivation of Boolean expression:-

Minterm :

minterm is a Product of all the literals within the logic System.

Step involved in minterm expansion of Expression

1. First convert the given expression in sum of product form.
2. In each term is any variable is missing(e.g. in the following example Y is missing in first term and X is missing in second term), multiply that term with (missing term +complement(missing term))factor e.g. if Y is missing multiply with Y+Y")
3. Expand the expression .
4. Remove all duplicate terms and we will have minterm form of an expression.

Example: Convert X + Y

X + Y = X.1 + Y.1
=X.(Y+Y") + Y(X+X")
=XY + XY"+XY+X"Y
=XY+XY"+XY

Other procedure for expansion could be

1. Write down all the terms
2. Put X"s where letters much be inserted to convert the term to a product term
3. Use all combination of X"s in each term to generate minterms
4. Drop out duplicate terms

Shorthand Minterm notation:

Since all the letters must appear in every product, a shorthand notation has been developed that saves actually writing down the letters themselves. To form this notation, following steps are to be followed:

1. First of all, Copy original terms
2. Substitute 0s for barred letters and 1s for nonbarred letters
3. Express the decimal equivalent of binary word as a subscript of m.

Rule1. Find Binary equivalent of decimal subscript e.g.,for m6 subscript is 6, binary equivalent of 6 is 110.

Rule 2. For every 1s write the variable as it is and for 0s write variables complemented form i.e., for 110 t is XYZ. XYZ is the required minterm for m6.

maxterm:

A maxterm is a sum of all the literals (with or without the bar) within the logic system. Boolean Expression composed entirely either of Minterms or Maxterms is referred to as Canonical Expression.

Canonical Form:

Canonical expression can be represented is derived from

(i) Sum-of-Products(SOP) form

(ii) Product-of-sums(POS) form

Sum of Product (SOP)

1. Various possible input values
2. The desired output values for each of the input combinations

X	Y	R
0	0	X′Y′
0	1	X′Y
1	0	XY′
1	1	XY

Product of Sum (POS)

When a Boolean expression is represented purely as product of Maxterms, it is said to be in Canonical Product-of-Sum from of expression**.**

X	Y	Z	Maxterm
0	0	0	X+Y+Z
0	0	1	X+Y+Z′
0	1	0	X+Y′+Z
0	1	1	X+Y′+Z′
1	0	0	X′+Y+Z
1	0	1	X′+Y+Z′
1	1	0	X′+Y′+Z
1	1	1	X′+Y′+Z′

Minimization of Boolean expressions:-

After obtaining SOP and POS expressions, the next step is to simplify the Boolean expression.

There are two methods of simplification of Boolean expressions.

1. **Algebraic Method**
2. **Karnaugh Map :**

1.Algebraic method: This method makes use of Boolean postulates, rules and theorems to simplify the expression.

Example No. 1: Reduce the expression $\overline{XY} + \overline{X} + XY$.

Solution. $\overline{XY} + \overline{X} + XY$

$= (\overline{X} + \overline{Y}) + \overline{X} + XY$ *(using DeMorgan's 2nd theorem i.e.,* $\overline{XY} = \overline{X} + \overline{Y}$)

$= \overline{X} + \overline{X} + \overline{Y} + XY$

$= \overline{X} + \overline{Y} + XY$ ($\because$ $\overline{X} + \overline{X} = \overline{X}$ as X + X = X)

$= \overline{X} + XY + \overline{Y}$

$= (\overline{X} + \overline{\overline{X}}Y) + \overline{Y} = (\overline{X} + XY) + \overline{Y}$ *(putting* $X = \overline{\overline{X}}$)

$= \overline{X} + Y + \overline{Y}$ $(X + \overline{X}Y = X + Y)$

$= \overline{X} + 1$ *(putting* $Y + \overline{Y} = 1$)

$= 1$ *(putting* $\overline{X} + 1 = 1$ as $1 + X = 1$)

Example No. 2: Minimise $AB + \overline{AC} + A\overline{B}C(AB + C)$.

Solution. $AB + \overline{AC} + A\overline{B}C(AB + C) = AB + \overline{AC} + A\overline{B}CAB + A\overline{B}CC$

$= AB + \overline{AC} + AAB\overline{B}C + ABCC$

$= AB + \overline{AC} + 0 + ABCC$ *(putting* $B\overline{B} = 0$)

$= AB + \overline{AC} + A\overline{B}.C$ *(putting* $C.C = C$)

$= AB + \overline{A} + \overline{C} + A\overline{B}C$ *(putting* $\overline{AC} = \overline{A} + \overline{C}$ *DeMorgan's 2nd theorem)*

$= \overline{A} + AB + \overline{C} + A\overline{B}C$ *(rearranging the terms)*

$= \overline{A} + B + C + A\overline{B}C$ *(putting* $\overline{A} + AB = A + B$ *because* $X + XY = X + Y$)

$= \overline{A} + \overline{C} + B + A\overline{B}C = \overline{A} + \overline{C} + B + \overline{B}AC$

$= \overline{A} + \overline{C} + B + AC$ *(putting* $B + \overline{B}AC = B + AC$ *because* $X + \overline{X}Y = X + Y$)

$= \overline{A} + B + \overline{C} + CA$

$= \overline{A} + B + \overline{C} + A$ ($\because$ $\overline{C} + CA = \overline{C} + A$)

$= A + \overline{A} + B + \overline{C}$

$= 1 + B + \overline{C}$ *(putting* $A + \overline{A} = 1$)

$= 1$ *(as* $1 + X = 1$ *i.e., anything added to 1 results in 1)*

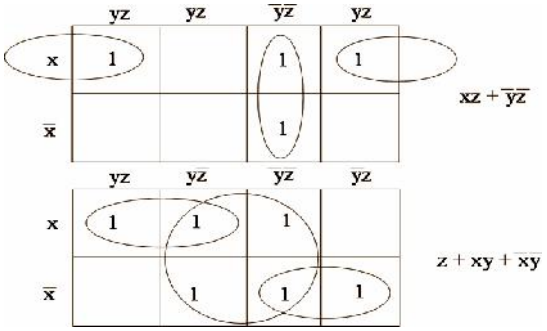
2. Using Karnaugh Map :

Karnaugh Maps:

Karnaugh map or K Map is a graphical display of the fundamental product in a truth table.

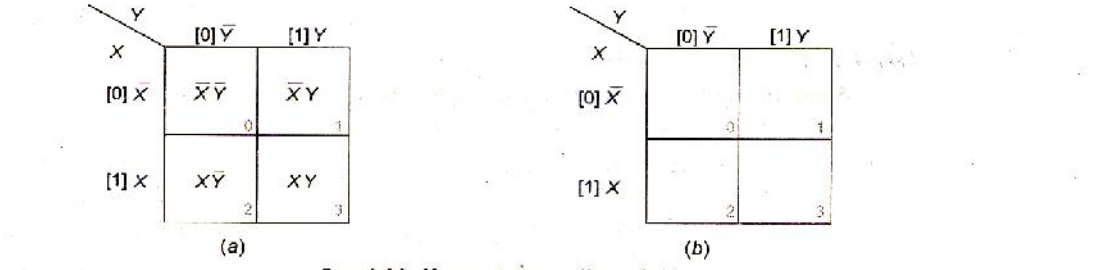
For example:

- Put a 1 in the box for any minterm that appears in the SOP expansion.
- Basic idea is to cover the **largest adjacent** blocks you can whose side length is some power of 2.
- Blocks can "wrap around" the edges.
- For example, the first K-map here represents $x\,y + x\,\overline{y} = x\,(y + \overline{y}) = x$. (since y+y'=1)
- The second K-map, similarly, shows $x\,y + \overline{x}\,y = (x + \overline{x})\,y = y$

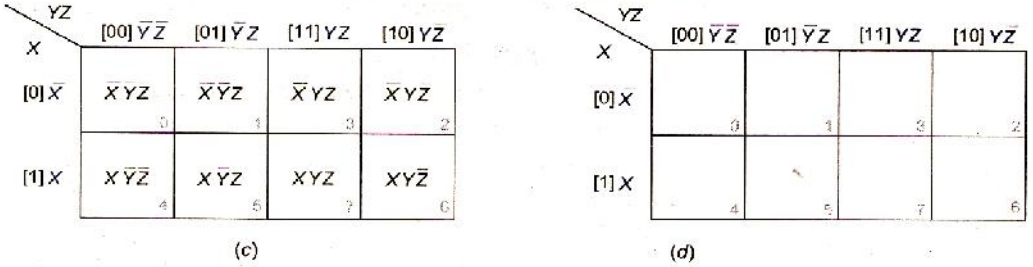


- Remember, group together adjacent cells of 1s, to form largest possible rectangles of sizes that are powers of 2. Notice that you can overlap the blocks if necessary.

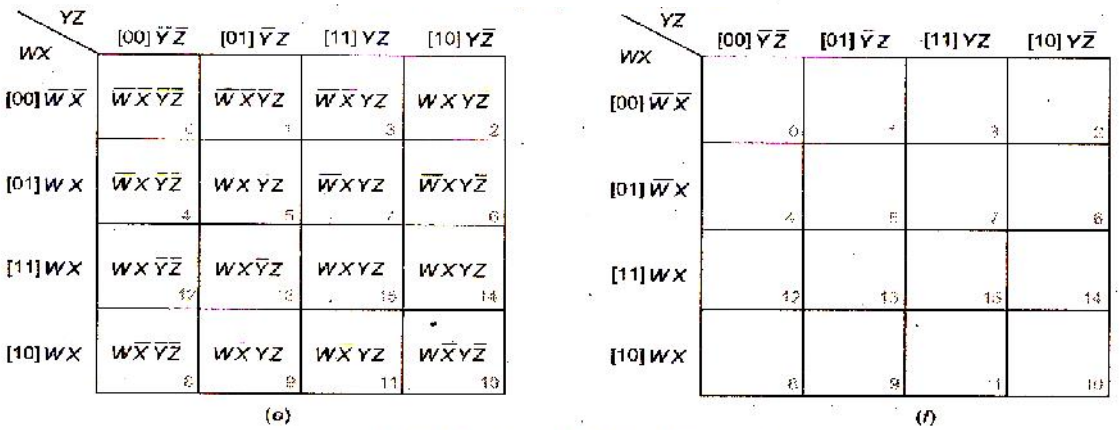
Sum Of Products Reduction using K- Map



2-variable K-map representing minterms.



3-variable K-map representing minterms



4-variable K-map representing minterms

For reducing the expression first mark Octet, Quad, Pair then single.

- Pair: Two adjacent 1's makes a pair.
- Quad: Four adjacent 1's makes a quad.
- Octet: Eight adjacent 1's makes an Octet.
- Pair removes one variable.
- Quad removes two variables.
- Octet removes three variables.

Reduction of expression: When moving vertically or horizontally in pair or a quad or an octet it can be observed that only one variable gets changed that can be eliminated directly in the expression.

For Example

In the above Ex

Step 1 : In K Map while moving from m_7 to m_{15} the variable A is changing its state Hence it can be removed directly, the solution becomes **B.CD = BCD.** This can be continued for all the pairs, Quads, and Octets.

Step 2 : In K map while moving from m_0 to m_8 and m_2 to m_{10} the variable A is changing its state. Hence **B'** can be taken similarly while moving from m_0 to m_2 and m_8 to m_{10} the variable C is changing its state. Hence **D'** can be taken; the solution becomes **B'.D'**

The solution for above expression using K map is BCD + B'D'.

Example1: Reduce the following Boolean expression using K-Map:
F(P,Q,R,S)=Σ(0,3,5,6,7,11,12,15)

	R'S'	R'S	RS	RS'
P'Q'	1 0	 1	1 3	 2
P'Q	 4	1 5	1 7	1 6
PQ	1 12	 13	1 15	 14
PQ'	 8	 9	1 11	 10

Soln:
This is 1 quad, 2pairs & 2 lock
Quad(m3+m7+m15+m11) reduces to RS
Pair(m5+m7) reduces to P‟‟QS
Pair (m7+m6) reduces to P‟‟QR
Block m0=P‟‟Q‟‟R‟‟S‟‟
M12=PQR‟‟S‟‟
hence the final expressions is F=RS + P‟‟QS + P‟‟QR + PQR‟‟S‟‟ + P‟‟Q‟‟R‟‟S‟‟

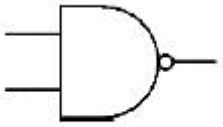
Example2: Reduce the following Boolean expression using K-Map:
F(A,B,C,D)=Π(0,1,3,5,6,7,10,14,15)

0	0	0	
	0	0	0
		0	0
			0

Soln:
Reduced expressions are as follows:
For pair 1, (A+B+C)
For pair 2, (A‟‟+C‟‟+D)
For Quad 1, (A+D‟‟)
For Quad 2, (B‟‟+C‟‟)
Hence final POS expression will be
$Y(A,B,C,D) = (A+B+C)\,(A+\overline{C}+\overline{D})\,(A+\overline{D})\,(\overline{B}+\overline{C})$

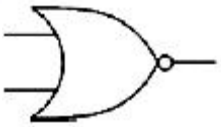
More about Gates:

NAND gate (NAND = Not AND)
This is an AND gate with the output inverted, as shown by the 'o' on the output. The output is true if input A AND input B are NOT both true: **Q = NOT (A AND B)** A NAND gate can have two or more inputs, its output is true if NOT all inputs are true.



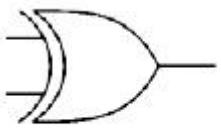
Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

NOR gate (NOR = Not OR)
This is an OR gate with the output inverted, as shown by the 'o' on the output. The output Q is true if NOT inputs A OR B are true: **Q = NOT (A OR B)** A NOR gate can have two or more inputs, its output is true if no inputs are true.



Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	0

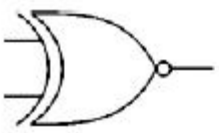
EX-OR (EXclusive-OR) gate
The output Q is true if either input A is true OR input B is true, **but not when both of them are true**: **Q = (A AND NOT B) OR (B AND NOT A)** This is like an OR gate but excluding both inputs being true. The output is true if inputs A and B are **DIFFERENT**. EX-OR gates can only have 2 inputs.



Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	0

Traditional symbol Truth Table

EX-NOR (EXclusive-NOR) gate
This is an EX-OR gate with the output inverted, as shown by the 'o' on the output. The output Q is true if inputs A and B are the **SAME** (both true or both false):



Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	1

Traditional symbol Truth Table

Q = (A AND B) OR (NOT A AND NOT B) EX-NOR gates can only have 2 inputs.

Summary truth tables

The summary truth tables below show the output states for all types of 2-input and 3-input gates.

Summary for all 2-input gates

Inputs		Output of each gate					
A	B	AND	NAND	OR	NOR	EX-OR	EX-NOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

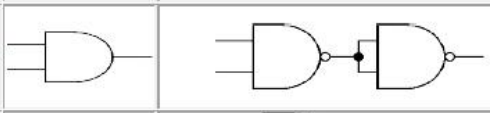
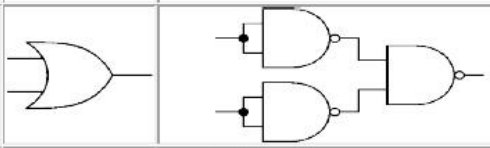
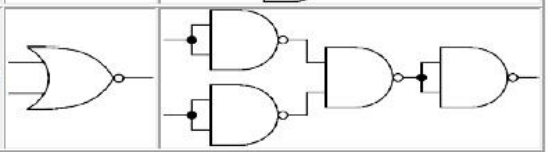
Note that EX-OR and EX-NOR gates can only have 2 inputs.

Summary for all 3-input gates

Inputs			Output of each gate			
A	B	C	AND	NAND	OR	NOR
0	0	0	0	1	0	1
0	0	1	0	1	1	0
0	1	0	0	1	1	0
0	1	1	0	1	1	0
1	0	0	0	1	1	0
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	0	1	0

NAND gate equivalents

The table below shows the NAND gate equivalents of NOT, AND, OR and NOR gates:

Gate	Equivalent in NAND gates
NOT	
AND	
OR	
NOR	

Low Order Thinking Questions: (Boolean Algebra)

a) State and verify absorption law in Boolean algebra.

Ans. Absorption Law states that :

a) X+XY=X b) X(X+Y)=X

b) Verify X'.Y+X.Y'=(X'+Y').(X+Y) algebraically.

Ans. LHS= X'Y + XY'

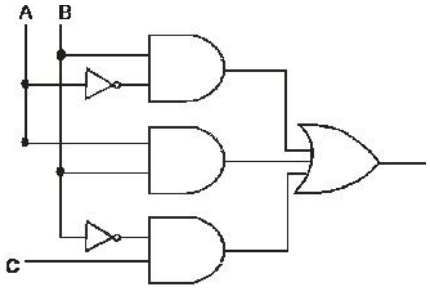
= (X'+X) (X'+Y') (Y+X) (Y+Y')

= 1.(X'+Y') (X+Y).1

= (X'+Y') (X+Y)

= RHS, hence proved

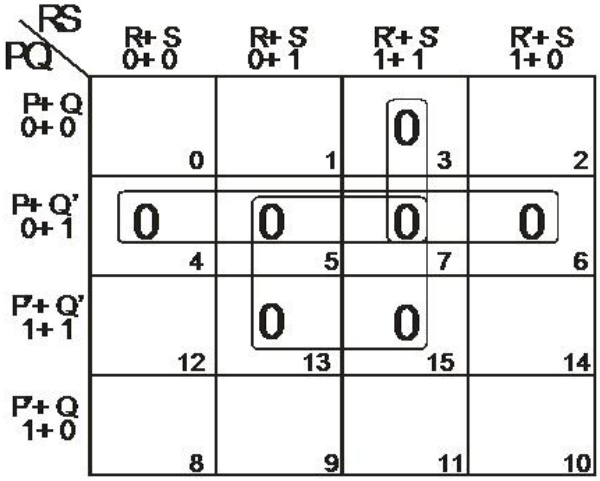
c) Write the equivalent Boolean Expression F for the following circuit diagram :



Ans.: A'B+AB+B'C

d) If F(P,Q,R,S) = ∏ (3,4,5,6,7,13,15) , obtain the simplified form using K-Map.

Ans.:



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Reduction of groups following the reduction rule :

Quad1 = M4.M5.M6.M7

= P+Q'

Quad2 = M5.M7.M13.M15

= Q'+S'

Pair = M3.M7

= P+R'+S'

Therefore POS of F(P,Q,R,S) = (P+Q')(Q'+S')(P+R'+S')

e) F(a,b,c,d)=Σ(0,2,4,5,7,8,10,12,13,15)

F(a,b,c,d)=B1+B2+B3

B1=m0+m4+m12+m8==c'd'

B2=m5+m7+m13+m15=bd

B3=m0+m2+m8+m10=b'd'

F(a,b,c,d)=c'd'+bd+b'd'

f) Write the equivalent Boolean expression for the following logic circuit:

X	Y	Z	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

- Express in the product of sums form, the Boolean function F(X,Y,Z), the truth table for which is given below:

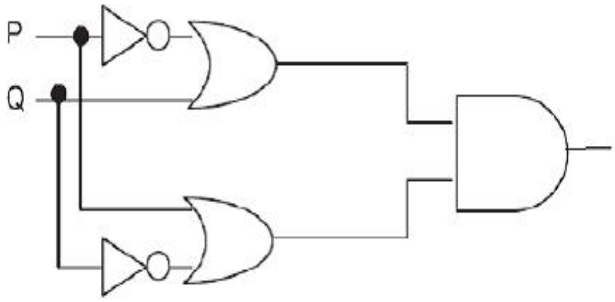
1/2 Marks Practice Questions:

1.State and Prove DeMorgan Law using Truth Table

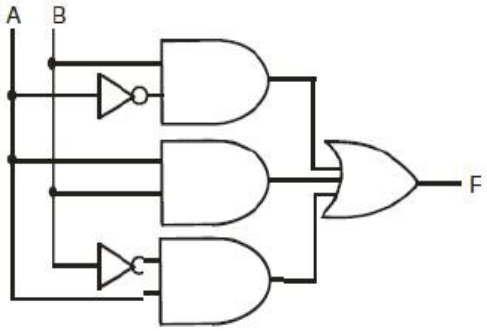
2. State and prove Absorption Law algebraically.

3. State and Prove Distributive Law algebraically.

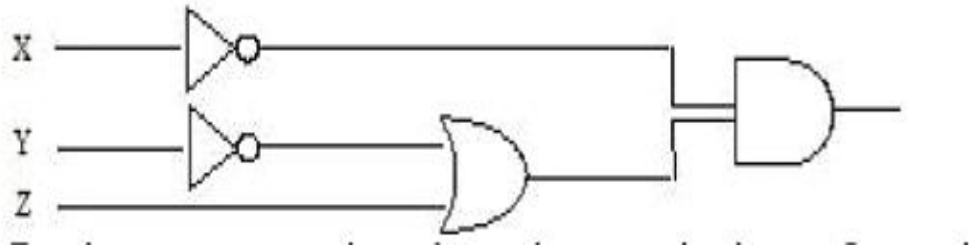
4. Write the equivalent Boolean Expression for the following Logic Circuit 2



5. Write the equivalent Boolean Expression F for the following circuit diagram : 2



6 Write the equivalent Boolean Expression F for the following circuit diagram : 2



7. Convert the following Boolean expression into its equivalent Canonical Sum of Product Form((SOP)

(X'+Y+Z').(X'+Y+Z).(X'+Y'+Z).(X'+Y'+Z') 1

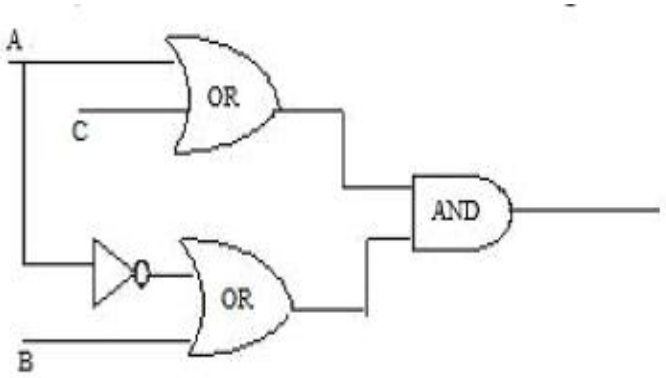
8. Convert the following Boolean expression into its equivalent Canonical Product of Sum form (POS):

A.B'.C + A'.B.C +A'.B.C' 1

9. Draw a Logical Circuit Diagram for the following Boolean expression:

A.(B+C') 2

10. Write the equivalent Boolean Expression F for the following circuit diagram: 2



11. Prove that XY+YZ+YZ'=Y algebraically 2

12. Design (A+B).(C+D) using NOR Gate. 2

3 Marks Practice Questions

13. If F(a,b,c,d)=Σ(0,2,4,5,7,8,10,12,13,15), obtain the simplified form using K-Map.

14. If F(a,b,c,d) =Σ(0,3,4,5,7,8,9,11,12,13,15), obtain the simplified form using KMap

15 Obtain a simplified form for a boolean expression

F(U,V,W,Z)= π (0,1,3,5,6,7,10,14,15)

16 . Reduce the following boolean expression using K-Map

F(A,B,C,D) = Σ(5,6,7,8,9,12,13,14,15)