

ECE 350

Laboratory Project Manual for

Real-Time Operating Systems

Keil MCB1700 Edition

by

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Preface

Who Should Read This Lab Manual?

This lab manual is written for students who will design and implement a small Real-Time Executive (RTX) for Keil MCB1700 board populated with an NXP LPC1768 microcontroller.

What is in This Lab Manual?

The first purpose of this document is to provide the descriptions and notes for the laboratory project. The second purpose of this document is a quick reference guide of the relevant development tools for completing laboratory projects. This manual is divided into three parts.

Part I describes the lab administration policies.

Part II is the project description. We break the project into the following four laboratory projects.

- P1: Memory Management
- P2: Task Management
- P3: Inter-task Communications and Console I/O
- P4: Real-Time Scheduling

Part III introduces the computing environment and the development tools. It includes a Keil MCB 1700 hardware and software reference guide. The topics are as follows.

- Keil MCB1700 Hardware Environment
- Keil Software Development Tools
- Programming MCB1700

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- ARM University Program for providing us with lab teaching materials and ARM DS gold edition software licenses.
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- TerasIC, the manufacturer, for shipping the boards in a timely manner.
- Imperas Software for providing us one evaluation license to experiment with their software tools during the lab development.

We gratefully thank our graduate teaching assistants: Zehan Gao, Ali H. A. Abyaneh, Weitian Xing, and Maizi Liao for their help in developing important parts of the lab and the lab manual. Our gratitude also goes out to Eric Praetzel for his continuous strong support of the IT infrastructure of RTOS lab hardware and the ARM DS software, Rasoul Keshavarzi-Valdani for lending us a DE1-SoC board to experiment with during the initial board selection phase of the lab development. Kim Pope and Reinier Torres Labrada both provided helpful FPGA tips and we gratefully acknowledge their expertise and help.

Finally we owe many thanks to our students who did ECE354, SE350 and ECE350 course projects in the past and provided constructive feedback. The lab projects won't exist without our students.

Part I

Lab Administration

Lab Administration Policy

Group Lab Policy

- **Group Size.** All labs are done in groups of *four*. When the class size cannot be evenly divided by four, a couple of groups can have size three. The project deliverables are the same for all groups regardless of group size.
- **Group Sign-up.** Use [LEARN](#) to self-enroll in a group. Late group sign-up is not accepted and will result in losing the entire lab sign-up mark. (See Table 0.1). Grace days do not apply to Group Sign-up. Any student without a lab group after the deadline will be randomly assigned to a lab group. This random assignment will first consider smaller size groups. We encourage students in the same lab section to form groups. If you have a hard time to find a group in your lab section, we allow cross-lab section groups provided that this won't cause any timing conflict with other courses.
- **Leave a Group.** Please choose your lab partners carefully and wisely and work together to prevent group breakup. Leaving a group should be used as the last resort to resolve group dynamic issues. You are allowed to join a new group, but not allowed to quit from the new group again. The code and documentation completed before the group split-up are the intellectual property of each students in the old group.

To quit a group, you need to notify the lab instructor in writing and sign the group split-up form (see the Appendix [B](#)) at least one week before the nearest lab project deadline.

Project Submission Policy.

- **Project Submissions.** The lab project is divided into four deliverables and the submission is on GitLab. Each submission has a required git tag name. Table 0.1 gives the submission commit tag names, weights, deadlines.
- **Late Submissions** Late submission is accepted within three days after the deadline. Please be advised that late submission is counted in a unit of day rather than hour or minute. An hour late submission is one day late, so does a fifteen

Deliverable	Tag Name	Weight	Due Date
P0 Group Sign-up		2%	23:00 May 10
P1 Memory Management	p1-submit	18%	23:00 May 24
P2 Task Management	p2-submit	30%	23:00 Jun 07
P3 Inter-task Communications and Console I/O	p3-submit	25%	23:00 Jul 01
P4 Real-Time Scheduling	p4-submit	25%	23:00 Jul 19

Table 0.1: Project Deliverable Tag Names, Weights and Deadlines. P0 is submitted to a dropbox on LEARN.

hour late submission. The number of days you are late is computed by the following function of the hours your are late.

```
#include <math.h>

int get_late_days(double late_hours) {
    return (int) (ceil(late_hours/24));
}
```

There are *three grace days*¹ that can be used for late submissions without incurring any penalty. When you use up all your grace days, a 15% per day late penalty will be applied to a late submission. *Submission is not accepted if it is more than three days late.*

Project Grading Policy

- **Project Grading Procedure.** The first three projects are graded by automated testing framework. The last project is graded by demonstration and automated testing framework. For each deliverable, we publish a small set of testing cases. We require students to pass these testing cases before they submit. If you are not able to pass these testing cases, then your project will be graded manually by spot checking the source code, which usually will result in a very undesirable lab grade.
- **Hardware vs. Simulator.** Submission will be evaluated by executing the code on the board. A 15% penalty will be applied to a submission that can only execute on the simulator, but not on the board.
- **Project Re-grading.** Lab grades are usually released before next scheduled lab session starts. Re-grading usually requires students to come to one of the

¹Grace days are calendar days. Days in weekends are counted.

lab help sessions to speak to the grading TA. Re-grading requests need to be directly submitted through LEARN re-grading request dropboxes within two calendar days after the lab grade is released. You will need to write a detailed appeal document to support your request. Acceptable regrading request reasons are:

- There is a data entry error of your lab grades on LEARN.
- You find a grading mistake. For example a bug in the unseen test code used in the demo.
- You find the grading is unfair.

Name the regrading request document as G<gid>-P<pid>-regrade.pdf, where gid is your group id and pid is the project id of 1, 2, 3 or 4. For example, G99-P2-regrade.pdf is the regrading request file submitted by Group 99 to appeal P2 grade. Please do not email us your regrading request. Dropbox submissions will help everyone to keep good track of all regrading requests. Your entire project will be re-evaluated and the chance that the new lab grade may be lower than your original lab grade exists.

- **Individual Lab Grade.** Normally everyone in the same group gets the same lab grade, which is the group project grade. If your group has serious workload distribution issue, you should submit the peer review form (available on LEARN) to the dropbox on Learn and notify the lab instructor by email to initiate a peer review process. Each group member will rate how satisfied he/she is with every other group member's contribution from 0 to 10, where the higher the rating, the more satisfied the student feels about the contribution the other member has done for the project. This is to review each group member's contribution to the project. We will use simple arithmetic average ratings each group member received and assign individual lab grade to each team member by multiplying the group project grade with a contribution percentage factor listed in Table 0.2.

Peer Rating	Contribution Factor CF
[7, 10]	100%
[6, 7)	80%
[5, 6)	60%
[4, 5)	40%
[0, 4)	0%

Table 0.2: Group Project contribution factor table. Each student's lab grade is their group project grade multiplied by the CF (Contribution Factor). This scheme only applies to groups who need peer reviews.

Note peer review only applies to those groups that have group dynamic issues

that need to be escalated. Majority of groups work well and do not participate peer review.

Lab Repeating Policy

For a student who repeats the course, labs need to be re-done with new lab partners. Simply turning in the old lab code is not allowed. We understand that the student may choose a similar route to the solution chosen last time the course was taken. However it should not be identical. The labs will be done a second time, we expect that the student will improve the older solutions. Also the new lab partners should be contributing equally, which will also lead to differences in the solutions.

Note that the policy is course specific to the discretion of the course instructor and the lab instructor.

Lab Projects Solution Internet Policy

Publishing your lab projects solution source code or lab report on the internet for public to access is a violation of academic integrity. Because this potentially enabling other groups to cheat the system in the current and future offerings of the course. For example, it is not acceptable to host a public repository on GitHub that contains your lab project solutions. A lab grade zero will automatically be assigned to the offender.

Seeking Help

- **Lab Help Sessions.** There are eight lab help sessions in the week before the lab is due. Coming to these sessions are the most effective way for you to get hands-on help from lab staff. Lab staff give students who are enrolled in the lab session the priority of service. Should lab staff have free cycles, they will serve students who come to an unenrolled lab session.
- **Discussion Forum.** We recommend students to use the Piazza discussion forum to ask the teaching team questions instead of sending individual emails. For questions related to lab projects, our target response time is *one m business day* before the lab deadline ². Questions asked in the weekend will be answered on the next business day. *There is no guarantee on the response time to questions of a lab after its deadline.*

²Our past experiences show that the number of questions spike when deadline is close. The teaching staff will not be able to guarantee one business day response time when workload is above average, though we always try our best to provide timely response.

- **Drop-in Office Hours.** There will be drop-in lab office hours before the due dates for P3 and P4. See LEARN calendar for exact time and location.
- **Appointments.** Students can arrange appointments with lab teaching staff by email. To make the appointment efficient and effective, when requesting an appointment, please specify three preferred times and roughly how long the appointment needs to be. On average, an appointment is fifteen minutes per project group. Please also summarize the main questions to be asked in your appointment requesting email.

Important Note

Teaching staff are not permitted to give direct solution to a lab assignment. Teaching staff will not debug student's program for the student. Debugging is a non-trivial part of the exercise of finishing a programming assignment. Teaching staff will be able to demonstrate how to use the debugger and provide case specific debugging tips. Guidance and hints will be provided to help students to find the solution by themselves.

Lab Facility After Hour Access Policy

After hour access to the lab will be given to the class. Please be advised that the after hour access is a privilege. Students are required to keep the lab equipment and furniture in good conditions to maintain this privilege.

No food or drink is allowed in the lab. Please be informed that you share the lab with other classes. When resources become too tight, certain cooperation is required such as taking turns to use the stations in the lab.

Part II

Lab Project

Chapter 1

Introduction

1.1 Overview

In this project, you will design a small real-time executive (RTX) and implement it on a Keil MCB1700 board populated with an NXP LPC1768 microcontroller . The executive will provide a basic multiprogramming environment, with different priority levels, preemption, dynamic memory management, mailbox for inter-task communications and synchronization, system console I/O and debugging support, and finally real-time scheduling.

Such an RTX is suitable for embedded computers which operate in real time. A cooperative, non-malicious software environment is assumed. The design of the RTX should allow its placement in ROM. Applications and non-kernel RTX tasks must execute at the unprivileged level of LPC1768. The RTX kernel will execute at the privileged level. There are two banks of 32K of RAM for use by the RTX and application tasks. The microcontroller has four timers, four UARTs and several other peripheral interface devices. The board has two RS-232 interfaces, from which UART0 is used for your RTX system console and UART1 is used for your RTX debug terminal.

1.2 Summary of RTX Requirements

The RTX requirements are listed as follows:

Memory Management

Binary buddy system dynamic memory allocation is supported. Refer to Chapter 3 for details.

Task Management

The maximum number of tasks that can run is decided at compile time. The RTX supports task creation and deletion during run time. The RTX supports task pre-emption. There are four user priority levels plus an additional “hidden” priority level for the Null task. There is no time slicing. FIFO (First In, First Out) scheduling policy at each priority level is supported. Refer to Chapter [4](#) for details.

Synchronization and Console I/O

The RTX provides mailbox utility for inter-task communication and synchronization. An interrupt-driven UART provides the console service. Refer to Chapter [5](#) for details.

Real-Time Scheduling

The Earliest Deadline First (EDF) scheduling policy is supported. Refer to Chapter [6](#) for details.

1.2.1 RTX Tasks

You are required to implement two types of tasks by using the RTX primitives and services. They are user tasks and system tasks.

User Tasks

These tasks are operating at the unprivileged level in thread mode. They are user applications that perform certain user defined functions. For each lab project, you will implement test tasks to help you test the RTX primitives and services you have designed and implemented. In later labs, you will add tasks that require console I/O services once you have the console I/O service ready.

System Tasks

These tasks are operating in thread mode. Some may require a privileged level of operation and some may be sufficient to operate at a unprivileged level. It is your design decision to justify which task will be operating at what privilege level. Three system tasks are required and they are null task (see Chapter [3](#)), console display task and keyboard command decoder task (see Chapter [5](#)).

1.2.2 RTX Footprint and Processor Loading

A reasonably *lean* implementation is expected. **No standard C library function call is allowed in the kernel code.** An implementation of simplified C library function of `printf` is provided in the starter code.

1.2.3 Error Detection and Recovery

The primitive will return a non-zero integer value upon an error and set the `errno` accordingly. No error recovery is required. It may be assumed that the application processes can deal with this situation.

Chapter 2

Lab0 Group Sign-up and Introduction to Keil MDK5

2.1 Objective

This lab is to get you prepared for the lab project development. After this lab, students will be able to

- find a lab project group on LEARN
- use Keil uVision (Integrated Development Environment) to edit, debug, simulate and execute a bare-metal uVision project written in C and assembly;

2.2 Starter Files

The starter file is on GitHub at <http://github.com/yqh/ece350/>. It contains the following files:

- manual_code/util/printf_uart: the printf source code and the uart polling source code. The printf outputs to the UART1 by polling.
- manual_code/util/debug_script: RAM.ini that initializes debugger to load code for in-memory execution; and the SIM.ini that maps the second bank of memory region on the board for the simulator to have read and write access.
- manual_code/lab0>HelloWorld/: a bare-metal project that outputs strings to UART0 and UART1 by polling. This is the solution of Task #3 of lab tasks for self-checking purpose.

2.3 Pre-Lab

Read Part I, Chapters 1 and 7.

2.4 Lab Tasks

2.4.1 Task #1: Group Signup

Enroll yourself to a lab project group on Learn. One of your group members should submit the Group Sign-up Form (see Appendix B) by the deadline (see Table 0.1). This task will be graded.

2.4.2 Task #2: Install Keil MDK 5

This task will not be graded and is optional. Most students find having a local installation of the development tool on their own computers helps a lot. See LEARN for a quick installation demo video.

2.4.3 Task #3: Create a Hello World Application

This task will not be graded. But you need to do it to prepare yourself for future labs. Follow the steps in Sections 7.1 - 7.8. Create a HelloWorld application for NXP LPC1768 microcontroller using MDK5 uVision. Create two different targets:

- A SIM target that can be debugged on the simulator; and
- A RAM target that uses the debugger to load the image to RAM and executes on the physical hardware.

Perform the following experiments:

- Build the SIM target and execute it on the simulator by using the debugger.
- Build the RAM target and load it to RAM to execute it on the board by using the hardware debugger.
- Download the SIM target to ROM and execute it on the board without using any debugger.

2.4.4 Task #4: Create an Application Linked with a Library

This task will not be graded. But you need to do it to prepare yourself for future labs.

- Create a software library (see Section [7.9](#)).
- Create an application that links with a Library (See Section [7.10](#)).
- Create a multi-project workspace (see Sections [7.11 - 7.13](#)).
- Execute the RTX-App project on the simulator and on the board.

2.5 Deliverable

There are two items in the deliverable and they are the following:

1. Enroll yourself to a project group on LEARN.
2. Sign and submit the ECE350 Group Sign-up Declaration Form (see Appendix [B](#)) to P0 Dropbox on LEARN. Note this is a group submission. Only one of the group members submits it.

Chapter 3

Lab1

To be released by May 11, 2022.

Chapter 4

Lab2

To be released by May 25, 2022.

Chapter 5

Lab3

To be released by June 8, 2022.

Chapter 6

Lab4

To be released by June 29, 2022.

Part III

Computing Environment and Development Tools Quick Reference Guide

Chapter 7

Keil Software Development Tools

The Keil MDK-ARM development tools are used for MCB1700 boards in our lab. The tools include

- uVision5 IDE which combines the project manager, source code editor and program debugger into one environment;
- ARM compiler, assembler, linker and utilities;
- ULINK USB-JTAG Adapter which allows you to debug the embedded programs running on the board.

The MDK-Lite is the evaluation version and does not require a license. It has a code size limit of 32KB, which is adequate for the lab projects. The MDK-Lite version 5 is installed on all lab computers. If you want to install the software on your own computer. MDK 5.35 installation files are on LEARN. The URL to download the latest version is <https://www2.keil.com/mdk5/editions/lite>.

7.1 Getting Started with uVision5 IDE

To get started with the Keil IDE, the Getting Started with MDK Guide at https://www.keil.com/support/man/docs/mdk_gs/ is a good place to start. We will walk you through the IDE by developing a simple HelloWorld application which displays Hello World through the UART0 and UART1 that are connected to the lab PC. Note the HelloWorld example uses polling on both UART0 and UART1 rather than interrupt.

7.2 Getting Starter Code from the GitHub

The ECE 350 lab starter github is at <https://github.com/yqh/ece350>. Let's first make a clone of this repository by using the following command:

```
git clone https://github.com/yqh/ece350.git
```

7.3 Start the Keil uVision5 IDE

The Keil uVision5 IDE shortcut should be accessible from the start menu on school computers. If not, then navigate to C:\Software\Keil_v5\UV4 folder and double click the UV4.exe to bring up the IDE (see Figure 7.1).

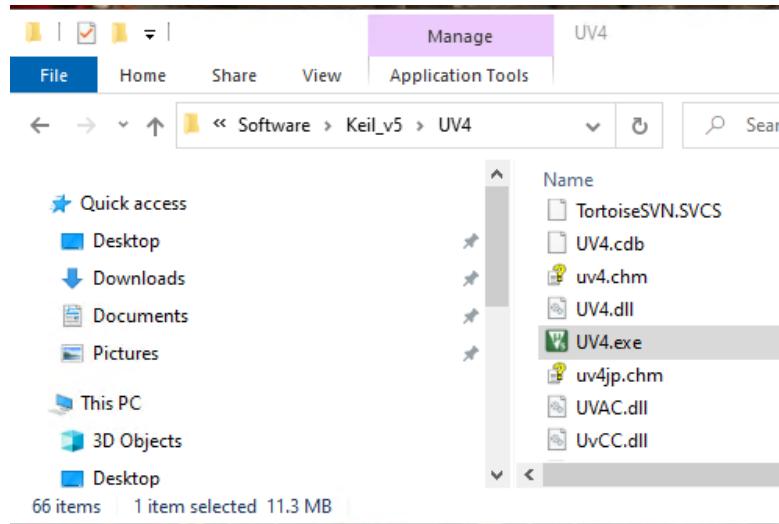


Figure 7.1: Keil IDE: Create a New Project

7.4 Create a New uVision5 Project

1. Create a directory named “HelloWorld” on your computer. The folder path name should not contain spaces on Nexus computers.
2. Create a sub-directory “src” under the “HelloWorld” directory. This sub-folder is where we want to put our source code of the project.
3. Copy the following files to “src” folder:
 - manual_code/util/printf_uart/uart_def.h
 - manual_code/util/printf_uart/uart_polling.h
 - manual_code/util/printf_uart/uart_polling.c
4. Create a new uVision project.
Open the file explorer and navigate to C:\Software\Keil_v5\UV4. Double click the UV4.exe program to start the IDE.

- Click Project → New uVision Project (See Figure 7.2).

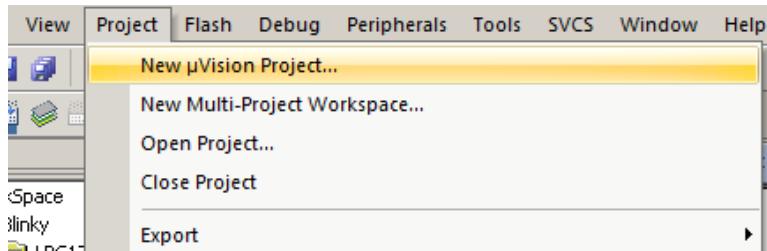


Figure 7.2: Keil IDE: Create a New Project

- Select NXP → LPC1700 Series → LPC176x → LPC1768 (See Figure 7.3).

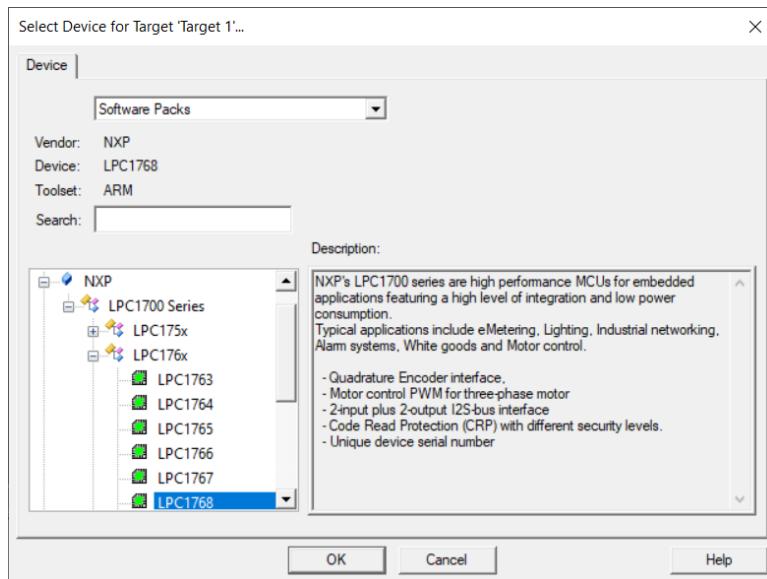


Figure 7.3: Keil IDE: Choose MCU

- Select CMSIS → CORE and Device → Startup (See Figure 7.4).

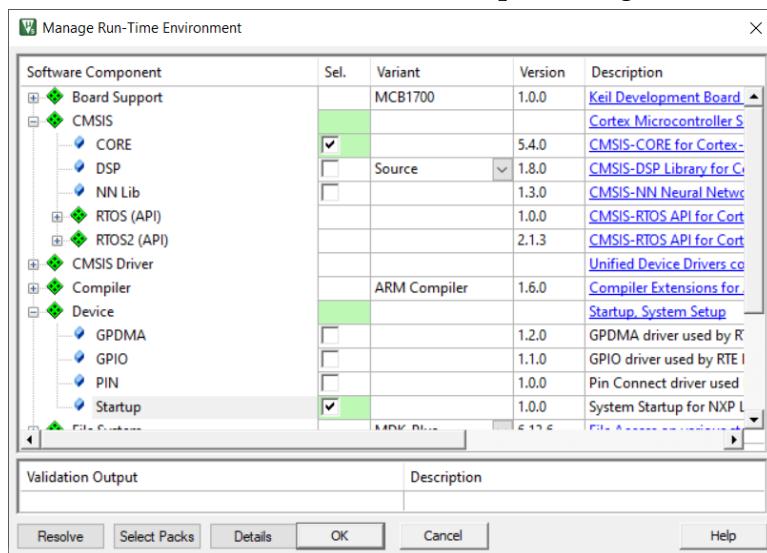


Figure 7.4: Keil IDE: Manage Run-time Environment

7.5 Managing Project Components

You just finished creating a new project. On the left side of the IDE is the Project window. Expand all objects. You will see the default project setup as shown in Figure 7.5.

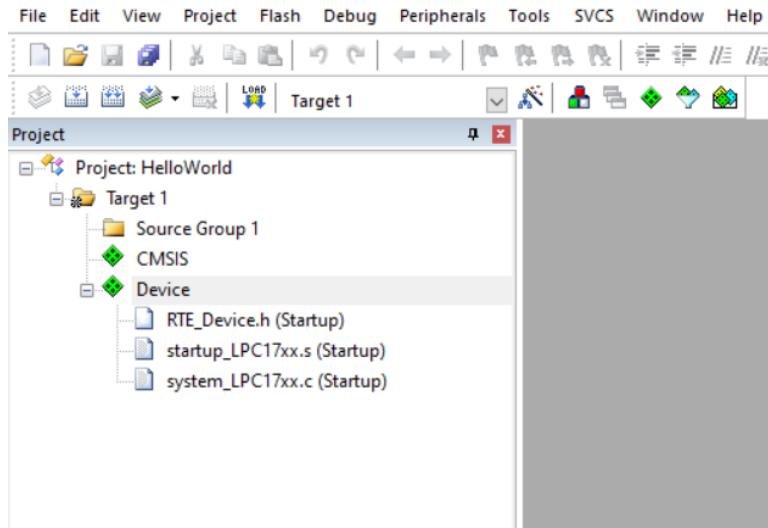


Figure 7.5: Keil IDE: A default new project

1. Rename the Target

The “Target 1” is the default name of the project build target and you can rename it. Select the target name to highlight it and then long press the left button of the mouse to make the target name editable. Input a new target name, say “HelloWorld SIM”.

2. Rename the Source Group

The IDE allows you to group source files to different groups to better manage the source code. By default “Source Group 1” is created and it contains no file. Let’s rename the source group to “System Code”¹.

3. Add a New Source Group

We can also add new source group in our project. Select the HelloWorld SIM item and right click to bring up the context window and select “Add Group...” (See Figure 7.6).

¹To rename a source group, select the source group to highlight it and long press the left mouse button to make the name editable.

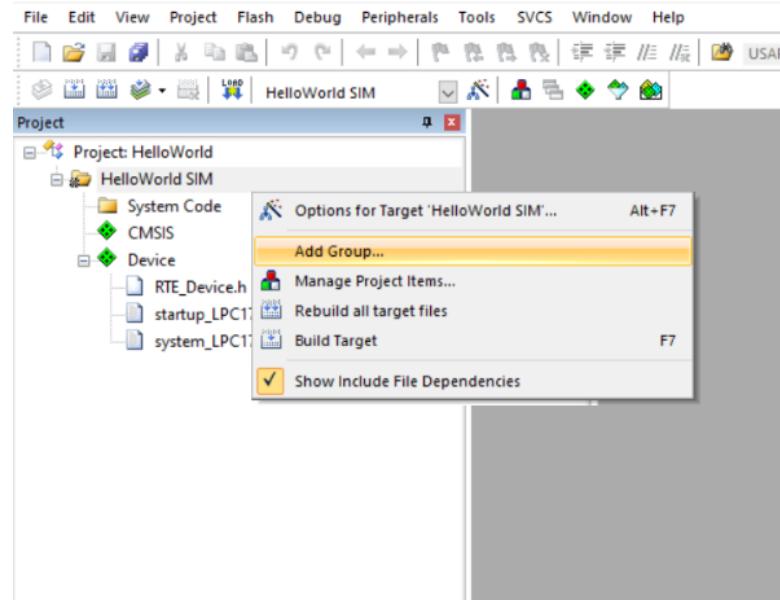


Figure 7.6: Keil IDE: Add Group

A new source group named “New Group” is added to the project. Let’s rename it to “User Code”. Your project will now look like Figure 7.7.

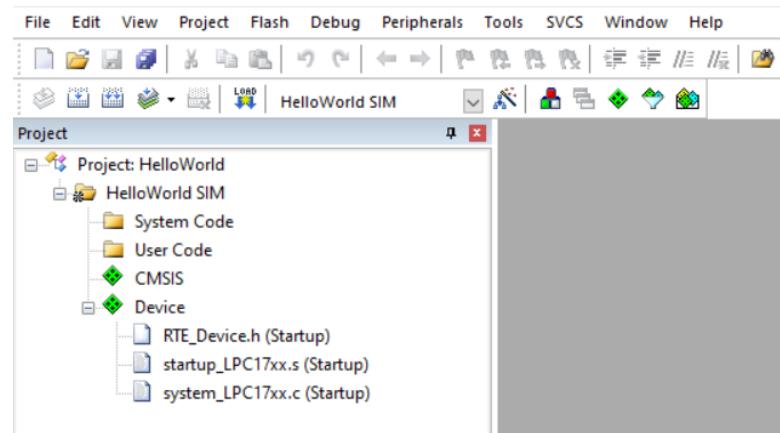


Figure 7.7: Keil IDE: Updated Project Profile

4. Add Source Code to a Source Group

Let’s add `uart_polling.c` to “System Code” group by double clicking the source group and choose the file from the file window. Double clicking the file name will add the file to the source group. Or you can select the file and click the “Add” button at the lower right corner of the window (See Figure 7.8).

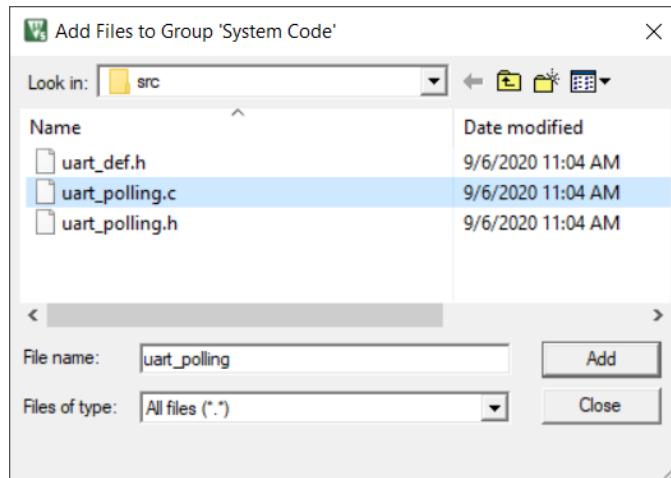


Figure 7.8: Keil IDE: Add Source File to Source Group
Your project will now look like Figure 7.9.

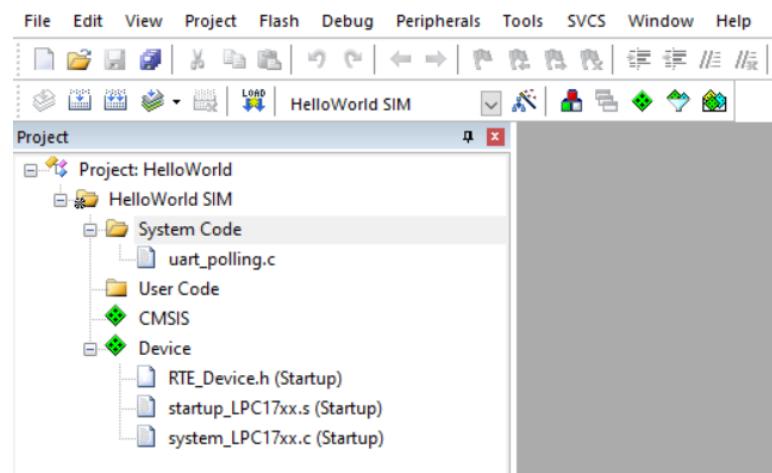


Figure 7.9: Keil IDE: Updated Project Profile

5. Create a new source file

The project does not have a main function yet. We now create a new file by selecting File → New (See Figure 7.10).

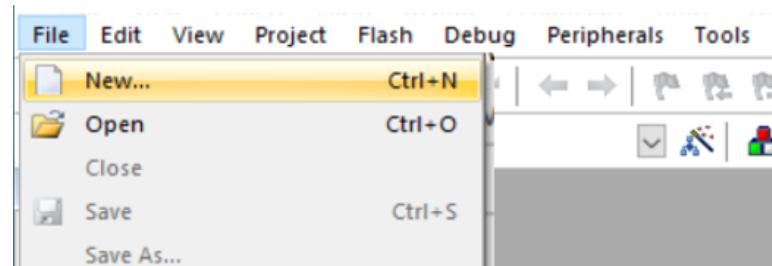


Figure 7.10: Keil IDE: Create New File

Before typing anything to the file, save the file and name it “main.c”.

Add main.c to the “Source Code” group. Type the source code as shown in Figure 7.11. Your final project would look like the screen shot in Figure 7.11.

```
#include <LPC17xx.h>
#include "uart_def.h"
#include "uart_polling.h"

int main() {
    SystemInit();
    uart0_init();
    uart1_init();
    uart0_put_string("UART0 - Howdy!\r\n");
    uart1_put_string("UART1 - Hello World!\r\n");
    return 0;
}
```

Figure 7.11: Keil IDE: Final Project Setting

7.6 Build the Project Target

To build a target, the main work is to configure the target options.

7.6.1 Configure Target Options

Most of the default settings of the target options are good. There are a few options that we need to modify.

1. Bring up the target option configuration window by pressing the target options button (See Figure 7.12).

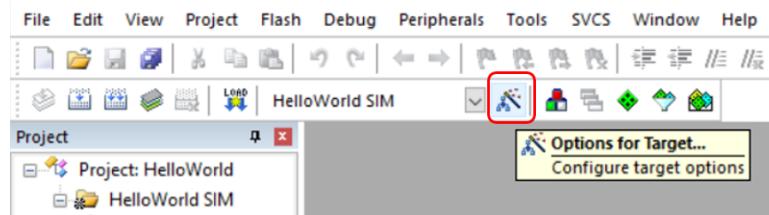


Figure 7.12: Keil IDE: Target Options Configuration

2. Configure the Target tab as shown in Figure 7.13. We want to use the version 5 arm compiler. If you see the default compiler version is 6, then change it to 5. We also want remove the IRAM2 from the default setting.

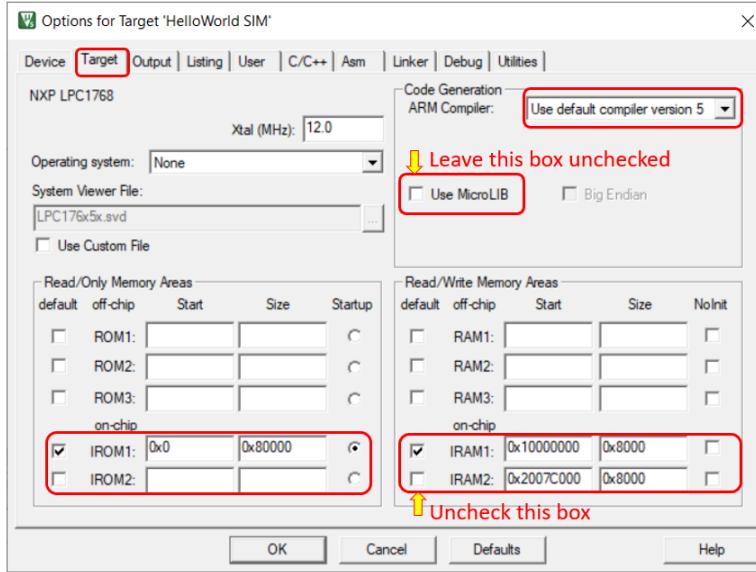


Figure 7.13: Keil IDE: Target Options Target Tab Configuration

3. Configure the C/C++ tab as shown in Figure 7.14. To enable c99, we need to check the C99 Mode box. We also want to keep the default optimization level of zero.

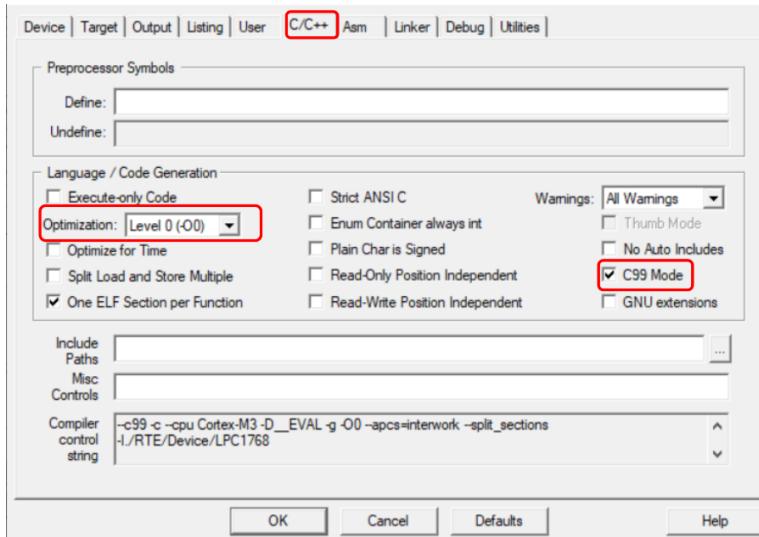


Figure 7.14: Keil IDE: Target Options C/C++ Tab Configuration

4. Configure the Linker tab as shown in Figure 7.15. This is to instruct the linker to use the memory layout from the Target tab setting instead of the default memory layout.

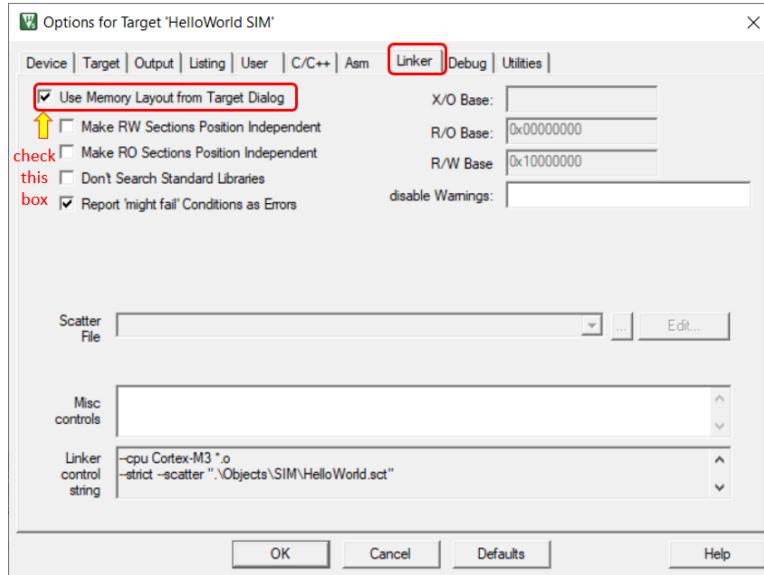


Figure 7.15: Keil IDE: Target Options Linker Tab Configuration

- Configure the Output tab so that the created executable will be put into a sub-folder of .\Objects\SIM. Note, when you press the Select Folder for Objects button (see Figure 7.16), the default directory to put the target is the .\Objects folder. You create SIM sub-folder under the default .\Objects folder and select the SIM sub-folder.



Figure 7.16: Keil IDE: Target Options Output Tab Configuration for SIM Target

- Press the “OK” button to finish the target option configuration.

7.6.2 Build the Target

To build the target, click the “Build” button (see Figure 7.17).

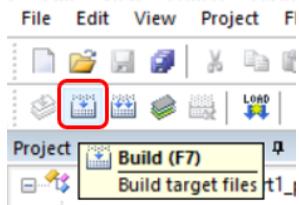


Figure 7.17: Keil IDE: Build Target

If nothing goes wrong, the build output window at the bottom of the IDE will show a log similar like the one shown in Figure 7.18.

```

Build Output
*** Using Compiler 'V5.06 (build 20)', folder: 'C:\Software\Keil_v5\ARM\ARMCC\Bin'
Build target 'HelloWorld SIM'
assembling startup_LPC17xx.s...
compiling system_LPC17xx.c...
compiling main.c...
compiling uart_polling.c...
linking...
Program Size: Code=924 RO-data=220 RW-data=0 ZI-data=608
".\Objects\SIM\HelloWorld.axf" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:02

```

Figure 7.18: Keil IDE: Build Target

7.7 Debug the Target

In theory, you may now load the target by pressing the LOAD button. However please *pause* before you attempt to do it. Our final goal is to build a project that is ready to be released and then load it to the on-chip flash to ship it to the customer. However we will need to do lots of debugging before we reach this goal. Keep flashing the board will greatly shorten the life of the on-chip memory since there is a limited number of times one can flash it. So for development purpose, developers rarely press the LOAD button in the IDE to load the image to the flash memory since each load action writes to the flash memory cells. Most of the time we use the simulator to debug and execute our project. We will also show you a commonly used technique to load the target to RAM, which has a lot longer life span than flash memory, and debug the target on the board by using the ULINK-ME hardware debugger in Section 7.7.2.

7.7.1 Debug the Project on Simulator

We will configure our project to use the simulator as the debugger.

1. Open up the target option window and select “Use Simulator” in the Debug tab and set the Dialog DLL and Parameters as shown Figure 7.19. The debug script `SIM.ini` provided in the starter code (see Listing A.1 in Appendix A) is needed to map the second bank of RAM area read and write accessible on the simulator.

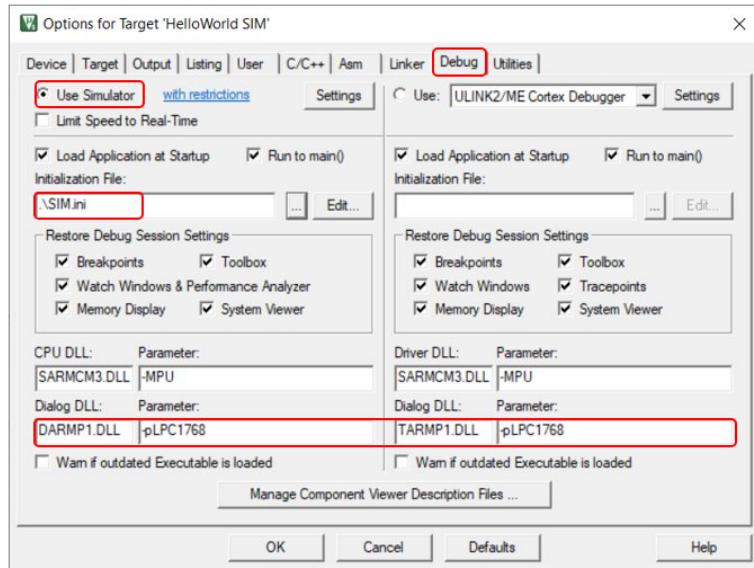


Figure 7.19: Keil IDE: Target Options Debug Tab Configuration

2. Press the “debug” button to bring up the debugger interface (See Figure 7.20).



Figure 7.20: Keil IDE: Debug Button

3. Select UART1 and UART2 (see Figure 7.21) from the serial window drop down list so that they appear on simulator (see Figure 7.22). Note that the hardware UART index starts from 0 and the simulator UART index starts from 1. So the UART1 window on simulator is for the UART0 on the board. The UART2 window on simulator is for the UART1 on the board.

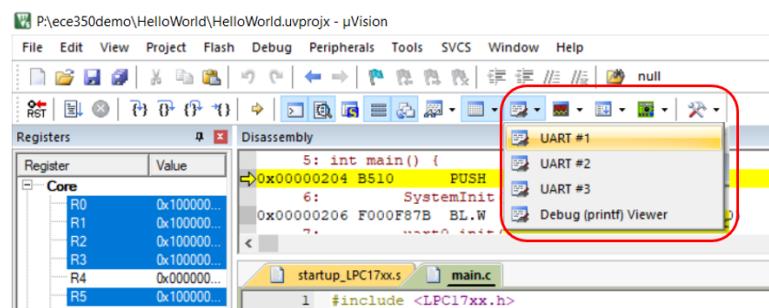


Figure 7.21: Keil IDE: Debugging. Enable Serial Window View.

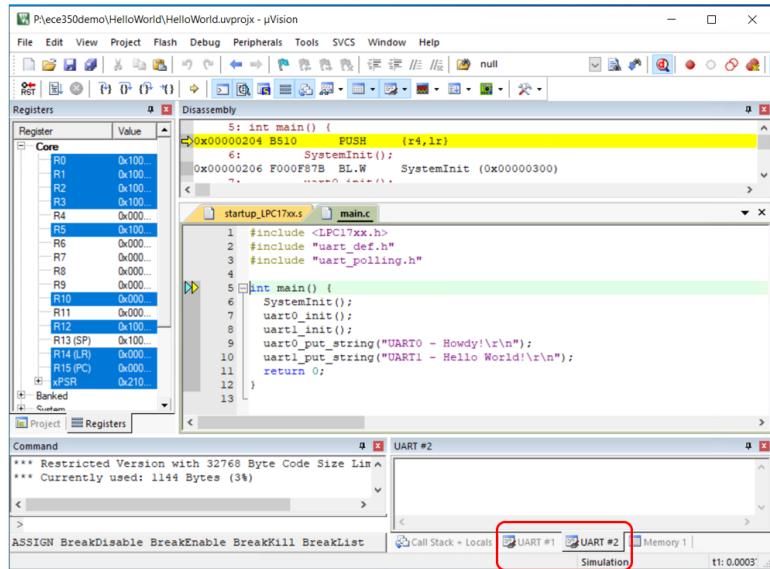


Figure 7.22: Keil IDE: Debugging. Both UART0 and UART1 views are enabled on simulator.

4. Press the “Run” button on the menu to let the program execute (see Figure 7.23). You will see the output of UART0 appearing in UART1 simulator window and the output of UART1 appearing in UART2 simulator window (see Figure 7.24). Note that we moved the UART windows from their default positions on the simulator for better view.

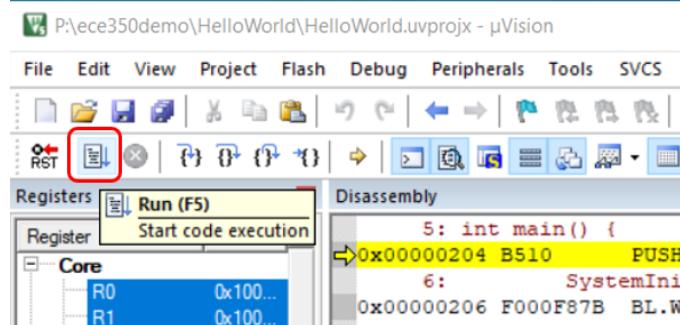


Figure 7.23: Keil IDE: Debugging. The Run Button.

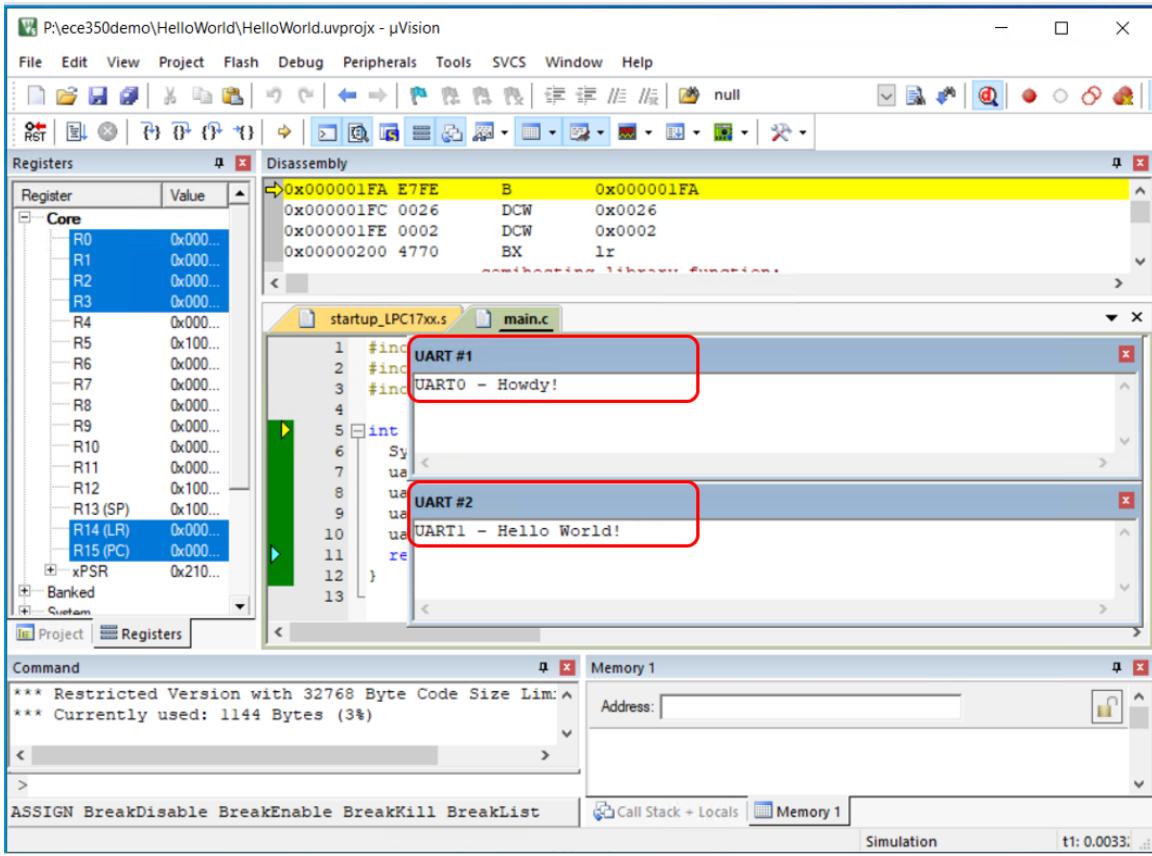


Figure 7.24: Keil IDE: Debugging Output.

- To exit the debugging session, press the “debug” button again (see Figure 7.20).

7.7.2 Debug the Project on the Board by In-Memory Execution

When debugging the code on the board, we use the ULINK-ME Cortex Debugger. The code will execute on the board. You will find creating a separate hardware debug target makes the development process easier.

- Press the Managing Project Item button (see Figure 7.25).

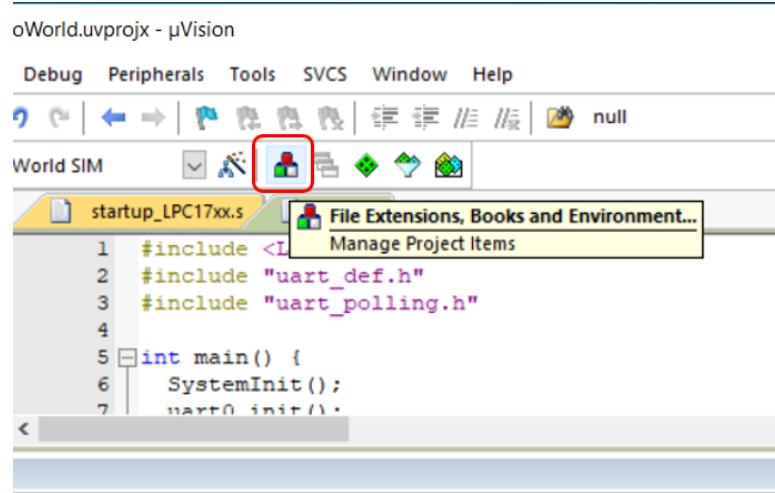


Figure 7.25: Keil IDE: Manage Project Items Button

2. Press the New icon to create a new target and name it “HelloWorld RAM”(see Figure 7.26). The new target duplicates the HelloWorld SIM target configuration.

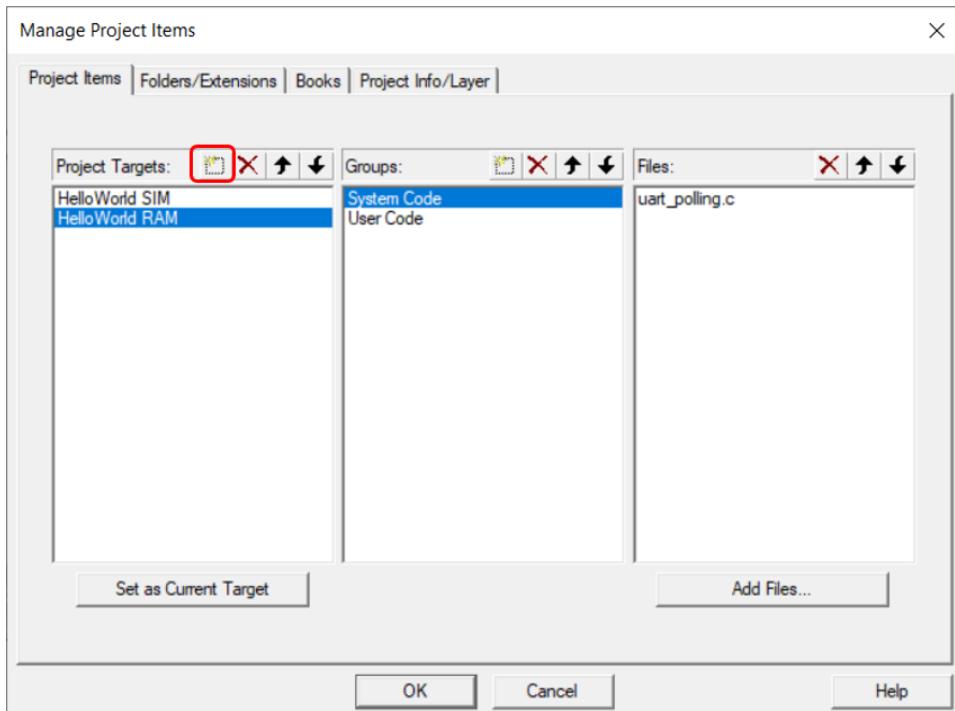


Figure 7.26: Keil IDE: Manage Project Items Window.

3. Switch your target to the newly created RAM target (See Figure 7.27).

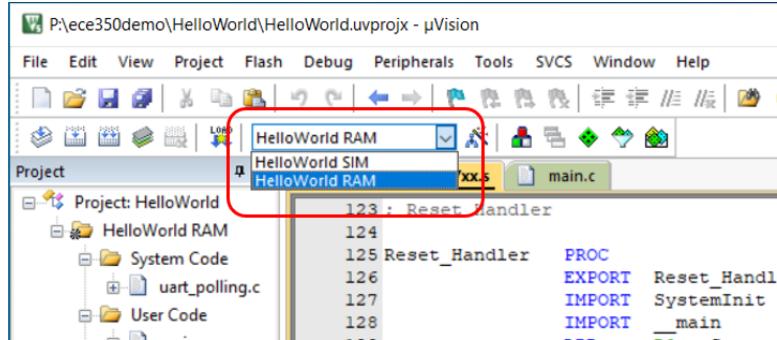


Figure 7.27: Keil IDE: Select HelloWorld RAM Target. Configure in-memory code execution as shown in Figure 7.28.

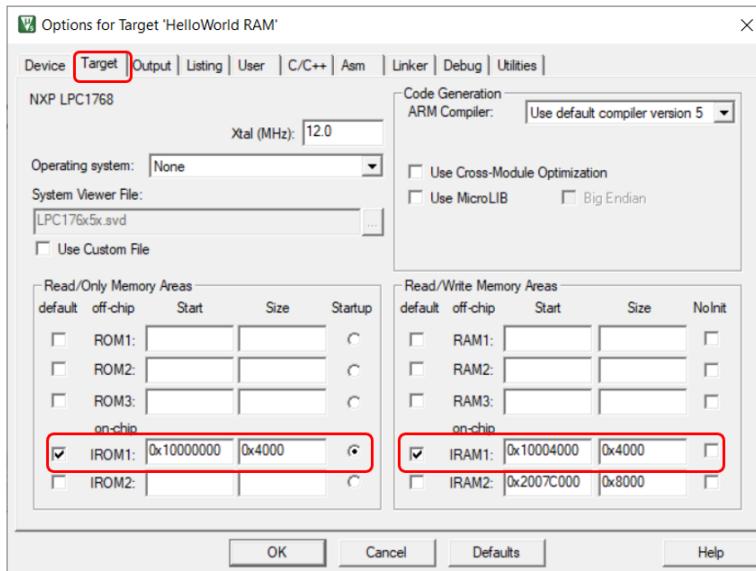


Figure 7.28: Keil IDE: Configure Target Options Target Tab for In-memory Execution.

The default image memory map setting is that the code is executed from the ROM (see Figure 7.13). Since the ROM portion of the code needs to be flashed in order to be executed on the board, this incurs wear-and-tear on the on-chip flash of the LPC1768. Since most attempts to write a functioning RTX will eventually require some more or less elaborate debugging, the flash memory might wear out quickly. Unlike the flash memory stick file systems where the wear is aimed to be uniformly distributed across the memory portion, this flash memory will get used over and over again in the same portion.

The ARM compiler can be configured to have a different starting address. The configuration in Figure 7.28 makes code starting address in RAM.

4. Select the Asm tab and input NO_CRP in the Conditional Assembly Control Symbols section as shown in Figure 7.29.

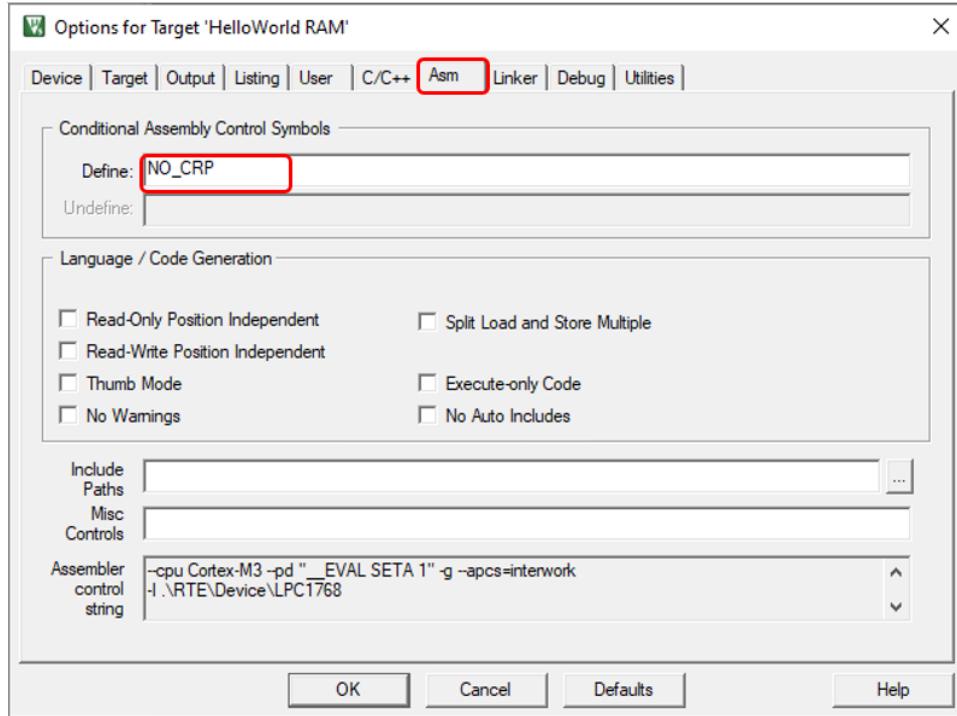


Figure 7.29: Keil IDE: RAM Target Asm Configuration.

5. Select the ULINK2/ME Cortex Debugger in the target options Debug tab and use an debug script RAM.ini provided in the starter code (See Figure 7.30) as a initialization file. An initialization file RAM.ini (see Listing A.2 in Appendix A) is needed to do the proper setting of SP, PC and vector table offset register.

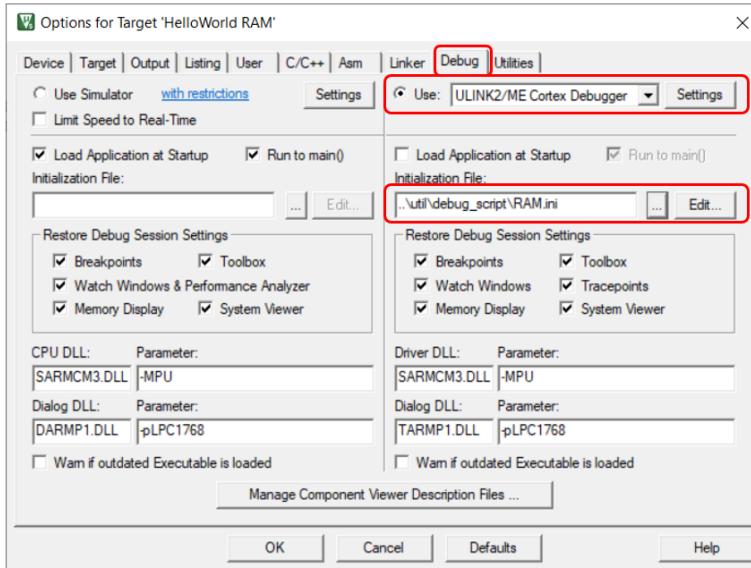


Figure 7.30: Keil IDE: Configure ULINK-ME Hardware Debugger.

6. Press the settings button beside the ULINK2/ME Cortex Debugger (see Figure 7.30) and select the Flash Download tab (see Figure 7.31). Remove the LPC17xx

IAP 512kB Flash algorithm to the Programming Algorithm field if it is there.

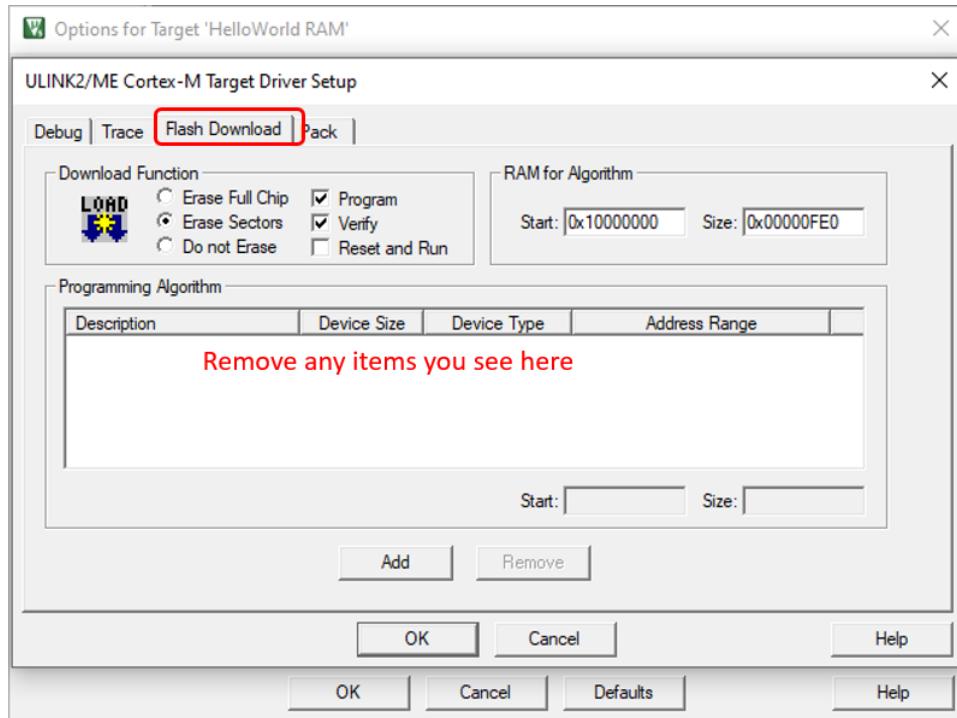


Figure 7.31: Keil IDE: Flash Download Programming Algorithm Configuration.

7. Select the Utilities tab and select the radio button beside “Use External Tool for Flash Programming” (see Figure 7.32).

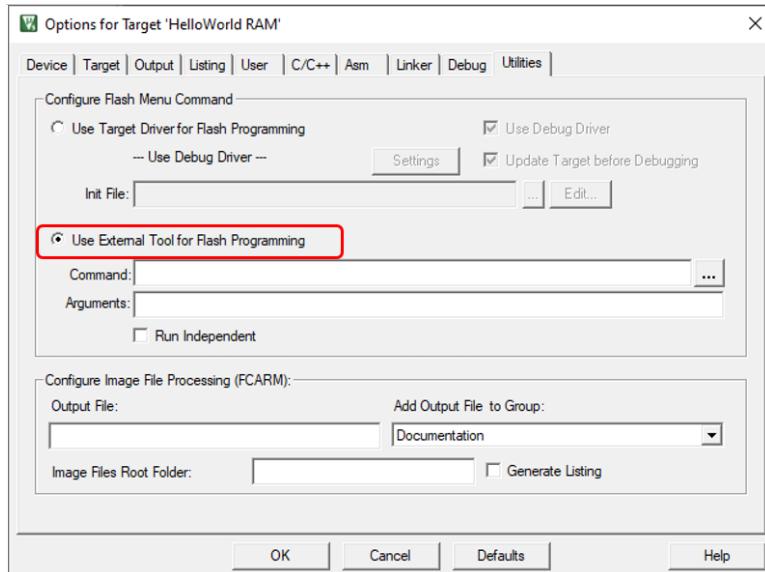


Figure 7.32: Keil IDE: Target Option Utilities Configuration for RAM Target.

8. Configure the Output tab so that the created executable will be put into a sub-folder of .\Objects\RAM (see Figure 7.33).

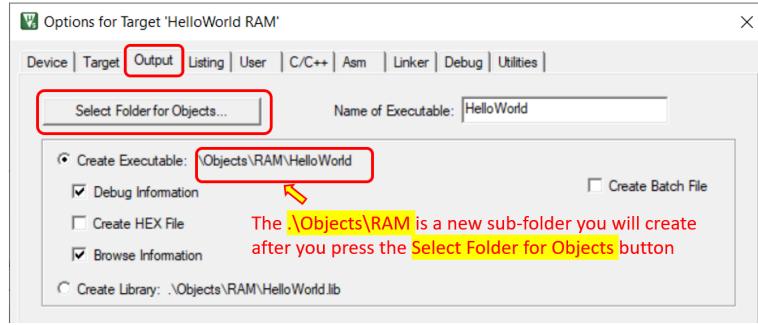


Figure 7.33: Keil IDE: Target Options Output Tab Configuration for RAM Target

9. Press the “OK” button to finish the target option configuration.
10. Build the RAM target by pressing the “Build” button (see Figure 7.17).
11. Open the PuTTY terminals to see the output. You will need a terminal emulator such as PuTTY that talks directly to COM ports in order to see output of the serial port. To find out the two COM ports, open up the device manager and expand the Ports (COM & LPT) line (see Figure 7.34).

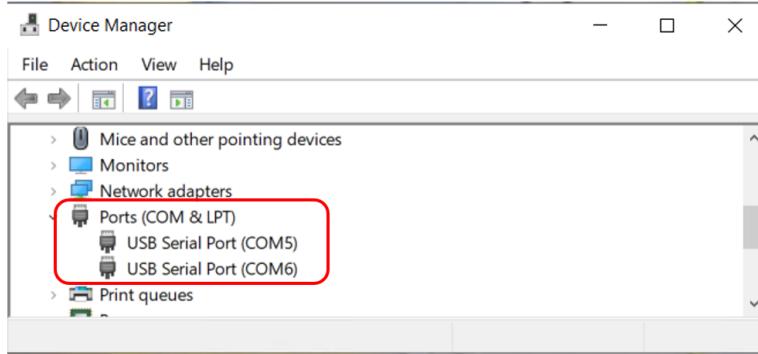


Figure 7.34: Device Manager COM Ports

Note the COM port numbers are different for each lab computer. The COM port numbers may also change after a reboot of the computer. An example PuTTY Serial configuration is shown in Figures 7.35 and 7.36.

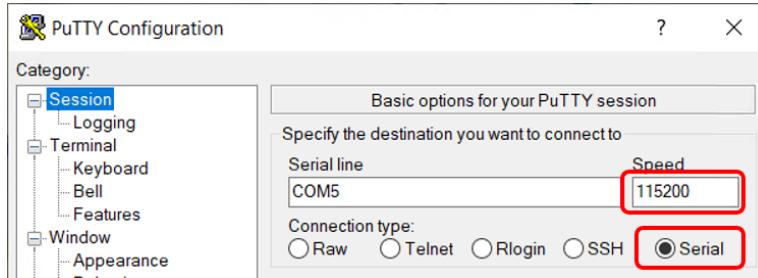


Figure 7.35: PuTTY Session for Serial Port Communication

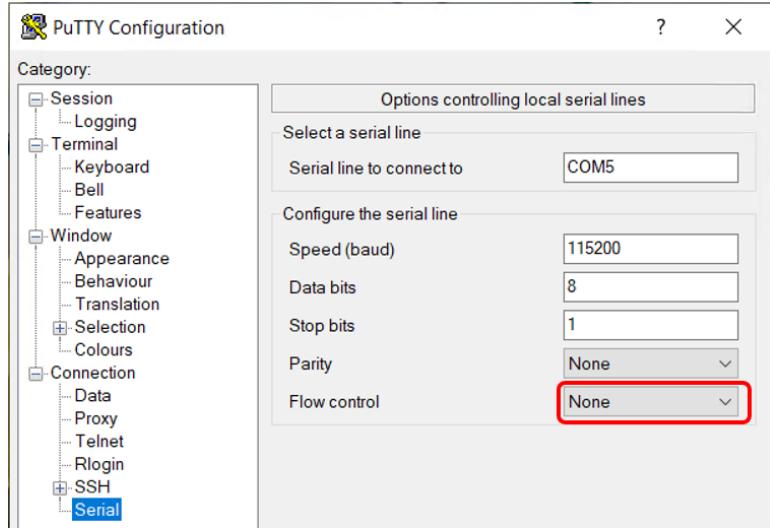


Figure 7.36: PuTTY Serial Port Configuration

12. To download the code to the board, *do not press the LOAD button*. Instead, the *debug button* is pressed to initiate a debug session and the RAM.ini file will load the code to the board.
13. Either step through the code or just press the Run button to execute the code till the end. You will see output from your PuTTY terminals (see Figure 7.37).



Figure 7.37: PuTTY Output

7.8 Download to ROM

Though we keep discouraging you to download the image to ROM, we walk you through the steps on how to do it to give you a feel of how a project that is ready to be released is loaded to the ROM. We expect that you already fixed your code by debugging the code on board by using the in-memory execution technique we showed you earlier. You should only do the following experiment once or twice. Please use the ROM sparingly.

Switch your target to the “HelloWorld SIM” target (see Figure 7.39). Open up the target option. Select the Debug tab and press the “Settings” button beside the ULINK2/ME Debugger (upper right portion of the window). Select the “Flash Download” tab and check the box “Reset and Run” in the Download Function section (See

Figure 7.38). This will execute the code automatically without the need to press the physical reset button on the board. Add the LPC17xx IAP 512kB Flash algorithm to the Programming Algorithm field if it is not already there. Apply all the changes and close the target options configuration window.

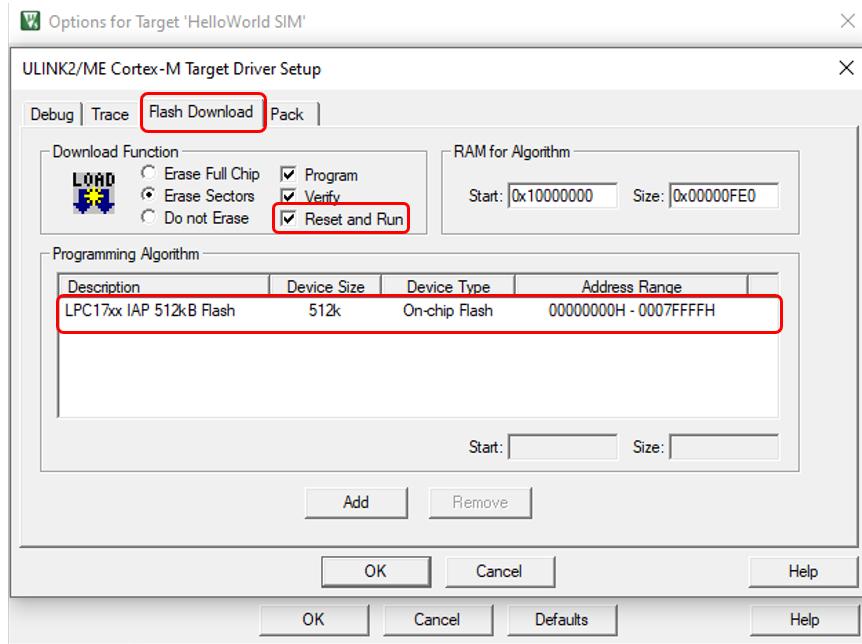


Figure 7.38: Flash Download Reset and Run Setting

To download the code to the on-chip ROM, click the “LOAD” button (see Figure 7.39). The download is through the ULINK-ME. The code automatically runs. You should see the output from PuTTY terminals.

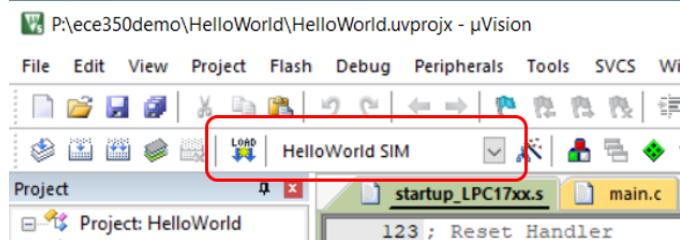


Figure 7.39: Keil IDE: Download Target to Flash

7.9 Create a Library Project

The uart polling code is not as convenient to use as the printf. We will show you how to build a simplified printf library so that printf will use the uart polling code to output to the UART #1 of the board. Note this printf is simplified version of the libc printf. It has small code size, hence has limited functionalities. But it is good enough for us to use to develop the lab project. Note the library does not execute by itself. It needs to be linked with an application project. We will show you how to do this in

7.9.1 Preparing Directory Structure

- Create a new folder and name it HelloWorld-Multi.
- Copy the entire HelloWorld application folder you created in previous steps to HelloWorld-Multi.
- Create RTX-Lib sub-folder inside HelloWorld-Multi folder.
 - Create src sub-folder inside the RTX-Lib.
 - Create bsp and libu sub-folders inside RTX-Lib\src folder.
 - Copy uart_polling.c into the bsp sub-folder.
 - Copy printf.c into the libu sub-folder (see Figure 7.40).
- Create include sub-folder inside HelloWorld-Multi folder.
 - Copy printf.h to include folder.
 - Create a bsp sub-folder inside include folder.
 - Create a sub-folder LPC1768 inside include\bsp folder.
 - Copy the following files to the include folder.
 - Copy the uart*.h files to LPC1768 folder.

Your directory structure should look like what is shown in Figure 7.40. Note we omitted the directory layout of the HelloWorld folder.

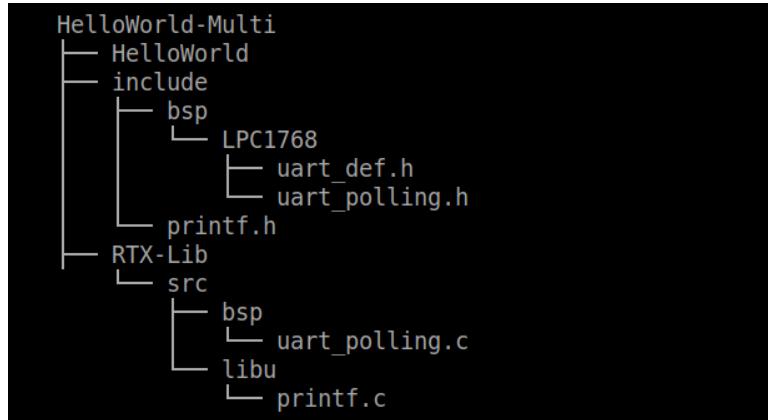


Figure 7.40: Directory Structure of a Multi-Project Workspace. The HelloWorld directory layout is omitted.

7.9.2 Create a New Library uVision Project

To create a new library uVision project, we follow the same steps of creating the new HelloWorld uVision project. Aside from giving the project a different name, the

big difference is that when asked for configuring the run-time environment, do not select anything, directly click the OK button (see Figure 7.41). Here are the steps.

- Click Project → New uVision Project (See Figure 7.2).
- Select NXP → LPC1700 Series → LPC176x → LPC1768 (See Figure 7.3).
- Do not select anything in the “Manage Run-Time Environment” pop-up window. Directly click the OK button. Compared with the HelloWorld application creation, the difference is that we should leave the CORE and Startup checkbox unchecked, which is the default setting (see Figure 7.41).

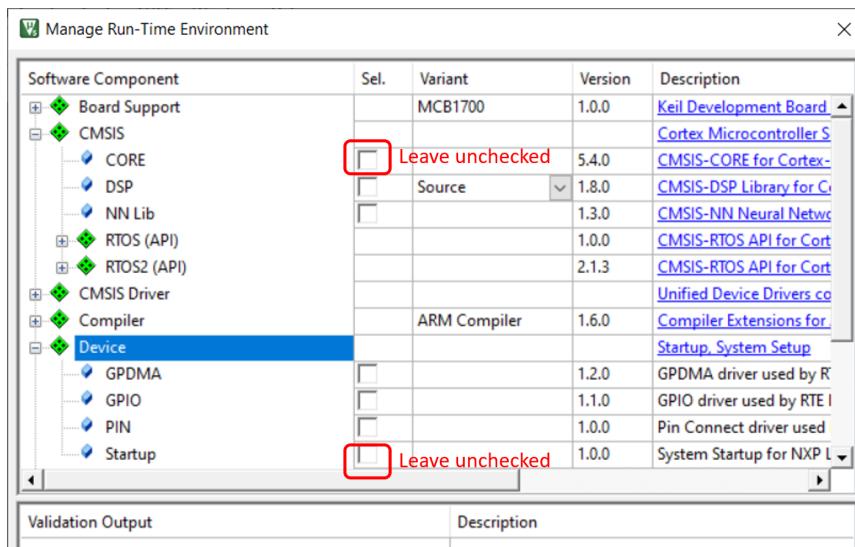


Figure 7.41: Directory Structure of a Multi-Project Workspace. The HelloWorld directory layout is omitted.

- Name the project file as `rtx-lib.uvprojx`.

7.9.3 Managing Library Project Component

You just finished creating another new project. The following steps are similar as creating your first HelloWorld project except that we are adding different source groups and we are adding different files to each source group. You can always refer Section 7.5 if you forget some of the steps.

1. Rename the Target
Rename the default “Target 1” to “RTX-Lib”.
2. Rename the Source Group
Rename the source group to “bsp”. Add a new source group and name it “libu”.

3. Add Source Code to a Source Groups

Add `uart_polling.c` to “bsp” source group. Add `printf.c` to “libu” source group. Your project will now look like Figure 7.42.

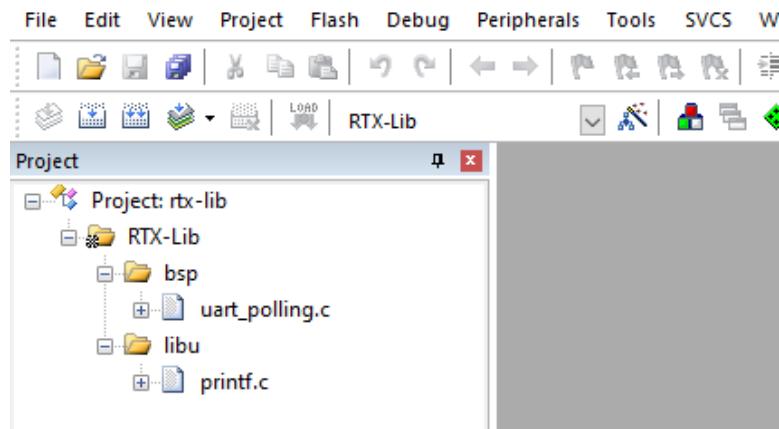


Figure 7.42: Keil IDE: A Library Project Profile

7.9.4 Configure a Library Target Options

Most of the default settings of the target options are good. There are a few options that we need to modify.

1. Bring up the target option configuration window by pressing the target options button (See Figure 7.12).
2. Configure the Target tab as shown in Figure 7.13. We want to use the default version 5 arm compiler. We also want remove the IRAM2 from the default setting. This is the same as the HelloWorld Application target tab configuration.
3. The most important step is to configure the output to be a library as shown in Figure 7.43

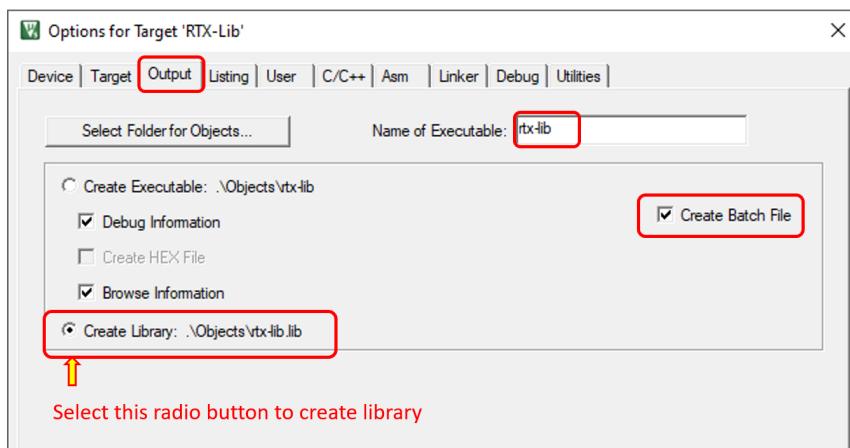


Figure 7.43: Keil IDE: Target Options Output Tab Library Creation Configuration

4. Configure the C/C++ tab as shown in Figure 7.44. In addition to the configuration you did for HellWorld application, you also need to specify the include path so the compiler knows where to find the header files. Note we moved the header files to a separate directory rather than having them in the same directory where the .c files are.

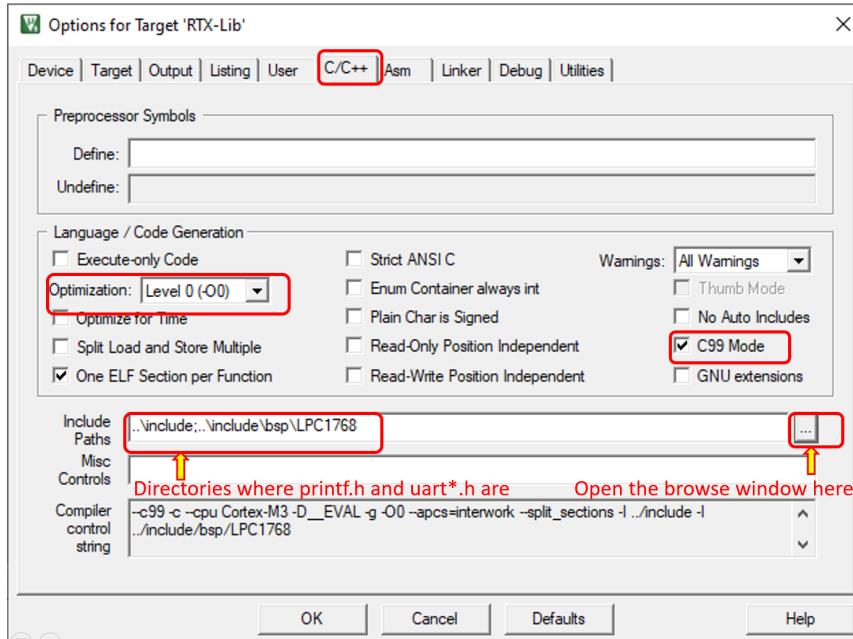


Figure 7.44: Keil IDE: Target Options C/C++ Tab Configuration

5. Configure the Linker tab the same way as you did for the HelloWorld application as shown in Figure 7.15.
6. Leave the rest of tab configurations as default.

7.9.5 Build the Library Target

To build the target, press the “Build” button (see Figure 7.17). If nothing goes wrong, the build output window at the bottom of the IDE will show a log similar like the one shown in Figure 7.45. Note the target is a .lib file and is in the default .\Objects directory. A library project cannot be executed. It needs to be linked with an application and the application generates an executable .axf file.

```
Build Output
Build started: Project: rtx-lib
*** Using Compiler 'V5.06 update 6 (build 750)', folder: 'C:\opt\Keil5\ARM\ARMCC\Bin'
*** Note: Rebuilding project, since 'Options->Output->Create Batch File' is selected.
Rebuild target 'RTX-Lib'
compiling printf.c...
compiling uart_polling.c...
creating Library...
".\Objects\rtx-lib.lib" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:00
```

Figure 7.45: Keil IDE: Build Library Target

7.10 Create an Application that Links with a Library

Let's now open up the copied HelloWorld application and remove the System Code group and its associated files from the project explorer window. Then we add a new Lib Group and add the library file `rtx-lib.lib` in the RTX-Lib/Objects to the Lib group (see Figure 7.46).

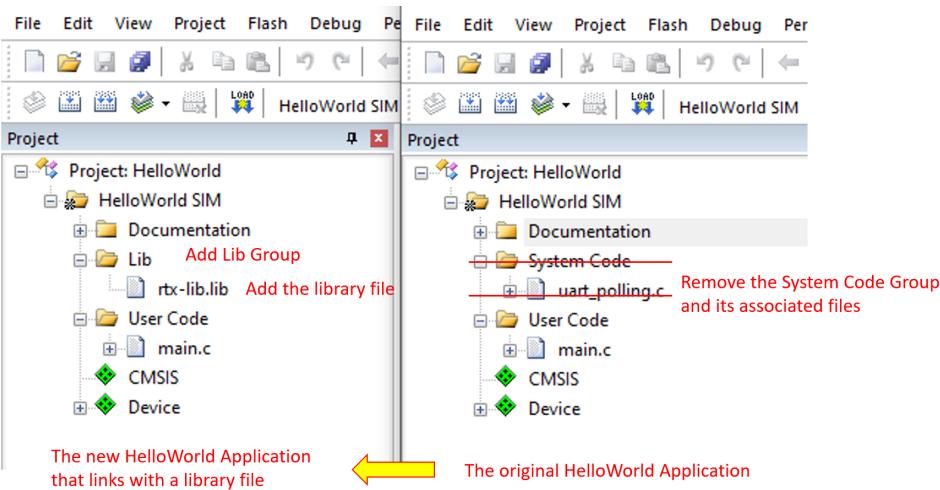


Figure 7.46: Keil IDE: HelloWorld Application that uses a Library

We then navigate to the `HelloWorld-Multi\HelloWorld\src` folder to remove `printf.[ch]` and `uart*. [ch]` files as shown in Figure 7.47.

Type	Name
C File	main
C File	printf
C File	uart_polling
H File	printf
H File	uart_def
H File	uart_polling

Figure 7.47: Keil IDE: Removing source code files from HelloWorld inside the Helloworld-Multi folder

We need to specify the include path in the C/C++ tab of the target option since now all header files are in a separate folder (see Figure 7.44). And we need to do this update for both the SIM and RAM targets. We are now ready to build the application, just press the build button as usual (see Figure 7.17). You will see the application is built and a `.axf` file is generated (see Figure 7.48). You may either use the debugger to run it on the simulator or on the board as usual.

```

Build Output
Build started: Project: HelloWorld
*** Using Compiler 'V5.06 update 6 (build 750)', folder: 'C:
Build target 'HelloWorld SIM'
linking...
Program Size: Code=1756 RO-data=236 RW-data=8 ZI-data=608
".\Objects\SIM\HelloWorld.axf" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:01

```

Figure 7.48: Keil IDE: Build Output of HelloWorld Application Linked with a Library

7.11 Create a Multi-Project Workspace

We now have two projects and they are related to each other. We want to put them into the same workspace. The uVision IDE can put multiple uVision projects into one workspace so that you can switch between projects easily. To create a uVision multi-project workspace, select Project → New Multi-Project Workspace (see Figure 7.49).

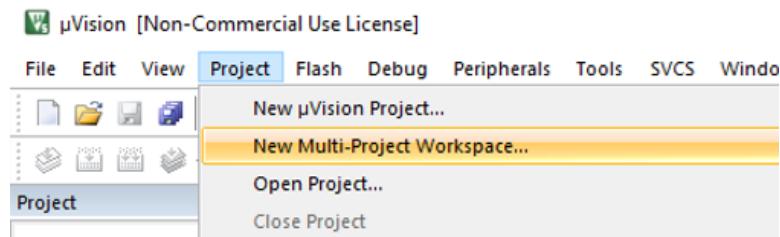


Figure 7.49: Keil IDE: Create a New Multi-Project Workspace Menu Item

You will be asked to save the multi-project profile file. Navigate to the HelloWorld-Multi folder and name the profile as HelloWorld-Multi.uvmpw. Then the “Create New Multi-Project Workspace” window appears for you to select individual projects you would like to add to the workspace (see Figure 7.50).

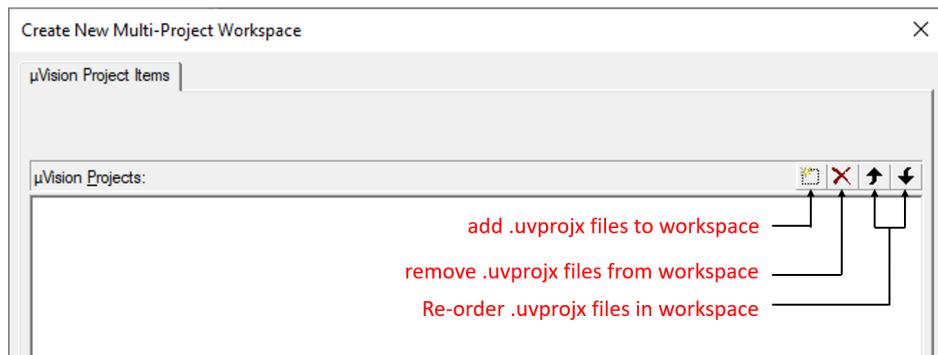


Figure 7.50: Keil IDE: Create a New Multi-Project Workspace Window

Let's first select the library project and then the application project (see Figure 7.51).

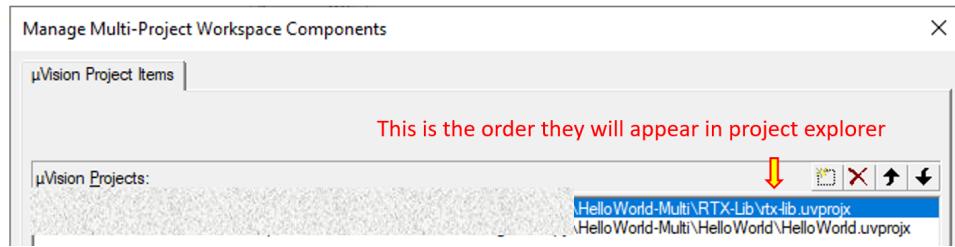


Figure 7.51: Keil IDE: Final New Multi-Project Workspace Window

Note that the order the projects are listed in the window is important. It determines the order of projects appearing in the project explorer window. The more important one is that it also determines the build order in batch build setup (see Section 7.12). After you press OK button, your setup should look like Figure 7.52.

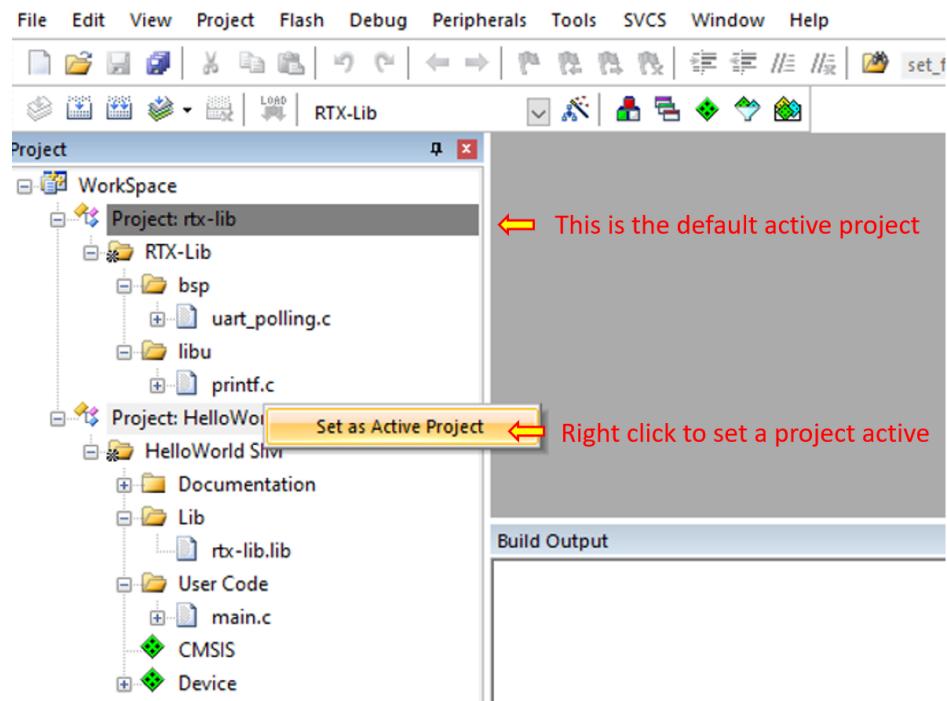


Figure 7.52: Keil IDE: Multi-Project Workspace Explorer

To take the full advantage of the IDE feature such as auto-suggesting function names and struct members, you need to make the project where the source code is associated with as the active project. There can only be one active project at a time. You will notice that when the library project is active, the debug button is greyed out. This is normal because a library is not an executable. The HelloWorld application that links with the library is an application that generates an executable. To make a project as the active project, right click the project to bring up the “Set as Active Project” context menu and select it (See Figure 7.52).

7.12 Batch Build

In the multi-project workspace, pressing the build button (see Figure 7.17) only builds the active project itself. Most of the time, we want to build all projects. This can be done by using the batch build feature of the IDE. To set up the batch build, select Project → Batch Setup (see Figure 7.53).

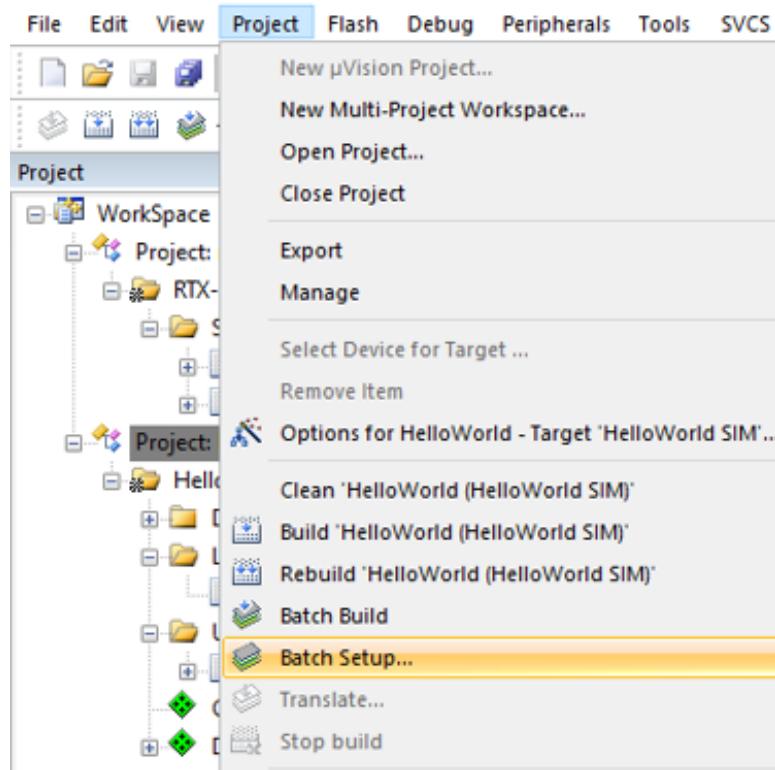


Figure 7.53: Keil IDE: Batch Setup Menu Item

We want to build all targets in the workspace (see Figure 7.54). Note the order of build sequence is important. We would like to first build the library, then the targets that are linked with the library. Reversing the order will make your application targets linked with the previously built library. Most of students will get frustrated when their newly built application code does not reflect the change they just made in the library. Not noticing the build order is culprit, one tends to start to move the Keil IDE down on the secret preferred IDE list. So we would like to bring your attention to this important point. At least this one is not the IDE's fault. When you are puzzled that why the change you made in the library does not appear in the application targets, batch build order is the first thing that you should check.



Figure 7.54: Keil IDE: Batch Setup Window

What if you want to change the build order? You can do so by bringing up the “Manage Multi-Project Workspace” context window to re-order the projects (see Figure 7.55).

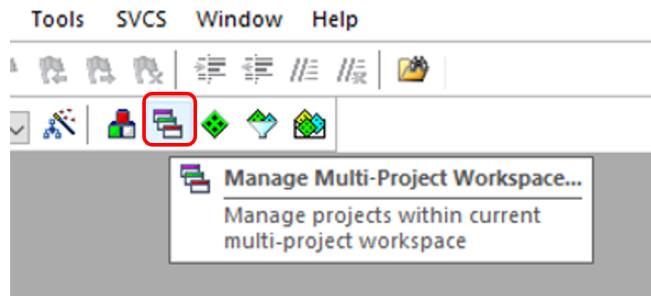


Figure 7.55: Keil IDE: Manage Multi-Project Workspace Button

To batch build the workspace, press the batch build button (see Figure 7.56). You can also select Project → Batch Build from the menu to achieve the same purpose.

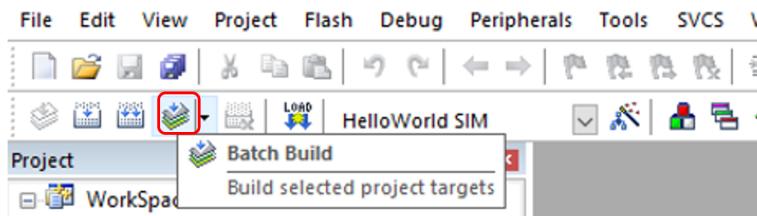


Figure 7.56: Keil IDE: Batch Build Button

You should watch carefully the build output message in the console window. Pay special attention to the last line of build summary (see Figure 7.57). If you have a compilation error of one of the projects, it shows up in the build summary. A commonly seen mistake is that the library failed to be built (due to syntax error), but students did not notice the error message. Then the application is successfully built, but linked with the previously built library. Hence students do not see the changes they made in the library project and once again too quickly move the IDE further down to their preferred IDE list.

```

Build Output

*** Using Compiler 'V5.06 update 6 (build 750)', folder: 'C:\opt\Keil5\ARM\ARMCC\Bin'
*** Note: Rebuilding project, since 'Options->Output->Create Batch File' is selected.
Rebuild Project 'rtx-lib' - Target 'RTX-Lib'
compiling printf.c...
compiling uart_polling.c...
creating Library...
".\Objects\rtx-lib.lib" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:03

*** Using Compiler 'V5.06 update 6 (build 750)', folder: 'C:\opt\Keil5\ARM\ARMCC\Bin'
Build Project 'HelloWorld' - Target 'HelloWorld SIM'
linking...
Program Size: Code=1756 RO-data=236 RW-data=8 ZI-data=608
".\Objects\SIM\HelloWorld.axf" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:00

*** Using Compiler 'V5.06 update 6 (build 750)', folder: 'C:\opt\Keil5\ARM\ARMCC\Bin'
Build Project 'HelloWorld' - Target 'HelloWorld RAM'
linking...
Program Size: Code=1736 RO-data=236 RW-data=8 ZI-data=608
".\Objects\RAM\HelloWorld.axf" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:01

Batch-Build summary: 3 succeeded, 0 failed, 0 skipped - Time Elapsed: 00:00:04

```

Figure 7.57: Keil IDE: Batch Build Output

7.13 Using the Library

To use the `printf` in the library we just built, just use the same syntax as the usual `libc printf` function. The `printf` library we have has limitations. It does not support floating point format output. The long format output also does not work properly. However we do not need them. The `%c`, `%d` and `%s` are what we need and they are supported. The `printf` prints to the second serial port by polling. Let's add some code to the `main.c` (see Figure 7.58) to see what it does. Without a memory allocator, we directly write data to the physical memory locations that we know that are free. Note the '`\n`' behaves differently on simulator terminal and the putty terminal (when using the board). The simulator automatically adds a `\r` when '`\n`' presents. The putty terminal does not.

```

main.c

37
38 #include <LPC17xx.h>
39 #include "uart_def.h"
40 #include "uart_polling.h"
41 #include "printf.h"
42
43 int main() {
44     SystemInit();
45     uart0_init();
46     uart1_init();
47     uart0_put_string("UART0 - Howdy!\r\n");
48     uart1_put_string("UART1 - Hello World!\r\n");
49     init_printf(NULL, putc);
50
51     char *p = (void *) 0x2007c000;
52     char *ptr = p;
53     for ( int i = 0; i < 26; i++ ) {
54         *ptr++ = 'A' + i;
55     }
56     *ptr = '\0';
57     printf("p = 0x%lx, ptr = 0x%lx\n", p, ptr);
58     for ( int i = 0; i < 3; i++ ) {
59         printf("i = %d: %s\r\n", i, p);
60     }
61     return 0;
62 }

```

Figure 7.58: The main.c code that uses printf

The output of the program by using the simulator is shown in Figure 7.59.

```

UART #2

UART1 - Hello World!
p = 0x2007c000, ptr = 0x2007c004
i = 0: ABCD
i = 1: ABCD
i = 2: ABCD

```

Figure 7.59: Keil IDE: demonstration of printf using simulator

The output of the program by using the simulator is shown in Figure 7.60.

```

COM9 - PuTTY

UART1 - Hello World!
p = 0x2007c000, ptr = 0x2007c004
i = 0: ABCD
i = 1: ABCD
i = 2: ABCD

```

Figure 7.60: Keil IDE: demonstration of printf on board

Now you may go to Chapter 3 to start adding a memory allocator to your RTX-Lib.

Chapter 8

Programming MCB1700

8.1 The Thumb-2 Instruction Set Architecture

The Cortex-M3 supports only the Thumb-2 (and traditional Thumb) instruction set. With support for both 16-bit and 32-bit instructions in the Thumb-2 instruction set, there is no need to switch the processor between Thumb state (16-bit instructions) and ARM state (32-bit instructions).

In the RTOS lab, you will need to program a little bit in the assembler language. We introduce a few assembly instructions that you most likely need to use in your project in this section.

The general formatting of the assembler code is as follows:

```
label
    opcode operand1, operand2, ... ; Comments
```

The `label` is optional. Normally the first operand is the destination of the operation (note `STR` is one exception).

Table 8.1 lists some assembly instructions that the RTX project may use. For complete instruction set reference, we refer the reader to Section 34.2 (ARM Cortex-M3 User Guide: Instruction Set) in [4].

8.2 ARM Architecture Procedure Call Standard (AAPCS)

The AAPCS (ARM Architecture Procedure Call Standard) defines how subroutines can be separately written, separately compiled, and separately assembled to work together. The C compiler follows the AAPCS to generate the assembly code. Table 8.2 lists registers used by the AAPCS.

Registers R0-R3 are used to pass parameters to a function and they are not preserved. The compiler does not generate assembler code to preserve the values of

Mnemonic	Operands/Examples	Description
LDR	$Rt, [Rn, \#offset]$	Load Register with word
	LDR R1, [R0, #24]	Load word value from memory address R0+24 into R1
LDM	$Rn\{!\}, reglist$	Load Multiple registers
	LDM R4, {R0 – R1}	Load word value from memory address R4 to R0, increment the address, load the value from the updated address to R1.
STR	$Rt, [Rn, \#offset]$	Store Register word
	STR R3, [R2, R6]	Store word in R3 to memory address R2+R6
	STR R1, [SP, #20]	Store word in R1 to memory address SP+20
MRS	$Rd, spec_reg$	Move from special register to general register
	MRS R0, MSP	Read MSP into R0
	MRS R0, PSP	Read PSP into R0
MSR	$spec_reg, Rm$	Move from general register to special register
	MSR MSP, R0	Write R0 to MSP
	MSR PSP, R0	Write R0 to PSP
PUSH	$reglist$	Push registers onto stack
	PUSH {R4 – R11, LR}	push in order of decreasing the register numbers
POP	$reglist$	Pop registers from stack
	POP {R4 – R11, PC}	pop in order of increasing the register numbers
BL	$label$	Branch with Link
	BL func	Branch to address labeled by func, return address stored in LR
BLX	Rm	Branch indirect with link
	BLX R12	Branch with link and exchange (Call) to an address stored in R12
BX	Rm	Branch indirect
	BX LR	Branch to address in LR, normally for function call return

Table 8.1: Assembler instruction examples

Register	Synonym	Special	Role in the procedure call standard
r15		PC	The Program Counter.
r14		LR	The Link Register.
r13		SP	The Stack Pointer (full descending stack).
r12		IP	The Intra-Procedure-call scratch register.
r11	v8		Variable-register 8.
r10	v7		Variable-register 7.
r9		v6 SB TR	Platform register. The meaning of this register is defined by platform standard.
r8	v5		Variable-register 5.
r7	v4		Variable-register 4.
r6	v3		Variable-register 3.
r5	v2		Variable-register 2.
r4	v1		Variable-register 1.
r3	a4		argument / scratch register 4
r2	a3		argument / scratch register 3
r1	a2		argument / result / scratch register 2
r0	a1		argument / result / scratch register 1

Table 8.2: Core Registers and AAPCS Usage

these registers. R0 is also used for return value of a function.

Registers R4-R11 are preserved by the called function. If the compiler generated assembler code uses registers in R4-R11, then the compiler generate assembler code to automatically push/pop the used registers in R4-R11 upon entering and exiting the function.

R12-R15 are special purpose registers. A function that has the `__svc_indirect` keyword makes the compiler put the first parameter in the function to R12 followed by an SVC instruction. R13 is the stack pointer (SP). R14 is the link register (LR), which normally is used to save the return address of a function. R15 is the program counter (PC).

Note that the exception stack frame automatically backs up R0-R3, R12, LR and PC together with the xPSR. This allows the possibility of writing the exception handler in purely C language without the need of having a small piece of assembly code to save/restore R0-R3, LR and PC upon entering/exiting an exception handler routine.

8.3 Cortex Microcontroller Software Interface Standard (CMSIS)

The Cortex Microcontroller Software Interface Standard (CMSIS) was developed by ARM. It provides a standardized access interface for embedded software products (see Figure 8.1). This improves software portability and re-usability. It enables soft-

ware solution suppliers to develop products that can work seamlessly with device libraries from various silicon vendors [3].

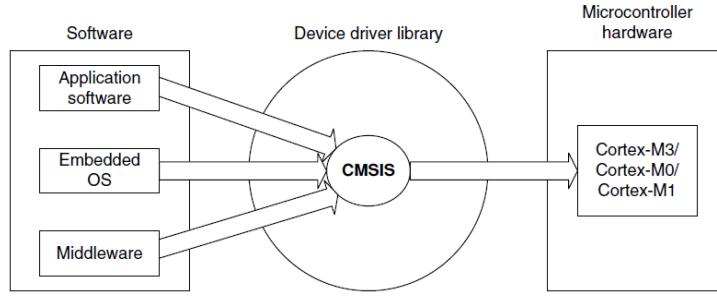


Figure 8.1: Role of CMSIS[5]

The CMSIS uses standardized methods to organize header files that makes it easy to learn new Cortex-M microcontroller products and improve software portability. With the `<device>.h` (e.g. `LPC17xx.h`) and system startup code files (e.g., `startup_LPC17xx.s`), your program has a common way to access

- **Cortex-M processor core registers** with standardized definitions for NVIC, SysTick, MPU registers, System Control Block registers , and their core access functions (see `core_cm*.[ch]` files).
- **system exceptions** with standardized exception number and handler names to allow RTOS and middleware components to utilize system exceptions without having compatibility issues.
- **intrinsic functions with standardized name** to produce instructions that cannot be generated by IEC/ISO C.
- **system initialization** by common methods for each MCU. Fore example, the standardized `SystemInit()` function to configure clock.
- **system clock frequency** with standardized variable named as `SystemFrequency` defined in the device driver.
- **vendor peripherals** with standardized C structure.

8.3.1 CMSIS files

The CMSIS is divided into multiple layers (See Figure 8.2). For each device, the MCU vendor provides a device header file `<device>.h` (e.g., `LPC17xx.h`) which pulls in additional header files required by the device driver library and the Core Peripheral Access Layer (see Figure 8.3).

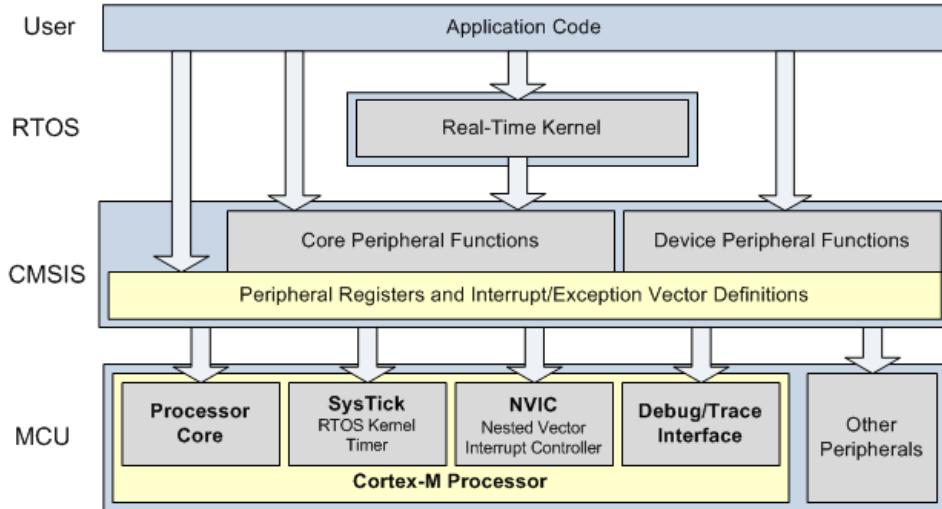


Figure 8.2: CMSIS Organization[3]

By including the `<device>.h` (e.g., `LPC17xx.h`) file into your code file. The first step to initialize the system can be done by calling the CMSIS function as shown in Listing 8.1.

```
SystemInit(); // Initialize the MCU clock
```

Listing 8.1: CMSIS SystemInit()

The CMSIS compliant device drivers also contain a startup code (e.g., `startup_LPC17xx.s`), which include the vector table with standardized exception handler names (See Section 8.3.3).

8.3.2 Cortex-M Core Peripherals

We only introduce the NVIC programming in this section. The Nested Vectored Interrupt Controller (NVIC) can be accessed by using CMSIS functions (see Figure 8.4). As an example, the following code enables the UART0 and TIMER0 interrupt

```
NVIC_EnableIRQ(UART0_IRQn); // UART0_IRQn is defined in LPC17xx.h
NVIC_EnableIRQ(TIMER0_IRQn); // TIMER0_IRQn is defined in LPC17xx.h
```

8.3.3 System Exceptions

Writing an exception handler becomes very easy. One just defines a function that takes no input parameter and returns void. The function takes the name of the standardized exception handler name as defined in the startup code (e.g., `startup_LPC17xx.s`).

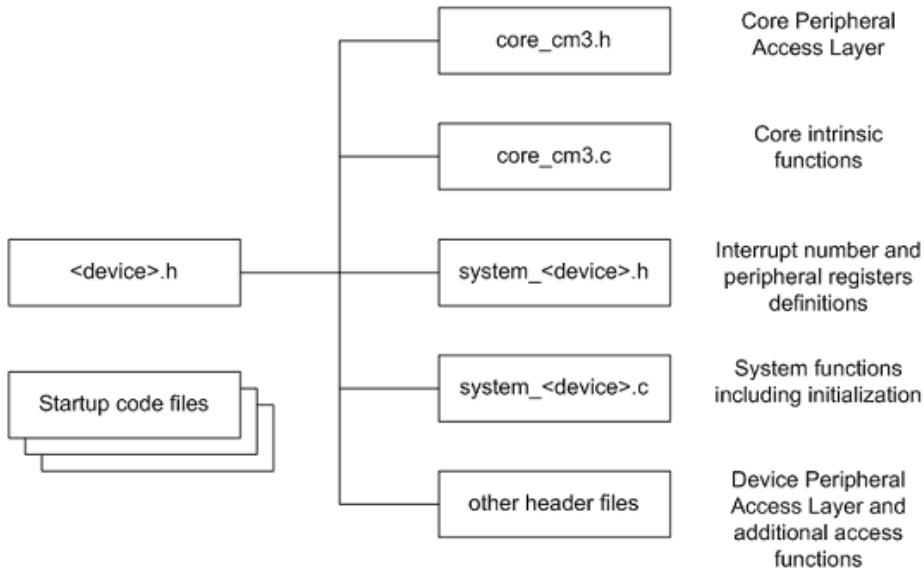


Figure 8.3: CMSIS Organization[3]

Function definition		Description
void	NVIC_SystemReset (void)	Resets the whole system including peripherals.
void	NVIC_SetPriorityGrouping (uint32_t priority_grouping)	Sets the priority grouping.
uint32_t	NVIC_GetPriorityGrouping (void)	Returns the value of the current priority grouping.
void	NVIC_EnableIRQ (IRQn_Type IRQn)	Enables the interrupt IRQn.
void	NVIC_DisableIRQ (IRQn_Type IRQn)	Disables the interrupt IRQn.
void	NVIC_SetPriority (IRQn_Type IRQn, int32_t priority)	Sets the priority for the interrupt IRQn.
uint32_t	NVIC_GetPriority (IRQn_Type IRQn)	Returns the priority for the specified interrupt.
void	NVIC_SetPendingIRQ (IRQn_Type IRQn)	Sets the interrupt IRQn pending.
IRQn_Type	NVIC_GetPendingIRQ (IRQn_Type IRQn)	Returns the pending status of the interrupt IRQn.
void	NVIC_ClearPendingIRQ (IRQn_Type IRQn)	Clears the pending status of the interrupt IRQn, if it is not already running or active.
IRQn_Type	NVIC_GetActive (IRQn_Type IRQn)	Returns the active status for the interrupt IRQn.

Figure 8.4: CMSIS NVIC Functions[3]

The following listing shows an example to write the UART0 interrupt handler entirely in C.

```

void UART0_Handler (void)
{
    // write your IRQ here
}

```

Another way is to use the embedded assembly code:

Instruction		CMSIS Intrinsic Function
CPSIE I		void __enable_irq(void)
CPSID I		void __disable_irq(void)
Special Register	Access	CMSIS Function
CONTROL	Read	uint32_t __get_CONTROL(void)
	Write	void __set_CONTROL(uint32_t value)
MSP	Read	uint32_t __get_MSP(void)
	Write	void __set_MSP(uint32_t value)
PSP	Read	uint32_t __get_PSP(void)
	Write	void __set_PSP(uint32_t value)

Table 8.3: CMSIS intrinsic functions defined in `core_cmFunc.h`

```

__asm void UART0_Handler(void)
{
    ; do some asm instructions here
    BL __cpp(a_c_function) ; a_c_function is a regular C function
    ; do some asm instructions here,
}

```

8.3.4 Intrinsic Functions

ANSI cannot directly access some Cortex-M3 instructions. The CMSIS provides intrinsic functions that can generate these instructions. The CMSIS also provides a number of functions for accessing the special registers using MRS and MSR instructions. The intrinsic functions are provided by the RealView Compiler. Table 8.3 lists some intrinsic functions that your RTOS project most likely will need to use. We refer the reader to Tables 613 and 614 one page 650 in Section 34.2.2 of [4] for the complete list of intrinsic functions.

8.3.5 Vendor Peripherals

All vendor peripherals are organized as C structure in the `<device>.h` file (e.g., `LPC17xx.h`). For example, to read a character received in the RBR of UART0, we can use the following code.

```

unsigned char ch;
ch = LPC_UART0->RBR; // read UART0 RBR and save it in ch

```

8.4 Accessing C Symbols from Assembly

Both inline and embedded assembly are supported in MDK5. We will mainly using embedded assembly in this lab. To write an embedded assembly function, you need to use the `__asm` keyword. For example the the function “`embedded_asm_function`” in Listing 8.3 is an embedded assembly function. You can only put assembly instructions inside this function.

The `__cpp` keyword allows one to access C compile-time constant expressions, including the addresses of data or functions with external linkage, from the assembly code. The expression inside the `__cpp` can be one of the followings:

- A global variable defined in C. In Listing 8.2, we have two C global variables `g_pcb` and `g_var`. We can use the `__cpp` to access them as shown in Listing 8.3. Note to access the value of a variable, it needs to be a constant variable. For a non-constant variable, the assembly code access the address of the variable.

```
#define U32 unsigned int
#define SP_OFFSET 4

typedef struct pcb {
    struct pcb *mp_next;
    U32 *mp_sp; // 4 bytes offset from the starting address of
                 // this structure
    //other variables...
} PCB;

PCB g_pcb;
const U32 g_var;
```

Listing 8.2: Example of accessing C global variables from assembly. The C code.

```
__asm embedded_asm_function(void) {
    LDR R3,=__cpp(&g_pcb) ; load R3 with the address of g_pcb
    LDM R3, {R1, R2}      ; load R1 with g_pcb.mp_next
                           ; load R2 with g_pcb.mp_sp
    LDR R4,=__cpp(g_var) ; load R4 with the value of g_var, which is
                           a constant
    STR R4, [R3, #SP_OFFSET] ; write R4 value to g_pcb.mp_sp
}
```

Listing 8.3: Example of accessing global variable from assembly

- A C function. In Listing 8.4, `a_c_function` is a function written in C. We can invoke this function by using the assembly language.

```
extern void a_c_function(void);
...
__asm embedded_asm_function(void) {
    ;.....
    BL __cpp(a_c_function) ; a_c_function is regular C function
```

```
    ;.....  
}
```

Listing 8.4: Example of accessing c function from assembly

- A constant expression in the range of 0 – 255 defined in C. In Listing 8.5, `g_flag` is such a constant. We can use `MOV` instruction on it. Note the `MOV` instruction only applies to immediate constant value in the range of 0 – 255.

```
unsigned char const g_flag;  
  
__asm embedded_asm_function(void) {  
    ;.....  
    MOV R4, #__cpp(g_flag) ; load g_flag value into R4  
    ;.....  
}
```

Listing 8.5: Example of accessing constant from assembly

You can also use the `IMPORT` directive to import a C symbol in the embedded assembly function and then start to use the imported symbol just as a regular assembly symbol (see Listing 8.6).

```
void a_c_function (void) {  
    // do something  
}  
  
__asm embedded_asm_add(void) {  
    IMPORT a_c_function ; a_c_function is a regular C function  
    BL a_c_function ; branch with link to a_c_function  
}
```

Listing 8.6: Example of using `IMPORT` directive to import a C symbol.

Names in the `#__cpp` expression are looked up in the C context of the `__asm` function. Any names in the result of the `#__cpp` expression are mangled as required and automatically have `IMPORT` statements generated from them.

8.5 SVC Programming: Writing an RTX API Function

A function in RTX API requires a service from the operating system. It needs to be implemented through the proper gateway by *trapping* from the user level into the kernel level. On Cortex-M3, the `SVC` instruction is used to achieve this purpose.

The basic idea is that when a function in RTX API is called from the user level, this function will trigger an `SVC` instruction. The `SVC_Handler`, which is the CMSIS standardized exception handler for `SVC` exception will then invoke the kernel function that provides the actual service (see Figure 8.5). Effectively, the RTX API function is a wrapper that invokes `SVC` exception handler and passes corresponding kernel service operation information to the `SVC` handler.

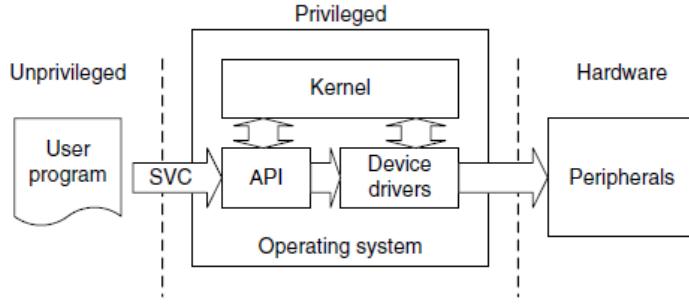


Figure 8.5: SVC as a Gateway for OS Functions [5]

The kernel needs to know which system call maps to which kernel functions call. We can use different SVC number for different system calls if there are sufficient number of SVC numbers the instruction supports. We can use a single SVC number as system call entry to kernel and then use register R12 to encode the information for the kernel to find the corresponding kernel function for a system call.

To generate an SVC instruction, there are two methods. One is to directly program at assembly instruction level. The other one is to use arm compiler-specific keywords to let the compiler generate SVC instructions.

8.5.1 Programming in Assembly Language

We can use the embedded assembly to write SVC instruction directly. Assume we want to create a system call `void *sys_func(size_t size)` and the kernel counter part of this system call is `void *k_sys_func(size_t t)`. One way of implementation is to assign an SVC number, say `0x0` to `sys_func`. Listing 8.7 shows one implementation.

```
__asm void *sys_func(size_t size) {
    LDR R12,=__cpp(k_sys_func)
    ; code fragment omitted
    SVC 0
    BX LR
    ALIGN
}
```

Listing 8.7: Code Snippet of `sys_func`

The corresponding kernel function is a C function `k_sys_func`. This function entry point is loaded to register `r12`. Then `SVC 0` causes an SVC exception with immediate number 0. In the SVC exception handler, we can then branch with link and exchange to the address stored in `r12`. Listing 8.8 is an excerpt of `SVC_Handler` written in assembly.

```

__asm void SVC_Handler(void) {
    MRS R0, PSP
    ; code that may use R0-R3 and R12 for computation
    ; Extract SVC number, if SVC 0, then do the following
    LDM R0, {R0-R3, R12}; Read R0-R3, R12 from stack

    ; code to save cpu registers omitted

    BLX R12 ; R12 contains the kernel function entry point

    ; code to restore registers omitted
    ; code to handle return value of C function omitted
    MVN LR, #:NOT:0xFFFFFFF; set EXC_RETURN, thread mode, PSP
    BX LR
}

```

Listing 8.8: Code Snippet of SVC_Handler

8.5.2 Programming in C with ARM Compiler Keywords

The second method is to ask the compiler to generate the SVC instruction from C code. The ARM compiler provides two keywords. One is `__svc` and the other is `__svc_indirect`.

The `__svc` keyword declares a *SuperVisor Call* (SVC) function taking up to four integer-like arguments and returning up to four results in a `value_in_regs` structure [1]. The immediate value used in the SVC needs to be provided to the compiler. The syntax of it is as follows:

```

__svc(int svc_num) return_type function_name([argument-list]);

```

Listing 8.9: `__svc` compiler keyword syntax

This causes function invocations to be compiled inline as an AAPCS-compliant operation that behaves similarly to a normal call to a function. The `__value_in_regs` qualifier can be used to specify a small structure of up to 16 bytes in registers for return, rather than by the usual structure-passing mechanism defined in the AAPCS.

The following C code creates a system call of `void *sys_call(size_t size)`, the compiler generates the SVC 0 instruction. This is the mechanism we will use in lab.

```

#define SVC_SYS_CALL 0
__svc(0) void *sys_call(size_t size);

```

Listing 8.10: `__svc` compiler keyword example

Another way of making the compiler to generate SVC instructions is to use the `__svc_indirect` keyword which passes an operation code to the SVC handler in

`r12` [1]. This keyword is a function qualifier. The two inputs we need to provide to the compiler are

- `svc_num`, the immediate value used in the SVC instruction and
- `op_num`, the value passed in `r12` to the handler to determine the function to perform. The following is the syntax of an indirect SVC.

```
__svc_indirect(int svc_num)
    return_type function_name(int op_num[, argument-list]);
```

Listing 8.11: `__svc_indirect` compiler keyword syntax

The SVC handler must make use of the `r12` value to select the required operation. Using the example system call `void *sys_call(size_t size)` again, the following code is relevant to the implementation of the function so that it will use SVC 0 to enter the SVC handler with the corresponding kernel function address loaded in R12.

```
#define __SVC_0 __svc_indirect(0)
extern void *k_sys_call(size_t size);
#define sys_call(size) _sys_call((U32)k_sys_call, size);
extern void *_sys_call(U32 p_func, size_t size) __SVC_0;
```

Listing 8.12: `__svc_indirect` compiler keyword example

The compiler generates two assembly instructions

```
LDR.W r12, [pc, #offset]; Load k_sys_call into r12
SVC 0x00
```

The `SVC_handler` in Listing 8.8 then can be used to handle the SVC 0 exception.

8.6 UART Programming

The ultimate reference of LPC1768 UART is chapters 15 and 16 of [4]. There are four UARTs on the chip. We use UART0 and UART1. The UART data transmission can be interrupt driven or polled. In this project, we configure UART0 to be interrupt driven for both receiving and transmitting. UART1 is configured to use polling for both data receiving and transmitting.

The LPC1768 UART receiver and transmitter have a 16-element FIFO each and they are referred as RX FIFO and TX FIFO respectively. The Receiver Buffer Register (RBR) is the top byte (i.e. the oldest byte) of the RX FIFO. The Transmit Holding Register (THR) is the top byte (i.e. the newest byte) of the TX FIFO. To write to the THR,

one needs to make sure the THR is empty. Otherwise, the write will overwrite the byte in THR which is not shifted out by the transmit shift register. When programming the UART by polling, one can poll the status bits in the Line Status Register (LSR). When programming the UART as interrupt-driven, the interrupt is the FIFO status indicator.

To program a UART on MCB1700 board, one first needs to configure the UART by following the steps listed in Section 15.1 in [4] (referred as LPC17xx_UM in the sample code comments). Listings 8.13, 8.14 8.15, and 8.16 give one possible implementation of programming UART0 interrupts. This implementation configures the RX FIFO interrupt to be triggered when one character is received by the RX FIFO. The transmit interrupt is triggered when the transmit holding register becomes empty. The RX FIFO interrupt is always on and the TX FIFO interrupt is turned off when there are no data to transmit by the interrupt handler and turned back on when there are data to transmit by the main program. The UART Interrupt Enable Register (IER) controls the UART device level interrupt source setting.

```

/********************* // **
 * @file uart_def.h
 ****
#ifndef UART_DEF_H_
#define UART_DEF_H_

/* The following macros are from NXP uart.h */
#define IER_RBR    0x01
#define IER_THRE   0x02
#define IER_RLS    0x04

#define IIR_PEND   0x01
#define IIR_RLS    0x03
#define IIR_RDA    0x02
#define IIR_CTI    0x06
#define IIR_THRE   0x01

#define LSR_RDR    0x01
#define LSR_OE     0x02
#define LSR_PE     0x04
#define LSR_FE     0x08
#define LSR_BI     0x10
#define LSR_THRE   0x20
#define LSR_TEMT   0x40
#define LSR_RXFE   0x80

#define BUFSIZE    0x40
/* end of NXP uart.h file reference */

/* convenient macro for bit operation */
#define BIT(X)      ( 1U << (X) )

/*

```

```

8 bits, no Parity, 1 Stop bit

0x83 = 1000 0011 = 1 0 00 0 0 11
LCR[7] =1 enable Divisor Latch Access Bit DLAB
LCR[6] =0 disable break transmission
LCR[5:4]=00 odd parity
LCR[3] =0 no parity
LCR[2] =0 1 stop bit
LCR[1:0]=11 8-bit char len
See table 279, pg306 LPC17xx_UM
*/
#define UART_8N1 0x83

#ifndef NULL
#define NULL 0
#endif

#endif /* !UART_DEF_H */

```

Listing 8.13: UART0 IRQ Code uart_def.h

```

/********************************************//**
* @file uart_irq.h
*****
#ifndef UART_IRQ_H_
#define UART_IRQ_H_

/* typedefs */
#include <stdint.h>
#include "uart_def.h"

/* initialize the n_uart to use interrupt */
int uart_irq_init(int n_uart);

#endif /* ! UART_IRQ_H */

```

Listing 8.14: UART0 IRQ Code uart_irq.h

```

/********************************************//**
* @file uart_irq.c
* @brief UART IRQ handler. It receives input char through RX interrupt
*        and then writes a string containing the input char through
*        TX interrupts.
*****
#include <LPC17xx.h>
#include "uart_irq.h"
#include "uart_polling.h"
#ifdef DEBUG_0
#include "printf.h"
#endif

uint8_t g_buffer[] = "You Typed a Q\r\n";
uint8_t *gp_buffer = g_buffer;

```

```

uint8_t g_send_char = 0;
uint8_t g_char_in;
uint8_t g_char_out;

/*
 ****
 * @brief: initialize the n_uart
 * @note: It only supports UART0.
 *        It can be easily extended to support UART1 IRQ.
 *        The step number in the comments matches the item number
 *        in Section 14.1 on pg 298 of LPC17xx_UM
 ****
 */
int uart_irq_init(int n_uart) {

    LPC_UART_TypeDef *pUart;

    if (n_uart == 0) {
        /*
         Steps 1 & 2: system control configuration.
         Under CMSIS, system_LPC17xx.c does these two steps

        -----
        Step 1: Power control configuration.
        See table 46 pg63 in LPC17xx_UM
        -----
        Enable UART0 power, this is the default setting
        done in system_LPC17xx.c under CMSIS.
        Enclose the code for your reference
        //LPC_SC->PCONP |= BIT(3);

        -----
        Step2: Select the clock source.
        Default PCLK=CCLK/4 , where CCLK = 100MHZ.
        See tables 40 & 42 on pg56-57 in LPC17xx_UM.
        -----
        Check the PLL0 configuration to see how XTAL=12.0MHZ
        gets to CCLK=100MHZin system_LPC17xx.c file.
        PCLK = CCLK/4, default setting after reset.
        Enclose the code for your reference
        //LPC_SC->PCLKSEL0 &= ~(BIT(7)|BIT(6));

        -----
        Step 5: Pin Ctrl Block configuration for TXD and RXD
        See Table 79 on pg108 in LPC17xx_UM.
        -----
        Note this is done before Steps3-4 for coding purpose.
        */

        /* Pin P0.2 used as TXD0 (Com0) */
        LPC_PINCON->PINSEL0 |= (1 << 4);

        /* Pin P0.3 used as RXD0 (Com0) */

```

```

LPC_PINCON->PINSEL0 |= (1 << 6);

pUart = (LPC_UART_TypeDef *) LPC_UART0;

} else if ( n_uart == 1) {

/* see Table 79 on pg108 in LPC17xx_UM */
/* Pin P2.0 used as TXD1 (Com1) */
LPC_PINCON->PINSEL4 |= (2 << 0);

/* Pin P2.1 used as RXD1 (Com1) */
LPC_PINCON->PINSEL4 |= (2 << 2);

pUart = (LPC_UART_TypeDef *) LPC_UART1;

} else {
    return 1; /* not supported yet */
}

/*
-----
Step 3: Transmission Configuration.
    See section 14.4.12.1 pg313-315 in LPC17xx_UM
    for baud rate calculation.
-----
*/
/* Step 3a: DLAB=1, 8N1 */
pUart->LCR = UART_8N1; /* see uart.h file */

/* Step 3b: 115200 baud rate @ 25.0 MHZ PCLK */
pUart->DLM = 0; /* see table 274, pg302 in LPC17xx_UM */
pUart->DLL = 9; /* see table 273, pg302 in LPC17xx_UM */

/* FR = 1.507 ~ 1/2, DivAddVal = 1, MulVal = 2
   FR = 1.507 = 25MHZ/(16*9*115200)
   see table 285 on pg312 in LPC_17xxUM
*/
pUart->FDR = 0x21;

/*
-----
Step 4: FIFO setup.
    see table 278 on pg305 in LPC17xx_UM
-----
enable Rx and Tx FIFOs, clear Rx and Tx FIFOs
Trigger level 0 (1 char per interrupt)
*/
pUart->FCR = 0x07;

/* Step 5 was done between step 2 and step 4 a few lines above */

```

```

/*
-----
Step 6 Interrupt setting and enabling
-----
*/
/* Step 6a:
   Enable interrupt bit(s) wihtin the specific peripheral register.
   Interrupt Sources Setting: RBR, THRE or RX Line Stats
   See Table 50 on pg73 in LPC17xx_UM for all possible UART0 interrupt
   sources
   See Table 275 on pg 302 in LPC17xx_UM for IER setting
*/
/* disable the Divisior Latch Access Bit DLAB=0 */
pUart->LCR &= ~(BIT(7));

/* enable RBR and RLS interrupts */
pUart->IER = IER_RBR | IER_RLS;

/* Step 6b: set UART interrupt priority and enable the UART interrupt
   from the system level */
if ( n_uart == 0 ) {
    /* UART0 IRQ priority setting */
    NVIC_SetPriority(UART0_IRQn, 0x08);
    NVIC_EnableIRQ(UART0_IRQn);
} else if ( n_uart == 1 ) {
    NVIC_SetPriority(UART1_IRQn, 0x08);
    NVIC_EnableIRQ(UART1_IRQn);
} else {
    return 1; /* not supported yet */
}

//pUart->THR = '\0';
return 0;
}

/**
 * @brief: use CMSIS ISR for UART0 IRQ Handler
 * NOTE: This example shows how to save/restore all registers rather than
   just
 *      those backed up by the exception stack frame. We add extra
 *      push and pop instructions in the assembly routine.
 *      The actual c_UART0_IRQHandler does the rest of irq handling
 */
__asm void UART0_IRQHandler(void)
{
    PRESERVE8
    IMPORT c_UART0_IRQHandler
    CPSID I
    PUSH{r4-r11, lr}
    BL c_UART0_IRQHandler
    CPSIE I
    POP{r4-r11, pc}
}

```

```

}

/***
 * @brief: c UART0 IRQ Handler
 */
void c_UART0_IRQHandler(void)
{
    uint8_t IIR_IntId; /* Interrupt ID from IIR */
    LPC_UART_TypeDef *pUart = (LPC_UART_TypeDef *)LPC_UART0;

#ifdef DEBUG_0
    uart1_put_string("Entering c_UART0_IRQHandler\r\n");
#endif // DEBUG_0

    /* Reading IIR automatically acknowledges the interrupt */
    IIR_IntId = (pUart->IIR) >> 1; /* skip pending bit in IIR */
    if (IIR_IntId & IIR_RDA) { /* Receive Data Available */
        /* Read UART. Reading RBR will clear the interrupt */
        g_char_in = pUart->RBR;
#ifdef DEBUG_0
        uart1_put_string("Reading a char = ");
        uart1_put_char(g_char_in);
        uart1_put_string("\r\n");
#endif /* DEBUG_0 */
        g_buffer[12] = g_char_in; /* nasty hack */
        g_send_char = 1;
    } else if (IIR_IntId & IIR_THRE) {
        /* THRE Interrupt, transmit holding register becomes empty */
        if (*gp_buffer != '\0' ) { // not end of the string yet
            g_char_out = *gp_buffer;
#endif /* DEBUG_0 */
        }
        pUart->THR = g_char_out;
        gp_buffer++;
    } else { // end of the string
#endif /* DEBUG_0 */
        uart1_put_string("Finish writing. Turning off IER_THRE\r\n");
#endif /* DEBUG_0 */
        pUart->IER &= ~IER_THRE; // clear the IER_THRE bit
        gp_buffer = g_buffer; // reset the buffer
    }
} else { /* not implemented yet */
#endif /* DEBUG_0 */
    uart1_put_string("Should not get here!\r\n");
#endif /* DEBUG_0 */
    return;
}
}

/*
=====
* END OF FILE
=====
```

```
 */
```

Listing 8.15: UART0 IRQ Code uart_irq.c

```
/* **** */
* @file      main_uart_irq.c
* @brief     Echoing user input through UART0 by interrupt.
*
*           uart1, a debugging terminal, is by polling.
* @note      The RLS and RBR interrupts are always on.
*           The THRE interrupt is only on when we need to
*           transmit data stream.
* ****

#include <LPC17xx.h>
#include "uart_irq.h"
#include "uart_polling.h"
#include "printf.h"

extern uint8_t g_send_char;
extern uint8_t g_char_in;

int main()
{
    LPC_UART_TypeDef *pUart;

    SystemInit();
    __disable_irq();

    uart_irq_init(0); // uart0 interrupt driven, for RTX console
    uart_init(1); // uart1 polling, for debugging
    init_printf(NULL, putc); // printf uses the polling terminal

    __enable_irq();

    uart1_put_string("COM1> Type a character at COM0 terminal\n\r");

    pUart = (LPC_UART_TypeDef *) LPC_UART0;
    while( 1 ) {
        if (g_send_char == 1) { // This flag is set by the IRQ handler upon an
            //RX interrupt
            //pUart->THR &= ~IER_THRE;// turn off TX interrupt if it is on.
            // But in this example, TX interrupt is off by the time we reach
            // here
            pUart->THR = g_char_in; // the THR must be empty at this moment
            pUart->IER |= IER_THRE; // turn on the TX interrupt
            g_send_char = 0; // clear the flag
        }
    }
}
```

Listing 8.16: UART0 IRQ Code main_uart_irq.c

Listings 8.17 and 8.18 give one sample implementation of programming UART0

by polling.

```
/********************************************//**  
* @file      uart_polling.h  
* @brief     uart polling header file  
*****  
  
#ifndef UART_POLLING_H_  
#define UART_POLLING_H_  
  
#include <stdint.h> /* typedefs */  
#include "uart_def.h"  
  
#define uart0_init() uart_init(0)  
#define uart0_get_char() uart_get_char(0)  
#define uart0_put_char(c) uart_put_char(0,c)  
#define uart0_put_string(s) uart_put_string(0,s)  
  
#define uart1_init() uart_init(1)  
#define uart1_get_char() uart_get_char(1)  
#define uart1_put_char(c) uart_put_char(1,c)  
#define uart1_put_string(s) uart_put_string(1,s)  
  
int uart_init(int n_uart); /* initialize the n_uart */  
int uart_get_char(int n_uart); /* read a char from the n_uart */  
int uart_put_char(int n_uart, char c); /* write a char to n_uart */  
int uart_put_string(int n_uart, char *s);/* write a string to n_uart */  
void putc(void *p, char c); /* call back function for printf, use uart1  
 */  
  
#endif /* ! UART_POLLING_H_ */
```

Listing 8.17: UART0 Polling Code uart_polling.h

```
/********************************************//**  
* @file      uart_polling.c  
* @brief     polling UART to send and receive data  
* @note      the code handles UART0/1  
*****  
  
#include <LPC17xx.h>  
#include "uart_polling.h"  
  
*****  
* @brief: initialize the n_uart  
* @param: n_uart 0 for UART 0 and 1 for UART1  
*****  
  
int uart_init(int n_uart) {  
  
    LPC_UART_TypeDef *pUart; // ptr to memory mapped device UART, check  
                           // LPC17xx.h for UART register C structure overlay  
  
    if (n_uart == 0) {
```

```

/*
Step 1: system control configuration

step 1a: power control configuration, table 46 pg63
enable UART0 power, this is the default setting
also already done in system_LPC17xx.c
enclose the code below for reference
LPC_SC->PCONP |= BIT(3);

step 1b: select the clock source, default PCLK=CCLK/4 , where
          CCLK = 100MHZ.
tables 40 and 42 on pg56 and pg57
Check the PLL0 configuration to see how XTAL=12.0MHZ gets to CCLK
          =100MHZ
in system_LPC17xx.c file
enclose code below for reference
LPC_SC->PCLKSEL0 &= ~(BIT(7)|BIT(6)); // PCLK = CCLK/4, default
          setting after reset

Step 2: Pin Ctrl Block configuration for TXD and RXD
Listed as item #5 in LPC_17xxum UART0/2/3 manual pag298
*/
LPC_PINCON->PINSEL0 |= (1 << 4); /* Pin P0.2 used as TXD0 (Com0) */
LPC_PINCON->PINSEL0 |= (1 << 6); /* Pin P0.3 used as RXD0 (Com0) */

pUart = (LPC_UART_TypeDef *) LPC_UART0;

} else if (n_uart == 1) {
    LPC_PINCON->PINSEL4 |= (2 << 0); /* Pin P2.0 used as TXD1 (Com1) */
    LPC_PINCON->PINSEL4 |= (2 << 2); /* Pin P2.1 used as RXD1 (Com1) */

    pUart = (LPC_UART_TypeDef *) LPC_UART1;

} else {
    return -1; /* not supported yet */
}

/* Step 3: Transmission Configuration */

/* step 3a: DLAB=1, 8N1 */
pUart->LCR = UART_8N1;

/* step 3b: 115200 baud rate @ 25.0 MHZ PCLK */
pUart->DLM = 0;
pUart->DLL = 9;
pUart->FDR = 0x21; /* FR = 1.507 ~ 1/2, DivAddVal = 1, MulVal = 2 */
/* FR = 1.507 = 25MHZ/(16*9*115200) */
pUart->LCR &= ~(BIT(7)); /* disable the Division Latch Access Bit DLAB
                           =0 */

return 0;
}

```

```

/********************* / **
 * @brief: read a char from the n_uart, blocking read
***** / */

int uart_get_char(int n_uart)
{
    LPC_UART_TypeDef *pUart;

    if (n_uart == 0) {
        pUart = (LPC_UART_TypeDef *) LPC_UART0;
    } else if (n_uart == 1) {
        pUart = (LPC_UART_TypeDef *) LPC_UART1;
    } else {
        return -1; /* UART2,3 not supported yet */
    }

    /* polling the LSR RDR (Receiver Data Ready) bit to wait it is not
       empty */
    while (!(pUart->LSR & LSR_RDR));
    return (pUart->RBR);
}

/********************* / **
 * @brief: write a char c to the n_uart
***** / */

int uart_put_char(int n_uart, char c)
{
    LPC_UART_TypeDef *pUart;

    if (n_uart == 0) {
        pUart = (LPC_UART_TypeDef *) LPC_UART0;
    } else if (n_uart == 1) {
        pUart = (LPC_UART_TypeDef *) LPC_UART1;
    } else {
        return -1; // UART2,3 not supported
    }

    /* polling LSR THRE bit to wait it is empty */
    while (!(pUart->LSR & LSR_THRE));
    return (pUart->THR = c); /* write c to the THR */
}

/********************* / **
 * @brief write a string to UART
***** / */

int uart_put_string(int n_uart, char *s)
{
    if (n_uart > 1) return -1; /* only uart0, 1 are supported for now */
    while (*s != 0) { /* loop through each char in the string */
        uart_put_char(n_uart, *s++); /* print the char, then ptr increments
                                         */
    }
}

```

```

        return 0;
    }

/********************* @brief call back function for printf
 * NOTE: first parameter p is not used for now. UART1 used.
 ****/
void putc(void *p, char c)
{
    if (p != NULL) {
        uart1_put_string("putc: first parameter needs to be NULL");
    } else {
        uart1_put_char(c);
    }
}

```

Listing 8.18: UART0 Polling Code uart_polling.c

8.7 Timer Programming

To program a TIMER on MCB1700 board, one first needs to configure the TIMER by following the steps listed in Section 21.1 in [4]. Listings 8.19 and 8.20 give one sample implementation of programming TIMER0 interrupts. The timer interrupt fires every one millisecond.

```

/**
 * @brief timer.h - Timer header file
 * @author Y. Huang
 * @date 2013/02/12
 */
#ifndef _TIMER_H_
#define _TIMER_H_

extern uint32_t timer_init ( uint8_t n_timer ); /* initialize timer
   n_timer */

#endif /* ! _TIMER_H_ */

```

Listing 8.19: Timer0 IRQ Sample Code timer.h

```

/**
 * @brief timer.c - Timer example code. Timer IRQ is invoked every 1ms
 * @author T. Reidemeister
 * @author Y. Huang
 * @author NXP Semiconductors
 * @date 2012/02/12
 */

#include <LPC17xx.h>
#include "timer.h"

```

```

#define BIT(X) (1<<X)

volatile uint32_t g_timer_count = 0; // increment every 1 ms

/***
 * @brief: initialize timer. Only timer 0 is supported
 */
uint32_t timer_init(uint8_t n_timer)
{
    LPC_TIM_TypeDef *pTimer;
    if (n_timer == 0) {
        /*
        Steps 1 & 2: system control configuration.
        Under CMSIS, system_LPC17xx.c does these two steps

        -----
        Step 1: Power control configuration.
        See table 46 pg63 in LPC17xx_UM
        -----
        Enable UART0 power, this is the default setting
        done in system_LPC17xx.c under CMSIS.
        Enclose the code for your refrence
        //LPC_SC->PCOMP |= BIT(1);

        -----
        Step2: Select the clock source,
        default PCLK=CCLK/4 , where CCLK = 100MHZ.
        See tables 40 & 42 on pg56-57 in LPC17xx_UM.
        -----
        Check the PLL0 configuration to see how XTAL=12.0MHZ
        gets to CCLK=100MHZ in system_LPC17xx.c file.
        PCLK = CCLK/4, default setting in system_LPC17xx.c.
        Enclose the code for your reference
        //LPC_SC->PCLKSEL0 &= ~(BIT(3)|BIT(2));

        -----
        Step 3: Pin Ctrl Block configuration.
        Optional, not used in this example
        See Table 82 on pg110 in LPC17xx_UM
        -----
    */
    pTimer = (LPC_TIM_TypeDef *) LPC_TIM0;

} else /* other timer not supported yet */
    return 1;
}

/*
-----
Step 4: Interrupts configuration
-----
*/

```

```

/* Step 4.1: Prescale Register PR setting
   CCLK = 100 MHZ, PCLK = CCLK/4 = 25 MHZ
   2*(12499 + 1)*(1/25) * 10^(-6) s = 10^(-3) s = 1 ms
   TC (Timer Counter) toggles b/w 0 and 1 every 12500 PCLKs
   see MR setting below
*/
pTimer->PR = 12499;

/* Step 4.2: MR setting, see section 21.6.7 on pg496 of LPC17xx_UM. */
pTimer->MR0 = 1;

/* Step 4.3: MCR setting, see table 429 on pg496 of LPC17xx_UM.
   Interrupt on MR0: when MR0 matches the value in the TC,
   generate an interrupt.
   Reset on MR0: Reset TC if MR0 matches it.
*/
pTimer->MCR = BIT(0) | BIT(1);

g_timer_count = 0;

/* Step 4.4: CMSIS enable timer0 IRQ */
NVIC_EnableIRQ(TIMER0_IRQn);

/* Step 4.5: Enable the TCR. See table 427 on pg494 of LPC17xx_UM. */
pTimer->TCR = 1;

return 0;
}

/***
* @brief: use CMSIS ISR for TIMER0 IRQ Handler
* NOTE: This example shows how to save/restore all registers rather than
*       just
*       those backed up by the exception stack frame. We add extra
*       push and pop instructions in the assembly routine.
*       The actual c_TIMER0_IRQHandler does the rest of irq handling
*/
__asm void TIMER0_IRQHandler(void)
{
    PRESERVE8
    IMPORT c_TIMER0_IRQHandler
    PUSH{r4-r11, lr}
    BL c_TIMER0_IRQHandler
    POP{r4-r11, pc}
}

/***
* @brief: c TIMER0 IRQ Handler
*/
void c_TIMER0_IRQHandler(void)
{
    /* ack interrupt, see section 21.6.1 on pg 493 of LPC17XX_UM */
    LPC_TIM0->IR = BIT(0);

    g_timer_count++ ;
}

```

```
}
```

Listing 8.20: Timer0 IRQ Sample Code timer.c

Chapter 9

Keil MCB1700 Hardware Environment

9.1 MCB1700 Board Overview

The Keil MCB1700 board is populated with NXP *LPC1768* Microcontroller. Figure 9.1 shows the important interface and hardware components of the MCB1700 board.

Figure 9.2 is the hardware block diagram that helps you to understand the MCB1700 board components. Note that our lab will only use a small subset of the components which include the LPC1768 CPU, COM and Dual RS232.

The LPC1768 is a 32-bit ARM Cortex-M3 microcontroller for embedded applications requiring a high level of integration and low power dissipation. The LPC1768 operates at up to an 100 MHz CPU frequency. The peripheral complement of LPC1768 includes 512KB of on-chip flash memory, 64KB of on-chip SRAM and a variety of other on-chip peripherals. Among the on-chip peripherals, there are system control block, pin connect block, 4 UARTs and 4 general purpose timers, some of which will be used in your RTX course project. Figure 9.3 is the simplified LPC1768 block diagram [4], where the components to be used in your RTX project are circled with red. Note that this manual will only discuss the components that are relevant to the RTX course project. The LPC17xx User Manual is the complete reference for LPC1768 MCU.

9.2 Cortex-M3 Processor

The Cortex-M3 processor is the central processing unit (CPU) of the LPC1768 chip. The processor is a 32-bit microprocessor with a 32-bit data path, a 32-bit register bank, and 32-bit memory interfaces. Figure 9.4 is the simplified block diagram of the Cortex-M3 processor [5]. The processor has private peripherals which are system control block, system timer, NVIC (Nested Vectored Interrupt Controller) and MPU (Memory Protection Unit). The processor includes a number of internal debugging components which provides debugging features such as breakpoints and

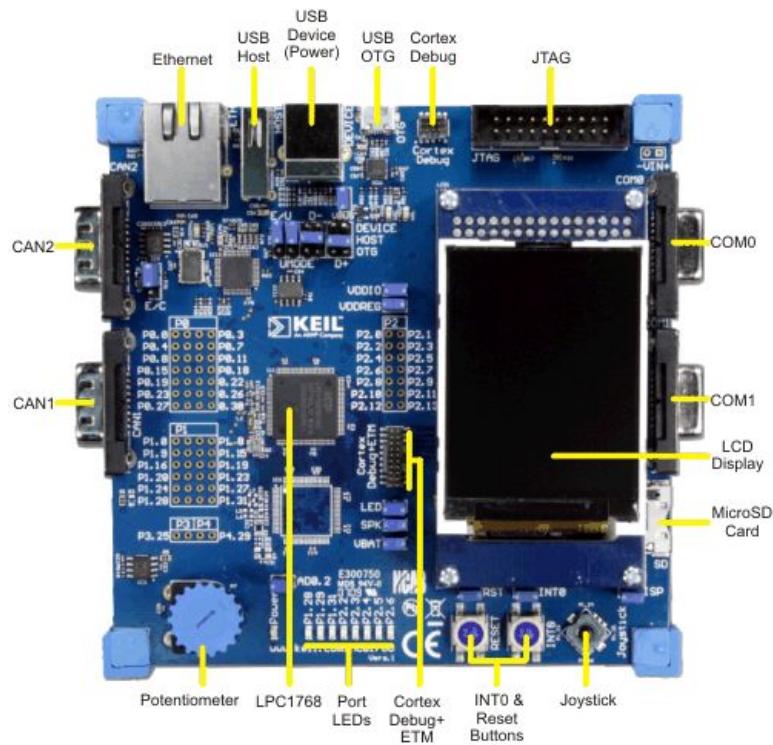


Figure 9.1: MCB1700 Board Components [2]

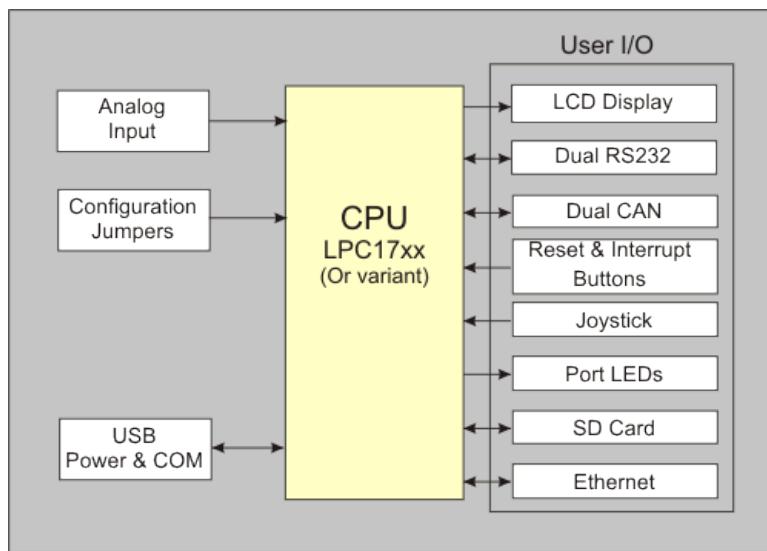


Figure 9.2: MCB1700 Board Block Diagram [2]

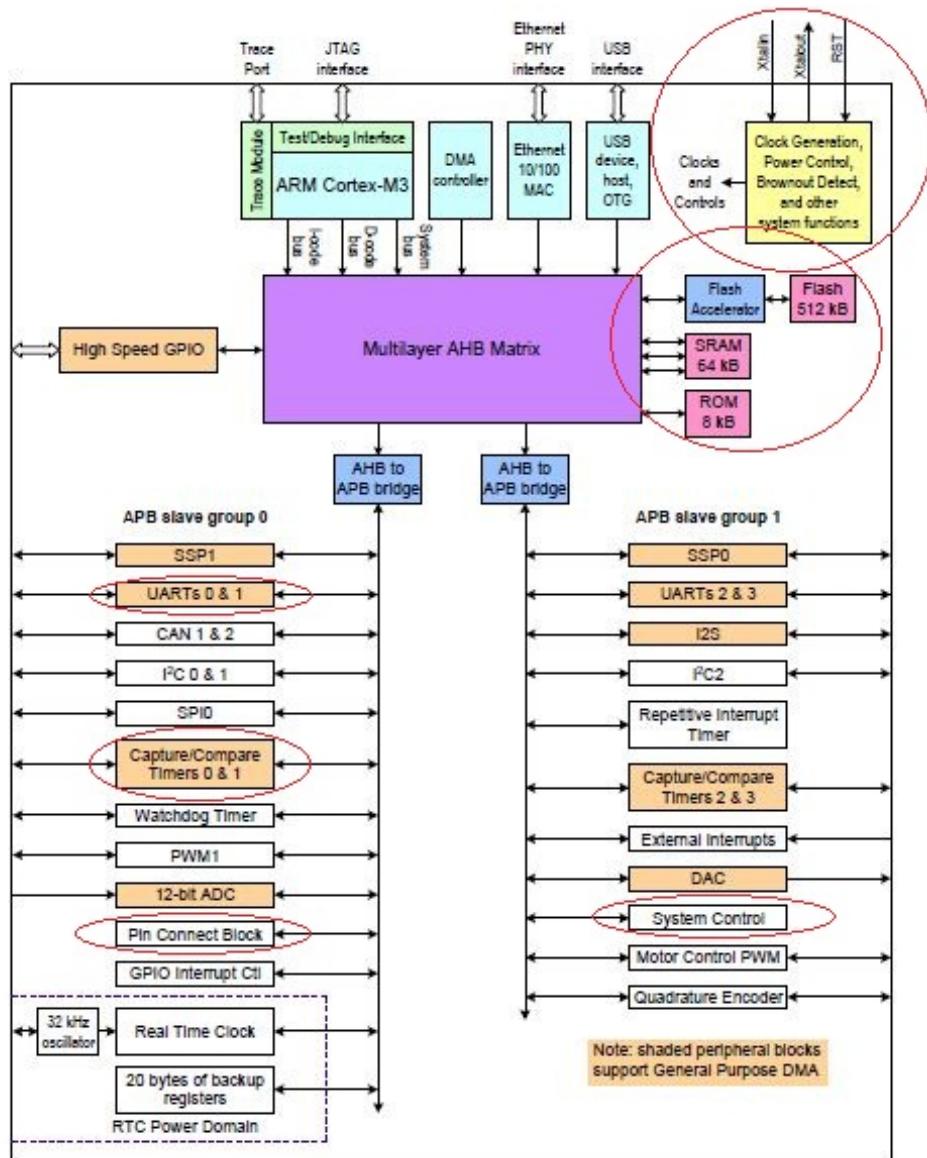


Figure 9.3: LPC1768 Block Diagram. The circled blocks are the ones that we will use in the lab project.

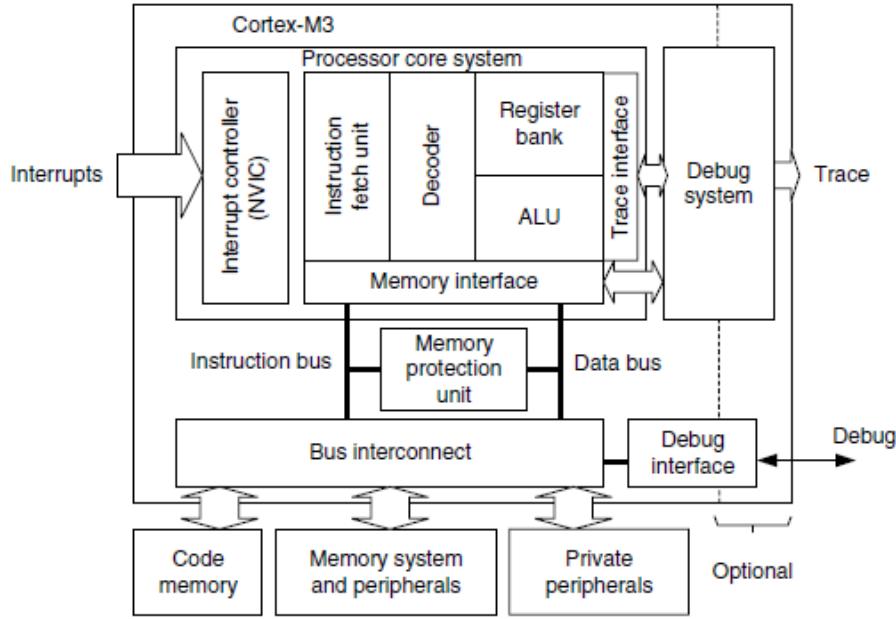


Figure 9.4: Simplified Cortex-M3 Block Diagram[5]

watchpoints.

9.2.1 Registers

The processor core registers are shown in Figure 9.5. For detailed description of each register, Chapter 34 in [4] is the complete reference.

- R0-R12 are 32-bit general purpose registers for data operations. Some 16-bit Thumb instructions can only access the low registers (R0-R7).
- R13(SP) is the stack pointer alias for two banked registers shown as follows:
 - *Main Stack Pointer (MSP)*: This is the default stack pointer and also reset value. It is used by the OS kernel and exception handlers.
 - *Process Stack Pointer (PSP)*: This is used by user application code.

On reset, the processor loads the MSP with the value from address 0x00000000. The lowest 2 bits of the stack pointers are always 0, which means they are always word aligned.

In Thread mode, when bit[1] of the CONTROL register is 0, MSP is used. When bit[1] of the CONTROL register is 1, PSP is used.

- R14(LR) is the link register. The return address of a subroutine is stored in the link register when the subroutine is called.
- R15(PC) is the program counter. It can be written to control the program flow.

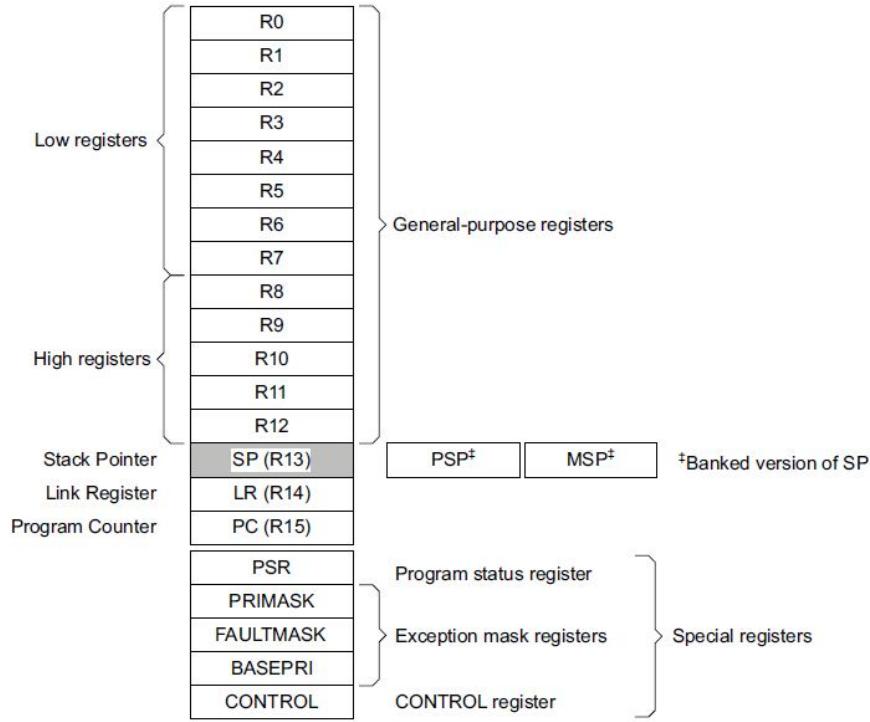


Figure 9.5: Cortex-M3 Registers[4]

- Special Registers are as follows:
 - Program Status registers (PSRs)
 - Interrupt Mask registers (PRIMASK, FAULTMASK, and BASEPRI)
 - Control register (CONTROL)

When at privilege level, all the registers are accessible. When at unprivileged (user) level, access to these registers are limited.

9.2.2 Processor mode and privilege levels

The Cortex-M3 processor supports two modes of operation, Thread mode and Handler mode.

- Thread mode is entered upon Reset and is used to execute application software.
- Handler mode is used to handle exceptions. The processor returns to Thread mode when it has finished exception handling.

Software execution has two access levels, Privileged level and Unprivileged (User) level.

- Privileged

The software can use all instructions and has access to all resources. Your RTOS kernel functions are running in this mode.

- Unprivileged (User)

The software has limited access to MSR and MRS instructions and cannot use the CPS instruction. There is no access to the system timer, NVIC , or system control block. The software might also have restricted access to memory or peripherals. User processes such as the wall clock process should run at this level.

When the processor is in Handler mode, it is at the privileged level. When the processor is in Thread mode, it can run at privileged or unprivileged (user) level. The bit[0] in CONTROL register determines the execution privilege level in Thread mode. When this bit is 0 (default), it is privileged level when in Thread mode. When this bit is 1, it is unprivileged when in Thread mode. Figure 9.6 illustrate the mode and privilege level of the processor.

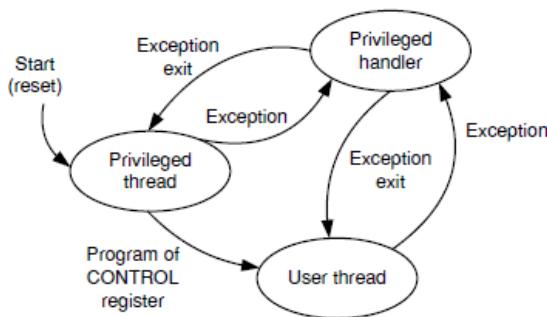


Figure 9.6: Cortex-M3 Operating Mode and Privilege Level[5]

Note that only privileged software can write to the CONTROL register to change the privilege level for software execution in Thread mode. Unprivileged software can use the SVC instruction to make a supervisor call to transfer control to privileged software. When we are in the privileged thread mode, we can directly set the control register to change to unprivileged thread mode. We also can change to unprivileged thread mode by calling SVC to raise an exception first and then inside the exception handler we set the privilege level to unprivileged by setting the control register. Then we modify the EXC_RETURN value in the LR (R14) to indicate the mode and stack when returning from an exception. This mechanism is often used by the kernel in its initialization phase and also context switching between privileged processes and unprivileged processes.

9.2.3 Stacks

The processor uses a full descending stack. This means the stack pointer indicates the last stacked item on the stack memory. When the processor pushes a new item onto the stack, it decrements the stack pointer and then writes the item to the new memory location.

The processor implements two stacks, the *main stack* and the *process stack*. One of these two stacks is banked out depending on the stack in use. This means only one stack is visible at a time as R13. In Handler mode, the main stack is always used. The bit[1] in CONTROL register reads as zero and ignores writes in Handler mode. In Thread mode, the bit[1] setting in CONTROL register determines whether the main stack or the process stack is currently used. Table 9.1 summarizes the processor mode, execution privilege level, and stack use options.

Processor mode	Used to execute	Privilege level for software execution	CONTROL Bit[0]	CONTROL Bit[1]	Stack used
Thread	Applications	Privileged	0	0	Main Stack
		Privileged	0	1	Process Stack
		Unprivileged	1	1	Process Stack
Handler	Exception handlers	Privileged	-	0	Main Stack

Table 9.1: Summary of processor mode, execution privilege level, and stack use options

9.3 Memory Map

The Cortex-M3 processor has a single fixed 4GB address space. Table 9.2 shows how this space is used on the LPC1768.

Address Range	General Use	Address range details	Description
0x0000 0000 to 0x1FFF FFFF	On-chip non-volatile memory	0x0000 0000 – 0x0007 FFFF	512 KB flash memory
	On-chip SRAM	0x1000 0000 – 0x1000 7FFF	32 KB local SRAM
	Boot ROM	0x1FFF 0000 – 0x1FFF 1FFF	8 KB Boot ROM
0x2000 0000 to 0x3FFF FFFF	On-chip SRAM (typically used for peripheral data)	0x2007 C000 – 0x2007 FFFF	AHB SRAM - bank0 (16 KB)
		0x2008 0000 – 0x2008 3FFF	AHB SRAM - bank1 (16 KB)
	GPIO	0x2009 C000 – 0x2009 FFFF	GPIO
0x4000 0000 to 0x5FFF FFFF	APB Peripherals	0x4000 0000 – 0x4007 FFFF	APB0 Peripherals
	AHB peripherals	0x4008 0000 – 0x400F FFFF	APB1 Peripherals
0xE000 0000 to 0xE00F FFFF	Cortex-M3 Private Peripheral Bus (PPB)	0xE000 0000 – 0xE00F FFFF	Cortex-M3 private registers(NVIC, MPU and SysTick Timer et. al.)

Table 9.2: LPC1768 Memory Map

Note that the memory map is not continuous. For memory regions not shown in the table, they are reserved. When accessing reserved memory region, the processor's behavior is not defined. All the peripherals are memory-mapped and the

LPC17xx.h file defines the data structure to access the memory-mapped peripherals in C.

9.4 Exceptions and Interrupts

The Cortex-M3 processor supports system exceptions and interrupts. The processor and the Nested Vectored Interrupt Controller (NVIC) prioritize and handle all exceptions. The processor uses *Handler mode* to handle all exceptions except for reset.

9.4.1 Vector Table

Exceptions are numbered 1-15 for system exceptions and 16 and above for external interrupt inputs. LPC1768 NVIC supports 35 vectored interrupts. Table 9.3 shows system exceptions and some frequently used interrupt sources. See Table 50 and Table 639 in [4] for the complete exceptions and interrupts sources. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR (within the System Control Block) to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80.

Exception number	IRQ number	Vector address or offset	Exception type	Priority	C PreFix
1	-	0x00000004	Reset	-3, the highest	
2	-14	0x00000008	NMI	-2,	NMI_-
3	-13	0x0000000C	Hard fault	-1	HardFault_-
4	-12	0x00000010	Memory management fault	Configurable	MemManage_-
:					
11	-5	0x0000002C	SVCall	Configurable	SVC_-
:					
14	-2	0x00000038	PendSV	Configurable	PendSVC_-
15	-1	0x0000003C	SysTick	Configurable	SysTick_-
16	0	0x00000040	WDT	Configurable	WDT_IRQ
17	1	0x00000044	Timer0	Configurable	TIMER0_IRQ
18	2	0x00000048	Timer1	Configurable	TIMER1_IRQ
19	3	0x0000004C	Timer2	Configurable	TIMER2_IRQ
20	4	0x00000050	Timer3	Configurable	TIMER3_IRQ
21	5	0x00000054	UART0	Configurable	UART0_IRQ
22	6	0x00000058	UART1	Configurable	UART1_IRQ
23	7	0x0000005C	UART2	Configurable	UART2_IRQ
24	8	0x00000060	UART3	Configurable	UART3_IRQ
:					

Table 9.3: LPC1768 Exception and Interrupt Table

9.4.2 Exception Entry

Exception entry occurs when there is a pending exception with sufficient priority and either

- the processor is in Thread mode
- the processor is in Handler mode and the new exception is of higher priority than the exception being handled, in which case the new exception preempts the original exception (This is the nested exception case which is not required in our RTOS lab).

When an exception takes place, the following happens

- Stacking

When the processor invokes an exception (except for tail-chained or a late-arriving exception, which are not required in the RTOS lab), it automatically stores the following eight registers to the SP:

- R0-R3, R12
- PC (Program Counter)
- PSR (Processor Status Register)
- LR (Link Register, R14)

Figure 9.7 shows the exception stack frame. Note that by default the stack frame is aligned to double word address starting from Cortex-M3 revision 2. The alignment feature can be turned off by programming the STKALIGN bit in the System Control Block (SCB) Configuration Control Register (CCR) to 0. On exception entry, the processor uses bit[9] of the stacked PSR to indicate the stack alignment. On return from the exception, it uses this stacked bit to restore the correct stack alignment.

- Vector Fetching

While the data bus is busy stacking the registers, the instruction bus fetches the exception vector (the starting address of the exception handler) from the vector table. The stacking and vector fetch are performed on separate bus interfaces, hence they can be carried out at the same time.

- Register Updates

After the stacking and vector fetch are completed, the exception vector will start to execute. On entry of the exception handler, the following registers will be updated as follows:

- SP: The SP (MSP or PSP) will be updated to the new location during stacking. Stacking from the privileged/unprivileged thread to the first level of the exception handler uses the MSP/PSP. During the execution of exception handler routine, the MSP will be used when stack is accessed.

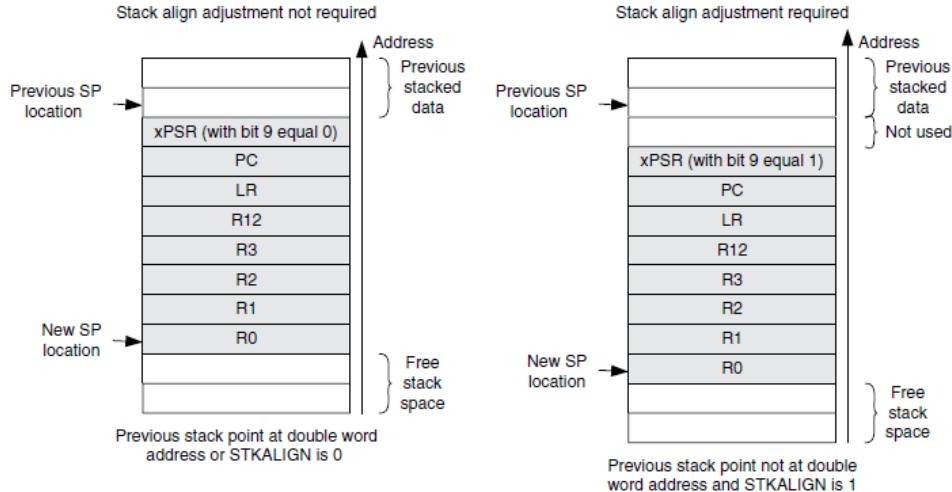


Figure 9.7: Cortex-M3 Exception Stack Frame [5]

- PSR: The IPSR will be updated to the new exception number
- PC: The PC will change to the vector handler when the vector fetch completes and starts fetching instructions from the exception vector.
- LR: The LR will be updated to a special value called EXC_RETURN. This indicates which stack pointer corresponds to the stack frame and what operation mode the processor was in before the exception entry occurred.
- Other NVIC registers: a number of other NVIC registers will be updated. For example the pending status of exception will be cleared and the active bit of the exception will be set.

9.4.3 EXC_RETURN Value

EXC_RETURN is the value loaded into the LR on exception entry. The exception mechanism relies on this value to detect when the processor has completed an exception handler. The EXC_RETURN bits [31 : 4] is always set to 0xFFFFFFFF by the processor. When this value is loaded into the PC, it indicates to the processor that the exception is complete and the processor initiates the exception return sequence. Table 9.4 describes the EXC_RETURN bit fields. Table 9.5 lists Cortex-M3 allowed EXC_RETURN values.

Bits	31:4	3	2	1	0
Description	0xFFFFFFFF	Return mode (Thread/Handler)	Return stack	Reserved; must be 0	Process state (Thumb/ARM)

Table 9.4: EXC_RETURN bit fields [5]

Value		Description	
	Return Mode	Exception return gets state from	SP after return
0xFFFFFFF1	Handler	MSP	MSP
0xFFFFFFF9	Thread	MSP	MSP
0xFFFFFFFFD	Thread	PSP	PSP

Table 9.5: EXC_RETURN Values on Cortex-M3

9.4.4 Exception Return

Exception return occurs when the processor is in Handler mode and executes one of the following instructions to load the EXC_RETURN value into the PC:

- a POP instruction that includes the PC. This is normally used when the EXC_RETURN in LR upon entering the exception is pushed onto the stack.
- a BX instruction with any register. This is normally used when LR contains the proper EXC_RETURN value before the exception return, then BX LR instruction will cause an exception return.
- a LDR or LDM instruction with the PC as the destination. This is another way to load PC with the EXC_RETURN value.

Note unlike the ColdFire processor which has the RTE as the special instruction for exception return, in Cortex-M3, a normal return instruction is used so that the whole interrupt handler can be implemented as a C subroutine.

When the exception return instruction is executed, the following exception return sequences happen:

- Unstacking: The registers (i.e. exception stack frame) pushed to the stack will be restored. The order of the POP will be the same as in stacking. The SP will also be changed back.
- NVIC register update: The active bit of the exception will be cleared. The pending bit will be set again if the external interrupt is still asserted, causing the processor to reenter the interrupt handler.

9.5 Data Types

The processor supports 32-bit words, 16-bit halfwords and 8-bit bytes. It supports 64-bit data transfer instructions. All data memory accesses are managed as little-endian.

Appendix A

The Debugger Initialization Files

The SIM.ini file in the starter code can be found in Listing A.1. The simulator by default does not detect the second bank of RAM (i.e. IRAM2 in the Target page of the Target option window), which starts 0x2007C000 and ends at 0x20083FFF. We use the MAP command to specify the memory access rights of this range of memory.

```
MAP 0x2007C000, 0x20083FFF READ WRITE // set up IRAM2 memory access
```

Listing A.1: The SIM.ini file

The RAM.ini file in the starter code can be found in Listing A.2. It relocates the vector table to RAM and load the code for in-memory execution (i.e. not to the ROM). This will avoid wear-and-tear on the on-chip flash memory.

```
FUNC void Setup (void) {
    SP = _DWORD(0x10000000); // Setup Stack Pointer
    PC = _DWORD(0x10000004); // Setup Program Counter
    XPSR = 0x01000000; // Set Thumb bit
    _DWORD(0xE000ED08, 0x10000000); // Setup Vector Table Offset Register
    _DWORD(0x400FC0C4, _DWORD(0x400FC0C4) | 1<<12); // Enable ADC Power
    _DWORD(0x40034034, 0x00000F00); // Setup ADC Trim
}
LOAD %L INCREMENTAL // Download

Setup(); // Setup for Running
g, main
```

Listing A.2: The RAM.ini file

Appendix B

Forms

ECE350 Lab forms are given in this appendix. They are

- Group Sign-up Declaration Form
- Leave a Group Form
- Meeting Copyright Form

These forms are also available on LEARN under Contents → Labs → Forms

ECE350 Group Sign-up Declaration Form

By signing the form, we affirm our agreement to the following statements:

1. Forming this project group will not cause any conflicts with other classes/labs.
2. Every member in this group can present themselves at the same time for an hour in one of the scheduled lab demo sessions without causing any conflicts with other classes/labs.
3. We will not use attending ECE350 lab session(s) as the reason to be absent from other classes/labs or seek absence permission from instructors of other classes/labs.
4. We understand violation of foregoing items 1 or 2 or 3 will result a zero grade in P4 for all group members.

Group Name*			
Name	Quest ID**	Signature	Date

*Group Name is listed on LEARN. Examples are “AM LAB Group 99” and “PM LAB Group 99”.

**Quest ID is your UW username. For example, “j128doe”.

ECE350 Request to Leave a Project Group Form

Name	
Quest ID	
Student ID	
Lab Project ID	
Group Name	

Provide the reason for leaving the project group here:

Signature

Date

ECE350 Meeting Copyright Form

The University of Waterloo subscribes to the strictest interpretation of academic integrity. Students who engage in academic dishonesty will be subject to disciplinary action under Policy 71.

This meeting involves viewing private test suites. It is protected by copyright. Reproduction or dissemination of this meeting or the contents or format of this meeting in any manner whatsoever (e.g., sharing the content with other students), without the express permission of the instructor, is strictly prohibited.

I confirm that I will keep the content of this meeting confidential.

Student Name (by signing or typing my name here I affirm my agreement to the foregoing statements)

Student ID

Date

Bibliography

- [1] Arm compiler v5.06 for uvision armcc user guide.
<https://www.keil.com/support/man/docs/armcc/default.htm>.
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- [4] LPC17xx User Manual, Rev2.0, 2010.
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