

ECE 350

Laboratory Project Manual for

Real-Time Operating Systems

by

Yiqing Huang
Seyed M. Zahedi

Electrical and Computer Engineering Department
University of Waterloo

Waterloo, Ontario, Canada, September 13, 2020

© Y. Huang and S.M. Zahedi 2020 - 2021

Contents

| | |
|--|-----|
| List of Tables | v |
| List of Figures | vii |
| Preface | 1 |
| | |
| I Lab Administration | 1 |
| | |
| II Lab Project | 6 |
| | |
| 1 Introduction | 7 |
| 1.1 Overview | 7 |
| 1.2 Summary of RTX Requirements | 7 |
| 1.2.1 RTX Primitives and Services | 7 |
| 1.2.2 RTX Tasks | 8 |
| 1.2.3 RTX Footprint and Processor Loading | 8 |
| 1.2.4 Error Detection and Recovery | 9 |
| | |
| 2 Lab1 Introduction to Kernel Programming and Memory Management | 10 |
| 2.1 Objective | 10 |
| 2.2 Starter Files | 10 |
| 2.3 Pre-lab Preparation | 11 |
| 2.4 Assignment | 11 |
| 2.4.1 Programming Project | 11 |
| 2.4.2 Report | 15 |
| 2.4.3 Third-party Testing and Source Code File Organization | 15 |

| | |
|---|-----------|
| 2.5 Deliverable | 16 |
| 2.5.1 Pre-Lab Deliverables | 16 |
| 2.5.2 Post-Lab Deliverables | 16 |
| 3 Lab2 Task Management | 17 |
| 4 Lab3 Synchronization and Console I/O | 18 |
| 5 Lab4 Timing Service and Real-Time Scheduling | 19 |
| 6 Lab5 Memory Protection and Stress Testing | 20 |

III Software Development Environment Quick Reference Guide

21

| | |
|---|-----------|
| 7 Keil MCB1700 Hardware Environment | 22 |
| 7.1 MCB1700 Board Overview | 22 |
| 7.2 Cortex-M3 Processor | 22 |
| 7.2.1 Registers | 25 |
| 7.2.2 Processor mode and privilege levels | 26 |
| 7.2.3 Stacks | 27 |
| 7.3 Memory Map | 28 |
| 7.4 Exceptions and Interrupts | 29 |
| 7.4.1 Vector Table | 29 |
| 7.4.2 Exception Entry | 30 |
| 7.4.3 EXC_RETURN Value | 31 |
| 7.4.4 Exception Return | 32 |
| 7.5 Data Types | 32 |
| 8 Keil Software Development Tools | 33 |
| 8.1 Creating an Application in uVision5 IDE | 33 |
| 8.1.1 Getting Starter Code from the GitHub | 33 |
| 8.1.2 Create a New Project | 34 |
| 8.1.3 Managing Project Components | 34 |
| 8.1.4 Build the Application | 38 |

| | | |
|-------------------|--|-----------|
| 8.2 | Debug the Target | 41 |
| 8.2.1 | Debug the Project in Simulator | 41 |
| 8.2.2 | Debug the Project on the Board | 44 |
| 8.3 | Download to ROM | 49 |
| 9 | Programming MCB1700 | 51 |
| 9.1 | The Thumb-2 Instruction Set Architecture | 51 |
| 9.2 | ARM Architecture Procedure Call Standard (AAPCS) | 51 |
| 9.3 | Cortex Microcontroller Software Interface Standard (CMSIS) | 53 |
| 9.3.1 | CMSIS files | 54 |
| 9.3.2 | Cortex-M Core Peripherals | 55 |
| 9.3.3 | System Exceptions | 55 |
| 9.3.4 | Intrinsic Functions | 57 |
| 9.3.5 | Vendor Peripherals | 57 |
| 9.4 | Accessing C Symbols from Assembly | 58 |
| 9.5 | SVC Programming: Writing an RTX API Function | 59 |
| 9.6 | UART Programming | 61 |
| 9.7 | Timer Programming | 72 |
| A | Forms | 75 |
| B | The RAM.ini File | 77 |
| References | | 78 |

List of Tables

| | | |
|-----|--|----|
| 0.1 | Project Deliverable Weight and Deadlines. Replace the “id” in “Gid” with the two digit group ID number. | 3 |
| 0.2 | Group Project contribution factor table. Each student’s lab grade is their group project grade multiplied by the CF (Contribution Factor). | 4 |
| 7.1 | Summary of processor mode, execution privilege level, and stack use options | 28 |
| 7.2 | LPC1768 Memory Map | 28 |
| 7.3 | LPC1768 Exception and Interrupt Table | 29 |
| 7.4 | EXC_RETURN bit fields | 31 |
| 7.5 | EXC_RETURN Values on Cortex-M3 | 32 |
| 9.1 | Assembler instruction examples | 52 |
| 9.2 | Core Registers and AAPCS Usage | 53 |
| 9.3 | CMSIS intrinsic functions | 57 |

List of Figures

| | | |
|------|---|----|
| 7.1 | MCB1700 Board Components | 23 |
| 7.2 | MCB1700 Board Block Diagram | 23 |
| 7.3 | LPC1768 Block Diagram | 24 |
| 7.4 | Simplified Cortex-M3 Block Diagram | 25 |
| 7.5 | Cortex-M3 Registers | 26 |
| 7.6 | Cortex-M3 Operating Mode and Privilege Level | 27 |
| 7.7 | Cortex-M3 Exception Stack Frame | 31 |
| 8.1 | Keil IDE: Create a New Project | 34 |
| 8.2 | Keil IDE: Choose MCU | 35 |
| 8.3 | Keil IDE: Manage Run-Time Environment | 35 |
| 8.4 | Keil IDE: A default new project | 36 |
| 8.5 | Keil IDE: Add Group | 36 |
| 8.6 | Keil IDE: Updated Project Profile | 37 |
| 8.7 | Keil IDE: Add Source File to Source Group | 37 |
| 8.8 | Keil IDE: Updated Project Profile | 38 |
| 8.9 | Keil IDE: Create New File | 38 |
| 8.10 | Keil IDE: Final Project Setting | 38 |
| 8.11 | Keil IDE: Target Options Configuration | 39 |
| 8.12 | Keil IDE: Target Options C/C++ Tab Configuration | 39 |
| 8.13 | Keil IDE: Target Options Target Tab Configuration | 40 |
| 8.14 | Keil IDE: Target Options Linker Tab Configuration | 40 |
| 8.15 | Keil IDE: Build Target | 41 |
| 8.16 | Keil IDE: Build Target | 41 |
| 8.17 | Keil IDE: Target Options Debug Tab Configuration | 42 |
| 8.18 | Keil IDE: Debug Button | 42 |

| | | |
|------|---|----|
| 8.19 | Keil IDE: Debugging. Enable Serial Window View. | 42 |
| 8.20 | Keil IDE: Debugging. Both UART0 and UART1 views are enabled in simulator. | 43 |
| 8.21 | Keil IDE: Debugging. The Run Button. | 43 |
| 8.22 | Keil IDE: Debugging Output. | 44 |
| 8.23 | Keil IDE: Manage Project Items Button | 45 |
| 8.24 | Keil IDE: Manage Project Items Window. | 45 |
| 8.25 | Keil IDE: Select HelloWorld RAM Target. | 46 |
| 8.26 | Keil IDE: Configure Target Options Target Tab for In-memory Execution. | 46 |
| 8.27 | Keil IDE: Configure ULINK-ME Hardware Debugger. | 47 |
| 8.28 | Keil IDE: Flash Download Programming Algorithm Configuration. | 47 |
| 8.29 | Device Manger COM Ports | 48 |
| 8.30 | PuTTY Session for Serial Port Communication | 48 |
| 8.31 | PuTTY Serial Port Configuration | 48 |
| 8.32 | PuTTY Output | 49 |
| 8.33 | Flash Download Reset and Run Setting | 50 |
| 8.34 | Keil IDE: Download Target to Flash | 50 |
| 9.1 | Role of CMSIS | 54 |
| 9.2 | CMSIS Organization | 55 |
| 9.3 | CMSIS Organization | 56 |
| 9.4 | CMSIS NVIC Functions | 56 |
| 9.5 | SVC as a Gateway for OS Functions [5] | 59 |

Preface

Who Should Read This Lab Manual?

This lab manual is written for students who will design and implement a small Real-Time Executive (RTX) for Keil MCB1700 board populated with an NXP LPC1768 microcontroller.

What is in This Lab Manual?

The first purpose of this document is to provide the descriptions and notes for the laboratory project. The second purpose of this document is a quick reference guide of the relevant development tools for completing laboratory projects. This manual is divided into three parts.

Part I describes the lab administration policies.

Part II is the project description. We break the project into the following five laboratory projects.

- P1: Introduction to Kernel Programming and Memory Management
- P2: Task Management
- P3: Synchronization and Console I/O
- P4: Timing Service and Real-Time Scheduling
- P5: Memory Protection and Stress Testing

Part III introduces the computing environment and the development tools. It includes a Keil MCB 1700 hardware and software reference guide. The topics are as follows.

- Windows 10 Remote Desktop
- Keil MCB1700 Hardware Environment
- Keil Software Development Tools
- Programming MCB1700

Acknowledgments

Our project is inspired by the original ECE354 RTX course project created by Professor Paul Dasiewicz. Professor Dasiewicz provided detailed notes and sample code to us. We sincerely thank ARM University Program for providing us with lab teaching materials and development software licenses. We also own many thanks to our students who did ECE354 and SE350 course projects in the past and provided constructive feedback. Professor Sebastian Fischmeister made the Keil Boards donations possible. Our gratitude also goes out to Eric Praetzel supports the IT infrastructure of RTOS lab hardware and the ARM-MDK software.

Part I

Lab Administration

Lab Administration Policy

Group Lab Policy

- **Group Size.** All labs are done in groups of *four*. A group size of less than four is not recommended. There is no reduction in project deliverables regardless the size of the project group. The Learn system (<http://learn.uwaterloo.ca>) is used to signup for groups. The lab group sign-up is due by 8:30 am on Monday of the second academic week (see Table 0.1). Late group sign-up is not accepted and will result in losing the entire lab sign-up mark, which is 2% of the total lab project grade. Grace days do not apply to Group Sign-up. Any student without a lab group after the sign-up deadline will be randomly assigned to a lab group by the lab teaching staff.
- **Group Project Manager.** The group elects one member as the group project manager. The project manager can be the same person for all deliverables or a different person for a different deliverable. Rotating project manager's role gives each group member an opportunity to practice group project management. However this role rotation is a choice rather than requirement. It is up to the group to decide.
- **Quitting from a Group.** If you notice workload imbalance, try to solve it as soon as possible within your group. Quitting from the group should be used as the last resort. Group quitting is only allowed once. You are allowed to join another group which has three or less number of students. You are not allowed to quit from the newly formed group again. There is *one grace day deduction penalty* to be applied to each member in the old group. We highly recommend everyone to stay with your group members as much as possible, for the ability to do team work will be an important skill in your future career. Please choose your lab partners carefully and wisely. The code and documentation completed before the group split-up are the intellectual property of each students in the old group.
- **Group Quitting Deadline.** To quit from your group, you need to notify the lab instructor in writing and sign the group split-up form (see the Appendix A) at least one week before the nearest lab project deadline.

| Deliverable | Weight | Due Date | File Name |
|---------------------------------------|---------------|-----------------|------------------|
| P0 Group Sign-up | 2 % | 08:30 Sep 14 | |
| P1 Memory Management | 18 % | 20:30 Sep 25 | p1_Gid.zip |
| P2 Task Management | 20 % | 20:30 Oct 09 | p2_Gid.zip |
| P3 Synchronization and Console I/O | 25 % | 20:30 Nov 02 | p3_Gid.zip |
| P4 Timing and Real-Time Scheduling | 20 % | 20:30 Nov 16 | p4_Gid.zip |
| P5 Memory Protection and Stress Tests | 15 % | 20:30 Nov 30 | p5_Gid.zip |

Table 0.1: Project Deliverable Weight and Deadlines. Replace the “id” in “Gid” with the two digit group ID number.

Lab Project Submission and Grading Policy.

- **Project Deliverables.** The lab project is divided into five deliverables. For each deliverable, there is a pre-lab deliverable and a post-lab deliverable.

Students are required to finish the pre-lab deliverable before attempting the lab assignments. For the terms we have scheduled lab sessions, pre-lab is due by the time your scheduled lab session starts. For the terms we do not have scheduled lab sessions, pre-lab is due by the deadline of the previous lab’s post-lab.

Each post-lab deliverable includes the source code and a lab report (in pdf) file. Create a directory and name it “labN”, where N is 1, 2, ..., 5. Create a sub-directory named “code”. Put your uVision 5 application folder under the code directory. Name your lab report file “pN_report.pdf”, where N is 1, 2, ..., N and put it under labN directory. Include a README file with group identification, project manager name and a description of directory contents. Put the README file under labN directory. Archive all files for each deliverable in a single file and submit it to the corresponding Learn Dropbox. Table 0.1 gives the weight, deadline and naming convention of each post-lab deliverable.

- **Project Grading.** Submissions will be evaluated on the board connected to a Microsoft Windows 10 lab machine. Lab machines are accessible through [ENGLab remote desktop session](#) when connected to the campus virtual private network ([VPN](#)). A 15% penalty will be applied to a deliverable that is only able to function inside the simulator but not on the actual hardware.

For each deliverable, we will conduct an anonymous peer review within a group. A student will rate how satisfied he/she is with every other group member’s contribution from 0 to 10, where the higher the rating, the more satisfied the student feels about the contribution the other member has done for the project. This is to make sure everyone in the group will contribute their fair share to the project. We will use simple arithmetic average ratings each group member received and assign individual lab grade to each team member

| Peer Rating | Contribution Factor CF |
|-------------|------------------------|
| [8, 10] | 100% |
| [7, 8) | 80% |
| [6, 7) | 60% |
| [4, 6) | 40% |
| [0, 4) | 0% |

Table 0.2: Group Project contribution factor table. Each student's lab grade is their group project grade multiplied by the CF (Contribution Factor).

by multiplying the project grade with a contribution percentage factor listed in Table 0.2.

- **Project Re-grading.** To initiate a re-grading process, contact the grading TA in charge first. The re-grading is a rigid process. The entire project will be re-graded. Your new grades may be lower, unchanged or higher than the original grade received. If you are still not satisfied with the grades received after the re-grading, escalate your case to the lab instructor to request a review and the lab instructor will finalize the case by re-grading the entire project a second time.
- **Late Submissions.** Late submission is accepted within three days after the deadline of the lab project. There are *five grace days*¹ that can be used for project deliverables late submissions without incurring any penalty. A group split-up will consume one grace day. When you use up all your grace days, a 15% per day late penalty will be applied to a late submission. *Submission is not accepted if it is more than three days late.* Please be advised that to simplify the book-keeping, late submission is counted in a unit of day rather than hour or minute. An hour late submission is one day late, so does a fifteen hour late submission. Unless notified otherwise, we always take the latest submission from the Learn dropbox.

Lab Repeating Policy

For a student who repeats the course, labs need to be re-done with new lab partners. Simply turning in the old lab code is not allowed. We understand that the student may choose a similar route to the solution chosen last time the course was taken. However it should not be identical. The labs will be done a second time, we expect that the student will improve the older solutions. Also the new lab partners should be contributing equally, which will also lead to differences in the solutions.

¹Grace days are calendar days. Days in weekends are counted.

Note that the policy is course specific to the discretion of the course instructor and the lab instructor.

Lab Projects Solution Internet Policy

Publishing your lab projects solution source code or lab report on the internet for public to access is a violation of academic integrity. Because this potentially enabling other groups to cheat the system in the current and future offerings of the course. For example, it is not acceptable to host a public repository on GitHub that contains your lab project solutions. A lab grade zero will automatically be assigned to the offender.

Seeking Help

- **Discussion Forum.** We recommend students to use the Piazza discussion forum to ask the teaching team questions instead of sending individual emails to lab teaching staff. For questions related to lab projects, our target response time is one business day before the deadline of the particular lab in question². *There is no guarantee on the response time to questions of a lab that passes the submission deadline.*
- **Office Hours.** The Learn system calendar gives the office hour details.
- **Appointments.** Students can also make appointments with lab teaching staff should their problems are not resolved by discussion forum or during office hours. The appointment booking is by email.

To make the appointment efficient and effective, when requesting an appointment, please specify three preferred times and roughly how long the appointment needs to be. On average, an appointment is fifteen minutes per project group. Please also summarize the main questions to be asked in your appointment requesting email. If a question requires teaching staff to look at a code fragment, please make sure your code is accessible by the lab teaching staff.

Please note that teaching staff will not debug student's program for the student. Debugging is part of the exercise of finishing a programming assignment. Teaching staff will be able to demonstrate how to use the debugger and provide case specific debugging tips. Teaching staff will not give direct solution to a lab assignment. Guidances and hints will be provided to help students to find the solution by themselves.

²Our past experiences show that the number of questions spike when deadline is close. The teaching staff will not be able to guarantee one business day response time when workload is above average, though we always try our best to provide timely response.

Part II

Lab Project

Chapter 1

Introduction

1.1 Overview

In this project, you will design a small real-time executive (RTX) and implement it on a Keil MCB1700 board populated with an NXP LPC1768 microcontroller . The executive will provide a basic multiprogramming environment, with five priority levels, preemption, dynamic memory management, shared memory and semaphore for inter-task communication and synchronization, a basic timing service, system console I/O and debugging support.

Such an RTX is suitable for embedded computers which operate in real time. A cooperative, non-malicious software environment is assumed. The design of the RTX should allow its placement in ROM. Applications and non-kernel RTX tasks must execute in the unprivileged level of LPC1768. The RTX kernel will execute in the privileged level ¹. There is 32K of RAM for use by the RTX and application tasks. The microcontroller has four timers, four UARTs and several other peripheral interface devices. The board has two RS-232 interfaces, from which UART0 is used for your RTX system console and UART1 is used for your RTX debug terminal.

1.2 Summary of RTX Requirements

The RTX requirements are listed as follows:

1.2.1 RTX Primitives and Services

The RTX provides primitives and services for as following.

¹We do not require application processes to use Process Stack Pointer (PSP). You may use the Main Stack Pointer (MSP) both for your kernel and non-kernel code. However non-trivial implementations that are not required such as using PSP for user processes be rewarded with bonus marks.

Memory Management

First fit dynamic memory allocation is supported. Refer to Chapter [2](#) for details.

Task Management

The RTX fixed number of tasks. The maximum number of tasks that can run is decided at compile time. The RTX supports task creation and deletion during run time. The RTX is supports task preemption. There are four user priority levels plus an additional “hidden” priority level for the Null task. There is no time slicing. FIFO (First In, First Out) scheduling policy at each priority level is supported. Refer to Chapter [3](#) for details.

Synchronization, Timing Service and Console I/O

The RTX provides semaphore utility for inter-task communication synchronization. An interrupt-driven UART provides the console service. The RTX provides a primitive for a task to pause itself and for a primitive to query the kernel internal clock ticks. Refer to Chapter [4](#) for details.

Real-Time Dynamic Scheduling

The EDF (Earliest Deadline First) scheduling policy at each priority level is supported. Refer to Chapter [5](#) for details.

1.2.2 RTX Tasks

You are required to implement two types of tasks by using the RTX primitives and services. They are user tasks and system tasks.

User Tasks

These tasks are operating at a unprivileged level in thread mode. They are user applications that perform certain user defined functions. For each lab project, you will implement test tasks to help you test the RTX primitives and services you have designed and implemented. In Lab3, you will add a wall clock user task and a set process priority task once you have the console I/O service ready.

System Tasks

These tasks are operating in thread mode. Some may require a privileged level of operation and some may be sufficient to operate at a unprivileged level. It is your design decision to justify which task will be operating at what privilege level. Three system tasks are required and they are null task (see Chapter [2](#)), console display task and keyboard command decoder task (see Chapter [4](#)).

1.2.3 RTX Footprint and Processor Loading

A reasonably *lean* implementation is expected. No standard C library function call is allowed in the kernel code.

1.2.4 Error Detection and Recovery

The primitive will return an error code (a non-zero integer value) upon an error. No error recovery is required. It may be assumed that the application processes can deal with this situation.

Chapter 2

Lab1 Introduction to Kernel Programming and Memory Management

2.1 Objective

This lab is to introduce kernel programming for the Keil MCB1700 board. You will become familiar with the Keil uVision5 IDE (Integrated Development Environment). You will create a set of memory management system calls that are part of the services that your RTX provides. After this lab you will be able to answer the following questions:

- How to use the Keil uVision5 IDE to edit, debug, simulate and execute a bare-metal uVision project
- How to use SVC as a gateway to program a system call in the kernel space for ARM Cortex-M3 processor
- How to design and implement first fit memory management data structure and algorithm

2.2 Starter Files

The starter file is on GitHub at http://github.com/yqh/ece350/manual_code/. It contains the following files:

- util/printf_uart: printf source code and the uart polling source code. The printf outputs to the UART1 by polling.
- util/debug_script: RAM.ini that initializes debugger to load code for in-memory execution.

- `HelloWorld/`: a bare-metal project that outputs strings to UART0 and UART1 by polling.
- `SVC/`: a bare-metal project that uses the SVC as a gateway to transfer from user space to kernel space. It is the skeleton project file for your lab1. Aside from the `printf` and `uart` polling source code, it contains the following under the `src/` folder:
 - `k_mem.h`: the kernel memory management routine header file;
 - `k_mem.c`: the kernel memory management C source code template file to be completed by students;
 - `main_svc.c`: a main method file for writing testing cases;
 - `common.h`: the header file both the kernel and the user can include; and
 - `rtx.h`: the user RTX API file. You should not modify this file.

2.3 Pre-lab Preparation

- Create a Hello World application for Keil MCB1700 using MDK uVision (See Chapter 8)
- Read “Keil MCB1700 Hardware Environment” in Chapter 7
- Read “SVC Programming: Writing an RTX API Function” in Section 9.5.
- Execute the `HelloWorld` project in the simulator and the board.
- Execute the `SVC` project in the simulator and on the board.
- Read “Free-Space Management” at <http://pages.cs.wisc.edu/~remzi/OSTEP/vm-freespace.pdf>.

2.4 Assignment

There is a programming project and a report, which documents the data structure and algorithms of the programming project.

2.4.1 Programming Project

You are to implement the first fit memory allocation algorithm. You will first implement a memory initialization function, which initializes the RTX with the smallest size of memory manageable. Then you will implement an allocation function and a de-allocation function. One utility function will also be implemented to help analyze the efficiency of allocation algorithm and its implementation. You will also write tests to verify your implementation.

Description of Functions

The specification of each function to be implemented are described below:

Memory Initialization Function

NAME

`mem_init` - initialize the dynamic memory manager

SYNOPSIS

```
#include "rtx.h"

int mem_init(size_t blk_size, int algo);
```

DESCRIPTION

The `mem_init()` system call initializes the system's memory manager with the smallest memory block size that the manager is able to manage and the allocation algorithm used.

The input parameter `blk_size` is the smallest memory block size in bytes that the memory manager can manage. The smallest memory block size is a multiple of word size. In our case, we have a 32 bit machine. Our word size is 4 bytes.

The input parameter `algo` specifies the memory allocation algorithm. The full list of memory allocation algorithms are as follows:

FIRST_FIT

The first fit memory allocation algorithm is used.

RETURN VALUE

The function returns 0 on success and -1 on failure. For example, some causes of failure could be that the `blk_size` value is too small or an unsupported memory allocation algorithm is specified.

The system call traps into the kernel and then initializes the memory allocation data structure based on the specified memory allocation algorithm. You are responsible for designing and implementing data structures used to track what memory is currently allocated and what is free¹.

Allocation Function:

NAME

`mem_alloc` - allocate dynamic memory

¹In Lab2, where multi-tasking is supported, you will also need to start making your memory management data structures to track which task holds which allocated memory. This is not required in Lab1 since multi-tasking is not in your kernel yet.

SYNOPSIS

```
#include "rtx.h"

void *mem_alloc(size_t size);
```

DESCRIPTION

The `mem_alloc()` system call allocates `size` bytes and returns a pointer to the allocated memory². The allocated memory is not initialized. If `size` is 0, then `mem_alloc()` returns NULL.

The input parameter `size` is the number of bytes requested from the allocator. The allocator then returns the starting address of a block of memory of the appropriate size. The memory address should be four bytes aligned. Memory requests may be of any size from one byte all the way up to the maximum size of the physical memory on the board. If the smallest size of the memory manageable is S bytes, for a request for N bytes, return a memory block of $(N + \delta)$ bytes, where $\delta = 0, 1, 2, 3, \dots, S$ and $(N + \delta)$ is a multiple of four. Should $\delta > 0$, the additional space is just the internal fragmentation which can be ignored (and the user will not be told).

RETURN VALUE

The function returns a pointer to the allocated memory or NULL if the request fails.

Deallocation Function:

NAME

`mem_dealloc` - Free dynamic memory

SYNOPSIS

```
#include "rtx.h"

void mem_dealloc(void *ptr);
```

DESCRIPTION

The `mem_dealloc()` system call frees the memory space pointed to by `ptr`, which must have been returned by a previous call to `mem_alloc()`. Otherwise, or if `mem_dealloc(ptr)` has already been called before, undefined behaviour occurs. If `ptr` is NULL, no operation is performed.

If the freed memory block is adjacent to other free memory blocks, it is merged with them immediately (i.e. immediate coalescence) and the combined block is then re-integrated into the memory under management.

²The `mem_init()` needs to be invoked before calling `mem_alloc()`.

You are not required to clear the block (that is, to fill the memory with zeros).

RETURN VALUE

This function returns no value.

Utility Function:

NAME

`mem_count_extfrag` - Count external fragmented memory blocks

SYNOPSIS

```
#include "rtx.h"  
  
int mem_count_extfrag(size_t size);
```

DESCRIPTION

This system call counts the number of free (i.e. unallocated) memory blocks in memory that are of a size less than the input value of `size`. The input value `size` is in bytes. The space your structures need to maintain un-allocated (free) memory is considered as free in this context.

Testing

In order to test your implementation of the required functions, write an application to allocate and de-allocate memory in different ways and possibly multiple times. The provided `main_svc.c` file is for writing your testing code. Create a set of testing scenarios to verify functions implemented. Document the testing specification in the report (See [2.4.2](#)). Implement the tests in `main_svc.c` file.

There is no hard requirement on what tests to be implemented. The rule of thumb is that the tests will convince yourself that your implementation is correct. However to provide more leads to testing ideas, you may want to consider repeatedly requesting and then releasing and make sure no extra memory appears or no memory gets lost. The sum of free memory and allocated memory should always be constant.

Another test you want to include is about the external fragmentation. Allocate and de-allocate memory with different sizes and see how external fragmentation is affected. The utility function `mem_count_exfrag()` is a useful tool.

Since the tests have no knowledge of your detailed internal design, they only invoke the functions specified by the RTX API. We require the testing results to comply with the following format and you output the results to the UART terminal by polling (i.e. UART1):

Gid_test: START

```
Gid_test: test n OK
Gid_test: test m FAIL
Gid_test: x/N tests OK
Gid_test: y/N tests FAIL
Gid_test: END
```

For example, assume that you are in group G099 and you have 3 testing cases in total. If two of the testing cases pass and one of the testing cases does not pass, the final testing results should be output to the putty terminal as follows:

```
G099_test: START
G099_test: total 3 tests
G099_test: test 1 OK
G099_test: test 2 OK
G099_test: test 3 FAIL
G099_test: 2/3 tests OK
G099_test: 1/3 tests FAIL
G099_test: END
```

2.4.2 Report

Write the following items in a report and name it `p1_report.pdf`.

- Statement of the problem to be discussed in the report
- Descriptions of the data structures and algorithms used to implement the allocation strategy
- Testing scenario description

To illustrate key algorithm, pseudocode is a good way to describe the algorithm from a high-level point of view.

2.4.3 Third-party Testing and Source Code File Organization

We will write a third-party testing program to verify the correctness of your implementation of the functions. In order to do so, we will need to enforce certain source code file organization standard. You should keep the file organization in the provided skeleton code, which has a `src` sub-directory inside. There are dos and don'ts you need to follow.

Don'ts

- Keep all existing files inside the `src` directory. Do not move any one of them to other directories.

- Do not change the file names under the src directory.
- Do not make any changes of the contents of the `rtx.h` file.
- Do not change the existing function prototype in the given `k_mem.[ch]` files.
- Do not include any new header files in the `main_svc.c`.

Dos

- You are allowed to add new self-defined functions to `k_mem.[ch]`.
- You are also allowed to create new `.h` and `.c` files ³.
- The newly created `.h` file is allowed to be included in the `k_mem.c` file.
- Any new files you add to the project can be put into either the src directory or other directories you will create.

Note that the `main_svc.c` calls the memory management functions you will implement. During the third-party testing, the `main_svc.c` file will be replaced by a third-party testing code with the same file name. Using the provided template `main_svc.c` to write your own testing code.

2.5 Deliverable

2.5.1 Pre-Lab Deliverables

Fill the [project_manager.csv](#) template file and submit it to Lab1 Dropbox on Learn.

2.5.2 Post-Lab Deliverables

Create a directory named “lab1”. Then create a sub-directory named “code” under “lab1”. Put your uVision Project folder under “lab1/code”. Put the `report.pdf` under the “lab1” directory. Include a README file with group identification, project manager name and a description of directory contents. Put the README file under the “lab1” directory. Zip everything inside the lab1 directory and submit it to Learn Lab1 Dropbox.

³For example, you may want to create linked list data structure functions or some helper functions. You may want to create new files to hold these functions for better file organization.

Chapter 3

Lab2 Task Management

To be released by Sep 25th 2020.

Chapter 4

Lab3 Synchronization and Console I/O

To be released by October 9th 20202.

Chapter 5

Lab4 Timing Service and Real-Time Scheduling

To be released by Nov 2nd, 2020.

Chapter 6

Lab5 Memory Protection and Stress Testing

To be released by Nov 16, 2020.

Part III

Software Development Environment Quick Reference Guide

Chapter 7

Keil MCB1700 Hardware Environment

7.1 MCB1700 Board Overview

The Keil MCB1700 board is populated with NXP *LPC1768* Microcontroller. Figure 7.1 shows the important interface and hardware components of the MCB1700 board.

Figure 7.2 is the hardware block diagram that helps you to understand the MCB1700 board components. Note that our lab will only use a small subset of the components which include the LPC1768 CPU, COM and Dual RS232.

The LPC1768 is a 32-bit ARM Cortex-M3 microcontroller for embedded applications requiring a high level of integration and low power dissipation. The LPC1768 operates at up to an 100 MHz CPU frequency. The peripheral complement of LPC1768 includes 512KB of on-chip flash memory, 64KB of on-chip SRAM and a variety of other on-chip peripherals. Among the on-chip peripherals, there are system control block, pin connect block, 4 UARTs and 4 general purpose timers, some of which will be used in your RTX course project. Figure 7.3 is the simplified LPC1768 block diagram [4], where the components to be used in your RTX project are circled with red. Note that this manual will only discuss the components that are relevant to the RTX course project. The LPC17xx User Manual is the complete reference for LPC1768 MCU.

7.2 Cortex-M3 Processor

The Cortex-M3 processor is the central processing unit (CPU) of the LPC1768 chip. The processor is a 32-bit microprocessor with a 32-bit data path, a 32-bit register bank, and 32-bit memory interfaces. Figure 7.4 is the simplified block diagram of the Cortex-M3 processor [5]. The processor has private peripherals which are system control block, system timer, NVIC (Nested Vectored Interrupt Controller) and MPU (Memory Protection Unit). The processor includes a number of internal debugging components which provides debugging features such as breakpoints and

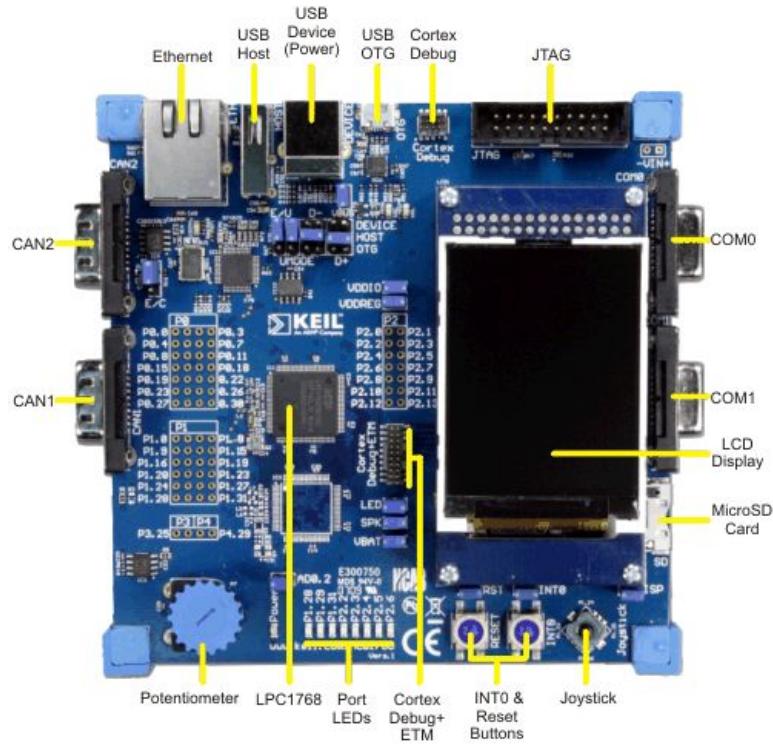


Figure 7.1: MCB1700 Board Components [1]

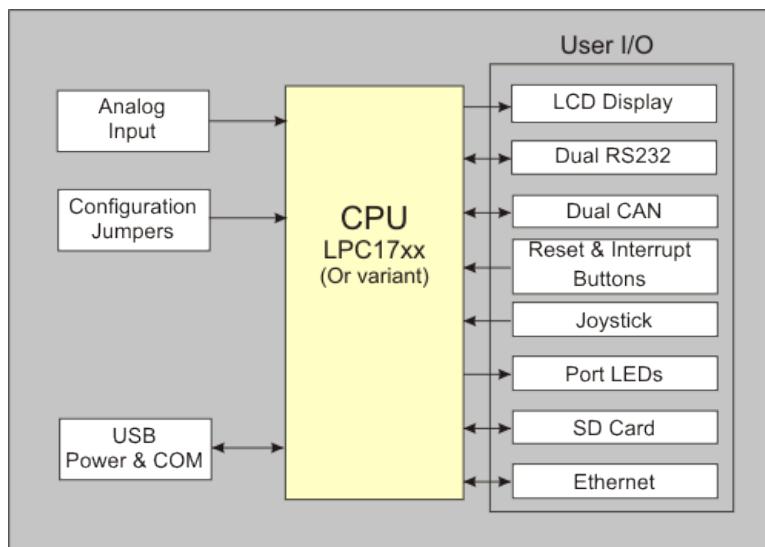


Figure 7.2: MCB1700 Board Block Diagram [1]

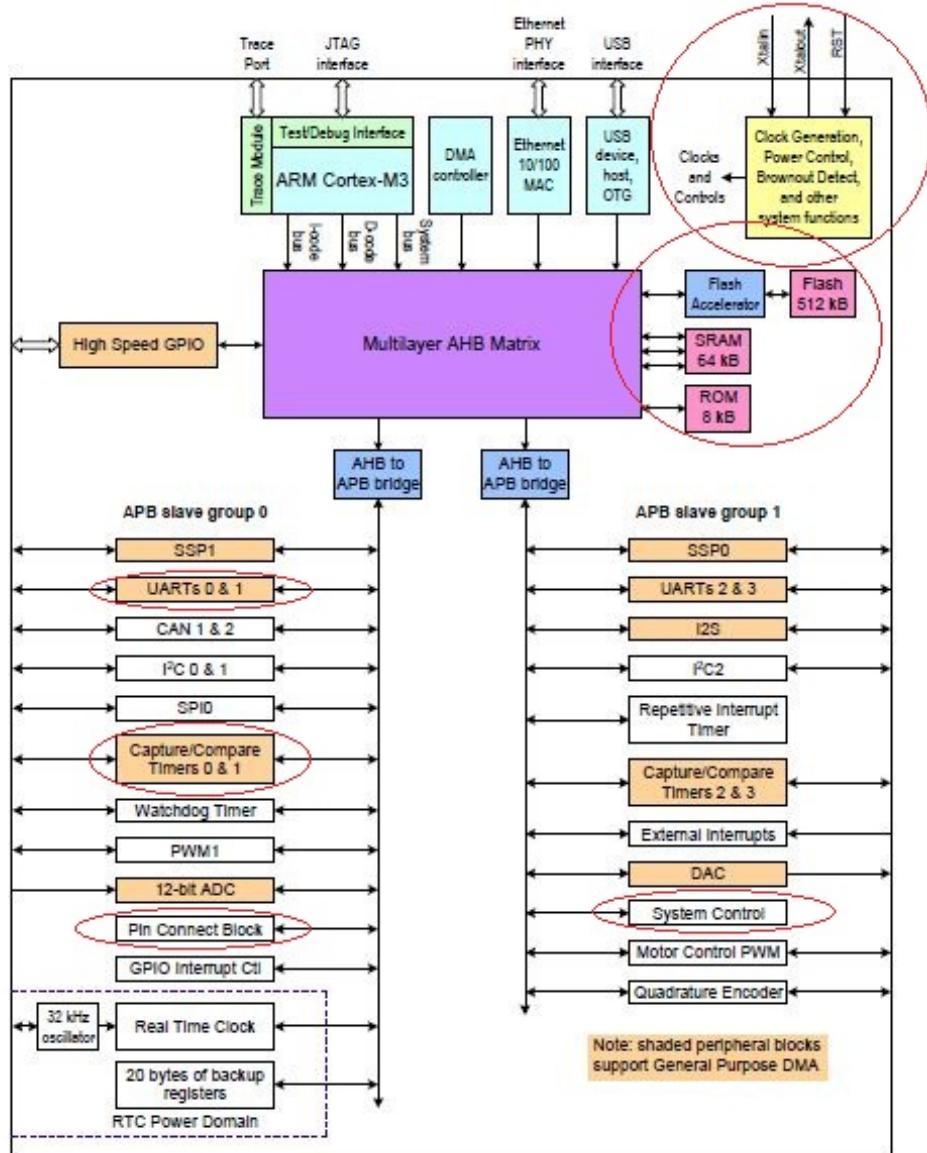


Figure 7.3: LPC1768 Block Diagram. The circled blocks are the ones that we will use in the lab project.

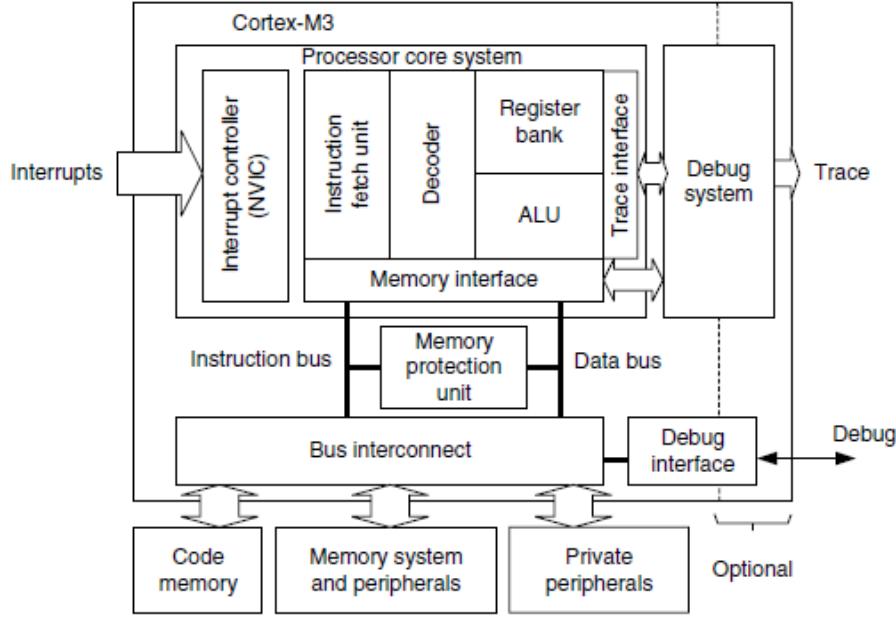


Figure 7.4: Simplified Cortex-M3 Block Diagram[5]

watchpoints.

7.2.1 Registers

The processor core registers are shown in Figure 7.5. For detailed description of each register, Chapter 34 in [4] is the complete reference.

- R0-R12 are 32-bit general purpose registers for data operations. Some 16-bit Thumb instructions can only access the low registers (R0-R7).
- R13(SP) is the stack pointer alias for two banked registers shown as follows:
 - *Main Stack Pointer (MSP)*: This is the default stack pointer and also reset value. It is used by the OS kernel and exception handlers.
 - *Process Stack Pointer (PSP)*: This is used by user application code.

On reset, the processor loads the MSP with the value from address 0x00000000. The lowest 2 bits of the stack pointers are always 0, which means they are always word aligned.

In Thread mode, when bit[1] of the CONTROL register is 0, MSP is used. When bit[1] of the CONTROL register is 1, PSP is used.

- R14(LR) is the link register. The return address of a subroutine is stored in the link register when the subroutine is called.
- R15(PC) is the program counter. It can be written to control the program flow.

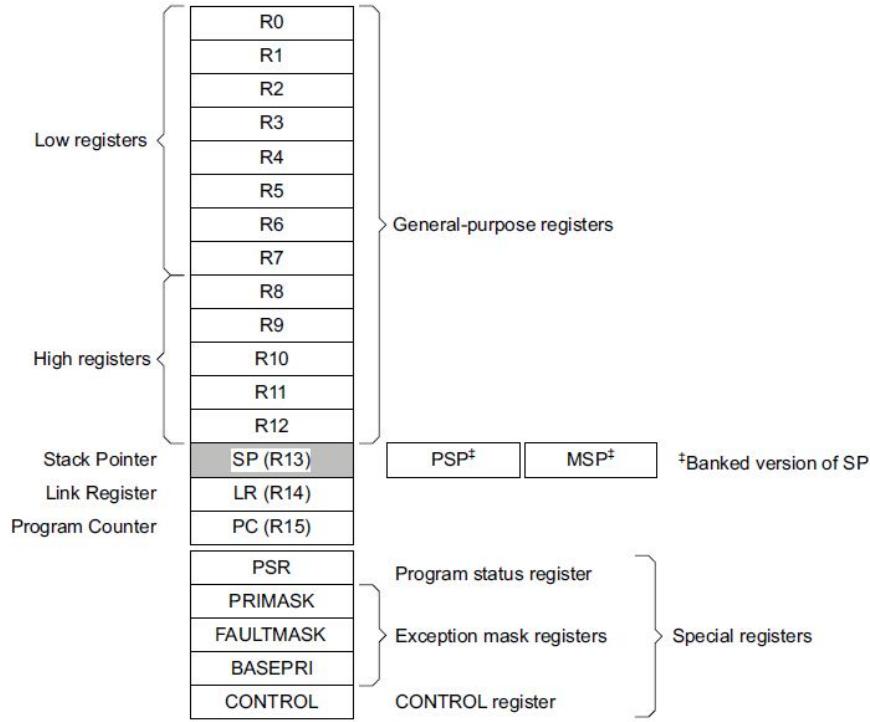


Figure 7.5: Cortex-M3 Registers[4]

- Special Registers are as follows:
 - Program Status registers (PSRs)
 - Interrupt Mask registers (PRIMASK, FAULTMASK, and BASEPRI)
 - Control register (CONTROL)

When at privilege level, all the registers are accessible. When at unprivileged (user) level, access to these registers are limited.

7.2.2 Processor mode and privilege levels

The Cortex-M3 processor supports two modes of operation, Thread mode and Handler mode.

- Thread mode is entered upon Reset and is used to execute application software.
- Handler mode is used to handle exceptions. The processor returns to Thread mode when it has finished exception handling.

Software execution has two access levels, Privileged level and Unprivileged (User) level.

- Privileged

The software can use all instructions and has access to all resources. Your RTOS

kernel functions are running in this mode.

- Unprivileged (User)

The software has limited access to MSR and MRS instructions and cannot use the CPS instruction. There is no access to the system timer, NVIC , or system control block. The software might also have restricted access to memory or peripherals. User processes such as the wall clock process should run at this level.

When the processor is in Handler mode, it is at the privileged level. When the processor is in Thread mode, it can run at privileged or unprivileged (user) level. The bit[0] in CONTROL register determines the execution privilege level. Figure 7.6 illustrate the mode and privilege level of the processor.

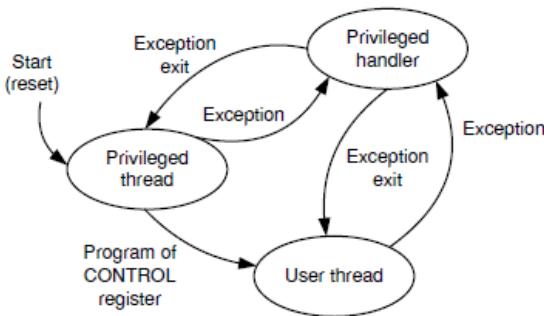


Figure 7.6: Cortex-M3 Operating Mode and Privilege Level[5]

Note that only privileged software can write to the CONTROL register to change the privilege level for software execution in Thread mode. Unprivileged software can use the SVC instruction to make a supervisor call to transfer control to privileged software. When we are in the privileged thread mode, we can directly set the control register to change to unprivileged thread mode. We also can change to unprivileged thread mode by calling SVC to raise an exception first and then inside the exception handler we set the privilege level to unprivileged by setting the control register. Then we modify the EXC_RETURN value in the LR (R14) to indicate the mode and stack when returning from an exception. This mechanism is often used by the kernel in its intialization phase and also context switching between privileged processes and unprivileged processes.

7.2.3 Stacks

The processor uses a full descending stack. This means the stack pointer indicates the last stacked item on the stack memory. When the processor pushes a new item onto the stack, it decrements the stack pointer and then writes the item to the new memory location.

The processor implements two stacks, the *main stack* and the *process stack*. One of these two stacks is banked out depending on the stack in use. This means only one stack is visible at a time as R13. In Handler mode, the main stack is always used. The bit[1] in CONTROL register reads as zero and ignores writes in Handler mode. In Thread mode, the bit[1] setting in CONTROL register determines whether the main stack or the process stack is currently used. Table 7.1 summarizes the processor mode, execution privilege level, and stack use options.

| Processor mode | Used to execute | Privilege level for software execution | CONTROL Bit[0] | CONTROL Bit[1] | Stack used |
|----------------|--------------------|--|----------------|----------------|---------------|
| Thread | Applications | Privileged | 0 | 0 | Main Stack |
| | | Unprivileged | 1 | 1 | Process Stack |
| Handler | Exception handlers | Privileged | - | 0 | Main Stack |

Table 7.1: Summary of processor mode, execution privilege level, and stack use options

7.3 Memory Map

The Cortex-M3 processor has a single fixed 4GB address space. Table 7.2 shows how this space is used on the LPC1768.

| Address Range | General Use | Address range details | Description |
|----------------------------|---|---------------------------|--|
| 0x0000 0000 to 0x1FFF FFFF | On-chip non-volatile memory | 0x0000 0000 – 0x0007 FFFF | 512 KB flash memory |
| | On-chip SRAM | 0x1000 0000 – 0x1000 7FFF | 32 KB local SRAM |
| | Boot ROM | 0x1FFF 0000 – 0x1FFF 1FFF | 8 KB Boot ROM |
| 0x2000 0000 to 0x3FFF FFFF | On-chip SRAM (typically used for peripheral data) | 0x2007 C000 – 0x2007 FFFF | AHB SRAM - bank0 (16 KB) |
| | GPIO | 0x2008 0000 – 0x2008 3FFF | AHB SRAM - bank1 (16 KB) |
| | GPIO | 0x2009 C000 – 0x2009 FFFF | GPIO |
| 0x4000 0000 to 0x5FFF FFFF | APB Peripherals | 0x4000 0000 – 0x4007 FFFF | APB0 Peripherals |
| | | 0x4008 0000 – 0x400F FFFF | APB1 Peripherals |
| | AHB peripherals | 0x5000 0000 – 0x501F FFFF | DMA Controller, Ethernet interface, and USB interface |
| 0xE000 0000 to 0xE00F FFFF | Cortex-M3 Private Peripheral Bus (PPB) | 0xE000 0000 – 0xE00F FFFF | Cortex-M3 private registers(NVIC, MPU and SysTick Timer et. al.) |

Table 7.2: LPC1768 Memory Map

Note that the memory map is not continuous. For memory regions not shown in the table, they are reserved. When accessing reserved memory region, the processor's behavior is not defined. All the peripherals are memory-mapped and the

LPC17xx.h file defines the data structure to access the memory-mapped peripherals in C.

7.4 Exceptions and Interrupts

The Cortex-M3 processor supports system exceptions and interrupts. The processor and the Nested Vectored Interrupt Controller (NVIC) prioritize and handle all exceptions. The processor uses *Handler mode* to handle all exceptions except for reset.

7.4.1 Vector Table

Exceptions are numbered 1-15 for system exceptions and 16 and above for external interrupt inputs. LPC1768 NVIC supports 35 vectored interrupts. Table 7.3 shows system exceptions and some frequently used interrupt sources. See Table 50 and Table 639 in [4] for the complete exceptions and interrupts sources. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR (within the System Control Block) to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80.

| Exception number | IRQ number | Vector address or offset | Exception type | Priority | C PreFix |
|------------------|------------|--------------------------|-------------------------|-----------------|-------------|
| 1 | - | 0x00000004 | Reset | -3, the highest | |
| 2 | -14 | 0x00000008 | NMI | -2, | NMI_- |
| 3 | -13 | 0x0000000C | Hard fault | -1 | HardFault_- |
| 4 | -12 | 0x00000010 | Memory management fault | Configurable | MemManage_- |
| : | | | | | |
| 11 | -5 | 0x0000002C | SVCall | Configurable | SVC_- |
| : | | | | | |
| 14 | -2 | 0x00000038 | PendSV | Configurable | PendSVC_- |
| 15 | -1 | 0x0000003C | SysTick | Configurable | SysTick_- |
| 16 | 0 | 0x00000040 | WDT | Configurable | WDT_IRQ |
| 17 | 1 | 0x00000044 | Timer0 | Configurable | TIMER0_IRQ |
| 18 | 2 | 0x00000048 | Timer1 | Configurable | TIMER1_IRQ |
| 19 | 3 | 0x0000004C | Timer2 | Configurable | TIMER2_IRQ |
| 20 | 4 | 0x00000050 | Timer3 | Configurable | TIMER3_IRQ |
| 21 | 5 | 0x00000054 | UART0 | Configurable | UART0_IRQ |
| 22 | 6 | 0x00000058 | UART1 | Configurable | UART1_IRQ |
| 23 | 7 | 0x0000005C | UART2 | Configurable | UART2_IRQ |
| 24 | 8 | 0x00000060 | UART3 | Configurable | UART3_IRQ |
| : | | | | | |

Table 7.3: LPC1768 Exception and Interrupt Table

7.4.2 Exception Entry

Exception entry occurs when there is a pending exception with sufficient priority and either

- the processor is in Thread mode
- the processor is in Handler mode and the new exception is of higher priority than the exception being handled, in which case the new exception preempts the original exception (This is the nested exception case which is not required in our RTOS lab).

When an exception takes place, the following happens

- Stacking

When the processor invokes an exception (except for tail-chained or a late-arriving exception, which are not required in the RTOS lab), it automatically stores the following eight registers to the SP:

- R0-R3, R12
- PC (Program Counter)
- PSR (Processor Status Register)
- LR (Link Register, R14)

Figure 7.7 shows the exception stack frame. Note that by default the stack frame is aligned to double word address starting from Cortex-M3 revision 2. The alignment feature can be turned off by programming the STKALIGN bit in the System Control Block (SCB) Configuration Control Register (CCR) to 0. On exception entry, the processor uses bit[9] of the stacked PSR to indicate the stack alignment. On return from the exception, it uses this stacked bit to restore the correct stack alignment.

- Vector Fetching

While the data bus is busy stacking the registers, the instruction bus fetches the exception vector (the starting address of the exception handler) from the vector table. The stacking and vector fetch are performed on separate bus interfaces, hence they can be carried out at the same time.

- Register Updates

After the stacking and vector fetch are completed, the exception vector will start to execute. On entry of the exception handler, the following registers will be updated as follows:

- SP: The SP (MSP or PSP) will be updated to the new location during stacking. Stacking from the privileged/unprivileged thread to the first level of the exception handler uses the MSP/PSP. During the execution of exception handler routine, the MSP will be used when stack is accessed.

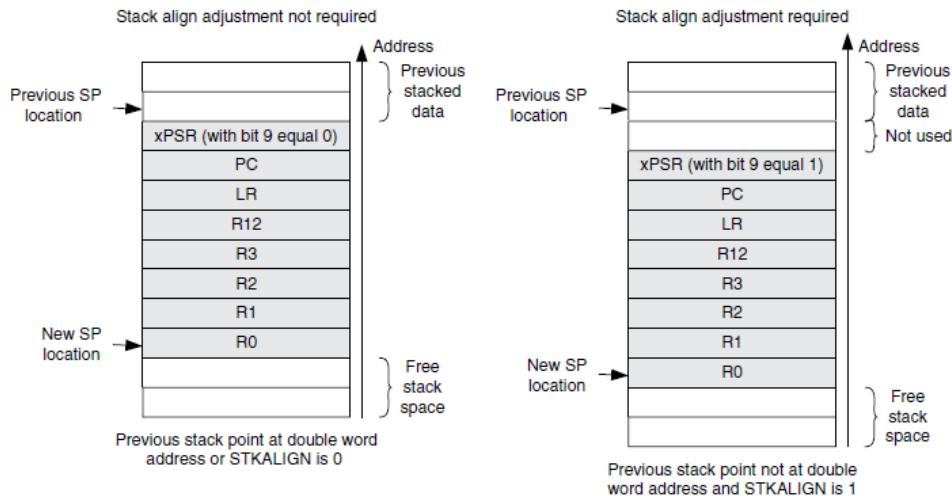


Figure 7.7: Cortex-M3 Exception Stack Frame [5]

- PSR: The IPSR will be updated to the new exception number
- PC: The PC will change to the vector handler when the vector fetch completes and starts fetching instructions from the exception vector.
- LR: The LR will be updated to a special value called EXC_RETURN. This indicates which stack pointer corresponds to the stack frame and what operation mode the processor was in before the exception entry occurred.
- Other NVIC registers: a number of other NVIC registers will be updated .For example the pending status of exception will be cleared and the active bit of the exception will be set.

7.4.3 EXC_RETURN Value

EXC_RETURN is the value loaded into the LR on exception entry. The exception mechanism relies on this value to detect when the processor has completed an exception handler. The EXC_RETURN bits [31 : 4] is always set to 0xFFFFFFFF by the processor. When this value is loaded into the PC, it indicates to the processor that the exception is complete and the processor initiates the exception return sequence. Table 7.4 describes the EXC_RETURN bit fields. Table 7.5 lists Cortex-M3 allowed EXC_RETURN values.

| Bits | 31:4 | 3 | 2 | 1 | 0 |
|-------------|------------|---------------------------------|--------------|------------------------|------------------------------|
| Description | 0xFFFFFFFF | Return mode (Thread/Handler) | Return stack | Reserved; must be 0 | Process state (Thumb/ARM) |

Table 7.4: EXC_RETURN bit fields [5]

| Value | Description | | |
|-------------|-------------|----------------------------------|-----------------|
| | Return Mode | Exception return gets state from | SP after return |
| 0xFFFFFFFF1 | Handler | MSP | MSP |
| 0xFFFFFFFF9 | Thread | MSP | MSP |
| 0xFFFFFFFFD | Thread | PSP | PSP |

Table 7.5: EXC_RETURN Values on Cortex-M3

7.4.4 Exception Return

Exception return occurs when the processor is in Handler mode and executes one of the following instructions to load the EXC_RETURN value into the PC:

- a POP instruction that includes the PC. This is normally used when the EXC_RETURN in LR upon entering the exception is pushed onto the stack.
- a BX instruction with any register. This is normally used when LR contains the proper EXC_RETURN value before the exception return, then BX LR instruction will cause an exception return.
- a LDR or LDM instruction with the PC as the destination. This is another way to load PC with the EXC_RETURN value.

Note unlike the ColdFire processor which has the RTE as the special instruction for exception return, in Cortex-M3, a normal return instruction is used so that the whole interrupt handler can be implemented as a C subroutine.

When the exception return instruction is executed, the following exception return sequences happen:

- Unstacking: The registers (i.e. exception stack frame) pushed to the stack will be restored. The order of the POP will be the same as in stacking. The SP will also be changed back.
- NVIC register update: The active bit of the exception will be cleared. The pending bit will be set again if the external interrupt is still asserted, causing the processor to reenter the interrupt handler.

7.5 Data Types

The processor supports 32-bit words, 16-bit halfwords and 8-bit bytes. It supports 64-bit data transfer instructions. All data memory accesses are managed as little-endian.

Chapter 8

Keil Software Development Tools

The Keil MDK-ARM development tools are used for MCB1700 boards in our lab. The tools include

- uVision5 IDE which combines the project manager, source code editor and program debugger into one environment;
- ARM compiler, assembler, linker and utilities;
- ULINK USB-JTAG Adapter which allows you to debug the embedded programs running on the board.

The MDK-Lite is the evaluation version and does not require a license. It has a code size limit of 32KB, which is adequate for the lab projects. The MDK-Lite version 5 is installed on all lab computers. If you want to install the software on your own computer. MDK 5.30 installation file is in Learn Lab/RTX Project section. The downloading link for the latest version is <https://www2.keil.com/mdk5/editions/lite>.

8.1 Creating an Application in uVision5 IDE

To get started with the Keil IDE, the Getting Started with MDK Guide at https://www.keil.com/support/man/docs/mdk_gs/ is a good place to start. We will walk you through the IDE by developing a simple HelloWorld application which displays Hello World through the UART0 and UART1 that are connected to the lab PC. Note the HelloWorld example uses polling on both UART0 and UART1 rather than interrupt.

8.1.1 Getting Starter Code from the GitHub

The ECE 350 lab starter github is at <https://github.com/yqh/ece350>. Let's first make a clone of this repository by using the following command:

```
git clone https://github.com/yqh/ece350
```

8.1.2 Create a New Project

1. Create a directory named “HelloWorld” on your computer. The folder path name should not contain spaces on Nexus computers.
2. Create a sub-directory “src” under the “HelloWorld” directory. This sub-folder is where we want to put our source code of the project.
3. Copy the following files to “src” folder:
 - manual_code/util/printf_uart/uart_def.h
 - manual_code/util/printf_uart/uart_polling.h
 - manual_code/util/printf_uart/uart_polling.c
4. Create a new uVision project.
Open the file explorer and navigate to C:\Software\Keil_v5\UV4. Double click the UV4.exe program to start the IDE.
 - Click Project → New uVision Project (See Figure 8.1).

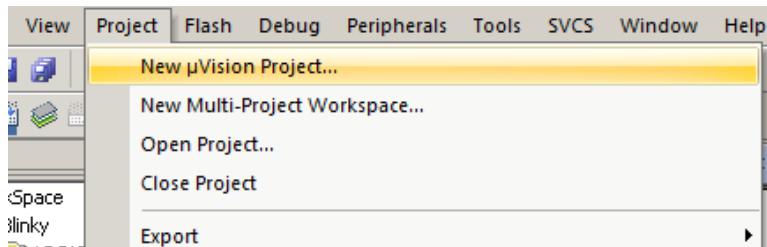


Figure 8.1: Keil IDE: Create a New Project

- Select NXP → LPC1700 Series → LPC176x → LPC1768 (See Figure 8.2).
- Select CMSIS → CORE and Device → Startup (See Figure 8.3).

8.1.3 Managing Project Components

You just finished creating a new project. On the left side of the IDE is the Project window. Expand all objects. You will see the default project setup as shown in Figure 8.4.

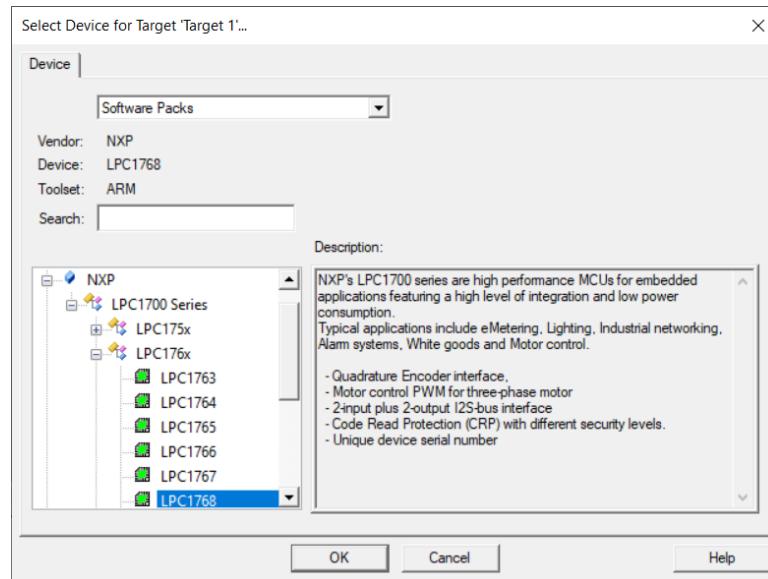


Figure 8.2: Keil IDE: Choose MCU

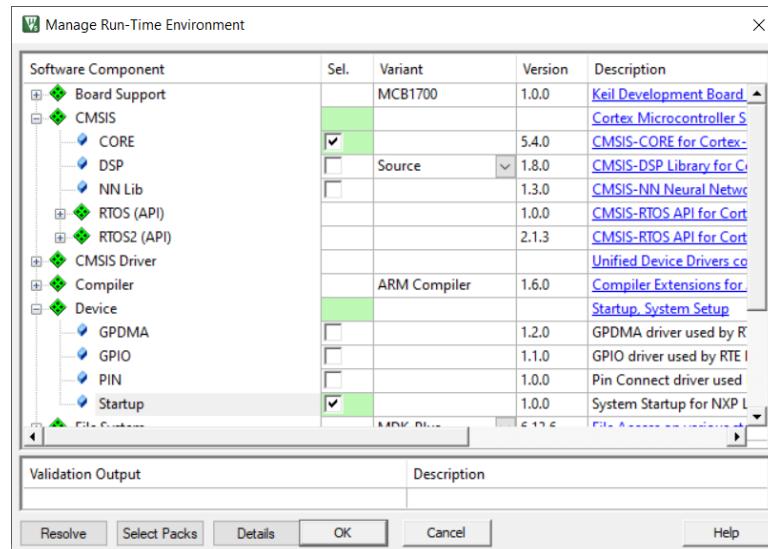


Figure 8.3: Keil IDE: Manage Run-Time Environment

1. Rename the Target

The “Target 1” is the default name of the project build target and you can rename it. Select the target name to highlight it and then long press the left button of the mouse to make the target name editable. Input a new target name, say “HelloWorld SIM”.

2. Rename the Source Group

The IDE allows you to group source files to different groups to better manage the source code. By default “Source Group 1” is created and it contains no file.

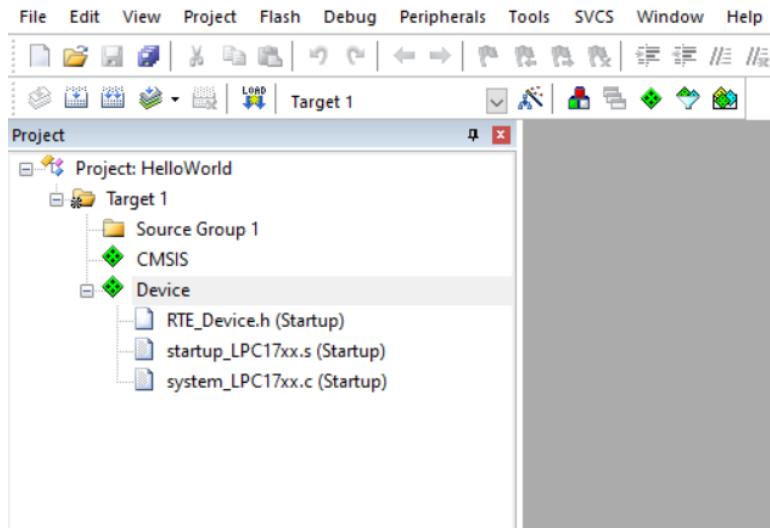


Figure 8.4: Keil IDE: A default new project

Let's rename the source group to "System Code"¹.

3. Add a New Source Group

We can also add new source group in our project. Select the HelloWorld SIM item and right click to bring up the context window and select "Add Group..." (See Figure 8.5).

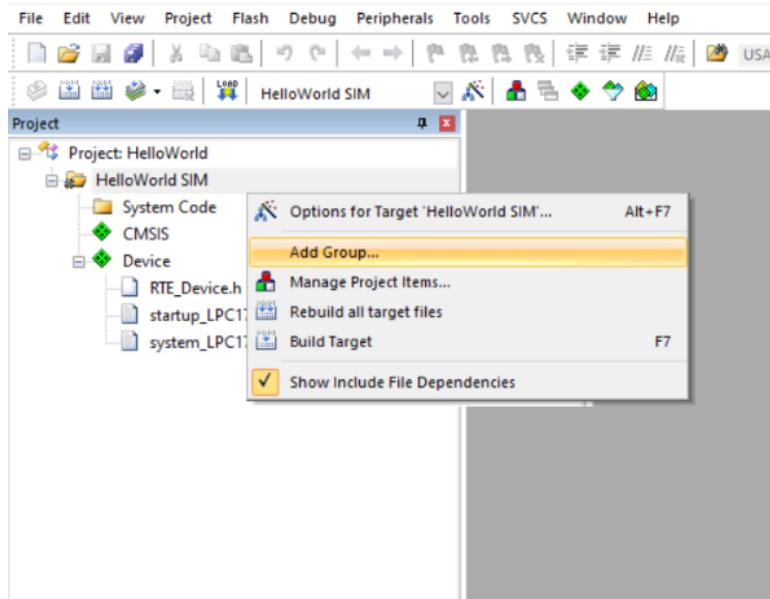


Figure 8.5: Keil IDE: Add Group

¹To rename a source group, select the source group to highlight it and long press the left mouse button to make the name editable.

A new source group named “New Group” is added to the project. Let’s rename it to “User Code”. Your project will now look like Figure 8.6.

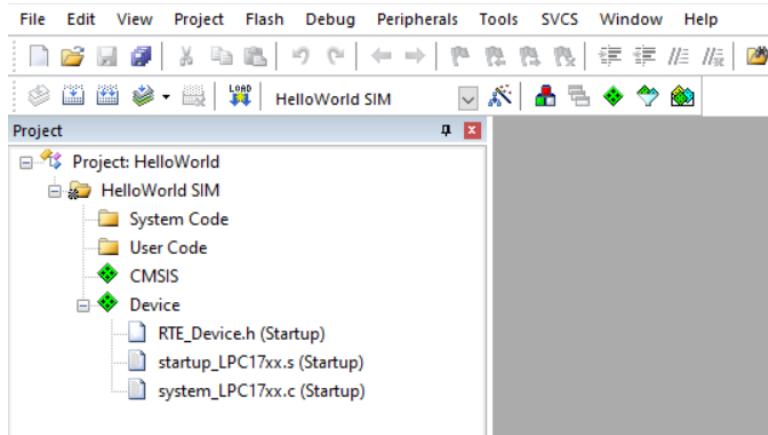


Figure 8.6: Keil IDE: Updated Project Profile

4. Add Source Code to a Source Group

Let’s add `uart_polling.c` to “System Code” group by double clicking the source group and choose the file from the file window. Double clicking the file name will add the file to the source group. Or you can select the file and click the “Add” button at the lower right corner of the window (See Figure 8.7).

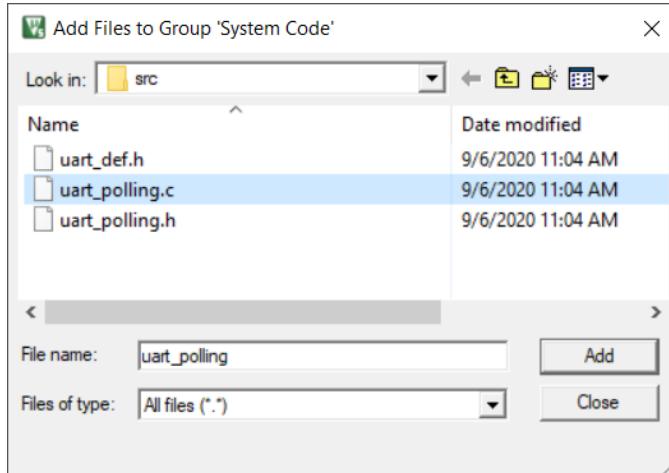


Figure 8.7: Keil IDE: Add Source File to Source Group

Your project will now look like Figure 8.8.

5. Create a new source file

The project does not have a main function yet. We now create a new file by selecting File → New (See Figure 8.9). Before typing anything to the file, save the file and name it “main.c”. Add main.c to the “Source Code” group. Type

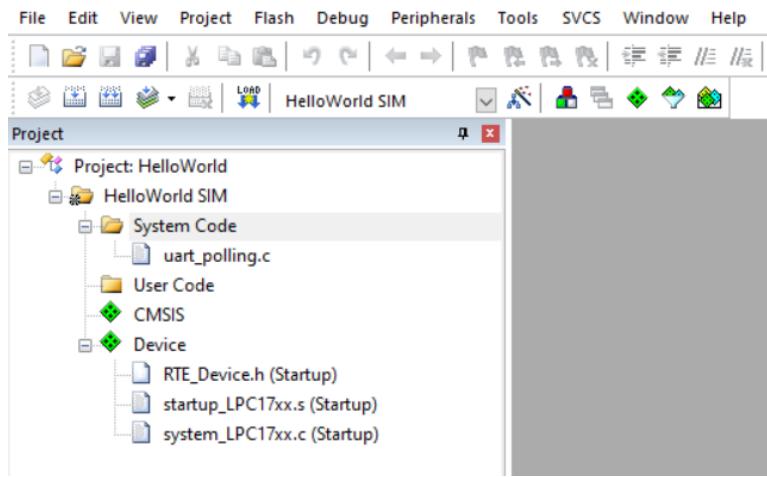


Figure 8.8: Keil IDE: Updated Project Profile

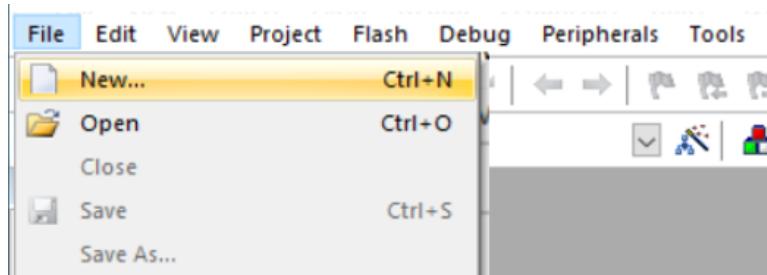


Figure 8.9: Keil IDE: Create New File

the source code as shown in Figure 8.10. Your final project would look like the screen shot in Figure 8.10.

A screenshot of the Keil IDE interface showing the final project setup. The 'Project' view on the left shows the 'HelloWorld' project with its components: 'HelloWorld RAM', 'System Code' (containing 'uart_polling.c'), 'User Code' (containing 'main.c'), 'CMSIS', and 'Device'. The main workspace shows two tabs: 'startup_LPC17xx.s' (selected) and 'main.c'. The 'main.c' tab displays the following C code:

```
1 #include <LPC17xx.h>
2 #include "uart_def.h"
3 #include "uart_polling.h"
4
5 int main() {
6     SystemInit();
7     uart0_init();
8     uart1_init();
9     uart0_put_string("UART0 - Howdy!\r\n");
10    uart1_put_string("UART1 - Hello World!\r\n");
11    return 0;
12 }
```

Figure 8.10: Keil IDE: Final Project Setting

8.1.4 Build the Application

To build a target, the main work is to configure the target options.

Configure Target Options

Most of the default settings of the target options are good. There are a few options that we need to modify.

1. Bring up the target option configuration window by pressing the target options button (See Figure 8.11).

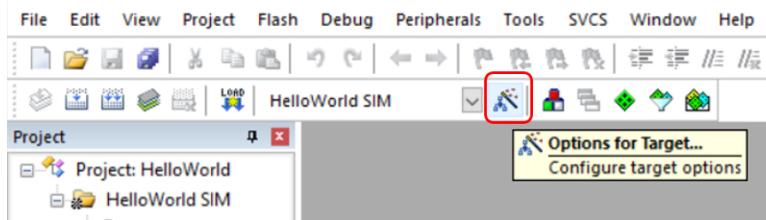


Figure 8.11: Keil IDE: Target Options Configuration

2. Configure the C/C++ tab as shown in Figure 8.12. We do not need c99 for this example. So we leave it unchecked. If you click OK to finish the Target option setting now, you will find the red cross at line 2 (See Figure 8.10) is now gone. Now re-open the target options configuration window and proceed to the next step.

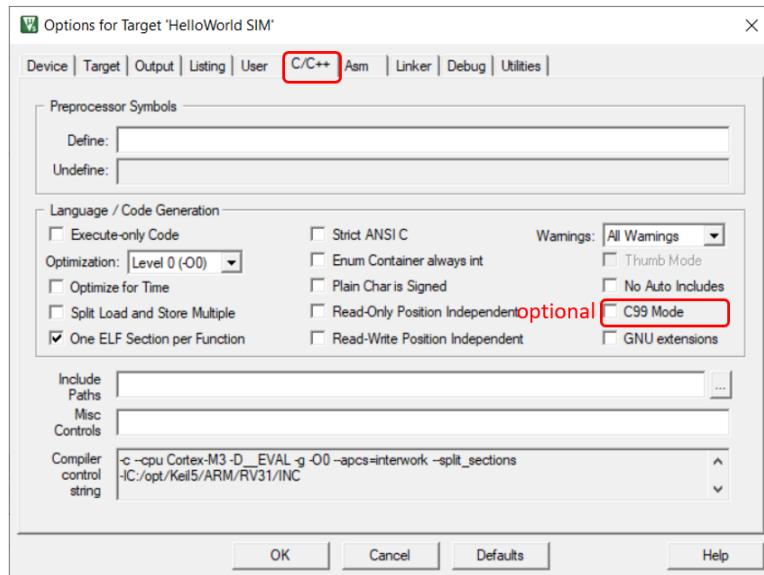


Figure 8.12: Keil IDE: Target Options C/C++ Tab Configuration

3. Configure the Target tab as shown in Figure 8.13. We want to use the default version 5 arm compiler. We also want remove the IRAM2 from the default setting.

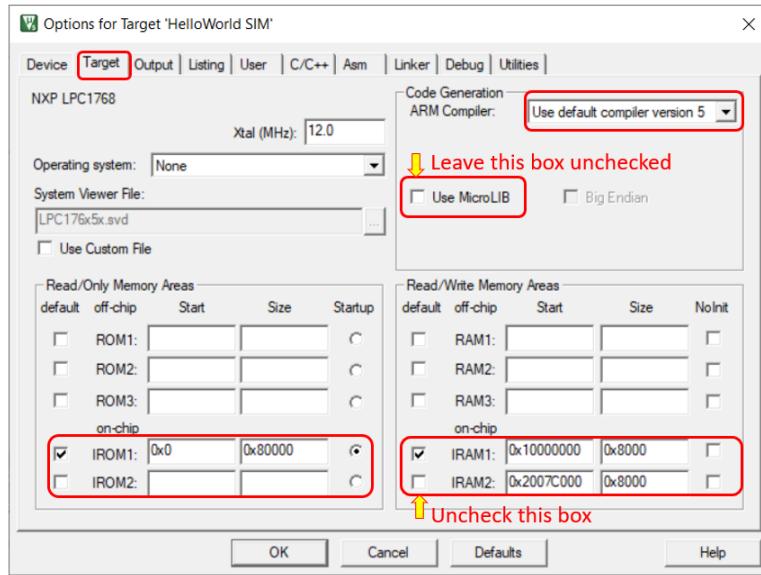


Figure 8.13: Keil IDE: Target Options Target Tab Configuration

- Configure the Linker tab as shown in Figure 8.14. This is to instruct the linker to use the memory layout from the Target tab rather than default memory layout.

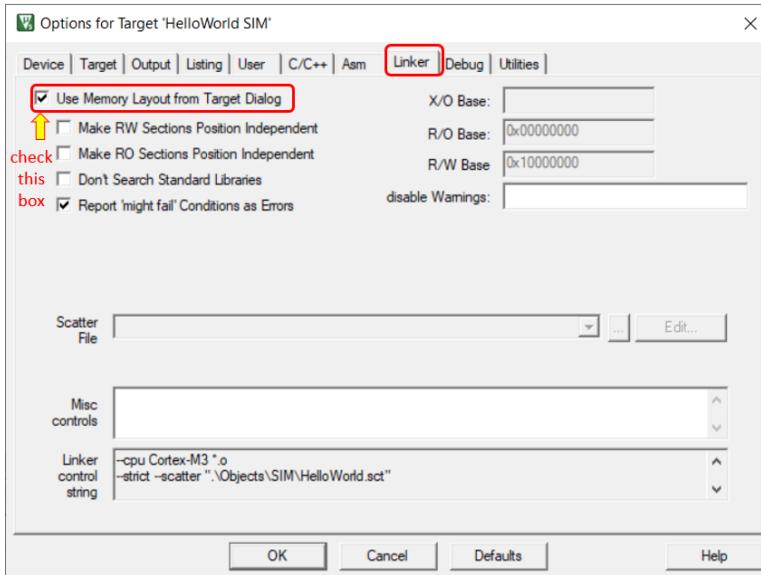


Figure 8.14: Keil IDE: Target Options Linker Tab Configuration

Build the Target

To build the target, click the “Build” button (see Figure 8.15). If nothing goes wrong,

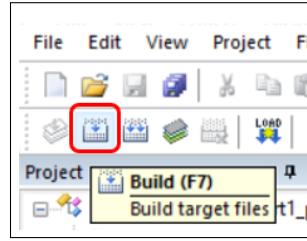


Figure 8.15: Keil IDE: Build Target

the build output window at the bottom of the IDE will show a log similar like the one shown in Figure 8.16.

```

Build Output
*** Using Compiler 'V5.06 (build 20)', folder: 'C:\Software\Keil_v5\ARM\ARMCC\Bin'
Build target 'HelloWorld SIM'
assembling startup_LPC17xx.s...
compiling system_LPC17xx.c...
compiling main.c...
compiling uart_polling.c...
linking...
Program Size: Code=924 RO-data=220 RW-data=0 ZI-data=608
".\Objects\SIM\HelloWorld.axf" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:02

```

Figure 8.16: Keil IDE: Build Target

8.2 Debug the Target

In theory, you may now load the target by pressing the LOAD button. However please *pause* before you attempt to do it. Our final goal is to build a project that is ready to be released and then load it to the on-chip flash to ship it to the customer. However we will need to do lots of debugging before we reach this goal. Keep flashing the board will greatly shorten the life of the on-chip memory since there is a limited number of times one can flash it. So for development purpose, developers rarely press the LOAD button in the IDE to load the image to the flash memory since each load action writes to the flash memory cells. Most of the time we use the simulator to debug and execute our project. We will also show you a commonly used technique to load the target to RAM, which has a lot longer life span than flash memory, and debug the target on the board by using the ULINK-ME hardware debugger in Section 8.2.2.

8.2.1 Debug the Project in Simulator

We will configure our project to use the simulator as the debugger.

1. Open up the target option window and select “Use Simulator” in the Debug tab and set the Dialog DLL and Parameters as shown Figure 8.17.

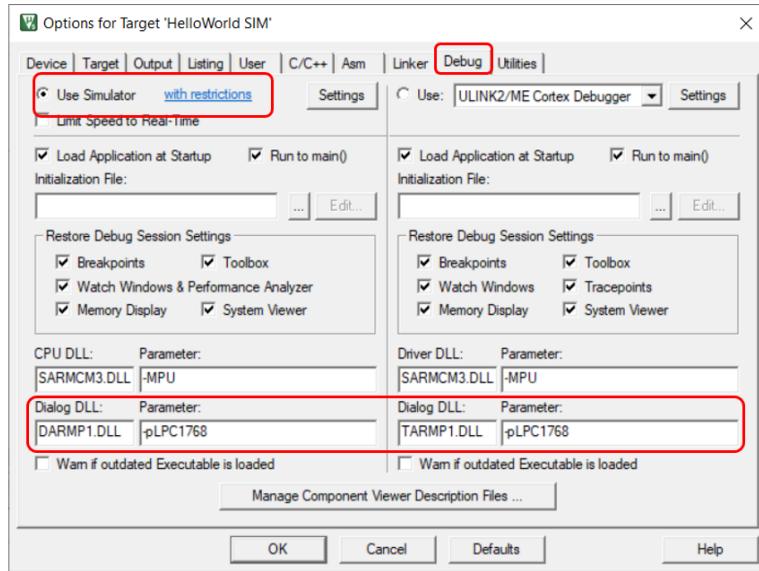


Figure 8.17: Keil IDE: Target Options Debug Tab Configuration

2. Press the “debug” button to bring up the debugger interface (See Figure 8.18).

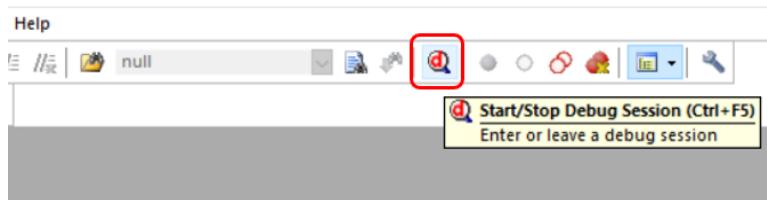


Figure 8.18: Keil IDE: Debug Button

3. Select UART1 and UART2 (see Figure 8.19) from the serial window drop down list so that they appear in simulator (see Figure 8.20). Note that the hardware UART index starts from 0 and the simulator UART index starts from 1. So the UART1 window in simulator is for the UART0 on the board. The UART2 window in simulator is for the UART1 on the board.

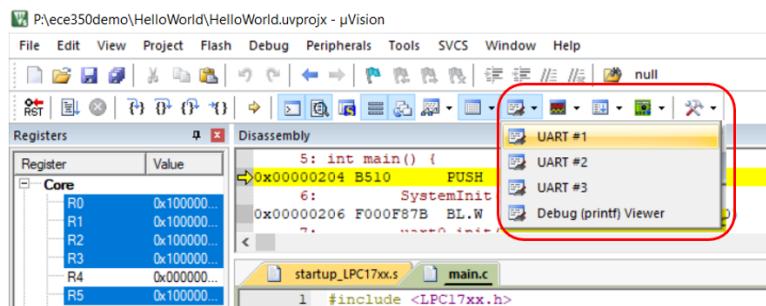


Figure 8.19: Keil IDE: Debugging. Enable Serial Window View.

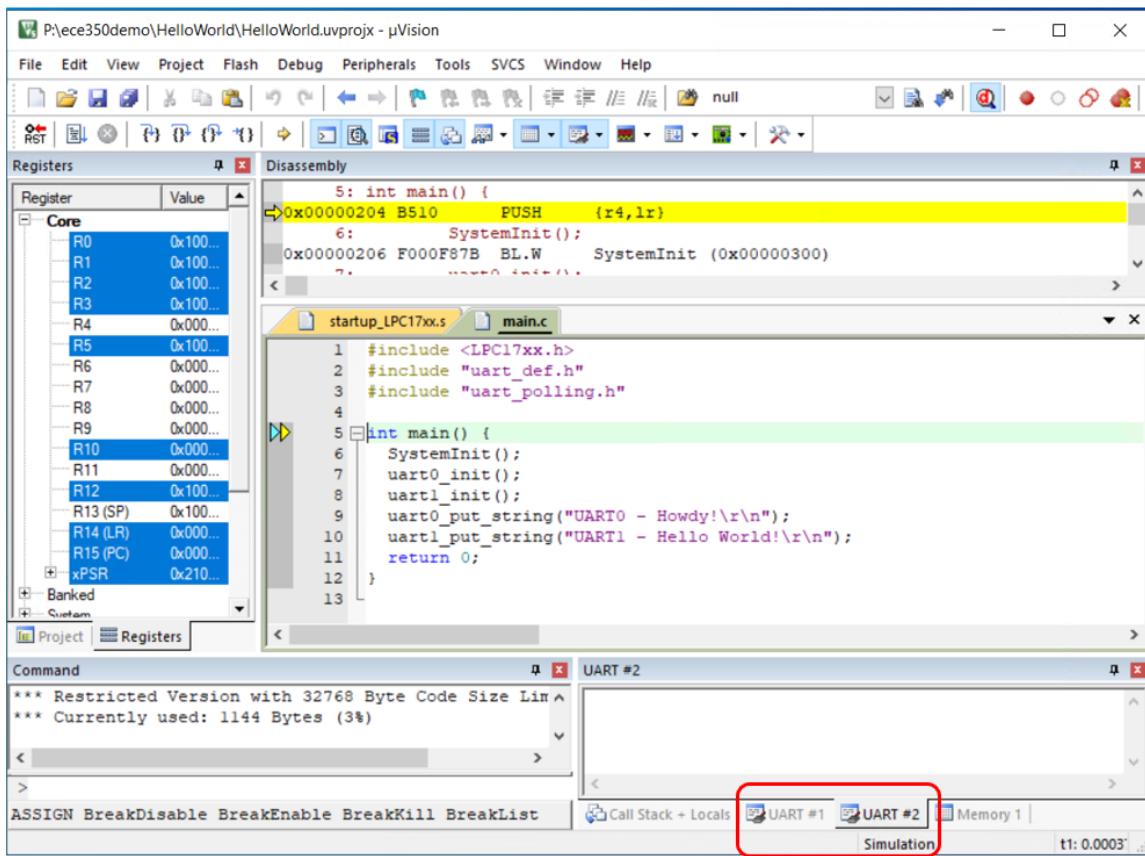


Figure 8.20: Keil IDE: Debugging. Both UART0 and UART1 views are enabled in simulator.

4. Press the “Run” button on the menu to let the program execute (see Figure 8.21). You will see the output of UART0 appearing in UART1 simulator window and the output of UART1 appearing in UART2 simulator window (see Figure 8.22). Note that we moved the UART windows from their default positions in the simulator for better view.

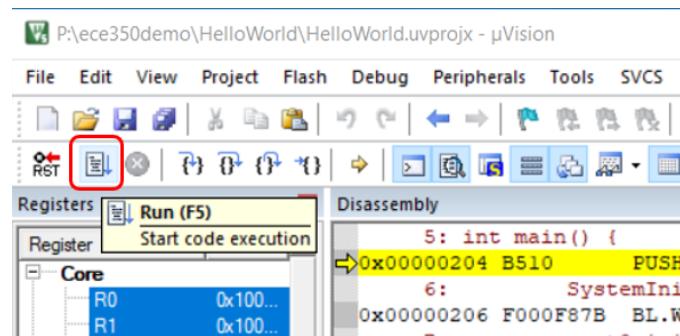


Figure 8.21: Keil IDE: Debugging. The Run Button.

5. To exit the debugging session, press the “debug” button again (see Figure 8.18).

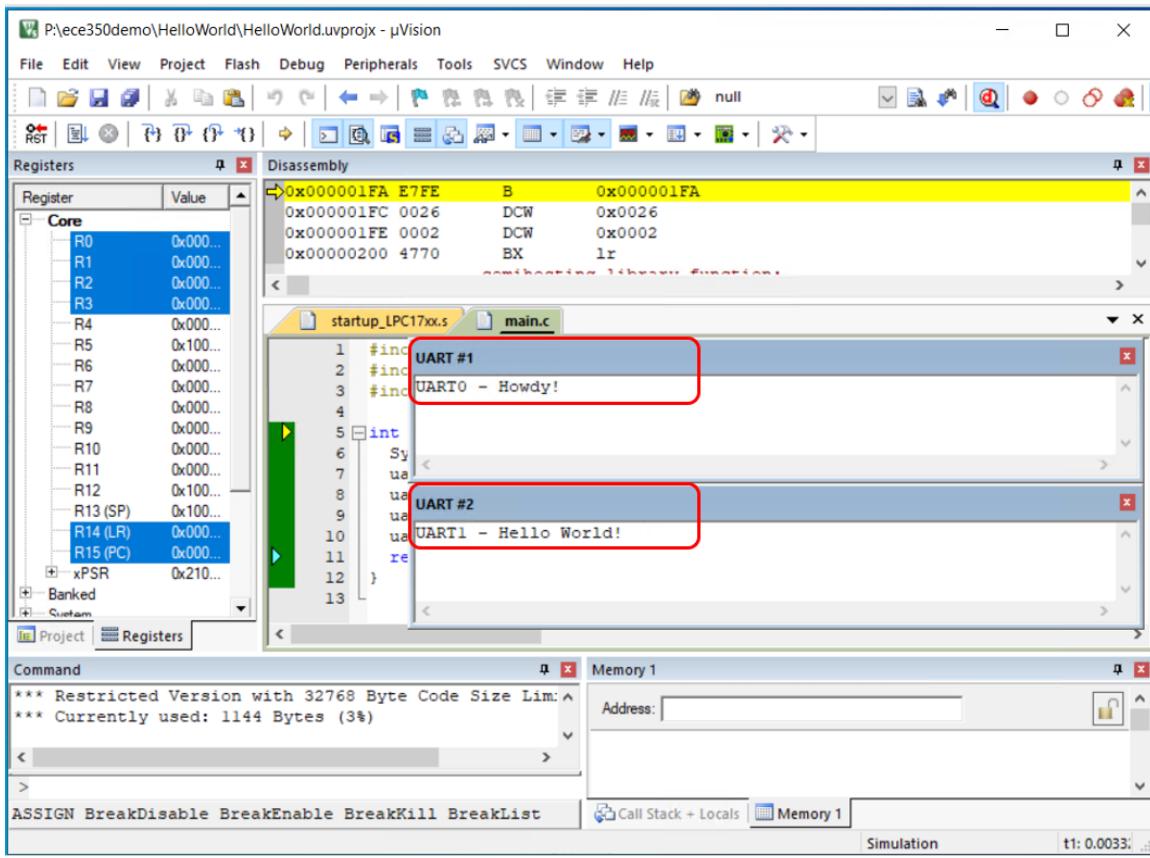


Figure 8.22: Keil IDE: Debugging Output.

8.2.2 Debug the Project on the Board

When debugging the code on the board, we use the ULINK-ME Cortex Debugger. The code will execute on the board. You will find creating a separate hardware debug target makes the development process easier.

1. Press the Managing Project Item button (see Figure 8.23).
2. Press the New icon to create a new target and name it “HelloWorld RAM” (see Figure 8.24). The new target duplicates the HelloWorld SIM target configuration.
3. Switch your target to the newly created RAM target (See Figure 8.25). Configure in-memory code execution as shown in Figure 8.26.

The default image memory map setting is that the code is executed from the ROM (see Figure 8.13). Since the ROM portion of the code needs to be flashed in order to be executed on the board, this incurs wear-and-tear on the on-chip flash of the LPC1768. Since most attempts to write a functioning RTX will eventually require some more or less elaborate debugging, the flash memory might wear out quickly. Unlike the flash memory stick file systems where the

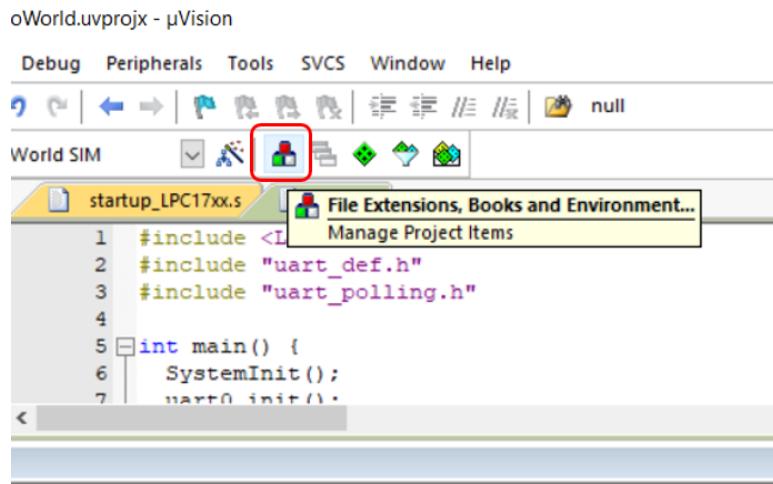


Figure 8.23: Keil IDE: Manage Project Items Button

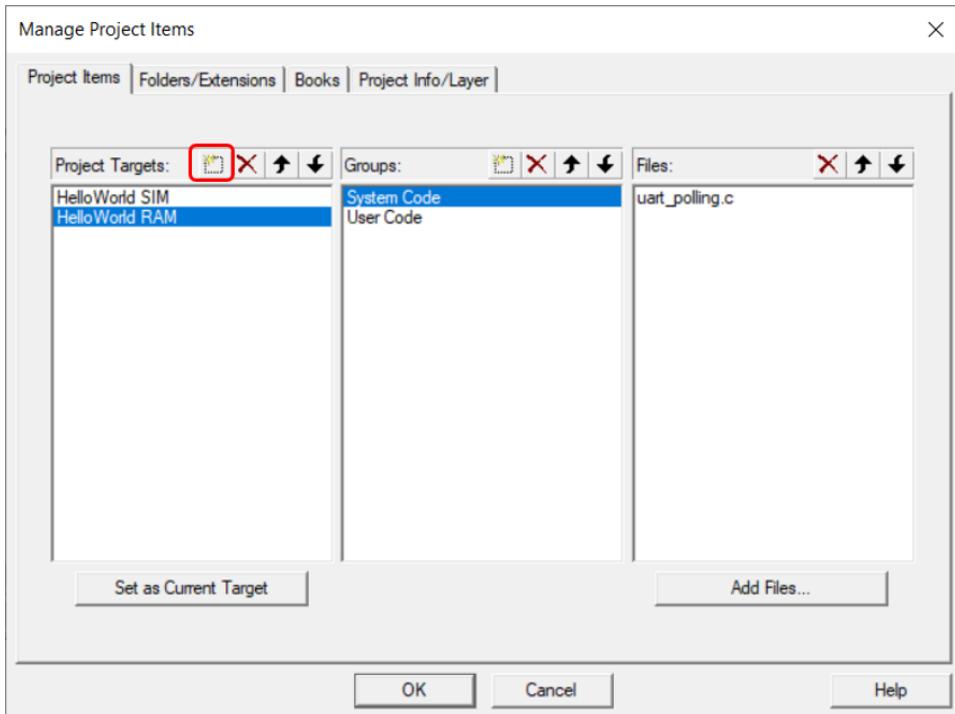


Figure 8.24: Keil IDE: Manage Project Items Window.

wear is aimed to be uniformly distributed across the memory portion, this flash memory will get used over and over again in the same portion.

The ARM compiler can be configured to have a different starting address. The configuration in Figure 8.26 makes code starting address in RAM.

4. Select the ULINK2/ME Cortex Debugger in the target options Debug tab and use an debug script RAM.ini provided in the starter code (See Figure 8.27) as

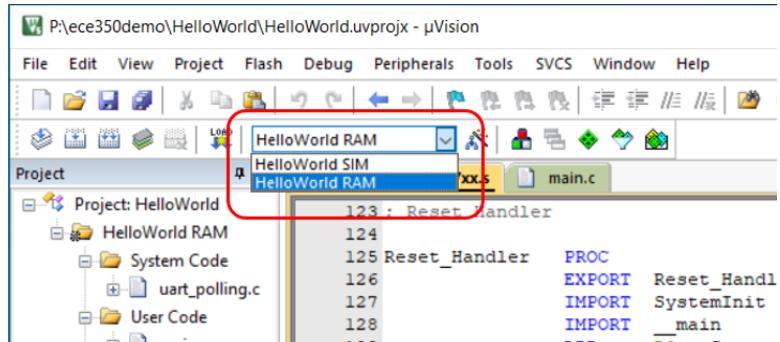


Figure 8.25: Keil IDE: Select HelloWorld RAM Target.

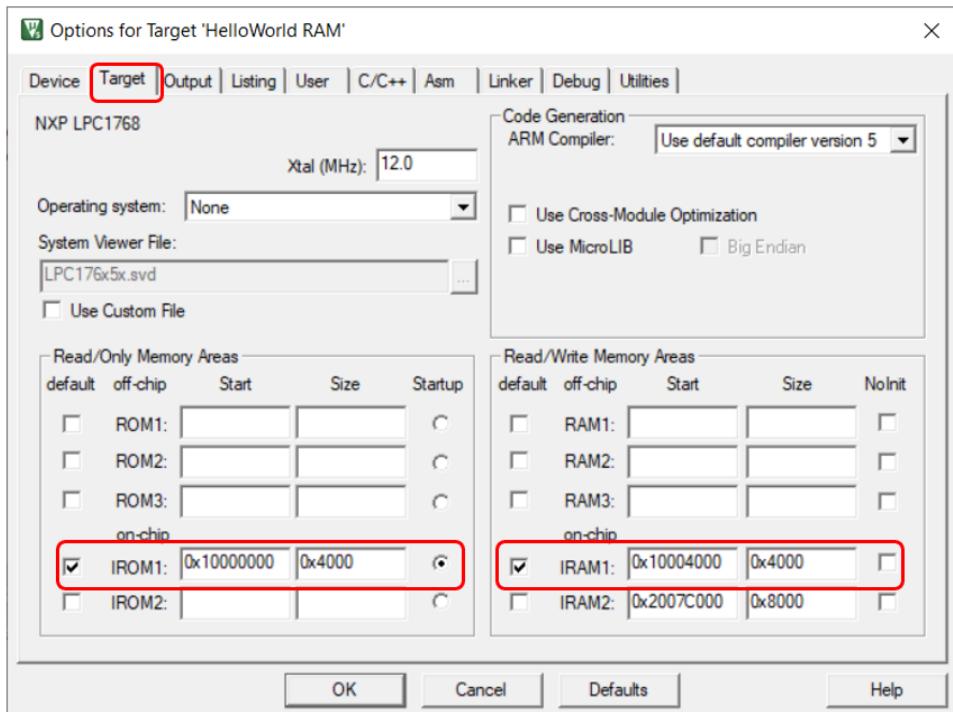


Figure 8.26: Keil IDE: Configure Target Options Target Tab for In-memory Execution.

a initialization file. An initialization file `RAM.ini` (see Listing B.1 in Appendix B) is needed to do the proper setting of SP, PC and vector table offset register.

5. Press the settings button beside the ULINK2/ME Cortex Debugger (see Figure 8.27) and select the Flash Download tab (see Figure 8.28). You should add the LPC17xx IAP 512kB Flash algorithm to the Programming Algorithm field if it is not already there.
6. Open the PuTTY terminals to see the output.

You will need a terminal emulator such as PuTTY that talks directly to COM ports in order to see output of the serial port. To find out the two COM ports,

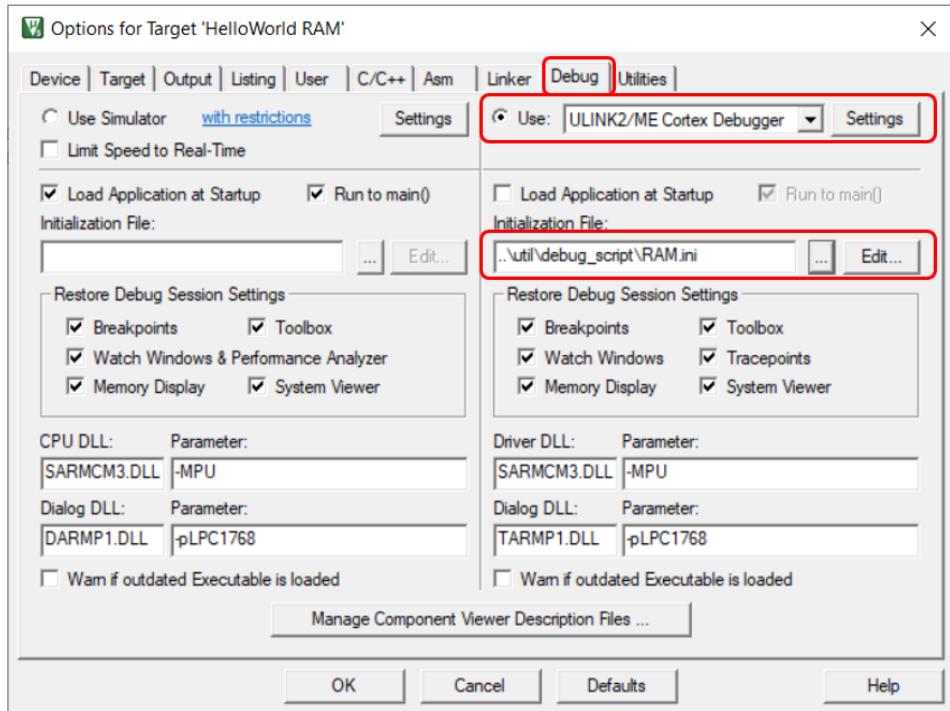


Figure 8.27: Keil IDE: Configure ULINK-ME Hardware Debugger.

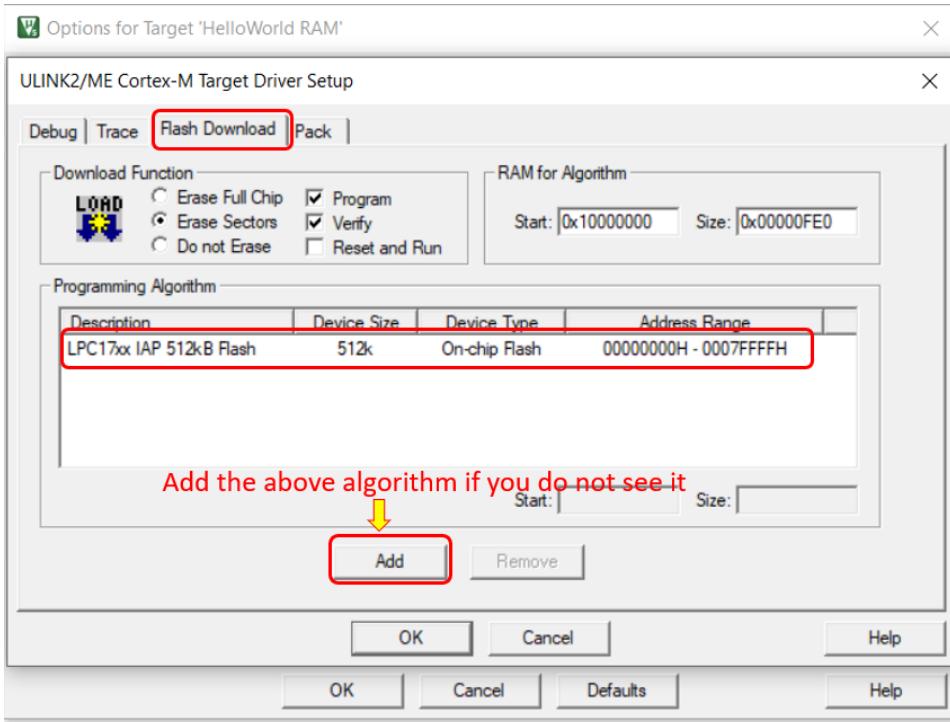


Figure 8.28: Keil IDE: Flash Download Programming Algorithm Configuration.

open up the device manager and expand the Ports (COM & LPT) line (see Figure 8.29). Note the COM port numbers are different for each lab computer. The COM port numbers may also change after a reboot of the computer. An example PuTTY Serial configuration is shown in Figures 8.30 and 8.31.

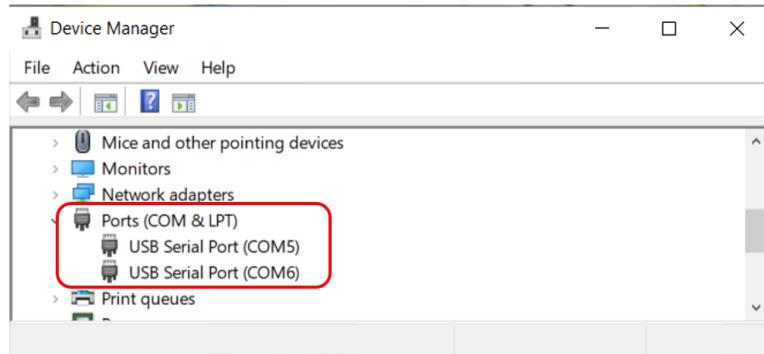


Figure 8.29: Device Manager COM Ports

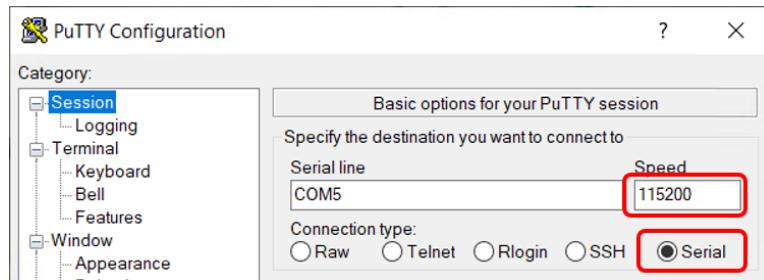


Figure 8.30: PuTTY Session for Serial Port Communication

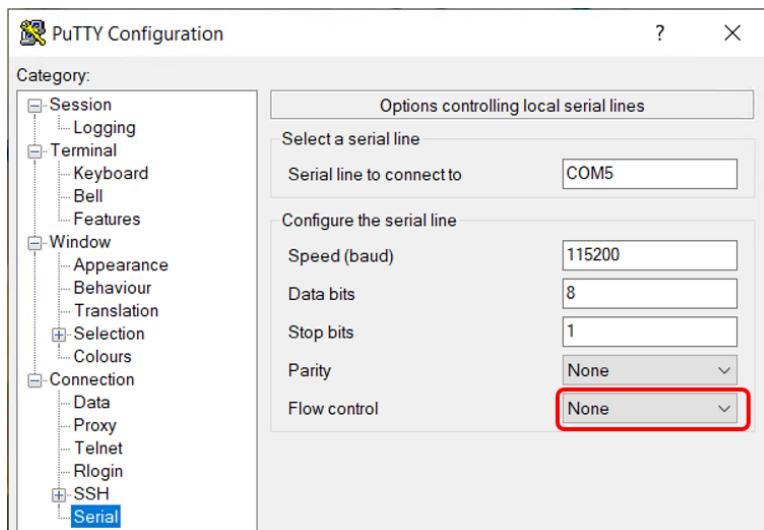


Figure 8.31: PuTTY Serial Port Configuration

7. To download the code to the board, *do not press the LOAD button*. Instead, the *debug button* is pressed to initiate a debug session and the `RAM.ini` file will load the code to the board.
8. Either step through the code or just press the Run button to execute the code till the end. You will see output from your PuTTY terminals (see Figure 8.32).



Figure 8.32: PuTTY Output

8.3 Download to ROM

Though we keep discouraging you to download the image to ROM, we walk you through the steps on how to do it to give you a feel of how a project that is ready to be released is loaded to the ROM. We expect that you already fixed your code by debugging the code on board by using the in-memory execution technique we showed you earlier. You should only do the following experiment once or twice. Please use the ROM sparingly.

Switch your target to the “HelloWorld SIM” target (see Figure 8.34). Open up the target option. Select the Debug tab and press the “Settings” button beside the ULINK2/ME Debugger (upper right portion of the window). Select the “Flash Download” tab and check the box “Reset and Run” in the Download Function section (See Figure 8.33). This will execute the code automatically without the need to press the physical reset button on the board. Apply all the changes and close the target options configuration window.

To download the code to the on-chip ROM, click the “Load” button (see Figure 8.34). The download is through the ULINK-ME. The code automatically runs. You should see the output from PuTTY terminals.

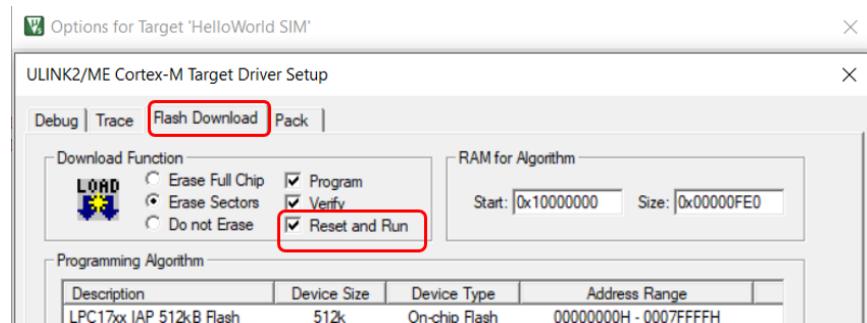


Figure 8.33: Flash Download Reset and Run Setting

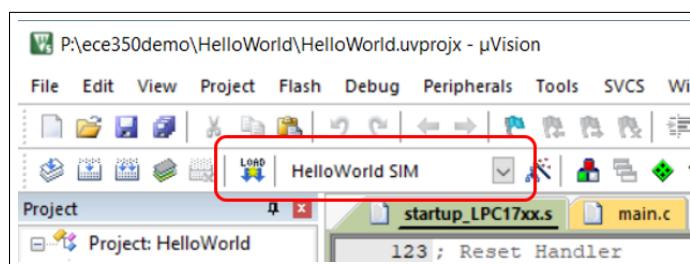


Figure 8.34: Keil IDE: Download Target to Flash

Chapter 9

Programming MCB1700

9.1 The Thumb-2 Instruction Set Architecture

The Cortex-M3 supports only the Thumb-2 (and traditional Thumb) instruction set. With support for both 16-bit and 32-bit instructions in the Thumb-2 instruction set, there is no need to switch the processor between Thumb state (16-bit instructions) and ARM state (32-bit instructions).

In the RTOS lab, you will need to program a little bit in the assembler language. We introduce a few assembly instructions that you most likely need to use in your project in this section.

The general formatting of the assembler code is as follows:

```
label
    opcode operand1, operand2, ... ; Comments
```

The `label` is optional. Normally the first operand is the destination of the operation (note `STR` is one exception).

Table 9.1 lists some assembly instructions that the RTX project may use. For complete instruction set reference, we refer the reader to Section 34.2 (ARM Cortex-M3 User Guide: Instruction Set) in [4].

9.2 ARM Architecture Procedure Call Standard (AAPCS)

The AAPCS (ARM Architecture Procedure Call Standard) defines how subroutines can be separately written, separately compiled, and separately assembled to work together. The C compiler follows the AAPCS to generate the assembly code. Table 9.2 lists registers used by the AAPCS.

Registers R0-R3 are used to pass parameters to a function and they are not preserved. The compiler does not generate assembler code to preserve the values of

| Mnemonic | Operands/Examples | Description |
|----------|----------------------|---|
| LDR | $Rt, [Rn, \#offset]$ | Load Register with word |
| | LDR R1, [R0, #24] | Load word value from memory address R0+24 into R1 |
| LDM | $Rn\{!\}, reglist$ | Load Multiple registers |
| | LDM R4, {R0 – R1} | Load word value from memory address R4 to R0, increment the address, load the value from the updated address to R1. |
| STR | $Rt, [Rn, \#offset]$ | Store Register word |
| | STR R3, [R2, R6] | Store word in R3 to memory address R2+R6 |
| | STR R1, [SP, #20] | Store word in R1 to memory address SP+20 |
| MRS | $Rd, spec_reg$ | Move from special register to general register |
| | MRS R0, MSP | Read MSP into R0 |
| | MRS R0, PSP | Read PSP into R0 |
| MSR | $spec_reg, Rm$ | Move from general register to special register |
| | MSR MSP, R0 | Write R0 to MSP |
| | MSR PSP, R0 | Write R0 to PSP |
| PUSH | $reglist$ | Push registers onto stack |
| | PUSH {R4 – R11, LR} | push in order of decreasing the register numbers |
| POP | $reglist$ | Pop registers from stack |
| | POP {R4 – R11, PC} | pop in order of increasing the register numbers |
| BL | $label$ | Branch with Link |
| | BL func | Branch to address labeled by func, return address stored in LR |
| BLX | Rm | Branch indirect with link |
| | BLX R12 | Branch with link and exchange (Call) to an address stored in R12 |
| BX | Rm | Branch indirect |
| | BX LR | Branch to address in LR, normally for function call return |

Table 9.1: Assembler instruction examples

| Register | Synonym | Special | Role in the procedure call standard |
|----------|---------|----------------|---|
| r15 | | PC | The Program Counter. |
| r14 | | LR | The Link Register. |
| r13 | | SP | The Stack Pointer (full descending stack). |
| r12 | | IP | The Intra-Procedure-call scratch register. |
| r11 | v8 | | Variable-register 8. |
| r10 | v7 | | Variable-register 7. |
| r9 | | v6 SB TR | Platform register. The meaning of this register is defined by platform standard. |
| r8 | v5 | | Variable-register 5. |
| r7 | v4 | | Variable-register 4. |
| r6 | v3 | | Variable-register 3. |
| r5 | v2 | | Variable-register 2. |
| r4 | v1 | | Variable-register 1. |
| r3 | a4 | | argument / scratch register 4 |
| r2 | a3 | | argument / scratch register 3 |
| r1 | a2 | | argument / result / scratch register 2 |
| r0 | a1 | | argument / result / scratch register 1 |

Table 9.2: Core Registers and AAPCS Usage

these registers. R0 is also used for return value of a function.

Registers R4-R11 are preserved by the called function. If the compiler generated assembler code uses registers in R4-R11, then the compiler generate assembler code to automatically push/pop the used registers in R4-R11 upon entering and exiting the function.

R12-R15 are special purpose registers. A function that has the `__svc_indirect` keyword makes the compiler put the first parameter in the function to R12 followed by an SVC instruction. R13 is the stack pointer (SP). R14 is the link register (LR), which normally is used to save the return address of a function. R15 is the program counter (PC).

Note that the exception stack frame automatically backs up R0-R3, R12, LR and PC together with the xPSR. This allows the possibility of writing the exception handler in purely C language without the need of having a small piece of assembly code to save/restore R0-R3, LR and PC upon entering/exiting an exception handler routine.

9.3 Cortex Microcontroller Software Interface Standard (CMSIS)

The Cortex Microcontroller Software Interface Standard (CMSIS) was developed by ARM. It provides a standardized access interface for embedded software products (see Figure 9.1). This improves software portability and re-usability. It enables soft-

ware solution suppliers to develop products that can work seamlessly with device libraries from various silicon vendors [2].

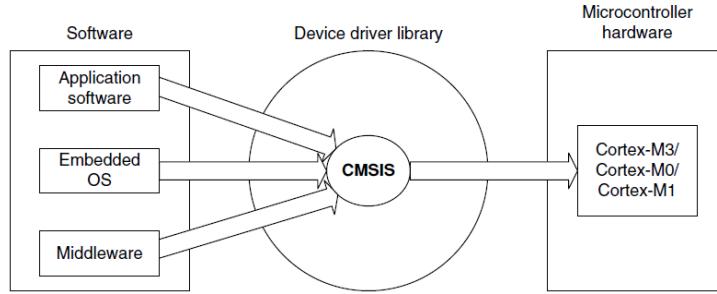


Figure 9.1: Role of CMSIS[5]

The CMSIS uses standardized methods to organize header files that makes it easy to learn new Cortex-M microcontroller products and improve software portability. With the `<device>.h` (e.g. `LPC17xx.h`) and system startup code files (e.g., `startup_LPC17xx.s`), your program has a common way to access

- **Cortex-M processor core registers** with standardized definitions for NVIC, SysTick, MPU registers, System Control Block registers , and their core access functions (see `core_cm *.[ch]` files).
- **system exceptions** with standardized exception number and handler names to allow RTOS and middleware components to utilize system exceptions without having compatibility issues.
- **intrinsic functions with standardized name** to produce instructions that cannot be generated by IEC/ISO C.
- **system initialization** by common methods for each MCU. Fore example, the standardized `SystemInit()` function to configure clock.
- **system clock frequency** with standardized variable named as `SystemFrequency` defined in the device driver.
- **vendor peripherals** with standardized C structure.

9.3.1 CMSIS files

The CMSIS is divided into multiple layers (See Figure 9.2). For each device, the MCU vendor provides a device header file `<device>.h` (e.g., `LPC17xx.h`) which pulls in additional header files required by the device driver library and the Core Peripheral Access Layer (see Figure 9.3).

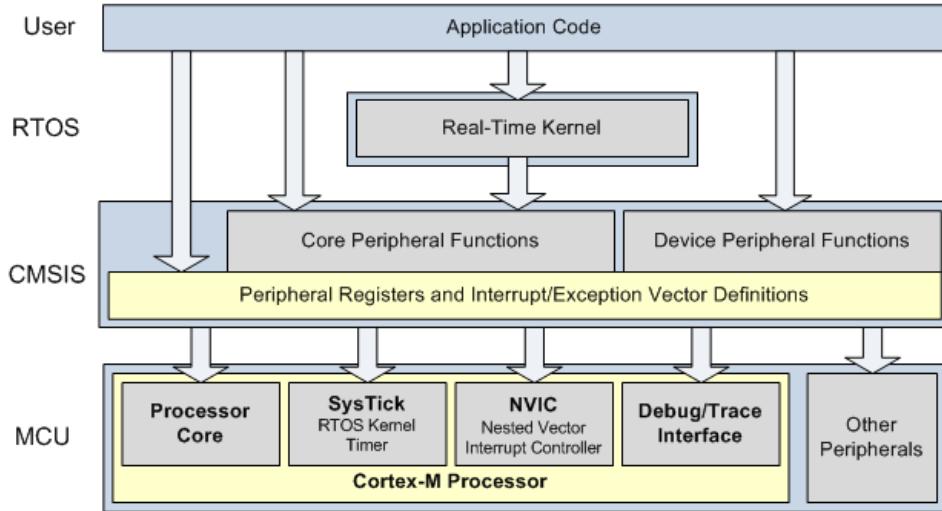


Figure 9.2: CMSIS Organization[2]

By including the `<device>.h` (e.g., `LPC17xx.h`) file into your code file. The first step to initialize the system can be done by calling the CMSIS function as shown in Listing 9.1.

```
SystemInit(); // Initialize the MCU clock
```

Listing 9.1: CMSIS SystemInit()

The CMSIS compliant device drivers also contain a startup code (e.g., `startup_LPC17xx.s`), which include the vector table with standardized exception handler names (See Section 9.3.3).

9.3.2 Cortex-M Core Peripherals

We only introduce the NVIC programming in this section. The Nested Vectored Interrupt Controller (NVIC) can be accessed by using CMSIS functions (see Figure 9.4). As an example, the following code enables the UART0 and TIMER0 interrupt

```
NVIC_EnableIRQ(UART0_IRQn); // UART0_IRQn is defined in LPC17xx.h
NVIC_EnableIRQ(TIMER0_IRQn); // TIMER0_IRQn is defined in LPC17xx.h
```

9.3.3 System Exceptions

Writing an exception handler becomes very easy. One just defines a function that takes no input parameter and returns void. The function takes the name of the standardized exception handler name as defined in the startup code (e.g., `startup_LPC17xx.s`).

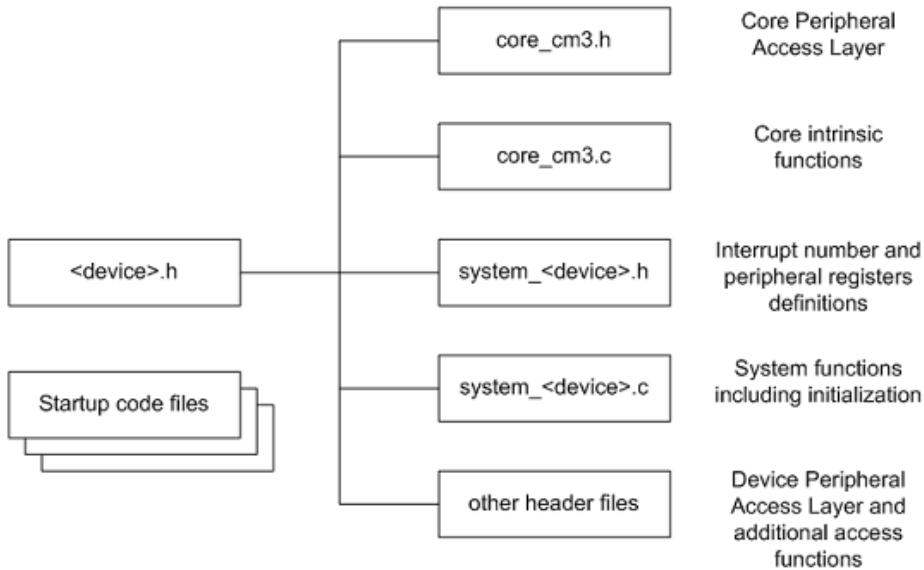


Figure 9.3: CMSIS Organization[2]

| Function definition | | Description |
|---------------------|--|--|
| void | NVIC_SystemReset (void) | Resets the whole system including peripherals. |
| void | NVIC_SetPriorityGrouping (uint32_t priority_grouping) | Sets the priority grouping. |
| uint32_t | NVIC_GetPriorityGrouping (void) | Returns the value of the current priority grouping. |
| void | NVIC_EnableIRQ (IRQn_Type IRQn) | Enables the interrupt IRQn. |
| void | NVIC_DisableIRQ (IRQn_Type IRQn) | Disables the interrupt IRQn. |
| void | NVIC_SetPriority (IRQn_Type IRQn, int32_t priority) | Sets the priority for the interrupt IRQn. |
| uint32_t | NVIC_GetPriority (IRQn_Type IRQn) | Returns the priority for the specified interrupt. |
| void | NVIC_SetPendingIRQ (IRQn_Type IRQn) | Sets the interrupt IRQn pending. |
| IRQn_Type | NVIC_GetPendingIRQ (IRQn_Type IRQn) | Returns the pending status of the interrupt IRQn. |
| void | NVIC_ClearPendingIRQ (IRQn_Type IRQn) | Clears the pending status of the interrupt IRQn, if it is not already running or active. |
| IRQn_Type | NVIC_GetActive (IRQn_Type IRQn) | Returns the active status for the interrupt IRQn. |

Figure 9.4: CMSIS NVIC Functions[2]

The following listing shows an example to write the UART0 interrupt handler entirely in C.

```

void UART0_Handler ( void )
{
    // write your IRQ here
}

```

Another way is to use the embedded assembly code:

| Instruction | CMSIS Intrinsic Function | |
|------------------|--------------------------|------------------------------------|
| CPSIE I | void __enable_irq(void) | |
| CPSID I | void __disable_irq(void) | |
| Special Register | Access | CMSIS Function |
| CONTROL | Read | uint32_t __get_CONTROL(void) |
| | Write | void __set_CONTROL(uint32_t value) |
| MSP | Read | uint32_t __get_MSP(void) |
| | Write | void __set_MSP(uint32_t value) |
| PSP | Read | uint32_t __get_PSP(void) |
| | Write | void __set_PSP(uint32_t value) |

Table 9.3: CMSIS intrinsic functions defined in `core_cmFunc.h`

```
__asm void UART0_Handler(void)
{
    ; do some asm instructions here
    BL __cpp(a_c_function) ; a_c_function is a regular C function
    ; do some asm instructions here,
}
```

9.3.4 Intrinsic Functions

ANSI cannot directly access some Cortex-M3 instructions. The CMSIS provides intrinsic functions that can generate these instructions. The CMSIS also provides a number of functions for accessing the special registers using MRS and MSR instructions. The intrinsic functions are provided by the RealView Compiler. Table 9.3 lists some intrinsic functions that your RTOS project most likely will need to use. We refer the reader to Tables 613 and 614 one page 650 in Section 34.2.2 of [4] for the complete list of intrinsic functions.

9.3.5 Vendor Peripherals

All vendor peripherals are organized as C structure in the `<device>.h` file (e.g., `LPC17xx.h`). For example, to read a character received in the RBR of UART0, we can use the following code.

```
unsigned char ch;
ch = LPC_UART0->RBR; // read UART0 RBR and save it in ch
```

9.4 Accessing C Symbols from Assembly

Only embedded assembly is support in Cortex-M3. To write an embedded assembly function, you need to use the `__asm` keyword. For example the the function “`embedded_asm_function`” in Listing ?? is an embedded assembly function. You can only put assembly instructions inside this function. Note that inline assembly is not supported in Cortex-M3.

The `__cpp` keyword allows one to access C compile-time constant expressions, including the addresses of data or functions with external linkage, from the assembly code. The expression inside the `__cpp` can be one of the followings:

- A global variable defined in C. In Listing 9.2, we have two C global variables `g_pcb` and `g_var`. We can use the `__cpp` to access them as shown in Listing 9.3.

```
#define U32 unsigned int
#define SP_OFFSET 4

typedef struct pcb {
    struct pcb *mp_next;
    U32 *mp_sp; // 4 bytes offset from the starting address of
                 // this structure
    //other variables...
} PCB;

PCB g_pcb;
U32 g_var;
```

Listing 9.2: Example of accessing C global variables from assembly. The C code.

```
__asm embedded_asm_function(void) {
    LDR R3,=__cpp(&g_pcb) ; load R3 with the address of g_pcb
    LDM R3, {R1, R2}      ; load R1 with g_pcb.mp_next
                           ; load R2 with g_pcb.mp_sp
    LDR R4,=__cpp(g_var) ; load R4 with the value of g_var
    STR R4, [R3, #SP_OFFSET] ; write R4 value to g_pcb.mp_sp
}
```

Listing 9.3: Example of accessing global variable from assembly

- A C function. In Listing 9.4, `a_c_function` is a function written in C. We can invoke this function by using the assembly language.

```
extern void a_c_function(void);
...
__asm embedded_asm_function(void) {
    .....
    BL __cpp(a_c_function) ; a_c_function is regular C function
    .....
}
```

Listing 9.4: Example of accessing c function from assembly

- A constant expression in the range of 0 – 255 defined in C. In Listing 9.5, `g_flag` is such a constant. We can use `MOV` instruction on it. Note the `MOV` instruction only applies to immediate constant value in the range of 0 – 255.

```
unsigned char const g_flag;

__asm embedded_asm_function(void) {
;.....
MOV R4, #__cpp(g_flag) ; load g_flag value into R4
;.....
}
```

Listing 9.5: Example of accessing constant from assembly

You can also use the `IMPORT` directive to import a C symbol in the embedded assembly function and then start to use the imported symbol just as a regular assembly symbol (see Listing 9.6).

```
void a_c_function (void) {
    // do something
}

__asm embedded_asm_add(void) {
    IMPORT a_c_function ; a_c_function is a regular C function
    BL a_c_function ; branch with link to a_c_function
}
```

Listing 9.6: Example of using `IMPORT` directive to import a C symbol.

Names in the `#__cpp` expression are looked up in the C context of the `__asm` function. Any names in the result of the `#__cpp` expression are mangled as required and automatically have `IMPORT` statements generated from them.

9.5 SVC Programming: Writing an RTX API Function

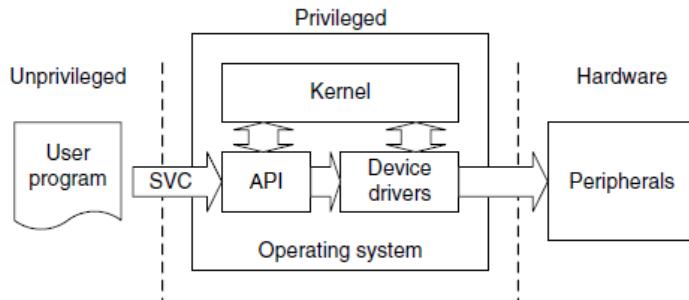


Figure 9.5: SVC as a Gateway for OS Functions [5]

A function in RTX API requires a service from the operating system. It needs to be implemented through the proper gateway by *trapping* from the user level into the kernel level. On Cortex-M3, the SVC instruction is used to achieve this purpose.

The basic idea is that when a function in RTX API is called from the user level, this function will trigger an SVC instruction. The SVC_Handler, which is the CM-SIS standardized exception handler for SVC exception will then invoke the kernel function that provides the actual service (see Figure 9.5). Effectively, the RTX API function is a wrapper that invokes SVC exception handler and passes corresponding kernel service operation information to the SVC handler.

To generate an SVC instruction, there are two methods. One is a direct method and the other one is an indirect method.

The direct method is to program at assembly instruction level. We can use the embedded assembly mechanism and write SVC assembly instruction inside the embedded assembly function. One implementation of `void *mem_alloc(size_t size)` is shown in Listing 9.7.

```
__asm void *mem_alloc(size_t size) {
    LDR R12,=__cpp(k_mem_alloc)
    ; privileged mode code handling omitted
    SVC 0
    BX LR
    ALIGN
}
```

Listing 9.7: Code Snippet of mem_alloc

The corresponding kernel function is the C function `k_mem_alloc`. This function entry point is loaded to register `r12`. Then `SVC 0` causes an SVC exception with immediate number 0. In the SVC exception handler, we can then branch with link and exchange to the address stored in `r12`. Listing 9.8 is an excerpt of the `HAL.c` from the starter code.

```
__asm void SVC_Handler(void) {
    MRS R0, PSP

    ; Extract SVC number, if SVC 0, then do the following
    LDM R0, {R0-R3, R12}; Read R0-R3, R12 from stack

    ; code to save cpu registers omitted

    BLX R12 ; R12 contains the kernel function entry point

    ; Code to restore registers omitted

    MVN LR, #:NOT:0xFFFFFFF; set EXC_RETURN, thread mode, PSP
    BX LR
}
}
```

Listing 9.8: Code Snippet of SVC_Handler

The indirect method is to ask the compiler to generate the SVC instruction from C code. The ARM compiler provides an intrinsic keyword named `__svc_indirect` which passes an operation code to the SVC handler in `r12[3]`. This keyword is a function qualifier. The two inputs we need to provide to the compiler are

- `svc_num`, the immediate value used in the SVC instruction and
- `op_num`, the value passed in `r12` to the handler to determine the function to perform. The following is the syntax of an indirect SVC.

```
__svc_indirect(int svc_num)
    return_type function_name(int op_num[, argument-list]);
```

The system handler must make use of the `r12` value to select the required operation. For example, the `mem_alloc` is a user function with the following signature:

```
#include <rtx.h>
void *mem_alloc(size_t size);
```

In `rtx.h`, the following code is relevant to the implementation of the function.

```
#define __SVC_0 __svc_indirect(0)
extern void *k_mem_alloc(size_t size);
#define mem_alloc(size) _mem_alloc((U32)k_mem_alloc, size);
extern void *_mem_alloc(U32 p_func, size_t size) __SVC_0;
```

The compiler generates two assembly instructions

```
LDR.W r12, [pc, #offset]; Load k_mem_alloc into r12
SVC 0x00
```

The `SVC_handler` in Listing 9.8 then can be used to handle the `SVC 0` exception.

9.6 UART Programming

To program a UART on MCB1700 board, one first needs to configure the UART by following the steps listed in Section 15.1 in [4] (referred as `LPC17xx UM` in the sample code comments). Listings 9.9, 9.10 and 9.11 give one sample implementation of programming UART0 interrupts.

```
/** 
 * @brief: UART defines
 * @file: uart_def.h
 * @author: Yiqing Huang
```

```

* @date: 2014/02/08
*/
#ifndef UART_DEF_H_
#define UART_DEF_H_

/* The following macros are from NXP uart.h */
#define IER_RBR 0x01
#define IER_THRE 0x02
#define IER_RLS 0x04

#define IIR_PEND 0x01
#define IIR_RLS 0x03
#define IIR_RDA 0x02
#define IIR_CTI 0x06
#define IIR_THRE 0x01

#define LSR_RDR 0x01
#define LSR_OE 0x02
#define LSR_PE 0x04
#define LSR_FE 0x08
#define LSR_BI 0x10
#define LSR_THRE 0x20
#define LSR_TEMT 0x40
#define LSR_RXFE 0x80

#define BUFSIZE 0x40
/* end of NXP uart.h file reference */

/* convenient macro for bit operation */
#define BIT(X) ( 1 << X )

/*
  8 bits, no Parity, 1 Stop bit

0x83 = 1000 0011 = 1 0 00 0 0 11
LCR[7] =1 enable Divisor Latch Access Bit DLAB
LCR[6] =0 disable break transmission
LCR[5:4]=00 odd parity
LCR[3] =0 no parity
LCR[2] =0 1 stop bit
LCR[1:0]=11 8-bit char len
See table 279, pg306 LPC17xx_UM
*/
#define UART_8N1 0x83

#ifndef NULL
#define NULL 0
#endif

#endif /* !UART_DEF_H_ */

```

Listing 9.9: UART0 IRQ Sample Code uart_def.h

```
/**  
 * @brief: uart.h  
 * @author: Yiqing Huang  
 * @date: 2014/02/08  
 */  
  
#ifndef UART_IRQ_H_  
#define UART_IRQ_H_  
  
/* typedefs */  
#include <stdint.h>  
#include "uart_def.h"  
  
/* The following macros are from NXP uart.h */  
/*  
#define IER_RBR 0x01  
#define IER_THRE 0x02  
#define IER_RLS 0x04  
  
#define IIR_PEND 0x01  
#define IIR_RLS 0x03  
#define IIR_RDA 0x02  
#define IIR_CTI 0x06  
#define IIR_THRE 0x01  
  
#define LSR_RDR 0x01  
#define LSR_OE 0x02  
#define LSR_PE 0x04  
#define LSR_FE 0x08  
#define LSR_BI 0x10  
#define LSR_THRE 0x20  
#define LSR_TEMT 0x40  
#define LSR_RXFE 0x80  
  
#define BUFSIZE 0x40  
*/  
/* end of NXP uart.h file reference */  
  
/* convenient macro for bit operation */  
//#define BIT(X) ( 1 << X )  
  
/*  
 8 bits, no Parity, 1 Stop bit  
  
0x83 = 1000 0011 = 1 0 00 0 0 11  
LCR[7] =1 enable Divisor Latch Access Bit DLAB  
LCR[6] =0 disable break transmission  
LCR[5:4]=0 odd parity  
LCR[3] =0 no parity
```

```

LCR[2] =0 1 stop bit
LCR[1:0]=11 8-bit char len
See table 279, pg306 LPC17xx_UM
*/
//#define UART_8N1 0x83

#define uart0_irq_init() uart_irq_init(0)
#define uart1_irq_init() uart_irq_init(1)

/* initialize the n_uart to use interrupt */
int uart_irq_init(int n_uart);

#endif /* ! UART_IRQ_H */

```

Listing 9.10: UART0 IRQ Sample Code uart.h

```

/**
 * @brief: uart_irq.c
 * @author: NXP Semiconductors
 * @author: Y. Huang
 * @date: 2014/02/08
 */

#include <LPC17xx.h>
#include "uart.h"
#include "uart_polling.h"
#ifndef DEBUG_0
#include "printf.h"
#endif

uint8_t g_buffer[] = "You Typed a Q\n\r";
uint8_t *gp_buffer = g_buffer;
uint8_t g_send_char = 0;
uint8_t g_char_in;
uint8_t g_char_out;

/**
 * @brief: initialize the n_uart
 * NOTES: It only supports UART0. It can be easily extended to support
 *        UART1 IRQ.
 * The step number in the comments matches the item number in Section 14.1
 *        on pg 298
 * of LPC17xx_UM
 */
int uart_irq_init(int n_uart) {

    LPC_UART_TypeDef *pUart;

    if ( n_uart ==0 ) {
        /*
        Steps 1 & 2: system control configuration.
        Under CMSIS, system_LPC17xx.c does these two steps

```

```

-----  

Step 1: Power control configuration.  

    See table 46 pg63 in LPC17xx_UM  

-----  

Enable UART0 power, this is the default setting  

done in system_LPC17xx.c under CMSIS.  

Enclose the code for your refrence  

//LPC_SC->PCONF |= BIT(3);  

-----  

Step2: Select the clock source.  

    Default PCLK=CCLK/4 , where CCLK = 100MHZ.  

    See tables 40 & 42 on pg56-57 in LPC17xx_UM.  

-----  

Check the PLL0 configuration to see how XTAL=12.0MHZ  

gets to CCLK=100MHZin system_LPC17xx.c file.  

PCLK = CCLK/4, default setting after reset.  

Enclose the code for your reference  

//LPC_SC->PCLKSEL0 &= ~(BIT(7)|BIT(6));  

-----  

Step 5: Pin Ctrl Block configuration for TXD and RXD  

    See Table 79 on pg108 in LPC17xx_UM.  

-----  

Note this is done before Steps3-4 for coding purpose.  

*/  

/* Pin P0.2 used as TXD0 (Com0) */  

LPC_PINCON->PINSEL0 |= (1 << 4);  

/* Pin P0.3 used as RXD0 (Com0) */  

LPC_PINCON->PINSEL0 |= (1 << 6);  

pUart = (LPC_UART_TypeDef *) LPC_UART0;  

} else if ( n_uart == 1) {  

    /* see Table 79 on pg108 in LPC17xx_UM */  

    /* Pin P2.0 used as TXD1 (Com1) */  

    LPC_PINCON->PINSEL4 |= (2 << 0);  

    /* Pin P2.1 used as RXD1 (Com1) */  

    LPC_PINCON->PINSEL4 |= (2 << 2);  

    pUart = (LPC_UART_TypeDef *) LPC_UART1;  

} else {  

    return 1; /* not supported yet */  

}  

/*
-----  

Step 3: Transmission Configuration.

```

```

    See section 14.4.12.1 pg313-315 in LPC17xx_UM
    for baud rate calculation.

-----
*/



/* Step 3a: DLAB=1, 8N1 */
pUart->LCR = UART_8N1; /* see uart.h file */

/* Step 3b: 115200 baud rate @ 25.0 MHZ PCLK */
pUart->DLM = 0; /* see table 274, pg302 in LPC17xx_UM */
pUart->DLL = 9; /* see table 273, pg302 in LPC17xx_UM */

/* FR = 1.507 ~ 1/2, DivAddVal = 1, MulVal = 2
   FR = 1.507 = 25MHZ/(16*9*115200)
   see table 285 on pg312 in LPC_17xxUM
*/
pUart->FDR = 0x21;

-----



/*
-----



Step 4: FIFO setup.
    see table 278 on pg305 in LPC17xx_UM
-----
enable Rx and Tx FIFOs, clear Rx and Tx FIFOs
Trigger level 0 (1 char per interrupt)
*/
pUart->FCR = 0x07;

/* Step 5 was done between step 2 and step 4 a few lines above */

/*
-----



Step 6 Interrupt setting and enabling
-----
*/
/* Step 6a:
   Enable interrupt bit(s) wihtin the specific peripheral register.
   Interrupt Sources Setting: RBR, THRE or RX Line Stats
   See Table 50 on pg73 in LPC17xx_UM for all possible UART0 interrupt
   sources
   See Table 275 on pg 302 in LPC17xx_UM for IER setting
*/
/* disable the Divisor Latch Access Bit DLAB=0 */
pUart->LCR &= ~(BIT(7));

//pUart->IER = IER_RBR | IER_THRE | IER_RLS;
pUart->IER = IER_RBR | IER_RLS;

/* Step 6b: enable the UART interrupt from the system level */

if ( n_uart == 0 ) {

```

```

        NVIC_EnableIRQ(UART0_IRQn); /* CMSIS function */
    } else if ( n_uart == 1 ) {
        NVIC_EnableIRQ(UART1_IRQn); /* CMSIS function */
    } else {
        return 1; /* not supported yet */
    }
    pUart->THR = '\0';
    return 0;
}

/***
 * @brief: use CMSIS ISR for UART0 IRQ Handler
 * NOTE: This example shows how to save/restore all registers rather than
 *       just
 *       those backed up by the exception stack frame. We add extra
 *       push and pop instructions in the assembly routine.
 *       The actual c_UART0_IRQHandler does the rest of irq handling
 */
__asm void UART0_IRQHandler(void)
{
    PRESERVE8
    IMPORT c_UART0_IRQHandler
    PUSH{r4-r11, lr}
    BL c_UART0_IRQHandler
    POP{r4-r11, pc}
}

/***
 * @brief: c UART0 IRQ Handler
 */
void c_UART0_IRQHandler(void)
{
    uint8_t IIR_IntId; // Interrupt ID from IIR
    LPC_UART_TypeDef *pUart = (LPC_UART_TypeDef *)LPC_UART0;

#ifdef DEBUG_0
    uart1_put_string("Entering c_UART0_IRQHandler\n\r");
#endif // DEBUG_0

    /* Reading IIR automatically acknowledges the interrupt */
    IIR_IntId = (pUart->IIR) >> 1; // skip pending bit in IIR
    if (IIR_IntId & IIR_RDA) { // Receive Data Available
        /* read UART. Read RBR will clear the interrupt */
        g_char_in = pUart->RBR;
#ifdef DEBUG_0
        uart1_put_string("Reading a char = ");
        uart1_put_char(g_char_in);
        uart1_put_string("\n\r");
#endif // DEBUG_0

        g_buffer[12] = g_char_in; // nasty hack
        g_send_char = 1;
    } else if (IIR_IntId & IIR_THRE) {
        /* THRE Interrupt, transmit holding register becomes empty */

```

```

    if (*gp_buffer != '\0' ) {
        g_char_out = *gp_buffer;
#ifdef DEBUG_0
        //uart1_put_string("Writing a char = ");
        //uart1_put_char(g_char_out);
        //uart1_put_string("\n\r");

        // you could use the printf instead
        printf("Writing a char = %c \n\r", g_char_out);
#endif // DEBUG_0
        pUart->THR = g_char_out;
        gp_buffer++;
    } else {
#ifdef DEBUG_0
        uart1_put_string("Finish writing. Turning off IER_THRE\n\r");
#endif // DEBUG_0
        pUart->IER ^= IER_THRE; // toggle the IER_THRE bit
        pUart->THR = '\0';
        g_send_char = 0;
        gp_buffer = g_buffer;
    }

} else { /* not implemented yet */
#ifdef DEBUG_0
    uart1_put_string("Should not get here!\n\r");
#endif // DEBUG_0
    return;
}
}

```

Listing 9.11: UART0 IRQ Sample Code `uart_irq.c`

Listings 9.12 and 9.13 give one sample implementation of programming UART0 by polling.

```

/***
 * @brief: uart_polling.h
 * @author: Yiqing Huang
 * @date: 2014/01/05
 */

#ifndef UART_POLLING_H_
#define UART_POLLING_H_

#include <stdint.h> /* typedefs */
#include "uart_def.h"

#define uart0_init() uart_init(0)
#define uart0_get_char() uart_get_char(0)
#define uart0_put_char(c) uart_put_char(0,c)
#define uart0_put_string(s) uart_put_string(0,s)

#define uart1_init() uart_init(1)

```

```

#define uart1_get_char() uart_get_char(1)
#define uart1_put_char(c) uart_put_char(1,c)
#define uart1_put_string(s) uart_put_string(1,s)

int uart_init(int n_uart); /* initialize the n_uart */
int uart_get_char(int n_uart); /* read a char from the n_uart */
int uart_put_char(int n_uart, unsigned char c); /* write a char to n_uart
   */
int uart_put_string(int n_uart, unsigned char *s); /* write a string to
   n_uart */
void putc(void *p, char c); /* call back function for printf, use uart1
   */

#endif /* ! UART_POLLING_H_ */

```

Listing 9.12: UART0 IRQ Sample Code `uart_polling.h`

```

/**
 * @brief: uart_polling.c, polling UART to send and receive data
 * @author: Yiqing Huang
 * @date: 2014/01/05
 * NOTE: the code only handles UART0 for now.
 */

#include <LPC17xx.h>
#include "uart_polling.h"

/**
 * @brief: initialize the n_uart
 * NOTES: only tested uart0 so far, but can be easily extended to other
 *        uarts.
 *        it should work with uart1, but no testing was done.
 */
int uart_init(int n_uart) {

    LPC_UART_TypeDef *pUart; /* ptr to memory mapped device UART, check */
                                /* * LPC17xx.h for UART register C structure overlay
                                */
    if (n_uart == 0 ) {
        /*
        Step 1: system control configuration

        step 1a: power control configuration, table 46 pg63
        enable UART0 power, this is the default setting
        also already done in system_LPC17xx.c
        enclose the code below for reference
        LPC_SC->PCONP |= BIT(3);

        step 1b: select the clock source, default PCLK=CCLK/4 , where CCLK =
                  100MHZ.
        tables 40 and 42 on pg56 and pg57
    }
}

```

```

Check the PLL0 configuration to see how XTAL=12.0MHZ gets to CCLK=100
    MHZ
in system_LPC17xx.c file
enclose code below for reference
LPC_SC->PCLKSEL0 &= ~(BIT(7)|BIT(6)); // PCLK = CCLK/4, default
    setting after reset

Step 2: Pin Ctrl Block configuration for TXD and RXD
Listed as item #5 in LPC_17xxum UART0/2/3 manual pag298
*/
LPC_PINCON->PINSEL0 |= (1 << 4); /* Pin P0.2 used as TXD0 (Com0) */
LPC_PINCON->PINSEL0 |= (1 << 6); /* Pin P0.3 used as RXD0 (Com0) */

pUart = (LPC_UART_TypeDef *) LPC_UART0;

} else if (n_uart == 1) {
    LPC_PINCON->PINSEL4 |= (2 << 0); /* Pin P2.0 used as TXD1 (Com1) */
    LPC_PINCON->PINSEL4 |= (2 << 2); /* Pin P2.1 used as RXD1 (Com1) */

    pUart = (LPC_UART_TypeDef *) LPC_UART1;

} else {
    return -1; /* not supported yet */
}

/* Step 3: Transmission Configuration */

/* step 3a: DLAB=1, 8N1 */
pUart->LCR = UART_8N1;

/* step 3b: 115200 baud rate @ 25.0 MHZ PCLK */
pUart->DLM = 0;
pUart->DLL = 9;
pUart->FDR = 0x21; /* FR = 1.507 ~ 1/2, DivAddVal = 1, MulVal = 2 */
                    /* FR = 1.507 = 25MHZ/(16*9*115200) */
pUart->LCR &= ~(BIT(7)); /* disable the Divisor Latch Access Bit DLAB=0
    */

    return 0;
}

/**
 * @brief: read a char from the n_uart, blocking read
 */

int uart_get_char(int n_uart)
{
    LPC_UART_TypeDef *pUart;

    if (n_uart == 0) {
        pUart = (LPC_UART_TypeDef *) LPC_UART0;
    } else if (n_uart == 1) {
        pUart = (LPC_UART_TypeDef *) LPC_UART1;
}

```

```

    } else {
        return -1; /* UART2,3 not supported yet */
    }

    /* polling the LSR RDR (Receiver Data Ready) bit to wait it is not empty
     */
    while (!(pUart->LSR & LSR_RDR));
    return (pUart->RBR);
}

/***
 * @brief: write a char c to the n_uart
 */
int uart_put_char(int n_uart, unsigned char c)
{
    LPC_UART_TypeDef *pUart;

    if (n_uart == 0) {
        pUart = (LPC_UART_TypeDef *)LPC_UART0;
    } else if (n_uart == 1) {
        pUart = (LPC_UART_TypeDef *)LPC_UART1;
    } else {
        return -1; // UART2,3 not supported
    }

    /* polling LSR THRE bit to wait it is empty */
    while (!(pUart->LSR & LSR_THRE));
    return (pUart->THR = c); /* write c to the THR */
}

/***
 * @brief write a string to UART
 */
int uart_put_string(int n_uart, unsigned char *s)
{
    if (n_uart >1 ) return -1; /* only uart0, 1 are supported for now */
    while (*s !=0) { /* loop through each char in the string */
        uart_put_char(n_uart, *s++);/* print the char, then ptr increments */
    }
    return 0;
}

/***
 * @brief call back function for printf
 * NOTE: first parameter p is not used for now. UART1 used.
 */
void putc(void *p, char c)
{
    if ( p != NULL ) {
        uart1_put_string("putc: first parameter needs to be NULL");
    } else {
        uart1_put_char(c);
    }
}

```

```
}
```

Listing 9.13: UART0 IRQ Sample Code `uart_polling.c`

9.7 Timer Programming

To program a TIMER on MCB1700 board, one first needs to configure the TIMER by following the steps listed in Section 21.1 in [4]. Listings 9.14 and 9.15 give one sample implementation of programming TIMER0 interrupts. The timer interrupt fires every one millisecond.

```
/**  
 * @brief timer.h - Timer header file  
 * @author Y. Huang  
 * @date 2013/02/12  
 */  
#ifndef _TIMER_H_  
#define _TIMER_H_  
  
extern uint32_t timer_init ( uint8_t n_timer ); /* initialize timer  
n_timer */  
  
#endif /* ! _TIMER_H_ */
```

Listing 9.14: Timer0 IRQ Sample Code `timer.h`

```
/**  
 * @brief timer.c - Timer example code. Tiemr IRQ is invoked every 1ms  
 * @author T. Reidemeister  
 * @author Y. Huang  
 * @author NXP Semiconductors  
 * @date 2012/02/12  
 */  
  
#include <LPC17xx.h>  
#include "timer.h"  
  
#define BIT(X) (1<<X)  
  
volatile uint32_t g_timer_count = 0; // increment every 1 ms  
  
/**  
 * @brief: initialize timer. Only timer 0 is supported  
 */  
uint32_t timer_init(uint8_t n_timer)  
{  
    LPC_TIM_TypeDef *pTimer;  
    if (n_timer == 0) {  
        /*  
        Steps 1 & 2: system control configuration.  
    }
```

```

Under CMSIS, system_LPC17xx.c does these two steps

-----
Step 1: Power control configuration.
        See table 46 pg63 in LPC17xx_UM
-----
Enable UART0 power, this is the default setting
done in system_LPC17xx.c under CMSIS.
Enclose the code for your reference
//LPC_SC->PCOMP |= BIT(1);

-----
Step2: Select the clock source,
        default PCLK=CCLK/4 , where CCLK = 100MHZ.
        See tables 40 & 42 on pg56-57 in LPC17xx_UM.
-----
Check the PLL0 configuration to see how XTAL=12.0MHZ
gets to CCLK=100MHZ in system_LPC17xx.c file.
PCLK = CCLK/4, default setting in system_LPC17xx.c.
Enclose the code for your reference
//LPC_SC->PCLKSEL0 &= ~(BIT(3)|BIT(2));

-----
Step 3: Pin Ctrl Block configuration.
        Optional, not used in this example
        See Table 82 on pg110 in LPC17xx_UM
-----
*/
pTimer = (LPC_TIM_TypeDef *) LPC_TIM0;

} else /* other timer not supported yet */
    return 1;
}

/*
-----
Step 4: Interrupts configuration
-----
*/
/* Step 4.1: Prescale Register PR setting
   CCLK = 100 MHZ, PCLK = CCLK/4 = 25 MHZ
   2*(12499 + 1)*(1/25) * 10^(-6) s = 10^(-3) s = 1 ms
   TC (Timer Counter) toggles b/w 0 and 1 every 12500 PCLKs
   see MR setting below
*/
pTimer->PR = 12499;

/* Step 4.2: MR setting, see section 21.6.7 on pg496 of LPC17xx_UM. */
pTimer->MR0 = 1;

/* Step 4.3: MCR setting, see table 429 on pg496 of LPC17xx_UM.
   Interrupt on MR0: when MR0 matches the value in the TC,
   generate an interrupt.

```

```

    Reset on MR0: Reset TC if MR0 matches it.
 */
pTimer->MCR = BIT(0) | BIT(1);

g_timer_count = 0;

/* Step 4.4: CMSIS enable timer0 IRQ */
NVIC_EnableIRQ(TIMER0_IRQn);

/* Step 4.5: Enable the TCR. See table 427 on pg494 of LPC17xx_UM. */
pTimer->TCR = 1;

return 0;
}

/***
 * @brief: use CMSIS ISR for TIMER0 IRQ Handler
 * NOTE: This example shows how to save/restore all registers rather than
 * just
 *      those backed up by the exception stack frame. We add extra
 *      push and pop instructions in the assembly routine.
 *      The actual c_TIMER0_IRQHandler does the rest of irq handling
 */
__asm void TIMER0_IRQHandler(void)
{
    PRESERVE8
    IMPORT c_TIMER0_IRQHandler
    PUSH{r4-r11, lr}
    BL c_TIMER0_IRQHandler
    POP{r4-r11, pc}
}

/***
 * @brief: c TIMER0 IRQ Handler
 */
void c_TIMER0_IRQHandler(void)
{
    /* ack interrupt, see section 21.6.1 on pg 493 of LPC17XX_UM */
    LPC_TIM0->IR = BIT(0);

    g_timer_count++ ;
}

```

Listing 9.15: Timer0 IRQ Sample Code timer.c

Appendix A

Forms

Lab administration related forms are given in this appendix.

ECE 350 Request to Leave a Project Group Form

| | |
|------------------------------|--|
| Name | |
| Quest ID | |
| Student ID | |
| Lab Project ID | |
| Group ID | |
| Name of Other Group Member 1 | |
| Name of Other Group Member 2 | |
| Name of Other Group Member 3 | |

Provide the reason for leaving the project group here:

Signature _____

Date _____

Appendix B

The RAM.ini File

The RAM.ini file in the starter code can be found in Listing B.1. It relocates the vector table to RAM and load the code for in-memory execution (i.e. not to the ROM). This will avoid wear-and-tear on the on-chip flash memory.

```
FUNC void Setup (void) {
    // Setup Stack Pointer
    SP = _RDWORD(0x10000000);
    // Setup Program Counter
    PC = _RDWORD(0x10000004);
    // Set Thumb bit
    XPSR = 0x01000000;
    // Setup Vector Table Offset Register
    _WDWORD(0xE000ED08, 0x10000000);
    // Enable ADC Power
    _WDWORD(0x400FC0C4, _RDWORD(0x400FC0C4) | 1<<12);
    // Setup ADC Trim
    _WDWORD(0x40034034, 0x00000F00);
}
// Download
LOAD %L INCREMENTAL

// Setup for Running
Setup();
g, main
```

Listing B.1: The RAM.ini file

Bibliography

- [1] MCB1700 User's Guide. <http://www.keil.com/support/man/docs/mcb1700>.
- [2] MDK Primer. <http://www.keil.com/support/man/docs/gsac>.
- [3] Realview compilation tools version 4.0: Compiler reference guide, 2007-2010.
- [4] LPC17xx User Manual, Rev2.0, 2010.
- [5] J. Yiu. *The Definitive Guide to the ARM Cortex-M3*. Newnes, 2009.