

PLD Logic Components

The components in the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

Adders

The components in the **Adders Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

ADD_FULL

This device is a full adder with the result on 1 bit.

A full adder is a digital circuit that adds two input bits and an input carry and produces a sum and an output carry.

Logic functions:

$$\text{SUM} = \overline{\text{ABCIN}} + \overline{\text{ABCIN}} + \overline{\text{ABCIN}} + \text{ABCIN}$$

$$\text{CARRY} = \text{AB} + (\overline{\text{A}} + \overline{\text{B}})\text{CIN}$$

The output SUM can be generated by two 2-input exclusive-OR gates. The first must generate the term $(\overline{\text{AB}} + \overline{\text{AB}})$, and the second has as its inputs the output of the first XOR gate and the input carry (CIN). The output CARRY is a 1 when both inputs to the first XOR gate are 1s or when both inputs to the second XOR gate are 1s.

Function table:

Input A	Input B	Input CIN	Output CARRY	Output SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

This topic refers to education-specific features of Multisim.

ADD_FULL4_FCR

This device is a 4-bit full adder with fast carry.

This high-speed 4-bit binary full adder with internal carry look-ahead accepts two 4-bit binary words (A1-A4, B1-B4) and a Carry input (C0). It generates the binary Sum outputs (SUM_1- SUM_4) and the Carry output (C4) from the most significant bit. It operates with either active HIGH or active LOW operands (positive or negative logic).

Function table:

	C0	A1	A2	A3	A4	B1	B2	B3	B4	SUM_1	SUM_2	SUM_3	SUM_4	C4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active High	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active Low	1	1	0	1	0	0	1	1	0	0	0	1	1	0

H = HIGH voltage level

L = LOW voltage Level

This topic refers to education-specific features of Multisim.

ADD_HALF

This device is a half adder with the result on 1 bit.

A half adder is a digital circuit that adds two bits and produces a sum and an output carry. It cannot handle input carries.

Logic functions:

$$\text{CARRY} = AB$$

$$\text{SUM} = \bar{A}\bar{B} + A\bar{B}$$

The output CARRY is produced with an AND gate with A and B on the inputs, and the SUM output is generated with an exclusive-OR gate.

Function table:

Input A	Input B	Output CARRY	Output SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

This topic refers to education-specific features of Multisim.

Buffers

The components in the **Buffers Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

BUF

This device is a non-inverting buffer.

Logic function:

$$O = I$$

Truth table:

Input I	Output O
L	L
H	H

H = HIGH voltage level

L = LOW voltage Level

This topic refers to education-specific features of Multisim.

BUF_3S_AHOE

This device is a 3-state buffer with an active HIGH output enable.

The output Y follows the input data (A) when the output enable (C) is HIGH. When input C is LOW, the output Y is in a high impedance state.

Truth table:

Input A	Input C	Output Y
L	H	L
H	H	H
X	L	Z

H = HIGH voltage level
 L = LOW voltage Level
 X= Either HIGH or LOW voltage level
 Z= High impedance 'OFF' state

This topic refers to education-specific features of Multisim.

BUF_3S_ALOE

This device is a 3-state buffer with an active LOW output enable.

The output Y follows the input data (A) when the output enable (C) is LOW. When input C is HIGH, the output Y is in a high impedance state.

Truth table:

Input A	Input C	Output Y
L	L	L
H	L	H
X	H	Z

H = HIGH voltage level
 L = LOW voltage Level
 X= Either HIGH or LOW voltage level
 Z= High impedance 'OFF' state

This topic refers to education-specific features of Multisim.

BUF_CO

This device is a true/complement buffer which provides both an inverted active LOW output ($\sim O$) and a non-inverted active HIGH output (O) for each input (I).

Logic function:

$$\begin{aligned}\sim O &= \bar{I} \\ O &= I\end{aligned}$$

The output $\sim O$ is true when the input I is NOT true, and the output O is true when the input I is true.

Input I	Output O	Output $\sim O$
L	H	L
H	L	H

H = HIGH voltage level
 L = LOW voltage Level

This topic refers to education-specific features of Multisim.

BUF_INV

This device is an inverting buffer.

Logic function:

$$O = \bar{I}$$

The output O is true when the input I is NOT true, the output is the inverse of the input: $O = \text{NOT } I$.

Input I	Output O
L	H
H	L

H = HIGH voltage level
 L = LOW voltage Level

This topic refers to education-specific features of Multisim.

Comparators

The components in the **Comparators Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

COMP_4

This device is a 4-bit magnitude comparator.

The basic function of a comparator is to compare the magnitudes of two binary quantities to determine the relationship of those quantities.

This is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A0-A3) and (B0-B3) where A3 and B3 are the most significant bits. The operation of the comparator is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme. The expansion inputs AGTB(A>B), and AEQB(A=B) and ALTB(A<B) are the least significant bit positions. When used for series expansion, the OAGTB, OAEQB and OALTB outputs of the least significant word are connected to the corresponding AGTB, AEQB and ALTB inputs of the next higher stage. Stages can be added in this manner to any length.

For proper operation, the expansion inputs of the least significant word should be tied as follows: AGTB= LOW, AEQB = HIGH , and ALTB = LOW.

Function table:

COMPARING INPUTS				EXPANSION INPUTS			OUTPUTS		
A3,B3	A2,B2	A1,B1	A0,B0	AGTB	AEQB	ALTB	OAGTB	OAEQB	OALTB
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L

H = HIGH voltage level

L = LOW voltage Level

X= Either HIGH or LOW voltage level

This topic refers to education-specific features of Multisim.

Counters

The components in the **Counters Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

CNTR_4BIN_AS

This device is a 4 Bit Ripple Type Counter partitioned into two sections: a divide-by-two section and a divide-by-eight section which is triggered by a HIGH-to-LOW transition on the clock input. Each section can be used separately or tied together (QA to INB) to form a Modulo-16 counter. A gated AND asynchronous Master Reset (R01·R02) is provided which clears all the flip-flops.

The device may be operated in various counting modes:

- 4-Bit Ripple Counter - The output QA must be externally connected to input INB. The input count pulses are applied to input INA . Simultaneous divisions of 2, 4, 8 and 16 are performed at the QA, QB, QC and QD outputs as shown in the truth table.
- 3-Bit Ripple Counter - The input count pulses are applied to input INB. Simultaneous frequency divisions of 2, 4 and 8 are available at the QB, QC and QD outputs.

Mode selection table:

RESET INPUTS		OUTPUTS			
R01	R02	QA	QB	QD	
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Level.

L = LOW Level.

Truth table:

COUNT	OUTPUT			
	QA	QB	QC	QD
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH Level.

L = LOW Level.

Note: QA is connected to input INB.

This topic refers to education-specific features of Multisim.

CNTR_4BIN_ASCLR

This device is a 4 Bit positive-edge-triggered Synchronous Counter. It has an Asynchronous Reset (Clear) input that overrides all other control inputs and independent of the clock input. Three control inputs - LOAD, ENP and ENT - select the mode of operation as shown in the Mode selection table below. The Count Mode is enabled when the ENP, ENT and LOAD inputs are HIGH. When LOAD is LOW, the counter will synchronously load the data from the parallel inputs into the flip-flops on the LOW-to-HIGH transition of the clock. Either the ENP or ENT can be used to inhibit the count sequence.

This device is a Modulo 16 counter. The Ripple Carry Output (RCO) is HIGH when ENT input is HIGH while the counter is in its maximum count state (HHHH). It will be HIGH only for one count state.

The Master Reset (CLR) is asynchronous. When CLR is LOW it sets all the outputs LOW.

Mode selection table:

CLR	LOAD	ENT	ENP	CLK	OPERATION
L	X	X	X	X	RESET
H	L	X	X	↑	LOAD
H	H	H	H	↑	COUNT
H	H	L	X	X	HOLD
H	H	X	L	X	HOLD

H = HIGH Level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH transition of the Clock pulse.

This topic refers to education-specific features of Multisim.

CNTR_4BIN_S

This device is a 4 Bit positive-edge-triggered Synchronous Counter. It has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the LOW-to-HIGH transition of the clock. Three control inputs - LOAD, ENP and ENT - select the mode of operation as shown in the Mode selection table below. The Count Mode is enabled when the ENP, ENT and LOAD inputs are HIGH. When LOAD is LOW, the counter will synchronously load the data from the parallel inputs into the flip-flops on the LOW-to-HIGH transition of the clock. Either the ENP or ENT can be used to inhibit the count sequence.

CNTR_4BIN_S is a Modulo 16 counter. The Ripple Carry Output (RCO) is HIGH when ENT input is HIGH while the counter is in its maximum count state (HHHH). It will be HIGH only for one count state.

The active LOW synchronous Reset (CLR) input of the counter acts as an edge-triggered control input, overriding ENP, ENT and LOAD, and resetting the four counter flip-flops on the LOW-to-HIGH transition of the clock.

Mode selection table:

CLR	LOAD	ENT	ENP	Action on the Rising Clock Edge (↑)
L	X	X	X	RESET
H	L	X	X	LOAD
H	H	H	H	COUNT
H	H	L	X	HOLD
H	H	X	L	HOLD

H = HIGH Level.

L = LOW Level.

X = Don't Care.

This topic refers to education-specific features of Multisim.

CNTR_4BINS_DC

This device is a Synchronous UP/DOWN Modulo 16 Binary Counter featuring separate Count Up and Count Down Clocks. Separate Carry Output and Borrow Output are provided which are used as the clocks for subsequent stages without extra logic.

A LOW-to-HIGH transition on the UP Clock input advances the count by one; a similar transition on the DOWN Clock input decreases the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit either counts by twos or not at all.

The Carry Output and the Borrow Output are normally HIGH. When the counter has reached the maximum count state (HHHH) the next HIGH-to-LOW transition of the UP Clock will cause CO to go LOW. CO will stay LOW until UP Clock goes HIGH again. Similarly, the BO output will go LOW when the circuit is in the zero state (LLLL) and the DOWN Clock goes LOW.

The counter has an asynchronous parallel load capability permitting the counter to be preset. When the LOAD and the Master Reset (CLR) are LOW, information present on the Parallel Data inputs (A,B,C,D) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the CLR input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state.

Mode selection table:

CLR	LOAD	UP	DOWN	MODE
H	X	X	X	RESET
L	L	X	X	LOAD
L	H	H	H	HOLD
L	H	↑	H	COUNT UP
L	H	H	↑	COUNT DOWN

H = HIGH Level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH transition of the Clock input.

This topic refers to education-specific features of Multisim.

CNTR_4BIN_SU_D

This device is a Synchronous UP/DOWN Modulo 16 Binary Counter. A LOW-to-HIGH transition on the clock input advances the count by one.

The counter has an asynchronous parallel load capability permitting the counter to be preset. When the LOAD is LOW, information present on the Parallel Data inputs (A,B,C,D) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the CTEN input inhibits counting. When CTEN is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition on the clock input. The direction of counting is determined by the U/D input signal as indicated in the Mode selection table below.

Two types of outputs are provided as overflow/underflow indicators. The MAX/MIN output is normally LOW and goes HIGH when the counter reaches zero (LLLL) in the count-down mode or reaches maximum (HHHH) in the count-up mode. The RCO output is normally HIGH but when CTEN is LOW and MAX/MIN is HIGH it will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again.

Mode selection table:

PL	CTEN	U/D	CLK	MODE
H	L	L	↑	COUNT UP
H	L	H	↑	COUNT DOWN
L	X	X	X	LOAD
H	H	X	X	HOLD

H = HIGH Level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH transition of the Clock input.

RCO Truth table:

CTEN	MAX/MIN	CLK	MODE
L	H	L	L
H	X	X	H
X	L	X	H

H = HIGH Level.

L = LOW Level.

X = Don't Care.

This topic refers to education-specific features of Multisim.

CNTR_7BIN

This device is a 7 Stage Binary Counter. The counter is reset to its logical 0 (LLLLLL) stage by a HIGH signal on the Master Reset (MR) input. The counter is advanced one count on the negative transition of each clock pulse.

Counter function table:

MR	CP	OPERATION
H	X	RESET
L	↓	COUNT
L	L	HOLD

H = HIGH Level.

L = LOW Level.

X = Don't Care.

↓ = HIGH-to-LOW transition of the Clock input.

This topic refers to education-specific features of Multisim.

CNTR_BCD_S

This device is a (BCD) Decade positive-edge-triggered Synchronous Counter. It has a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the LOW-to-HIGH transition of the clock. Three control inputs - LOAD, ENP and ENT - select the mode of operation as shown in the Mode selection table below. The Count Mode is enabled when the ENP, ENT and LOAD inputs are HIGH. When LOAD is LOW, the counter will synchronously load the data from the parallel inputs into the flip-flops on the LOW-to-HIGH transition of the clock. Either the ENP or ENT can be used to inhibit the count sequence.

CNTR_BCD_S is a Decade counter. The Ripple Carry Output (RCO) is HIGH when ENT input is HIGH while the counter is in its maximum count state (HLLH). It will be HIGH only for one count state.

The active LOW synchronous Reset (CLR) input of the counter acts as an edge-triggered control input, overriding ENP, ENT and LOAD, and resetting the four counter flip-flops on the LOW-to-HIGH transition of the clock.

Mode selection table:

CLR	LOAD	ENT	ENP	Action on the Rising Clock Edge (↑)
L	X	X	X	RESET
H	L	X	X	LOAD
H	H	H	H	COUNT
H	H	L	X	HOLD
H	H	X	L	HOLD

H = HIGH Level.

L = LOW Level.

X = Don't Care.

This topic refers to education-specific features of Multisim.

CNTR_BCD_SDC

This device is an Synchronous UP/DOWN (BCD) Decade Counter featuring separate Count Up and Count Down Clocks. Separate Carry Output and Borrow Output are provided which are used as the clocks for subsequent stages without extra logic.

A LOW-to-HIGH transition on the UP Clock input will advance the count by one; a similar transition on the DOWN Clock input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all.

The Carry Output and the Borrow Output are normally HIGH. When the counter has reached the maximum count state (HLLH) the next HIGH-to-LOW transition of the UP Clock will cause CO to go LOW. CO will stay LOW until UP Clock goes HIGH again. Similarly, the BO output will go LOW when the circuit is in the zero state (LLLL) and the DOWN Clock goes LOW.

The counter has an asynchronous parallel load capability permitting the counter to be preset. When the LOAD and the Master Reset (CLR) are LOW, information present on the Parallel Data inputs (A,B,C,D) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the CLR input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state.

Mode selection table:

CLR	LOAD	UP	DOWN	MODE
H	X	X	X	RESET
L	L	X	X	LOAD
L	H	H	H	HOLD
L	H	↑	H	COUNT UP
L	H	H	↑	COUNT DOWN

H = HIGH Level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH transition of the Clock input.

This topic refers to education-specific features of Multisim.

CNTR_BCD_SU_D

This device is an Synchronous UP/DOWN (BCD) Decade Binary Counter. A LOW-to-HIGH transition on the clock input will advance the count by one.

The counter has an asynchronous parallel load capability permitting the counter to be preset. When the **LOAD** is LOW, information present on the Parallel Data inputs (**A,B,C,D**) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the **CTEN** input inhibits counting. When **CTEN** is LOW, internal state change are initiated synchronously by the LOW-to-HIGH transition on the clock input. The direction of counting is determined by the **U/D** input signal as indicated in the Mode selection table below.

Two types of outputs are provided as overflow/underflow indicators. The MAX/MIN output is normally LOW and goes HIGH when the counter reaches zero (LLLL) in the count-down mode or reaches maximum (HLLH) in the count-up mode. The **RCO** output is normally HIGH but when **CTEN** is LOW and MAX/MIN is HIGH it will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again.

Mode selection table:

PL	CTEN	U/D	CLK	MODE
H	L	L	↑	COUNT UP
H	L	H	↑	COUNT DOWN
L	X	X	X	LOAD
H	H	X	X	HOLD

H = HIGH Level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH transition of the Clock input.

RCO Truth table:

CTEN	MAX/MIN	CLK	MODE
L	H	L	L
H	X	X	H
X	L	X	H

H = HIGH Level.

L = LOW Level.

X = Don't Care.

This topic refers to education-specific features of Multisim.

CNTR_BIN_DEC_SU_D

This device is a pre-settable UP/DOWN Counter which counts in either binary or decade mode depending on the signal present at the **BIN/DEC** input. When **BIN/DEC** is HIGH the counter counts in binary, otherwise it counts in decade. The counter counts up when the **UP/DN** input HIGH, otherwise it counts down. A HIGH signal present at Preset Enable input (PE) allows information on the data inputs (P0 to P3) to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the LOW-to-HIGH clock (CP) transition when the **Cl** and PE inputs are LOW.

The Carry Output (TC) is normally HIGH and goes LOW when the counter reaches its maximum count in the UP mode or the minimum count in the DOWN mode provided that CI input is LOW.

Counter Functional table:

CONTROL INPUT	LOGIC LEVEL	ACTION
BIN/ DEC	H	BINARY COUNT
	L	DECade COUNT
UP/ DN	H	UP COUNT
	L	DOWN COUNT
PE	H	PARALLEL LOAD
	L	NO LOAD
<u>CI</u>	H	NO ADVANCE AT ↑
	L	ADVANCE AT ↑

H = HIGH Level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH Clock transition.

This topic refers to education-specific features of Multisim.

CNTR_JOHNSON

This device is a 5 Stage Johnson Decade Counter with 10 decoded active HIGH outputs (Q0 to Q9), an active LOW output from the most significant flip-flop (O5-9), active HIGH and active LOW clock inputs (CP0, CP1) and overriding asynchronous Master Reset (MR) input. The counter is advanced by either a LOW-to-HIGH transition at CP0 while CP1 is LOW or a HIGH-to-LOW transition at CP1 while CP0 is HIGH. A HIGH on MR resets the counter to zero (Q0= O5-9 =HIGH; Q1 to Q9=LOW) independent of the clock inputs CP0, CP1.

Counter function table:

MR	CP0	CP1	OPERATION
H	X	X	RESET
L	H	↓	COUNTER ADVANCES
L	↑	L	COUNTER ADVANCES
L	L	X	NO CHANGE
L	X	H	NO CHANGE
L	H	↑	NO CHANGE
L	↓	L	NO CHANGE

H = HIGH Level.

L = LOW Level.

X = Don't Care.

↓ = HIGH-to-LOW transition of the Clock input.

↑ = LOW-to-HIGH transition of the Clock input.

This topic refers to education-specific features of Multisim.

Decoders

The components in the **Decoders Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

DEC2_4

This device is a 2 to 4 Line Decoder. It decodes one of the four lines based upon the conditions at the two binary select inputs (A, B) and enable input (G).

Decoder function table:

INPUTS		OUTPUTS							
ENABLE G	SELECT B A	Y0		Y1		Y2		Y3	
		H	X	H	H	H	H	H	L
H	X	X	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H
L	H	L	H	H	L	H	H	H	H
L	H	H	H	H	H	H	H	L	H

H – HIGH level

L = LOW Level

X = Don't Care

This topic refers to education-specific features of Multisim.

DEC3_8

This device is a 3 to 8 Line Decoder. It decodes one of the eight lines based upon the conditions at the three binary select inputs and the three enable inputs. There are two active-LOW and one active-HIGH enable inputs.

Decoder function table:

ENABLE			SELECT			OUTPUTS							
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH level

L = LOW Level

X = Don't Care

This topic refers to education-specific features of Multisim.

DEC4_10

This device is a BCD-to-decimal decoder.

A decoder is a digital circuit that detects the presence of a specified combination of bits (code) on its inputs and indicates the presence of that code by a specified output level.

This decoder consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

Function table:

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage level

L = LOW voltage level

This topic refers to education-specific features of Multisim.

DEC_BCD_7

This device is a BCD to 7-Segment Decoder/Driver. It decodes the input data (A, B, C, D) indicated in the Truth Table below. A LOW signal applied to BI/RBO turns off all segment outputs. A LOW signal applied to LT turns on all segment outputs.

Decoder truth table:

DEC NO.	INPUTS							OUTPUTS						
	LT	RBI	D	C	B	A	BI/RBO	OA	OB	OC	OD	OE	OF	OG
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L

H = HIGH level

L = LOW Level

X = Don't Care

DEC_BCD_10_INV

This device is a BCD-to-decimal decoder with inverted outputs.

A decoder is a digital circuit that detects the presence of a specified combination of bits (code) on its inputs and indicates the presence

of that code by a specified output level.

This decoder consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

Function table:

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	H	L	L	L	L	L	L	L	L	L
1	L	L	L	H	L	H	L	L	L	L	L	L	L	L
2	L	L	H	L	L	L	H	L	L	L	L	L	L	L
3	L	L	H	H	L	L	L	H	L	L	L	L	L	L
4	L	H	L	L	L	L	L	L	H	L	L	L	L	L
5	L	H	L	H	L	L	L	L	L	H	L	L	L	L
6	L	H	H	L	L	L	L	L	L	L	H	L	L	L
7	L	H	H	H	L	L	L	L	L	L	L	H	L	L
8	H	L	L	L	L	L	L	L	L	L	L	L	H	L
9	H	L	L	H	L	L	L	L	L	L	L	L	L	H
Extraordinary States	H	L	H	L	L	L	L	L	L	L	L	L	H	L
	H	L	H	H	L	L	L	L	L	L	L	L	L	H
	H	H	L	L	L	L	L	L	L	L	L	L	H	L
	H	H	L	H	L	L	L	L	L	L	L	L	L	H
	H	H	H	L	L	L	L	L	L	L	L	L	H	L
	H	H	H	H	L	L	L	L	L	L	L	L	L	H

Function Table

H = HIGH voltage level

L = LOW voltage level

This topic refers to education-specific features of Multisim.

Demultiplexers

The components in the **Demultiplexers Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

DEM4_16

This device is a 4-to-16 line decoder/demultiplexer. It accepts four active-HIGH binary address inputs and provide 16 active-LOW outputs. It feature an enable gate that is an AND gate which must be LOW to enable the outputs.

Demultiplexer function table:

		INPUTS				OUTPUT LOW
G1	G2	A	B	C	D	
H	H	X	X	X	X	None
H	L	X	X	X	X	None
L	H	X	X	X	X	None
L	L	L	L	L	L	$\overline{O_0}$
L	L	L	L	L	H	$\overline{O_1}$
L	L	L	L	H	L	$\overline{O_2}$
L	L	L	L	H	H	$\overline{O_3}$
L	L	L	H	L	L	$\overline{O_4}$
L	L	L	H	L	H	$\overline{O_5}$
L	L	L	H	H	L	$\overline{O_6}$
L	L	L	H	H	H	$\overline{O_7}$
L	L	H	L	L	L	$\overline{O_8}$
L	L	H	L	L	H	$\overline{O_9}$
L	L	H	L	H	L	$\overline{O_{10}}$
L	L	H	L	H	H	$\overline{O_{11}}$
L	L	H	H	L	L	$\overline{O_{12}}$
L	L	H	H	L	H	$\overline{O_{13}}$
L	L	H	H	H	L	$\overline{O_{14}}$
L	L	H	H	H	H	$\overline{O_{15}}$

H = HIGH Level.

L = LOW Level.

X = Don't Care.

This topic refers to education-specific features of Multisim.

Encoders

The components in the **Encoders Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

ENC8_3

This device is a 8-line-to-3 -line priority encoder.

A priority encoder offers additional flexibility in that it can be used in applications that require priority detection. The priority function means that the encoder produces a 3 bit output corresponding to the highest-order octal digit input that is active and ignores any other lower-order active inputs.

This is a priority encoder that has eight active-LOW inputs and three active-LOW binary outputs. This device can be used for converting octal inputs (recall that the octal digits are 0 through 7) to a 3-bit binary code. To enable the device, the EI (enable input) must be LOW. It also has the EO (enable output) and GS output for expansion purposes. The EO is LOW when the EI is LOW and none of the inputs (0 through 7) is active. GS is LOW when EI is LOW and any of the inputs is active.

This device encodes eight data lines to three-line (4-2-1) binary (octal). By providing cascading circuitry (Enable Input EI and Enable Output EO) octal expansion is allowed without needing external circuitry.

Function table:

INPUTS								OUTPUTS					
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	L	L	H

H = HIGH voltage level

L = LOW voltage level

X= Either HIGH or LOW voltage level

This topic refers to education-specific features of Multisim.

ENC10_4

This device is a decimal -to- BCD encoder. This type of encoder has ten inputs, one for each decimal digit, and four outputs corresponding to the BCD code. This is a 10-line-to-4-1line encoder.

A priority encoder offers additional flexibility in that it can be used in applications that require priority detection. The priority function means that the encoder will produce a BCD output corresponding to the highest-order decimal digit input that is active and will ignore any other lower-order active inputs. For instance, if the 6 and the 3 inputs are both active, the BCD output is 0110 (which represents decimal 6).

This is a priority encoder with active-LOW inputs (0) for decimal digits 1 through 9 and active-LOW BCD outputs. A BCD zero output is represented when none of the inputs is active.

This device encodes nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition does not require an input condition because zero is encoded when all nine data lines are at a high logic level.

Function table:

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level

L = LOW voltage level

X= Either HIGH or LOW voltage level

This topic refers to education-specific features of Multisim.

Flip-Flops

The components in the **Flip-Flops Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

FF_D_CO

This device is a positive-edge-triggered flip-flop with complementary outputs. The information on the D input is transferred to the outputs on the rising edge of the clock pulse.

D Flip-Flop function table:

INPUTS		OUTPUTS	
CLK	D	Q	\overline{Q}
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q_0}$

H = HIGH Level.

L = LOW Level.

X = Don't Care.

Q_0 = The level of Q before the indicated input conditions were established.

↑ = LOW-to-HIGH Clock transition.

This topic refers to education-specific features of Multisim.

FF_D4_CLR_CO

This device is a 4 bit positive-edge-triggered D Flip-Flop with clear and complementary outputs. When Clear is inactive (HIGH), the information on the D inputs is transferred to the outputs on the rising edge of the clock pulse. A low level at the clear input resets the outputs.

D flip-flop function table:

INPUTS			OUTPUTS	
CLR	CLK	D_n	Q_n	$\overline{Q_n}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_{n0}	$\overline{Q_{n0}}$

H = HIGH Level.

L = LOW Level.

X = Don't Care.

Q_{n0} = The level of Q_n before the indicated input conditions were established.

↑ = LOW-to-HIGH Clock transition.

This topic refers to education-specific features of Multisim.

FF_JK_NSCLR_CO

This device is a negative-edge-triggered flip-flop with preset, clear and complementary outputs. The J and K inputs must be stable prior to the high-to-low clock transition for predictable operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as mentioned in the function table.

JK flip-flop function table:

INPUTS					OUTPUTS	
\overline{PR}	\overline{CLR}	CLK	J	K	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^+	H^+
H	H	\downarrow	L	L	Q_0	$\overline{Q_0}$
H	H	\downarrow	H	L	H	L
H	H	\downarrow	L	H	L	H
H	H	\downarrow	H	H	TOGGLE	

H = HIGH Level.

L = LOW Level.

X = Don't Care.

Q_0 = The level of Q before the indicated input conditions were established.

\downarrow = HIGH-to-LOW Clock transition.

H^+ = This configuration is non-stable; that is, it will not persist when either the reset and/or clear inputs return to their inactive (HIGH) level.

This topic refers to education-specific features of Multisim.

FF_JK_PSCLR_CO

This device is a positive-edge-triggered flip-flop with preset, clear and complementary outputs. The J and K inputs must be stable prior to the LOW-to-HIGH clock transition for predictable operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as mentioned in the function table.

JK flip-flop function table:

INPUTS					OUTPUTS	
\overline{PR}	\overline{CLR}	CLK	J	K	Q	\overline{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H^+	H^+
H	H	\uparrow	L	L	Q_0	$\overline{Q_0}$
H	H	\uparrow	H	L	H	L
H	H	\uparrow	L	H	L	H
H	H	\uparrow	H	H	TOGGLE	

H = HIGH Level.

L = LOW Level.

X = Don't Care.

Q_0 = The level of Q before the indicated input conditions were established.

\uparrow = LOW-to-HIGH Clock transition.

H^+ = This configuration is non-stable; that is, it will not persist when either the reset and/or clear inputs return to their inactive (HIGH) level.

This topic refers to education-specific features of Multisim.

FF_D_PCLR_CO

This device is a positive-edge-triggered flip-flop with preset, clear and complementary outputs. When preset and clear are inactive (HIGH), the information on the D input is transferred to the outputs on the rising edge of the clock pulse. A low level at the preset or clear inputs sets or resets the outputs.

D flip-flop function table:

INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H^+	H^+
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

H = HIGH Level.

L = LOW Level.

X = Don't Care.

Q_0 = The level of Q before the indicated input conditions were established.

↑ = LOW-to-HIGH Clock transition.

H^+ = This configuration is non-stable; that is, it will not persist when either the reset and/or clear inputs return to their inactive (HIGH) level.

This topic refers to education-specific features of Multisim.

FF_T_CLR_CO

This device is a T flip-flop featuring an asynchronous Clear input and complementary outputs. When CLR input is LOW the Q output is set to LOW. If CLR input is held HIGH for every rising clock edge, and when T input is HIGH, the outputs of the latch toggle.

T Flip-Flop function table:

INPUTS			OUTPUTS	
T	\overline{CLR}	CLK	Q	\overline{Q}
X	L	X	L	H
L	H	↑	Q_0	$\overline{Q_0}$
H	H	↑	TOGGLE	
X	H	L	Q_0	$\overline{Q_0}$

H = HIGH level.

L = LOW Level.

X = Don't Care.

Q_0 = The level of Q before the LOW-to-HIGH transition of Enable.

This topic refers to education-specific features of Multisim.

Generators

The components in the **Generators Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

LA_CARRY_GEN

This device is a look-ahead carry generator which accepts up to four pairs of active-low Carry Propagate ($\overline{P_0} \ \overline{P_1} \ \overline{P_2} \ \overline{P_3}$) and Carry Generate ($G_0 \ G_1 \ G_2 \ G_3$) signals and an active-high Carry input (CN) and provides anticipated active-HIGH carries ($CN+X, CN+Y, CN+Z$). LA_CARRY_GEN also has active-LOW Carry Propagate (P) and Carry Generate (G) outputs which may be used for further levels of look-ahead.

Generator function table:

INPUTS									OUTPUTS				
CN	G0	P0	G1	P1	G2	P2	G3	P3	CN+ X	CN+ Y	CN+ Z	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H					L			
X	X	X	H	H	H	X				L			
X	H	H	H	X	H	X				L			
L	H	X	H	X	H	X				L			
X	X	X	X	L	X					H			
X	X	X	L	X	X	L				H			
X	L	X	X	L	X	L				H			
H	X	L	X	L	X	L				H			
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	L	X	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
	H		X		X		X	X				H	
	X		H		X		X	X				H	
	X		X		H		X	X				H	
	X		X		X		H					H	
	L		L		L		L	L				L	

H = HIGH Level.

L = LOW Level.

X = Don't Care.

This topic refers to education-specific features of Multisim.

PG_9_0_E

This device is a 9 Bit parity generator/checker which feature odd/even outputs. The word length capability is easily expanded by cascading. When the number of inputs (A thru I) that are HIGH is even the EVEN output will be HIGH and the ODD output will be LOW. When the number of inputs that are HIGH is odd then the EVEN output will be LOW and the ODD output will be HIGH.

Generator function table:

Number of inputs (A thru I) that are HIGH	EVEN	ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Level.

L = LOW Level.

This topic refers to education-specific features of Multisim.

PG_13

This device is a parity checker/generator with 13 parity inputs (I0 thru I12) and a parity output (O). When the number of parity inputs that are HIGH is even, the output is LOW. When the number of parity inputs that are HIGH is odd, the output is HIGH. It can be cascaded by connecting the output of one PG_13 to any parity input of another PG_13.

Generator/Checker function table:

INPUTS														OUTPUT
I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	I ₈	I ₉	I ₁₀	I ₁₁	I ₁₂	O	
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
Any odd number of inputs HIGH														H
Any even number of inputs HIGH														L
H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Level.

L = LOW Level.

This topic refers to education-specific features of Multisim.

Latches

The components in the **Latches Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

LATCH_D

This device is a Gated D Latch with complementary outputs. When the D input is HIGH and the EN input is HIGH, the latch sets. When the D input is LOW and EN is HIGH, the latch resets. When EN is LOW there is no change at the outputs.

D Latch function table:

INPUTS		OUTPUTS	
D	EN	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

H = HIGH level

L = LOW Level

X = Don't Care

Q_0 = The level of Q before the indicated steady state input conditions were established.

This topic refers to education-specific features of Multisim.

LATCH_D2

This device is a 2 Bit Bi-stable Latch with complementary outputs. Information present at a Data (D) input is transferred to the Q output when the enable is HIGH, and the Q output will follow the data input as long as the enable remains HIGH. When the enable goes LOW, the information is retained at the Q output until the enable goes HIGH.

D Latch function table:

INPUTS		OUTPUTS	
D	Enable	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

H – HIGH level

L = LOW Level

X = Don't Care

Q_0 = The level of Q before the HIGH-to-LOW transition of Enable

This topic refers to education-specific features of Multisim.

LATCH_D4_SR_OE

This device is a 4 Bit Bi-stable Latch with Strobe, Reset and Output Enable. While the Strobe (ST) input is HIGH, the data on the D inputs appear at the corresponding Q outputs provided the Output Enable input is HIGH. Changing the ST input to LOW locks the data into the latch. If the Master Reset input (MR) is HIGH it forces the outputs to a LOW level regardless of the state of the ST input. The outputs are forced to the High-Impedance state by a LOW signal at the EO input.

Latch function table:

INPUTS			OUTPUTS	
MR	EO	ST	Dn	Qn
L	H	H	H	H
L	H	H	L	L
L	H	L	X	LATCHED
H	H	X	X	L
X	L	X	X	Z

H = HIGH level

L = LOW Level

X = Don't Care

Z = High Impedance

This topic refers to education-specific features of Multisim.

LATCH_SR

This device is a gated Set-Reset Latch. The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input. The latch will not change until EN is HIGH. An invalid state occurs when both S and R are simultaneously HIGH.

SR Latch function table:

INPUTS			OUTPUTS	
S	R	EN	Q	\bar{Q}
X	X	L	Q_0	\bar{Q}_0
L	L	H	Q_0	\bar{Q}_0
L	H	H	L	H
H	L	H	H	L
H	H	H	Restricted combination	

H = HIGH level

L = LOW Level

X = Don't Care

Q_0 = The level of Q before the indicated steady state input conditions were established.

This topic refers to education-specific features of Multisim.

Logic Gates

The components in the **Logic Gates Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

AND2

This device performs the logic function of a 2 input AND gate.

Logic function:

$$Y = AB$$

AND gate truth table:

Input A	Input B	Output Y
0	0	0
0	1	0
1	0	0
1	1	1

This topic refers to education-specific features of Multisim.

AND3

This device performs the logic function of a 3 input AND gate.

Logic function:

$$Y = ABC$$

AND gate truth table:

Input A	Input B	Input C	Output Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

This topic refers to education-specific features of Multisim.

AND4

This device performs the logic function of a 4 input AND gate.

Logic function:

$$Y = ABCD$$

AND gate truth table:

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

This topic refers to education-specific features of Multisim.

AND5

This device performs the logic function of a 5 input AND gate.

Logic function:

$$Y=ABCDE$$

AND gate truth table:

Input A	Input B	Input C	Input D	Input E	Output Y
X	X	X	X	0	0
X	X	X	0	X	0
X	X	0	X	X	0
X	0	X	X	X	0
0	X	X	X	X	0
1	1	1	1	1	1

X= Either '0' or '1'

This topic refers to education-specific features of Multisim.

AND6

This device performs the logic function of a 6 input AND gate.

Logic function:

$$Y=ABCDEF$$

Truth table:

Input A	Input B	Input C	Input D	Input E	Input F	Output Y
X	X	X	X	X	0	0
X	X	X	X	0	X	0
X	X	X	0	X	X	0
X	X	0	X	X	X	0
X	0	X	X	X	X	0
0	X	X	X	X	X	0
1	1	1	1	1	1	1

X= Either '0' or '1'

This topic refers to education-specific features of Multisim.

AND7

This device performs the logic function of a 7 input AND gate.

Logic function:

$$Y=ABCDEFG$$

Truth table:

Input A	Input B	Input C	Input D	Input E	Input F	Input G	Output Y
X	X	X	X	X	X	0	0
X	X	X	X	X	0	X	0
X	X	X	X	0	X	X	0
X	X	X	0	X	X	X	0
X	X	0	X	X	X	X	0
X	0	X	X	X	X	X	0
0	X	X	X	X	X	X	0
1	1	1	1	1	1	1	1

X= Either '0' or '1'

This topic refers to education-specific features of Multisim.

AND8

This device performs the logic function of a 8 input AND gate.

Logic function:

$$Y=ABCDEFGH$$

Truth table:

Input A	Input B	Input C	Input D	Input E	Input F	Input G	Input H	Output Y
X	X	X	X	X	X	X	0	0
X	X	X	X	X	X	0	X	0
X	X	X	X	X	0	X	X	0
X	X	X	X	0	X	X	X	0
X	X	X	0	X	X	X	X	0
X	X	0	X	X	X	X	X	0
X	0	X	X	X	X	X	X	0
0	X	X	X	X	X	X	X	0
1	1	1	1	1	1	1	1	1

X= Either '0' or '1'

This topic refers to education-specific features of Multisim.

INV (Inverter)

This device performs the logic function of a 1 input NOT gate.

Logic function:

$$Y = \bar{A}$$

The output Y is true when the input A is NOT true. The output is the inverse of the input: $Y = \text{NOT } A$.

Input A	Output Y
0	1
1	0

This topic refers to education-specific features of Multisim.

NAND2

This device performs the logic function of a 2 input NAND gate.

Logic function:

$$Y = \bar{AB}$$

NAND gate truth table:

Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

This topic refers to education-specific features of Multisim.

NAND3

This device performs the logic function of a 3 input NAND gate.

Logic function:

$$Y = \overline{ABC}$$

NAND gate truth table:

Input A	Input B	Input C	Output Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

This topic refers to education-specific features of Multisim.

NAND4

This device performs the logic function of a 4 input NAND gate.

Logic function:

$$Y = \overline{ABCD}$$

NAND gate truth table:

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

This topic refers to education-specific features of Multisim.

NAND5

This device performs the logic function of a 5 input NAND gate.

Logic function:

$$Y = \overline{ABCDE}$$

Truth table:

Inputs A thru E	Output Y
All inputs 1	0
One or more inputs 0	1

NAND6

This device performs the logic function of a 6 input NAND gate.

Logic function:

$$Y = \overline{ABCDEF}$$

Truth table:

Inputs A thru F	Output Y
All inputs 1	0
One or more inputs 0	1

This topic refers to education-specific features of Multisim.

NAND7

This device performs the logic function of a 7 input NAND gate.

Logic function:

$$Y = \overline{ABCDEFG}$$

Truth table:

Inputs A thru G	Output Y
All inputs 1	0
One or more inputs 0	1

This topic refers to education-specific features of Multisim.

NAND8

This device performs the logic function of a 8 input NAND gate.

Logic function:

$$Y = \overline{ABCDEFGH}$$

Truth table:

Inputs A thru H	Output Y
All inputs 1	0
One or more inputs 0	1

This topic refers to education-specific features of Multisim.

NAND13

This device performs the logic function of a 13 input NAND gate.

Logic function:

$$Y = \overline{ABCDEF}GH\overline{IJKL}M$$

Truth table:

Inputs A thru M	Output Y
All inputs 1	0
One or more inputs 0	1

This topic refers to education-specific features of Multisim.

NOR2

This device performs the logic function of a 2 input NOR gate.

Logic function:

$$Y = \overline{A+B}$$

NOR gate truth table:

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	0

This topic refers to education-specific features of Multisim.

NOR3

This device performs the logic function of a 3 input NOR gate.

Logic function:

$$Y = \overline{A+B+C}$$

NOR gate truth table:

Input A	Input B	Input C	Output Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

This topic refers to education-specific features of Multisim.

NOR4

This device performs the logic function of a 4 input NOR gate.

Logic function:

$$Y = \overline{A+B+C+D}$$

Truth table:

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

This topic refers to education-specific features of Multisim.

NOR5

This device performs the logic function of a 5 input NOR gate.

Logic function:

$$Y = \overline{A+B+C+D+E}$$

Truth table:

Input A	Input B	Input C	Input D	Input E	Output Y
X	X	X	X	1	0
X	X	X	1	X	0
X	X	1	X	X	0
X	1	X	X	X	0
1	X	X	X	X	0
0	0	0	0	0	1

X= Either '0' or '1'

This topic refers to education-specific features of Multisim.

NOR6

This device performs the logic function of a 6 input NOR gate.

Logic function:

$$Y = \overline{A+B+C+D+E+F}$$

Truth table:

Inputs A thru F	Output Y
All inputs 0	1
One or more inputs 1	0

This topic refers to education-specific features of Multisim.

NOR7

This device performs the logic function of a 7 input NOR gate.

Logic function:

$$Y = \overline{A+B+C+D+E+F+G}$$

Truth table:

Inputs A thru G	Output Y
All inputs 0	1
One or more inputs 1	0

This topic refers to education-specific features of Multisim.

NOR8

This device performs the logic function of a 8 input NOR gate.

Logic function:

$$Y = \overline{A+B+C+D+E+F+G+H}$$

Truth table:

Inputs A thru H	Output Y
All inputs 0	1
One or more inputs 1	0

This topic refers to education-specific features of Multisim.

OR2

This device performs the logic function of a 2 input OR gate.

Logic function:

$$Y = A+B$$

OR gate truth table:

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	1

This topic refers to education-specific features of Multisim.

OR3

This device performs the logic function of a 3 input OR gate.

Logic function:

$$Y=A+B+C$$

Truth table:

Input A	Input B	Input C	Output Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

This topic refers to education-specific features of Multisim.

OR4

This device performs the logic function of a 3 input OR gate.

Logic function:

$$Y = A + B + C + D$$

Truth table:

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

This topic refers to education-specific features of Multisim.

OR5

This device performs the logic function of a 5 input OR gate.

Logic function:

$$Y = A + B + C + D + E$$

Truth table:

Input A	Input B	Input C	Input D	Input E	Output Y
X	X	X	X	1	1
X	X	X	1	X	1
X	X	1	X	X	1
X	1	X	X	X	1
1	X	X	X	X	1
0	0	0	0	0	0

X= Either '0' or '1'

This topic refers to education-specific features of Multisim.

OR6

This device performs the logic function of a 6 input OR gate.

Logic function:

$$Y = A + B + C + D + E + F$$

Truth table:

Input A	Input B	Input C	Input D	Input E	Input F	Output Y
X	X	X	X	X	1	1
X	X	X	X	1	X	1
X	X	X	1	X	X	1
X	X	1	X	X	X	1
X	1	X	X	X	X	1
1	X	X	X	X	X	1
0	0	0	0	0	0	0

This topic refers to education-specific features of Multisim.

OR7

This device performs the logic function of a 7 input OR gate.

Logic function:

$$Y = A + B + C + D + E + F + G$$

Truth table:

Inputs A thru G	Output Y
All inputs 0	0
One or more inputs 1	1

This topic refers to education-specific features of Multisim.

OR8

This device performs the logic function of a 8 input OR gate.

Logic function:

$$Y = A + B + C + D + E + F + G + H$$

Truth table:

Inputs A thru H	Output Y
All inputs 0	0
One or more inputs 1	1

This topic refers to education-specific features of Multisim.

XNOR2

This device performs the logic function of a 2 input XNOR gate.

Logic function:

$$Y = AB + \overline{AB}$$

Truth table:

Input A	Input B	Output Y
0	0	1
0	1	0
1	0	0
1	1	1

This topic refers to education-specific features of Multisim.

XNOR3

This device performs the logic function of a 3 input XNOR gate.

Logic function:

$$Y = \overline{ABC} + \overline{ABC} + \overline{ABC} + ABC$$

Truth table:

Input A	Input B	Input C	Output Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

This topic refers to education-specific features of Multisim.

XNOR4

This device performs the logic function of a 4 input XNOR gate.

Logic function:

$$Y = \overline{ABCD} + \overline{ABCD} + \overline{ABCD} + \overline{ABCD} + \overline{ABCD} + \overline{ABCD} + ABCD$$

Truth table:

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

This topic refers to education-specific features of Multisim.

XNOR5

This device performs the logic function of a 5 input XNOR gate.

The output is true when the number of 1s at its inputs is even, and is false when the number of incoming 1s is odd.

Truth table:

Input A	Input B	Input C	Input D	Input E	Output Y
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	0

This topic refers to education-specific features of Multisim.

XNOR6

This device performs the logic function of a 6 input XNOR gate.

The output is true when the number of 1s at its inputs is even, and is false when the number of incoming 1s is odd.

Truth table:

INPUTS						Output Y
A	B	C	D	E	F	O
0	0	0	0	0	0	1
Any odd number of inputs '1'						0
Any even number of inputs '1'						1
1	1	1	1	1	1	1

This topic refers to education-specific features of Multisim.

XNOR7

This device performs the logic function of a 7 input XNOR gate.

The output is true when the number of 1s at its inputs is even, and is false when the number of incoming 1s is odd.

Truth table:

INPUTS							Output Y
A	B	C	D	E	F	G	O
0	0	0	0	0	0	0	0
Any odd number of inputs '1'							0
Any even number of inputs '1'							1
1	1	1	1	1	1	1	0

This topic refers to education-specific features of Multisim.

XNOR8

This device performs the logic function of a 8 input XNOR gate.

The output is true when the number of 1s at its inputs is even, and is false when the number of incoming 1s is odd.

Truth table:

INPUTS								Output Y
A	B	C	D	E	F	G	H	O
0	0	0	0	0	0	0	0	1
Any odd number of inputs '1'								0
Any even number of inputs '1'								1
1	1	1	1	1	1	1	1	1

This topic refers to education-specific features of Multisim.

XOR2

This device performs the logic function of a 2 input XOR gate.

Logic function:

$$Y = \overline{A} \oplus B$$

The output is true if inputs A and B are DIFFERENT.

XOR truth table:

Input A	Input B	Output Y
0	0	0
0	1	1
1	0	1
1	1	0

This topic refers to education-specific features of Multisim.

XOR3

This device performs the logic function of a 3 input XOR gate.

Logic function:

$$Y = \overline{ABC} + \overline{ACB} + \overline{BAC} + ABC$$

The output is true when the number of 1s at its inputs is odd, and is false when the number of incoming 1s is even.

XOR truth table:

Input A	Input B	Input C	Output Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

This topic refers to education-specific features of Multisim.

XOR4

This device performs the logic function of a 4 input XOR gate.

Logic function:

$$Y = \overline{ABCD} + \overline{ABC}\bar{D} + \overline{A}\overline{BCD} + \overline{ABC}\bar{D} + \overline{ABC}\bar{D} + \overline{ABC}\bar{D} + A\overline{BC}\bar{D} + A\overline{B}\overline{C}\bar{D} + A\overline{B}\overline{C}\bar{D}$$

The output is true when the number of 1s at its inputs is odd, and is false when the number of incoming 1s is even.

XOR truth table:

Input A	Input B	Input C	Input D	Output Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

This topic refers to education-specific features of Multisim.

XOR5

This device performs the logic function of a 5 input XOR gate.

The output is true when the number of 1s at its inputs is odd, and is false when the number of incoming 1s is even.

Truth table:

Input A	Input B	Input C	Input D	Input E	Output Y
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	1	0	0	0	0
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	1

This topic refers to education-specific features of Multisim.

XOR6

This device performs the logic function of a 6 input XOR gate.

The output is true when the number of 1s at its inputs is odd, and is false when the number of incoming 1s is even.

Truth table:

INPUTS						Output Y
A	B	C	D	E	F	O
0	0	0	0	0	0	0
Any odd number of inputs '1'						1
Any even number of inputs '1'						0
1	1	1	1	1	1	0

This topic refers to education-specific features of Multisim.

XOR7

This device performs the logic function of a 7 input XOR gate.

The output is true when the number of 1s at its inputs is odd, and is false when the number of incoming 1s is even.

INPUTS							Output Y
A	B	C	D	E	F	G	O
0	0	0	0	0	0	0	0
Any odd number of inputs '1'							1
Any even number of inputs '1'							0
1	1	1	1	1	1	1	1

This topic refers to education-specific features of Multisim.

XOR8

This device performs the logic function of a 8 input XOR gate.

The output is true when the number of 1s at its inputs is odd, and is false when the number of incoming 1s is even.

Truth table:

INPUTS								Output Y
A	B	C	D	E	F	G	H	O
0	0	0	0	0	0	0	0	0
Any odd number of inputs '1'								1
Any even number of inputs '1'								0
1	1	1	1	1	1	1	1	0

This topic refers to education-specific features of Multisim.

Misc

The components in the **Misc Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

Test Label

This device is a visible label for PLD schematics.

This topic refers to education-specific features of Multisim.

Multiplexers

The components in the **Multiplexers Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

MUX2_1

This device is a 2-line-to-1-line multiplexer.

A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination. The basic multiplexer has several data-input lines and a single output line. It also has data-select inputs, which permit digital data on anyone of the inputs to be switched to the output line. Multiplexers are also known as data selectors.

This 2-input multiplexer has a data-select line ($\sim A/B$) and an Enable ($\sim G$). Because there are only two inputs to be selected in the multiplexer, a single data-select input is sufficient.

A LOW on the Enable input allows the selected input data to pass through to the output. A HIGH on the Enable input prevents data from going through to the output; that is, it disables the multiplexer.

Function table:

INPUTS				OUTPUT
$\sim G$	$\sim A/B$	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = HIGH voltage level

L = LOW voltage level

X = Either HIGH or LOW voltage level

This topic refers to education-specific features of Multisim.

MUX2_1_INV

This device is a 2-line to 1-line multiplexer with inverting output.

A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination. The basic multiplexer has several data-input lines and a single output line. It also has data-select inputs, which permit digital data on anyone of the inputs to be switched to the output line. Multiplexers are also known as data selectors.

This 2-input multiplexer has a data-select line ($\sim A/B$) and an Enable ($\sim G$). Because there are only two inputs to be selected in the multiplexer, a single data-select input is sufficient.

A LOW on the Enable input allows the selected input data to pass through to the output. A HIGH on the Enable input prevents data from going through to the output; that is, it disables the multiplexer.

Function table:

INPUTS				OUTPUT
$\sim G$	$\sim A/B$	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level

L = LOW voltage level

X = Either HIGH or LOW voltage level

This topic refers to education-specific features of Multisim.

MUX2_1INV_3S

This device is a 3-state output, 2-line to 1-line multiplexer with inverting output.

A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination. The basic multiplexer has several data-input lines and a single output line. It also has data-select inputs, which permit digital data on anyone of the inputs to be switched to the output line. Multiplexers are also known as data selectors.

This 2-input multiplexer has a data-select line ($\sim A/B$) and an Enable ($\sim G$). Because there are only two inputs to be selected in the multiplexer, a single data-select input is sufficient.

A LOW on the Enable input allows the selected input data to pass through to the output. A HIGH on the Enable input prevents data from going through to the output; that is, it puts the output in a high impedance state.

Function table:

INPUTS				OUTPUT
$\sim G$	$\sim A/B$	A	B	Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level

L = LOW voltage level

X= Either HIGH or LOW voltage level

Z= High impedance ‘OFF’ state

This topic refers to education-specific features of Multisim.

MUX4_1

This device is a 4-line-to-1-line multiplexer.

A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination. The basic multiplexer has several data-input lines and a single output line. It also has data-select inputs, which permit digital data on anyone of the inputs to be switched to the output line. Multiplexers are also known as data selectors.

This 4-input multiplexer can select 1 bit of data from up to four sources selected by Select inputs (S0, S1). The 4-input multiplexer circuit has active-Low Enables ($\sim EN$) which can be used to strobe the output. Output (Y) is forced Low when the Enable ($\sim EN$) is High.

This device is the logic implementation of a 1-pole, 4-position switch where the switch is determined by the logic levels supplied to the select inputs.

Function table:

INPUTS							OUTPUT
S0	S1	$\sim EN$	I0	I1	I2	I3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level

L = LOW voltage level

X= Either HIGH or LOW voltage level

This topic refers to education-specific features of Multisim.

MUX4_1_INVO

This device is a 4-line to 1-line multiplexer with the output inverted.

A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination. The basic multiplexer has several data-input lines and a single output line. It also has data-select inputs, which permit digital data on anyone of the inputs to be switched to the output line. Multiplexers are also known as data selectors.

This 4-input multiplexer can select 1 bit of data from up to four sources selected by Select inputs (S0, S1). The 4-input multiplexer circuit has active-Low Enables ($\sim EN$) which can be used to strobe the output. Output (Y) is forced Low when the Enable ($\sim EN$) is High.

This device is the logic implementation of a 1-pole, 4-position switch where the switch is determined by the logic levels supplied to the select inputs.

Function table:

INPUTS							OUTPUT
S0	S1	~EN	I0	I1	I2	I3	Y
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH voltage level

L = LOW voltage level

X= Either HIGH or LOW voltage level

This topic refers to education-specific features of Multisim.

MUX8_1

This device is a 8-line-to-1-line multiplexer.

A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination. The basic multiplexer has several data-input lines and a single output line. It also has data-select inputs, which permit digital data on anyone of the inputs to be switched to the output line. Multiplexers are also known as data selectors.

This multiplexer has eight data inputs (D0 -D7) and, therefore, three data-select or address input lines (A, B, C). Three bits are required to select any one of the eight data inputs ($2^3 = 8$). A LOW on the Enable input allows the selected input data to pass through to the output.

This device is the logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs (A, B, C).

Function table:

INPUTS												OUTPUT
~G	C	B	A	D0	D1	D2	D3	D4	D5	D6	D7	Y
H	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	L	H	X	L	X	X	X	X	X	X	L
L	L	L	H	X	H	X	X	X	X	X	X	H
L	L	H	L	X	X	L	X	X	X	X	X	L
L	L	H	L	X	X	H	X	X	X	X	X	H
L	L	H	H	X	X	X	L	X	X	X	X	L
L	L	H	H	X	X	X	H	X	X	X	X	H
L	H	L	L	X	X	X	X	L	X	X	X	L
L	H	L	L	X	X	X	H	X	X	X	X	H
L	H	L	H	X	X	X	X	X	L	X	X	L
L	H	L	H	X	X	X	X	H	X	X	X	H
L	H	H	L	X	X	X	X	X	X	L	X	L
L	H	H	H	X	X	X	X	X	X	X	L	L
L	H	H	H	X	X	X	X	X	X	X	H	H

H = HIGH voltage level

L = LOW voltage level

X= Either HIGH or LOW voltage level

This topic refers to education-specific features of Multisim.

Shift Registers

The components in the **Shift Registers Family** of the **PLD Logic Group** are only available from a PLD schematic.

Refer to the [PLD Schematics](#) section for more information.

This topic refers to education-specific features of Multisim.

SR_4BIDI

This device is a 4 Bit Bidirectional Universal Shift Register. It features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs and overriding clear input.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is HIGH and S1 is LOW. Serial data for this mode is entered at the shift right data input (SR). When S0 is LOW and S1 is HIGH, data shifts left synchronously and new data is entered at the shift left serial input (SL).

Synchronous parallel loading is accomplished by applying the four bits of data (A, B, C, D) and taking both mode control inputs, S0 and S1, HIGH. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input.

The clock input is inhibited when both mode control inputs are LOW.

Shift Register function table:

CLR	INPUTS								OUTPUTS				
	MODE		CLK	SERIAL		PARALLEL				QA	QB	QC	QD
	S1	S0		SL	SR	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	QA ₀	QB ₀	QC ₀	QD ₀
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	QA _n	QB _n	QC _n
H	L	H	↑	X	L	X	X	X	X	L	QA _n	QB _n	QC _n
H	H	L	↑	H	X	X	X	X	X	QB _n	QC _n	QD _n	H
H	H	L	↑	L	X	X	X	X	X	QB _n	QC _n	QD _n	L
H	L	L	X	X	X	X	X	X	X	QA ₀	QB ₀	QC ₀	QD ₀

H = HIGH level

L = LOW Level

X = Don't Care

QA₀, QB₀, QC₀, QD₀ = The level of QA, QB, QC, QD before the indicated steady state input conditions were established.

QA_n, QB_n, QC_n, QD_n = The level of QA, QB, QC, QD before most recent LOW-to-HIGH transition of the Clock.

↑ = LOW-to-HIGH transition of the Clock.

This topic refers to education-specific features of Multisim.

SR_4P_P_3SO

This device is a 4 Bit Shifter with 3 State Outputs that make possible to perform shifts of 0, 1, 2 or 3 places on words. A 4 bit data word is introduced at the In inputs and is shifted according to the code applied to the select inputs S0 and S1. Outputs Y0 to Y3 are 3 State outputs and are controlled by an active LOW Output Enable input (**OE**). When **OE** is LOW, data outputs follow selected data inputs. When **OE** is HIGH the outputs are forced to the high impedance state.

Shift Register function table:

INPUTS			OUTPUTS			
OE	S1	S0	Y0	Y1	Y2	Y3
H	X	X	Z	Z	Z	Z
L	L	L	I0	I1	I2	I3
L	L	H	I-1	I0	I1	I2
L	H	L	I-2	I-1	I0	I1
L	H	H	I-3	I-2	I-1	I0

H = HIGH level.

L = LOW Level.

X = Don't Care.

Z = High Impedance.

This topic refers to education-specific features of Multisim.

SR_4P_P_INV

This device is a 4 Bit Parallel-In/Parallel-Out Shift Register with one extra complemented output. The Shift Register has two modes of operation, shift from QA toward QD and parallel load which are controlled by the **SH/ LD** input. When **SH/ LD** is HIGH serial data enters the first flip-flop via the J and K inputs and is shifted in the direction mentioned above following each LOW-to-HIGH transition of the clock (CLK) input. When **SH/ LD** input is LOW the data on the parallel inputs (A, B, C, D) is transferred to the outputs following the LOW-to-HIGH transition of the clock.

A LOW on the asynchronous Master Reset (**CLR**) input sets all outputs LOW, independent of any other input condition.

Shift Register function table:

OPERATING MODE	INPUTS					OUTPUT				
	CLR	SH/ LD	J	K	Pn	QA	QB	QC	QD	QD
RESET	L	X	X	X	X	L	L	L	L	H
SHIFT, Set First Stage	H	h	h	h	X	H	q0	q1	q2	q2
SHIFT, Reset First	H	h	l	l	X	L	q0	q1	q2	q2
SHIFT, Toggle First Stage	H	h	h	l	X	q0	q0	q1	q2	q2
SHIFT, Retain First Stage	H	h	l	h	X	q0	q0	q1	q2	q2
Parallel Load	H	l	X	X	pn	p0	p1	p2	p3	p3

H – HIGH level.

L = LOW Level.

X = Don't Care.

l = LOW level one setup time prior to the LOW-to-HIGH clock transition.

h = HIGH level one setup time prior to the LOW-to-HIGH clock transition.

pn, qn = The state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

↑ = LOW-to-HIGH transition of the Clock.

This topic refers to education-specific features of Multisim.

SR_4S_P

This device is a 4 Stage Serial-In/Parallel-Out Shift Register. The data present at the D input is shifted over one stage at each LOW-to-HIGH transition of the clock pulse (CP). A HIGH signal present at the RESET input will reset all stages asynchronously with the clock pulse.

Shift Register function table:

INPUTS			OUTPUTS	
CP	D	R	Q1	Qn
↑	L	L	L	Qn-1
↑	H	L	H	Qn-1
↓	X	L	Q1	Qn
X	X	H	L	L

H – HIGH level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH transition of the Clock.

This topic refers to education-specific features of Multisim.

SR_8P_2S

This device is an 8 Stage Serial-In/Parallel and Serial-Out Shift Register. It consists of an 8 Bit shift register and an 8 Bit latch with 3 State Output buffer. Data is shifted on the LOW-to-HIGH transition of the clock pulse (CP). The data in each shift register stage is transferred to the storage register when the Strobe input (STR) is HIGH. Data in the storage register appears at the outputs when the Output Enable input (OE) is HIGH. Two serial outputs (QS1, QS2) are available for cascading more shift registers. Data is available at the QS1 output on the LOW-to-HIGH Clock transition. The same information is available at the QS2 output on the next HIGH-to-LOW

Clock transition.

Shift Register function table:

INPUTS				PARALLEL OUTPUTS		SERIAL OUTPUTS	
CP	OE	STR	D	Q0	Qn	QS1	QS2
↑	L	X	X	Z	Z	Q'6	NC
↓	L	X	X	Z	Z	NC	Q7
↑	H	L	X	NC	NC	Q'6	NC
↑	H	H	L	L	Qn-1	Q'6	NC
↑	H	H	H	H	Qn-1	Q'6	NC
↓	H	H	H	NC	NC	NC	Q7

H = HIGH level.

L = LOW Level.

X = Don't Care.

NC = No Change.

Z = High Impedance.

↑ = LOW-to-HIGH transition of the Clock.

↓ = HIGH-to-LOW transition of the Clock.

Q'6 = The information in the seventh register stage is transferred to the 8th register stage and Qn output at the LOW-to-HIGH Clock transition.

This topic refers to education-specific features of Multisim.

SR_8P_S

This device is an 8 Bit Parallel-In/Serial-Out Shift Register with complementary outputs which shifts data in the direction QA toward QH on the rising edge of the clock input (CLK). In the Shift Mode QA gets the value at the Serial Input (SER) on the rising edge of the clock. Data at the parallel inputs (A to H) are loaded into the register on a HIGH-to-LOW transition of the SH/ LD input regardless of the logic levels on the clock, clock inhibit or serial inputs.

A HIGH level at the INH input inhibits clocking.

Shift Register function table:

SH/ LD	INH	CLK	SERIAL	INPUTS		OUTPUTS	
				PARALLEL		QH	\overline{QH}
L	X	X	X	a...h		h	\overline{h}
H	L	L	X	X		QH_0	$\overline{QH_0}$
H	L	↑	H	X		QG_0	$\overline{QG_0}$
H	L	↑	L	X		QG_0	$\overline{QG_0}$
H	H	X	X	X		QH_0	$\overline{QH_0}$

H – HIGH level.

L = LOW Level.

X = Don't Care.

QH_0, QG_0 = The level of QH, QG before the indicated steady state input conditions were established.

a...h = Data at the parallel inputs

↑ = LOW-to-HIGH transition of the Clock.

This topic refers to education-specific features of Multisim.

SR_8P_S_C

This device is an 8 Bit Parallel-In/Serial-Out Shift Register with overriding clear (\overline{CLR}) input which shifts data in the direction QA toward QH on the rising edge of the clock input (CLK). In the Shift Mode QA gets the value at the Serial Input (SER) on the rising edge of the clock. Data at the parallel inputs (A to H) are loaded synchronously into the register if the SH/ LD input is LOW. During parallel loading, serial data flow is inhibited. The CLR overrides all inputs, including CLK. A LOW signal at the CLR input sets all internal flip-flops to zero.

A HIGH level at the INH input inhibits clocking.

Shift Register function table:

INPUTS						OUTPUTS	
CLR	SH/ LD	INH	CLK	SER	PARALLEL		QH
					A ... H		
L	X	X	X	X	X		L
H	X	L	L	X	X		QH ₀
H	L	L	↑	X	a...h		H
H	H	L	↑	H	X		QG ₀
H	H	L	↑	L	X		QG ₀
H	X	H	↑	X	X		QH ₀

H – HIGH level.

L = LOW Level.

X = Don't Care.

QH₀, QG₀ = The level of QH, QG before the indicated steady state input conditions were established.

a...h = Data at the parallel inputs

↑ = LOW-to-HIGH transition of the Clock.

This topic refers to education-specific features of Multisim.

SR_8PS_S_ASL

This device is a 8 Stage Parallel or Serial-In/Serial-Out Shift Register with Parallel/Serial control inputs, a single serial data input (DS) and individual parallel inputs (P0 to P7) to each register stage. In addition to the output from the 8th stage O8, O7 and O6 outputs are also available from stages 7 and 6. Serial entry is made on the LOW-to-HIGH transition of the Clock pulse (CP). Entry is controlled by the Parallel/Serial control input (P/S). When PE is LOW, data is serially shifted into the 8 Stage register synchronously with the LOW-to-HIGH transition of the clock pulse. When P/S is HIGH data is loaded into the 8 Stage register via the parallel input lines asynchronously with the clock pulse.

Shift Register function table:

INPUTS					OUTPUTS	
CP	DS	P/S	P0	Pn	Q1 (internal)	Qn
X	X	H	L	L	L	L
X	X	H	L	H	L	H
X	X	H	H	L	H	L
X	X	H	H	H	H	H
↑	L	L	X	X	L	Q _{n-1}
↑	H	L	X	X	H	Q _{n-1}
↓	X	L	X	X	Q1	Qn

H – HIGH level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH transition of the Clock.

↓ = HIGH-to-LOW transition of the Clock.

This topic refers to education-specific features of Multisim.

SR_8PS_S_SL

This device is an 8 Stage Parallel or Serial-In/Serial-Out Shift Register with Parallel/Serial control inputs, a single serial data input (DS) and individual parallel inputs (P0 to P7) to each register stage. In addition to the output from the 8th stage O8, O7 and O6 outputs are also available from stages 7 and 6. Parallel and serial entry is made on the LOW-to-HIGH transition of the clock pulse (CP). Entry is controlled by the Parallel/Serial control input (PE). When PE is LOW, data is serially shifted into the 8 Stage register synchronously with the LOW-to-HIGH transition of the clock pulse. When PE is HIGH data is loaded into the 8 Stage register via the parallel input lines synchronously with the LOW-to-HIGH transition of the clock pulse.

Shift Register function table:

INPUTS					OUTPUTS	
CP	DS	PE	P0	Pn	Q1 (internal)	Qn
↑	X	H	L	L	L	L
↑	X	H	H	L	H	L
↑	X	H	L	H	L	H
↑	X	H	H	H	H	H
↑	L	L	X	X	L	Qn-1
↑	H	L	X	X	H	Qn-1
↓	X	X	X	X	Q1	Qn

H = HIGH level.

L = LOW Level.

X = Don't Care.

↑ = LOW-to-HIGH transition of the Clock.

↓ = HIGH-to-LOW transition of the Clock.

This topic refers to education-specific features of Multisim.

SR_8S_P

This device is a 8 Bit Serial-In/Parallel-Out Shift Register. Data is entered serially through one of the two inputs (A or B) synchronously with the LOW-to-HIGH transition of the clock input (CLK).

A LOW on the asynchronous Master Reset ($\overline{\text{CLR}}$) input sets all outputs LOW, independent of any other input condition.

Shift Register function table:

OPERATING MODE	INPUTS			OUTPUTS	
	CLR	A	B	QA	QB...QH
RESET	L	X	X	L	L...L
SHIFT	H	l	l	L	q0...q6
SHIFT	H	l	h	L	q0...q6
SHIFT	H	h	l	L	q0...q6
SHIFT	H	h	h	H	q0...q6

H – HIGH level.

L = LOW Level.

X = Don't Care.

l = LOW level one setup time prior to the LOW-to-HIGH clock transition.

h = HIGH level one setup time prior to the LOW-to-HIGH clock transition.

qn = The state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.

This topic refers to education-specific features of Multisim.