Main Radio Control State Transition Times

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- *MARC*
- *System Clock Division*
- *Frequency Synthesizer Calibration*
- *CC1110*
- *CC1111*
- *CC2510*
- *CC2511*

1 Introduction

The ***CC1110Fx/CC1111Fx*** and ***CC2510Fx/CC2511Fx*** have built-in state machines called main radio controller (MARC) which are used to switch between operation states (modes). Changing between states is done either by using command strobes or by internal events such as completing the transmission of a packet.

The possible destination states are IDLE, FSTXON, TX, and RX (there are more states but they are not discussed in this design note).
Table 71 in the data sheets ([1] and [2]) shows the state transition timing when the system clock is not divided, i.e., `CLKCON.CLKSPD`=000_b, and recommended settings from SmartRF™ Studio [3] are used (version 6.9.2.0). However, the timings will vary if the divided system clock is utilized (`CLKCON.CLKSPD`≠000_b) or if the recommended settings are altered. This design note explains the variations of the state transition timings for non-standard usage of the radio peripheral. A portion of the state transition timings are scaled linearly with the clock division factor, while other parts are not. The variations are explained in Section 3.

The frequency synthesizer calibration time is also variable based on the values of `TEST0` and `FSCAL3.CHP_CURR_CAL_EN`. This is explained in Section 3.2.

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2 Abbreviations

FS	Frequency Synthesizer
MARC	Main Radio Controller
PA	Power Amplifier
VCO	Voltage Controlled Oscillator

3 State Transition Times

The main radio controller needs to wait in certain states in order to make sure that the internal analog/digital parts have settled down and are ready to operate in the new states. A number of factors are important for the state transition times:

- The crystal oscillator frequency, f_{xosc}
- The system clock division factor
- PA ramping enabled or not
- The data rate in cases where PA ramping is enabled
- The value of the TEST0, TEST1, and FSCAL3 registers

In this document, f_{Ref} is used to denote the reference frequency. For ***CC1110Fx*** and ***CC2510Fx*** $f_{Ref} = f_{xosc}$ and for ***CC1111Fx*** and ***CC2511Fx*** $f_{Ref} = f_{xosc}/2$.

3.1 Overall State Transition Times

Table 1 summarizes the transition times for important states. The system clock frequency is denoted as f_{sys} and is divided when CLKCON.CLKSPD≠000_b. That is, $f_{sys} = f_{Ref}/2^{CLKCON.CLKSPD}$.

Description	**Transition Time (Recommended settings from SmartRF™ Studio [3], no PA ramping)**	**Transition Time [µs] when f_{Ref} = 26 MHz, CLKCON.CLKSPD=000_b, data rate = 250 kBaud, TEST0=0x0B and FSCAL3.CHP_CURR_CAL_EN=10 (max calibration time)**
IDLE to RX, no calibration	$1953/f_{sys}$	75.1
IDLE to RX, with calibration	$1953/f_{sys}$ + FS calibration Time	799
IDLE to TX/FSTXON, no calibration	$1954/f_{sys}$	75.2
IDLE to TX/FSTXON, with calibration	$1953/f_{sys}$ + FS calibration Time	799
TX to RX switch	$782/f_{sys}$ + $0.25/f_{symbol}$	31.1
RX to TX switch	$782/f_{sys}$	30.1
TX to IDLE, no calibration	~$0.25/f_{symbol}$	~1
TX to IDLE, with calibration	~$0.25/f_{symbol}$ + FS calibration Time	725
RX to IDLE, no calibration	$2/f_{sys}$	~0.1
RX to IDLE, with calibration	$2/f_{sys}$ + FS calibration Time	724
Manual calibration	$283/f_{sys}$ + FS calibration Time	735

Table 1. Overall State Transition Times

The values in Table 1 are valid when TEST1 is set to the values recommended by SmartRF™ Studio [3] (preferred settings).

Note that TX to IDLE and TX to RX transition times are functions of data rate (f_{symbol}). When PA ramping is enabled (this option is only available for CC111x) (i.e., FREND0.PA_POWER≠000_b), TX to IDLE and TX to RX will require (FREND0.PA_POWER)/8·f_{symbol} longer times than the times stated in Table 1, where f_{symbol} is the symbol rate for data transmission.

3.2 Frequency Synthesizer Calibration Time

The frequency synthesizer's characteristics will vary with temperature and supply voltage changes. In addition, the VCO's characteristics will be different for different operation frequencies. Therefore, in order to ensure reliable operation, the frequency synthesizer should be calibrated regularly. The calibration must be performed after turning on the power

and before using a new frequency or channel. ***CC1110Fx/CC1111Fx*** and ***CC2510Fx/CC2511Fx*** include a self-calibration circuitry which calibrates the VCO, charge pump circuitry, and other parts of the frequency synthesizer. The self-calibration circuitry consists of a state machine which controls the required timings. The calibration circuit operates directly with reference clock from the crystal oscillator (f_{Ref}), and will not vary with different system clock settings.

Table 2 summarizes the calibration times for possible settings of TEST0 and FSCAL3.CHP_CURR_CAL_EN. Setting FSCAL3.CHP_CURR_CAL_EN to 00_b disables the charge pump calibration stage. TEST0 is set to the values recommended by SmartRF™ Studio [3]. The possible values for TEST0 when operating with different frequency bands are 0x09 and 0x0B. SmartRF™ Studio [3] always sets FSCAL3.CHP_CURR_CAL_EN to 10_b.

TEST0	FSCAL3.CHP_CURR_CAL_EN	FS Calibration Time
0x09	00_b	$3764/f_{Ref}$
0x09	10_b	$18506/f_{Ref}$
0x0B	00_b	$4073/f_{Ref}$
0x0B	10_b	$18815/f_{Ref}$

Table 2. Frequency Synthesizer Calibration Times

4 Low Power Transceiver Strategy

A receiver system may need to wait for a packet for a time interval because of uncertainty in the packet arrival time. In most systems when waiting for a packet the system is idle or has a low activity and it might therefore be advantageous to lower the system clock frequency to save power. It is important to note that when a large clock division ratio is used, the state transitions might take up to several milliseconds. Clock division is originally done for reducing the power consumption of the digital units in idle/low traffic periods. However, the longer transition times due to clock division may cause larger power consumption compared to full-clock speed.

A solution to this problem is to keep the system clock undivided until the MARC enters RX or TX state and then reduce the system clock speed. Note that from Table 1, RX to TX (and TX to RX) switch time is 782 system clock cycles and therefore is a function of division ratio. If a large division ratio is used, this switching may take up to several milliseconds. For low power application it is important to switch back to full system clock speed before switching from RX to TX or vice versa.

Figure 1 depicts the transient total current for IDLE to RX state transitions (with calibration) for four cases (Series 1 - 4). In Series 1 and 2, the CPU is halted immediately after strobing RX. In Series 3 and 4, after strobing RX, the system will wait until MARC enters the RX state (MARCSTATE=RX) and then halt the CPU.

It can be seen that lowering the system clock using clock division with the purpose of lowering the power consumption may be beneficial; however, special care must be taken with respect to longer transition times. In fact, the low power strategy may vary for different applications.

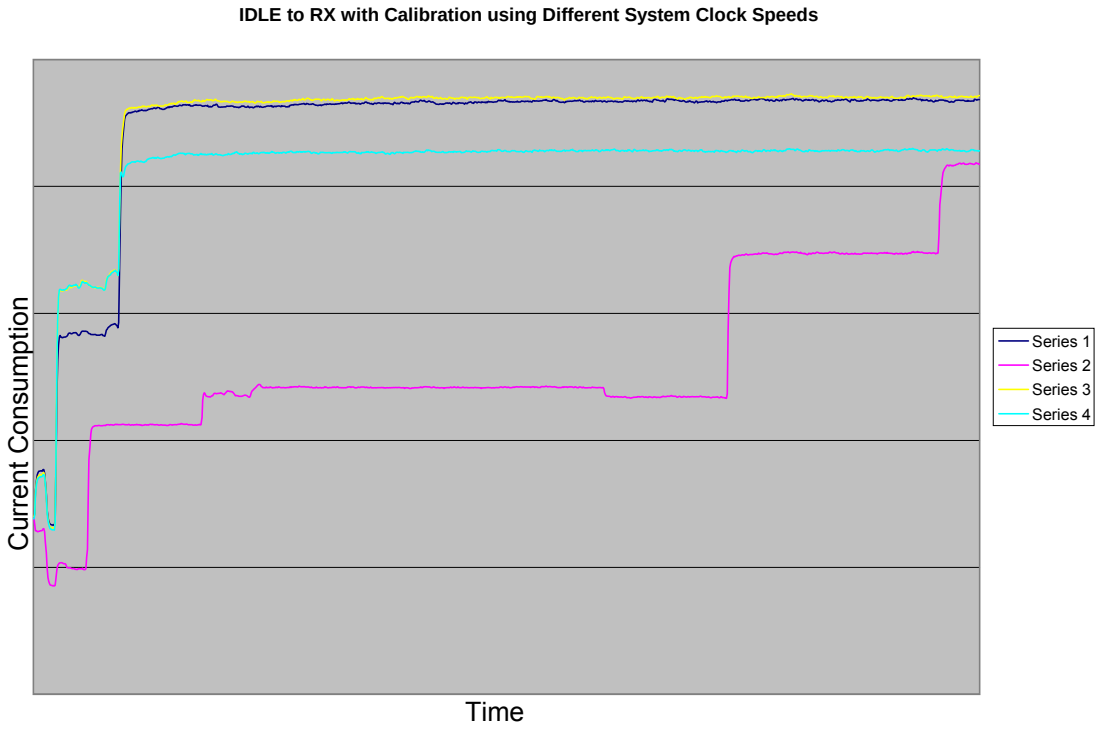

Figure 1. Transient Total Current for IDLE to RX State Transition (with calibration)

Series 1:

Wake up from PM2 and turn on XOSC (26 MHz)
Strobe RX (with calibration)
Enter PM0 (CPU idle)

Series 2:

Wake up from PM2 and turn on XOSC (203.125 kHz)
Strobe RX (with calibration)
Enter PM0 (CPU idle)

Series 3:

Wake up from PM2 and turn on XOSC (26 MHz)
Strobe RX (with calibration)
Wait for RX state (polling `MARCSTATE`)
Enter PM0 (CPU idle)

Series 4:

Wake up from PM2 and turn on XOSC (26 MHz)
Strobe RX (with calibration)
Wait for RX state (polling `MARCSTATE`)
Change system clock to 203.125 kHz
Enter PM0 (CPU idle)

5 Examples

In order to illustrate how the clock division can be used to reduce the power consumption three examples are considered.

5.1 Example 1

The following conditions are assumed in this example:

Reference Clock Frequency = 26 MHz
The chip is in sleep mode and wakes up every 10 seconds to receive a packet of length 10 ms. Each time the chip wakes up it strobes RX, performs FS calibration and enters RX state. Then it waits for an average of 100 ms to receive a packet. After receiving the packet the chip will go to sleep until the next wake-up happens.

By integrating the transient total current (Figure 1) over time, the average current for infinitely large time for these scenarios will be:

Series 1: I_{av} = 1.112 mA (f_{sys} = 26 MHz, IDLE to RX time from Table 1 is 799 µs).

Series 2: I_{av} = 1.100 mA (f_{sys} = 203.125 kHz, IDLE to RX time from Table 1 is 10.338 ms).

Series 3: I_{av} = 1.114 mA (IDLE to RX time from Table 1 is 799 µs).

Series 4: I_{av} = 1.093 mA (IDLE to RX time from Table 1 is 799 µs).

Series 4, i.e., polling `MARCSTATE` and changing the system clock speed when `MARCSTATE`=RX gives the lowest power consumption.

5.2 Example 2

The following conditions are assumed in this example:

Reference Clock Frequency = 26 MHz
The chip is in sleep mode and wakes up every 100 ms to receive a packet of length 1 ms. Each time the chip wakes up it strobes RX, performs FS calibration and enters RX state. Then it waits for an average of 3 ms to receive a packet. After receiving the packet the chip will go to sleep until the next wake-up happens.

By integrating the transient total current (Figure 1) over time, the average current for infinitely large time for these scenarios will be:

Series 1: I_{av} = 1.773 mA (f_{sys} = 26 MHz, IDLE to RX time from Table 1 is 799 µs).

Series 2: I_{av} = 2.609 mA (f_{sys} = 203.125 kHz, IDLE to RX time from Table 1 is 10.338 ms).

Series 3: I_{av} = 1.793 mA (IDLE to RX time from Table 1 is 799 µs).

Series 4: I_{av} = 1.714 mA (IDLE to RX time from Table 1 is 799 µs).

Series 4, i.e., polling `MARCSTATE` and changing the system clock speed when `MARCSTATE`=RX gives the lowest power consumption. Note that, Series 2 in this example give very large power consumptions while in Example 1, Series 2 gives relatively low power consumption

5.3 Example 3

The following conditions are assumed in this example:

Reference Clock Frequency = 26 MHz
The chip is in sleep mode and wakes up every 15 ms to receive a packet. In this example, RX will be terminated if the received signal strength indicator (RSSI) is lower than programmed threshold (`MCSM2.RX_TIME_RSSI`=1_b). Each time the chip wakes up it strobes RX, performs FS calibration and enters RX state. The time required to compute the RSSI value is dependent on the data-rate and other parameters as discussed in [4]. After the RSSI value is computed, RX will be terminated if the signal strength is not sufficient. In this example, it is assumed that the computed RSSI value will be always lower than the threshold and all RX attempts will be terminated and chip will go to sleep until the next wake-up happens. The time

needed to compute the RSSI value in this example is approximately 240 µs (10 kBaud, see DN505 [4]).

By integrating the transient total current (Figure 1) over time, the average current for this scenario will be:

Series 1: I_{av} = 1.733 mA (f_{sys} = 26 MHz, IDLE to RX time from Table 1 is 799 µs).
Series 2: I_{av} = 7.875 mA (f_{sys} = 203.125 kHz, IDLE to RX time from Table 1 is 10.338 ms).
Series 3: I_{av} = 1.830 mA (IDLE to RX time from Table 1 is 799 µs).
Series 4: I_{av} = 1.797 mA (IDLE to RX time from Table 1 is 799 µs).

In this example Series 1 gives the lowest power consumption.

6 References

[1] CC1110Fx/CC1111Fx Low-Power SoC (System-on-Chip) with MCU, Memory, Sub-1 GHz RF Transceiver, and USB Controller (cc1110f32.pdf)

[2] CC2510Fx/CC2511Fx Low-Power SoC (System-on-Chip) with MCU, Memory, Sub-1 GHz RF Transceiver, and USB Controller (cc2510f32.pdf)

[3] SmartRF™ Studio (swrc046.zip)

[4] DN505 RSSI Interpretation and Timing, Design Note DN505, (swra114.pdf)

7 General Information

7.1 Document History

Revision	Date	Description/Changes
SWRA191	2008.07.11	Initial release.

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