

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages)

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state [1]	Description
PIO0_0 to PIO0_11			I/O		Port 0 — Port 0 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pins depends on the function selected through the IOCONFIG register block.
RESET/PIO0_0	23 [2]	yes	I	I; PU	RESET — External reset input with 20 ns glitch filter. A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. In deep power-down mode, this pin must be pulled HIGH externally. The RESET pin can be left unconnected or be used as a GPIO pin if an external RESET function is not needed and Deep power-down mode is not used.
					I/O - PIO0_0 — General purpose digital input/output pin with 10 ns glitch filter.
PIO0_1/CLKOUT/ CT32B0_MAT2	24 [3]	yes	I/O	I; PU	PIO0_1 — General purpose digital input/output pin. A LOW level on this pin during reset starts the ISP command handler.
			O	-	CLKOUT — Clockout pin.
			O	-	CT32B0_MAT2 — Match output 2 for 32-bit timer 0.
PIO0_2/SSEL0/ CT16B0_CAP0	25 [3]	yes	I/O	I; PU	PIO0_2 — General purpose digital input/output pin.
			I/O	-	SSEL0 — Slave Select for SPI0.
			I	-	CT16B0_CAP0 — Capture input 0 for 16-bit timer 0.
PIO0_3	26 [3]	yes	I/O	I; PU	PIO0_3 — General purpose digital input/output pin.
PIO0_4/SCL	27 [4]	yes	I/O	I; IA	PIO0_4 — General purpose digital input/output pin (open-drain).
			I/O	-	SCL — I ² C-bus, open-drain clock input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_5/SDA	5 [4]	yes	I/O	I; IA	PIO0_5 — General purpose digital input/output pin (open-drain).
			I/O	-	SDA — I ² C-bus, open-drain data input/output. High-current sink only if I ² C Fast-mode Plus is selected in the I/O configuration register.
PIO0_6/SCK0	6 [3]	yes	I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
PIO0_7/CTS	28 [3]	yes	I/O	I; PU	PIO0_7 — General purpose digital input/output pin (high-current output driver).
			I	-	CTS — Clear To Send input for UART.
PIO0_8/MISO0/ CT16B0_MAT0	1 [3]	yes	I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
			I/O	-	MISO0 — Master In Slave Out for SPI0.
			O	-	CT16B0_MAT0 — Match output 0 for 16-bit timer 0.
PIO0_9/MOSI0/ CT16B0_MAT1	2 [3]	yes	I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
			I/O	-	MOSI0 — Master Out Slave In for SPI0.
			O	-	CT16B0_MAT1 — Match output 1 for 16-bit timer 0.

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages) ...continued

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state [1]	Description
SWCLK/PIO0_10/ SCK0/ CT16B0_MAT2	3 [3]	yes	I	I; PU	SWCLK — Serial wire clock.
			I/O	-	PIO0_10 — General purpose digital input/output pin.
			I/O	-	SCK0 — Serial clock for SPI0.
			O	-	CT16B0_MAT2 — Match output 2 for 16-bit timer 0.
R/PIO0_11/ AD0/CT32B0_MAT3	4 [5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO0_11 — General purpose digital input/output pin.
			I	-	AD0 — A/D converter, input 0.
			O	-	CT32B0_MAT3 — Match output 3 for 32-bit timer 0.
PIO1_0 to PIO1_9			I/O		Port 1 — Port 1 is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 1 pins depends on the function selected through the IOCONFIG register block.
R/PIO1_0/ AD1/CT32B1_CAP0	9 [5]	yes	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_0 — General purpose digital input/output pin.
			I	-	AD1 — A/D converter, input 1.
			I	-	CT32B1_CAP0 — Capture input 0 for 32-bit timer 1.
R/PIO1_1/ AD2/CT32B1_MAT0	10 [5]	no	O	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_1 — General purpose digital input/output pin.
			I	-	AD2 — A/D converter, input 2.
			O	-	CT32B1_MAT0 — Match output 0 for 32-bit timer 1.
R/PIO1_2/ AD3/CT32B1_MAT1	11 [5]	no	I	I; PU	R — Reserved. Configure for an alternate function in the IOCONFIG block.
			I/O	-	PIO1_2 — General purpose digital input/output pin.
			I	-	AD3 — A/D converter, input 3.
			O	-	CT32B1_MAT1 — Match output 1 for 32-bit timer 1.
SWDIO/PIO1_3/ AD4/CT32B1_MAT2	12 [5]	no	I/O	I; PU	SWDIO — Serial wire debug input/output.
			I/O	-	PIO1_3 — General purpose digital input/output pin.
			I	-	AD4 — A/D converter, input 4.
			O	-	CT32B1_MAT2 — Match output 2 for 32-bit timer 1.
PIO1_4/AD5/ CT32B1_MAT3/ WAKEUP	13 [5]	no	I/O	I; PU	PIO1_4 — General purpose digital input/output pin with 10 ns glitch filter. In Deep power-down mode, this pin serves as the Deep power-down mode wake-up pin with 20 ns glitch filter. Pull this pin HIGH externally before entering Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
			I	-	AD5 — A/D converter, input 5.
			O	-	CT32B1_MAT3 — Match output 3 for 32-bit timer 1.

Table 7. LPC1100L series: LPC1112/14 pin description table (TSSOP28 and DIP28 packages) ...continued

Symbol	Pin TSSOP28/ DIP28	Start logic input	Type	Reset state [1]	Description
PIO1_5/RTS/ CT32B0_CAP0	14 [3]	no	I/O	I; PU	PIO1_5 — General purpose digital input/output pin.
			O	-	RTS — Request To Send output for UART.
			I	-	CT32B0_CAP0 — Capture input 0 for 32-bit timer 0.
PIO1_6/RXD/ CT32B0_MAT0	15 [3]	no	I/O	I; PU	PIO1_6 — General purpose digital input/output pin.
			I	-	RXD — Receiver input for UART.
			O	-	CT32B0_MAT0 — Match output 0 for 32-bit timer 0.
PIO1_7/TXD/ CT32B0_MAT1	16 [3]	no	I/O	I; PU	PIO1_7 — General purpose digital input/output pin.
			O	-	TXD — Transmitter output for UART.
			O	-	CT32B0_MAT1 — Match output 1 for 32-bit timer 0.
PIO1_8/ CT16B1_CAP0	17 [3]	no	I/O	I; PU	PIO1_8 — General purpose digital input/output pin.
			I	-	CT16B1_CAP0 — Capture input 0 for 16-bit timer 1.
PIO1_9/ CT16B1_MAT0	18 [3]	no	I/O	I; PU	PIO1_9 — General purpose digital input/output pin.
			O	-	CT16B1_MAT0 — Match output 0 for 16-bit timer 1.
V _{DD}	21	-	-	-	3.3 V supply voltage to the internal regulator and the external rail.
V _{DDA}	7	-	-	-	3.3 V supply voltage to the ADC. Also used as the ADC reference voltage.
XTALIN	20 [6]	-	I	-	Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.8 V.
XTALOUT	19 [6]	-	O	-	Output from the oscillator amplifier.
V _{SS}	22	-	-	-	Ground.
V _{SSA}	8	-	-	-	Analog ground.

[1] Pin state at reset for default function: I = Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad. **RESET** functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode. See [Figure 52](#) for the reset pad configuration.

[3] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis (see [Figure 51](#)).

[4] I²C-bus pads compliant with the I²C-bus specification for I²C standard mode and I²C Fast-mode Plus. The pin requires an external pull-up to provide output functionality. When power is switched off, this pin is floating and does not disturb the I²C lines. Open-drain configuration applies to all functions on this pin.

[5] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors, configurable hysteresis, and analog input. When configured as a ADC input, digital section of the pad is disabled and the pin is not 5 V tolerant (see [Figure 51](#)).

[6] When the system oscillator is not used, connect XTALIN and XTALOUT as follows: XTALIN can be left floating or can be grounded (grounding is preferred to reduce susceptibility to noise). XTALOUT should be left floating.