

### Memory

- Up to 8 kB flash
- Flash is in-system programmable in 512-Byte sectors
- Up to 512 Bytes RAM (256 + 256)

### On-Chip Debug

- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (no emulator required)
- Provides breakpoints, single stepping, inspect/modify memory and registers

### 12-Bit Analog-to-Digital Converter

- Up to 16 input channels
- Up to 200 kspS 12-bit mode or 800 kspS 10-bit mode
- Internal VREF or external VREF supported

### Internal Low-Power Oscillator

- Calibrated to 24.5 MHz
- Low supply current
- ±2% accuracy over supply and temperature

### Internal Low-Frequency Oscillator

- 80 kHz nominal operation
- Low supply current
- Independent clock source for watchdog timer

### 2 Analog Comparators

- Programmable hysteresis and response time
- Configurable as interrupt or reset source
- Low current

### General-Purpose I/O

- Up to 18 pins
- 5 V-Tolerant
- Crossbar-enabled

### High-Speed CIP-51 µC Core

- Efficient, pipelined instruction architecture
- Up to 25 MIPS throughput with 25 MHz clock
- Uses standard 8051 instruction set
- Expanded interrupt handler

### Communication Peripherals

- UART
- I<sup>2</sup>C / SMBus™
- SPI™

### Timer/Counters and PWM

- 4 General-Purpose 16-bit Timer/Counters
- 16-bit Programmable Counter Array (PCA) with three channels of PWM, capture/compare, or frequency output capability, and hardware kill/safe state capability

### Additional Support Peripherals

- Independent watchdog timer clocked from LFO
- 16-bit CRC engine

### Unique Identifier

- 32-bit unique key for each device

### Supply Voltage

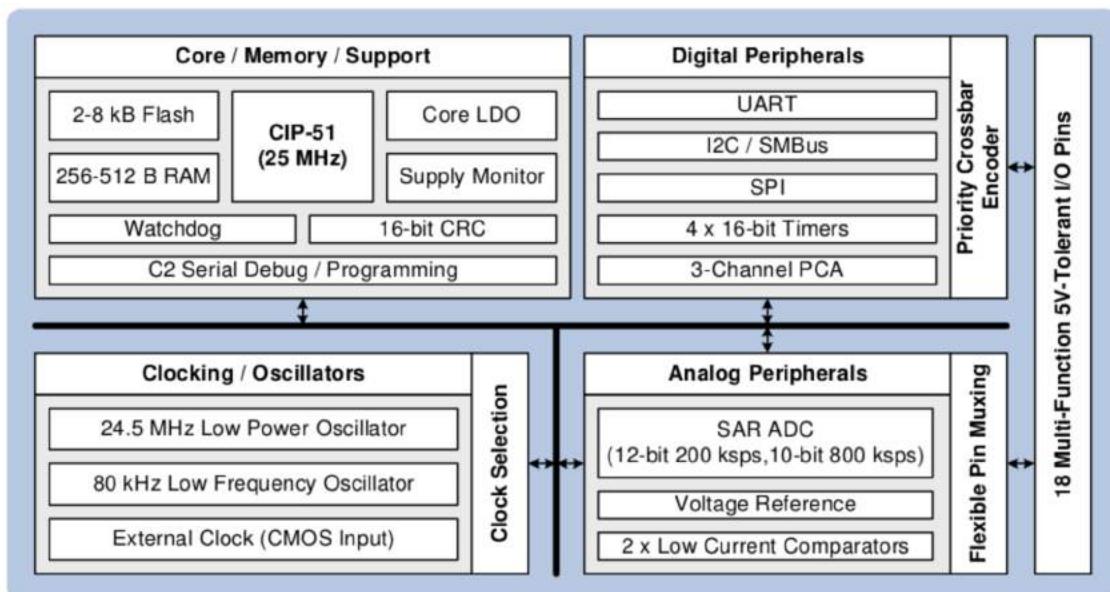
- 2.2 to 3.6 V

### Package Options

- 16-pin SOIC
- 20-pin QFN, 3 x 3 mm
- 24-pin QSOP
- Available in die form
- Qualified to AEC-Q100 Standards

### Temperature Ranges:

- -40 to +125 °C (-Ix) and -40 to +85 °C (-Gx)



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## 1. Electrical Specifications

### 1.1. Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in Table 1.1, unless stated otherwise.

**Table 1.1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V <sub>DD</sub>		2.2	—	3.6	V
System Clock Frequency	f <sub>SYSCLK</sub>		0	—	25	MHz
Operating Ambient Temperature	T <sub>A</sub>	Commercial Grade Devices (-GM, -GS, -GU)	-40	—	85	°C
		Industrial Grade Devices (-IM, -IS, -IU)	-40	—	125	°C

Note: All voltages with respect to GND

**Table 1.2. Power Consumption**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Digital Core Supply Current (–Gx Devices, –40°C to +85°C)</b>						
Normal Mode—Full speed with code executing from flash	I <sub>DD</sub>	F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>	—	4.45	4.85	mA
		F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>	—	915	1150	mA
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup> , T <sub>A</sub> = 25 °C	—	250	290	mA
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>	—	250	380	mA
Idle Mode—Core halted with peripherals running	I <sub>DD</sub>	F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>	—	2.05	2.3	mA
		F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>	—	550	700	mA
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup> , T <sub>A</sub> = 25 °C	—	125	130	mA
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>	—	125	200	mA
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I <sub>DD</sub>	Internal LDO ON, T <sub>A</sub> = 25 °C	—	105	120	mA
		Internal LDO ON	—	105	170	mA
		Internal LDO OFF	—	0.2	—	mA

**Notes:**

- 1. Currents are additive. For example, where I<sub>DD</sub> is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
- 2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
- 3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
- 4. ADC0 always-on power excludes internal reference supply current.
- 5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

**Table 1.2. Power Consumption (Continued)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>Digital Core Supply Current (–Ix Devices, –40°C to +125°C)</b>							
Normal Mode—Full speed with code executing from flash	I <sub>DD</sub>	F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>	—	4.45	5.25	mA	
		F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>	—	915	1600	mA	
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup> , T <sub>A</sub> = 25 °C	—	250	290	mA	
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>	—	250	725	mA	
Idle Mode—Core halted with peripherals running	I <sub>DD</sub>	F <sub>SYSCLK</sub> = 24.5 MHz <sup>2</sup>	—	2.05	2.6	mA	
		F <sub>SYSCLK</sub> = 1.53 MHz <sup>2</sup>	—	550	1000	mA	
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup> , T <sub>A</sub> = 25 °C	—	125	130	mA	
		F <sub>SYSCLK</sub> = 80 kHz <sup>3</sup>	—	125	550	mA	
Stop Mode—Core halted and all clocks stopped, Supply monitor off.	I <sub>DD</sub>	Internal LDO ON, T <sub>A</sub> = 25 °C	—	105	120	mA	
		Internal LDO ON	—	105	270	mA	
		Internal LDO OFF	—	0.2	—	mA	
<b>Analog Peripheral Supply Currents (Both –Gx and –Ix Devices)</b>							
High-Frequency Oscillator	I <sub>HFOSC</sub>	Operating at 24.5 MHz, T <sub>A</sub> = 25 °C	—	155	—	μA	
Low-Frequency Oscillator	I <sub>LFOSC</sub>	Operating at 80 kHz, T <sub>A</sub> = 25 °C	—	3.5	—	μA	
ADC0 Always-on <sup>4</sup>	I <sub>ADC</sub>	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings V <sub>DD</sub> = 3.0 V	—	845	1200	μA	
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings V <sub>DD</sub> = 3.0 V	—	425	580	μA	
ADC0 Burst Mode, 10-bit single conversions, external reference	I <sub>ADC</sub>	200 ksps, V <sub>DD</sub> = 3.0 V	—	370	—	μA	
		100 ksps, V <sub>DD</sub> = 3.0 V	—	185	—	μA	
		10 ksps, V <sub>DD</sub> = 3.0 V	—	19	—	μA	
<b>Notes:</b>							
<ol style="list-style-type: none"> <li>1. Currents are additive. For example, where I<sub>DD</sub> is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.</li> <li>2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.</li> <li>3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.</li> <li>4. ADC0 always-on power excludes internal reference supply current.</li> <li>5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.</li> </ol>							

**Table 1.2. Power Consumption (Continued)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I <sub>ADC</sub>	200 ksps, V <sub>DD</sub> = 3.0 V	—	490	—	µA
		100 ksps, V <sub>DD</sub> = 3.0 V	—	245	—	µA
		10 ksps, V <sub>DD</sub> = 3.0 V	—	23	—	µA
ADC0 Burst Mode, 12-bit single conversions, external reference	I <sub>ADC</sub>	100 ksps, V <sub>DD</sub> = 3.0 V	—	530	—	µA
		50 ksps, V <sub>DD</sub> = 3.0 V	—	265	—	µA
		10 ksps, V <sub>DD</sub> = 3.0 V	—	53	—	µA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I <sub>ADC</sub>	100 ksps, V <sub>DD</sub> = 3.0 V, Normal bias	—	950	—	µA
		50 ksps, V <sub>DD</sub> = 3.0 V, Low power bias	—	420	—	µA
		10 ksps, V <sub>DD</sub> = 3.0 V, Low power bias	—	85	—	µA
Internal ADC0 Reference, Always-on <sup>5</sup>	I <sub>REF</sub>	Normal Power Mode	—	680	790	µA
		Low Power Mode	—	160	210	µA
Temperature Sensor	I <sub>TSENSE</sub>		—	75	120	µA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I <sub>CMP</sub>	CPnMD = 11	—	0.5	—	µA
		CPnMD = 10	—	3	—	µA
		CPnMD = 01	—	10	—	µA
		CPnMD = 00	—	25	—	µA
Voltage Supply Monitor (VMON0)	I <sub>VMON</sub>		—	15	20	µA

**Notes:**

1. Currents are additive. For example, where I<sub>DD</sub> is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount.
2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator.
3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator.
4. ADC0 always-on power excludes internal reference supply current.
5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.

**Table 1.3. Reset and Supply Monitor**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V <sub>DD</sub> Supply Monitor Threshold	V <sub>VDDM</sub>		1.85	1.95	2.1	V
Power-On Reset (POR) Threshold	V <sub>POR</sub>	Rising Voltage on V <sub>DD</sub>	—	1.4	—	V
		Falling Voltage on V <sub>DD</sub>	0.75	—	1.36	V
V <sub>DD</sub> Ramp Time	t <sub>RMP</sub>	Time to V <sub>DD</sub> ≥ 2.2 V	10	—	—	μs
Reset Delay from POR	t <sub>POR</sub>	Relative to V <sub>DD</sub> ≥ V <sub>POR</sub>	3	10	31	ms
Reset Delay from non-POR source	t <sub>RST</sub>	Time between release of reset source and code execution	—	39	—	μs
RST Low Time to Generate Reset	t <sub>RSTL</sub>		15	—	—	μs
Missing Clock Detector Response Time (final rising edge to reset)	t <sub>MCD</sub>	F <sub>SYSCLK</sub> > 1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F <sub>MCD</sub>		—	7.5	13.5	kHz
V <sub>DD</sub> Supply Monitor Turn-On Time	t <sub>MON</sub>		—	2	—	μs

**Table 1.4. Flash Memory**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time <sup>1,2</sup>	t <sub>WRITE</sub>	One Byte, F <sub>SYSCLK</sub> = 24.5 MHz	19	20	21	μs
Erase Time <sup>1,2</sup>	t <sub>ERASE</sub>	One Page, F <sub>SYSCLK</sub> = 24.5 MHz	5.2	5.35	5.5	ms
V <sub>DD</sub> Voltage During Programming <sup>3</sup>	V <sub>PROG</sub>		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N <sub>WE</sub>		20k	100k	—	Cycles

**Notes:**

- 1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
- 2. The internal High-Frequency Oscillator has a programmable output frequency using the OSCICL register, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the OSCICL register back to its reset value when writing or erasing flash.
- 3. Flash can be safely programmed at any voltage above the supply monitor threshold (V<sub>VDDM</sub>).
- 4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

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**Table 1.5. Internal Oscillators**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>High Frequency Oscillator (24.5 MHz)</b>						
Oscillator Frequency	$f_{HFOSC}$	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	$PSS_{HFOSC}$	$T_A = 25^\circ C$	—	0.5	—	%/V
Temperature Sensitivity	$TS_{HFOSC}$	$V_{DD} = 3.0 V$	—	40	—	ppm/ $^\circ C$
<b>Low Frequency Oscillator (80 kHz)</b>						
Oscillator Frequency	$f_{LFOSC}$	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	$PSS_{LFOSC}$	$T_A = 25^\circ C$	—	0.05	—	%/V
Temperature Sensitivity	$TS_{LFOSC}$	$V_{DD} = 3.0 V$	—	65	—	ppm/ $^\circ C$

**Table 1.6. External Clock Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	$f_{CMOS}$		0	—	25	MHz
External Input CMOS Clock High Time	$t_{CMOSH}$		18	—	—	ns
External Input CMOS Clock Low Time	$t_{CMOSL}$		18	—	—	ns

**Table 1.7. ADC**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N <sub>bits</sub>	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f <sub>S</sub>	12 Bit Mode	—	—	200	kspS
		10 Bit Mode	—	—	800	kspS
Throughput Rate (Low Power Mode)	f <sub>S</sub>	12 Bit Mode	—	—	62.5	kspS
		10 Bit Mode	—	—	250	kspS
Tracking Time	t <sub>TRK</sub>	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t <sub>PWR</sub>		1.2	—	—	μs
SAR Clock Frequency	f <sub>SAR</sub>	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t <sub>CNV</sub>	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.	1.1			μs
Sample/Hold Capacitor	C <sub>SAR</sub>	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C <sub>IN</sub>		—	20	—	pF
Input Mux Impedance	R <sub>MUX</sub>		—	550	—	Ω
Voltage Reference Range	V <sub>REF</sub>		1	—	V <sub>DD</sub>	V
Input Voltage Range*	V <sub>IN</sub>	Gain = 1	0	—	V <sub>REF</sub>	V
		Gain = 0.5	0	—	2xV <sub>REF</sub>	V
Power Supply Rejection Ratio	PSRR <sub>ADC</sub>		—	70	—	dB
<b>DC Performance</b>						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	-1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB

\*Note: Absolute input pin voltage is limited by the V<sub>DD</sub> supply.

**Table 1.7. ADC (Continued)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset Error	$E_{OFF}$	12 Bit Mode, VREF = 1.65 V	-3	0	3	LSB
		10 Bit Mode, VREF = 1.65 V	-2	0	2	LSB
Offset Temperature Coefficient	$T_{COFF}$		—	0.004	—	LSB/°C
Slope Error	$E_M$	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
<b>Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin</b>						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	71	—	dB
		10 Bit Mode	—	70	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	-79	—	dB
		10 Bit Mode	—	-74	—	dB

\*Note: Absolute input pin voltage is limited by the  $V_{DD}$  supply.

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**Table 1.8. Voltage Reference**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Internal Fast Settling Reference</b>						
Output Voltage (Full Temperature and Supply Range)	$V_{REFFS}$	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, $V_{DD} \geq 2.6$ V	2.35	2.4	2.45	V
Temperature Coefficient	$TC_{REFFS}$		—	50	—	ppm/ $^{\circ}$ C
Turn-on Time	$t_{REFFS}$		—	—	1.5	$\mu$ s
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
<b>External Reference</b>						
Input Current	$I_{EXTREF}$	Sample Rate = 800 ksps; $V_{REF} = 3.0$ V	—	5	—	$\mu$ A

**Table 1.9. Temperature Sensor**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	$V_{OFF}$	$T_A = 0$ $^{\circ}$ C	—	757	—	mV
Offset Error*	$E_{OFF}$	$T_A = 0$ $^{\circ}$ C	—	17	—	mV
Slope	M		—	2.85	—	mV/ $^{\circ}$ C
Slope Error*	$E_M$		—	70	—	$\mu$ V/ $^{\circ}$ C
Linearity			—	0.5	—	$^{\circ}$ C
Turn-on Time			—	1.8	—	$\mu$ s

\*Note: Represents one standard deviation from the mean.

**Table 1.10. Comparators**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPnMD = 00 (Highest Speed)	$t_{RESP0}$	+100 mV Differential	—	100	—	ns
		-100 mV Differential	—	150	—	ns
Response Time, CPnMD = 11 (Lowest Power)	$t_{RESP3}$	+100 mV Differential	—	1.5	—	$\mu$ s
		-100 mV Differential	—	3.5	—	$\mu$ s
Positive Hysteresis Mode 0 (CPnMD = 00)	$HYS_{CP+}$	CPnHYP = 00	—	0.4	—	mV
		CPnHYP = 01	—	8	—	mV
		CPnHYP = 10	—	16	—	mV
		CPnHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPnMD = 00)	$HYS_{CP-}$	CPnHYN = 00	—	-0.4	—	mV
		CPnHYN = 01	—	-8	—	mV
		CPnHYN = 10	—	-16	—	mV
		CPnHYN = 11	—	-32	—	mV
Positive Hysteresis Mode 1 (CPnMD = 01)	$HYS_{CP+}$	CPnHYP = 00	—	0.5	—	mV
		CPnHYP = 01	—	6	—	mV
		CPnHYP = 10	—	12	—	mV
		CPnHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPnMD = 01)	$HYS_{CP-}$	CPnHYN = 00	—	-0.5	—	mV
		CPnHYN = 01	—	-6	—	mV
		CPnHYN = 10	—	-12	—	mV
		CPnHYN = 11	—	-24	—	mV
Positive Hysteresis Mode 2 (CPnMD = 10)	$HYS_{CP+}$	CPnHYP = 00	—	0.7	—	mV
		CPnHYP = 01	—	4.5	—	mV
		CPnHYP = 10	—	9	—	mV
		CPnHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPnMD = 10)	$HYS_{CP-}$	CPnHYN = 00	—	-0.6	—	mV
		CPnHYN = 01	—	-4.5	—	mV
		CPnHYN = 10	—	-9	—	mV
		CPnHYN = 11	—	-18	—	mV

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**Table 1.10. Comparators**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Positive Hysteresis Mode 3 (CPnMD = 11)	HYS <sub>CP+</sub>	CPnHYP = 00	—	1.5	—	mV
		CPnHYP = 01	—	4	—	mV
		CPnHYP = 10	—	8	—	mV
		CPnHYP = 11	—	16	—	mV
Negative Hysteresis Mode 3 (CPnMD = 11)	HYS <sub>CP-</sub>	CPnHYN = 00	—	-1.5	—	mV
		CPnHYN = 01	—	-4	—	mV
		CPnHYN = 10	—	-8	—	mV
		CPnHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V <sub>IN</sub>		-0.25	—	V <sub>DD</sub> +0.25	V
Input Pin Capacitance	C <sub>CP</sub>		—	7.5	—	pF
Common-Mode Rejection Ratio	CMRR <sub>CP</sub>		—	70	—	dB
Power Supply Rejection Ratio	PSRR <sub>CP</sub>		—	72	—	dB
Input Offset Voltage	V <sub>OFF</sub>	T <sub>A</sub> = 25 °C	-10	0	10	mV
Input Offset Tempco	TC <sub>OFF</sub>		—	3.5	—	µV/°C

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**Table 1.11. Port I/O**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (High Drive)	$V_{OH}$	$I_{OH} = -3 \text{ mA}$	$V_{DD} - 0.7$	—	—	V
Output Low Voltage (High Drive)	$V_{OL}$	$I_{OL} = 8.5 \text{ mA}$	—	—	0.6	V
Output High Voltage (Low Drive)	$V_{OH}$	$I_{OH} = -1 \text{ mA}$	$V_{DD} - 0.7$	—	—	V
Output Low Voltage (Low Drive)	$V_{OL}$	$I_{OL} = 1.4 \text{ mA}$	—	—	0.6	V
Input High Voltage	$V_{IH}$		$V_{DD} - 0.6$	—	—	V
Input Low Voltage	$V_{IL}$		—	—	0.6	V
Pin Capacitance	$C_{IO}$		—	7	—	pF
Weak Pull-Up Current ( $V_{IN} = 0 \text{ V}$ )	$I_{PU}$	$V_{DD} = 3.6$	-30	-20	-10	$\mu\text{A}$
Input Leakage (Pullups off or Analog)	$I_{LK}$	$GND \leq V_{IN} \leq V_{DD}$	-1.1	—	1.1	$\mu\text{A}$
Input Leakage Current with $V_{IN}$ above $V_{DD}$	$I_{LK}$	$V_{DD} < V_{IN} < V_{DD} + 2.0 \text{ V}$	0	5	150	$\mu\text{A}$

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## 1.2. Typical Performance Curves

### 1.2.1. Operating Supply Current

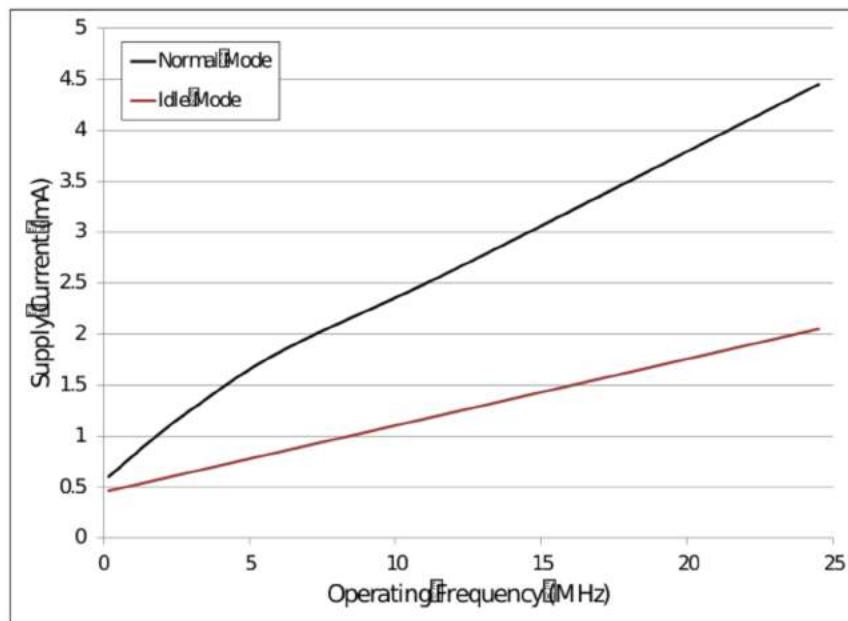


Figure 1.1. Typical Operating Current Running From 24.5 MHz Internal Oscillator

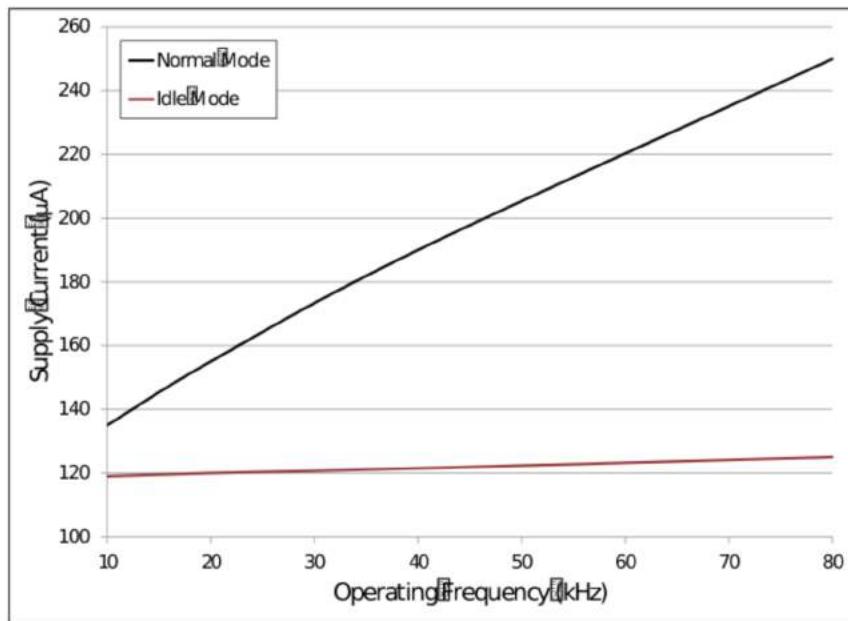


Figure 1.2. Typical Operating Current Running From 80 kHz Internal Oscillator

### 1.2.2. ADC Supply Current

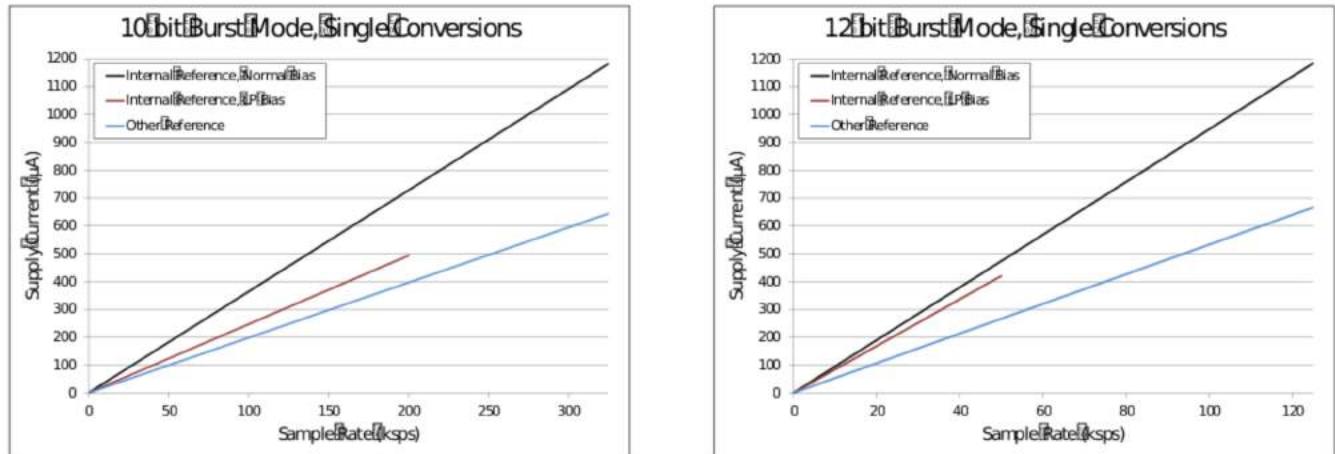


Figure 1.3. Typical ADC and Internal Reference Power Consumption in Burst Mode

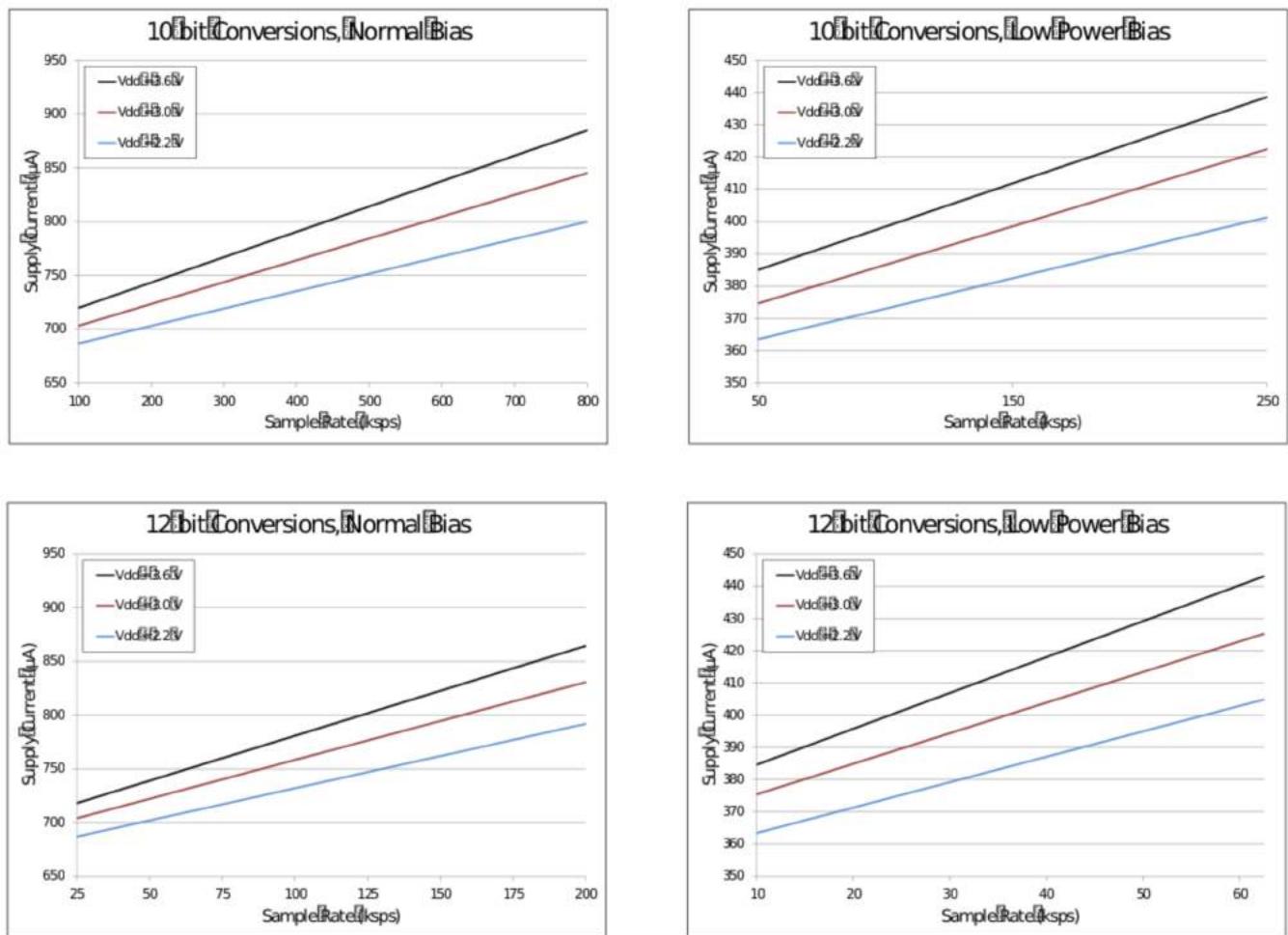


Figure 1.4. Typical ADC Power Consumption in Normal (Always-On) Mode

### 1.2.3. Port I/O Output Drive

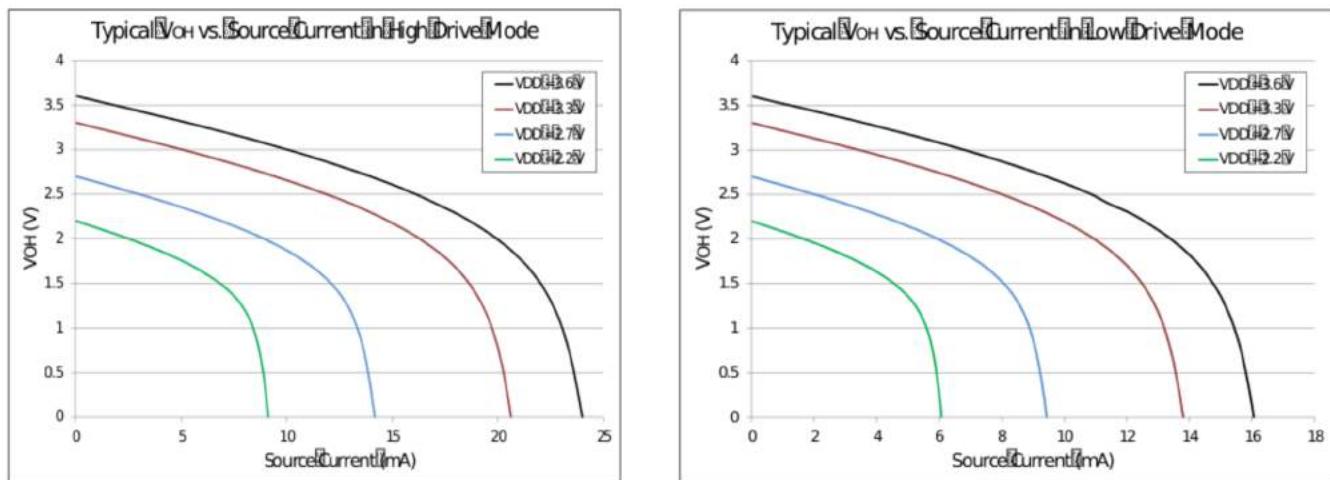


Figure 1.5. Typical  $V_{OH}$  vs. Source Current

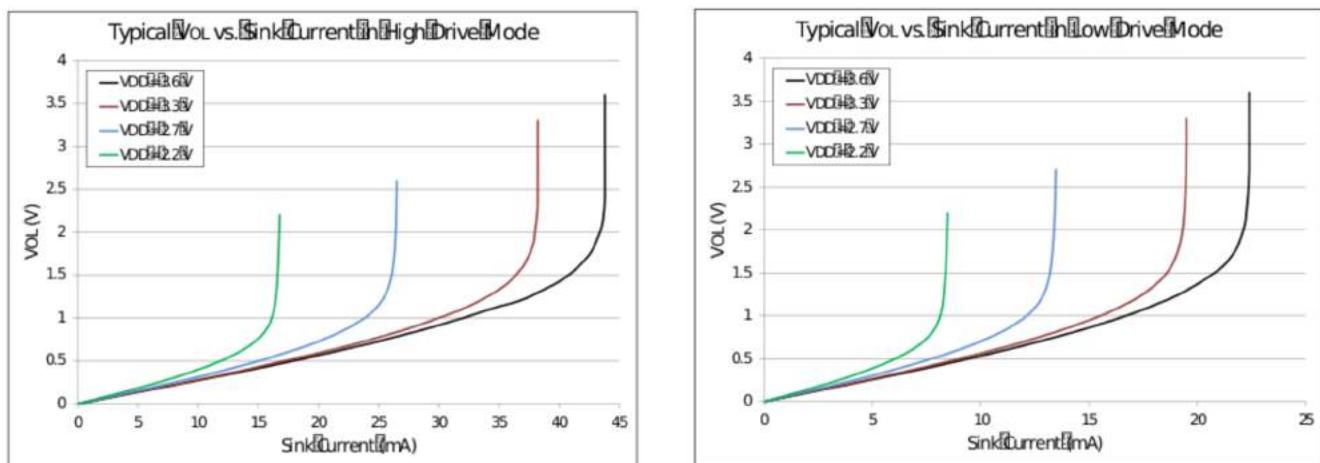


Figure 1.6. Typical  $V_{OL}$  vs. Sink Current

### 1.3. Thermal Conditions

Table 1.12. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance*	$\Theta_{JA}$	SOIC-16 Packages	—	70	—	$^{\circ}\text{C/W}$
		QFN-20 Packages	—	60	—	$^{\circ}\text{C/W}$
		QSOP-24 Packages	—	65	—	$^{\circ}\text{C/W}$

\*Note: Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

#### 1.4. Absolute Maximum Ratings

Stresses above those listed under Table 1.13 may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

**Table 1.13. Absolute Maximum Ratings**

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	$T_{BIAS}$		-55	125	°C
Storage Temperature	$T_{STG}$		-65	150	°C
Voltage on $V_{DD}$	$V_{DD}$		GND-0.3	4.2	V
Voltage on I/O pins or $\overline{RST}$	$V_{IN}$	$V_{DD} \geq 3.3\text{ V}$	GND-0.3	5.8	V
		$V_{DD} < 3.3\text{ V}$	GND-0.3	$V_{DD}+2.5$	V
Total Current Sunk into Supply Pin	$I_{VDD}$		—	400	mA
Total Current Sourced out of Ground Pin	$I_{GND}$		400	—	mA
Current Sourced or Sunk by Any I/O Pin or $\overline{RST}$	$I_{PIO}$		-100	100	mA
Operating Junction Temperature	$T_J$	Commercial Grade Devices (-GM, -GS, -GU)	-40	105	°C
		Industrial Grade Devices (-IM, -IS, -IU)	-40	125	°C
Note: Exposure to maximum rating conditions for extended periods may affect device reliability.					

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## 2. System Overview

The C8051F85x/86x device family are fully integrated, mixed-signal system-on-a-chip MCUs. Highlighted features are listed below. Refer to Table 4.1 for specific product feature selection and part ordering numbers.

■ **Core:**

- Pipelined CIP-51 Core
- Fully compatible with standard 8051 instruction set
- 70% of instructions execute in 1-2 clock cycles
- 25 MHz maximum operating frequency

■ **Memory:**

- 2-8 kB flash; in-system programmable in 512-byte sectors
- 512 bytes RAM (including 256 bytes standard 8051 RAM and 256 bytes on-chip XRAM)

■ **Power:**

- Internal low drop-out (LDO) regulator for CPU core voltage
- Power-on reset circuit and brownout detectors

■ **I/O: Up to 18 total multifunction I/O pins:**

- All pins 5 V tolerant under bias
- Flexible peripheral crossbar for peripheral routing
- 5 mA source, 12.5 mA sink allows direct drive of LEDs

■ **Clock Sources:**

- Low-power internal oscillator: 24.5 MHz  $\pm 2\%$
- Low-frequency internal oscillator: 80 kHz
- External CMOS clock option

■ **Timers/Counters and PWM:**

- 3-channel Programmable Counter Array (PCA) supporting PWM, capture/compare and frequency output modes
- 4x 16-bit general-purpose timers
- Independent watchdog timer, clocked from low frequency oscillator

■ **Communications and Other Digital Peripherals:**

- UART
- SPI™
- I<sup>2</sup>C / SMBus™
- 16-bit CRC Unit, supporting automatic CRC of flash at 256-byte boundaries

■ **Analog:**

- 12-Bit Analog-to-Digital Converter (ADC)
- 2 x Low-Current Comparators

■ **On-Chip Debugging**

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the C8051F85x/86x devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware.

The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging.

Each device is specified for 2.2 to 3.6 V operation, and are available in 20-pin QFN, 16-pin SOIC or 24-pin QSOP packages. All package options are lead-free and RoHS compliant. The device is available in two temperature grades: -40 to +85 °C or -40 to +125 °C. See Table 4.1 for ordering information. A block diagram is included in Figure 2.1.

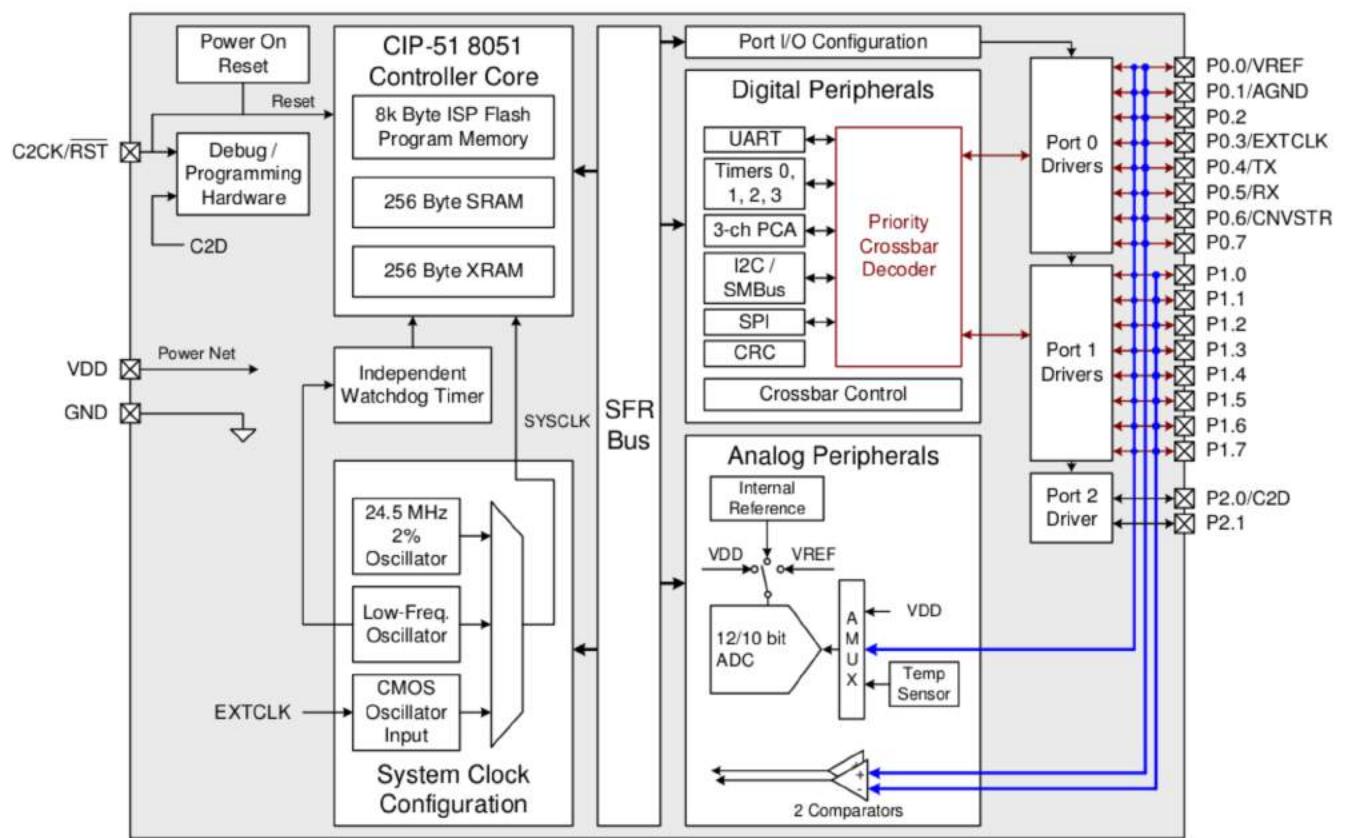


Figure 2.1. C8051F85x/86x Family Block Diagram (QSOP-24 Shown)

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## 2.1. Power

### 2.1.1. LDO

The C8051F85x/86x devices include an internal regulator to regulate the supply voltage down the core operating voltage of 1.8 V. This LDO consumes little power, but can be shut down in the power-saving Stop mode.

### 2.1.2. Voltage Supply Monitor (VMON0)

The C8051F85x/86x devices include a voltage supply monitor which allows devices to function in known, safe operating condition without the need for external hardware.

The supply monitor module includes the following features:

- Holds the device in reset if the main VDD supply drops below the VDD Reset threshold.

### 2.1.3. Device Power Modes

The C8051F85x/86x devices feature three low power modes in addition to normal operating mode, allowing the designer to save power when the core is not in use. All power modes are detailed in Table 2.1.

**Table 2.1. C8051F85x/86x Power Modes**

Mode	Description	Mode Entrance	Mode Exit
Normal	Core and peripherals operating at full speed		
Idle	<ul style="list-style-type: none"><li>■ Core halted</li><li>■ Peripherals operate at full speed</li></ul>	Set IDLE bit in PCON	Any enabled interrupt or reset source
Stop	<ul style="list-style-type: none"><li>■ All clocks stopped</li><li>■ Core LDO and (optionally) comparators still running</li><li>■ Pins retain state</li></ul>	Clear STOPCF in REG0MD and Set STOP bit in PCON	Device reset
Shutdown	<ul style="list-style-type: none"><li>■ All clocks stopped</li><li>■ Core LDO and all analog circuits shut down</li><li>■ Pins retain state</li></ul>	Set STOPCF in REG0MD and Set STOP bit in PCON	Device reset

In addition, the user may choose to lower the clock speed in Normal and Idle modes to save power when the CPU requirements allow for lower speed.

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### **2.1.3.1. Normal Mode**

Normal mode encompasses the typical full-speed operation. The power consumption of the device in this mode will vary depending on the system clock speed and any analog peripherals that are enabled.

### **2.1.3.2. Idle Mode**

Setting the IDLE bit in PCON causes the hardware to halt the CPU and enter idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the IDLE bit to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

### **2.1.3.3. Stop Mode (Regulator On)**

Setting the STOP bit in PCON when STOPCF in REG0CN is clear causes the controller core to enter stop mode as soon as the instruction that sets the bit completes execution. In stop mode the internal oscillator, CPU, and all digital peripherals are stopped. Each analog peripheral may be shut down individually prior to entering stop mode. Stop mode can only be terminated by an internal or external reset.

### **2.1.3.4. Shutdown Mode (Regulator Off)**

Shutdown mode is an extension of the normal stop mode operation. Setting the STOP bit in PCON when STOPCF in REG0CN is also set causes the controller core to enter shutdown mode as soon as the instruction that sets the bit completes execution, and then the internal regulator is powered down. In shutdown mode, all core functions, memories and peripherals are powered off. An external pin reset or power-on reset is required to exit shutdown mode.

## **2.2. I/O**

### **2.2.1. General Features**

The C8051F85x/86x ports have the following features:

- Push-pull or open-drain output modes and analog or digital modes.
- Port Match allows the device to recognize a change on a port pin value and wake from idle mode or generate an interrupt.
- Internal pull-up resistors can be globally enabled or disabled.
- Two external interrupts provide unique interrupt vectors for monitoring time-critical events.
- Above-rail tolerance allows 5 V interface when device is powered.

### **2.2.2. Crossbar**

The C8051F85x/86x devices have a digital peripheral crossbar with the following features:

- Flexible peripheral assignment to port pins.
- Pins can be individually skipped to move peripherals as needed for design or layout considerations.

The crossbar has a fixed priority for each I/O function and assigns these functions to the port pins. When a digital resource is selected, the least-significant unassigned port pin is assigned to that resource. If a port pin is assigned, the crossbar skips that pin when assigning the next selected resource. Additionally, the crossbar will skip port pins whose associated bits in the PnSKIP registers are set. This provides some flexibility when designing a system: pins involved with sensitive analog measurements can be moved away from digital I/O and peripherals can be moved around the chip as needed to ease layout constraints.

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## 2.3. Clocking

The C8051F85x/86x devices have two internal oscillators and the option to use an external CMOS input at a pin as the system clock. A programmable divider allows the user to internally run the system clock at a slower rate than the selected oscillator if desired.

## 2.4. Counters/Timers and PWM

### 2.4.1. Programmable Counter Array (PCA0)

The C8051F85x/86x devices include a three-channel, 16-bit Programmable Counter Array with the following features:

- 16-bit time base.
- Programmable clock divisor and clock source selection.
- Three independently-configurable channels.
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation).
- Output polarity control.
- Frequency output mode.
- Capture on rising, falling or any edge.
- Compare function for arbitrary waveform generation.
- Software timer (internal compare) mode.
- Can accept hardware "kill" signal from comparator 0.

### 2.4.2. Timers (Timer 0, Timer 1, Timer 2 and Timer 3)

Timers include the following features:

- Timer 0 and Timer 1 are standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Timer 2 and Timer 3 can each operate as 16-bit auto-reload or two independent 8-bit auto-reload timers, and include pin or LFO clock capture capabilities.

### 2.4.3. Watchdog Timer (WDT0)

The watchdog timer includes a 16-bit timer with a programmable reset period. The registers are protected from inadvertent access by an independent lock and key interface.

The Watchdog Timer has the following features:

- Programmable timeout interval.
- Runs from the low frequency oscillator.
- Lock-out feature to prevent any modification until a system reset.

---

## 2.5. Communications and other Digital Peripherals

### 2.5.1. Universal Asynchronous Receiver/Transmitter (UART0)

The UART uses two signals (TX and RX) and a predetermined fixed baud rate to provide asynchronous communications with other devices.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to SYSCLK / 2 (transmit) or SYSCLK / 8 (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.

### 2.5.2. Serial Peripheral Interface (SPI0)

SPI is a 3- or 4-wire communication interface that includes a clock, input data, output data, and an optional select signal.

The SPI module includes the following features:

- Supports 3- or 4-wire master or slave modes.
- Supports external clock frequencies up to SYSCLK / 2 in master mode and SYSCLK / 10 in slave mode.
- Support for all clock phase and polarity modes.
- 8-bit programmable clock rate.
- Support for multiple masters on the same data lines.

### 2.5.3. System Management Bus / I2C (SMBus0)

The SMBus interface is a two-wire, bi-directional serial bus compatible with both I2C and SMBus protocols. The two clock and data signals operate in open-drain mode with external pull-ups to support automatic bus arbitration.

Reads and writes to the interface are byte-oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/8th of the system clock as a master or slave, which can be faster than allowed by the SMBus / I2C specification, depending on the clock source used. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus interface may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and start/stop control and generation.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

### 2.5.4. 16/32-bit CRC (CRC0)

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for four CCITT-16 polynomial.

- 
- Byte-level bit reversal.
  - Automatic CRC of flash contents on one or more 256-byte blocks.
  - Initial seed selection of 0x0000 or 0xFFFF.

---

## 2.6. Analog Peripherals

### 2.6.1. 12-Bit Analog-to-Digital Converter (ADC0)

The ADC0 module on C8051F85x/86x devices is a Successive Approximation Register (SAR) Analog to Digital Converter (ADC). The key features of the ADC module are:

- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksp/s samples per second in 12-bit mode or 800 ksp/s samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Selectable asynchronous hardware conversion trigger.
- Output data window comparator allows automatic range checking.
- Support for Burst Mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.

### 2.6.2. Low Current Comparators (CMP0, CMP1)

The comparators take two analog input voltages and output the relationship between these voltages (less than or greater than) as a digital signal. The Low Power Comparator module includes the following features:

- Multiple sources for the positive and negative poles, including VDD, VREF, and I/O pins.
- Two outputs are available: a digital synchronous latched output and a digital asynchronous raw output.
- Programmable hysteresis and response time.
- Falling or rising edge interrupt options on the comparator output.
- Provide “kill” signal to PCA module.
- Comparator 0 can be used to reset the device.

---

## 2.7. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost.

The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For VDD Supply Monitor and power-on resets, the RST pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal low-power oscillator. The Watchdog Timer is enabled with the Low Frequency Oscillator (LFO0) as its clock source. Program execution begins at location 0x0000.

## 2.8. On-Chip Debugging

The C8051F85x/86x devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

### 3. Pin Definitions

#### 3.1. C8051F850/1/2/3/4/5 QSOP24 Pin Definitions

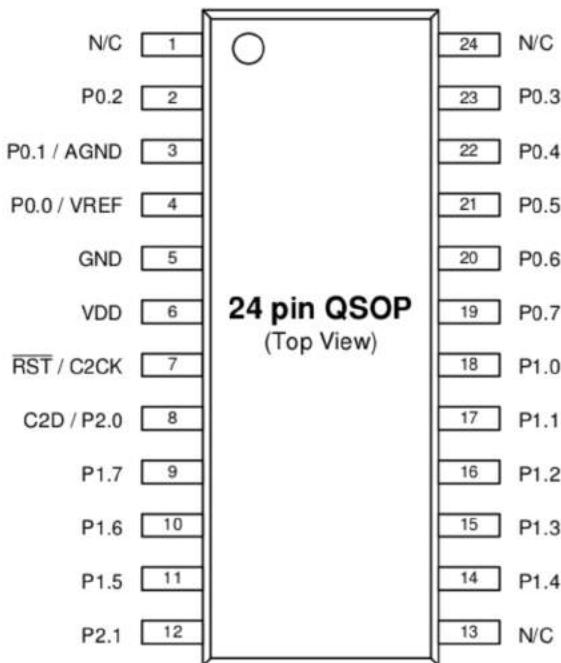


Figure 3.1. C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU Pinout

Table 3.1. Pin Definitions for C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	5			
VDD	Power	6			
RST / C2CK	Active-low Reset / C2 Debug Clock	7			

---

**Table 3.1. Pin Definitions for C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU**

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P0.0	Standard I/O	4	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0 VREF
P0.1	Standard I/O	3	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1 AGND
P0.2	Standard I/O	2	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
P0.3 / EXTCLK	Standard I/O / External CMOS Clock Input	23	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
P0.4	Standard I/O	22	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CP0P.4 CP0N.4
P0.5	Standard I/O	21	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CP0P.5 CP0N.5
P0.6	Standard I/O	20	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP0P.6 CP0N.6
P0.7	Standard I/O	19	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CP0P.7 CP0N.7

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**Table 3.1. Pin Definitions for C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU**

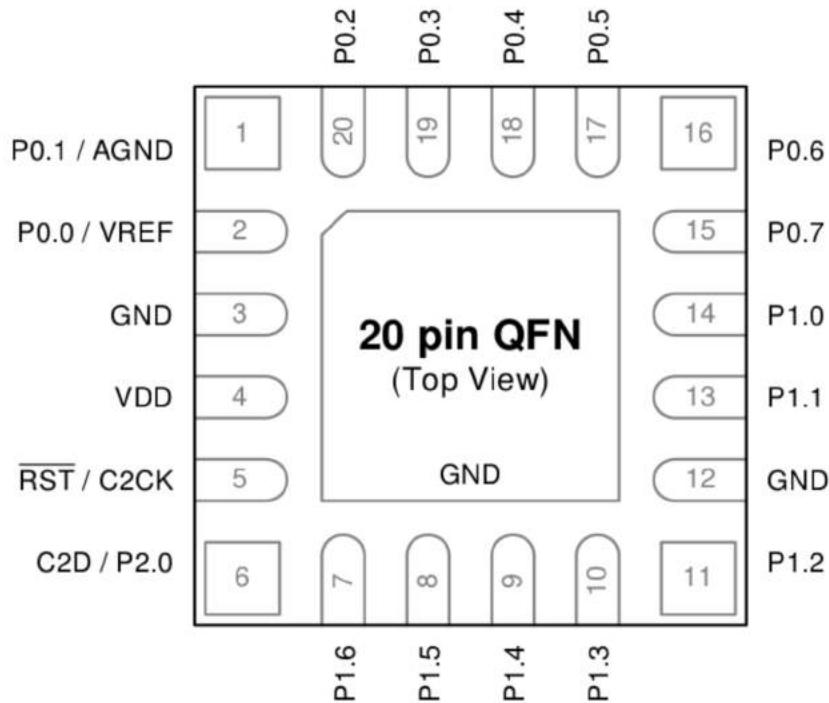
Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P1.0	Standard I/O	18	Yes	P1MAT.0	ADC0.8 CP1P.0 CP1N.0
P1.1	Standard I/O	17	Yes	P1MAT.1	ADC0.9 CP1P.1 CP1N.1
P1.2	Standard I/O	16	Yes	P1MAT.2	ADC0.10 CP1P.2 CP1N.2
P1.3	Standard I/O	15	Yes	P1MAT.3	ADC0.11 CP1P.3 CP1N.3
P1.4	Standard I/O	14	Yes	P1MAT.4	ADC0.12 CP1P.4 CP1N.4
P1.5	Standard I/O	11	Yes	P1MAT.5	ADC0.13 CP1P.5 CP1N.5
P1.6	Standard I/O	10	Yes	P1MAT.6	ADC0.14 CP1P.6 CP1N.6
P1.7	Standard I/O	9	Yes	P1MAT.7	ADC0.15 CP1P.7 CP1N.7
P2.0 / C2D	Standard I/O / C2 Debug Data	8			
P2.1	Standard I/O	12			

---

**Table 3.1. Pin Definitions for C8051F850/1/2/3/4/5-GU and C8051F850/1/2/3/4/5-IU**

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
N/C	No Connection	1 13 24			

### 3.2. C8051F850/1/2/3/4/5 QFN20 Pin Definitions



**Figure 3.2. C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM Pinout**

**Table 3.2. Pin Definitions for C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM**

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	Center 3 12			
VDD	Power	4			
$\overline{\text{RST}} / \text{C2CK}$	Active-low Reset / C2 Debug Clock	5			

---

**Table 3.2. Pin Definitions for C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM**

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P0.0	Standard I/O	2	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0 VREF
P0.1	Standard I/O	1	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1 AGND
P0.2	Standard I/O	20	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
P0.3	Standard I/O	19	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
P0.4	Standard I/O	18	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CP0P.4 CP0N.4
P0.5	Standard I/O	17	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CP0P.5 CP0N.5
P0.6	Standard I/O	16	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP0P.6 CP0N.6
P0.7	Standard I/O	15	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CP0P.7 CP0N.7

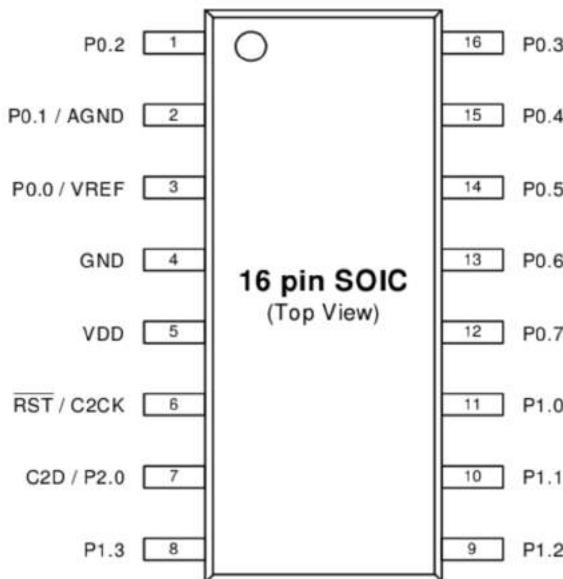
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**Table 3.2. Pin Definitions for C8051F850/1/2/3/4/5-GM and C8051F850/1/2/3/4/5-IM**

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P1.0	Standard I/O	14	Yes	P1MAT.0	ADC0.8 CP1P.0 CP1N.0
P1.1	Standard I/O	13	Yes	P1MAT.1	ADC0.9 CP1P.1 CP1N.1
P1.2	Standard I/O	11	Yes	P1MAT.2	ADC0.10 CP1P.2 CP1N.2
P1.3	Standard I/O	10	Yes	P1MAT.3	ADC0.11 CP1P.3 CP1N.3
P1.4	Standard I/O	9	Yes	P1MAT.4	ADC0.12 CP1P.4 CP1N.4
P1.5	Standard I/O	8	Yes	P1MAT.5	ADC0.13 CP1P.5 CP1N.5
P1.6	Standard I/O	7	Yes	P1MAT.6	ADC0.14 CP1P.6 CP1N.6
P2.0 / C2D	Standard I/O / C2 Debug Data	6			

### 3.3. C8051F860/1/2/3/4/5 SOIC16 Pin Definitions



**Figure 3.3. C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS Pinout**

**Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS**

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
GND	Ground	4			
VDD	Power	5			
RST / C2CK	Active-low Reset / C2 Debug Clock	6			
P0.0	Standard I/O	3	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CP0P.0 CP0N.0

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**Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS**

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P0.1	Standard I/O	2	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CP0P.1 CP0N.1
P0.2	Standard I/O	1	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CP0P.2 CP0N.2
P0.3 / EXTCLK	Standard I/O / External CMOS Clock Input	16	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CP0P.3 CP0N.3
P0.4	Standard I/O	15	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CP0P.4 CP0N.4
P0.5	Standard I/O	14	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CP0P.5 CP0N.5
P0.6	Standard I/O	13	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CP1P.0 CP1N.0
P0.7	Standard I/O	12	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CP1P.1 CP1N.1
P1.0	Standard I/O	11	Yes	P1MAT.0	ADC0.8 CP1P.2 CP1N.2

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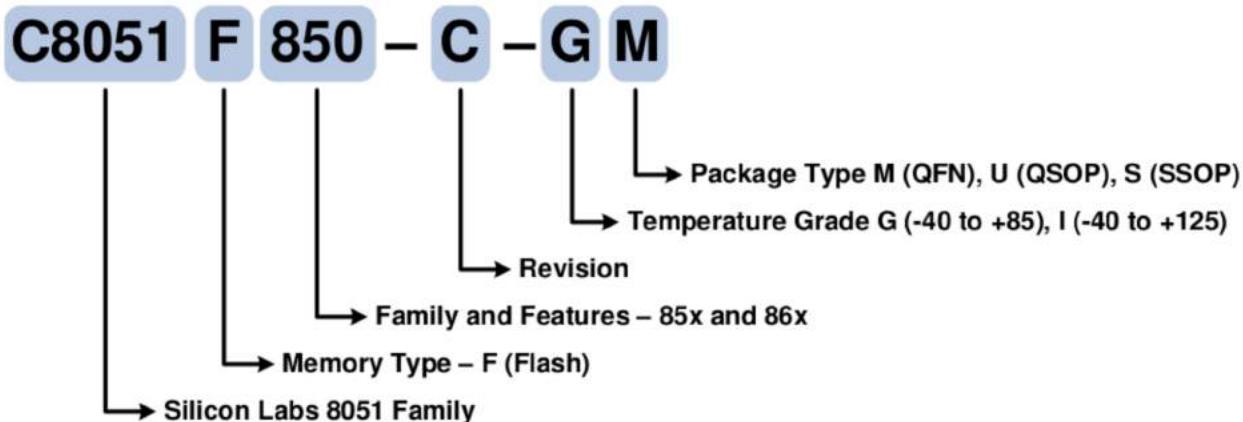
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**Table 3.3. Pin Definitions for C8051F860/1/2/3/4/5-GS and C8051F860/1/2/3/4/5-IS**

Pin Name	Type	Pin Numbers	Crossbar Capability	Additional Digital Functions	Analog Functions
P1.1	Standard I/O	10	Yes	P1MAT.1	ADC0.9 CP1P.3 CP1N.3
P1.2	Standard I/O	9	Yes	P1MAT.2	ADC0.10 CP1P.4 CP1N.4
P1.3	Standard I/O	8	Yes	P1MAT.3	ADC0.11 CP1P.5 CP1N.5
P2.0 / C2D	Standard I/O / C2 Debug Data	7			

---

## 4. Ordering Information



**Figure 4.1. C8051F85x/86x Part Numbering**

All C8051F85x/86x family members have the following features:

- CIP-51 Core running up to 25 MHz
- Two Internal Oscillators (24.5 MHz and 80 kHz)
- I2C/SMBus
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 16-bit CRC Unit

In addition to these features, each part number in the C8051F85x/86x family has a set of features that vary across the product line. The product selection guide in Table 4.1 shows the features available on each family member.

All devices in Table 4.1 are also available in an industrial version. For the industrial version, the -G in the ordering part number is replaced with -I. For example, the industrial version of the C8051F850-C-GM is the C8051F850-C-IM.

**Table 4.1. Product Selection Guide**

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of ADC0 Channels	I/O with Comparator 0/1 Inputs	Pb-free (RoHS Compliant)	AEC-Q100 Qualified	Temperature Range	Package
C8051F850-C-GM	8	512	16	15	15	☒	☒	-40 to 85 °C	QFN-20
C8051F850-C-GU	8	512	18	16	16	☒	☒	-40 to 85 °C	QSOP-24
C8051F851-C-GM	4	512	16	15	15	☒	☒	-40 to 85 °C	QFN-20
C8051F851-C-GU	4	512	18	16	16	☒	☒	-40 to 85 °C	QSOP-24
C8051F852-C-GM	2	256	16	15	15	☒	☒	-40 to 85 °C	QFN-20
C8051F852-C-GU	2	256	18	16	16	☒	☒	-40 to 85 °C	QSOP-24
C8051F853-C-GM	8	512	16	—	15	☒	☒	-40 to 85 °C	QFN-20
C8051F853-C-GU	8	512	18	—	16	☒	☒	-40 to 85 °C	QSOP-24
C8051F854-C-GM	4	512	16	—	15	☒	☒	-40 to 85 °C	QFN-20
C8051F854-C-GU	4	512	18	—	16	☒	☒	-40 to 85 °C	QSOP-24
C8051F855-C-GM	2	256	16	—	15	☒	☒	-40 to 85 °C	QFN-20
C8051F855-C-GU	2	256	18	—	16	☒	☒	-40 to 85 °C	QSOP-24
C8051F860-C-GS	8	512	13	12	12	☒	☒	-40 to 85 °C	SOIC-16
C8051F861-C-GS	4	512	13	12	12	☒	☒	-40 to 85 °C	SOIC-16
C8051F862-C-GS	2	256	13	12	12	☒	☒	-40 to 85 °C	SOIC-16
C8051F863-C-GS	8	512	13	—	12	☒	☒	-40 to 85 °C	SOIC-16
C8051F864-C-GS	4	512	13	—	12	☒	☒	-40 to 85 °C	SOIC-16
C8051F865-C-GS	2	256	13	—	12	☒	☒	-40 to 85 °C	SOIC-16

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**Table 4.1. Product Selection Guide**

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	Number of ADC0 Channels	I/O with Comparator 0/1 Inputs	Pb-free (RoHS Compliant)	AEC-Q100 Qualified	Temperature Range	Package
-IM, -IU and -IS extended temperature range devices (-40 to 125 °C) are also available.									

## 5. QSOP-24 Package Specifications

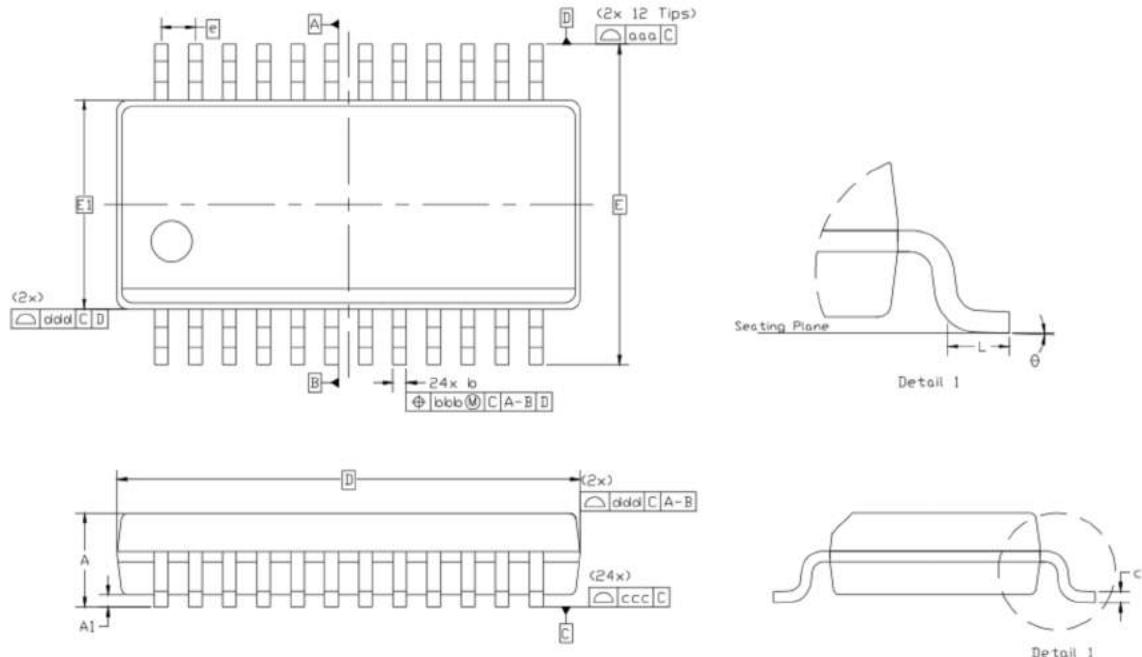


Figure 5.1. QSOP-24 Package Drawing

Table 5.1. QSOP-24 Package Dimensions

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—	—	1.75	e		0.635 BSC	
A1	0.10	—	0.25	L	0.40	—	1.27
b	0.20	—	0.30	$\theta$	0°	—	8°
c	0.10	—	0.25	aaa		0.20	
D		8.65 BSC		bbb		0.18	
E		6.00 BSC		ccc		0.10	
E1		3.90 BSC		ddd		0.10	

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

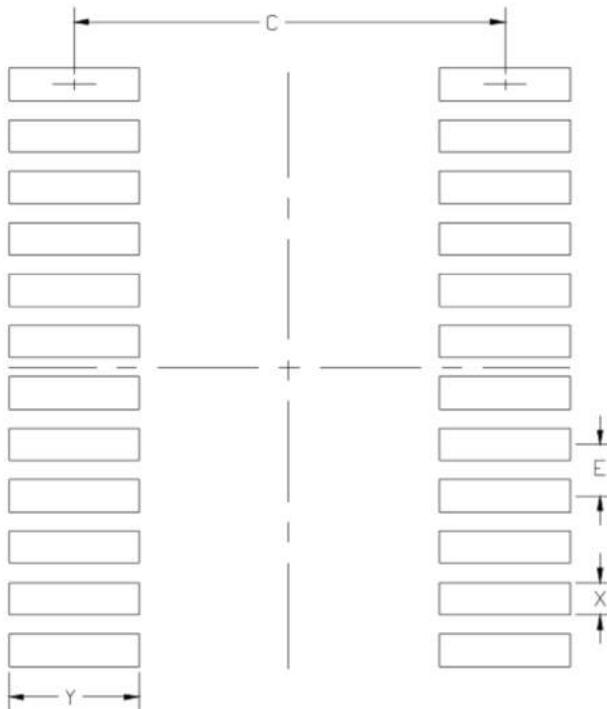


Figure 5.2. QSOP-24 PCB Land Pattern

Table 5.2. QSOP-24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.

**Solder Mask Design**

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

**Card Assembly**

7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 6. QFN-20 Package Specifications

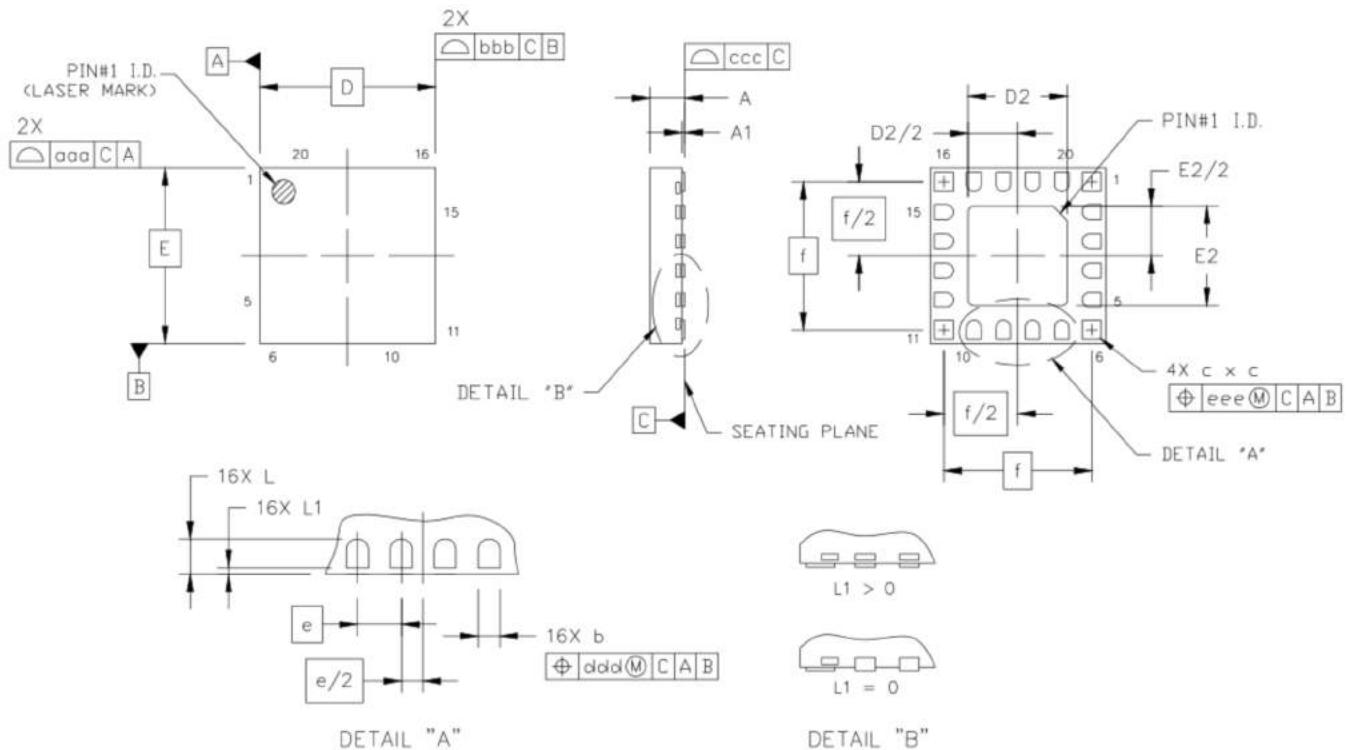


Figure 6.1. QFN-20 Package Drawing

Table 6.1. QFN-20 Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.25	0.30	0.35
D	3.00 BSC		
D2	1.6	1.70	1.8
e	0.50 BSC		
E	3.00 BSC		
E2	1.6	1.70	1.8

Symbol	Millimeters		
	Min	Nom	Max
f	2.53 BSC		
L	0.3	0.40	0.5
L1	0.00	—	0.10
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

**Notes:**

1. All dimensions are shown in millimeters unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.

# C8051F85x/86x

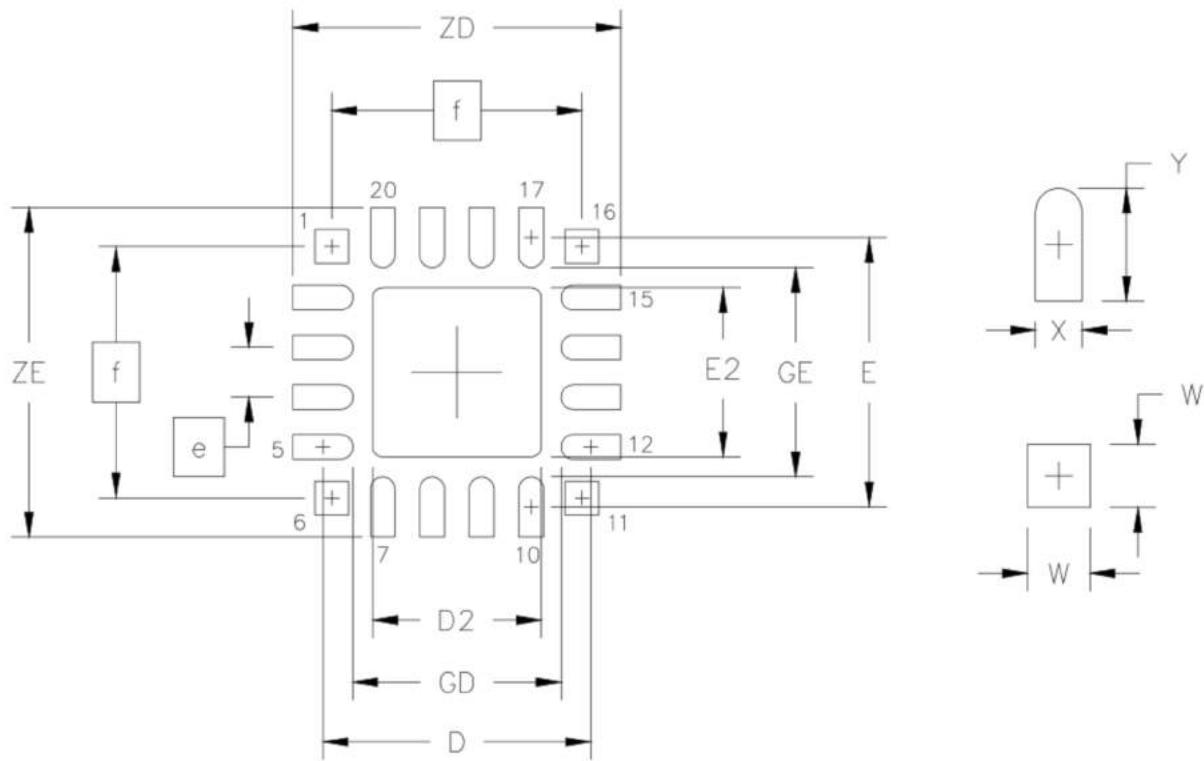


Figure 6.2. QFN-20 Landing Diagram

**Table 6.2. QFN-20 Landing Diagram Dimensions**

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
D	2.71	REF	GE	2.10	—
D2	1.60	1.80	W	—	0.34
e	0.50	BSC	X	—	0.28
E	2.71	REF	Y	0.61 REF	
E2	1.60	1.80	ZE	—	3.31
f	2.53	BSC	ZD	—	3.31
GD	2.10	—			

**Notes: General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Notes: Solder Mask Design**

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

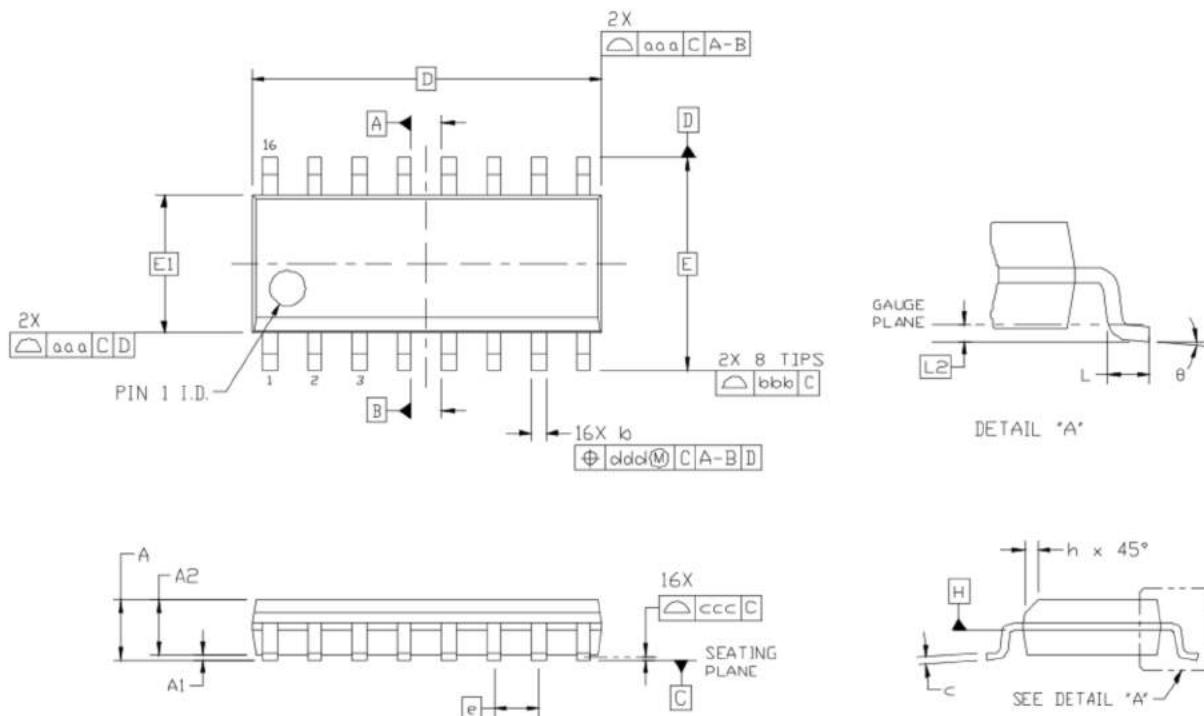
**Notes: Stencil Design**

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 1.45 x 1.45 mm square aperture should be used for the center pad. This provides approximately 70% solder paste coverage on the pad, which is optimum to assure correct component stand-off.

**Notes: Card Assembly**

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7. SOIC-16 Package Specifications



**Figure 7.1. SOIC-16 Package Drawing**

**Table 7.1. SOIC-16 Package Dimensions**

Dimension	Min	Nom	Max	Dimension	Min	Nom	Max
A	—		1.75	L	0.40		1.27
A1	0.10		0.25	L2		0.25 BSC	
A2	1.25		—	h	0.25		0.50
b	0.31		0.51	bbb		0.20	
c	0.17		0.25	ccc		0.10	
D		9.90 BSC		ddd		0.25	
E		6.00 BSC					
E1		3.90 BSC					
e		1.27 BSC					

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

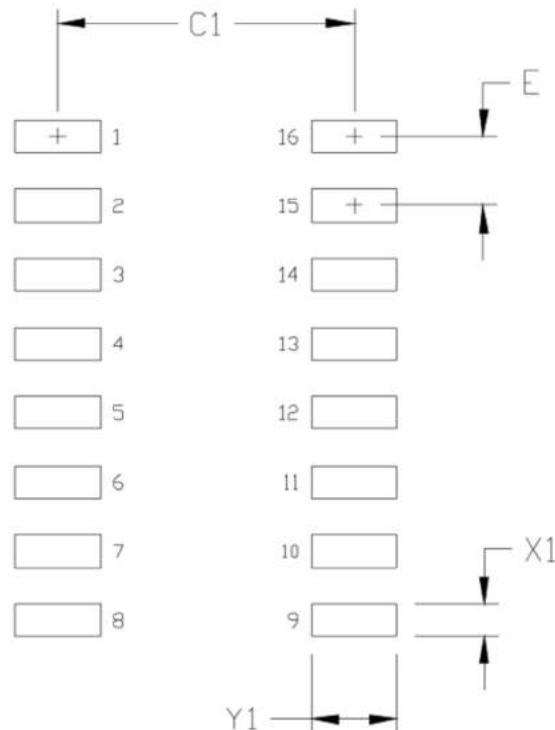


Figure 7.2. SOIC-16 PCB Land Pattern

Table 7.2. SOIC-16 PCB Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

**Notes:**

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 8. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. The memory organization of the C8051F85x/86x device family is shown in Figure 8.1.

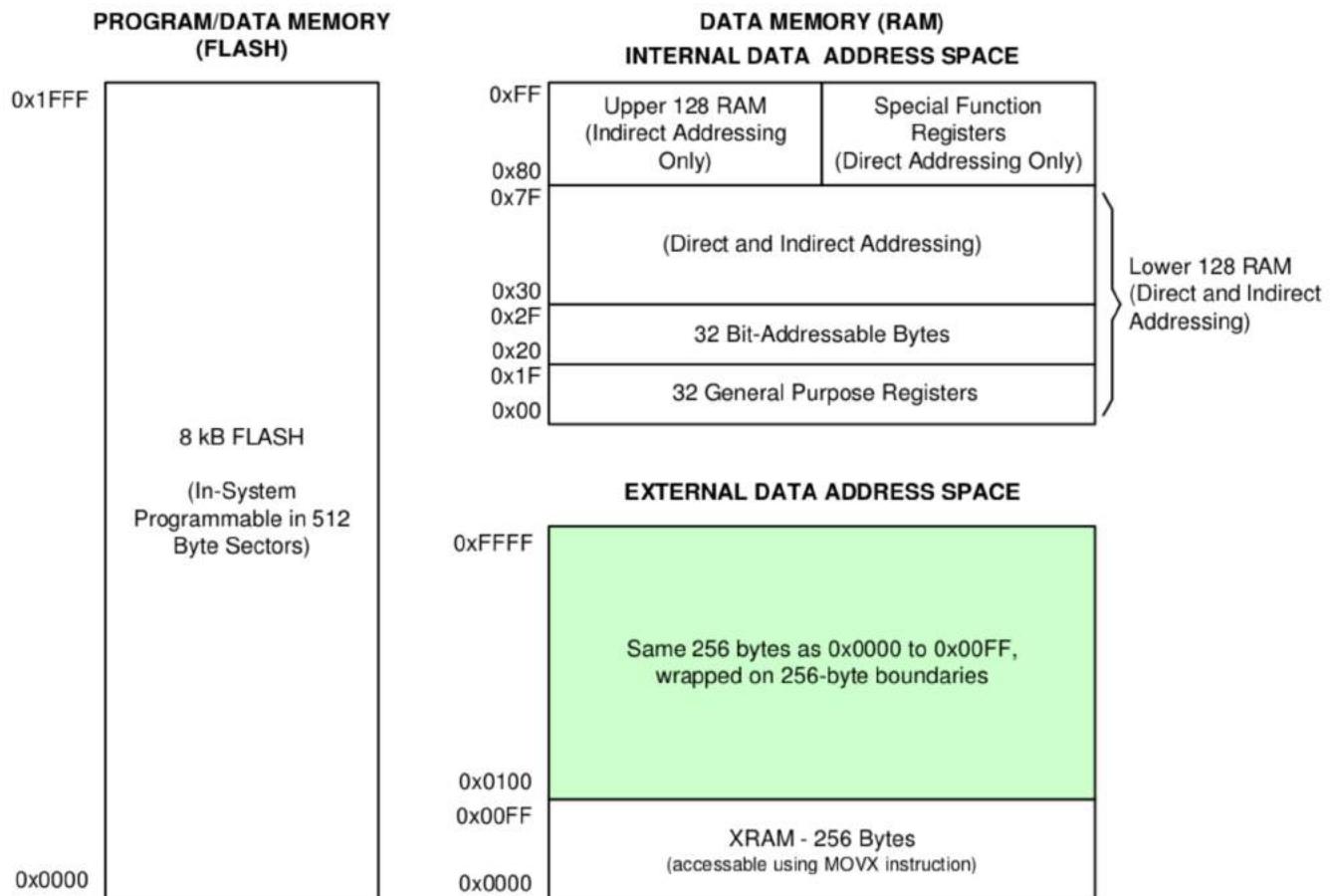


Figure 8.1. C8051F85x/86x Memory Map (8 kB flash version shown)

## 8.1. Program Memory

The CIP-51 core has a 64 kB program memory space. The C8051F85x/86x family implements 8 kB, 4 kB or 2 kB of this program memory space as in-system, re-programmable flash memory. The last address in the flash block (0x1FFF on 8 kB devices, 0x0FFF on 4 kB devices and 0x07FF on 2 kB devices) serves as a security lock byte for the device, and provides read, write and erase protection. Addresses above the lock byte within the 64 kB address space are reserved.

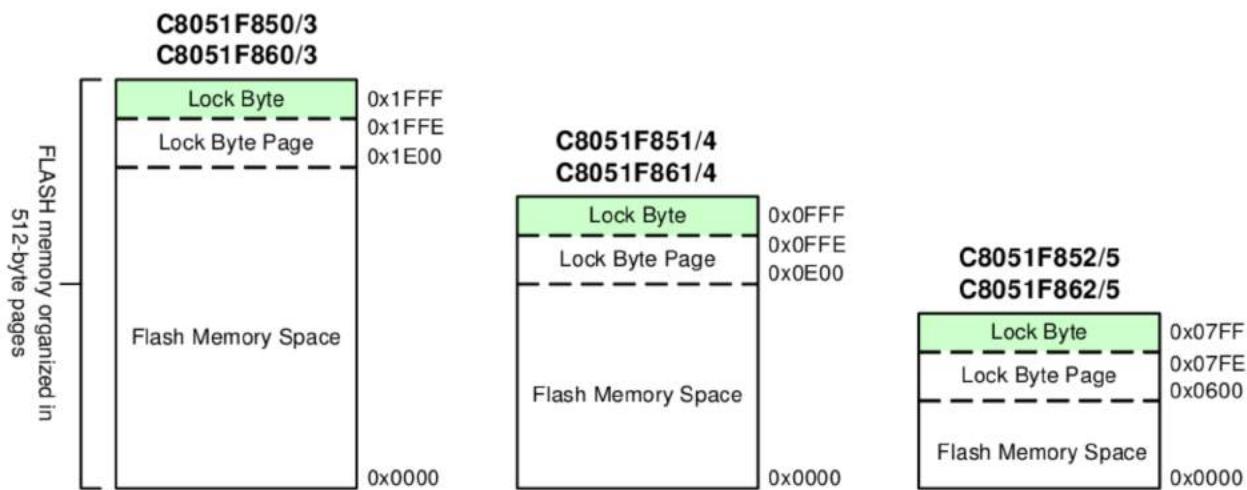


Figure 8.2. Flash Program Memory Map

### 8.1.1. MOVX Instruction and Program Memory

The MOVX instruction in an 8051 device is typically used to access external data memory. On the C8051F85x/86x devices, the MOVX instruction is normally used to read and write on-chip XRAM, but can be re-configured to write and erase on-chip flash memory space. MOVC instructions are always used to read flash memory, while MOVX write instructions are used to erase and write flash. This flash access feature provides a mechanism for the C8051F85x/86x to update program code and use the program memory space for non-volatile data storage. Refer to Section “10. Flash Memory” on page 61 for further details.

## 8.2. Data Memory

The C8051F85x/86x device family includes up to 512 bytes of RAM data memory. 256 bytes of this memory is mapped into the internal RAM space of the 8051. On devices with 512 bytes total RAM, 256 additional bytes of memory are available as on-chip “external” memory. The data memory map is shown in Figure 8.1 for reference.

### 8.2.1. Internal RAM

There are 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and scratch pad memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct addressing mode.

---

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F access the upper 128 bytes of data memory. Figure 8.1 illustrates the data memory organization of the C8051F85x/86x.

Revision C C8051F852/5 and C8051F862/5 devices implement the upper four bytes of internal RAM as a 32-bit Unique Identifier. More information can be found in "Device Identification and Unique Identifier" on page 68.

### 8.2.1.1. General Purpose Registers

The lower 32 bytes of data memory, locations 0x00 through 0x1F, may be addressed as four banks of general-purpose registers. Each bank consists of eight byte-wide registers designated R0 through R7. Only one of these banks may be enabled at a time. Two bits in the program status word (PSW) register, RS0 and RS1, select the active register bank. This allows fast context switching when entering subroutines and interrupt service routines. Indirect addressing modes use registers R0 and R1 as index registers.

### 8.2.1.2. Bit Addressable Locations

In addition to direct access to data memory organized as bytes, the sixteen data memory locations at 0x20 through 0x2F are also accessible as 128 individually addressable bits. Each bit has a bit address from 0x00 to 0x7F. Bit 0 of the byte at 0x20 has bit address 0x00 while bit7 of the byte at 0x20 has bit address 0x07. Bit 7 of the byte at 0x2F has bit address 0x7F. A bit access is distinguished from a full byte access by the type of instruction used (bit source or destination operands as opposed to a byte source or destination).

The MCS-51™ assembly language allows an alternate notation for bit addressing of the form XX.B where XX is the byte address and B is the bit position within the byte. For example, the instruction:

```
MOV C, 22.3h
```

moves the Boolean value at 0x13 (bit 3 of the byte at location 0x22) into the Carry flag.

### 8.2.1.3. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

## 8.2.2. External RAM

On devices with 512 bytes total RAM, there are 256 bytes of on-chip RAM mapped into the external data memory space. All of these address locations may be accessed using the external move instruction (MOVX) and the data pointer (DPTR), or using MOVX indirect addressing mode. Note: The 16-bit MOVX instruction is also used for writes to the flash memory. See Section "10. Flash Memory" on page 61 for details. The MOVX instruction accesses XRAM by default.

For a 16-bit MOVX operation (@DPTR), the upper 8 bits of the 16-bit external data memory address word are "don't cares". As a result, addresses 0x0000 through 0x00FF are mapped modulo style over the entire 64 k external data memory address range. For example, the XRAM byte at address 0x0000 is shadowed at addresses 0x0100, 0x0200, 0x0300, 0x0400, etc.

Revision C C8051F850/1/3/4 and C8051F860/1/3/4 devices implement the upper four bytes of external RAM as a 32-bit Unique Identifier. More information can be found in "Device Identification and Unique Identifier" on page 68.

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### **8.2.3. Special Function Registers**

The direct-access data memory locations from 0x80 to 0xFF constitute the special function registers (SFRs). The SFRs provide control and data exchange with the CIP-51's resources and peripherals. The CIP-51 duplicates the SFRs found in a typical 8051 implementation as well as implementing additional SFRs used to configure and access the sub-systems unique to the MCU. This allows the addition of new functionality while retaining compatibility with the MCS-51™ instruction set.

The SFR registers are accessed anytime the direct addressing mode is used to access memory locations from 0x80 to 0xFF. SFRs with addresses ending in 0x0 or 0x8 (e.g. P0, TCON, SCON0, IE, etc.) are bit-addressable as well as byte-addressable. All other SFRs are byte-addressable only. Unoccupied addresses in the SFR space are reserved for future use. Accessing these areas will have an indeterminate effect and should be avoided.

## 9. Special Function Register Memory Map

This section details the special function register memory map for the C8051F85x/86x devices.

**Table 9.1. Special Function Register (SFR) Memory Map**

F8	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	P0MAT	P0MASK	VDM0CN
F0	B	P0MDIN	P1MDIN	EIP1	-	-	PRTDRV	PCA0PWM
E8	ADC0CN0	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	P1MAT	P1MASK	RSTSRC
E0	ACC	XBR0	XBR1	XBR2	IT01CF	-	EIE1	-
D8	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	CRC0IN	CRC0DAT	ADC0PWR
D0	PSW	REF0CN	CRC0AUTO	CRC0CNT	P0SKIP	P1SKIP	SMB0ADM	SMB0ADR
C8	TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	CRC0CN	CRC0FLIP
C0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	OSCICL
B8	IP	ADC0TK	-	ADC0MX	ADC0CF	ADC0L	ADC0H	CPT1CN
B0	-	OSCLCN	ADC0CN1	ADC0AC	-	DEVICEID	REVID	FLKEY
A8	IE	CLKSEL	CPT1MX	CPT1MD	SMB0TC	DERIVID	-	-
A0	P2	SPI0CFG	SPI0CKR	SPI0DAT	P0MDOUT	P1MDOUT	P2MDOUT	-
98	SCON0	SBUF0	-	CPT0CN	PCA0CLR	CPT0MD	PCA0CENT	CPT0MX
90	P1	TMR3CN	TMR3RLL	TMR3RLH	TMR3L	TMR3H	PCA0POL	WDTCN
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	PSCTL
80	P0	SP	DPL	DPH	-	-	-	PCON
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)

(bit addressable)

**Table 9.2. Special Function Registers**

Register	Address	Register Description	Page
ACC	0xE0	Accumulator	122
ADC0AC	0xB3	ADC0 Accumulator Configuration	102
ADC0CF	0xBC	ADC0 Configuration	101
ADC0CN0	0xE8	ADC0 Control 0	99
ADC0CN1	0xB2	ADC0 Control 1	100
ADC0GTH	0xC4	ADC0 Greater-Than High Byte	107
ADC0GTL	0xC3	ADC0 Greater-Than Low Byte	108
ADC0H	0xBE	ADC0 Data Word High Byte	105

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**Table 9.2. Special Function Registers (Continued)**

<b>Register</b>	<b>Address</b>	<b>Register Description</b>	<b>Page</b>
ADC0L	0xBD	ADC0 Data Word Low Byte	106
ADC0LTH	0xC6	ADC0 Less-Than High Byte	109
ADC0LTL	0xC5	ADC0 Less-Than Low Byte	110
ADC0MX	0xBB	ADC0 Multiplexer Selection	111
ADC0PWR	0xDF	ADC0 Power Control	103
ADC0TK	0xB9	ADC0 Burst Mode Track Time	104
B	0xF0	B Register	123
CKCON	0x8E	Clock Control	269
CLKSEL	0xA9	Clock Selection	129
CPT0CN	0x9B	Comparator 0 Control	134
CPT0MD	0x9D	Comparator 0 Mode	135
CPT0MX	0x9F	Comparator 0 Multiplexer Selection	136
CPT1CN	0xBF	Comparator 1 Control	137
CPT1MD	0xAB	Comparator 1 Mode	138
CPT1MX	0xAA	Comparator 1 Multiplexer Selection	139
CRC0AUTO	0xD2	CRC0 Automatic Control	146
CRC0CN	0xCE	CRC0 Control	143
CRC0CNT	0xD3	CRC0 Automatic Flash Sector Count	147
CRC0DAT	0xDE	CRC0 Data Output	145
CRC0FLIP	0xCF	CRC0 Bit Flip	148
CRC0IN	0xDD	CRC0 Data Input	144
DERIVID	0xAD	Derivative Identification	70
DEVICEID	0xB5	Device Identification	69
DPH	0x83	Data Pointer Low	120
DPL	0x82	Data Pointer High	119
EIE1	0xE6	Extended Interrupt Enable 1	78
EIP1	0xF3	Extended Interrupt Priority 1	80
FLKEY	0xB7	Flash Lock and Key	67

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**Table 9.2. Special Function Registers (Continued)**

<b>Register</b>	<b>Address</b>	<b>Register Description</b>	<b>Page</b>
IE	0xA8	Interrupt Enable	75
IP	0xB8	Interrupt Priority	77
IT01CF	0xE4	INT0 / INT1 Configuration	150
OSCICL	0xC7	High Frequency Oscillator Calibration	127
OSCLCN	0xB1	Low Frequency Oscillator Control	128
P0	0x80	Port 0 Pin Latch	199
P0MASK	0xFE	Port 0 Mask	197
P0MAT	0xFD	Port 0 Match	198
P0MDIN	0xF1	Port 0 Input Mode	200
P0MDOUT	0xA4	Port 0 Output Mode	201
P0SKIP	0xD4	Port 0 Skip	202
P1	0x90	Port 1 Pin Latch	205
P1MASK	0xEE	Port 1 Mask	203
P1MAT	0xED	Port 1 Match	204
P1MDIN	0xF2	Port 1 Input Mode	206
P1MDOUT	0xA5	Port 1 Output Mode	207
P1SKIP	0xD5	Port 1 Skip	208
P2	0xA0	Port 2 Pin Latch	209
P2MDOUT	0xA6	Port 2 Output Mode	210
PCA0CENT	0x9E	PCA Center Alignment Enable	177
PCA0CLR	0x9C	PCA Comparator Clear Control	170
PCA0CN	0xD8	PCA Control	167
PCA0CPH0	0xFC	PCA Capture Module High Byte 0	175
PCA0CPH1	0xEA	PCA Capture Module High Byte 1	181
PCA0CPH2	0xEC	PCA Capture Module High Byte 2	183
PCA0CPL0	0xFB	PCA Capture Module Low Byte 0	174
PCA0CPL1	0xE9	PCA Capture Module Low Byte 1	180
PCA0CPL2	0xEB	PCA Capture Module Low Byte 2	182

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**Table 9.2. Special Function Registers (Continued)**

<b>Register</b>	<b>Address</b>	<b>Register Description</b>	<b>Page</b>
PCA0CPM0	0xDA	PCA Capture/Compare Mode 0	171
PCA0CPM1	0xDB	PCA Capture/Compare Mode 1	178
PCA0CPM2	0xDC	PCA Capture/Compare Mode 1	179
PCA0H	0xFA	PCA Counter/Timer Low Byte	173
PCA0L	0xF9	PCA Counter/Timer High Byte	172
PCA0MD	0xD9	PCA Mode	168
PCA0POL	0x96	PCA Output Polarity	176
PCA0PWM	0xF7	PCA PWM Configuration	169
PCON	0x87	Power Control	83
PRTDRV	0xF6	Port Drive Strength	196
PSCTL	0x8F	Program Store Control	66
PSW	0xD0	Program Status Word	124
REF0CN	0xD1	Voltage Reference Control	112
REG0CN	0xC9	Voltage Regulator Control	84
REVID	0xB6	Revision Identification	71
RSTSRC	0xEF	Reset Source	215
SBUFO	0x99	UART0 Serial Port Data Buffer	297
SCON0	0x98	UART0 Serial Port Control	295
SMB0ADM	0xD6	SMBus0 Slave Address Mask	257
SMB0ADR	0xD7	SMBus0 Slave Address	256
SMB0CF	0xC1	SMBus0 Configuration	251
SMB0CN	0xC0	SMBus0 Control	254
SMB0DAT	0xC2	SMBus0 Data	258
SMB0TC	0xAC	SMBus0 Timing and Pin Control	253
SP	0x81	Stack Pointer	121
SPI0CFG	0xA1	SPI0 Configuration	227
SPI0CKR	0xA2	SPI0 Clock Control	231
SPI0CN	0xF8	SPI0 Control	229

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**Table 9.2. Special Function Registers (Continued)**

<b>Register</b>	<b>Address</b>	<b>Register Description</b>	<b>Page</b>
SPI0DAT	0xA3	SPI0 Data	232
TCON	0x88	Timer 0/1 Control	271
TH0	0x8C	Timer 0 High Byte	275
TH1	0x8D	Timer 1 High Byte	276
TL0	0x8A	Timer 0 Low Byte	273
TL1	0x8B	Timer 1 Low Byte	274
TMOD	0x89	Timer 0/1 Mode	272
TMR2CN	0xC8	Timer 2 Control	277
TMR2H	0xCD	Timer 2 High Byte	282
TMR2L	0xCC	Timer 2 Low Byte	281
TMR2RLH	0xCB	Timer 2 Reload High Byte	280
TMR2RLL	0xCA	Timer 2 Reload Low Byte	279
TMR3CN	0x91	Timer 3 Control	283
TMR3H	0x95	Timer 3 High Byte	288
TMR3L	0x94	Timer 3 Low Byte	287
TMR3RLH	0x93	Timer 3 Reload High Byte	286
TMR3RLL	0x92	Timer 3 Reload Low Byte	285
VDM0CN	0xFF	Supply Monitor Control	216
WDTCN	0x97	Watchdog Timer Control	300
XBR0	0xE1	Port I/O Crossbar 0	193
XBR1	0xE2	Port I/O Crossbar 1	194
XBR2	0xE3	Port I/O Crossbar 2	195

## 10. Flash Memory

On-chip, re-programmable flash memory is included for program code and non-volatile data storage. The flash memory is organized in 512-byte pages. It can be erased and written through the C2 interface or from firmware by overloading the MOVX instruction. Any individual byte in flash memory must only be written once between page erase operations.

### 10.1. Security Options

The CIP-51 provides security options to protect the flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the flash memory from accidental modification by software. PSWE must be explicitly set to '1' before software can modify the flash memory; both PSWE and PSEE must be set to '1' before software can erase flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located in flash user space offers protection of the flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. See Section "8. Memory Organization" on page 52 for the location of the security byte. The flash security mechanism allows the user to lock  $n$  512-byte flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where  $n$  is the 1's complement number represented by the Security Lock Byte. **Note that the page containing the flash Security Lock Byte is unlocked when no other flash pages are locked (all bits of the Lock Byte are '1') and locked when any other flash pages are locked (any bit of the Lock Byte is '0')**. An example is shown in Figure 10.1.

Security Lock Byte:	11111101b
1s Complement:	00000010b
Flash pages locked:	3 (First two flash pages + Lock Byte Page)

**Figure 10.1. Security Byte Decoding**

The level of flash security depends on the flash access method. The three flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on unlocked pages, and user firmware executing on locked pages. Table 10.1 summarizes the flash security features of the C8051F85x/86x devices.

**Table 10.1. Flash Security Summary**

Action	C2 Debug Interface	User Firmware executing from:	
		an unlocked page	a locked page
Read, Write or Erase unlocked pages (except page with Lock Byte)	Permitted	Permitted	Permitted
Read, Write or Erase locked pages (except page with Lock Byte)	Not Permitted	Flash Error Reset	Permitted
Read or Write page containing Lock Byte (if no pages are locked)	Permitted	Permitted	N/A
Read or Write page containing Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted

---

**Table 10.1. Flash Security Summary (Continued)**

Read contents of Lock Byte (if no pages are locked)	Permitted	Permitted	N/A
Read contents of Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Erase page containing Lock Byte (if no pages are locked)	Permitted	Permitted	N/A
Erase page containing Lock Byte—Unlock all pages (if any page is locked)	C2 Device Erase Only	Flash Error Reset	Flash Error Reset
Lock additional pages (change 1s to 0s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Unlock individual pages (change 0s to 1s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Read, Write or Erase Reserved Area	Not Permitted	Flash Error Reset	Flash Error Reset

C2 Device Erase—Erases all flash pages including the page containing the Lock Byte.  
Flash Error Reset —Not permitted; Causes Flash Error Device Reset (FERROR bit in RSTSRC is '1' after reset).

- All prohibited operations that are performed via the C2 interface are ignored (do not cause device reset).
- Locking any flash page also locks the page containing the Lock Byte.
- Once written to, the Lock Byte cannot be modified except by performing a C2 Device Erase.
- If user code writes to the Lock Byte, the Lock does not take effect until the next device reset.

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## 10.2. Programming the Flash Memory

Writes to flash memory clear bits from logic 1 to logic 0, and can be performed on single byte locations. Flash erasures set bits back to logic 1, and occur only on full pages. The write and erase operations are automatically timed by hardware for proper execution; data polling to determine the end of the write/erase operation is not required. Code execution is stalled during a flash write/erase operation.

The simplest means of programming the flash memory is through the C2 interface using programming tools provided by Silicon Labs or a third party vendor. This is the only means for programming a non-initialized device.

To ensure the integrity of flash contents, it is strongly recommended that the on-chip supply monitor be enabled in any system that includes code that writes and/or erases flash memory from software.

### 10.2.1. Flash Lock and Key Functions

Flash writes and erases by user software are protected with a lock and key function. The Flash Lock and Key Register (FLKEY) must be written with the correct key codes, in sequence, before flash operations may be performed. The key codes are: 0xA5, 0xF1. The timing does not matter, but the codes must be written in order. If the key codes are written out of order, or the wrong codes are written, flash writes and erases will be disabled until the next system reset. Flash writes and erases will also be disabled if a flash write or erase is attempted before the key codes have been written properly. The flash lock resets after each write or erase; the key codes must be written again before a following flash operation can be performed.

### 10.2.2. Flash Erase Procedure

The flash memory can be programmed by software using the MOVX write instruction with the address and data byte to be programmed provided as normal operands. Before writing to flash memory using MOVX, flash write operations must be enabled by: (1) setting the PSWE Program Store Write Enable bit in the PSCTL register to logic 1 (this directs the MOVX writes to target flash memory); and (2) Writing the flash key codes in sequence to the Flash Lock register (FLKEY). The PSWE bit remains set until cleared by software.

A write to flash memory can clear bits to logic 0 but cannot set them; only an erase operation can set bits to logic 1 in flash. **A byte location to be programmed should be erased before a new value is written.** Erase operation applies to an entire page (setting all bytes in the page to 0xFF). To erase an entire page, perform the following steps:

1. Disable interrupts (recommended).
2. Set the PSEE bit (register PSCTL).
3. Set the PSWE bit (register PSCTL).
4. Write the first key code to FLKEY: 0xA5.
5. Write the second key code to FLKEY: 0xF1.
6. Using the MOVX instruction, write a data byte to any location within the page to be erased.
7. Clear the PSWE and PSEE bits.

### 10.2.3. Flash Write Procedure

Flash bytes are programmed by software with the following sequence:

1. Disable interrupts (recommended).
2. Erase the flash page containing the target location, as described in Section 10.2.2.
3. Set the PSWE bit (register PSCTL).
4. Clear the PSEE bit (register PSCTL).
5. Write the first key code to FLKEY: 0xA5.
6. Write the second key code to FLKEY: 0xF1.
7. Using the MOVX instruction, write a single data byte to the desired location within the desired

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page.

8. Clear the PSWE bit.

Steps 5–7 must be repeated for each byte to be written. After flash writes are complete, PSWE should be cleared so that MOVX instructions do not target program memory.

### 10.3. Non-Volatile Data Storage

The flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. Note: MOVX read instructions always target XRAM.

### 10.4. Flash Write and Erase Guidelines

Any system which contains routines which write or erase flash memory from software involves some risk that the write or erase routines will execute unintentionally if the CPU is operating outside its specified operating range of supply voltage, system clock frequency or temperature. This accidental execution of flash modifying code can result in alteration of flash memory contents causing a system failure that is only recoverable by re-flashing the code in the device.

To help prevent the accidental modification of flash by firmware, hardware restricts flash writes and erasures when the supply monitor is not active and selected as a reset source. As the monitor is enabled and selected as a reset source by default, it is recommended that systems writing or erasing flash simply maintain the default state.

The following guidelines are recommended for any system which contains routines which write or erase flash from code.

#### 10.4.1. Voltage Supply Maintenance and the Supply Monitor

1. If the system power supply is subject to voltage or current "spikes," add sufficient transient protection devices to the power supply to ensure that the supply voltages listed in the Absolute Maximum Ratings table are not exceeded.
2. Make certain that the minimum supply rise time specification is met. If the system cannot meet this rise time specification, then add an external supply brownout circuit to the RST pin of the device that holds the device in reset until the voltage supply reaches the lower limit, and re-asserts RST if the supply drops below the low supply limit.
3. Do not disable the supply monitor. If the supply monitor must be disabled in the system, firmware should be added to the startup routine to enable the on-chip supply monitor and enable the supply monitor as a reset source as early in code as possible. This should be the first set of instructions executed after the reset vector. For C-based systems, this may involve modifying the startup code added by the C compiler. See your compiler documentation for more details. Make certain that there are no delays in software between enabling the supply monitor and enabling the supply monitor as a reset source. Code examples showing this can be found in "AN201: Writing to Flash From Firmware", available from the Silicon Laboratories web site. **Note that the supply monitor must be enabled and enabled as a reset source when writing or erasing flash memory. A flash error reset will occur if either condition is not met.**
4. As an added precaution if the supply monitor is ever disabled, explicitly enable the supply monitor and enable the supply monitor as a reset source inside the functions that write and erase flash memory. The supply monitor enable instructions should be placed just after the instruction to set PSWE to a 1, but before the flash write or erase operation instruction.
5. Make certain that all writes to the RSTSRC (Reset Sources) register use direct assignment operators and explicitly DO NOT use the bit-wise operators (such as AND or OR). For example, "RSTSRC = 0x02" is correct. "RSTSRC |= 0x02" is incorrect.
6. Make certain that all writes to the RSTSRC register explicitly set the PORSF bit to a '1'. Areas to check are initialization code which enables other reset sources, such as the Missing Clock

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Detector or Comparator, for example, and instructions which force a Software Reset. A global search on "RSTSRC" can quickly verify this.

#### **10.4.2. PSWE Maintenance**

7. Reduce the number of places in code where the PSWE bit (in register PSCTL) is set to a 1. There should be exactly one routine in code that sets PSWE to a '1' to write flash bytes and one routine in code that sets PSWE and PSEE both to a '1' to erase flash pages.
8. Minimize the number of variable accesses while PSWE is set to a 1. Handle pointer address updates and loop variable maintenance outside the "PSWE = 1;... PSWE = 0;" area. Code examples showing this can be found in "AN201: Writing to Flash From Firmware", available from the Silicon Laboratories web site.
9. Disable interrupts prior to setting PSWE to a '1' and leave them disabled until after PSWE has been reset to 0. Any interrupts posted during the flash write or erase operation will be serviced in priority order after the flash operation has been completed and interrupts have been re-enabled by software.
10. Make certain that the flash write and erase pointer variables are not located in XRAM. See your compiler documentation for instructions regarding how to explicitly locate variables in different memory areas.
11. Add address bounds checking to the routines that write or erase flash memory to ensure that a routine called with an illegal address does not result in modification of the flash.

#### **10.4.3. System Clock**

12. If operating from an external crystal-based source, be advised that crystal performance is susceptible to electrical interference and is sensitive to layout and to changes in temperature. If the system is operating in an electrically noisy environment, use the internal oscillator or use an external CMOS clock.
13. If operating from the external oscillator, switch to the internal oscillator during flash write or erase operations. The external oscillator can continue to run, and the CPU can switch back to the external oscillator after the flash operation has completed.

Additional flash recommendations and example code can be found in "AN201: Writing to Flash From Firmware", available from the Silicon Laboratories website.

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## 10.5. Flash Control Registers

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### Register 10.1. PSCTL: Program Store Control

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Bit	7	6	5	4	3	2	1	0
Name			Reserved				PSEE	PSWE
Type			R				RW	RW
Reset	0	0	0	0	0	0	0	0
<b>SFR Address: 0x8F</b>								

**Table 10.2. PSCTL Register Bit Descriptions**

Bit	Name	Function
7:2	Reserved	Must write reset value.
1	PSEE	<b>Program Store Erase Enable.</b> Setting this bit (in combination with PSWE) allows an entire page of flash program memory to be erased. If this bit is logic 1 and flash writes are enabled (PSWE is logic 1), a write to flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter. 0: Flash program memory erasure disabled. 1: Flash program memory erasure enabled.
0	PSWE	<b>Program Store Write Enable.</b> Setting this bit allows writing a byte of data to the flash program memory using the MOVX write instruction. The flash location should be erased before writing data. 0: Writes to flash program memory disabled. 1: Writes to flash program memory enabled; the MOVX write instruction targets flash memory.

---

## Register 10.2. FLKEY: Flash Lock and Key

---

Bit	7	6	5	4	3	2	1	0
Name	FLKEY							
Type	RW							
Reset	0	0	0	0	0	0	0	0
<b>SFR Address: 0xB7</b>								

**Table 10.3. FLKEY Register Bit Descriptions**

Bit	Name	Function
7:0	FLKEY	<b>Flash Lock and Key Register.</b> Write: This register provides a lock and key function for flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a flash write or erase operation is attempted while these operations are disabled, the flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to flash, it can intentionally lock the flash by writing a non-0xA5 value to FLKEY from software. Read: When read, bits 1-0 indicate the current flash lock state. 00: Flash is write/erase locked. 01: The first key code has been written (0xA5). 10: Flash is unlocked (writes/erases allowed). 11: Flash writes/erases are disabled until the next reset.

---

## 11. Device Identification and Unique Identifier

The C8051F85x/86x has SFRs that identify the device family, derivative, and revision. These SFRs can be read by firmware at runtime to determine the capabilities of the MCU that is executing code. This allows the same firmware image to run on MCUs with different memory sizes and peripherals, and dynamically change functionality to suit the capabilities of that MCU.

In addition to the device identification registers, a 32-bit unique identifier (UID) is pre-programmed into all Revision C and later devices. The UID resides in the last four bytes of XRAM (C8051F850/1/3/4 and C8051F860/1/3/4) or RAM (C8051F852/5 and C8051F862/5). For devices with the UID in RAM, the UID can be read by firmware using indirect data accesses. For devices with the UID in XRAM, the UID can be read by firmware using MOVX instructions. The UID can also be read through the debug port for all devices.

Firmware can overwrite the UID during normal operation, and the bytes in memory will be automatically reinitialized with the UID value after any device reset. Firmware using this area of memory should always initialize the memory to a known value, as any previous data stored at these locations will be overwritten and not retained through a reset.

**Table 11.1. UID Implementation Information**

Device	Memory Segment	Addresses
C8051F850 C8051F851 C8051F853 C8051F854 C8051F860 C8051F861 C8051F863 C8051F864	XRAM	(MSB) 0x00FF, 0x00FE, 0x00FD, 0x00FC (LSB)
C8051F852 C8051F855 C8051F862 C8051F865	RAM (indirect)	(MSB) 0xFF, 0xFE, 0xFD, 0xFC (LSB)

---

## 11.1. Device Identification Registers

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### Register 11.1. DEVICEID: Device Identification

---

Bit	7	6	5	4	3	2	1	0
Name	DEVICEID							
Type	R							
Reset	0	0	1	1	0	0	0	0
<b>SFR Address: 0xB5</b>								

**Table 11.2. DEVICEID Register Bit Descriptions**

Bit	Name	Function
7:0	DEVICEID	<b>Device ID.</b> This read-only register returns the 8-bit device ID: 0x30 (C8051F85x/86x).

---

**Register 11.2. DERIVID: Derivative Identification**

---

Bit	7	6	5	4	3	2	1	0
Name	DERIVID							
Type	R							
Reset	X	X	X	X	X	X	X	X
<b>SFR Address: 0xAD</b>								

**Table 11.3. DERIVID Register Bit Descriptions**

Bit	Name	Function
7:0	DERIVID	<b>Derivative ID.</b> This read-only register returns the 8-bit derivative ID, which can be used by firmware to identify which device in the product family the code is executing on. The '{R}' tag in the part numbers below indicates the device revision letter in the ordering code. 0xD0: C8051F850-{R}-GU 0xD1: C8051F851-{R}-GU 0xD2: C8051F852-{R}-GU 0xD3: C8051F853-{R}-GU 0xD4: C8051F854-{R}-GU 0xD5: C8051F855-{R}-GU 0xE0: C8051F860-{R}-GS 0xE1: C8051F861-{R}-GS 0xE2: C8051F862-{R}-GS 0xE3: C8051F863-{R}-GS 0xE4: C8051F864-{R}-GS 0xE5: C8051F865-{R}-GS 0xF0: C8051F850-{R}-GM 0xF1: C8051F851-{R}-GM 0xF2: C8051F852-{R}-GM 0xF3: C8051F853-{R}-GM 0xF4: C8051F854-{R}-GM 0xF5: C8051F855-{R}-GM

---

**Register 11.3. REVID: Revision Identification**

---

Bit	7	6	5	4	3	2	1	0
Name	REVID							
Type	R							
Reset	X	X	X	X	X	X	X	X
<b>SFR Address: 0xB6</b>								

**Table 11.4. REVID Register Bit Descriptions**

Bit	Name	Function
7:0	REVID	<b>Revision ID.</b> This read-only register returns the 8-bit revision ID. 00000000: Revision A 00000001: Revision B 00000010: Revision C 00000011-11111111: Reserved.

---

## 12. Interrupts

The C8051F85x/86x includes an extended interrupt system supporting multiple interrupt sources with two priority levels. The allocation of interrupt sources between on-chip peripherals and external input pins varies according to the specific version of the device. Each interrupt source has one or more associated interrupt-pending flag(s) located in an SFR. When a peripheral or external source meets a valid interrupt condition, the associated interrupt-pending flag is set to logic 1.

If interrupts are enabled for the source, an interrupt request is generated when the interrupt-pending flag is set. As soon as execution of the current instruction is complete, the CPU generates an LCALL to a predetermined address to begin execution of an interrupt service routine (ISR). Each ISR must end with an RETI instruction, which returns program execution to the next instruction that would have been executed if the interrupt request had not occurred. If interrupts are not enabled, the interrupt-pending flag is ignored by the hardware and program execution continues as normal. The interrupt-pending flag is set to logic 1 regardless of the interrupt's enable/disable state.

Each interrupt source can be individually enabled or disabled through the use of an associated interrupt enable bit in an SFR (IE and EIE1). However, interrupts must first be globally enabled by setting the EA bit in the IE register to logic 1 before the individual interrupt enables are recognized. Setting the EA bit to logic 0 disables all interrupt sources regardless of the individual interrupt-enable settings.

Some interrupt-pending flags are automatically cleared by the hardware when the CPU vectors to the ISR. However, most are not cleared by the hardware and must be cleared by software before returning from the ISR. If an interrupt-pending flag remains set after the CPU completes the return-from-interrupt (RETI) instruction, a new interrupt request will be generated immediately and the CPU will re-enter the ISR after the completion of the next instruction.

### 12.1. MCU Interrupt Sources and Vectors

The C8051F85x/86x MCUs support interrupt sources for each peripheral on the device. Software can simulate an interrupt by setting any interrupt-pending flag to logic 1. If interrupts are enabled for the flag, an interrupt request will be generated and the CPU will vector to the ISR address associated with the interrupt-pending flag. MCU interrupt sources, associated vector addresses, priority order and control bits are summarized in Table 12.1. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

#### 12.1.1. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IP or EIP1) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate, given in Table 12.1.

#### 12.1.2. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock

---

cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction. If more than one interrupt is pending when the CPU exits an ISR, the CPU will service the next highest priority interrupt that is pending.

**Table 12.1. Interrupt Summary**

Interrupt Source	Interrupt Vector	Priority Order	Pending Flags	Bit addressable?	Cleared by HW?	Enable Flag
Reset	0x0000	Top	None	N/A	N/A	Always Enabled
External Interrupt 0 ( <u>INT0</u> )	0x0003	0	IE0 (TCON.1)	Y	Y	EX0 (IE.0)
Timer 0 Overflow	0x000B	1	TF0 (TCON.5)	Y	Y	ET0 (IE.1)
External Interrupt 1 ( <u>INT1</u> )	0x0013	2	IE1 (TCON.3)	Y	Y	EX1 (IE.2)
Timer 1 Overflow	0x001B	3	TF1 (TCON.7)	Y	Y	ET1 (IE.3)
UART0	0x0023	4	RI (SCON0.0) TI (SCON0.1)	Y	N	ES0 (IE.4)
Timer 2 Overflow	0x002B	5	TF2H (TMR2CN.7) TF2L (TMR2CN.6)	Y	N	ET2 (IE.5)
SPI0	0x0033	6	SPIF (SPI0CN.7) WCOL (SPI0CN.6) MODF (SPI0CN.5) RXOVRN (SPI0CN.4)	Y	N	ESPI0 (IE.6)
SMB0	0x003B	7	SI (SMB0CN.0)	Y	N	ESMB0 (EIE1.0)
Port Match	0x0043	8	None	N/A	N/A	EMAT (EIE1.1)
ADC0 Window Compare	0x004B	9	ADWINT (ADC0CN.3)	Y	N	EWADC0 (EIE1.2)
ADC0 Conversion Complete	0x0053	10	ADINT (ADC0CN.5)	Y	N	EADC0 (EIE1.3)
Programmable Counter Array	0x005B	11	CF (PCA0CN.7) CCFn (PCA0CN.n) COVF (PCA0PWM.6)	Y	N	EPCA0 (EIE1.4)
Comparator0	0x0063	12	CPFIF (CPT0CN.4) CPRIF (CPT0CN.5)	N	N	ECP0 (EIE1.5)
Comparator1	0x006B	13	CPFIF (CPT1CN.4) CPRIF (CPT1CN.5)	N	N	ECP1 (EIE1.6)
Timer 3 Overflow	0x0073	14	TF3H (TMR3CN.7) TF3L (TMR3CN.6)	N	N	ET3 (EIE1.7)

## 12.2. Interrupt Control Registers

### Register 12.1. IE: Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name	EA	ESPI0	ET2	ES0	ET1	EX1	ET0	EX0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

**SFR Address: 0xA8 (bit-addressable)**

Table 12.2. IE Register Bit Descriptions

Bit	Name	Function
7	EA	<b>Enable All Interrupts.</b> Globally enables/disables all interrupts and overrides individual interrupt mask settings. 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	ESPI0	<b>Enable SPI0 Interrupt.</b> This bit sets the masking of the SPI0 interrupts. 0: Disable all SPI0 interrupts. 1: Enable interrupt requests generated by SPI0.
5	ET2	<b>Enable Timer 2 Interrupt.</b> This bit sets the masking of the Timer 2 interrupt. 0: Disable Timer 2 interrupt. 1: Enable interrupt requests generated by the TF2L or TF2H flags.
4	ES0	<b>Enable UART0 Interrupt.</b> This bit sets the masking of the UART0 interrupt. 0: Disable UART0 interrupt. 1: Enable UART0 interrupt.
3	ET1	<b>Enable Timer 1 Interrupt.</b> This bit sets the masking of the Timer 1 interrupt. 0: Disable all Timer 1 interrupt. 1: Enable interrupt requests generated by the TF1 flag.
2	EX1	<b>Enable External Interrupt 1.</b> This bit sets the masking of External Interrupt 1. 0: Disable external interrupt 1. 1: Enable interrupt requests generated by the INT1 input.
1	ET0	<b>Enable Timer 0 Interrupt.</b> This bit sets the masking of the Timer 0 interrupt. 0: Disable all Timer 0 interrupt. 1: Enable interrupt requests generated by the TF0 flag.

---

**Table 12.2. IE Register Bit Descriptions**

Bit	Name	Function
0	EX0	<b>Enable External Interrupt 0.</b> This bit sets the masking of External Interrupt 0. 0: Disable external interrupt 0. 1: Enable interrupt requests generated by the INT0 input.

---

## Register 12.2. IP: Interrupt Priority

---

Bit	7	6	5	4	3	2	1	0
Name	Reserved	PSPI0	PT2	PS0	PT1	PX1	PT0	PX0
Type	R	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0

**SFR Address: 0xB8 (bit-addressable)**

**Table 12.3. IP Register Bit Descriptions**

Bit	Name	Function
7	Reserved	Must write reset value.
6	PSPI0	<b>Serial Peripheral Interface (SPI0) Interrupt Priority Control.</b> This bit sets the priority of the SPI0 interrupt. 0: SPI0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.
5	PT2	<b>Timer 2 Interrupt Priority Control.</b> This bit sets the priority of the Timer 2 interrupt. 0: Timer 2 interrupt set to low priority level. 1: Timer 2 interrupt set to high priority level.
4	PS0	<b>UART0 Interrupt Priority Control.</b> This bit sets the priority of the UART0 interrupt. 0: UART0 interrupt set to low priority level. 1: UART0 interrupt set to high priority level.
3	PT1	<b>Timer 1 Interrupt Priority Control.</b> This bit sets the priority of the Timer 1 interrupt. 0: Timer 1 interrupt set to low priority level. 1: Timer 1 interrupt set to high priority level.
2	PX1	<b>External Interrupt 1 Priority Control.</b> This bit sets the priority of the External Interrupt 1 interrupt. 0: External Interrupt 1 set to low priority level. 1: External Interrupt 1 set to high priority level.
1	PT0	<b>Timer 0 Interrupt Priority Control.</b> This bit sets the priority of the Timer 0 interrupt. 0: Timer 0 interrupt set to low priority level. 1: Timer 0 interrupt set to high priority level.
0	PX0	<b>External Interrupt 0 Priority Control.</b> This bit sets the priority of the External Interrupt 0 interrupt. 0: External Interrupt 0 set to low priority level. 1: External Interrupt 0 set to high priority level.

---

### Register 12.3. EIE1: Extended Interrupt Enable 1

---

Bit	7	6	5	4	3	2	1	0
Name	ET3	ECP1	ECP0	EPCA0	EADC0	EWADC0	EMAT	ESMBO
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0

**SFR Address: 0xE6**

**Table 12.4. EIE1 Register Bit Descriptions**

Bit	Name	Function
7	ET3	<b>Enable Timer 3 Interrupt.</b> This bit sets the masking of the Timer 3 interrupt. 0: Disable Timer 3 interrupts. 1: Enable interrupt requests generated by the TF3L or TF3H flags.
6	ECP1	<b>Enable Comparator1 (CP1) Interrupt.</b> This bit sets the masking of the CP1 interrupt. 0: Disable CP1 interrupts. 1: Enable interrupt requests generated by the comparator 1 CPRIF or CPFIF flags.
5	ECP0	<b>Enable Comparator0 (CP0) Interrupt.</b> This bit sets the masking of the CP0 interrupt. 0: Disable CP0 interrupts. 1: Enable interrupt requests generated by the comparator 0 CPRIF or CPFIF flags.
4	EPCA0	<b>Enable Programmable Counter Array (PCA0) Interrupt.</b> This bit sets the masking of the PCA0 interrupts. 0: Disable all PCA0 interrupts. 1: Enable interrupt requests generated by PCA0.
3	EADC0	<b>Enable ADC0 Conversion Complete Interrupt.</b> This bit sets the masking of the ADC0 Conversion Complete interrupt. 0: Disable ADC0 Conversion Complete interrupt. 1: Enable interrupt requests generated by the ADINT flag.
2	EWADC0	<b>Enable Window Comparison ADC0 Interrupt.</b> This bit sets the masking of ADC0 Window Comparison interrupt. 0: Disable ADC0 Window Comparison interrupt. 1: Enable interrupt requests generated by ADC0 Window Compare flag (ADWINT).
1	EMAT	<b>Enable Port Match Interrupts.</b> This bit sets the masking of the Port Match Event interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match.

---

**Table 12.4. EIE1 Register Bit Descriptions**

Bit	Name	Function
0	ESMB0	<b>Enable SMBus (SMB0) Interrupt.</b> This bit sets the masking of the SMB0 interrupt. 0: Disable all SMB0 interrupts. 1: Enable interrupt requests generated by SMB0.

---

#### Register 12.4. EIP1: Extended Interrupt Priority 1

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Bit	7	6	5	4	3	2	1	0
Name	PT3	PCP1	PCP0	PPCA0	PADC0	PWADC0	PMAT	PSMB0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0
<b>SFR Address: 0xF3</b>								

**Table 12.5. EIP1 Register Bit Descriptions**

Bit	Name	Function
7	PT3	<b>Timer 3 Interrupt Priority Control.</b> This bit sets the priority of the Timer 3 interrupt. 0: Timer 3 interrupts set to low priority level. 1: Timer 3 interrupts set to high priority level.
6	PCP1	<b>Comparator1 (CP1) Interrupt Priority Control.</b> This bit sets the priority of the CP1 interrupt. 0: CP1 interrupt set to low priority level. 1: CP1 interrupt set to high priority level.
5	PCP0	<b>Comparator0 (CP0) Interrupt Priority Control.</b> This bit sets the priority of the CP0 interrupt. 0: CP0 interrupt set to low priority level. 1: CP0 interrupt set to high priority level.
4	PPCA0	<b>Programmable Counter Array (PCA0) Interrupt Priority Control.</b> This bit sets the priority of the PCA0 interrupt. 0: PCA0 interrupt set to low priority level. 1: PCA0 interrupt set to high priority level.
3	PADC0	<b>ADC0 Conversion Complete Interrupt Priority Control.</b> This bit sets the priority of the ADC0 Conversion Complete interrupt. 0: ADC0 Conversion Complete interrupt set to low priority level. 1: ADC0 Conversion Complete interrupt set to high priority level.
2	PWADC0	<b>ADC0 Window Comparator Interrupt Priority Control.</b> This bit sets the priority of the ADC0 Window interrupt. 0: ADC0 Window interrupt set to low priority level. 1: ADC0 Window interrupt set to high priority level.
1	PMAT	<b>Port Match Interrupt Priority Control.</b> This bit sets the priority of the Port Match Event interrupt. 0: Port Match interrupt set to low priority level. 1: Port Match interrupt set to high priority level.

---

**Table 12.5. EIP1 Register Bit Descriptions**

Bit	Name	Function
0	PSMB0	<b>SMBus (SMB0) Interrupt Priority Control.</b> This bit sets the priority of the SMB0 interrupt. 0: SMB0 interrupt set to low priority level. 1: SMB0 interrupt set to high priority level.

---

## 13. Power Management and Internal Regulator

All internal circuitry on the C8051F85x/86x devices draws power from the VDD supply pin. Circuits with external connections (I/O pins, analog muxes) are powered directly from the VDD supply voltage, while most of the internal circuitry is supplied by an on-chip LDO regulator. The regulator output is fully internal to the device, and is available also as an ADC input or reference source for the comparators and ADC.

The devices support the standard 8051 power modes: idle and stop. For further power savings in stop mode, the internal LDO regulator may be disabled, shutting down the majority of the power nets on the device.

Although the C8051F85x/86x has idle and stop modes available, more control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

### 13.1. Power Modes

Idle mode halts the CPU while leaving the peripherals and clocks active. In stop mode, the CPU is halted, all interrupts and timers are inactive, and the internal oscillator is stopped (analog peripherals remain in their selected states; the external oscillator is not affected). Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode consumes the least power because the majority of the device is shut down with no clocks active. The Power Control Register (PCON) is used to control the C8051F85x/86x's Stop and Idle power management modes.

#### 13.1.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the hardware to halt the CPU and enter idle mode as soon as the instruction that sets the bit completes execution. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during idle mode.

Idle mode is terminated when an enabled interrupt is asserted or a reset occurs. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

**Note:** If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from Idle mode when a future interrupt occurs. Therefore, instructions that set the IDLE bit should be followed by an instruction that has two or more opcode bytes, for example:

```
// in 'C':  
PCON |= 0x01;                      // set IDLE bit  
PCON = PCON;                        // ... followed by a 3-cycle dummy instruction  
  
; in assembly:  
ORL PCON, #01h                      ; set IDLE bit  
MOV PCON, PCON                       ; ... followed by a 3-cycle dummy instruction
```

If enabled, the Watchdog Timer (WDT) will eventually cause an internal watchdog reset and thereby terminate the idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system.

### 13.1.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the controller core to enter stop mode as soon as the instruction that sets the bit completes execution. Before entering stop mode, the system clock must be sourced by the internal high-frequency oscillator. In stop mode the internal oscillator, CPU, and all digital peripherals are stopped; the state of the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering stop mode. Stop mode can only be terminated by an internal or external reset. On reset, the device performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout.

### 13.2. LDO Regulator

C8051F85x/86x devices include an internal regulator that regulates the internal core and logic supply. Under default conditions, the internal regulator will remain on when the device enters STOP mode. This allows any enabled reset source to generate a reset for the device and bring the device out of STOP mode. For additional power savings, the STOPCF bit can be used to shut down the regulator and the internal power network of the device when the part enters STOP mode. When STOPCF is set to 1, the RST pin and a full power cycle of the device are the only methods of generating a reset.

### 13.3. Power Control Registers

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#### Register 13.1. PCON: Power Control

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Bit	7	6	5	4	3	2	1	0
Name			GF				STOP	IDLE
Type			RW				RW	RW
Reset	0	0	0	0	0	0	0	0
SFR Address: 0x87								

Table 13.1. PCON Register Bit Descriptions

Bit	Name	Function
7:2	GF	<b>General Purpose Flags 5-0.</b> These are general purpose flags for use under software control.
1	STOP	<b>Stop Mode Select.</b> Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0.
0	IDLE	<b>Idle Mode Select.</b> Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0.

---

## 13.4. LDO Control Registers

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### Register 13.2. REG0CN: Voltage Regulator Control

---

Bit	7	6	5	4	3	2	1	0	
Name	Reserved				STOPCF	Reserved			
Type	R				RW	R			
Reset	0	0	0	0	0	0	0	0	
<b>SFR Address: 0xC9</b>									

**Table 13.2. REG0CN Register Bit Descriptions**

Bit	Name	Function
7:4	Reserved	Must write reset value.
3	STOPCF	<b>Stop Mode Configuration.</b> This bit configures the regulator's behavior when the device enters stop mode. 0: Regulator is still active in stop mode. Any enabled reset source will reset the device. 1: Regulator is shut down in stop mode. Only the RST pin or power cycle can reset the device.
2:0	Reserved	Must write reset value.

## 14. Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and-hold and a programmable window detector. These different modes allow the user to trade off speed for resolution. ADC0 also has an autonomous low-power burst mode which can automatically enable ADC0, capture and accumulate samples, then place ADC0 in a low power shutdown mode without CPU intervention. It also has a 16-bit accumulator that can automatically oversample and average the ADC results.

The ADC is fully configurable under software control via several registers. The ADC0 operates in single-ended mode and may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

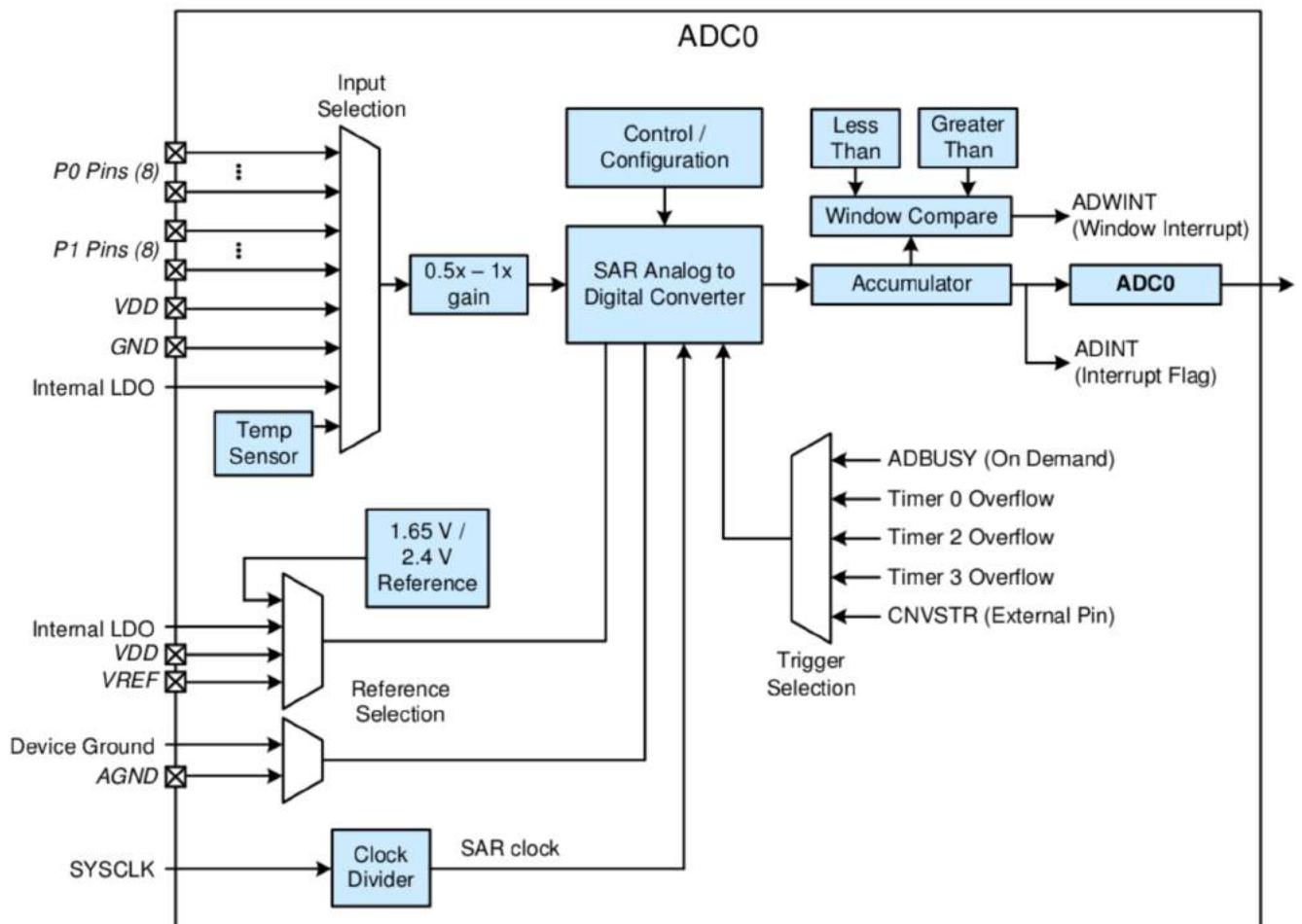


Figure 14.1. ADC0 Functional Block Diagram

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### 14.1. ADC0 Analog Multiplexer

ADC0 on C8051F85x/86x has an analog multiplexer capable of selecting any pin on ports P0 and P1 (up to 16 total), the on-chip temperature sensor, the internal regulated supply, the VDD supply, or GND. ADC0 input channels are selected using the ADC0MX register.

**Table 14.1. ADC0 Input Multiplexer Channels**

ADC0MX setting	Signal Name	QSOP24 Pin Name	QFN20 Pin Name	SOIC16 Pin Name
00000	ADC0.0	P0.0	P0.0	P0.0
00001	ADC0.1	P0.1	P0.1	P0.1
00010	ADC0.2	P0.2	P0.2	P0.2
00011	ADC0.3	P0.3	P0.3	P0.3
00100	ADC0.4	P0.4	P0.4	P0.4
00101	ADC0.5	P0.5	P0.5	P0.5
00110	ADC0.6	P0.6	P0.6	P0.6
00111	ADC0.7	P0.7	P0.7	P0.7
01000	ADC0.8	P1.0	P1.0	P1.0
01001	ADC0.9	P1.1	P1.1	P1.1
01010	ADC0.10	P1.2	P1.2	P1.2
01011	ADC0.11	P1.3	P1.3	P1.3
01100	ADC0.12	P1.4	P1.4	Reserved
01101	ADC0.13	P1.5	P1.5	Reserved
01110	ADC0.14	P1.6	P1.6	Reserved
01111	ADC0.15	P1.7	Reserved	Reserved
10000	Temp Sensor	Internal Temperature Sensor		
10001	LDO	Internal 1.8 V LDO Output		
10010	VDD	VDD Supply Pin		
10011	GND	GND Supply Pin		
10100-11111	None	No connection		

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Important note about ADC0 input configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN and disable the digital driver (PnMDOUT = 0 and Port Latch = 1). To force the crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP.