



Data Sheet

NT35521

One-chip Driver IC without internal GRAM
for 16.7M colors 800RGB x 1280 a-Si TFT LCD
with MIPI Interface

V0.02

Preliminary

REVISION HISTORY	6
1 DESCRIPTION	7
1.1 PURPOSE OF THIS DOCUMENT	7
1.2 GENERAL DESCRIPTION	7
2 FEATURES	8
3 BLOCK DIAGRAM	9
4 PIN DESCRIPTIONS	10
4.1 POWER SUPPLY PINS	10
4.2 MIPI INTERFACE PINS.....	11
4.3 INTERFACE LOGIC PINS	12
4.4 DRIVER OUTPUT PINS.....	14
4.5 DC/DC CONVERTER PINS.....	15
4.6 REGULATOR PINS	16
4.7 LED BACKLIGHT CONTROL PINS.....	17
4.8 TEST PINS	17
5 FUNCTIONAL DESCRIPTIONS	18
5.1 MPU INTERFACE.....	18
5.1.1 Interface Type Selection	18
5.2 MIPI INTERFACE	19
5.2.1 Display Module Pin Configuration for DSI	20
5.2.2 Display Serial Interface (DSI)	21
5.2.2.1 General Description	21
5.2.2.2 Interface Level Communication	21
5.2.2.3 Packet Level Communication.....	38
5.2.2.4 Video Mode Communication	96
5.2.3 System Power-Up and Initialization.....	102
5.3 INTERFACE PAUSE	103
5.4 DATA TRANSFER BREAK AND RECOVERY	104
5.5 TEARING EFFECT INFORMATION.....	105
5.5.1 Tearing Effect Output Line	105
5.5.1.1 Tearing Effect Line Modes	105
5.6 POWER ON/OFF SEQUENCE	107
5.6.1 Power On Sequence.....	108
5.6.2 Power Off Sequence	114
5.6.3 Uncontrolled Power Off	120

5.7 POWER LEVEL MODES.....	121
5.7.1 Definition.....	121
5.7.2 Power Level Mode Flow Chart.....	122
5.8 RESET FUNCTION	124
5.8.1 Register Default Value	124
5.8.2 Output or I/O Pins.....	125
5.8.3 Input Pins.....	125
5.9 SLEEP OUT-COMMAND AND SELF-DIAGNOSTIC FUNCTIONS OF THE DISPLAY MODULE.....	126
5.9.1 Register loading Detection.....	126
5.9.2 Functionality Detection.....	127
5.10 GAMMA FUNCTION	128
5.11 BASIC DISPLAY MODE	129
5.12 INSTRUCTION SETTING SEQUENCE	130
5.12.1 Sleep In/Out Sequence	130
5.12.2 Deep Standby Mode Enter/Exit Sequence.....	131
5.13 INSTRUCTION SETUP FLOW	132
5.13.1 Initializing with the Built-in Power Supply Circuits.....	132
5.13.2 Power OFF Sequence	133
5.14 MTP WRITE SEQUENCE.....	134
5.15 COLUMN, 1-DOT, 2-Dot, 3-Dot, 4-DOT AND Z INVERSION (VCOM DC DRIVE).....	135
5.16 DYNAMIC BACKLIGHT CONTROL FUNCTION.....	136
5.16.1 PWM Control Architecture.....	138
5.16.2 Dimming Function for CABC/Force PWM Function and Manual Brightness Control	141
5.16.3 PWM Signal Setting for CABC.....	143
5.16.4 Content Adaptive Brightness Control (CABC).....	145
6 COMMAND DESCRIPTIONS	146
6.1 USER COMMAND SET	146
NOP (00h).....	148
SWRESET: Software Reset (01h).....	149
RDDID: Read Display ID (04h).....	150
RDNUMED: Read Number of Errors on DSI (05h).....	151
RDDPM: Read Display Power Mode (0Ah)	152
RDDMADCTL: Read Display MADCTL (0Bh)	153
RDDCOLMOD: Read Display Pixel Format (0Ch)	154
RDDIM: Read Display Image Mode (0Dh).....	155

RDDSM: Read Display Signal Mode (0Eh)	156
RDDSDR: Read Display Self-Diagnostic Result (0Fh)	157
SLPIN: Sleep In (10h)	158
SLPOUT: Sleep Out (11h)	160
NORON: Normal Display Mode On (13h)	162
INVOFF: Display Inversion Off (20h)	163
INVON: Display Inversion On (21h)	164
ALLPOFF: All Pixel Off (22h)	165
ALLPON: All Pixel On (23h)	166
GAMSET: Gamma Set (26h)	168
DISPOFF: Display Off (28h)	169
DISPON: Display On (29h)	170
TEOFF: Tearing Effect Line OFF (34h)	171
TEON: Tearing Effect Line ON (35h)	172
MADCTL: Memory Data Access Control (36h)	173
IDMOFF: Idle Mode Off (38h)	175
IDMON: Idle Mode On (39h)	176
COLMOD: Interface Pixel Format (3Ah)	178
STESL: Set Tearing Effect Scan Line (44h)	179
GSL: Get Scan Line (45h)	180
DSTBON: Deep Standby Mode On (4Fh)	181
WRDISBV: Write Display Brightness (51h)	182
RDDISBV: Read Display Brightness (52h)	183
WRCTRLD: Write CTRL Display (53h)	184
RDCTRLD: Read CTRL Display Value (54h)	186
WRCABC: Write Content Adaptive Brightness Control (55h)	188
RDCABC: Read Content Adaptive Brightness Control (56h)	190
WRCABCMB: Write CABC minimum brightness (5Eh)	192
RDCABCMB: Read CABC minimum brightness (5Fh)	193
RDDDBS: Read DDB Start (A1h)	194
RDDDBC: Read DDB Continue (A8h)	196
RDID1: Read ID1 Value (DAh)	198
RDID2: Read ID2 Value (DBh)	199
RDID3: Read ID3 Value (DCh)	200
7 SPECIFICATIONS	201

7.1 ABSOLUTE MAXIMUM RATINGS.....	201
7.2 DC CHARACTERISTICS	202
7.2.1 <i>Basic Characteristics</i>	202
7.2.2 <i>MIPI Characteristics</i>	204
7.2.2.1 <i>DC Characteristics for DSI LP Mode</i>	204
7.2.2.2 <i>DC Characteristics for DSI HS Mode</i>	205
7.3 AC CHARACTERISTICS	206
7.3.1 <i>MIPI DSI Timing Characteristics</i>	206
7.3.1.1 <i>High Speed Mode</i>	206
7.3.1.2 <i>Low Power Mode</i>	207
7.3.1.3 <i>DSI Bursts</i>	208
7.3.2 <i>Reset Input Timing</i>	210
7.3.3 <i>Deep Standby Mode Timing</i>	211
8 REFERENCE APPLICATIONS.....	212
8.1 MICROPROCESSOR INTERFACE.....	212
8.2 CONNECTIONS WITH PANEL.....	213
8.2.1 <i>Connection for Panel with Column/Dot Inversion.</i>	213

NOVATEK CONFIDENTIAL
NO DISCLOSURE

REVISION HISTORY

Version	Contents	Prepared by	Checked by	Approved by	Date
0.00	Initial Version	Teresa	Charley		2012/2/22
0.01	Preliminary Version	S W Luoh	Eason Johnny	Dennis	2012/5/3
0.02	1. remove VGHO/VGLO & update LVGLGOUT (section 3 & 4.4) 2. not support TE trigger (section 5.2.2.2.3.2 & 5.2.2.3.3.1) 3. update min line time tL (section 5.2.2.4.5) 4. add RID[15:0] for DDB (Table 6.1.1 & command A1h, A8h) 5. add 36h command & update 0Bh command (section 5.8.1 & 6.1) 6. remove command 06h~08h (section 5.8.1 & 6.1) 7. update note and timing for DSTB (section 5.12.2 & 7.3.3) 8. update MTP_PWR voltage range (section 4.1) 9. update PWM figure (section 5.16.1) 10. update MTP Write Sequence flaw 11. Add Power Off Sequence t15 for wait time when screen clear	S.W Luoh Johnny	S.W Luoh Henry	Dennis Kuo	2012/9/20

NOVATEK CONFIDENTIAL
NO DISCLOSURE

1 DESCRIPTION

1.1 Purpose of this Document

This document has been created to provide complete reference specifications for the NT35521. IC design engineers should refer to these specifications when designing ICs, test engineers when testing the compliance of manufactured ICs to guarantee their performance, and application engineers when helping customers to make sure they are using this IC properly.

1.2 General Description

The NT35521 device is a single-chip solution for a-Si TFT LCD that incorporates gate drivers and is capable of 800RGBx1280, 768RGBx1280, 720RGBx1280, 640RGBx1024, 600RGBx1024 and 540RGB x 960 without internal CGRAM. It includes a timing controller with glass interface level-shifters and a glass power supply circuit.

The NT35521 supports MIPI Interface only.

The NT35521 is also able to make gamma correction settings separately for RGB dots to allow benign adjustments to panel characteristics, resulting in higher display qualities.

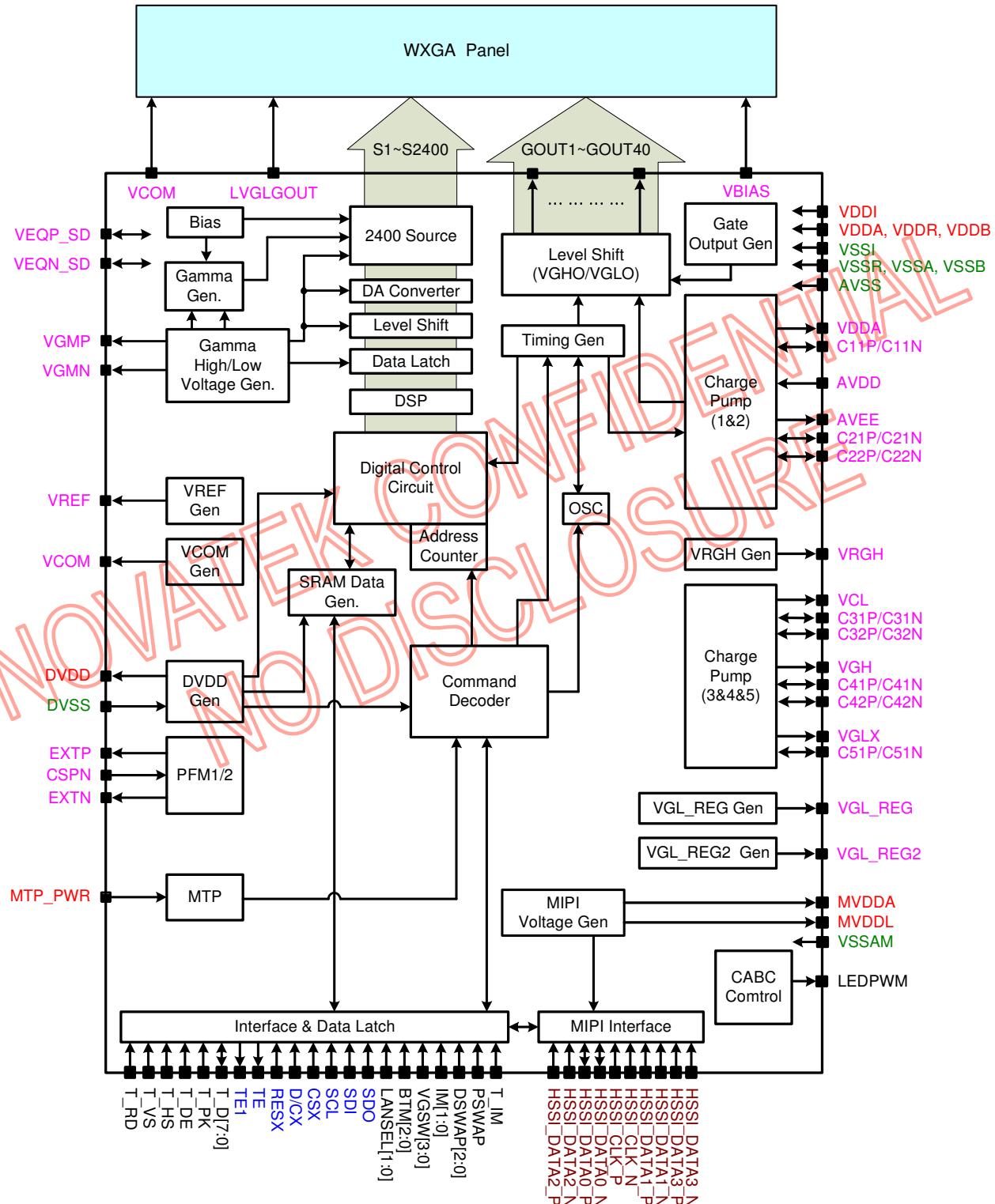
This LSI is suitable for small or medium-sized portable mobile solutions requiring long-term driving capabilities, including bi-directional pagers, digital audio players, cellular phones and handheld PDA.

NOVATEK CONFIDENTIAL
NO DISCLOSURE

2 FEATURES

- ◆ Single chip WXGA a-Si TFT LCD Controller/driver without Display RAM.
- ◆ Display resolution option
 - 800RGB x (480 + 4 x NL)
 - 768RGB x (480 + 4 x NL)
 - 720RGB x (480 + 4 x NL)
 - 640RGB x (480 + 4 x NL)
 - 600RGB x (480 + 4 x NL)
 - 540RGB x (480 + 4 x NL)
- ◆ Display mode (Color mode)
 - Full color mode: 16.7M-colors
 - Reduce color mode: 262K colors
 - Reduce color mode: 65K colors
 - Idle mode: 8-colors
- ◆ Interface
 - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0, 1 clock and 2, 3 or 4 data lane pairs)
- ◆ Display features
 - Individual gamma correction setting for RGB dots
 - Deep standby function
- ◆ On chip
 - VGHO/VGLO voltage generator for gate control signal and panel
 - Oscillator for display clock
 - Supports gate control signals to gate driver in the panel
 - Content Adaptive Brightness Control (CABC)
 - Image Enhancement (IE): include brightness/edge/vivid color enhancement
 - Sunlight Readability Enhancement (SRE)
- ◆ Supply voltage range (refer to the pin description of BTM[2:0])
 - I/O supply voltage range for VDDI to VSSI: 1.65V ~ 3.6V
 - Analog supply voltage range for VCI to VSS: 2.5V ~ 3.6V
 - Analog supply voltage range for AVDD to AVSS: 4.5V ~ 6.0V
 - Analog supply voltage range for AVEE to AVSS: -4.5V ~ -6.0V
 - Analog supply voltage range for VCL to AVSS: -2.5V ~ -4.0V
- ◆ Output voltage levels
 - Positive gate driver voltage range for VGH: 7 ~ 20V (AVDD-VCL ~ 2xAVDD-2xAVEE)
 - Positive gate driver voltage range for VRGH: 3 ~ 17V (VGH-1.0V)
 - Negative gate driver voltage range for VGLX: -7 ~ -15V (AVEE+VCL ~ 2xAVEE-AVDD)
 - Negative gate driver voltage range for VGL_REG, VGL_REG2: -3 ~ -14V (VGLX+1.0V)
 - Step-up 1 output voltage range for AVDD: 4.5 ~ 6.3V
 - Step-up 2 output voltage range for AVEE: -4.5 ~ -6.3V
 - Positive gamma high voltage range for VGMP: 3.0 ~ 6.0V (AVDD-0.5V)
 - Positive gamma low voltage range for VGSP: 0, 0.3 ~ 3.3V
 - Negative gamma high voltage range for VGMN: -3.0 ~ -6.0V (AVEE+0.5V)
 - Negative gamma low voltage range for VGSN: 0, -0.3 ~ -3.3V
 - Common electrode voltage range for VCOM: 0, -0.3 ~ -3.5V (VCL+0.5V)

3 BLOCK DIAGRAM



4 PIN DESCRIPTIONS

4.1 Power Supply Pins

Symbol	Name	Description
VDBB	DC/DC Power	Power supply for DC/DC converter. Please refer the description of pin BTM[2:0] for the voltage connection.
VDDA	Analog Power	Power supply for analog system. Please refer the description of pin BTM[2:0] for the voltage connection.
VDDR	Regulator Power	Power supply for regulator system Please refer the description of pin BTM[2:0] for the voltage connection.
VDDI	I/O Power	Power supply for interface system except MIPI interface pin.
VSSB	DC/DC GND	System ground for DC/DC converter.
VSSA	Analog GND	System ground for analog system.
VSSR	Regulator GND	System ground for regulator system.
VSSAM	MIPI GND	System ground for internal MIPI analog system.
VSSI	I/O GND	System ground for interface system except MIPI interface.
DVSS	Digital GND	System ground for internal digital system.
AVSS	Source OP GND	System ground for source OP system.
MTP_PWR	MTP Power	MTP programming power supply pin (7.5~8.0V and 7.75V typical). Must be left open or connected to DVSS in normal condition.

4.2 MIPI Interface Pins

Symbol	I/O	Description
HSSI_CLK_P HSSI_CLK_N	I	<ul style="list-style-type: none"> -These pins are DSI-CLK+/- differential clock signals if MIPI interface is used. -HSSI_CLK_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM. -When Driver IC enter to ULPM or Deep Standby Mode, please keep these pins to low.
HSSI_D0_P HSSI_D0_N	I/O	<ul style="list-style-type: none"> -These pins are DSI-D0+/- differential data signals if MIPI interface is used. -HSSI_D0_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM. -When Driver IC enter to ULPM or Deep Standby Mode, please keep these pins to low.
HSSI_D1_P HSSI_D1_N	I	<ul style="list-style-type: none"> -These pins are DSI-D1+/- differential data signals if MIPI interface is used. -HSSI_D1_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM. -When Driver IC enter to ULPM or Deep Standby Mode, please keep these pins to low.
HSSI_D2_P HSSI_D2_N	I	<ul style="list-style-type: none"> -These pins are DSI-D2+/- differential data signals if MIPI interface is used. -HSSI_D2_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM. -When Driver IC enter to ULPM or Deep Standby Mode, please keep these pins to low.
HSSI_D3_P HSSI_D3_N	I	<ul style="list-style-type: none"> -These pins are DSI-D3+/- differential data signals if MIPI interface is used. -HSSI_D3_P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM. -When Driver IC enter to ULPM or Deep Standby Mode, please keep these pins to low.

NOVATEK CONFIDENTIAL
NO DISCLOSURE

4.3 Interface Logic Pins

Symbol	I/O	Description									
RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.									
IM[1:0]	I	Interface type selection.									
		IM[1:0]	Display Data				Command				
		00	reserved				reserved				
		01	reserved				reserved				
		10	reserved				reserved				
LANSEL[1:0]	I	Input pin to select number of data lanes in MIPI interface.									
		LANSEL[1:0]	Data Lane of MIPI								
		00	reserved								
		01	2 data lanes								
		10	3 data lanes								
DSWAP[2:0] PSWAP	I	Input pin to select HSSI_D0/D1/D2/D3 data lane sequence and polarity in MIPI interface.									
		Pin Name		HSSI_D0_N	HSSI_D0_P	HSSI_D1_N	HSSI_D1_P	HSSI_CLK_N	HSSI_CLK_P	HSSI_D2_N	HSSI_D2_P
		PSWAP =1		DSWAP[2:0]=000	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-
		DSWAP[2:0]=001		D2-	D2+	D0-	D0+	CLK-	CLK+	D1-	D1+
		DSWAP[2:0]=010		D3-	D3+	D1-	D1+	CLK-	CLK+	D0-	D0+
DSWAP[2:0] PSWAP	I	DSWAP[2:0]=011		D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+
		DSWAP[2:0]=100		D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+
		DSWAP[2:0]=101		D3-	D3+	D1-	D1+	CLK-	CLK+	D2-	D2+
		DSWAP[2:0]=110		D0-	D0+	D2-	D2+	CLK-	CLK+	D1-	D1+
		DSWAP[2:0]=111		D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+
PSWAP =0	I	DSWAP[2:0]=000		D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-
		DSWAP[2:0]=001		D2+	D2-	D0+	D0-	CLK+	CLK-	D1+	D1-
		DSWAP[2:0]=010		D3+	D3-	D1+	D1-	CLK+	CLK-	D0+	D0-
		DSWAP[2:0]=011		D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-
		DSWAP[2:0]=100		D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-
BTM[2:0]	I	Note: The D2+/- and D3+/- are unused when LANSEL[1:0] = "01" and D3+/- is unused when LANSEL[1:0] = "10".									
		Boost mode selection for VCL, AVDD and AVEE.									
		BTM[2:0]		VDDI	VDDA	VDDR / VDBB	VCL	AVDD		AVEE	
		000	VDDI	VCI	VCI		Internal	Internal PFM		Internal PFM	
		001	VDDI	VCI	VCI		Internal	Internal PFM		Internal CP	
BTM[2:0]	I	010	VDDI	Internal	AVDD		Internal	AVDD		Internal PFM	
		011	VDDI	Internal	AVDD		Internal	AVDD		Internal CP	
		100	VDDI	Internal	AVDD		Internal	AVDD		AVEE	
		101	VDDI	VCI	AVDD		Internal	AVDD		AVEE	
		110	VDDI	VCI	AVDD		VCL	AVDD		AVEE	
		Note: The VDDI, VCI, VCL, AVDD and AVEE in above table mean external input voltage power.									

Symbol	I/O	Description
VGSW[3:0]	I	Input pin to select the different panel application.
TE	O	Frame head pulse signal, activated by S/W command. Utilize this signal when synchronizing display data write operations. <u>This pin is output low when it is not activated. If not used, please open this pin.</u>
TE1	O	The pulse output per scan line signal for noise sensing of TP. <u>This pin is output low when it is not activated. If not used, please open this pin.</u>

Note: "1" = VDDI level, "0" = VSSI level.

NOVATEK CONFIDENTIAL
NO DISCLOSURE

4.4 Driver Output Pins

Symbol	I/O	Description	
S1 ~ S2400	O	Pixel electrode driving output. The used source pins for different display resolution is shown below.	
		Display Resolution	Used Source Pins
		800RGB	S1~S2400
		768RGB	S1~S1152 and S1249~S2400
		720RGB	S1~S1080 and S1321~S2400
		640RGB	S1~S960 and S1441~S2400
		600RGB	S1~S900 and S1501~S2400
		540RGB	S1~S810 and S1591~S2400
SDUM0~3	O	Dummy Source, leave it Open if not used.	
GOUT1 ~ GOUT42, LVGLGOUT	O	Gate control signals for panel. The swing voltage level is VGH for high level and VGLX, VGL_REG or VGL_REG2 for low level.	
VBIAS	O	High voltage level for gate circuit of panel. This voltage is output VRGH level.	

NOVATEK CONFIDENTIAL
NO DISCLOSURE

4.5 DC/DC Converter Pins

Symbol	I/O	Description
AVDD	O	Output voltage from step-up circuit 1, generated from Vddb. Connect a capacitor for stabilization.
AVEE	O	Output voltage from step-up circuit 2, generated from Vddb or AVDD (refer to BTM[2:0]). Connect a capacitor for stabilization.
VCL	O	Output voltage from step-up circuit 3, generated from Vddb or AVDD (refer to BTM[2:0]). Connect a capacitor for stabilization.
VGH	O	Output voltage from step-up circuit 4. Connect a capacitor for stabilization.
VGLX	O	VGLX is output voltage from step-up circuit 5. Connect a capacitor for stabilization.
C11P, C11N	I/O	Capacitor connection pins for the step-up circuit which generate VDDA (refer to BTM[2:0]). Connect capacitor as requirement. When not in used, please open these pins.
C21P, C21N C22P, C22N	I/O	Capacitor connection pins for the step-up circuit which generate AVEE. Connect capacitor as requirement. When not in used, please open these pins.
C31P, C31N C32P, C32N	I/O	Capacitor connection pins for the step-up circuit which generate VCL. Connect capacitor as requirement. When not in used, please open these pins.
C41P, C41N C42P, C42N	I/O	Capacitor connection pins for the step-up circuit which generate VGH. Connect capacitor as requirement.
C51P, C51N	I/O	Capacitor connection pins for the step-up circuit which generate VGLX. Connect capacitor as requirement.
EXTP	O	- PFM1 control output for DC/DC converter to generate AVDD when BTM[2:0] = "000"~"011". - Connect to gate of external NMOS device. - Enable signal for NT50198 power IC or external DC/DC when BTM[2:0] = "100"~"110". When not in use, please open this pin.
EXTN	O	- PFM2 control output for DC/DC converter to generate AVEE when BTM[2:0] = "000"~"011". - Connect to gate of external PMOS device. - Control signal for NT50198 power IC when BTM[2:0] = "100"~"110". When not in use, please open this pin.
CSPN	I	Current sensing input for PFM1 and PFM2 DC/DC converter. When not in use, please connect to VSSB.

4.6 Regulator Pins

Symbol	I/O	Description
VRGH	O	Regulator output voltage generated from VGH. Connect a capacitor for stabilization. When not in use, please open this pin.
VGL_REG	O	Regulator output voltage generated from VGLX. Connect a capacitor for stabilization. When not in use, please open this pin.
VGL_REG2	O	Regulator output voltage generated from VGLX. Connect a capacitor for stabilization. When not in use, please open this pin.
VGMP	O	Regulator output voltage generated from AVDD (for positive gamma high voltage generator). Connect a capacitor for stabilization.
VGMN	O	Regulator output voltage generated from AVEE (for negative gamma high voltage generator). Connect a capacitor for stabilization.
VCOM	O	Regulator output generated from VCL (for common voltage of panel). Connect a capacitor for stabilization.
DVDD	O	Regulator output for logic system power. Connect a capacitor for stabilization.
MVDDA	O	Regulator output for internal MIPI analog system. Connect a capacitor for stabilization. If not use MIPI interface, please open this pin.
MVDDL	O	Regulator output for internal MIPI low power system. Connect a capacitor for stabilization. If not use MIPI interface, please open this pin.
VREF	O	Regulator output for internal reference voltage. Connect a capacitor for stabilization.
VEQP_SD	I/O	Positive voltage for source EQ. Connect a capacitor for charge sharing.
VEQN_SD	I/O	Negative voltage for source EQ. Connect a capacitor for charge sharing.

4.7 LED Backlight Control Pins

Symbol	I/O	Description
LEDPWM	O	This pin is connected to the external LED driver. It is a PWM type control signal for brightness of the LED backlight. The width of LEDPWM signal is set from 256 values between 0% (Low) and 100% (High) If not used, please open this pin.

4.8 Test Pins

Symbol	I/O	Description
T_VS	I	Test pin, not accessible to user. <i>This pin has internal pull-down resistor. Can be left open or connected to VSSI.</i>
T_HS	I	Test pin, not accessible to user. <i>This pin has internal pull-down resistor. Can be left open or connected to VSSI.</i>
T_DE	I	Test pin, not accessible to user. <i>This pin has internal pull-down resistor. Can be left open or connected to VSSI.</i>
T_PK	I	Test pin, not accessible to user. <i>This pin has internal pull-down resistor. Can be left open or connected to VSSI.</i>
T_D7~0	I/O	Test pin, not accessible to user. <i>These pins have internal pull-down resistor. Can be left open or connected to VSSI.</i>
T_IM	I	Test pin, not accessible to user. <i>This pin has internal pull-down resistor. Can be left open or connected to VSSI.</i>
T_RD	I	Test pin, not accessible to user. <i>This pin has internal pull-up resistor. Can be left open or connected to VDDI.</i>
CSX	I	Test pin, not accessible to user. Must be connected to VDDI.
DC/X	I	Test pin, not accessible to user. Must be connected to VDDI.
SCL	I	Test pin, not accessible to user. Must be connected to VDDI.
SDI	I	Test pin, not accessible to user. Must be connected to VDDI.
SDO	O	Test pin, not accessible to user. Must be left open.
OSC_MIPI	I/O	Test pin, not accessible to user. Must be left open.
TEST0~7	I/O	Test pin, not accessible to user. Must be left open.
TS0~7	I/O	Test pin, not accessible to user. Must be left open.
VSSBDUM2~3	O	These pins are dummy with VSSB potential (not have any function inside). Signal traces can't pass through on glass under these pads.
AVSSDUM4~63	O	These pins are dummy with AVSS potential (not have any function inside). Signal traces can't pass through on glass under these pads.

5 FUNCTIONAL DESCRIPTIONS

5.1 MPU Interface

NT35521 can interface with MPU at high speed. However, if the interface cycle time is faster than the limit, MPU needs to have dummy wait(s) to meet the cycle time limit.

5.1.1 Interface Type Selection

The selection of a given interfaces are done by setting IM1 and IM0 pins as show in **Table 5.1.1**

Table 5.1.1 Interface Type Selection

IM1	IM0	SRAM	Register
0	0	reserved	reserved
0	1	reserved	reserved
1	0	reserved	reserved
1	1	MIPI DSI, HSSI_D0_P/N, HSSI_D3_P/N	MIPI DSI, HSSI_D0_P/N, HSSI_D3_P/N

Note: "X" = Don't care.

NOVATEK CONFIDENTIAL
NO DISCLOSURE

5.2 MIPI Interface

The Display Serial Interface standard defines protocols between a host processor and peripheral devices that adhere to MIPI Alliance standards for mobile device interfaces. The DSI standard builds on existing standards by adopting pixel formats and command set defined in MIPI Alliance standards.

DSI-compliant peripherals support either of two basic modes of operation: Command Mode and Video Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display interconnect, but are not intended to restrict DSI from operating in other applications.

Typically, a peripheral is capable of Command Mode operation or Video Mode operation. Some Video Mode display modules also include a simplified form of Command Mode operation in which the display module may refresh its screen from a reduced-size, or partial, frame buffer, and the interface (DSI) to the host processor may be shut down to reduce power consumption.

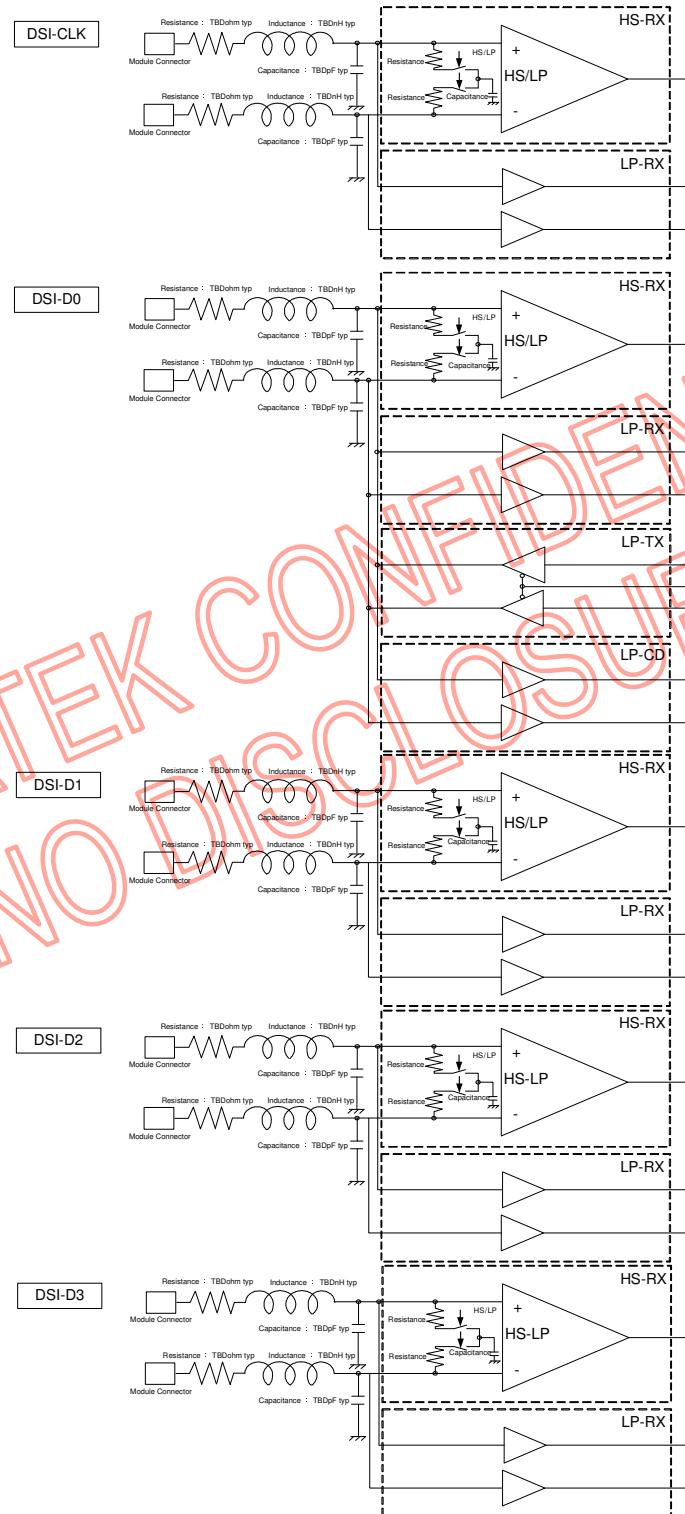
Command Mode refers to operation in which transactions primarily take the form of sending commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

Video Mode refers to operation in which transfers from the host processor to the peripheral take the form of a real-time pixel stream. In normal operation, the display module relies on the host processor to provide image data at sufficient bandwidth to avoid flicker or other visible artifacts in the displayed image. Video information should only be transmitted using High Speed Mode. Some Video Mode architectures may include a simple timing controller and partial frame buffer, used to maintain a partial-screen or lower-resolution image in standby or Low Power Mode. This permits the interface to be shut down to reduce power consumption. To reduce complexity and cost, systems that only operate in Video Mode may use a unidirectional data path.

Configuration:

Lane Pair	MCU (Master)	Display Module (Slave)
Clock Lane	Unidirectional Lane	<ul style="list-style-type: none"> ■ Clock Only ■ Escape Mode(ULPS Only)
Data Lane 0	Bi-directional Lane	<ul style="list-style-type: none"> ■ Forward High-Speed ■ Bi-directional Escape Mode ■ Bi-directional LPDT
Data Lane 1 Data Lane 2 Data Lane 3	Unidirectional Lane	<ul style="list-style-type: none"> ■ Forward High-Speed ■ Escape Mode (ULPM only) ■ No LPDT

5.2.1 Display Module Pin Configuration for DSI



5.2.2 Display Serial Interface (DSI)

5.2.2.1 General Description

Communication sequences between the MCU and the display module are described on chapter “5.2.2.3.3 Communication Sequences”.

The communication can be separated 2 different levels between the MCU and the display module:

- Low level communication what is done on the interface level
- High level communication what is done on the packet level

5.2.2.2 Interface Level Communication

5.2.2.2.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disabled (A termination resistor of the receiver is disabled) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enabled) are not used in the single end mode. There are used different modes and protocol in each mode when there is wanted to transfer information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed(HS)	Low-Power(LP)	
	Dn+ line	Dn- line		Burst Mode	Control Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

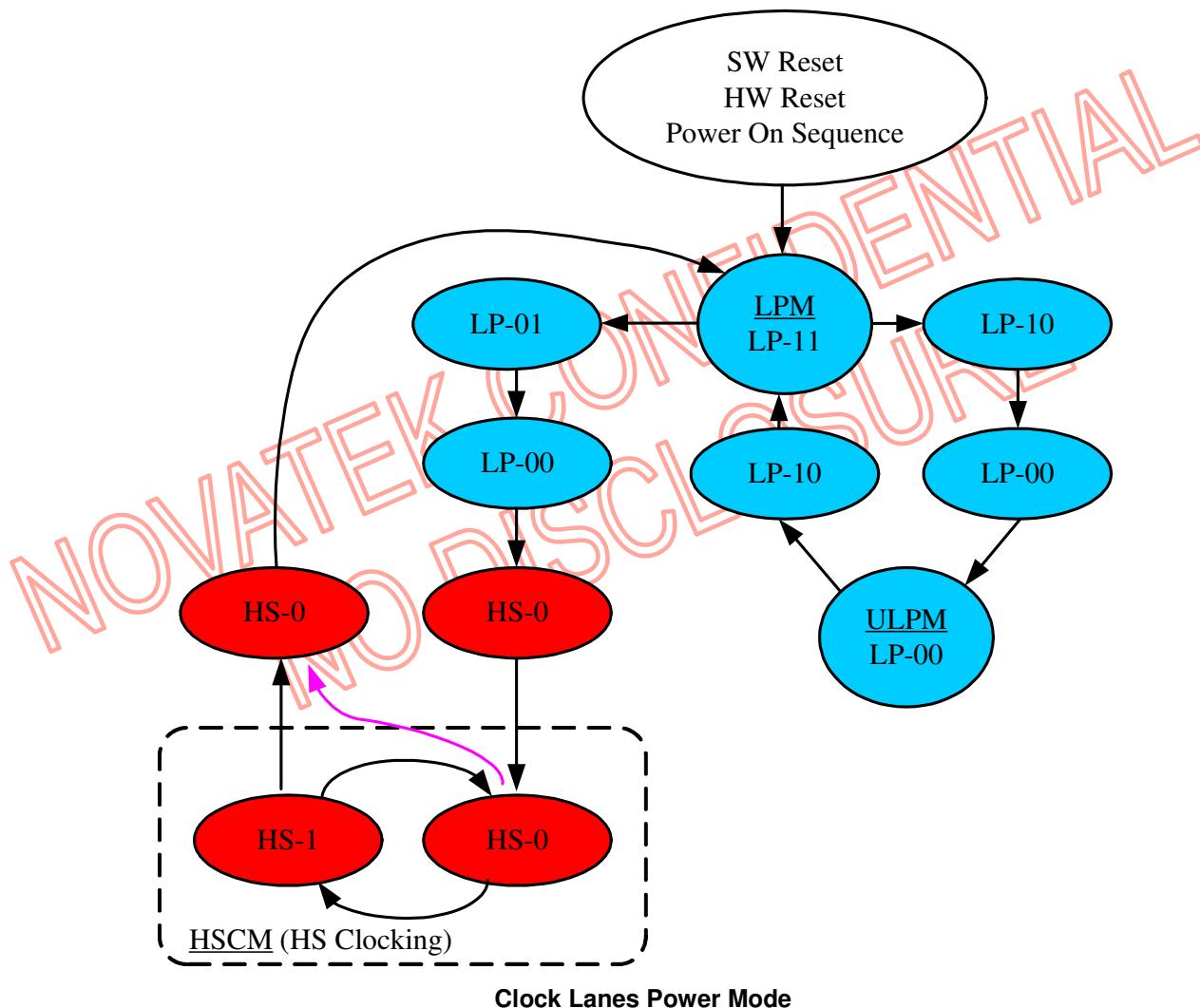
Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

5.2.2.2.2 DSI-CLK Lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM). Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode (LPM) or Ultra Low Power Mode (ULPM). Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving out High Speed Clock Mode (HSCM). These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

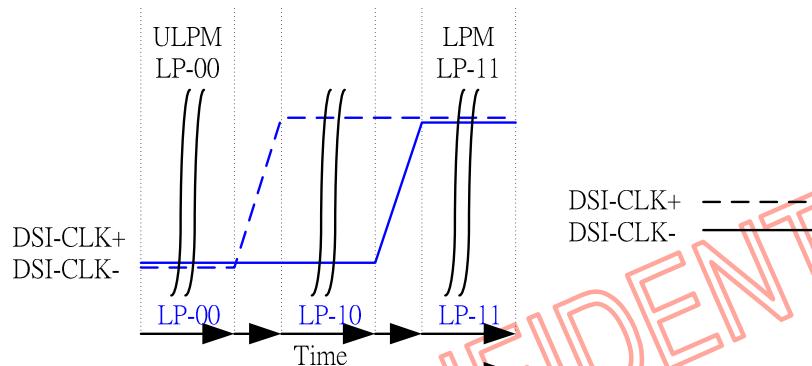
The principle flow chart of the different clock lanes power modes is illustrated below.



5.2.2.2.1 Low Power Mode (LPM)

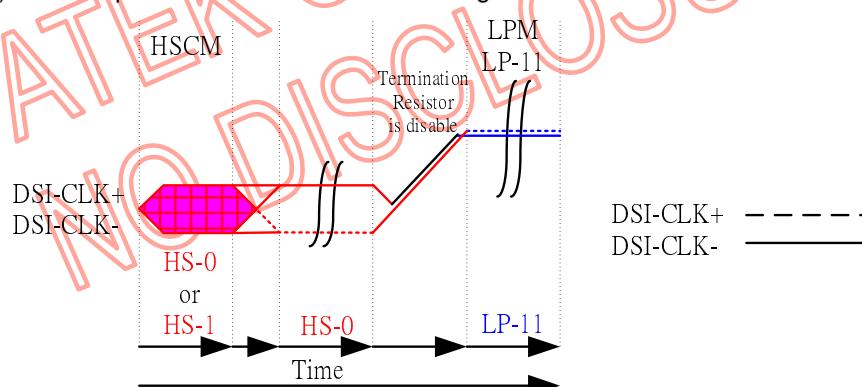
DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence =>LP-11
- 2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.



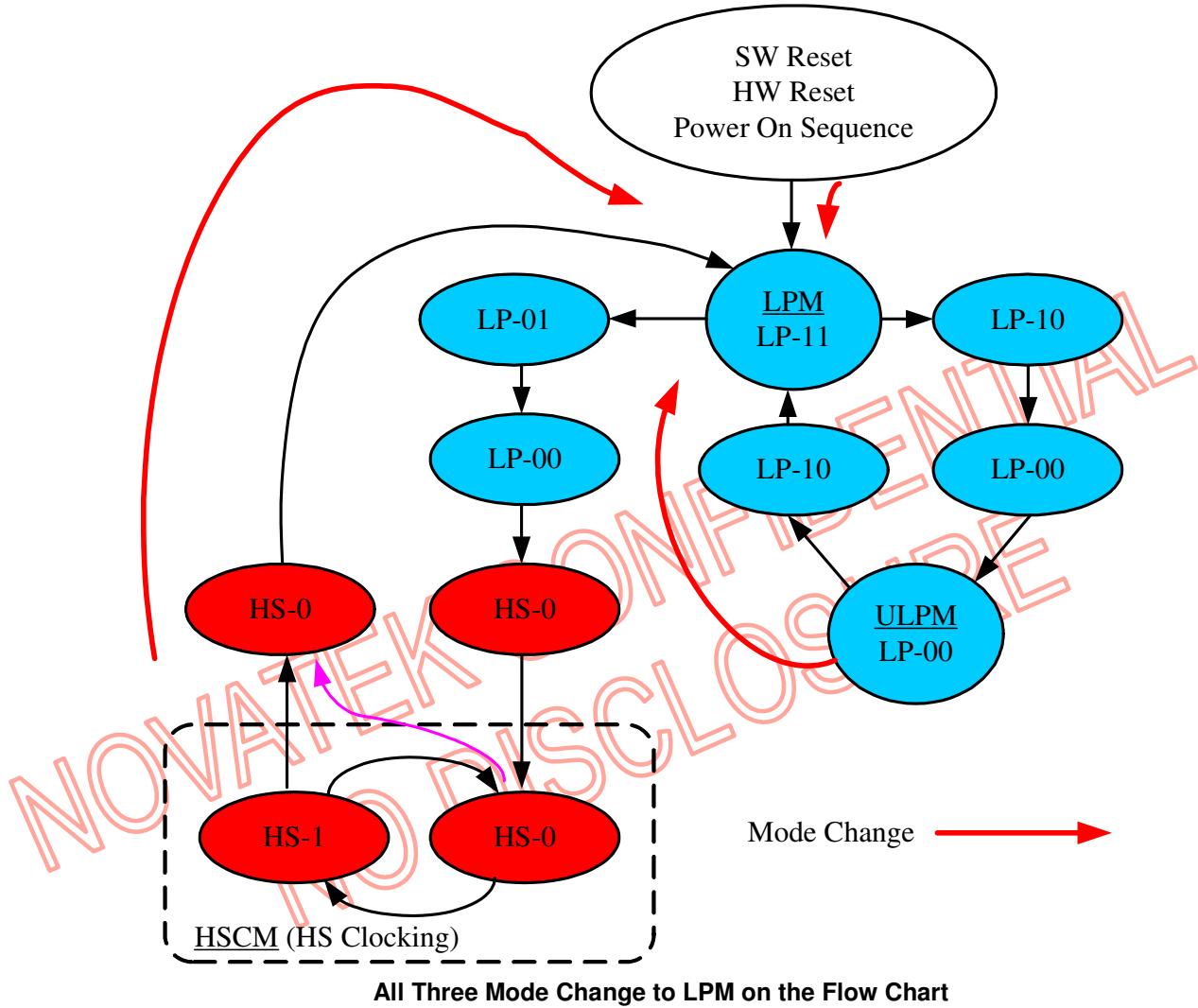
From ULPM to LPM

- 3) After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) =>HS-0 =>LP-11 (LPM). This sequence and all three mode changes are illustrated below.



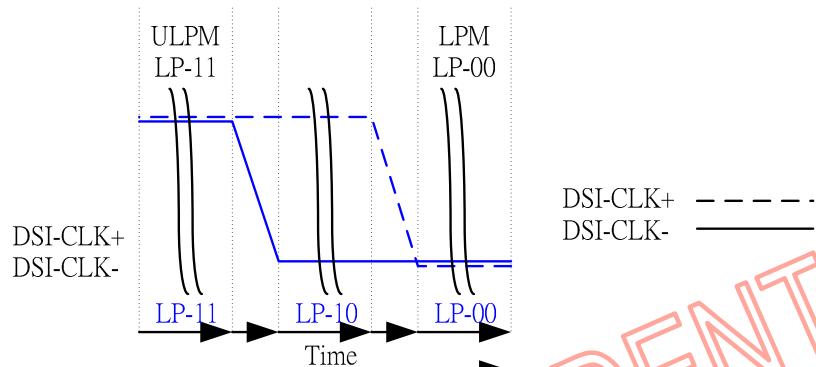
From High Speed Clock Mode (HSCM) to LPM

All three mode changes are illustrated a flow chart below.



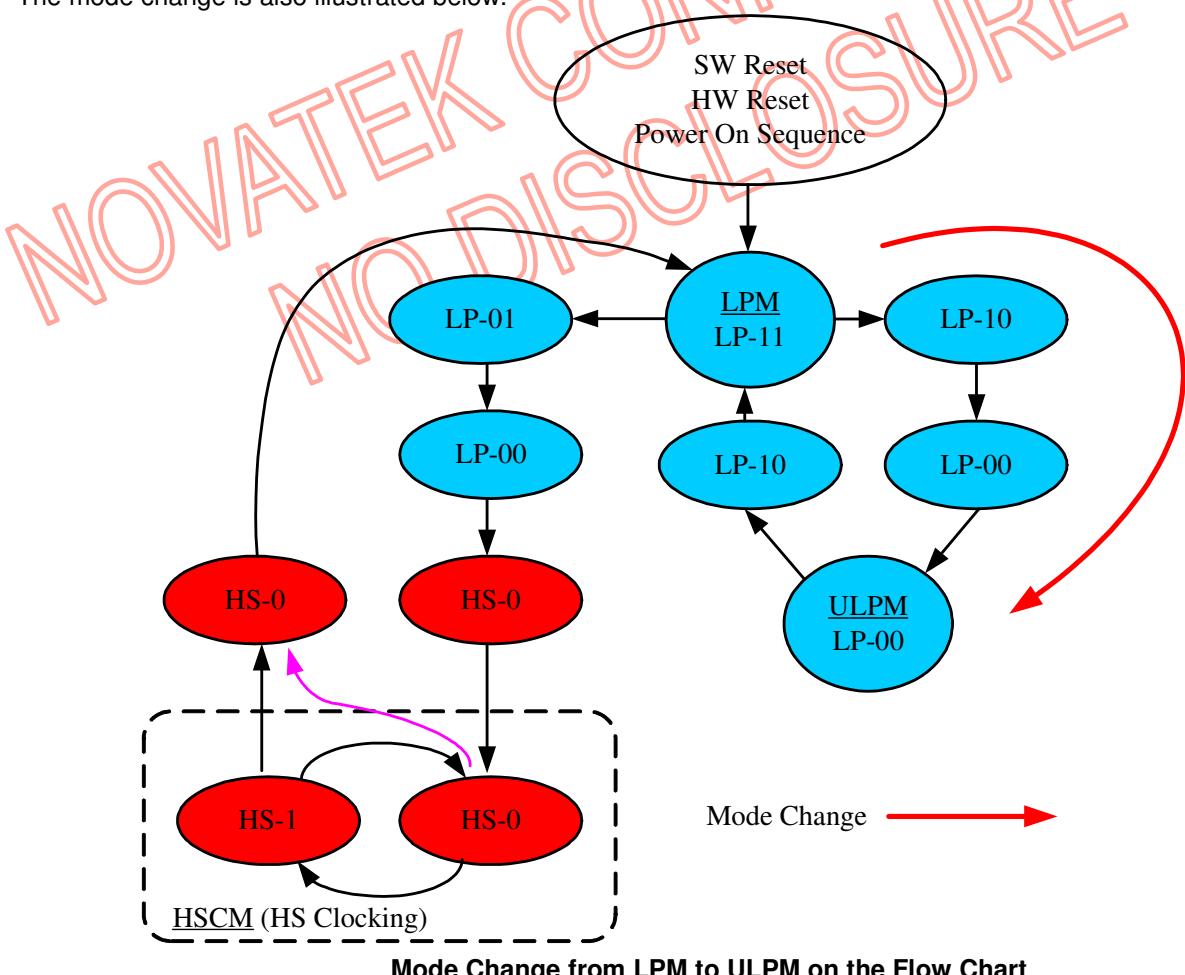
5.2.2.2.2 Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the Ultra Low power Mode (ULPM), when DSI-CLK lanes are entering LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-10 =>LP-00 (ULPM). This sequence is illustrated below.



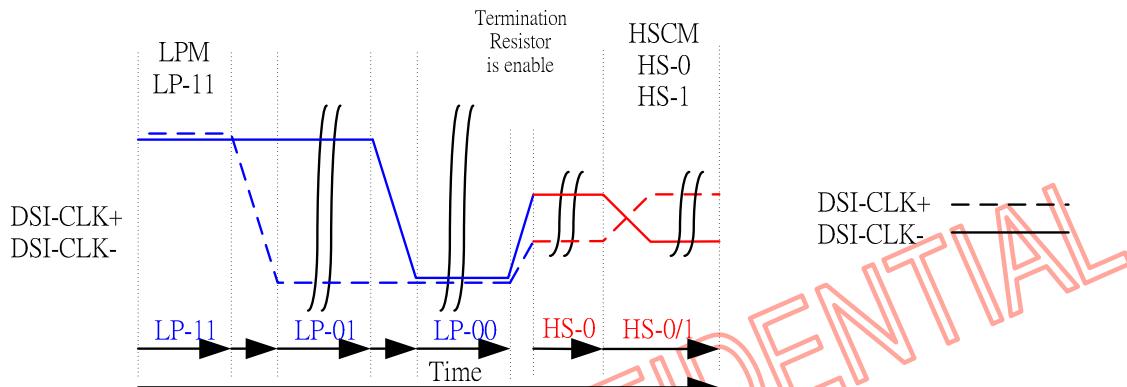
From LPM to ULPM

The mode change is also illustrated below.



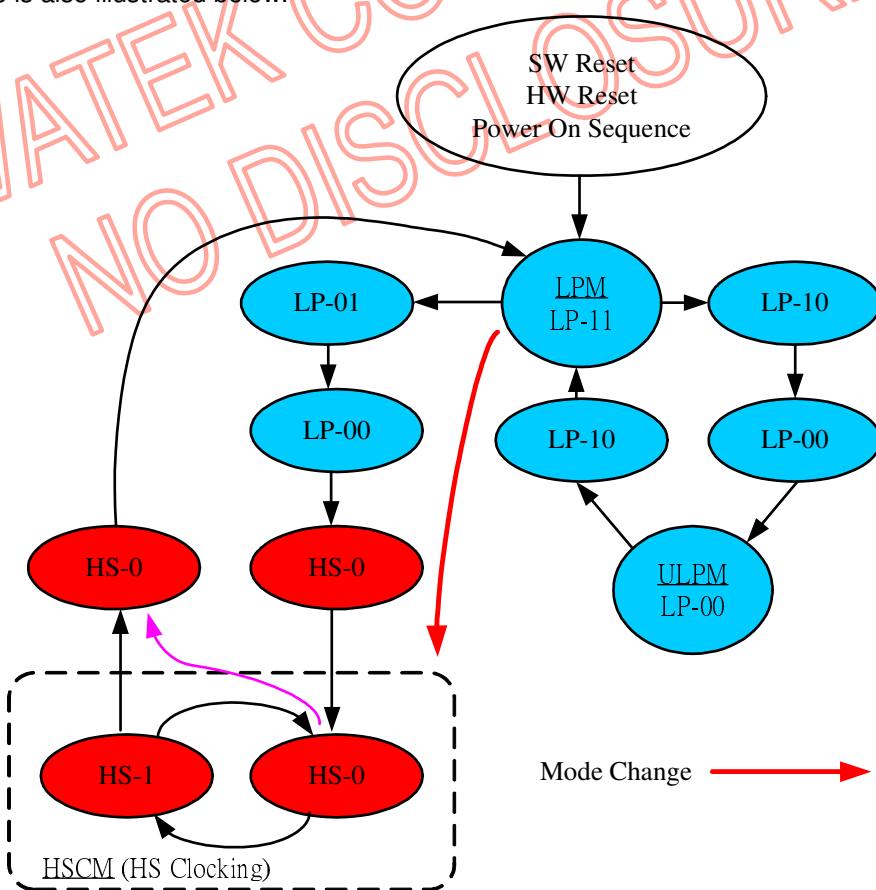
5.2.2.2.3 High Speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.



From LPM to HSCM

The mode change is also illustrated below.

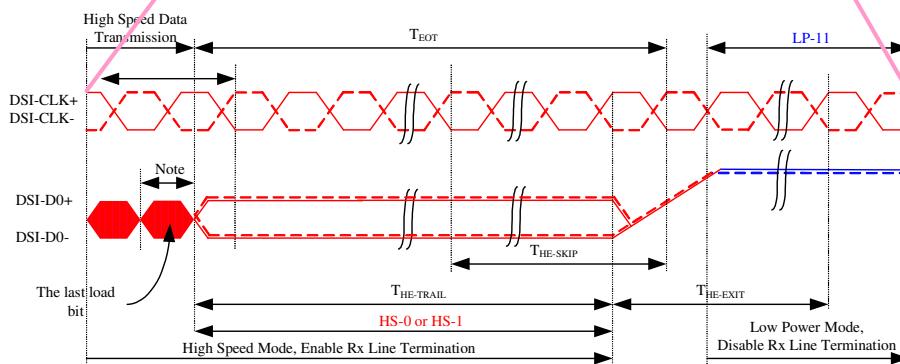
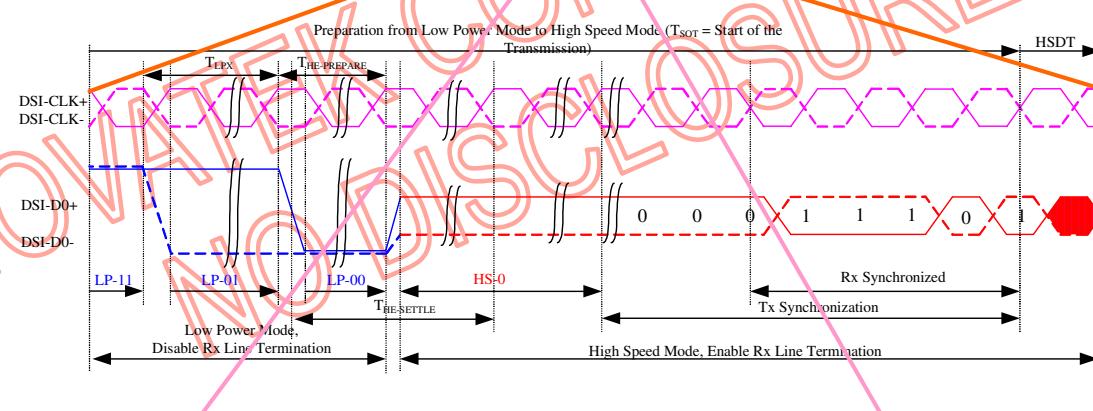
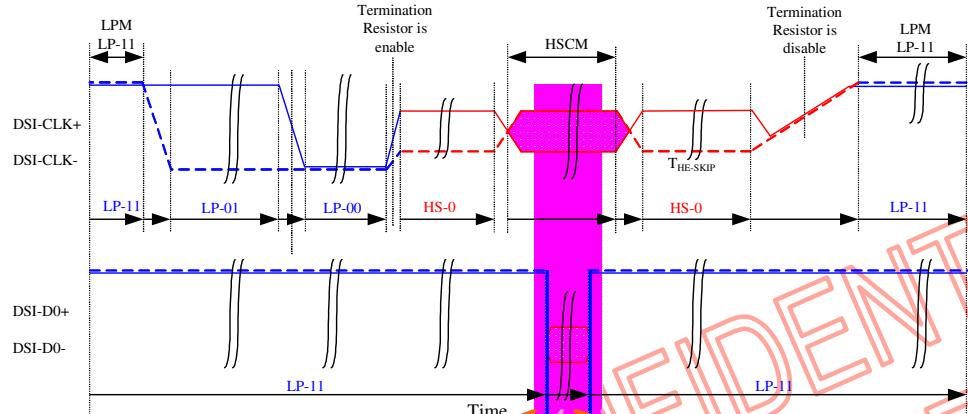


Mode Change from LPM to HSCM on the Flow Chart

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped.

The burst of the high speed clock consists of :

- Even number of transitions
- Start state is HS-0
- End state is HS-0



Note :

If the last load bit Is HS-0, the transmitter changes from HS-0 to HS-1.
 If the last load bit Is HS-1, the transmitter changes from HS-1 to HS-0.

DSI-CLK+, DSI-D0+ - - -
 DSI-CLK-, DSI-D0- —————

High Speed Clock Burst

5.2.2.2.3 DSI-DTAT Lanes

5.2.2.2.3.1 General

DSI-D0+/- Data Lanes can be driven in different modes which are:

- Escape Mode
- High-Speed Data Transmission
- Bus Turnaround Request

These modes and their entering codes are defined on the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11=>LP-10=>LP-00=>LP-01=>LP-00	LP-00=>LP-10=>LP-11(Mark-1)
High-Speed Data Transmission	LP-11=>LP-01=>LP-00=>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11=>LP-10=>LP-00=>LP-10=>LP-00	High-Z

Notes:

1. DSI-D0+/- data lane is used.
2. More information on section "Bus Turnaround (BTA)"

5.2.2.2.3.2 Escape Modes

Data lanes (DSI-D0+/-) can be used in different Escape Modes when data lanes are in Low Power (LP) mode.

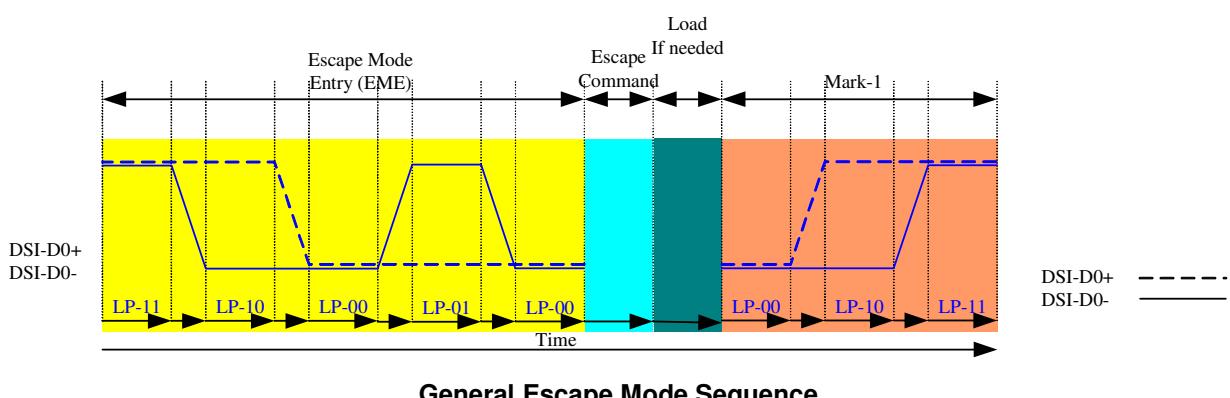
These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) e.g. from the MCU to the display module
- Drive data lanes to “Ultra-Low Power State” (ULPS)
- Indicate “Remote Application Reset” (RAR), which is reset the display module
- Indicate “Tearing Effect” (TEE), which is used for a TE trigger event from the display module to the MCU (NT35521 doesn't support TE trigger)
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the MCU

The basic sequence of the Escape Mode is as follow

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Escape Command (EC), which is coded, when one of the data lanes is changing from low-to-high-to-low then this changed data lane is presenting a value of the current data bit (DSI-D0+ = 1, DSI-D0- = 0) e.g. when DSI-D0- is changing from low-to-high-to-low, the receiver is latching a data bit, which value is logical 0. The receiver is using this low-to-high-to-low transition for its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11
- End: LP-11

This basic construction is illustrated below:



The number of the different Escape Commands (EC) is eight. These eight different escape commands (EC) can be divided 2 different groups: Mode or Trigger. The MCU is informing to the display module that it is controlling data lanes (DSI-D0+/-) with the mode e.g. The MCU can inform to the display module that it can put data lanes in the low power mode. The MCU is waiting from the display module event information, which has been set by the MCU, with the trigger e.g. when the display module finds no error for transmission packets, the display module sent to the MCU a Acknowledge (ACK), if the MCU has been requested it.

Escape commands are defined on the next table.

This basic construction is illustrated below:

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 _{bin}	-	X
Ultra-Low Power Mode	Mode	0001 1110 _{bin}	X	X
Underdefined-1, Note 1	Mode	1001 1111 _{bin}	-	-
Underdefined-2, Note 1	Mode	1101 1110 _{bin}	-	-
Remote Application Reset	Trigger	0110 0010 _{bin}	-	X
Tearing Effect	Trigger	0101 1101 _{bin}	-	-
Acknowledge	Trigger	0010 0001 _{bin}	-	X
Unknow-5, Note 1	Trigger	1010 0000 _{bin}	-	-

Notes:

1. This Escape command support has not been implemented on the display module.
2. n=1, 2 and 3.
3. "X"=Supported
4. "-"=Not Supported

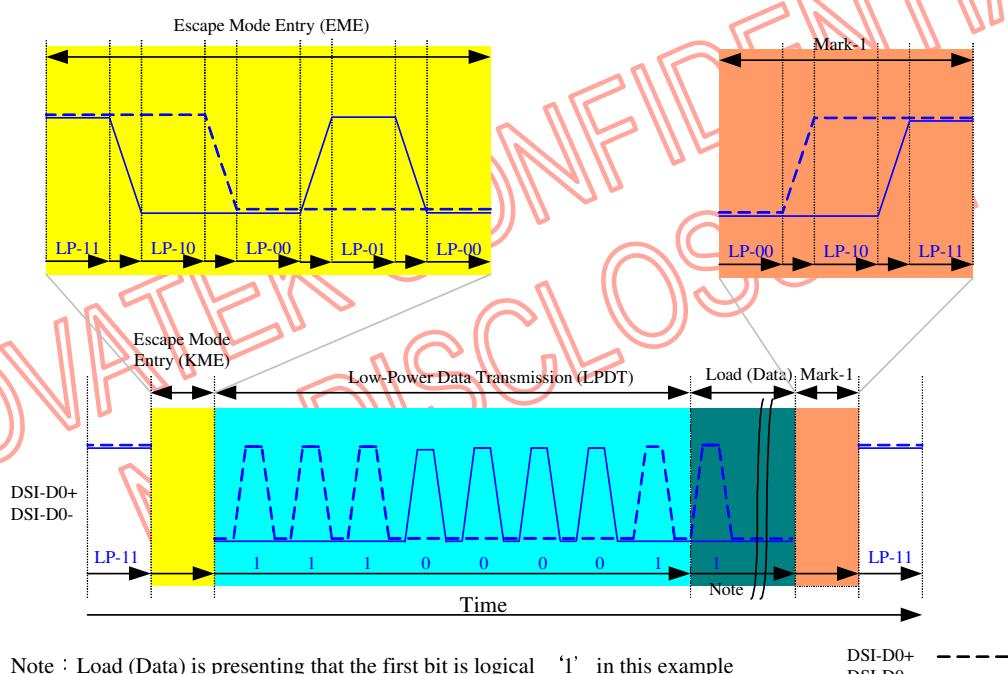
Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the MCU.

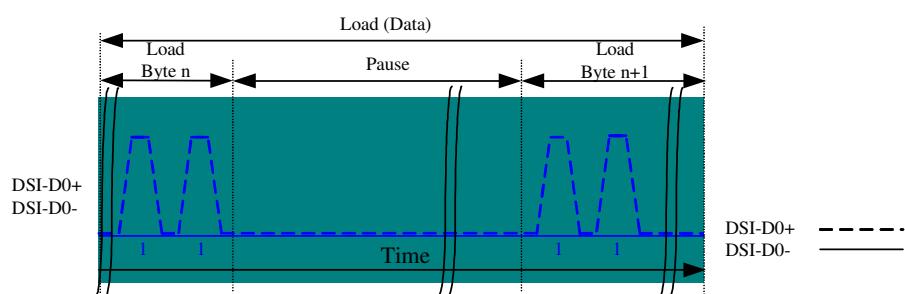
The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
- Load (Data):
 - One or more bytes (8 bit)
 - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Low-Power Data Transmission (LPDT)



Pause (Example)

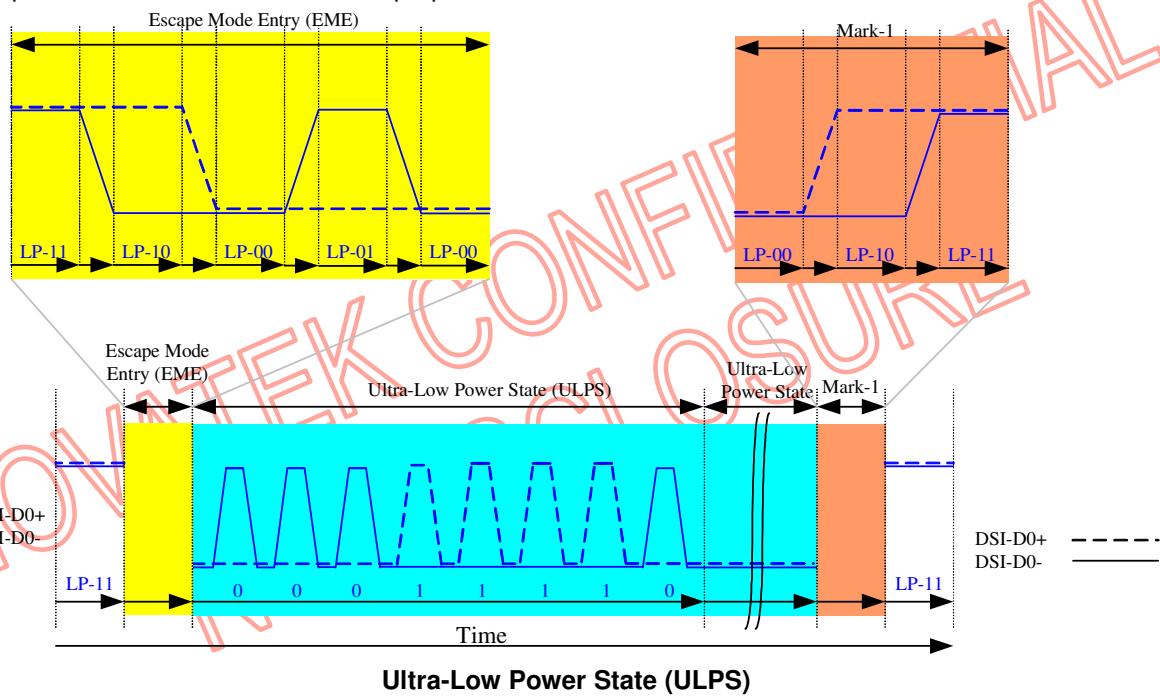
Ultra-Low Power State (ULPS)

The MCU can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the MCU is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



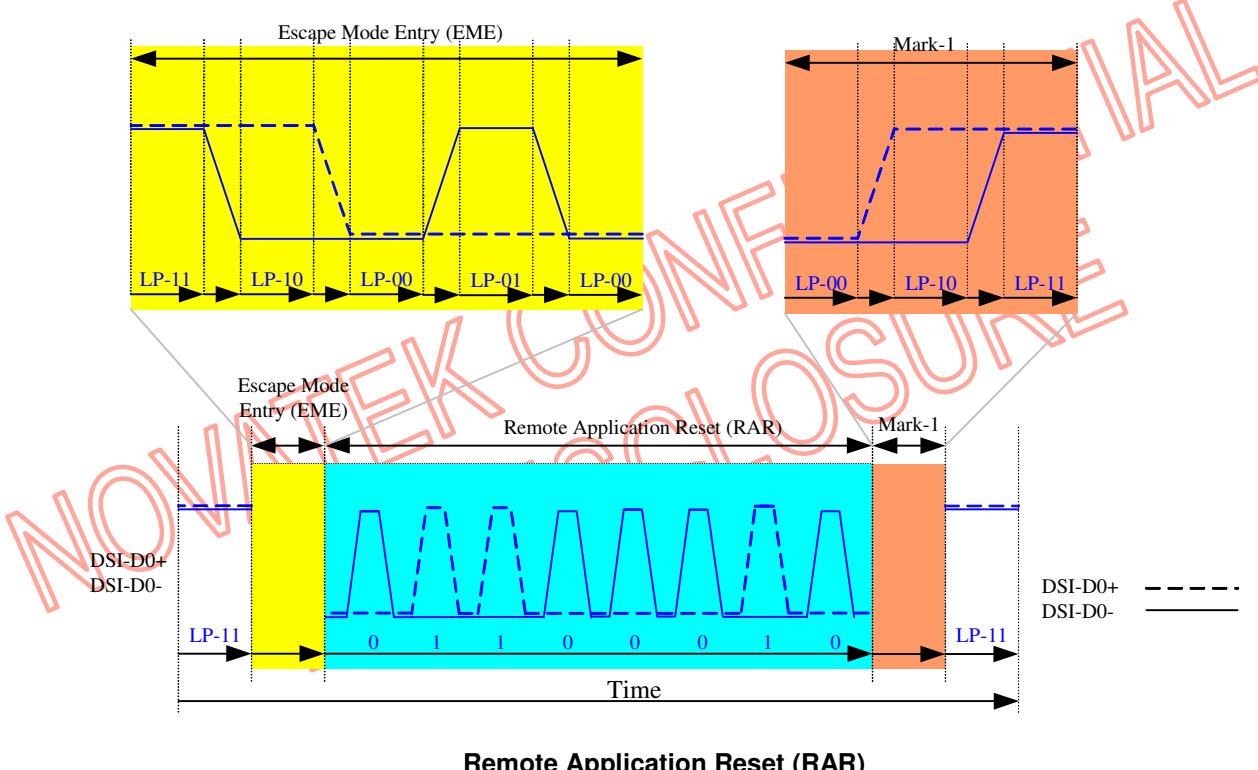
Remote Application Reset (RAR)

The MCU can inform to the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode.

The Remote Application Reset (RAR) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



Remote Application Reset (RAR)

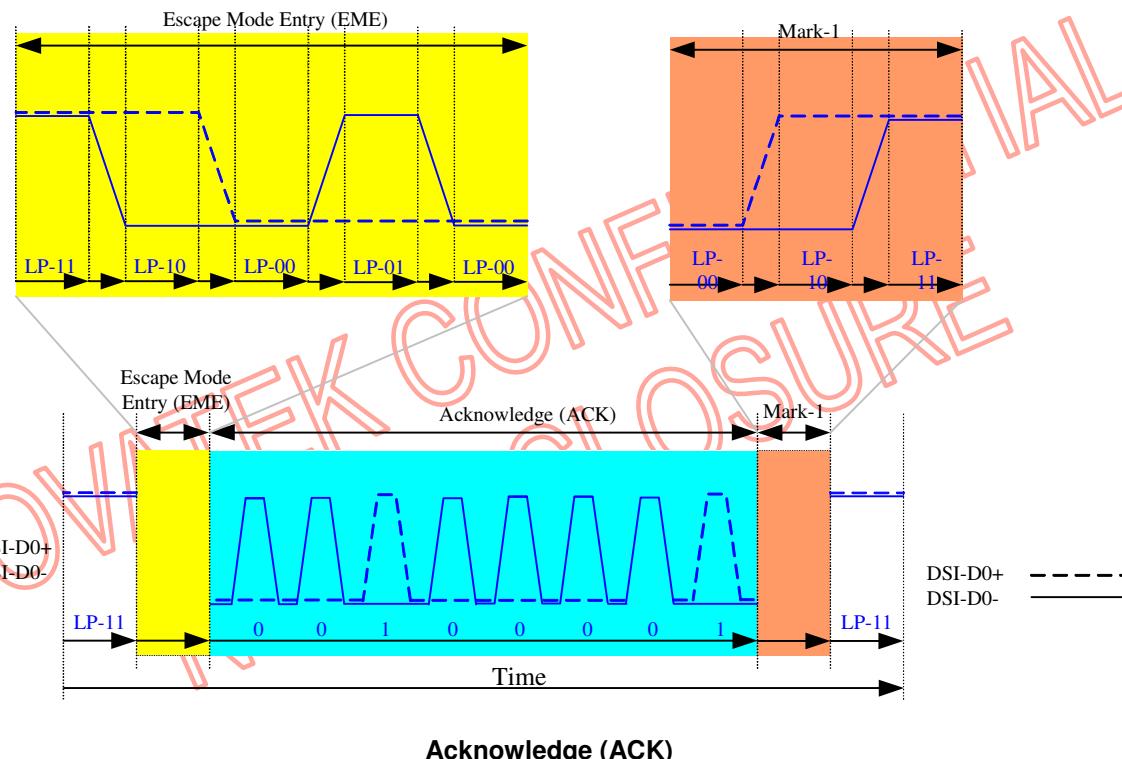
Acknowledge (ACK)

The display module can inform to the MCU when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) is using a following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:



5.2.2.2.3.3 High Speed Data Transmission (HSDT)

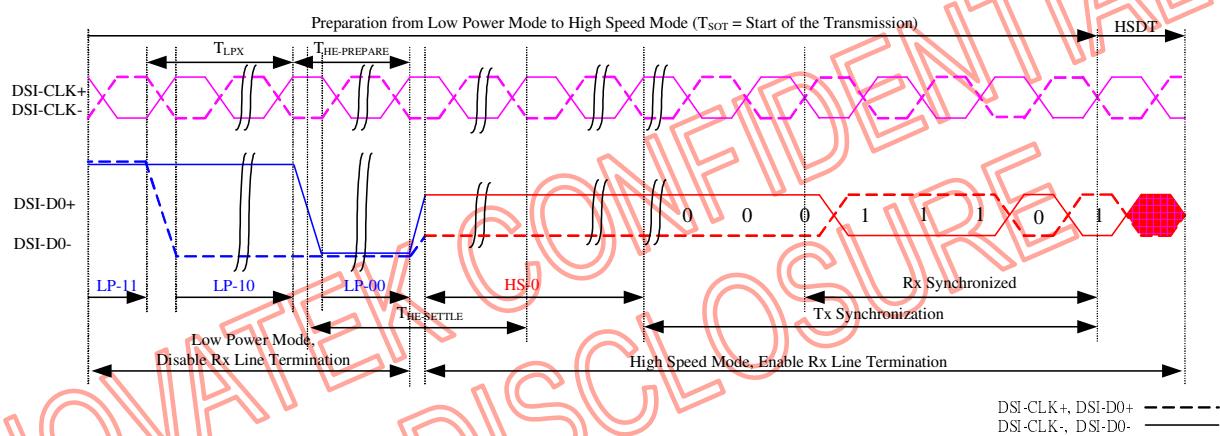
Entering High-Speed Data Transmission (T_{SOT} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the High-Speed Clock Mode (HSCM) by the MCU. See more information on chapter "5.2.2.2.3 High-Speed Clock Mode (HSCM)".

Data lanes of the display module are entering (T_{SOT}) in the High-Speed Data Transmission (HSDT) as follows

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below



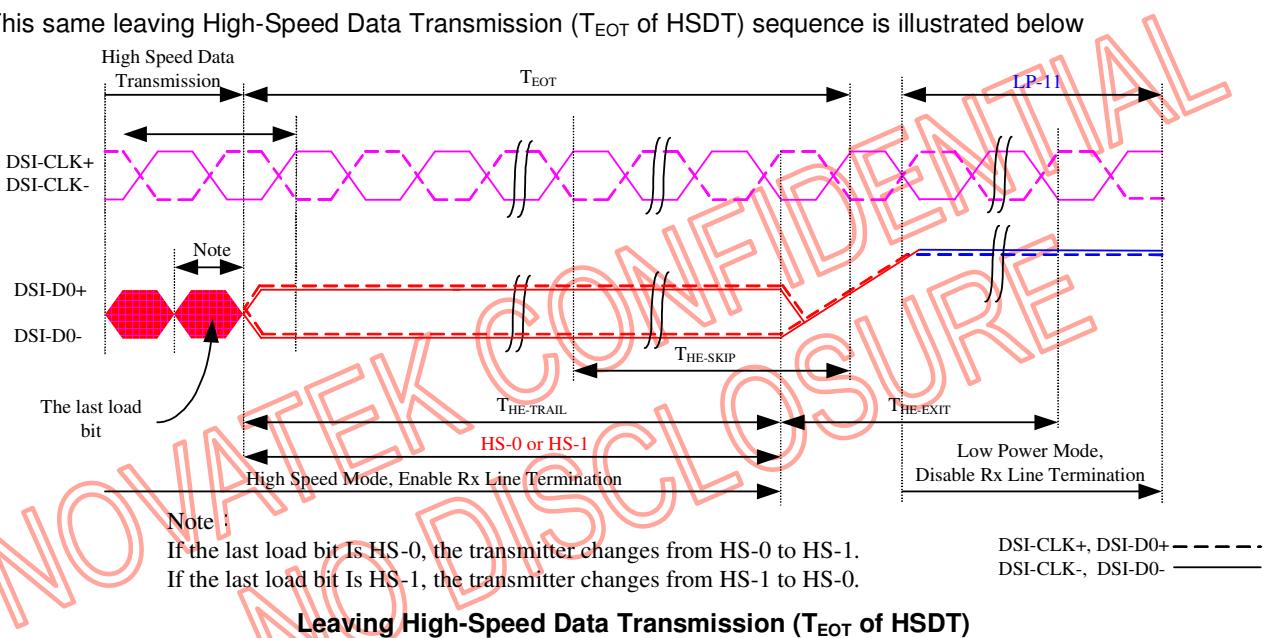
Leaving High-Speed Data Transmission (T_{EOT} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOT} of HSDT) when Clock lanes DSİ-CLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU and this HSCM is kept until data lanes are in LP-11 mode. See more information on chapter “5.2.2.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes of the display module are leaving from the High-Speed Data Transmission (T_{EOT} of HSDT) as follows

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
 - MCU changes to HS-1, if the last load bit is HS-0
 - MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

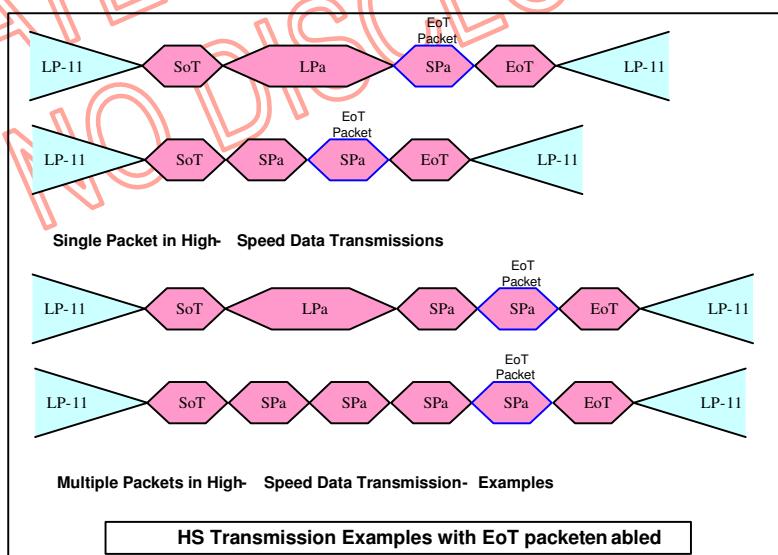
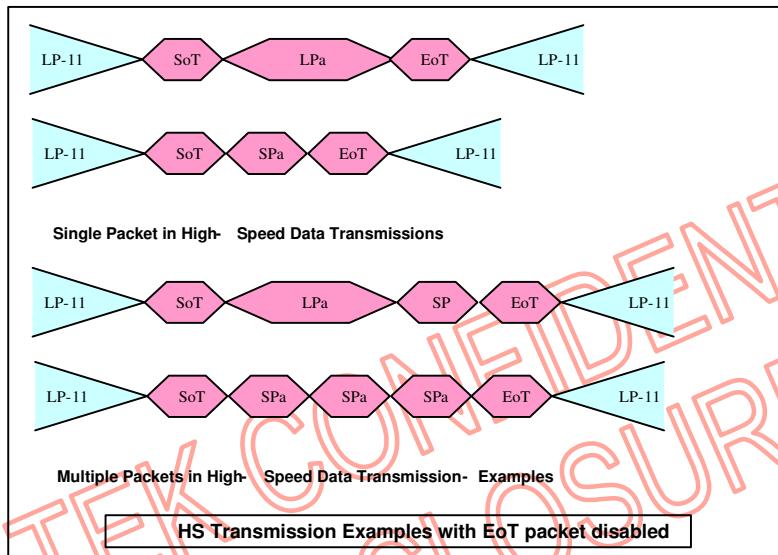
This same leaving High-Speed Data Transmission (T_{EOT} of HSDT) sequence is illustrated below



Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “5.1.9.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structures”.

These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.



Abbreviation	Explanation
EoT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SPa	Short Packet
SoT	Start of the Transmission

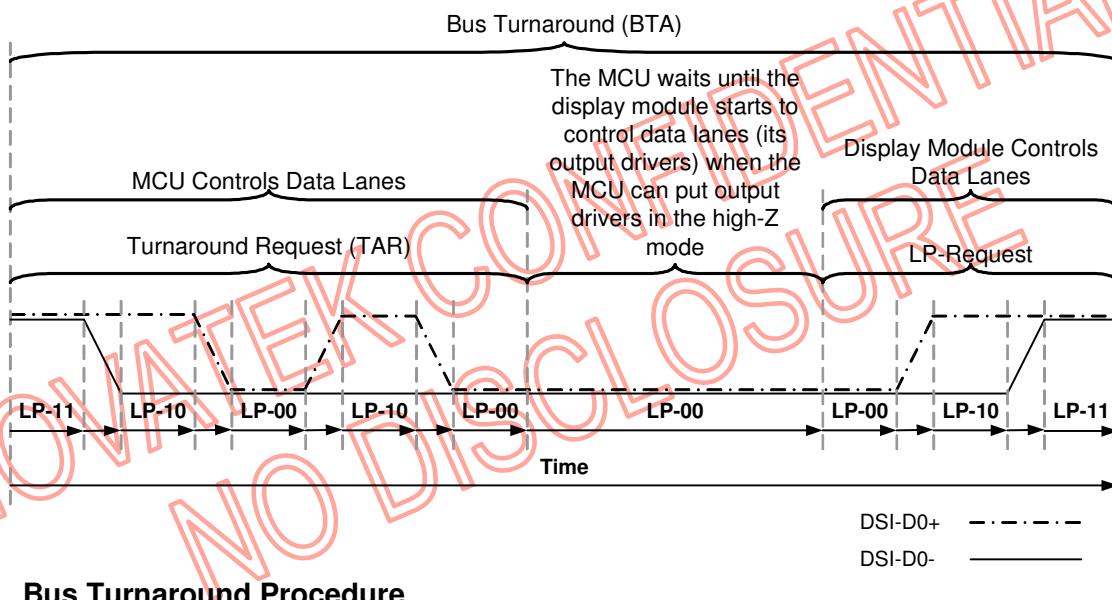
Bus Turnaround (BTA)

The MCU or display module, which is controlling DS1-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information from a receiver, which can be the MCU or display module.

The MCU or display module is using the same sequence when this bus turnaround procedure is used. This sequence is described for reference purposes, when the MCU wants to do the bus turnaround procedure to the display module, as follow.

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 → LP-10 → LP-00 → LP-10 → LP-00
- The MCU wait until the display module is starting to control DS1-D0+/- data lanes and the MCU stop to control DS1-D0+/- data lanes (=High-Z)
- The display module changes to the stop mode: LP-00 → LP-10 → LP-11

The same bus turnaround procedure (From the MCU to the display module) is illustrated below.



MCU and the display module terms are switched on above figure, if the Bus Turnaround (BTA) is from the display module to the MCU.

5.2.2.3 Packet Level Communication

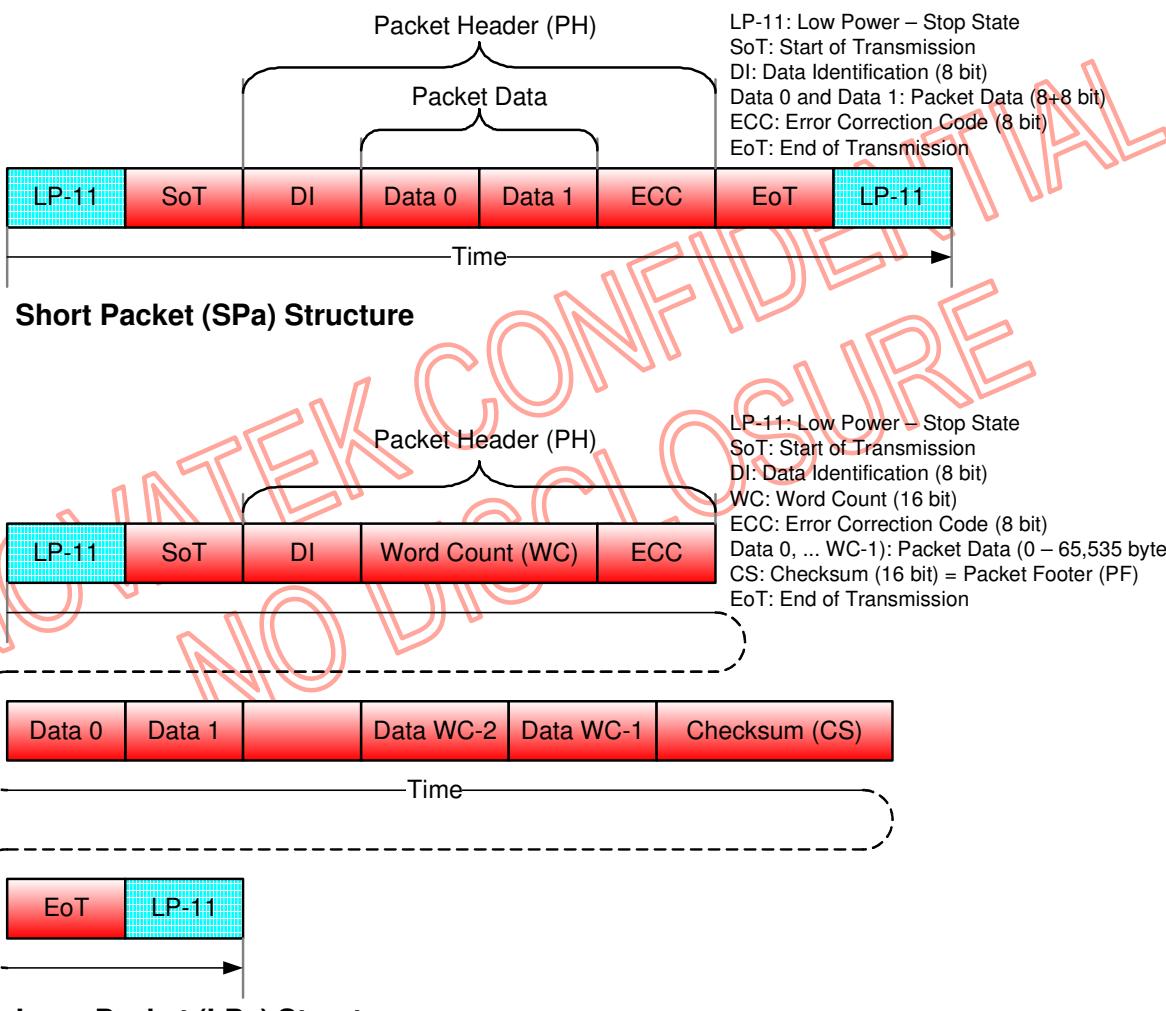
5.2.2.3.1 Short Packet (SPa) and Long Packet (LPa) Structure

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).



Long Packet (LPa) Structure

Note:

Short Packet (SPa) Structure and Long Packet (LPa) Structure are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sendings).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format e.g.

- * LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11
- * LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11
- * LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11

5.2.2.3.1.1 Bit Order of the Byte on Packets

The bit order of the byte, what is used on packets, is that the Least Significant Bit (LSB) of the byte is sent in the first and the Most Significant Bit (MSB) of the byte is sent in the last.

This same order is illustrated for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC											
29hex								01hex								00hex								06hex											
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0					
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B					
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7				
L	S	B						M	L							M	L								M	L					M	S	B		
								S	S							S	S								S	S					S				
								B	B							B	B								B	B					B				
Time →																																			

Bit Order of the Byte on Packets

5.2.2.3.1.2 Bit Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

WC(Least Significant Byte)								WC(Most Significant Byte)																											
01hex								00hex																											
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																				
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B																				
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7																				
L	S	B						M	L							M	S	B																	
								S	S							S	S								S	S					S				
								B	B							B	B								B	B					B				
Time →																																			

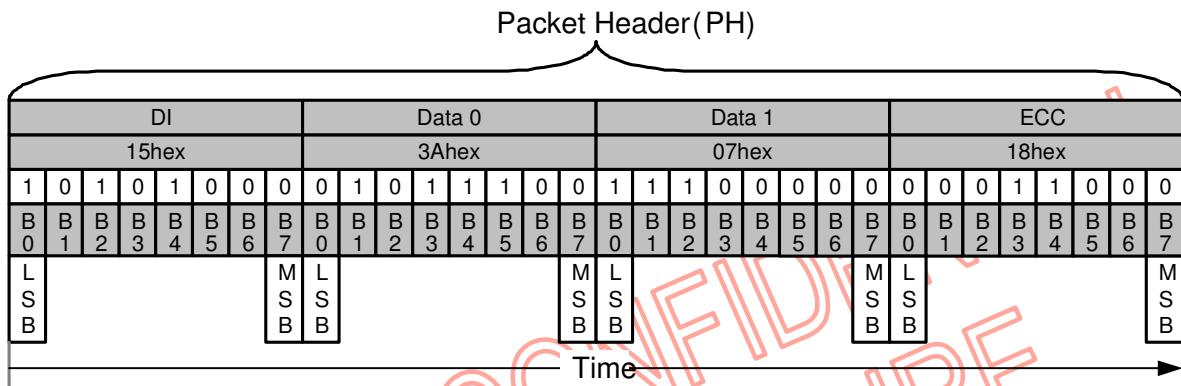
Byte Order of the Multiple Byte on Packets

5.2.2.3.1.3 Packet Header (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different if it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

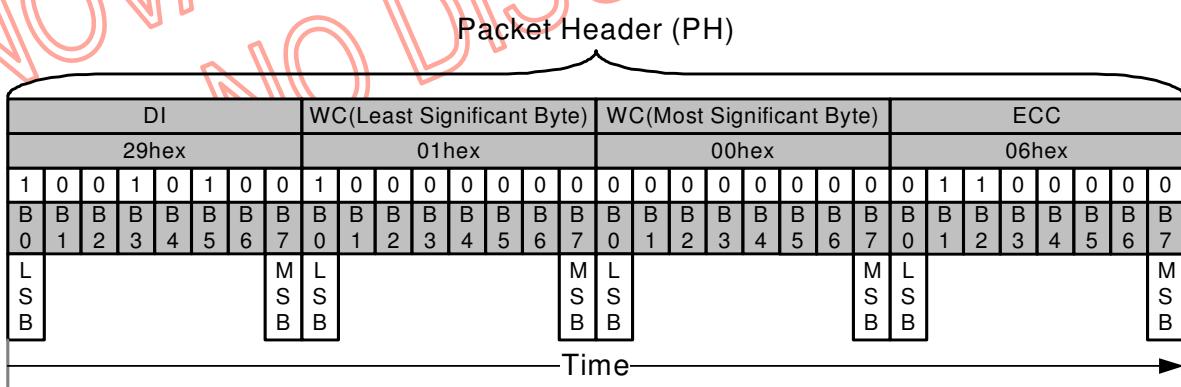
- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)



Packet Header (PH) on Long Packet (LPa)

Data Identification (DI)

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5...0]

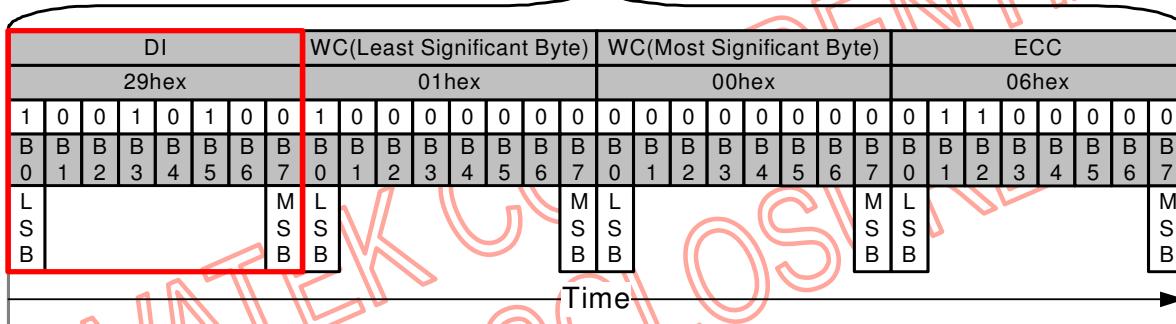
The Data Identification (DI) structure is illustrated on a table below.

Data Identification (DI) Structure

Data Identification (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

Packet Header (PH)

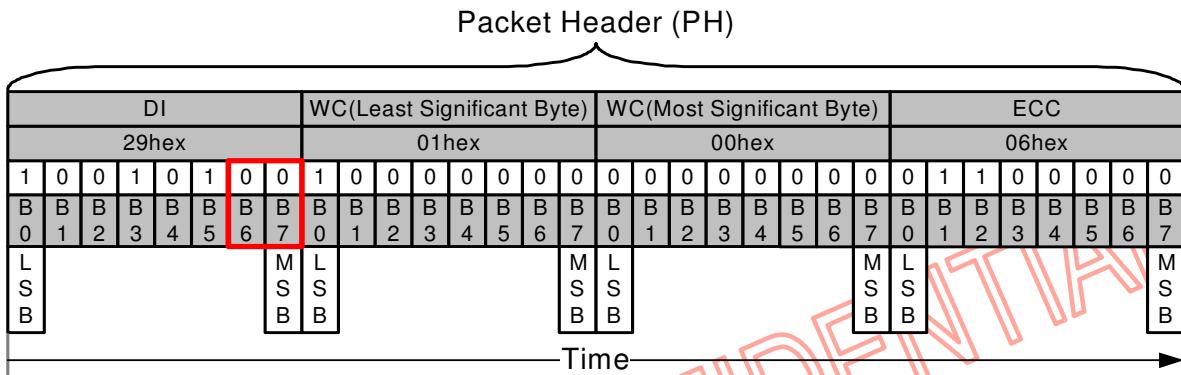


Data Identification (DI) on the Packet Header (PH)

Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure and it is used to address where a packet is wanted to send from the MCU.

Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

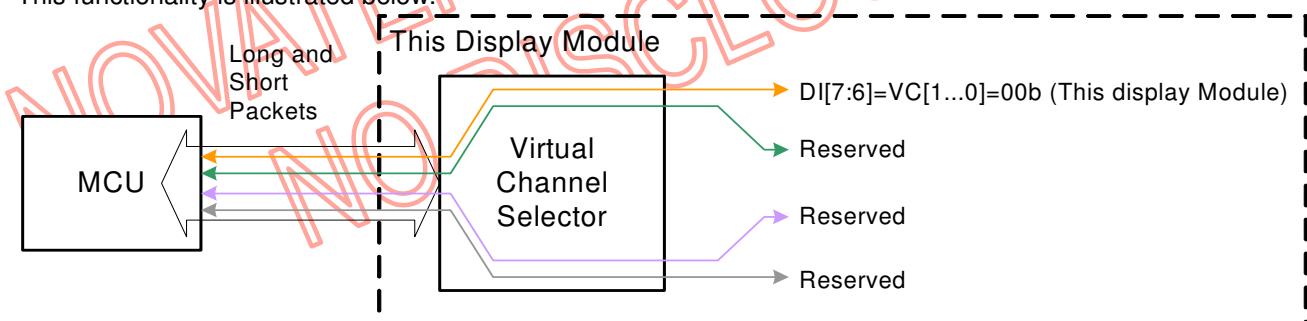


Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can address 4 different channels for e.g. 4 different display modules. Devices are using the same virtual channel what the MCU is using to send packets to them e.g.

- The MCU is using the virtual channel 0 when it sends packets to this display module
 - This display module is also using the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.



Virtual Channel (VC) Configuration

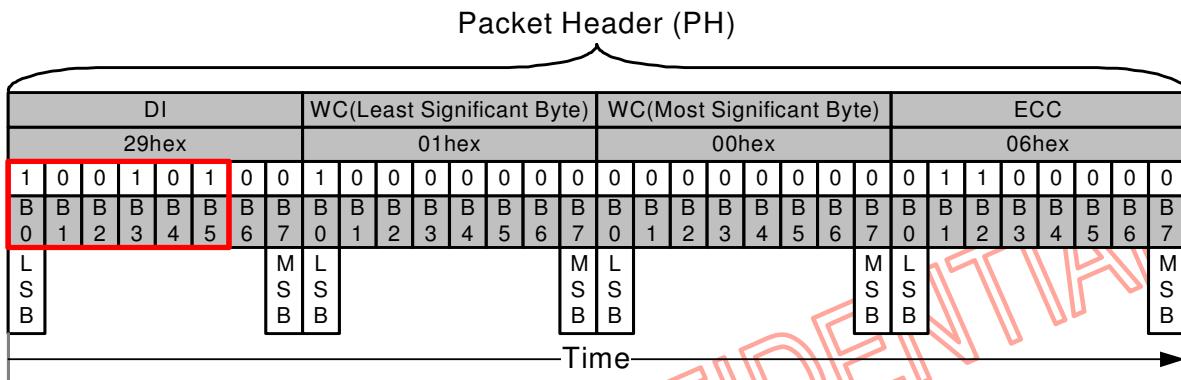
Virtual Channel (VC) always 0 ($D[7\dots6]=VC[1\dots0]000b$) when the MCU is sending “End of Transmission Packet” to the display module. See section “End of Transmission Packet (EoTP)”.

This display module is not supporting the virtual channel selector for other device (1 to 3) when only possible virtual channel (VC[1...0]) is 00b for this display module.

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5...0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.



Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa.

Data Types (DT) are defined on table below.

Data Type (DT) from MCU to the Display Module (or Other Devices)

Data Type Hex	Data Type Binary	Description	Packet Size	Note
08h	00 1000	End of Transmission packet	Short	1
05h	00 0101	DCS WRITE, no parameters	Short	
15h	01 0101	DCS WRITE, 1 parameter	Short	
06h	00 0110	DCS READ, no parameters	Short	
37h	11 0111	Set Maximum Return Packet Size	Short	
09h	00 1001	Null Packet, no data	Long	2
19h	01 1001	Blanking Packet, no data	Long	2
39h	11 1001	DCS Long Write/Write_LUT Command Packet	Long	
01h	00 0001	Sync Event, V Sync Start	Short	7
11h	01 0001	Sync Event, V Sync End	Short	7
21h	10 0001	Sync Event, H Sync Start	Short	7
31h	11 0001	Sync Event, H Sync End	Short	7
02h	00 0010	Color mode (CM) Off Command	Short	7
12h	01 0010	Color mode (CM) On Command	Short	7
22h	10 0010	Shut Down Peripheral Command	Short	7
32h	11 0010	Turn On Peripheral Command	Short	7
13h	01 0011	Generic Short Write, 1 parameter	Short	3,4,8
23h	10 0011	Generic Short Write, 2 parameter	Short	3,5,8
29h	10 1001	Generic Long Write	Long	3,8
14h	01 0100	Generic Read, 1 parameter	Short	3,4,8
0Eh	00 1110	Packed Pixel Stream,16-bit RGB, 5-6-5 Format	Long	7
1Eh	01 1110	Packed Pixel Stream,18-bit RGB, 6-6-6 Format	Long	7
2Eh	10 1110	Loosely Packed Pixel Stream,18-bit RGB, 6-6-6 Format	Long	7
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long	7

Notes:

1. This can be used when the MCU wants to secure that there is the end of transmission in High Speed Data Transmission (HSDT) mode.
2. This can be used when the data lanes are wanted to keep in High Speed Data Transmission (HSDT) mode.
3. The receiver process packets with data type (Generic Write/Read) the same way as data type (DCS Write / Read).
4. Generic Write/Read with 1 parameter: Payload Bytes = Command + 00h.
5. Generic Write/Read with 2 parameter: Payload Bytes = Command + Parameter.
6. The receiver will ignore packets with data type that neither listed in table above nor in MIPI DSI spec.

Data Type (DT) from the Display Module (or Other Devices) to the MCU

From the Display Module (or Other Devices) to the MCU										
Hex	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Description	Short/Lng Packet	Abbreviation	Note
02h	0	0	0	0	1	0	Acknowledge with Error Report	Short	AwER	
1Ch	0	1	1	1	0	0	DCS Read Long Response	Long	DCSRR-L	
21h	1	0	0	0	0	1	DCS Read Short Response, 1 byte returned	Short	DCSRR1-S	
22h	1	0	0	0	1	0	DCS Read Short Response, 2 byte returned	Short	DCSRR2-S	
1Ah	0	1	1	0	1	0	Generic Read Long Response	Long	GENRR-L	Note
11h	0	1	0	0	0	1	Generic Read Short Response, 1 byte returned	Short	GENRR1-S	Note
12h	0	1	0	0	1	0	Generic Read Short Response, 2 byte returned	Short	GENRR2-S	Note

The receiver will ignore other Data Type (DT) if they are not defined on tables: "Data Type (DT) from the MCU to the Display Module (or Other Devices)" or "Data Type (DT) from the Display Module (or Other Devices) to the MCU".

Note: The data type for Generic write/read: 1Ah, 11h, 12 will be disable (ignored packet) if bit DSIG is set to "0".

NOVATEK CONFIDENTIAL
NO DISCLOSURE

Packet Data (PD) on the Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send.

The Word Count (WC) indicates the number of Bytes of Packet of Packet Data (PD) send after the Packet Header.

Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1.

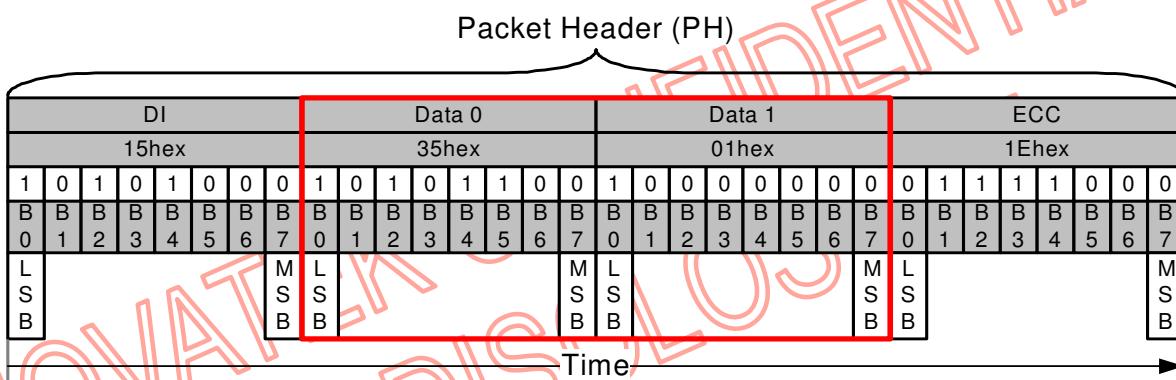
Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last.

Bits of Data 1 are set to '0' if the information length is 1 byte.

Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below, when Virtual Channel (VC) is 0.

Packet Data (PD) information:

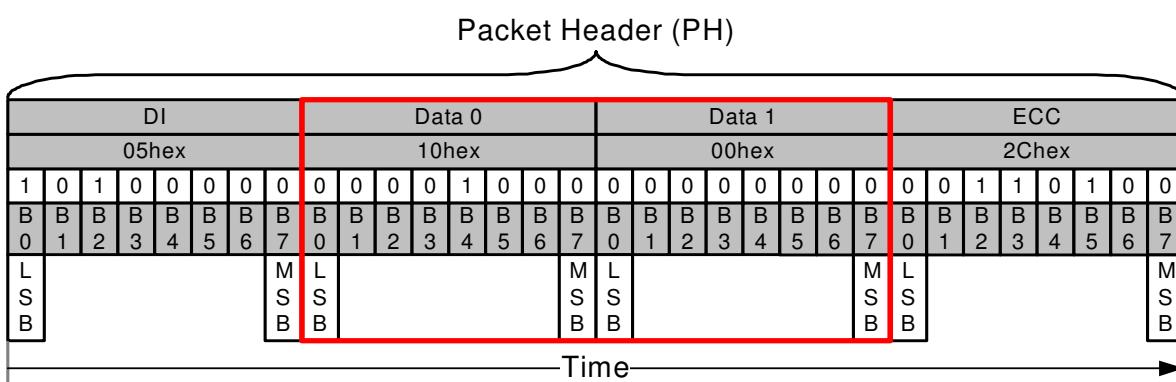
- Data 0: 35hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
 - Data 1: 01hex (DCS's parameter)



Packet Data (PD) for Short Packet (SPa). 2 Bytes Information

Packet Data (PD) information:

- Data 0: 00hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
 - Data 1: 00hex (Null)



Packet Data (PD) for Short Packet (SPa), 1 Bytes Information

Word Count (WC) on the Long Packet (LPa)

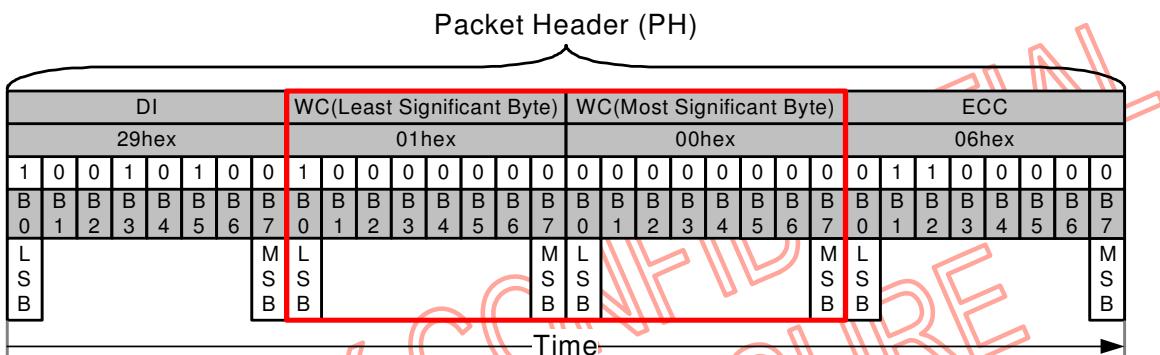
Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send.

Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH).

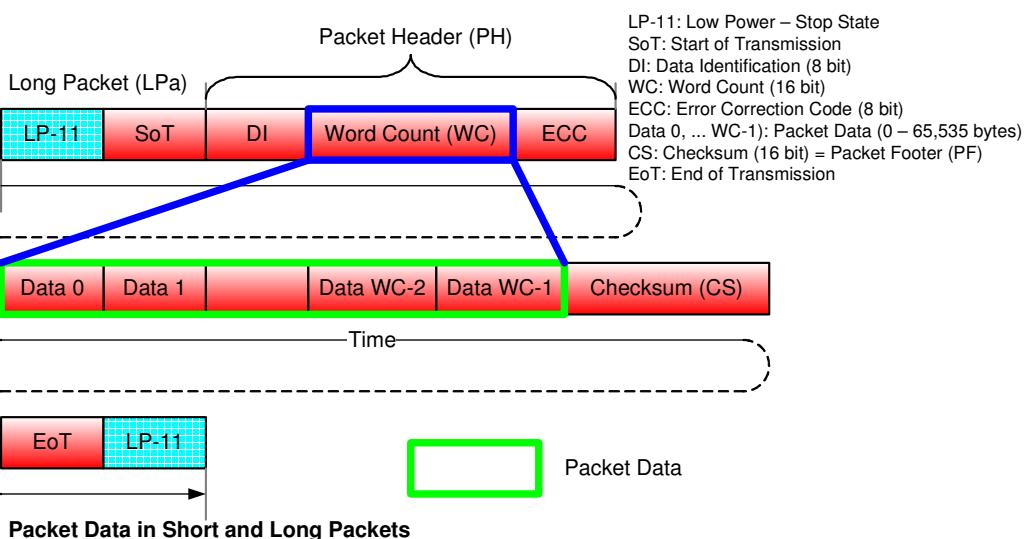
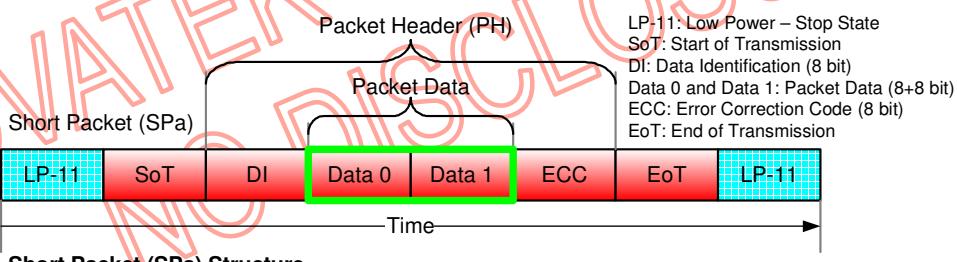
Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.



Word Count (WC) on the Long Packet (LPa)



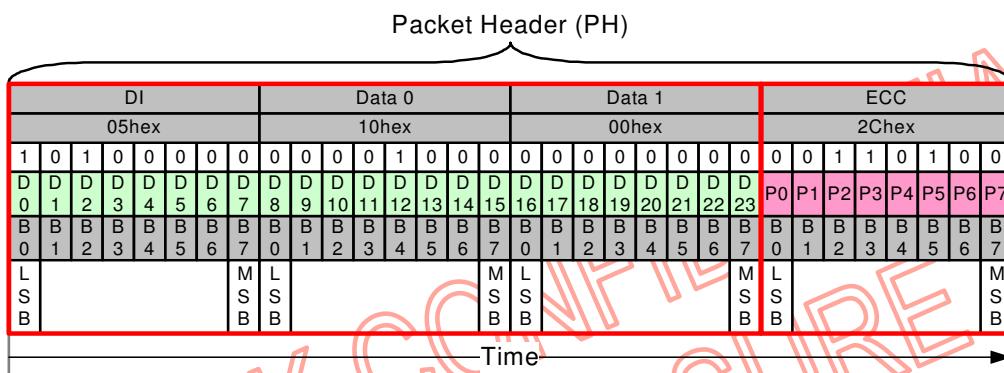
Error Correction Code (ECC)

Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors on the Packet Header (PH):

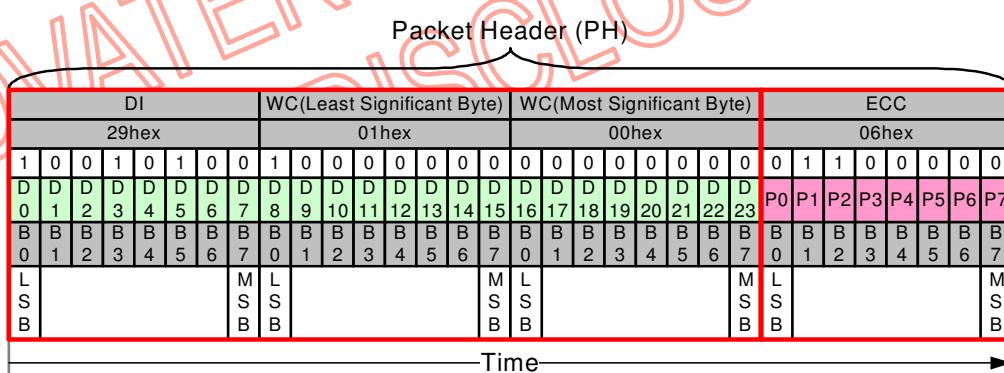
The ECC protects the following field"

- Short Packet (SPa): Data Identification (DI) byte (8 bits, D[0...7]), Packet Data (PD) bytes (16 bits, D[8...23]) and ECC(8 bits: P[0...7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits, D[0...7]), Word Count (WC) bytes (16 bits: D[8...23]) and ECC (8 bits, P[0...7])

D[23...0] and P[7...0] are illustrated for reference purposes below.



D[23...0] and P[7...0] on the Short Packet (SPa)



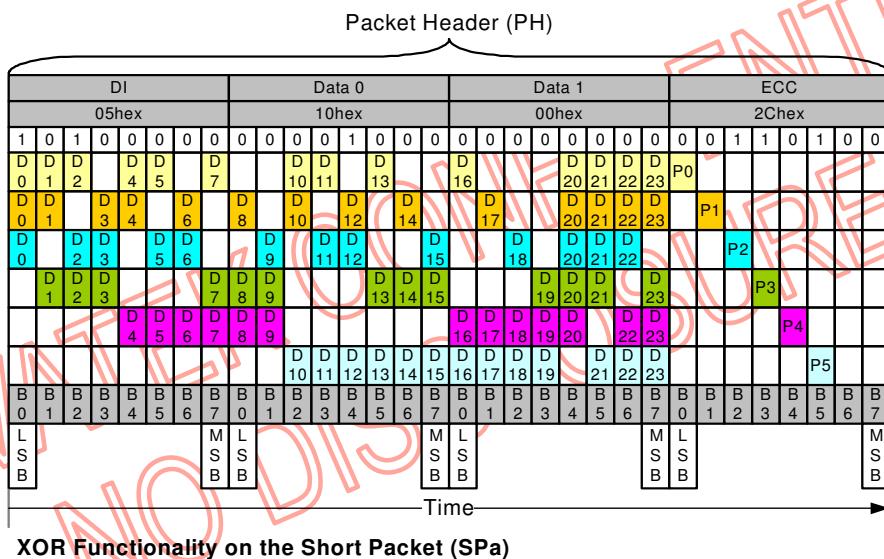
D[23...0] and P[7...0] on the Long Packet (LPa)

Error Correction Code (ECC) can recognize one error or several errors and makes correction in one bit error case.

Bits (P[7...0]) of the Error Correction Code (ECC) are defined, where the symbol '^' is presenting XOR function (Pn is '1' if there is odd number of '1's and Pn is '0' if there is even number of '1's), as follows.

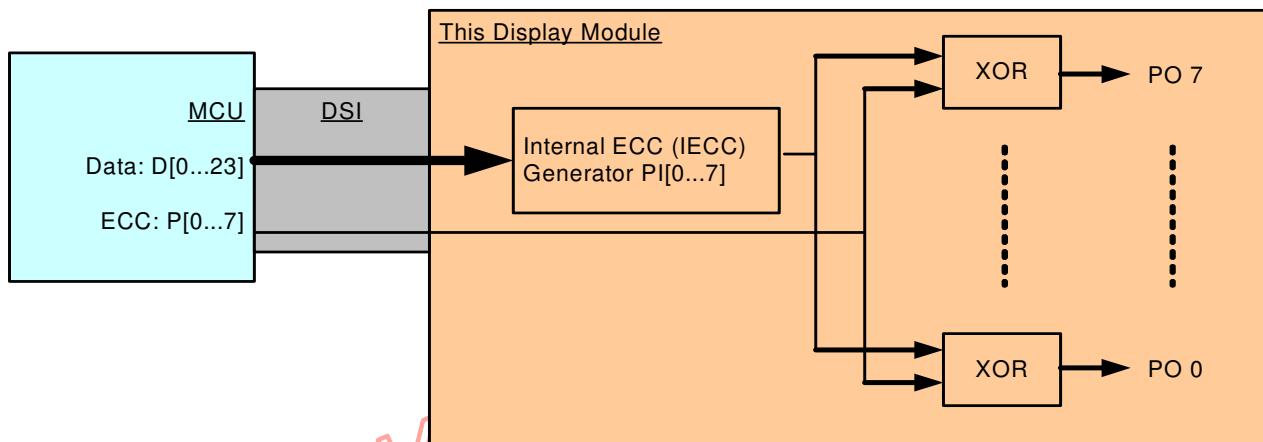
- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63...0]), but this implementation is based on 24 bit value (D[23...0]). Therefore, there is only needed 6 bits (P[5...0]) for Error Correction Code (ECC).



The transmitter (The MCU or the Display Module) is sending data bits D[23...0] and Error Correction Code (ECC) P[7...0]. The receiver (The Display module or the MCU) is calculate an Internal Error Correction Code (IECC) and compares the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have been done XOR function. The result of this function is PO[7...0].

This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.



Internal Error Correction Code (IECC) on the Display Module (The Receiver)

The sent data bits (D[23...0]) and ECC (P[7...0]) are received correctly, if a value of the PO[7...0] is 00h. The sent data bits (D[23...0]) and ECC (P[7...0]) are not received correctly, if a value of the PO[7...0] is not 00h.

ECC P[7...0]	1 1 0 0 0 0 0 0	03h
IECC PI[7...0]	1 1 0 0 0 0 0 0	03h
XOR(ECC,IECC) =>PO[7...0]	0 0 0 0 0 0 0 0	=00h => No Error
	L M S S B B	

Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7...0]	1 1 0 0 0 0 0 0	03h
IECC PI[7...0]	1 1 1 1 0 0 0 0	0Fh
XOR(ECC,IECC) =>PO[7...0]	0 0 1 1 0 0 0 0	=0Ch => Error
	L M S S B B	

Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) functionality is not used for data values D[23...0] on the transmitter side.

The number of the errors (one or more) can be defined when the value of the PO[7...0] is compared to values on the following table.

One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D[0]	0	0	0	0	0	1	1	1	07h
D[1]	0	0	0	0	1	0	1	1	0Bh
D[2]	0	0	0	0	1	1	0	1	0Dh
D[3]	0	0	0	0	1	1	1	0	0Eh
D[4]	0	0	0	1	0	0	1	1	13h
D[5]	0	0	0	1	0	1	0	1	15h
D[6]	0	0	0	1	0	1	1	0	16h
D[7]	0	0	0	1	1	0	0	1	19h
D[8]	0	0	0	1	1	0	1	0	1Ah
D[9]	0	0	0	1	1	1	0	0	1Ch
D[10]	0	0	1	0	0	0	1	1	23h
D[11]	0	0	1	0	0	1	0	1	25h
D[12]	0	0	1	0	0	1	1	0	26h
D[13]	0	0	1	0	1	0	0	1	29h
D[14]	0	0	1	0	1	0	1	0	2Ah
D[15]	0	0	1	0	1	1	0	0	2Ch
D[16]	0	0	1	1	0	0	0	1	31h
D[17]	0	0	1	1	0	0	1	0	32h
D[18]	0	0	1	1	0	1	0	0	34h
D[19]	0	0	1	1	1	0	0	0	38h
D[20]	0	0	0	1	1	1	1	1	1Fh
D[21]	0	0	1	0	1	1	1	1	2Fh
D[22]	0	0	1	1	0	1	1	1	37h
D[23]	0	0	1	1	1	0	1	1	3Bh

One error is detected if the value of the PO[7...0] is on : One Bit Error Value of the Error Correction Code (ECC) and the receiver can correct this one bit error because this found value also defines what is a location of the corrupt bit e.g.

- PO[7...0] = 0Eh
- The bit of the data (D[23...0]), what is not correct, is D[3]

More than one error is detected if the value of the PO[7...0] is not on: One Bit Error Value of the Error Correction Code (ECC) e.g. PO[7...0] = 0Ch.

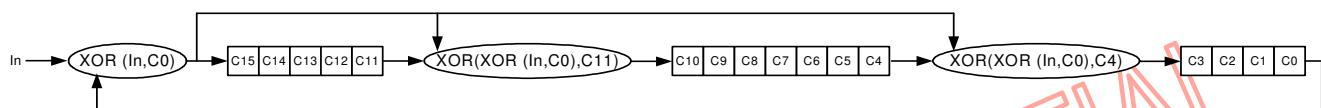
5.2.2.3.1.4 Packet Data (PD) on the Long Packet (LPa)

Packet Data (PD) of the Long Packet (LPa) is defined after Packet Header (PH) of the Long Packet (LPa). The number of the data bytes is defined on chapter "Word Count (WC) on the Long Packet (LPa)".

5.2.2.3.1.5 Packet Footer (PF) on the Long Packet (LPa)

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

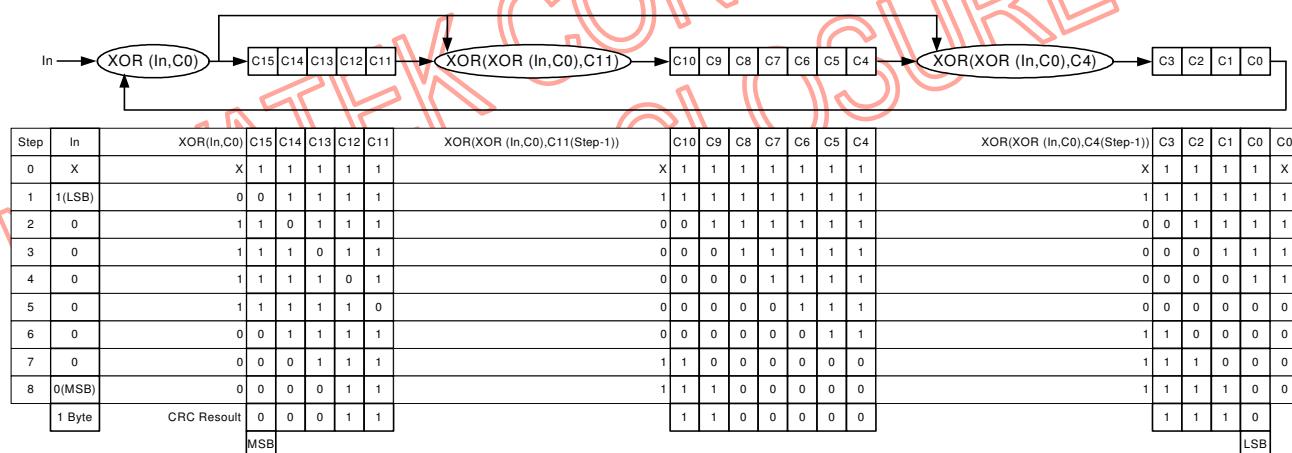
The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X^{16}+X^{12}+X^5+X^0$ as it is illustrated below.



16-bit Cyclic Redundancy Check (CRC) Calculation

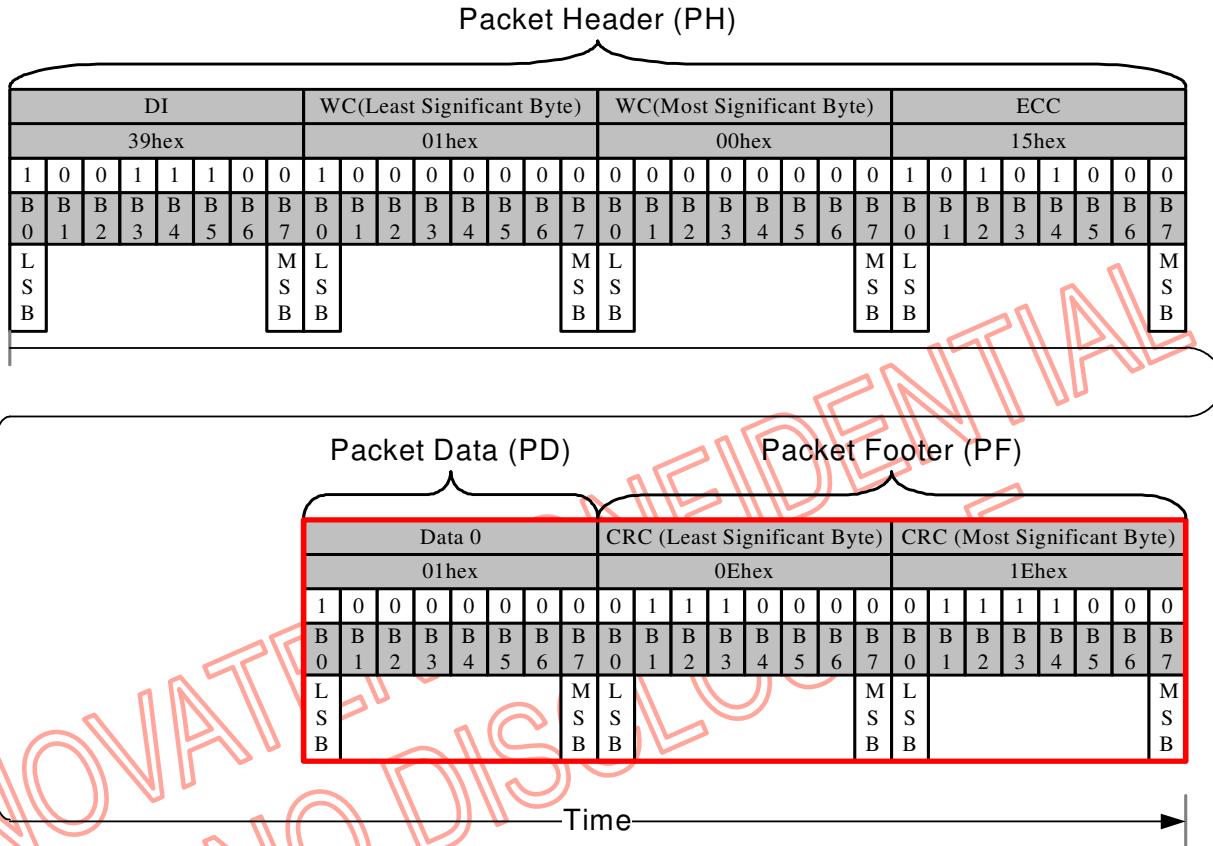
The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Least Significant Bit (LSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC).

An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of the Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



CRC Calculation – Packet Data (PD) is 01h

A value of the Packet Footer (PF) is 1E0Eh in this example. This example (Command 01h has been sent) is illustrated below.



Packet Footer (PF) Example

The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent.

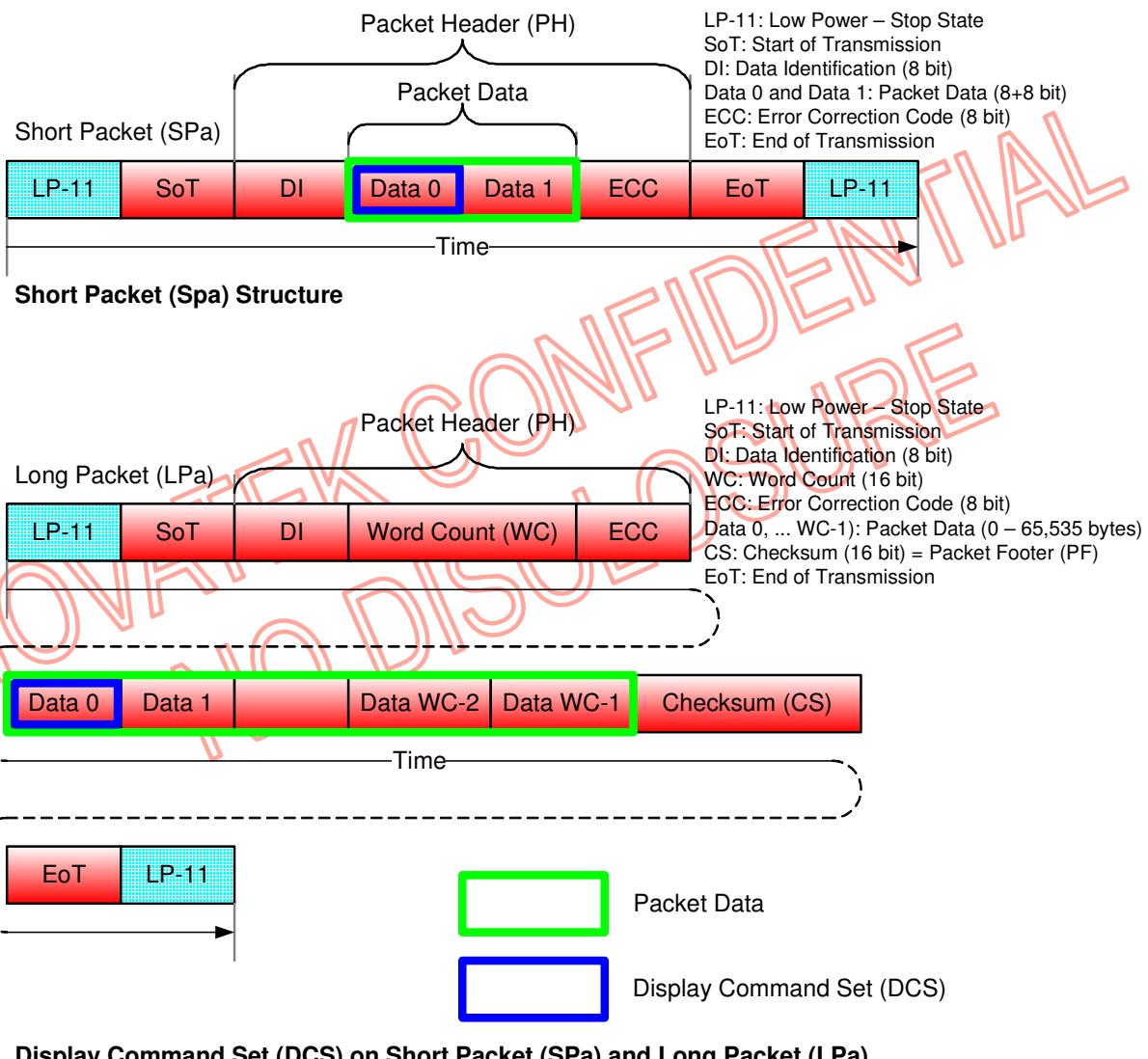
The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.2.2.3.2 Packet Transmissions

5.2.2.3.2.1 Packet from the MCU to the Display Module

Display Command Set (DCS)

Display Command Set (DCS), which is defined on chapter “6 Instruction Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.



Display Command Set (DCS) on Short Packet (SPa) and Long Packet (LPa)

Generic Write, 1 Parameter (GENW1-S), Data Type = 01 0011 (13h)

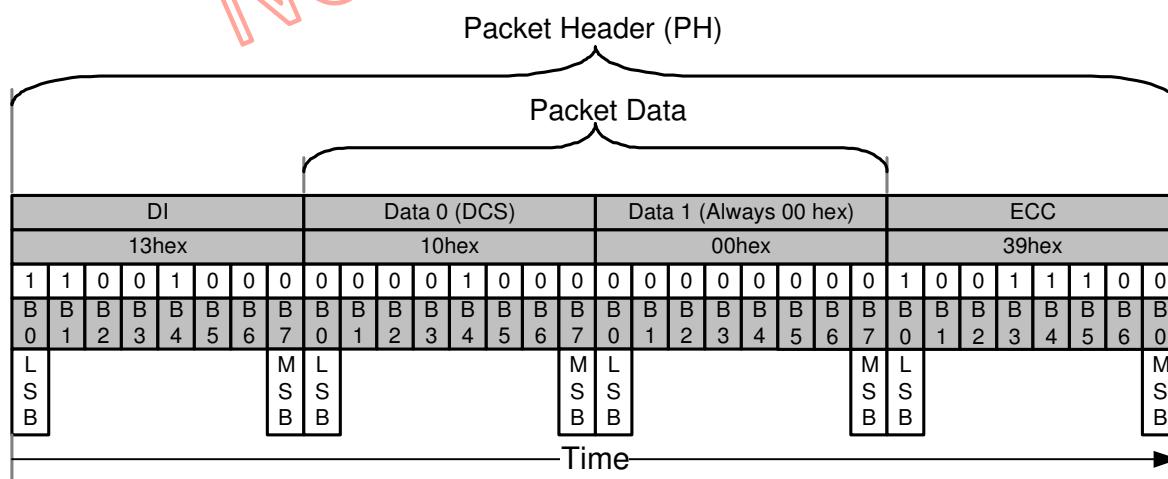
"Generic Write, 1 Parameter" (GENW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and 00h. These commands are defined on a table (See chapter "6 Instruction Description") below.

Command
NOP (00h)
SWRESET (01h)
SLPIN (10h)
SLPOUT (11h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
TEOFF (34h)
IDMOFF (38h)
IDMON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0011b
- Packet Data (PD)
 - Data 0: "Sleep In (10h)", Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 1 Parameter (GENW1-S) - Example

Generic Write, 2 Parameter (GENW2-S), Data Type = 10 0011 (23h)

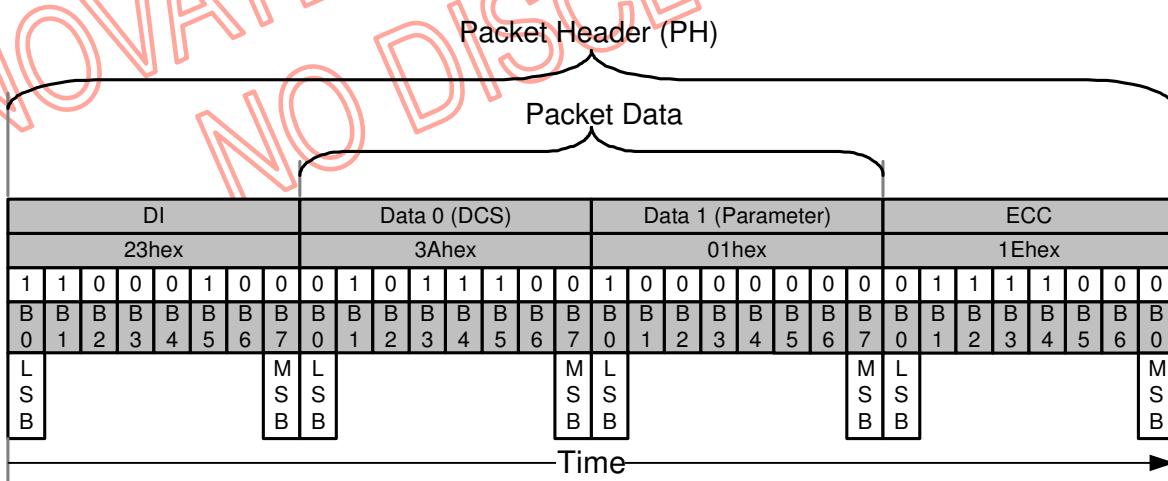
"Generic Write, 2 Parameter" (GENW2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0011b), from the MCU to the display module. The content of 2 payload bytes is "command" and "parameter". These commands are defined on a table (See chapter "6 Instruction Description") below.

Command
GAMSET (26h)
TEON (35h)
MADCTR (36h)
COLMOD (3Ah)
DSTBON (4Fh)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCM (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0011b
- Packet Data (PD)
 - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Generic Write, 2 Parameter (GENW2-S) - Example

Generic Write Long (GENW-L), Data Type = 10 1001 (29h)

"Generic Write Long" (GENW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 10 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "6 Instruction Description") below.

Command
NOP (00h) , Note1
SWRESET (01h) , Note1
SLPIN (10h) , Note1
SLPOUT (11h) , Note1
NORON (13h) , Note1
INVOFF (20h) , Note1
INVON (21h) , Note1
ALLPOFF (22h)
ALLPON (23h)
GAMSET (26h) , Note2
DISPOFF (28h) , Note1
DISPON (29h) , Note1
TEOFF (34h) , Note1
TEON (35h) , Note2
MADCTR (36h)
IDMOFF (38h) , Note1
IDMON (39h) , Note1
COLMOD (3Ah) , Note2
TEARLINE (44h)
DSTBON (4Fh) , Note2
WRDISBV (51h) , Note2
WRCTRLD (53h)
WRCABC (55h) , Note2
WRCABCMB (5Eh)

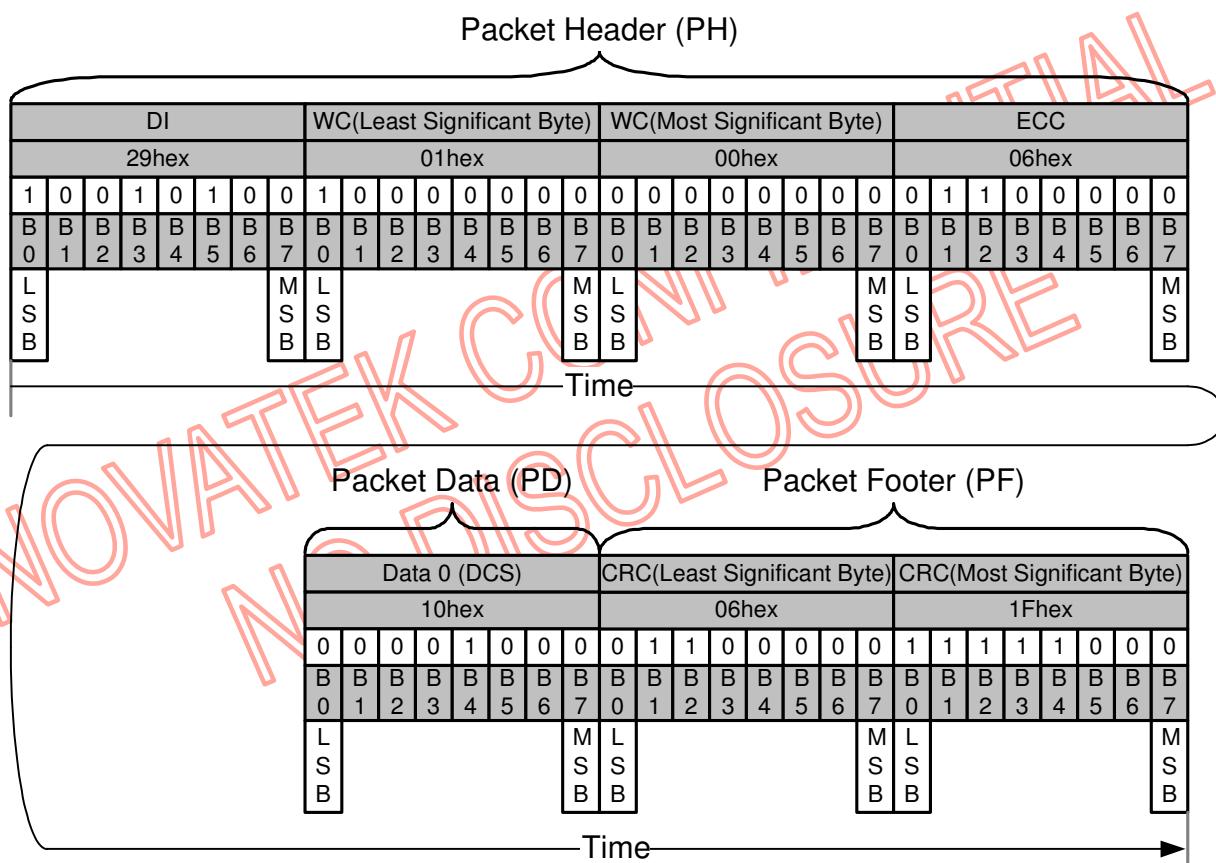
Notes :

1. Also Short Packet (Spa) can be used; See Generic Write, 1 Parameter.
2. Also Short Packet (Spa) can be used; See Generic Write, 2 Parameter.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 1001b
 - Word Count (WC)
 - Word Count (WC): 0001h
 - Error Correction Code (ECC)
 - Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
 - Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.

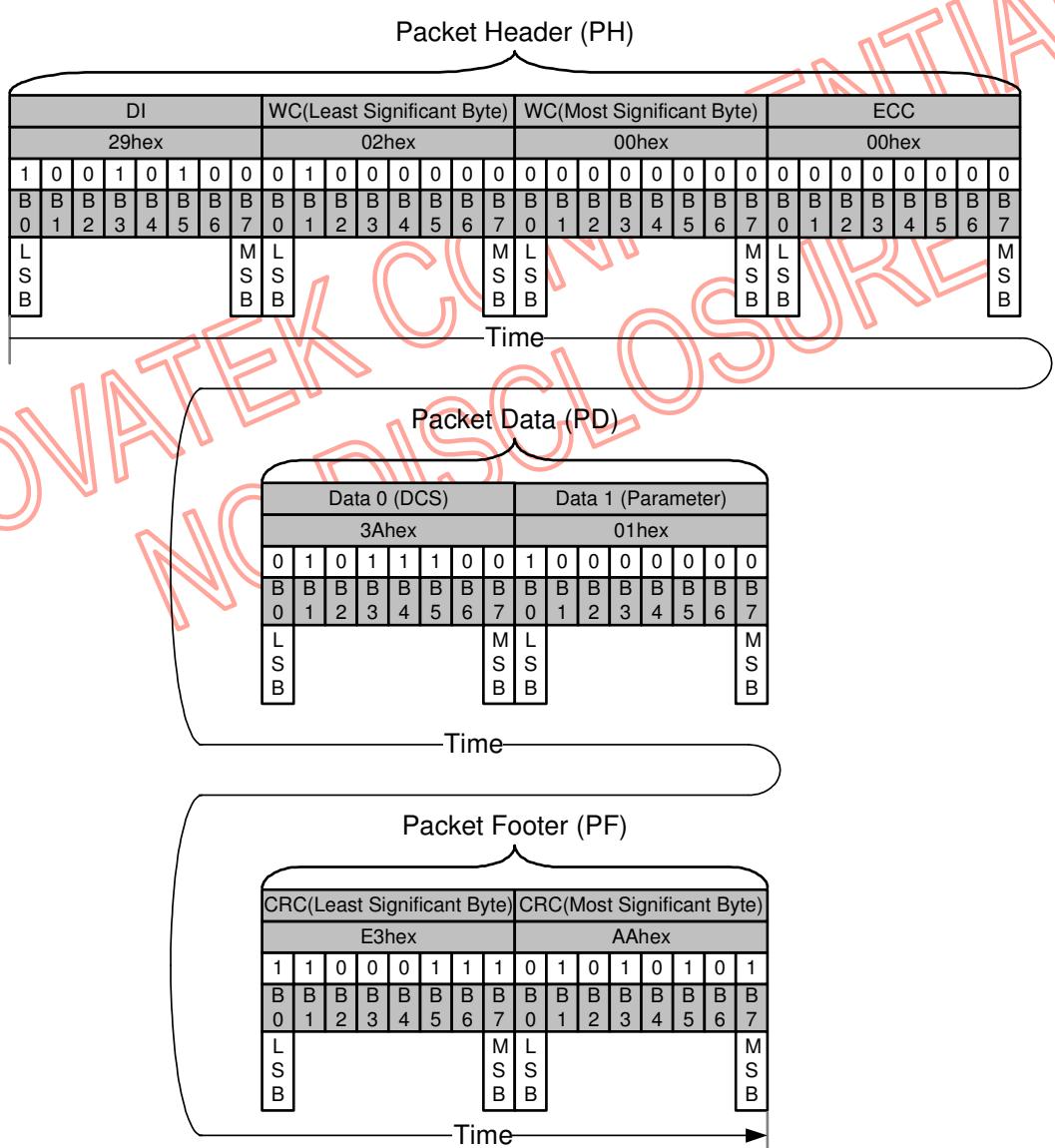


Generic Long Write (GENW-L) with DCS Only - Example

Long Packet (LPa), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 1001b
- Word Count (WC)
 - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Gamma Set (3Ah)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.



Generic Long Write (GENW-L) with DCS and 1 Parameter - Example

Generic Read, 1 Parameter (GENR1-S), Data Type = 01 0100 (14h)

"Generic Read, 1 Parameter (GENR1-S) is always using a Short Packet (Spa), what is defined on Data Type (DT, 01 0100b), from the MCU to the display module. This command is defined on a table (See chapter "6 Instruction Description") below.

The 1st parameter (Dummy Data) is not returned as it is done in MeSSI-8/16 cases. The first returned parameter is the 2nd parameter in DSI case.

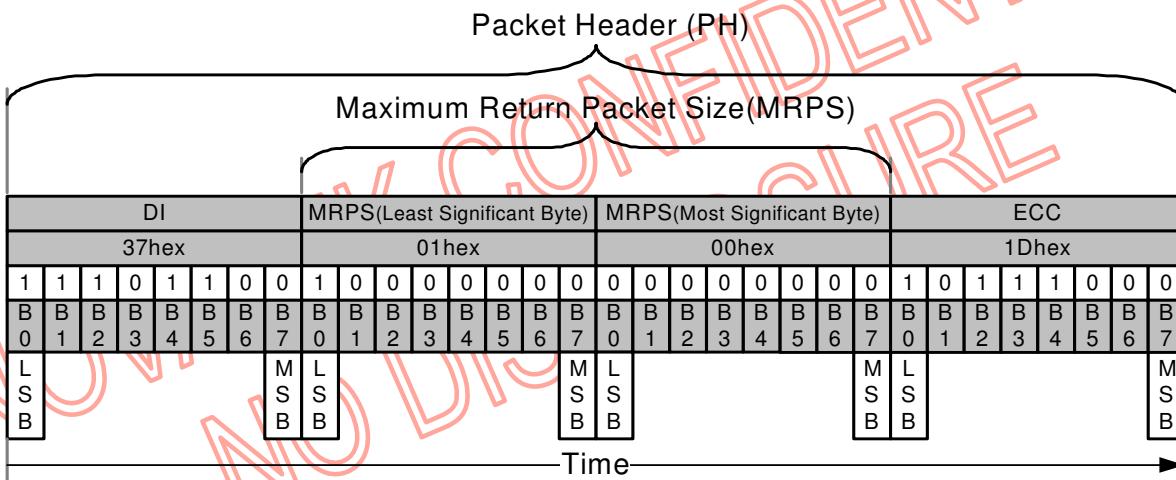
Command
RDDID (04h)
RDBLUE (08h)
RDDPM (0Ah)
RDDMADCTR (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
GSL (45h)
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDCABCMB (5Fh)
RDDDBST (A1h)
RDDDBC (A8h)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

NOVATEK CONFIDENTIAL
NO DISCLOSURE

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

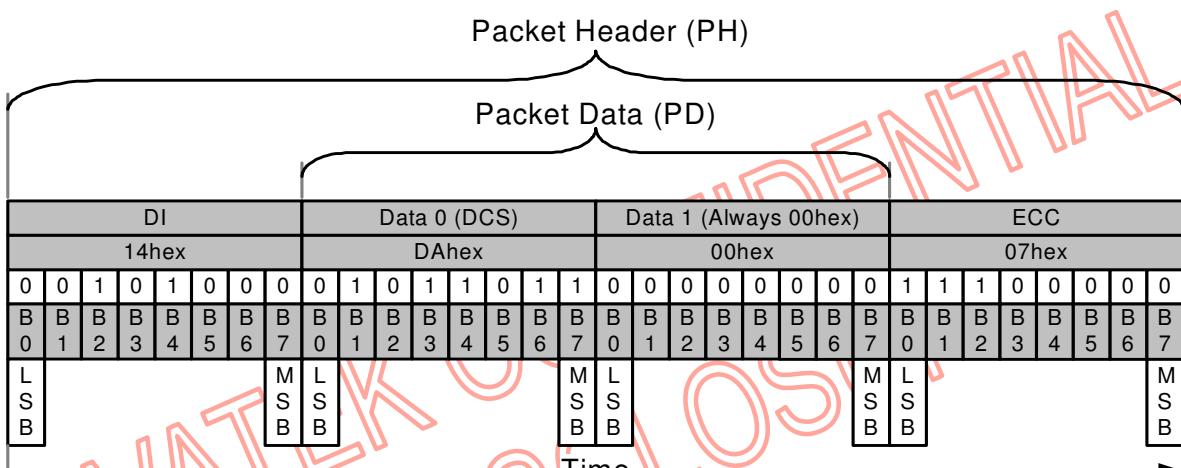
Step 1:

- The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - Data 0: 01hex
 - Data 1: 00hex
- Error Correction Code (ECC)



Step 2:

- The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Generic Read, 1 Parameter” to the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0100b
- Packet Data (PD)
 - Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)


Generic Read, 1 Parameter (GENR1-S) - Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.
2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

Display Command Set (DCS) Write, No Parameter (DCSWN-S), Data Type = 00 0101 (05h)

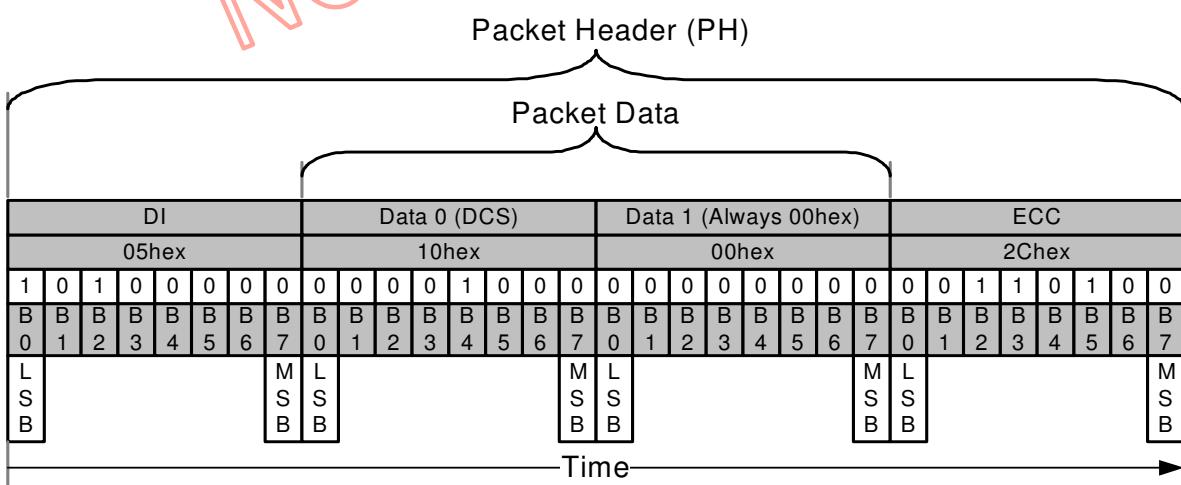
"Display Command Set (DCS) Write, No Parameter" is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "6 Instruction Description") below.

Command
NOP (00h)
SWRESET (01h)
SLPIN (10h)
SLPOUT (11h)
NORON (13h)
INVOFF (20h)
INVON (21h)
ALLPOFF (22h)
ALLPON (23h)
DISPOFF (28h)
DISPON (29h)
TEOFF (34h)
IDMOFF (38h)
IDMON (39h)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0101b
- Packet Data (PD)
 - Data 0: "Sleep In (10h)", Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.


Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

Display Command Set (DCS) Write, 1 Parameter (DCSW1-S), Data Type = 01 0101 (15h)

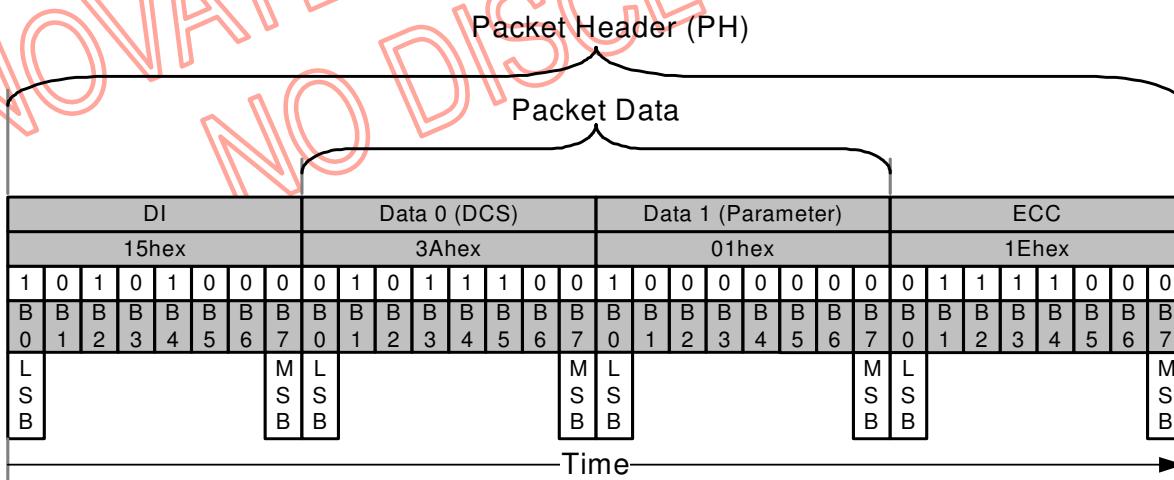
"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0101b), from the MCU to the display module. These commands are defined on a table (See chapter "6 Instruction Description") below.

Command
GAMSET (26h)
TEON (35h)
MADCTR (36h)
COLMOD (3Ah)
DSTBON (4Fh)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCM (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0101b
- Packet Data (PD)
 - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.


Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

Display Command Set (DCS) Write Long (DCSW-L), Data Type = 11 1001 (39h)

"Display Command Set (DCS) Write Long" (DCSW-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 11 1001b), from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters), are defined on a table (See chapter "6 Instruction Description") below

Command
NOP (00h) , Note1
SWRESET (01h) , Note1
SLPIN (10h) , Note1
SLPOUT (11h) , Note1
NORON (13h) , Note1
INVOFF (20h) , Note1
INVON (21h) , Note1
GAMSET (26h) , Note2
DISPOFF (28h) , Note1
DISPON (29h) , Note1
TEOFF (34h) , Note1
TEON (35h) , Note2
MADCTR (36h)
IDMOFF (38h) , Note1
IDMON (39h) , Note1
COLMOD (3Ah) , Note2
TEARLINE (44h)
DSTBON (4Fh) , Note2
WRDISBV (51h) , Note2
WRCTRLD (53h)
WRCABC (55h) , Note2
WRCABCMB (5Eh)

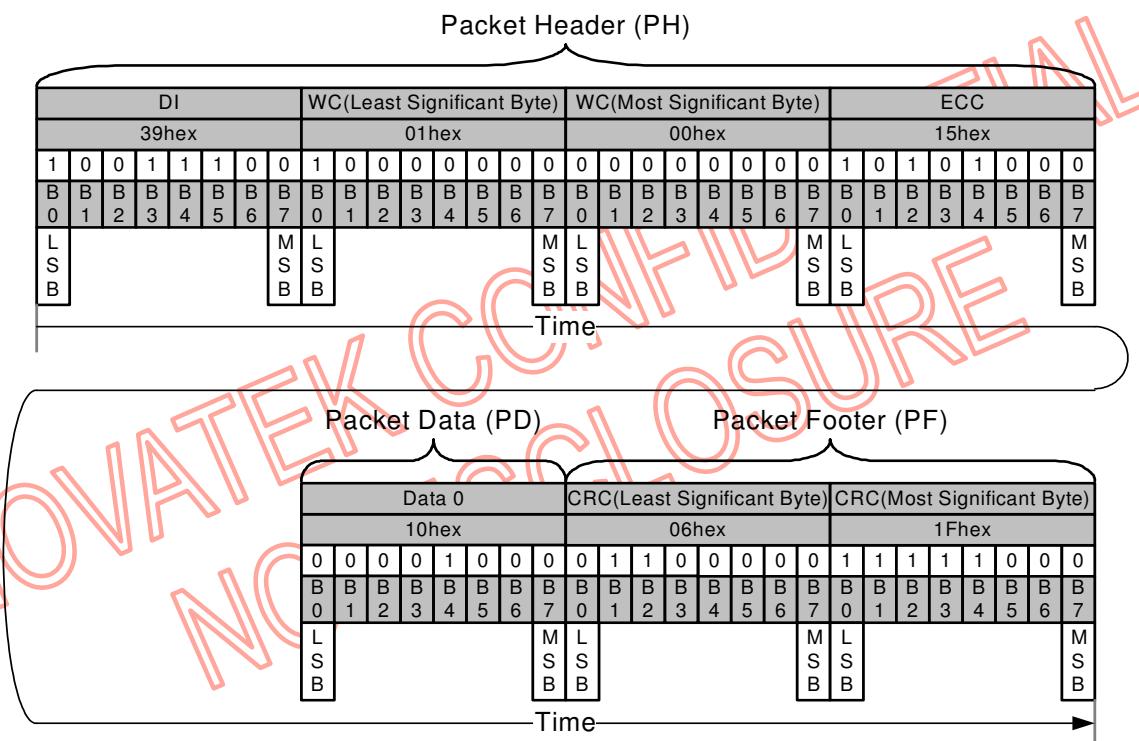
Notes :

1. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, No Parameter.
2. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.

Long Packet (LPA), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

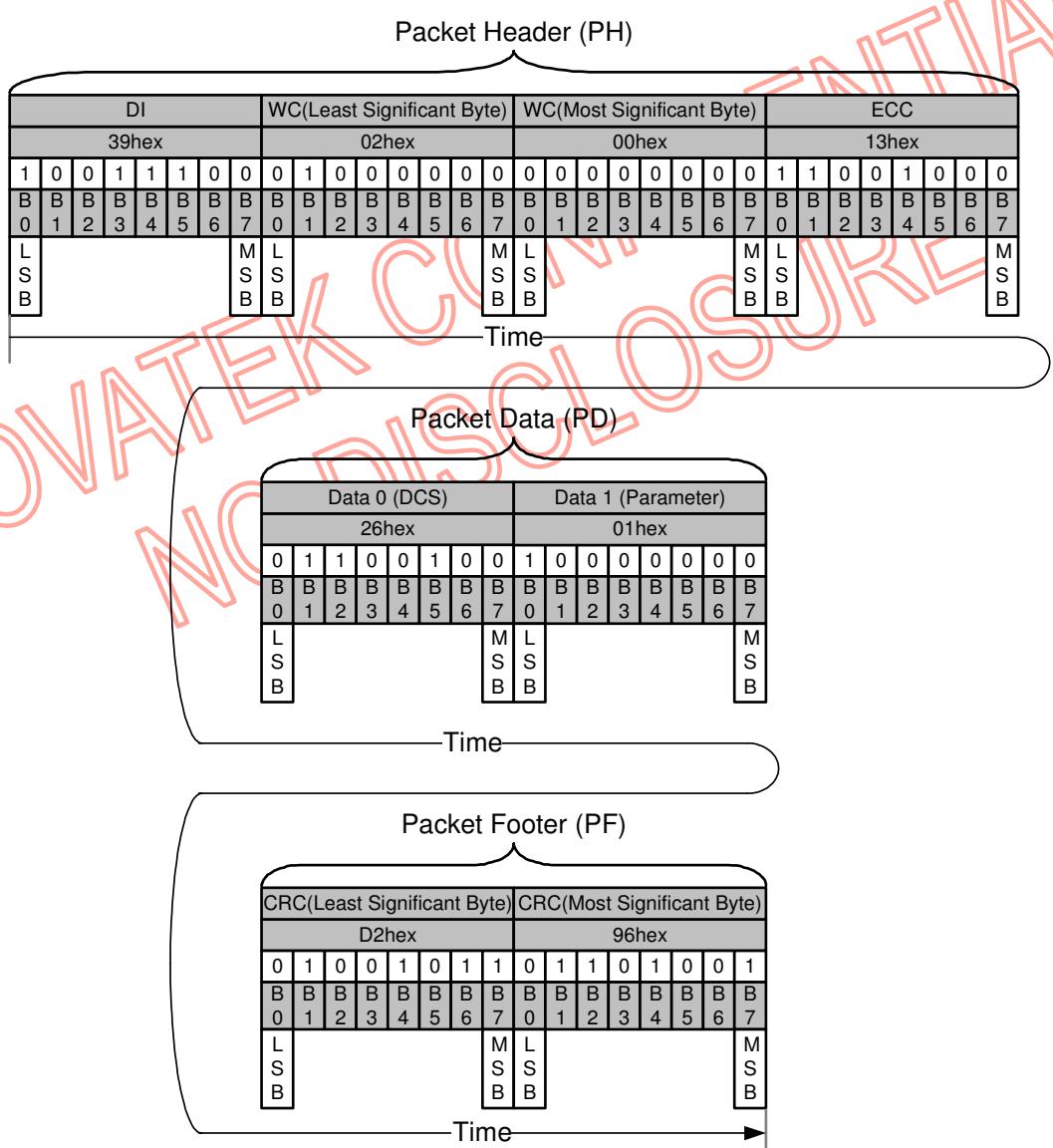


Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

Long Packet (LPA), when a Write (1 parameter) was sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 1001b
- Word Count (WC)
 - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: "Gamma Set (26h)", Display Command Set (DCS)
 - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.



Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

Display Command Set (DCS) Read, No Parameter (DCSRN-S), Data Type = 00 0110 (06h)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0110b), from the MCU to the display module. These commands are defined on a table (See chapter "6 Instruction Description") below.

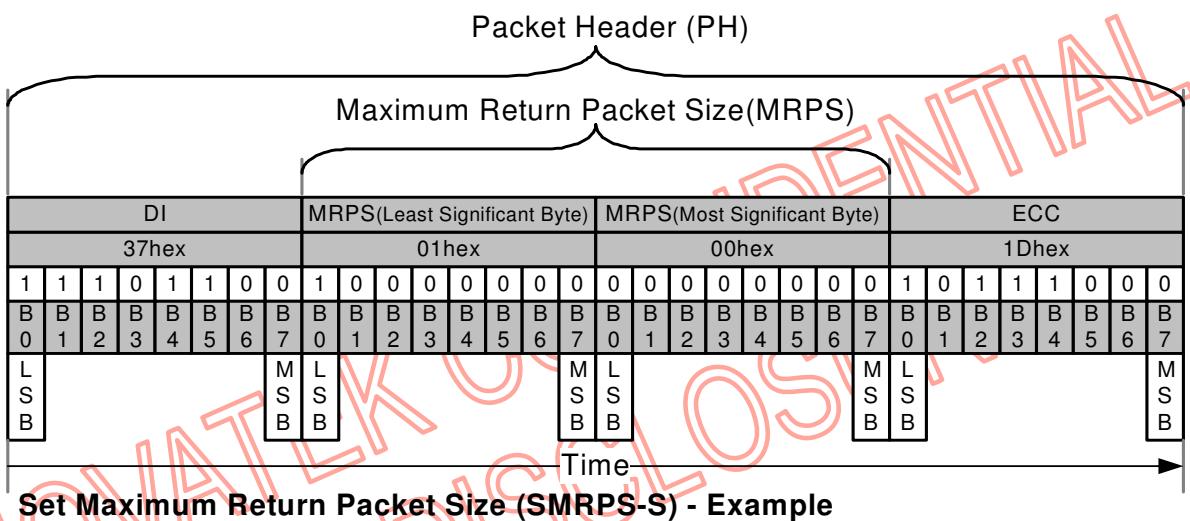
The 1st parameter (Dummy Data) is not returned as it is done in MeSSI-8/16 cases. The first returned parameter is the 2nd parameter in DSI case.

Command
RDDID (04h)
RDBLUE (08h)
RDDPM (0Ah)
RDDMADCTR (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
GSL (45h)
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDCABCMB (5Fh)
RDDDBST (A1h)
RDDDBC (A8h)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

The MCU has to define to the display module, what is the maximum size of the return packet. A command, what is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and which is using Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This same sequence is illustrated for reference purposes below.

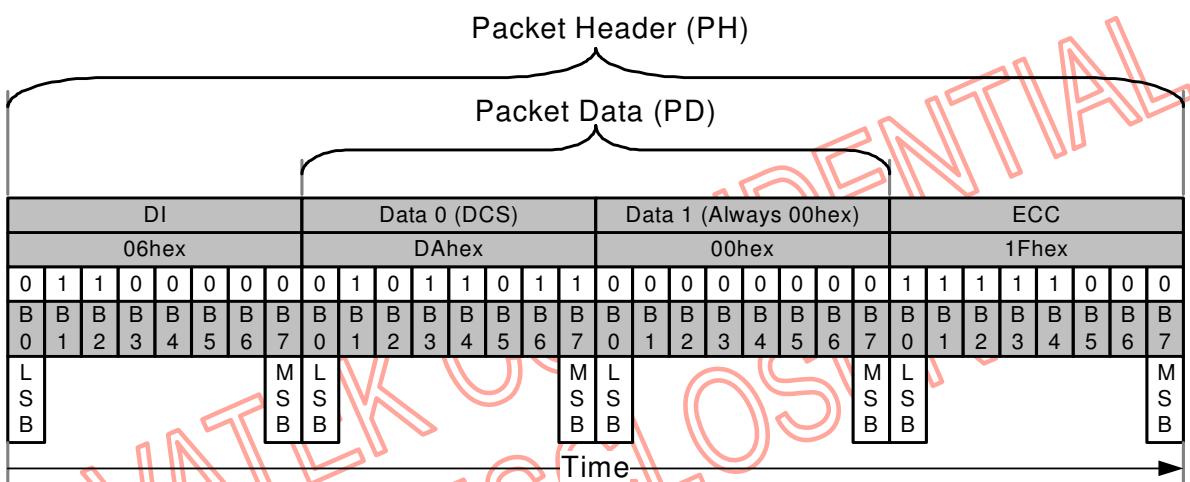
Step 1:

- The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - Data 0: 01hex
 - Data 1: 00hex
- Error Correction Code (ECC)



Step 2:

- The MCU wants to receive a value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0110b
- Packet Data (PD)
 - Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
 - Data 1: Always 00hex
- Error Correction Code (ECC)


Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3: The display module can send 2 different information to the MCU after Bus Turnaround (BTA)

1. An acknowledge with Error Report (AwER), which is using a Short Packet (SPa), if there is an error to receive a command. See section “Acknowledge with Error Report (AwER)”.
2. Information of the received command. Short Packet (SPa) or Long Packet (LPa)

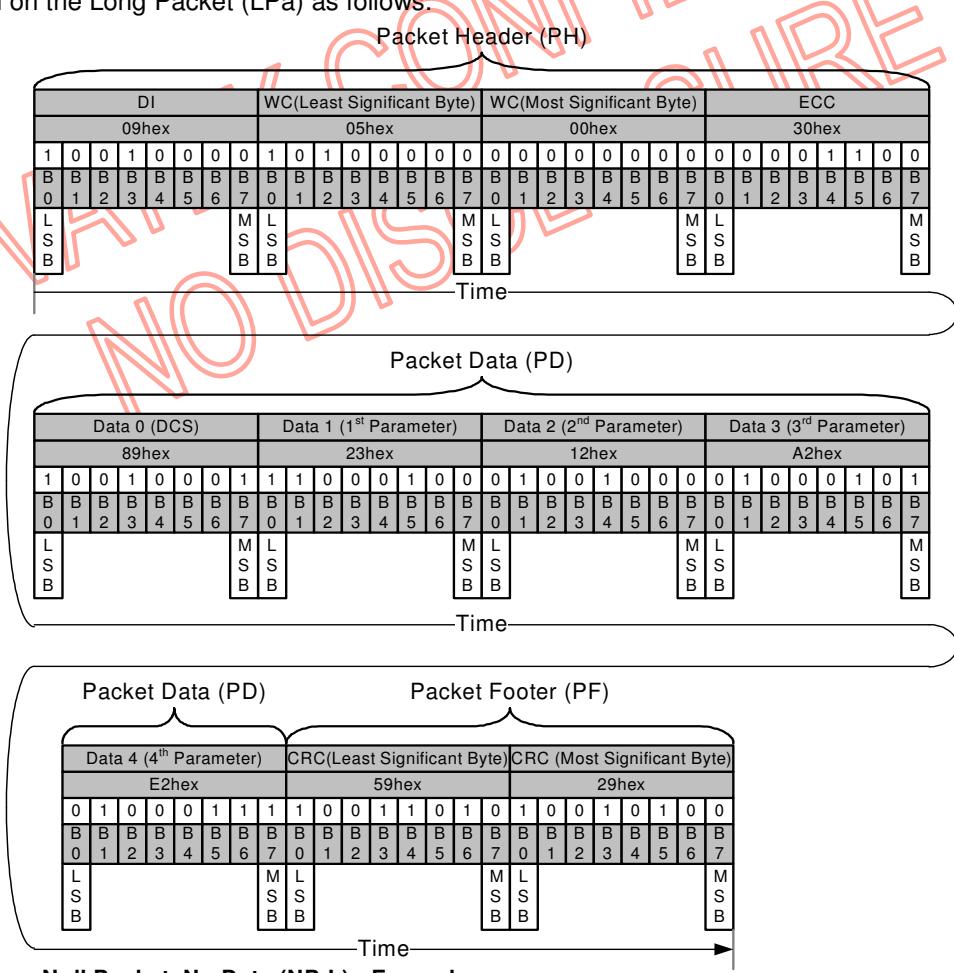
Null Packet, No Data (NP-L), Data Type = 00 1001 (09h)

"Null Packet, No Data" (NP-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 001001b), from the MCU to the display module. The purpose of this command is keeping data lanes in the high speed mode (HSDT), if it is needed. The display module is ignored Packet Data (PD) what the MCU is sending.

Long Packet (LPa), when 5 random data bytes of the Packet Data (PD) were sent, is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1001b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h (Random data)
 - Data 1: 23h (Random data)
 - Data 2: 12h (Random data)
 - Data 3: A2h (Random data)
 - Data 4: E2h (Random data)
- Packet Footer (PF)

This is defined on the Long Packet (LPa) as follows.


Null Packet, No Data (NP-L) - Example

End of Transmission Packet (EoTP), Data Type = 00 1000 (08h)

"End of Transmission Packet" (EoTP) is always using a Short Packet (SPa), what is defined on Data Type (DT, 001000b), from the MCU to the display module. The purpose of this command is terminated the high speed mode (HPDT) properly when there is added this extra packet after the last payload packet before "End of Transmission" (EoT), which is an interface level functionality.

The MCU can decide if it want to use the "End of Transmission Packet" (EoTP) or not. The NT35521 has the capability to support both: i.e. If MCU applies the EoTP, it shall report the "DSI Protocol Violation" error when the EoTP is not detected in the high speed (HS). This error reporting can be enable/disable by bit DIS_EoTP_HS of command B100h (page 0).

The display module is or isn't receiving "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Marked-1" (=leaving Escape mode) what ends the Low Power Data Transmission (LPDT) mode.

The display module is not allowed to send "End of Transmission Packet" (EoTP) to MCU during the Low Power Data Transmission (LPDT) mode.

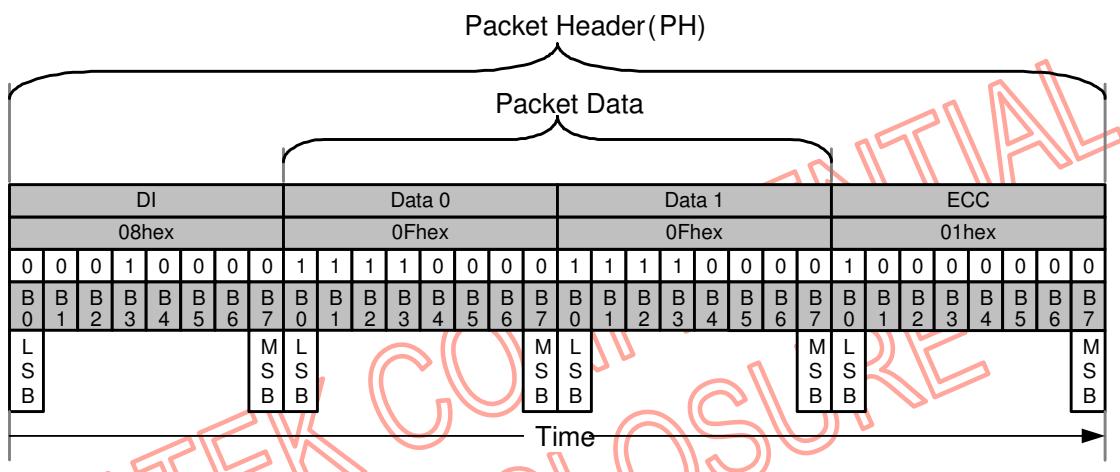
The summary of the receiving and transmitting EoTP is listed below.

Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HPDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Driver	With or Without EoTP is Supported	With or Without EoTP is Supported
Display Driver => MCU	HS Mode is not available (EoTP is not available)	EoTP can not be sent by the Display Driver

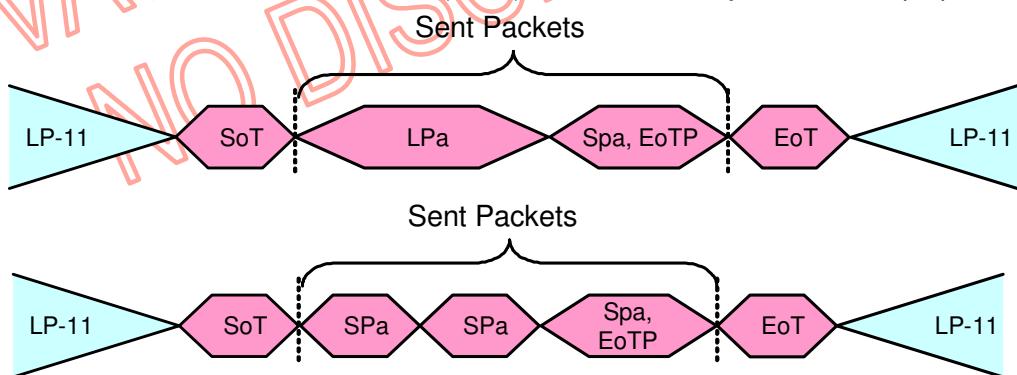
Short Packet (SPa) is using a fixed format as follow

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 1000b
- Packet Data (PD):
 - Data 0: 0Fh
 - Data 1: 0Fh
- Error Correction Code (ECC)
 - ECC: 01h



End of Transmission Packet (EoTP)

Some use case of the “End of Transmission Packet” (EoTP) are illustrated only for reference purpose below.



End of Transmission Packet (EoTP) - Examples

Sync Event (H Start, H End, V Start, V End), Data Type = xx 0001 (x1h)

Sync Events are Short packets and, therefore, can time-accurately represent events like the start and end of sync pulses. As “start” and “end” are separate and distinct events, the length of sync pulses, as well as position relative to active pixel data, e.g. front and back porch display timing, may be accurately conveyed to the peripheral. The Sync Events are defined as follows:

- Data Type = 00 0001 (01h) V Sync Start
- Data Type = 01 0001 (11h) V Sync End
- Data Type = 10 0001 (21h) H Sync Start
- Data Type = 11 0001 (31h) H Sync End

In order to represent timing information as accurately as possible a V Sync Start event represents the start of the VSA and also implies an H Sync Start event for the first line of the VSA. Similarly, a V Sync End event implies an H Sync Start event for the last line of the VSA..

Sync events should occur in pairs, Sync Start and Sync End, if accurate 1054 pulse-length information needs to be conveyed. Alternatively, if only a single point (event) in time is required, a single sync event (normally, Sync Start) may be transmitted to the peripheral. Sync events may be concatenated with blanking packets to convey inter-line timing accurately and avoid the overhead of switching between LPS and HS for every event. Note there is a power penalty for keeping the data line in HS mode, however. Display modules that do not need traditional sync/blanking/pixel timing should transmit pixel data in a high-speed burst then put the bus in Low Power Mode, for reduced power consumption. The recommended burst size is a scan line of pixels, which may be temporarily stored in a line buffer on the display module.

Color Mode On Command, and, Data Type = 01 0010 (12h)

Color Mode On is a Short packet command that switches a Video Mode display module to 8-colors mode for power saving.

Color Mode Off Command, Data Type = 00 0010 (02h)

Color Mode Off is a Short packet command that returns a Video Mode display module from 8-colors mode to normal display operation.

Shutdown Peripheral Command, Data Type = 10 0010 (22h)

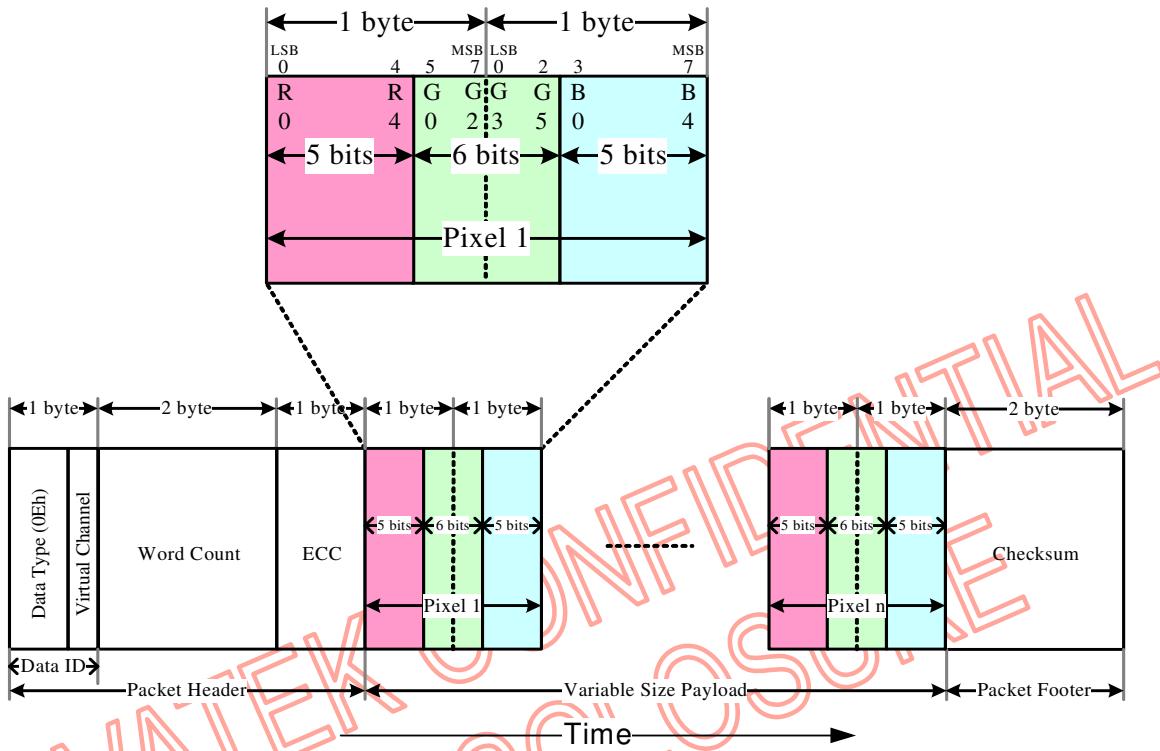
Shutdown Peripheral command is a Short packet command that turns off the display in a Video Mode display module for power saving. Note the interface shall remain powered in order to receive the turn-on, or wake-up, command.

Turn On Peripheral Command, Data Type = 11 0010 (32h)

Turn On Peripheral command is Short packet command that turns on the display in a Video Mode display module for normal display operation.

Blanking Packet (Long), Data Type = 01 1001 (19h)

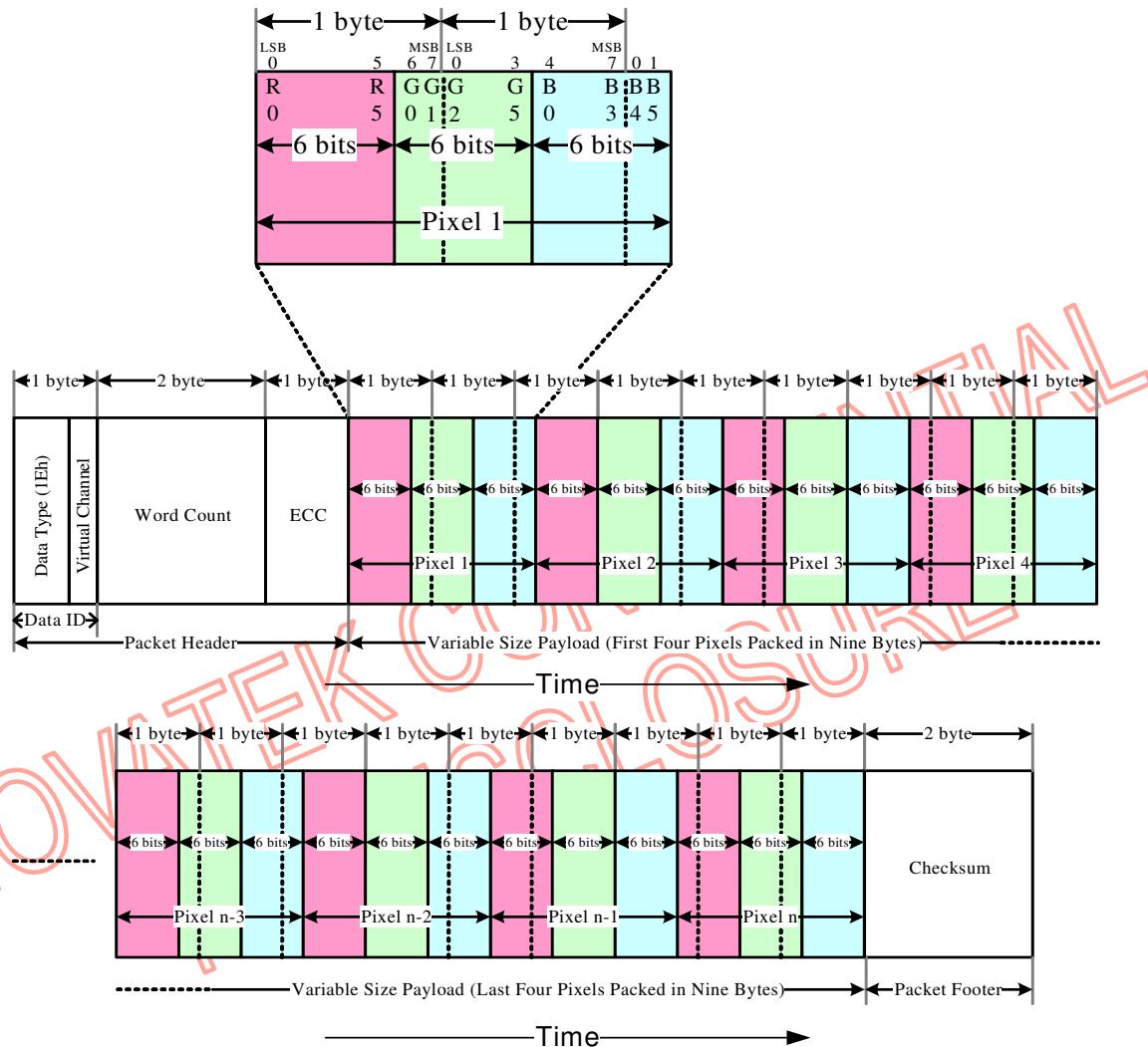
A Blanking packet is used to convey blanking timing information in a Long packet. Normally, the packet represents a period between active scan lines of a Video Mode display, where traditional display timing is provided from the host processor to the display module. The blanking period may have *Sync Event* packets interspersed between blanking segments. Like all packets, the Blanking packet contents shall be an integer number of bytes. Blanking packets may contain arbitrary data as payload. The Blanking packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte checksum.

Packed Pixel Stream, 16-bit Format, Long packet, Data Type = 00 1110 (0Eh)

16-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the "Green" component is split across two bytes. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

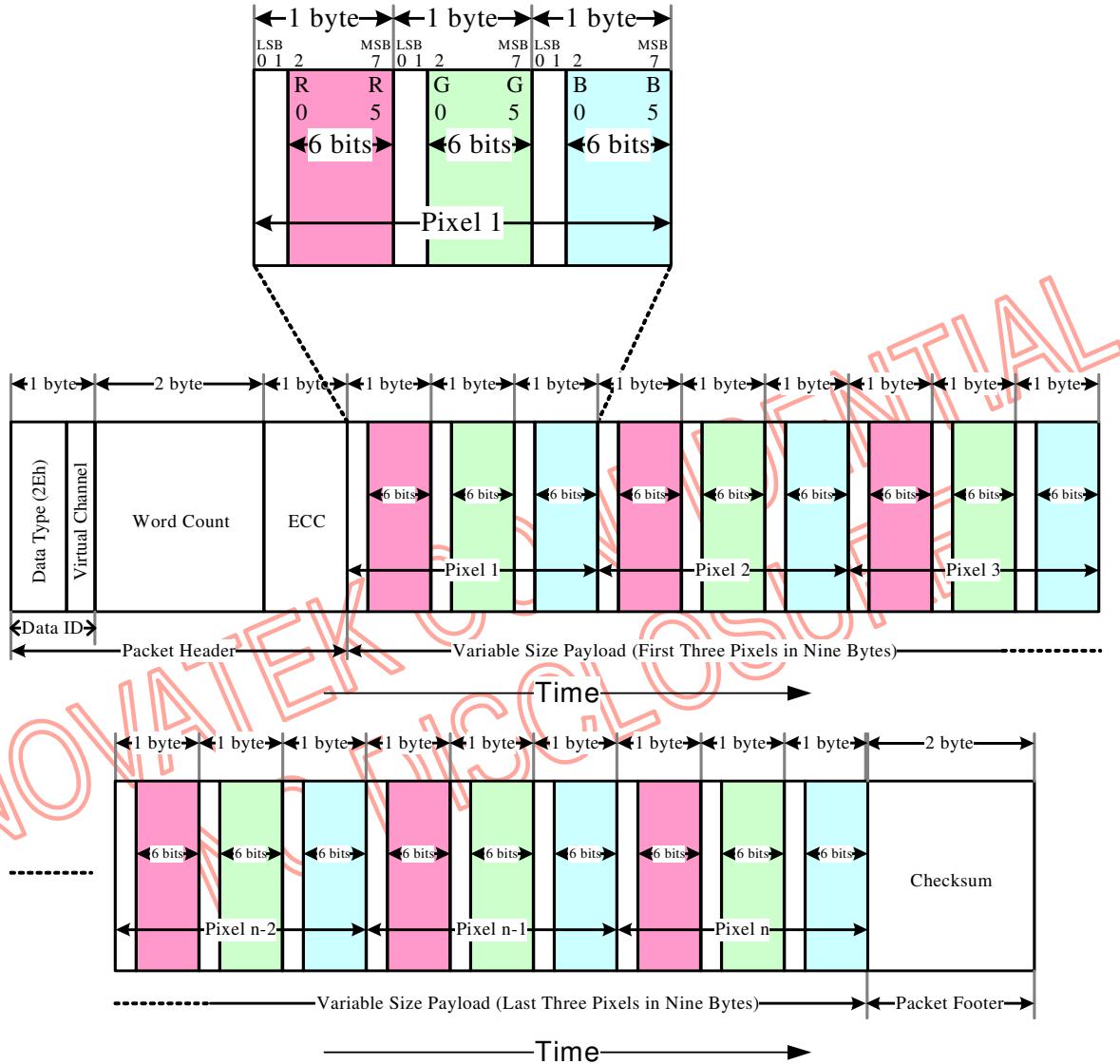
Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

Packed Pixel Stream, 18-bit Format, Long packet, Data type = 01 1110 (1Eh)

18-bit per Pixel (Packed)—RGB Color Format, Long packet

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

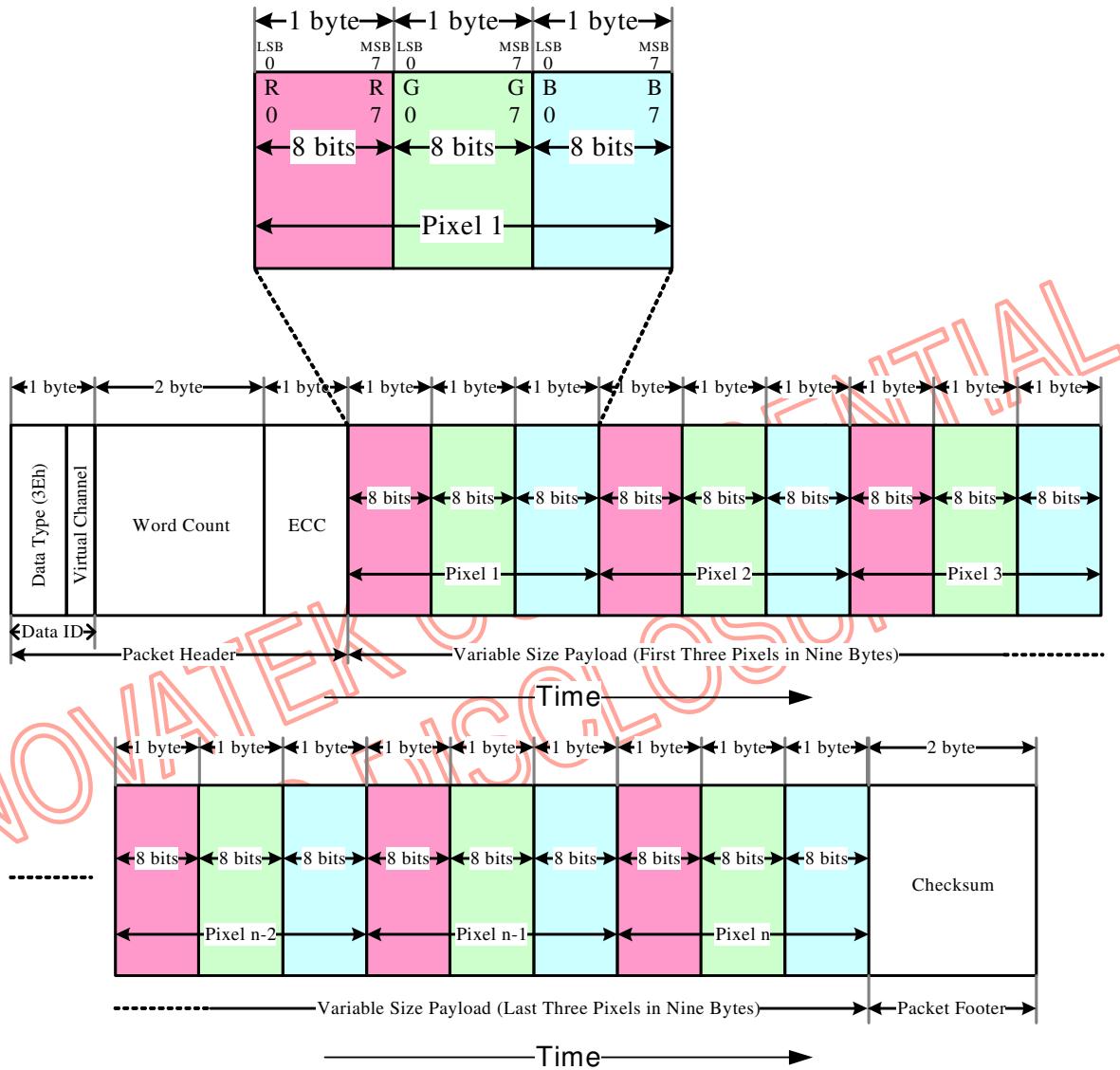
With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

Pixel Stream, 18-bit Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)

18-bit per Pixel (Loosely Packed)—RGB Color Format, Long packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

Packed Pixel Stream, 24-bit Format, Long packet, Data Type = 11 1110 (3Eh)

24-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

5.2.2.3.2.2 Packet from the Display Module to the MCU

Used Packet Types

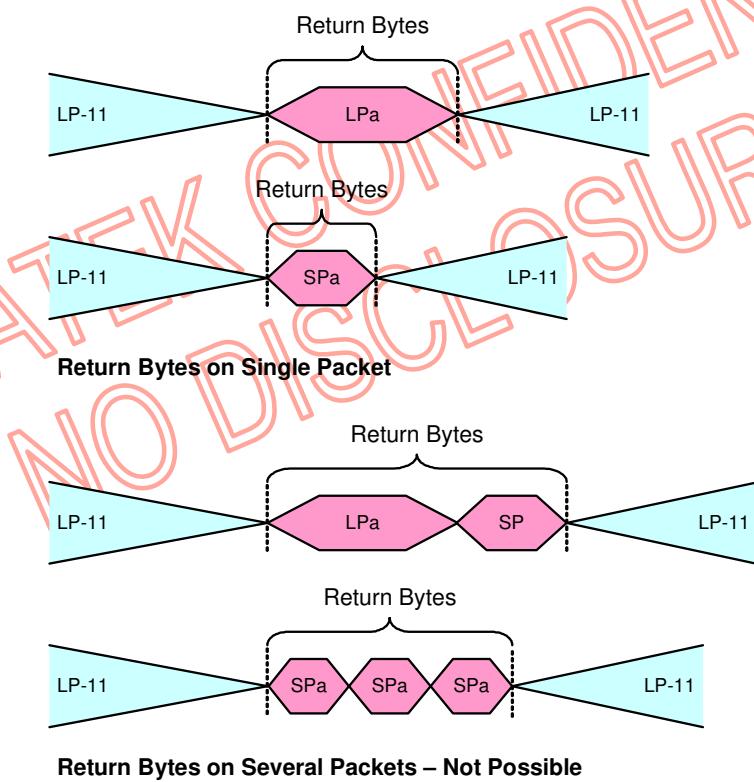
The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See chapter “5.2.2.3.2.1 Display Command Set (DCS) Read, No Parameter” (DCSRN-S)) or an Acknowledge with Error Report (See chapter: “5.2.2.3.2.2 Acknowledge with Error Report (AwER)” (AwER)).

The used packet type is defined on Data Type (DT). See chapter “5.2.2.3.1.3 Data Type (DT)”.

A number of the return bytes are more than the maximum size of the Packet Data (PD) on Long Packet (LPa) or Short Packet (SPa) when the display module is sending return bytes in several packets until all return bytes have been sent from the display module to the MCU.

It is not possible that the display module is sending return bytes in several packets even if the maximum size of the Packet Data (PD) could be sent on a packet.

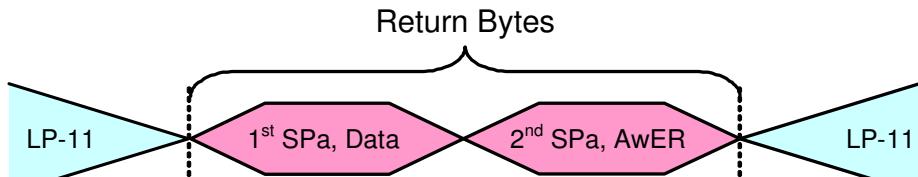
Both cases are illustrated for reference purposes below.



Data Types for Display Module-sourced Packets

Data Type Hex	Data Type Binary	Symbol	Description	Packet Size
02h	00 0010	AwER	Acknowledge & Error Report	Short
1Ch	01 1100	DCSRR-L	DCS Long Read Response	Long
21h	10 0001	DCSRR1-S	DCS Short Read Response, 1 Byte returned	Short
22h	10 0010	DCSRR2-S	DCS Short Read Response, 2 Byte returned	Short
1Ah	01 1010	GENRR-L	Generic Long Read Response	Long
11h	01 0001	GENRR1-S	Generic Short Read Response, 1 Byte returned	Short
12h	01 0010	GENRR2-S	Generic Short Read Response, 2 Byte returned	Short

The display module is return 2 packets (1st packet: Data, 2nd packet Acknowledge with Error Report) to the MCU when the display module has received a read command. See section “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” where has been detected and corrected a single bit error by the EEC (See bit 8 on Table “Acknowledge with Error Report (AwER) for Short Packet (SPa) Response”). This return packets are illustrated for reference purpose below.



AwER = Acknowledge with Error Report

Exception when Return Bytes on Several Packet

**NOVATEK CONFIDENTIAL
NO DISCLOSURE**

Acknowledge with Error Report (AwER), Data Type = 00 0010(02h)

"Acknowledge with Error Report" (AwER) is always using a Short Packet (SPa), what is defined on Data Type (DT, 00 0010b), from the display module to the MCU.

The Packet Data (PD) can include bits, which are defining the current error, when a corresponding bit is set to '1', as they are defined on the following table.

Acknowledge with Error Report (AwER) for Long Packet (LPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

Acknowledge with Error Report (AwER) for Short Packet (SPa) Response

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Set to "0" internally (Only for Long Packet (LP))
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to '0' internally
15	DSI Protocol Violation

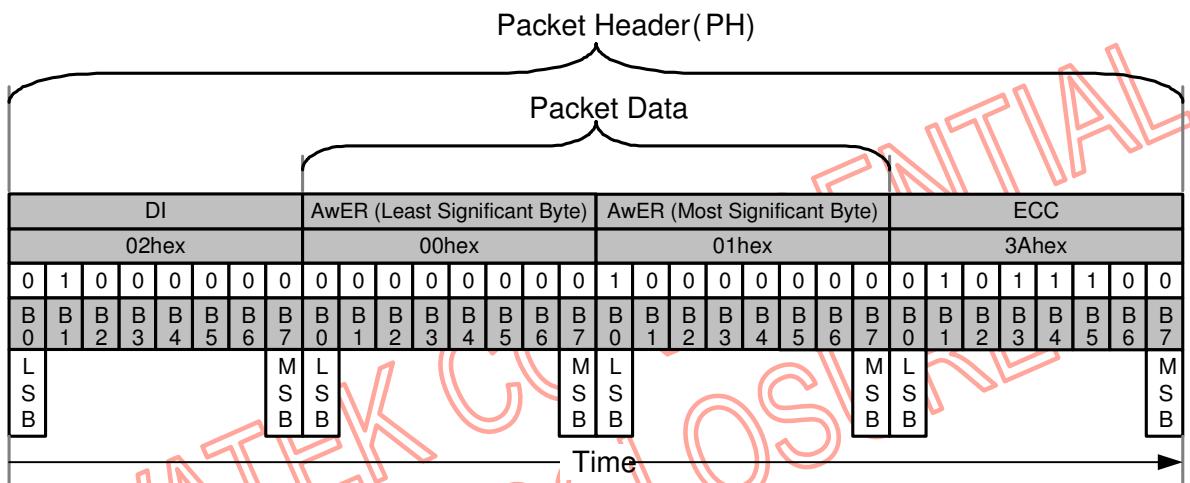
These errors are only included on the last packet, which has been received from the MCU to the display module before Bus Turnaround (BTA).

The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of the Short Packet (SPa) is defined e.g.

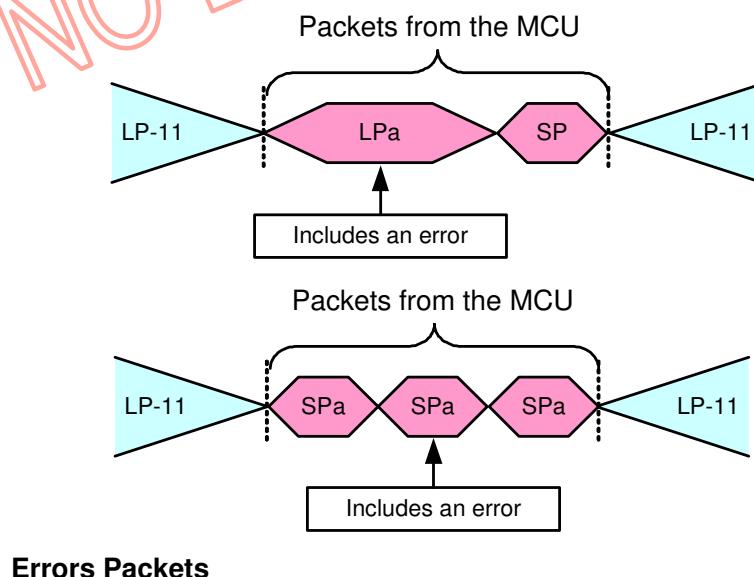
- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 00 0010b
- Packet Data (PD):
 - Bit 8: ECC Error, single-bit (detected and corrected)
 - AwER: 0100h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.



Acknowledge with Error Report (AwER) – Example

It is possible that the display module has received several packets, which have included errors, from the MCU before the MCU is doing Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

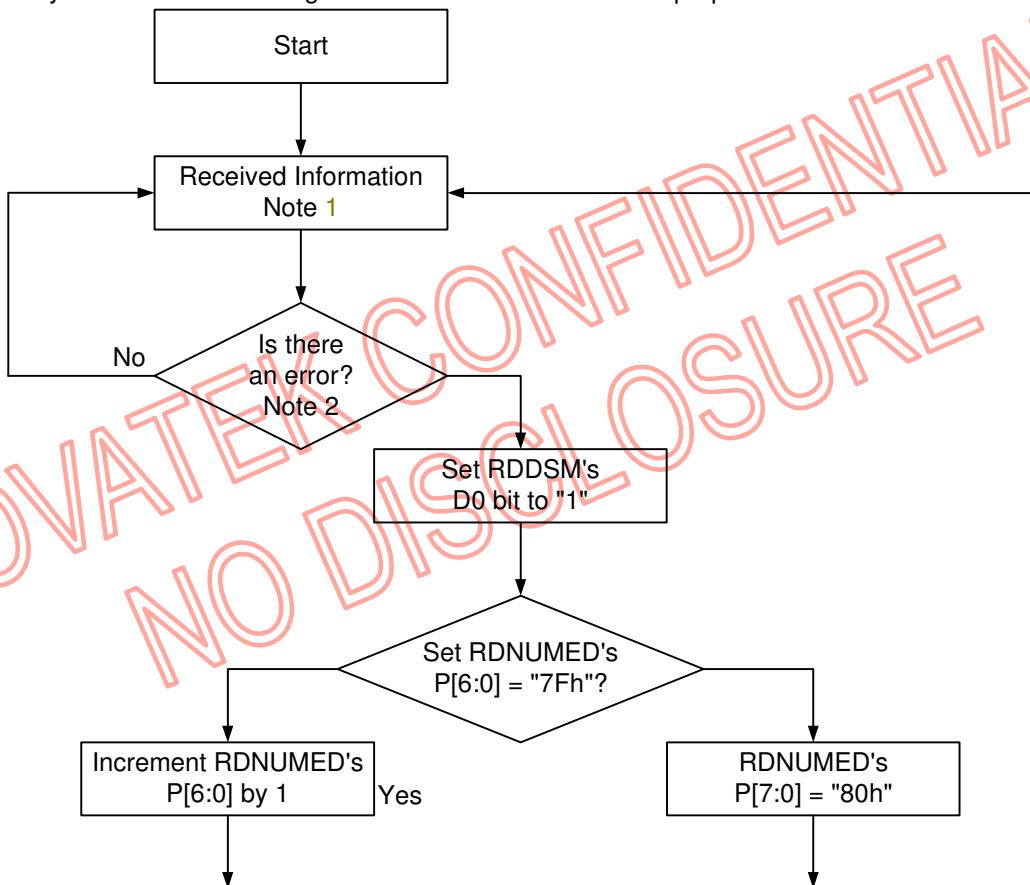


Therefore, there is needed a method to check if there has been errors on the previous packets. These errors of the previous packets can check “Read Display Signal Mode (0Eh)” and “Read Number of the Errors on DSI (05h)” commands.

The bit D0 of the “Read Display Signal Mode (0Eh)” command has been set to ‘1’ if a received packet includes an error.

The numbers of the packets, which are including an ECC or CRC error, are calculated on the RDNUMED register, which can read “Read Number of the Errors on DSI (05h)” command. This command also sets the RDNUMED register to 00h as well as set the bit D0 of the “Read Display Signal Mode (0Eh)” command to ‘0’ after the MCU has read the RDNUMED register from the display module.

The functionality of the RDNUMED register is illustrated for reference purposes below.



Notes:

1. *This information can Interface or Packet Level Communication but it is always from the MCU to the display module in this case.*
2. *CRC or ECC error.*

DCS Read Long Response (DCSRR-L), Data Type = 01 1100(1Ch)

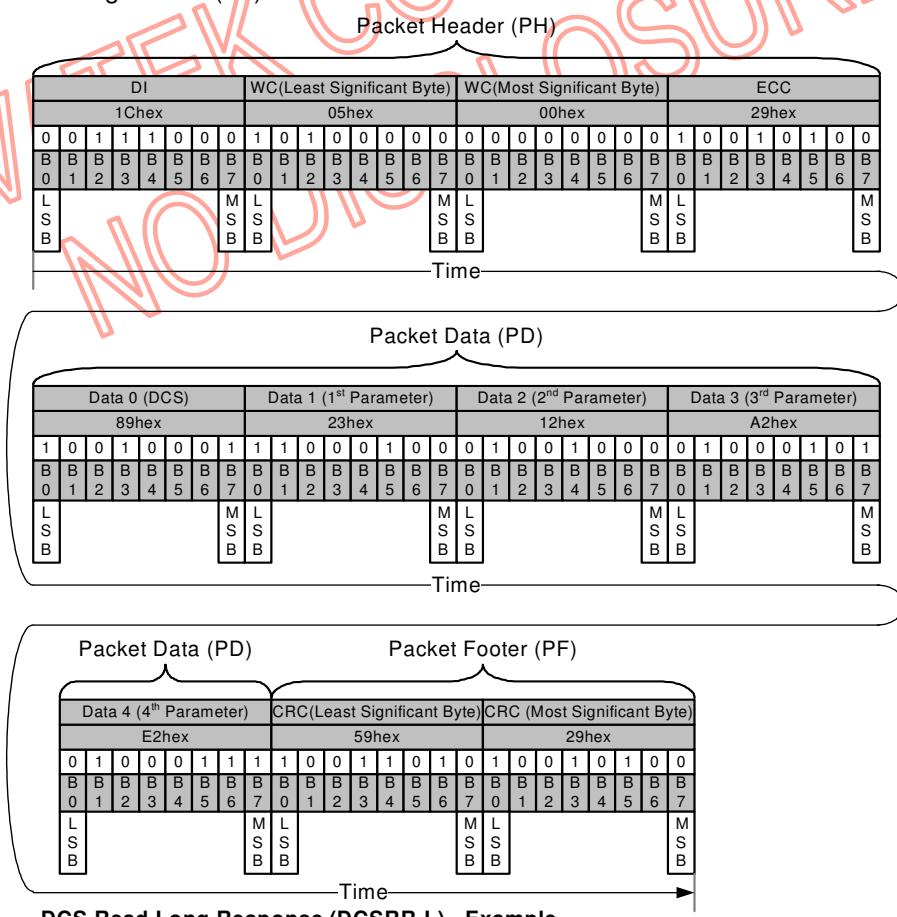
“DCS Read Long Response” (DCSRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1100b), from the display module to the MCU. “DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

“DCS Read Long Response” (DCSRR-L) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 1100b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - Data 0: 89h
 - Data 1: 23h
 - Data 2: 12h
 - Data 3: A2h
 - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.



DCS Read Long Response (DCSRR-L) - Example

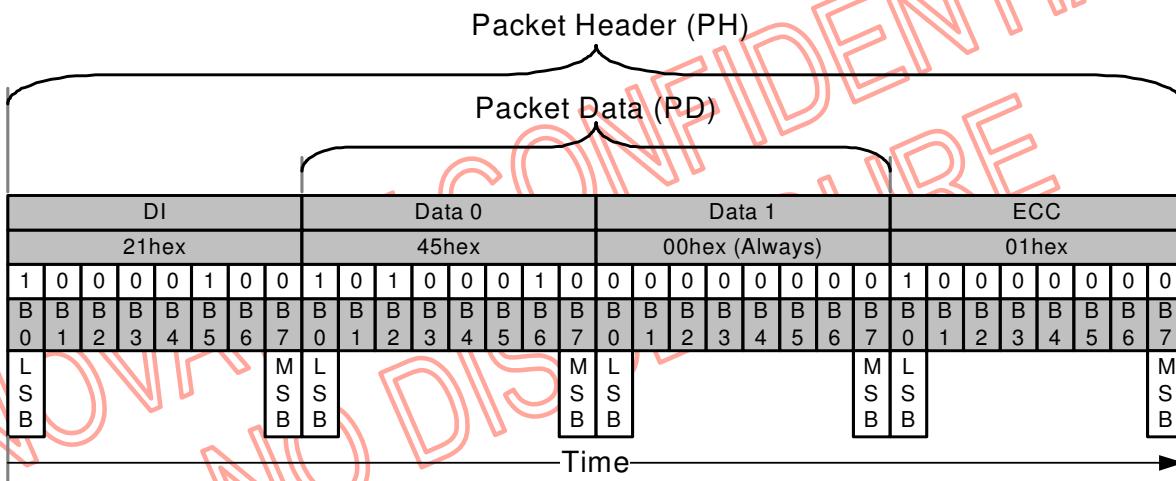
DCS Read Short Response, 1 Byte Returned (DCSRR1-S), Data Type = 10 0001(21h)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0001b), from the display module to the MCU. “DCS Read Short Response, 1 Byte Returned” (DCSRR1-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0001b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.


DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

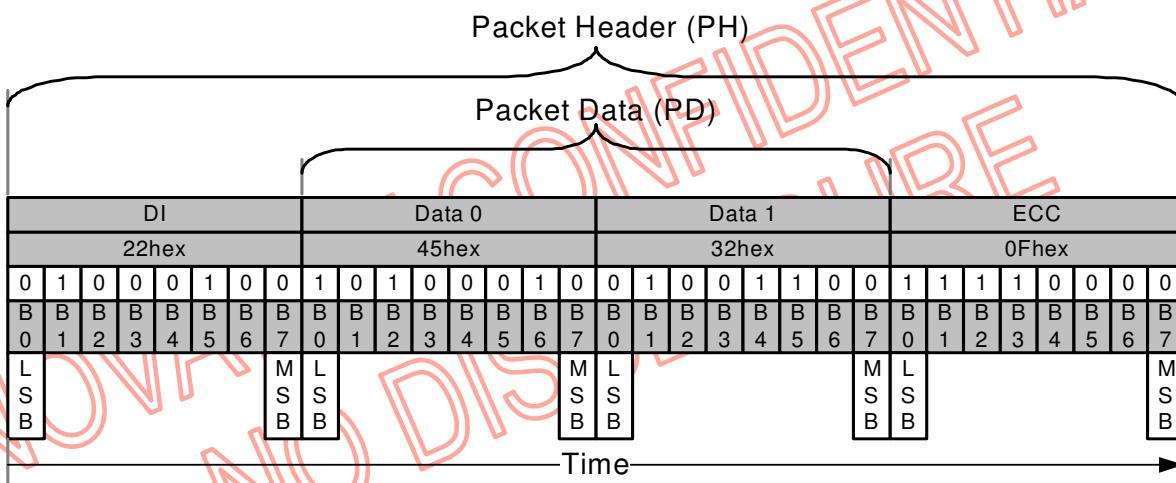
DCS Read Short Response, 2 Bytes Returned (DCSRR2-S), Data Type = 10 0010(22h)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 10 0010b), from the display module to the MCU. “DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to response a DCS Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 10 0010b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.


DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

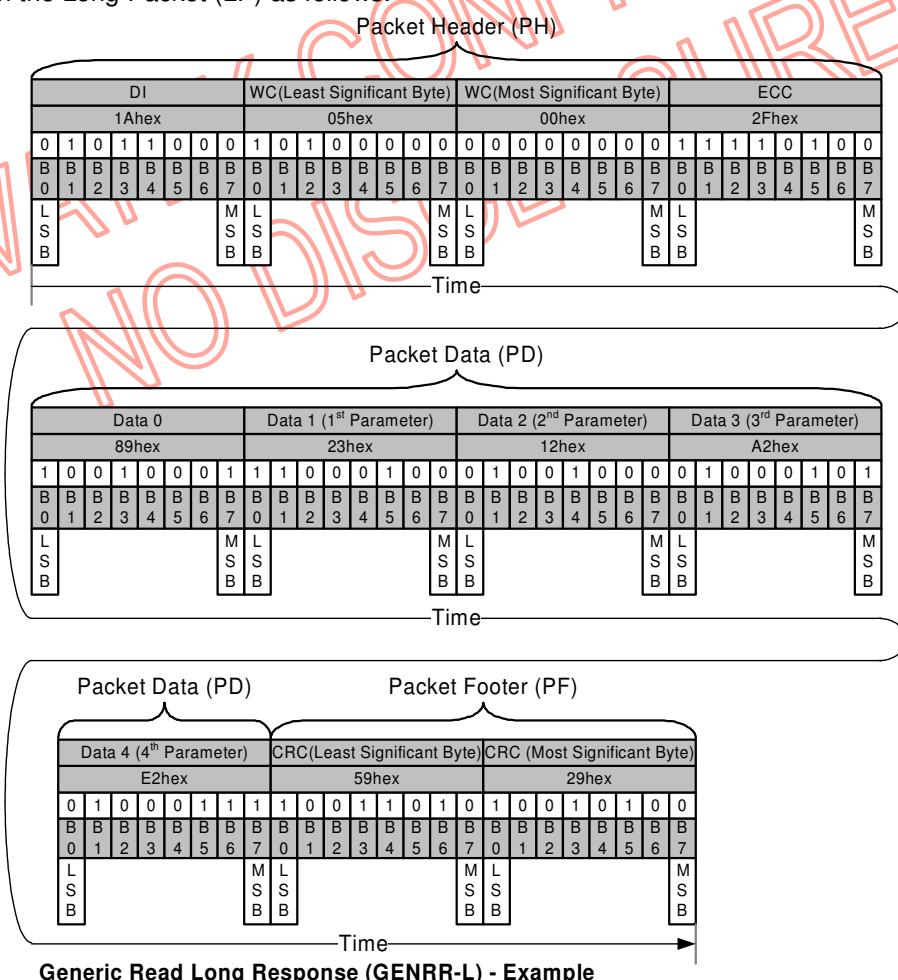
Generic Read Long Response (GENRR-L), Data Type = 01 1010(1Ah)

"Generic Read Long Response" (GENRR-L) is always using a Long Packet (LPa), what is defined on Data Type (DT, 01 1010b), from the display module to the MCU. "Generic Read Long Response" (GENRR-L) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 1010b
- Word Count (WC)
 - Word Count (WC): 0005h
- Error Correction Code (ECC)
 - Data 0: 89h
 - Data 1: 23h
 - Data 2: 12h
 - Data 3: A2h
 - Data 4: E2h
- Packet Footer (PF)

This is defined on the Long Packet (LP) as follows.


Generic Read Long Response (GENRR-L) - Example

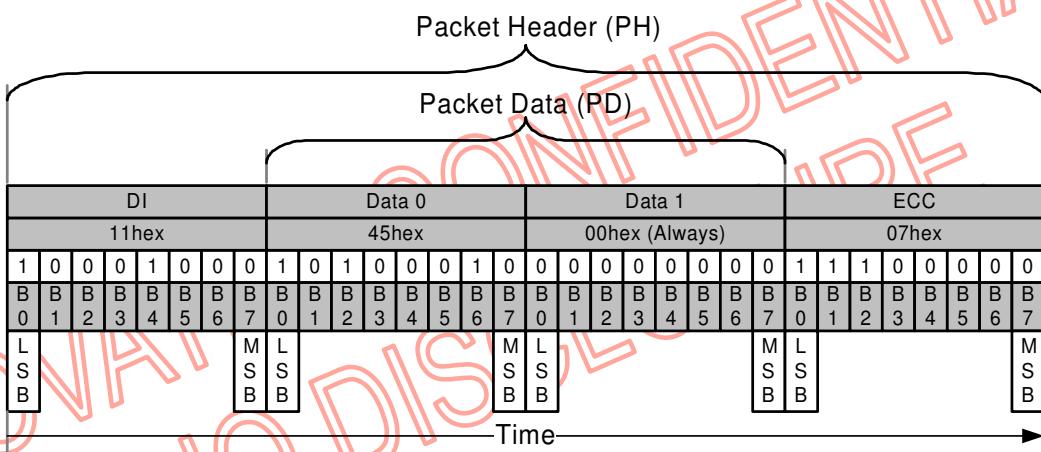
Generic Read Short Response, 1 Byte Returned (GENRR1-S), Data Type = 01 0001(11h)

"Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0001b), from the display module to the MCU. "Generic Read Short Response, 1 Byte Returned" (GENRR1-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0001b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 00h (Always)
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.



Generic Read Short Response, 1 Byte Returned (GENRR1-S) - Example

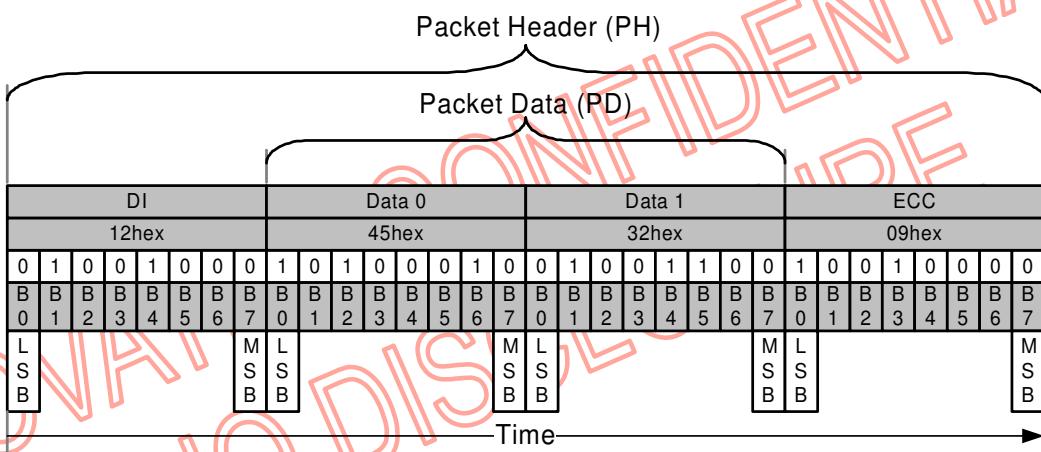
Generic Read Short Response, 2 Bytes Returned (GENRR2-S), Data Type = 01 0010(12h)

"Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is always using a Short Packet (SPa), what is defined on Data Type (DT, 01 0010b), from the display module to the MCU. "Generic Read Short Response, 2 Bytes Returned" (GENRR2-S) is used when the display module wants to response a Generic Read command, which the MCU has sent to the display module.

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
 - Virtual Channel (VC, DI[7...6]): 00b
 - Data Type (DT, DI[5...0]): 01 0010b
- Packet Data (PD):
 - Data 0: 45h
 - Data 1: 32h
- Error Correction Code (ECC)

This is defined on the Short Packet (SP) as follows.


Generic Read Short Response, 2 Bytes Returned (GENRR2-S) - Example

5.2.2.3.3 Communication Sequences

5.2.2.3.3.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See chapters “Interface Level Communication” and “Packet Level Communication”.

This communication sequence description is for DSI data lanes and it has been assumed that the needed low level communication is done on DSI clock lanes (DSI-CLK+/-) automatically.

Functions of the interface level communication are described on the following table.

Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra-Low power state
	RAR	Remote application reset
	TEE	Tearing effect event (Not supported)
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Functions of the packet level communication are described on the following table.

Packet Level Communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write, Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AWER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

5.2.2.3.3.2 Sequences

DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" is defined on chapter "Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)" and example sequences, how this packet is used, is described on following tables.

DCS Write, 1 Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, 1 Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Write, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, No Parameter Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

DCS Write, Long Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 2

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

DCS Write, Long Sequence - Example 3

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	
5	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
6	-	-	<=	LP-11	-	If no error => goto line 8 If error => goto line 13
7						
8	-	-	<=	ACK	-	No error
9	-	-	<=	LP-11	-	
10	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
11	-	LP-11	=>	-	-	End
12						
13	-	-	<=	LPDT	AwER	Error report
14	-	-	<=	LP-11	-	
15	-	BTA	<=>	BTA	-	
16	-	LP-11	=>	-	-	End

DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

DCS Read, No Parameter Sequence - Example 1

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5	-	LP-11	=>	-	-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error => goto line 9 If error => goto line 14 If error is corrected by ECC => go to line 19
8						
9	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>	-	-	End

Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Null Packet, No Parameter Sequence - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoT)” is defined on chapter “End of Transmission Packet (EoT)” and an example sequences, how this packet is used, is described on following tables.

End of Transmission Packet - Example

Line	MCU		Information Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
2	EoTP	HSDT	=>	-	-	End of Transmission Packet
3	-	LP-11	=>	-	-	End

5.2.2.4 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

5.2.2.4.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame, shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

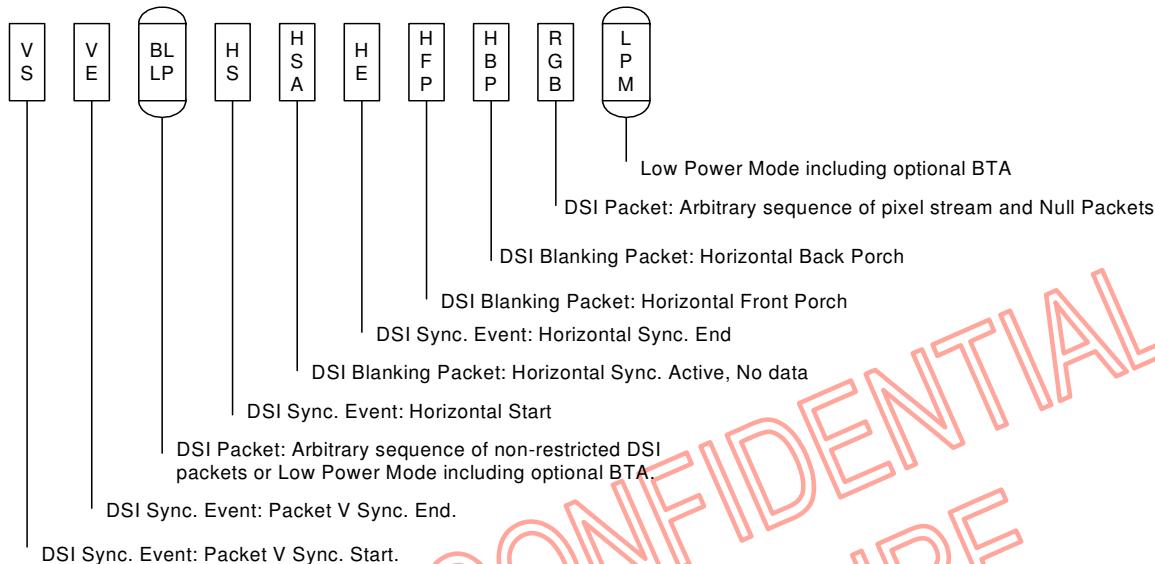
During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary, a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in Figure below unless otherwise specified.



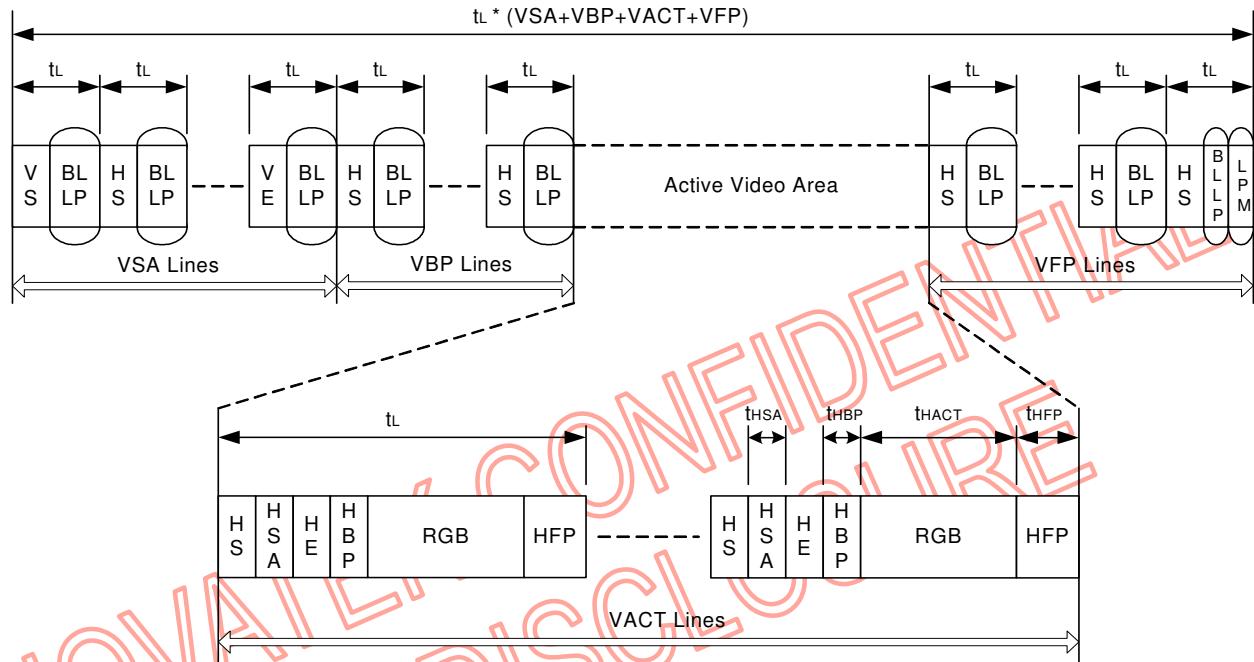
DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

**NOVATEK CONFIDENTIAL
NO DISCLOSURE**

5.2.2.4.2 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in Figure below.

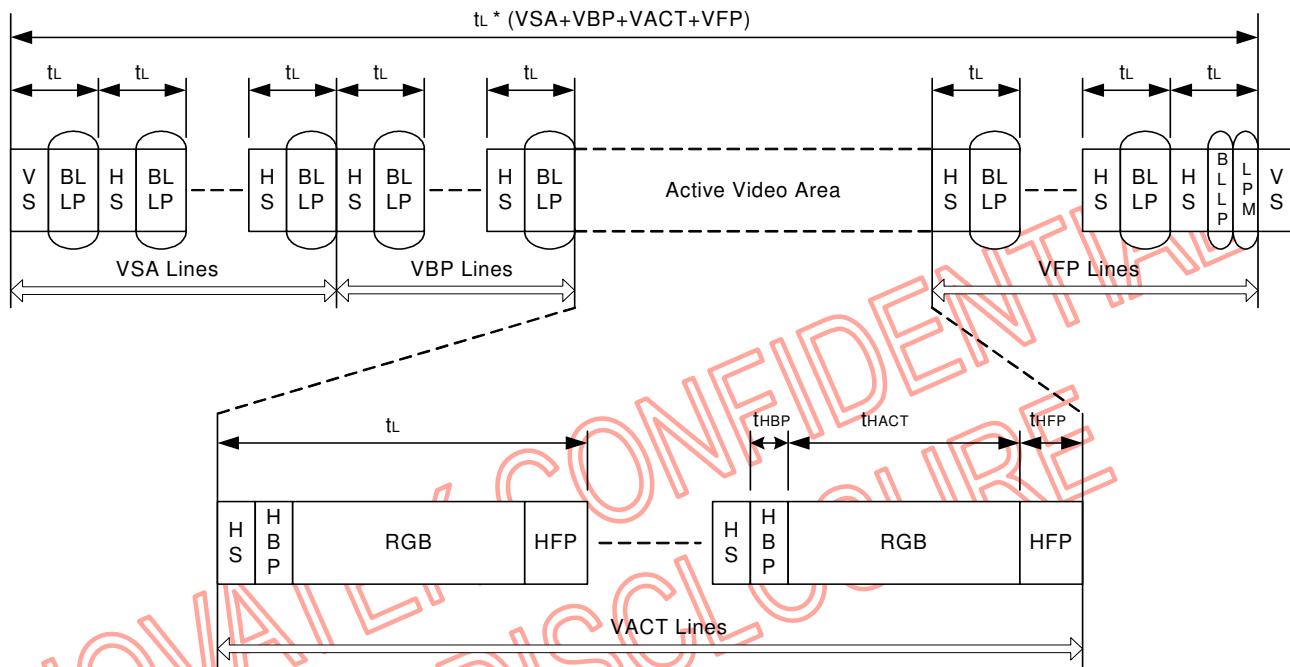


DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.2.2.4.3 Non-Burst Mode

This mode is a simplification of the format described in section 5.2.2.4.2 “Non-Burst Mode with Sync Pulse”. Only the start of each synchronization pulse is transmitted. The peripheral may regenerate sync pulses as needed from each Sync Event packet received. Pixels are transmitted at the same rate as they would in a corresponding parallel display interface such as DPI-2. An example of this mode is shown in Figure below.

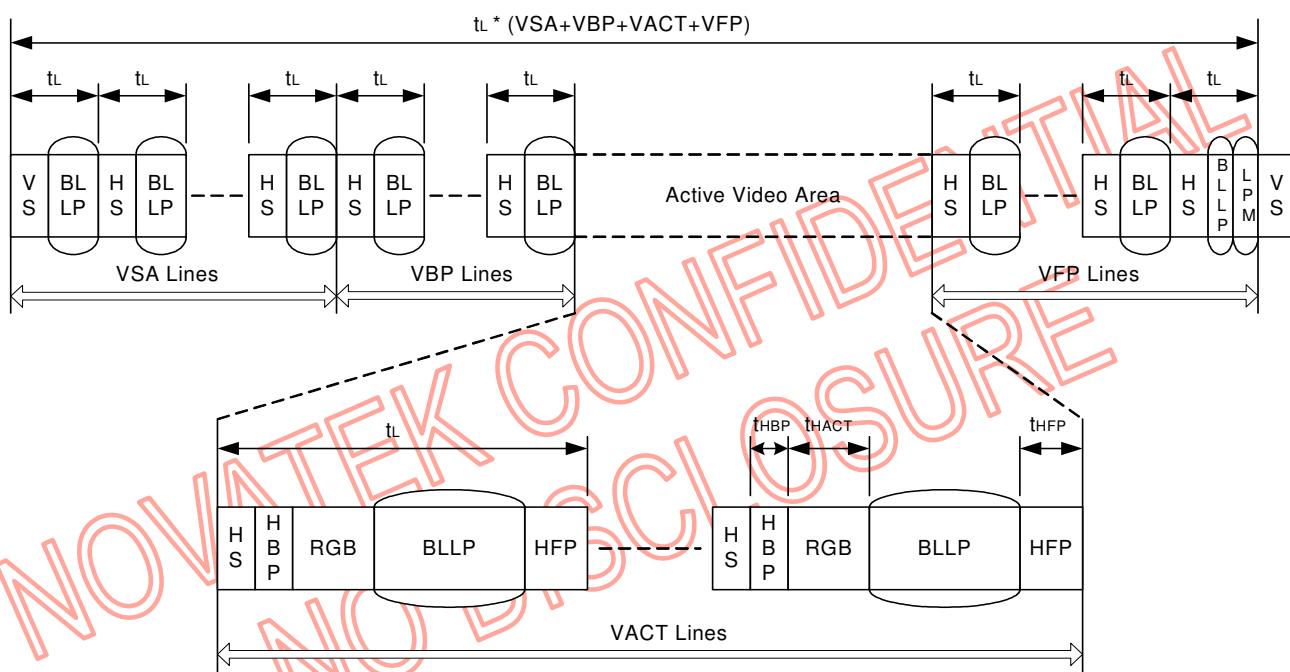


DSI Video Mode Interface Timing: Non-burst Transmission

As with the previous Non-Burst Mode, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.2.2.4.4 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in Figure below.



DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.2.2.4.5 Parameters

Below table documents the parameters used in the preceding figures. Peripheral supplier companies are responsible for specifying suitable values for all blank fields in the table. The host processor shall meet these requirements to ensure interoperability.

Required Peripheral Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Units
BRPHY	Bit rate total on all Lanes	WXGA	250	-	850	Mbps
tL	Line time	WXGA	-	12.8, Note1	-	us
tHBP	Horizontal back porch	WXGA	0.5	-	-	us
tHACT	Time for image data	4 data lanes	5.65, Note3	-	19.2	us
HACT	Active pixels per line	WXGA	-	800	-	pixels
tHFP	Horizontal front porch	-	0.5	-	-	us
VSA	Vertical sync active	-	1	-	-	H
VBP	Vertical back porch	-	Note2	-	-	H
VACT	Active lines per frame	WXGA	-	1280	-	H
VFP	Vertical front porch	-	6	-	-	H

Note1: Frame rate (Typ)=60Hz.

Note2: VBP (min) value are dependent on GOA timing.

Note3: $tHACT+tHBP+tHFP \geq tL = (SDT[5:0] \times 10 + EQS3[4:0] \times 5 + 440) / 50\text{MHz}$.

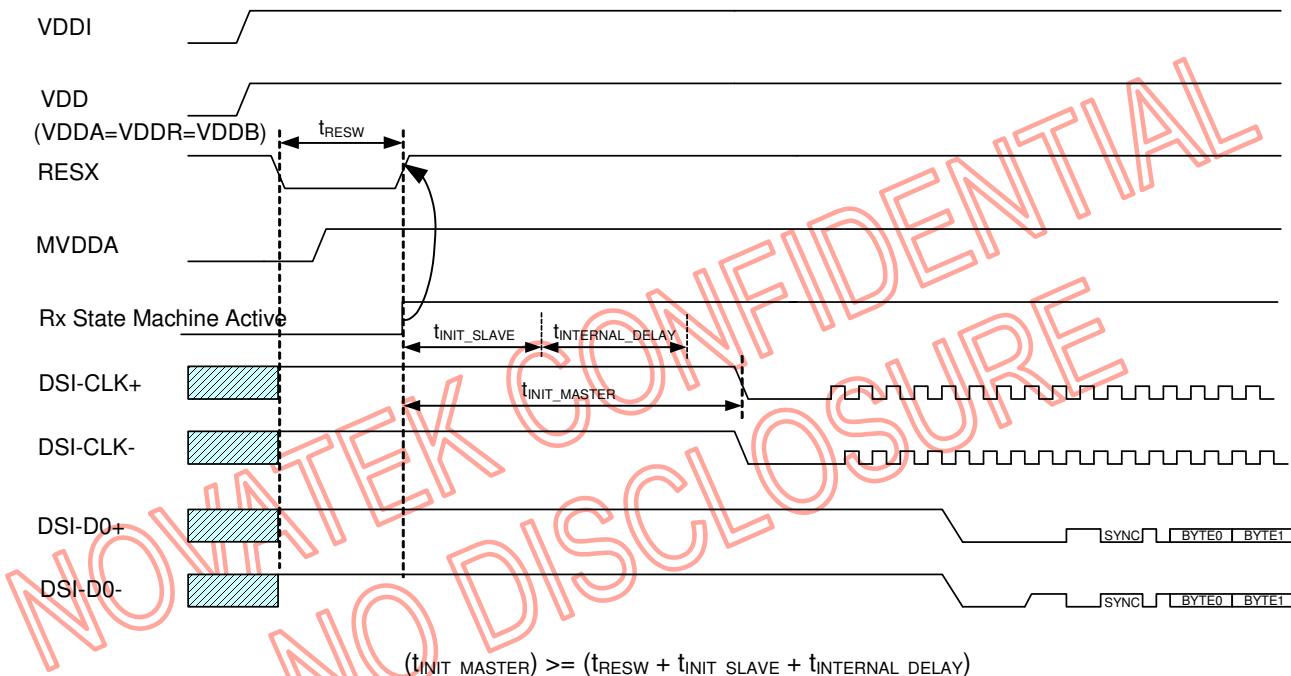
The 50MHz frequency can be changed by register PSELA[1:0].

NOVATEK CONFIDENTIAL
NO DISCLOSURE

5.2.3 System Power-Up and Initialization

After power-on, the host processor shall observe an initialization period, t_{INIT} , during which it shall drive a sustained Tx-Stop state (LP-11) on all Lanes of the Link.

Figure below illustrates an example power-up sequence for a DSI display module. In the figure, a hardware reset (RESX) mechanism is assumed for initialization. Internally within the display module, de-assertion of RESX could happen after both IO and core voltages were ramped up. In this example, the host's t_{INIT_MASTER} parameter is programmed for driving LP-11 for a period longer than the sum of t_{RESW} , t_{INIT_SLAVE} and $t_{INTERNAL_DELAY}$. The display module may ignore all Lane activities during this time.



Symbol	Parameter	Min	Typ	Max	Units
t_{INIT_MASTER}	MIPI Tx initialize time	5	-	-	mS
t_{RESW}	Reset "L" pulse width	Note	-	-	μ S
t_{INIT_SLAVE}	MIPI Rx initialize time	4	-	-	mS
$t_{INTERNAL_DELAY}$	Internal delay time.	500	-	-	μ S

Note: See "Reset Input Timing" (refer to section 7.3)

5.3 Interface Pause

It is possible when transferring a Command, Multiple Parameter Data to invoke a pause in the data transmission.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

MIPi Interface Pause

Pause can be done on DSI between Packets when they are sent to same or different receiver (Virtual Channel (VC)) e.g.

- 1) Same receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => ...
- 2) Different receiver: Packet 1 (VC=00) => Packet 2 (VC=00) => Packet 3 (VC=00) => ...

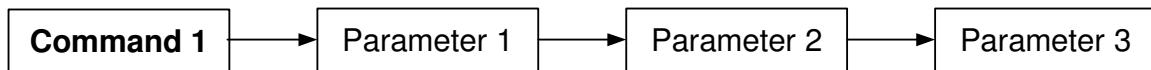
The means that “=>” symbol means a pause on DSI.

NOVATEK CONFIDENTIAL
NO DISCLOSURE

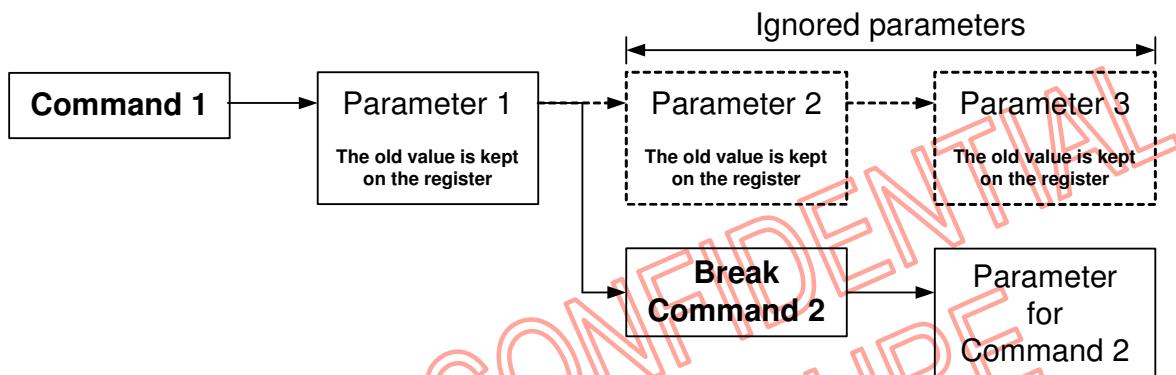
5.4 Data Transfer Break and Recovery

Display data transfer break is illustrated for reference purposes below.

Without break



With break (See and check also exceptions*)



Break can be e.g. another command or noise pulse.

Fig. 5.4.1 Break during Parameter

*) See also an exception on section “6.1 User Command Set” and Note 2.

The MCU can create a break condition when it is forcing DSI data lanes in the LP-11 mode

The NT35521 stops to control DSI data lanes (change from a transmitter mode to a received mode) if it was controlling DSI data lanes as a transmitter when the MCU is forcing DSI data lanes in the LP-11.

The break condition can be done any time when the MCU or the driver IC is controlling DSI data lanes e.g. the driver IC is sending data to the MCU.

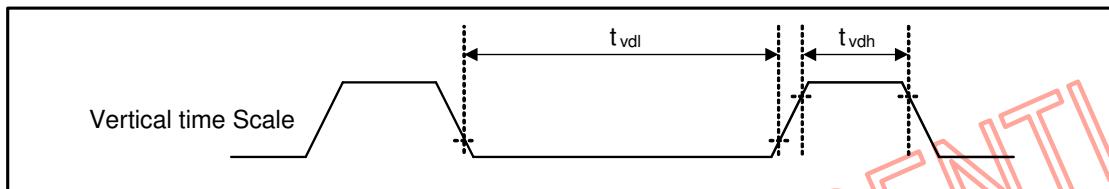
5.5 Tearing Effect Information

5.5.1 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.5.1.1 Tearing Effect Line Modes

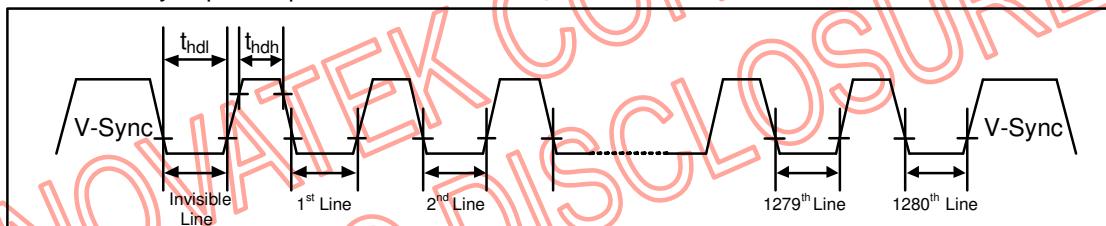
Mode 1, the Tearing Effect Output signal consists of V-Blinking Information only:



t_{vdh} = The LCD display is not updated from the Frame Memory

t_{vdl} = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

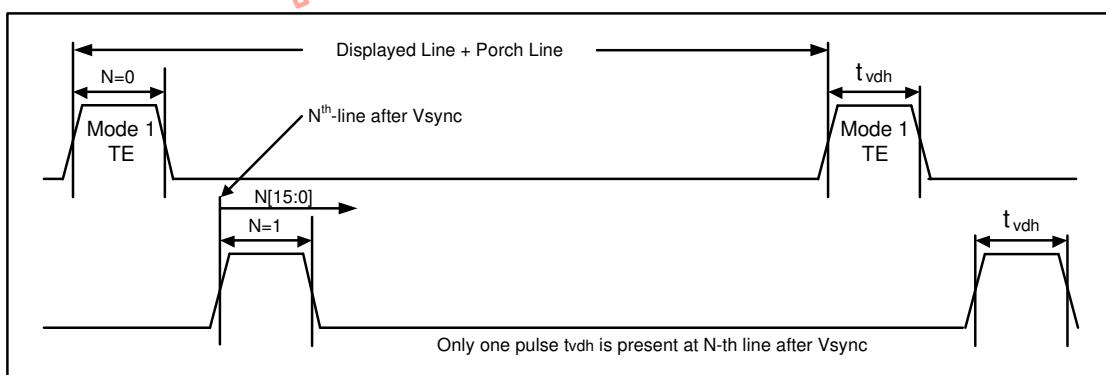
Mode 2, the Tearing Effect Output signal consists of V-Blinking and H-Blinking Information, there is one V-sync and 1280 H-sync pulses per field.



t_{dh} = The LCD display is not updated from the Frame Memory

t_{hd} = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

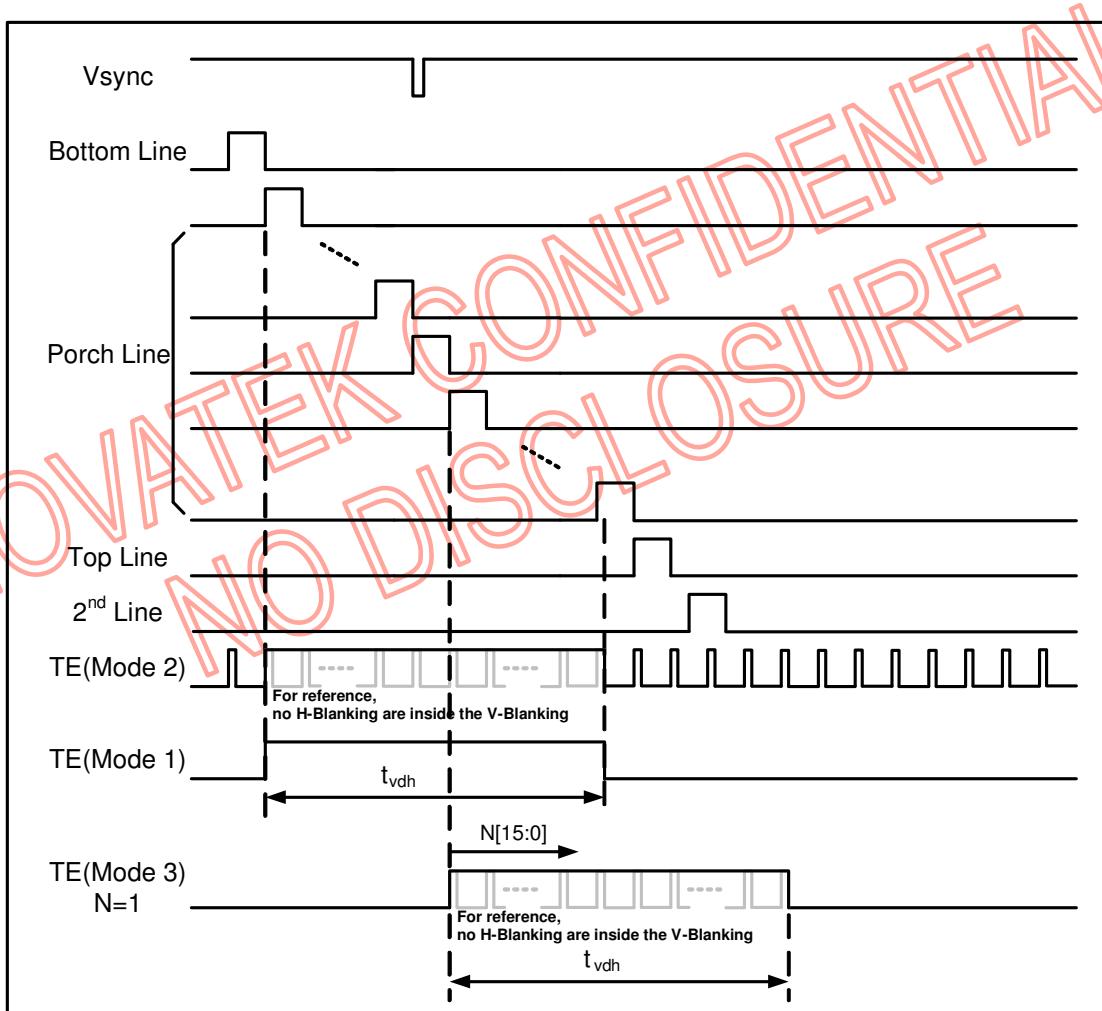
Mode 3, this mode turn on the Tearing Effect Output signal at line N after Vsync.



N = The N-th line, which set by register N[15:0] of command STESL (44h), after Vsync

The TE mode selection is described as below table

DOPCTR (B1h)	TEOFF (34h) TEON (35h)	STESL (44h)	TE Output
DSITE	M	N[15:0]	
0	X	X	TE off (output low)
1	34h	X	TE off (output low)
1	35h with M=0	N[15:0]=0	TE high in V-porch region (Mode 1)
1	35h with M=0	N[15:0]≠0	TE high at N-th line after Vsync (Mode 3)
1	35h with M=1	X	TE high in all V-porch and H-porch region (Mode 2)



Notes:

1. During Sleep In Mode, the Tearing Output Pin is active Low.
2. $N \leq$ Displayed line+Porch line. Porch line = VBPDA/B/C[7:0]+VFPDA/B/C[7:0]
 $t_{vdh} \approx$ width of porch line when $N \leq$ Displayed line.
 $t_{vdh} \approx$ width of (Displayed line+Porch line-N) when $N >$ Displayed line (falling edge of TE fixed at next Vsync).

5.6 Power On/Off Sequence

VDDI must be applied in advance of VDD (VDDA/VDDR/VDBB) or at the same time.

VDD (VDDA/VDDR/VDBB) must be powered down in advance of VDDI or at the same time.

During power off, if LCD is in the Sleep Out mode, VDD (VDDA/VDDR/VDBB) and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD (VDDA/VDDR/VDBB) can be powered down minimum 0msec after RESX has been released.

Notes:

1. There will be no damage to the display module if the power sequences are not met.
2. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
3. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.
4. If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.6.1 and 5.6.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.
5. There is not a limit for Rise/Fall time on VDDI and VDD (VDDA/VDDR/VDBB).
6. The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms after LP-11 (Clock and Data Channels), VDDI and VDD (VDDA/VDDR/VDBB) are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).

NOVATEK CONFIDENTIAL
NO DISCLOSURE

5.6.1 Power On Sequence

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10 μ sec after both VDD and VDDI have been applied.

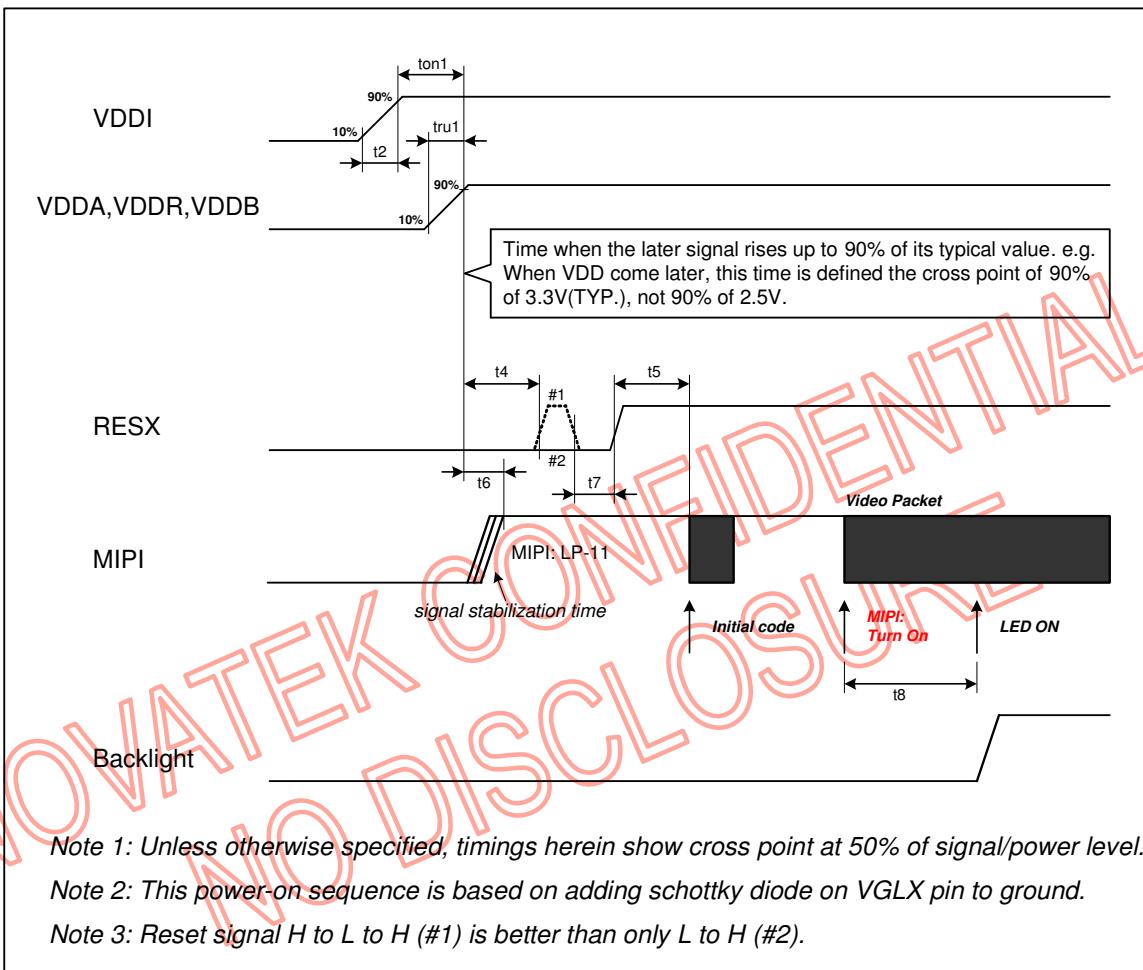
The power on sequence for different power input modes are shown below figures.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	-	No limit	-	ms	Schottky diode should add on VGLX
ton2	-	0 (Note)	-	ms	
ton3	-	No limit	-	ms	
ton4	-	No limit	-	ms	
t2	-	-	150	μ s	
tru1	-	-	150	μ s	
tru2	-	-	150	μ s	
tru3	-	-	150	μ s	
tru4	-	-	150	μ s	
t4	40	-	-	ms	
t5	120	-	-	ms	
t6	0	-	t4	ms	
t7	10	-	-	μ s	
t8	8	-	-	VS	Keep data more than 8 frames (VS)

Note: VDDA and AVDD/VDDR/VDBB should be turned on simultaneous when using 4 Input Power mode (BTM[2:0] = "101") or 5 Input Power mode (BTM[2:0] = "110"). If VDDA and AVDD/VDDR/VDBB can not be turned on simultaneous, please change to use 3 Input Power mode (BTM[2:0] = "100").

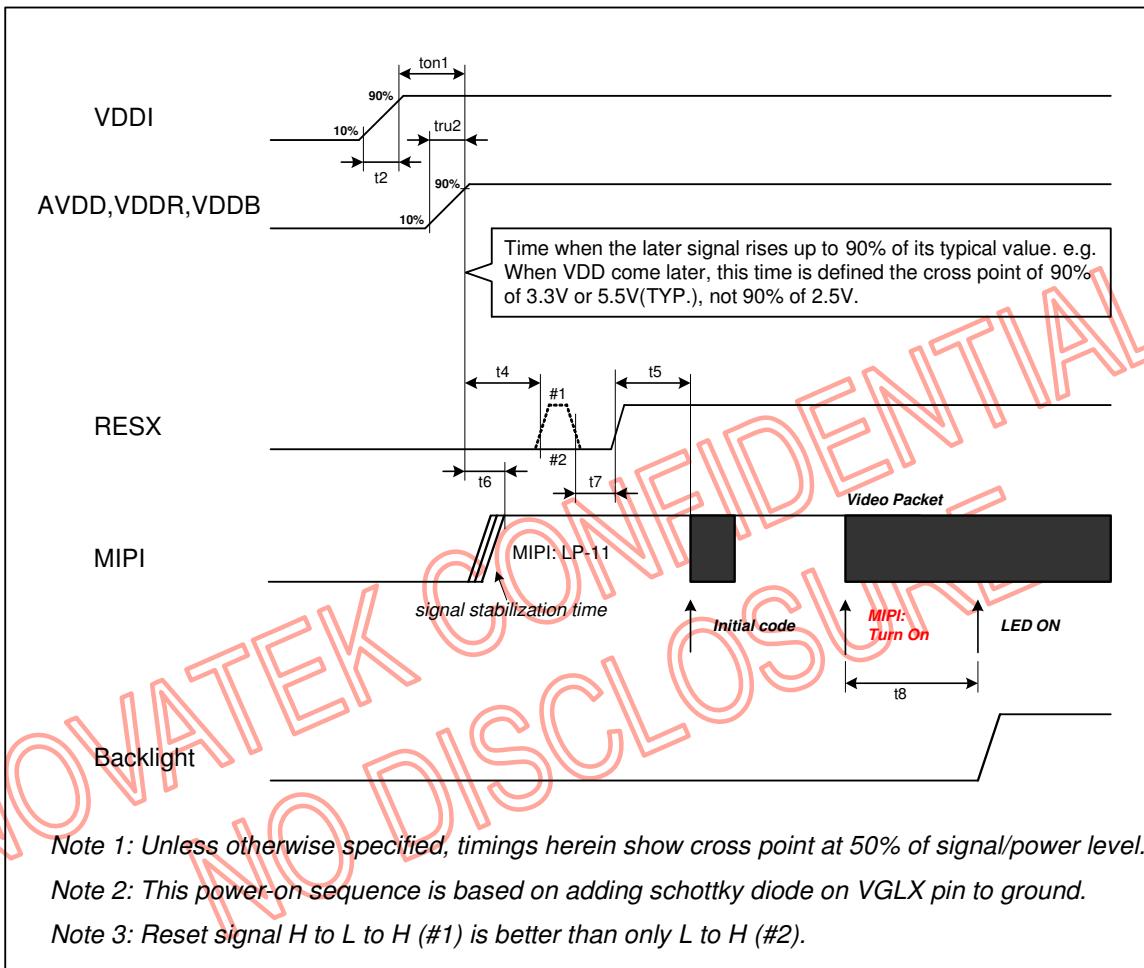
- 2 Input power (BTM[2:0] = "000" or "001"):

VDDI=1.65~3.6V, VDDA=VDDR=VDBB=2.5~3.6V



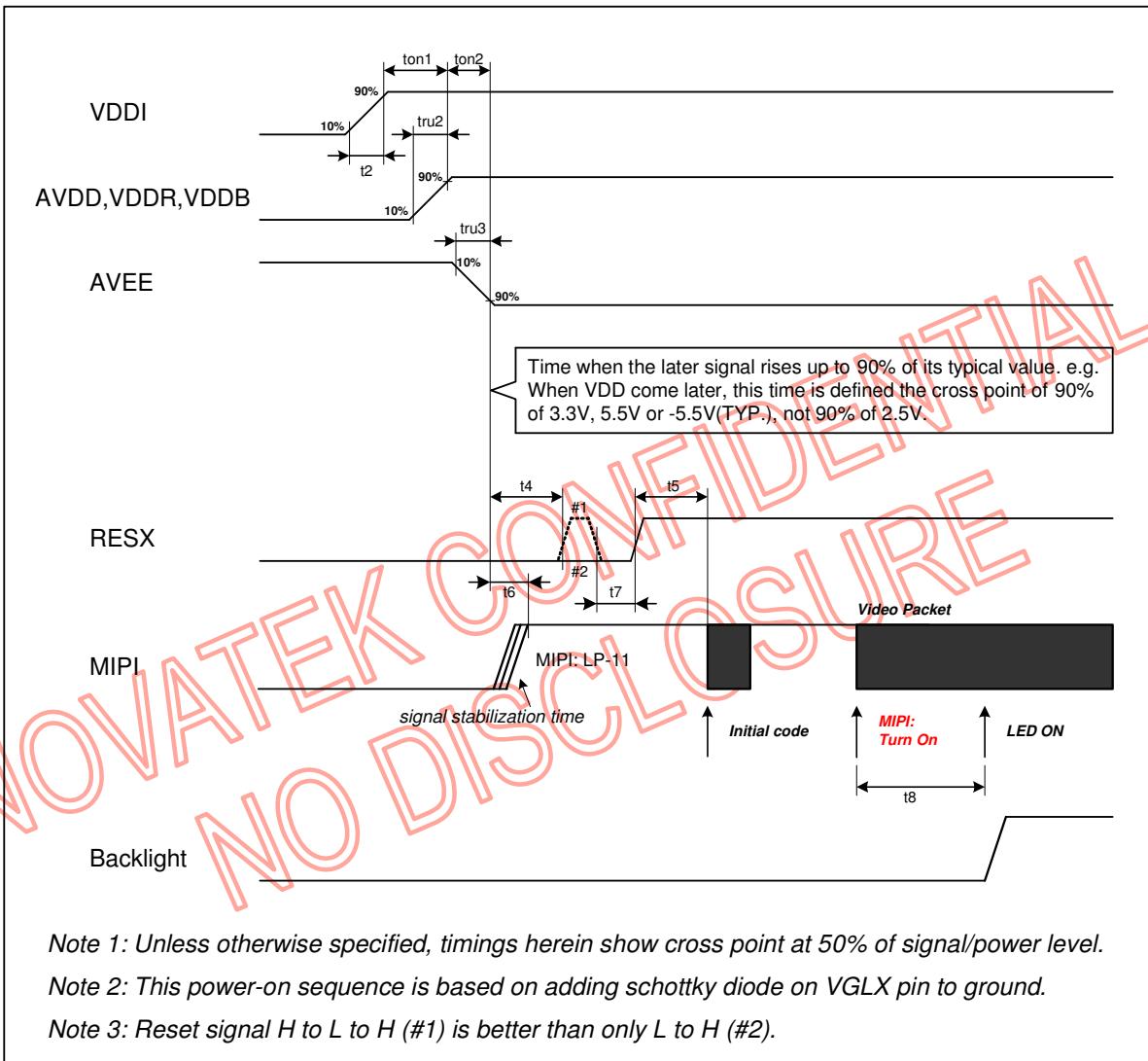
- 2 Input power (BTM[2:0] = "010" or "011"):

VDDI=1.65~3.6V, AVDD=VDDR=VDBB=4.5~6.0V



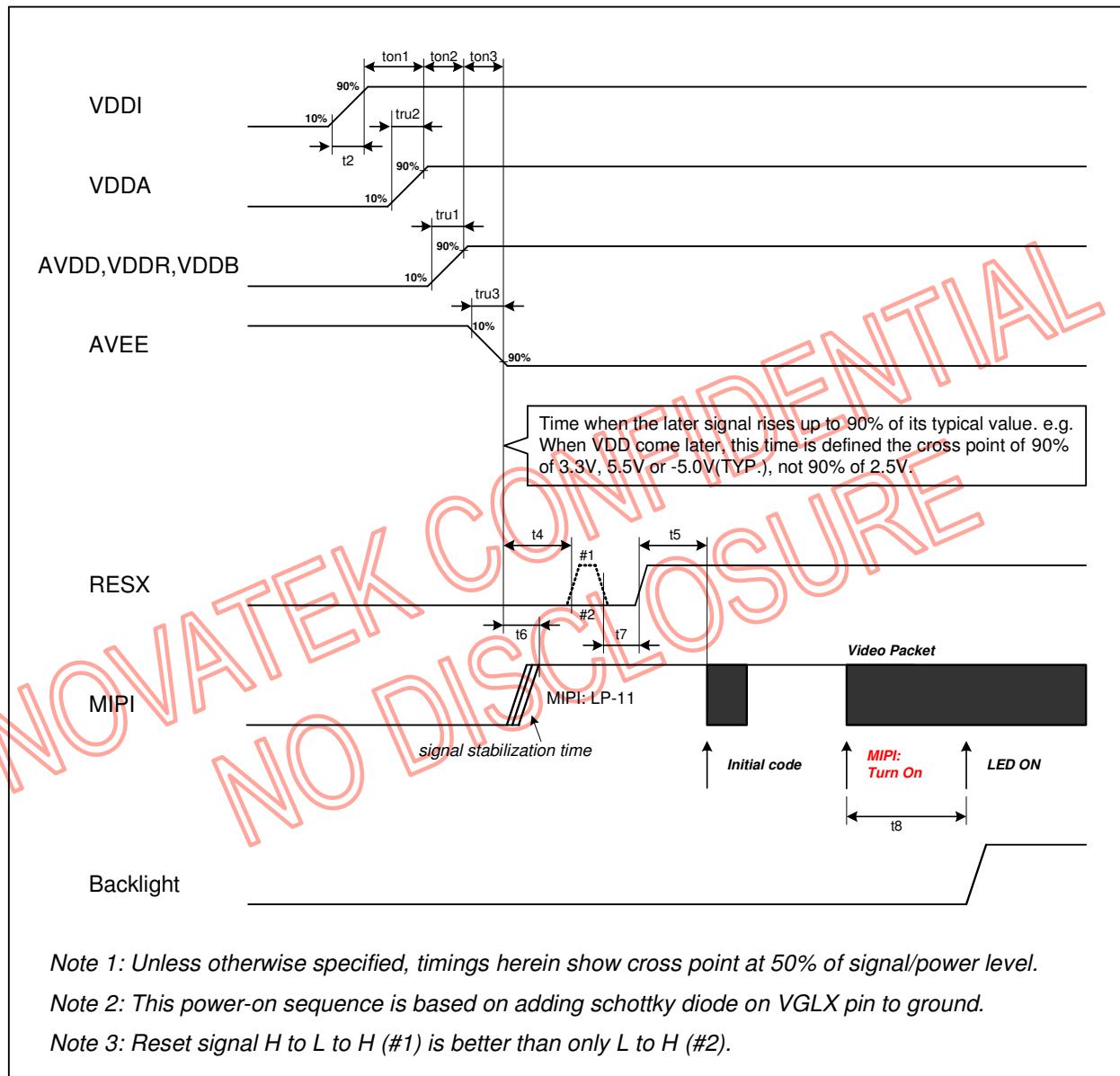
- 3 Input power (BTM[2:0] = "100"):

VDDI=1.65~3.6V, AVDD=VDDR=VDBB=4.5~6.0V, AVEE=-4.5~-6.0V



- 4 Input power (BTM[2:0] = "101"):

VDDI=1.65~3.6V, VDDA=2.5~3.6V, AVDD=VDDR=VDBB=4.5~6.0V, AVEE=-4.5~6.0V



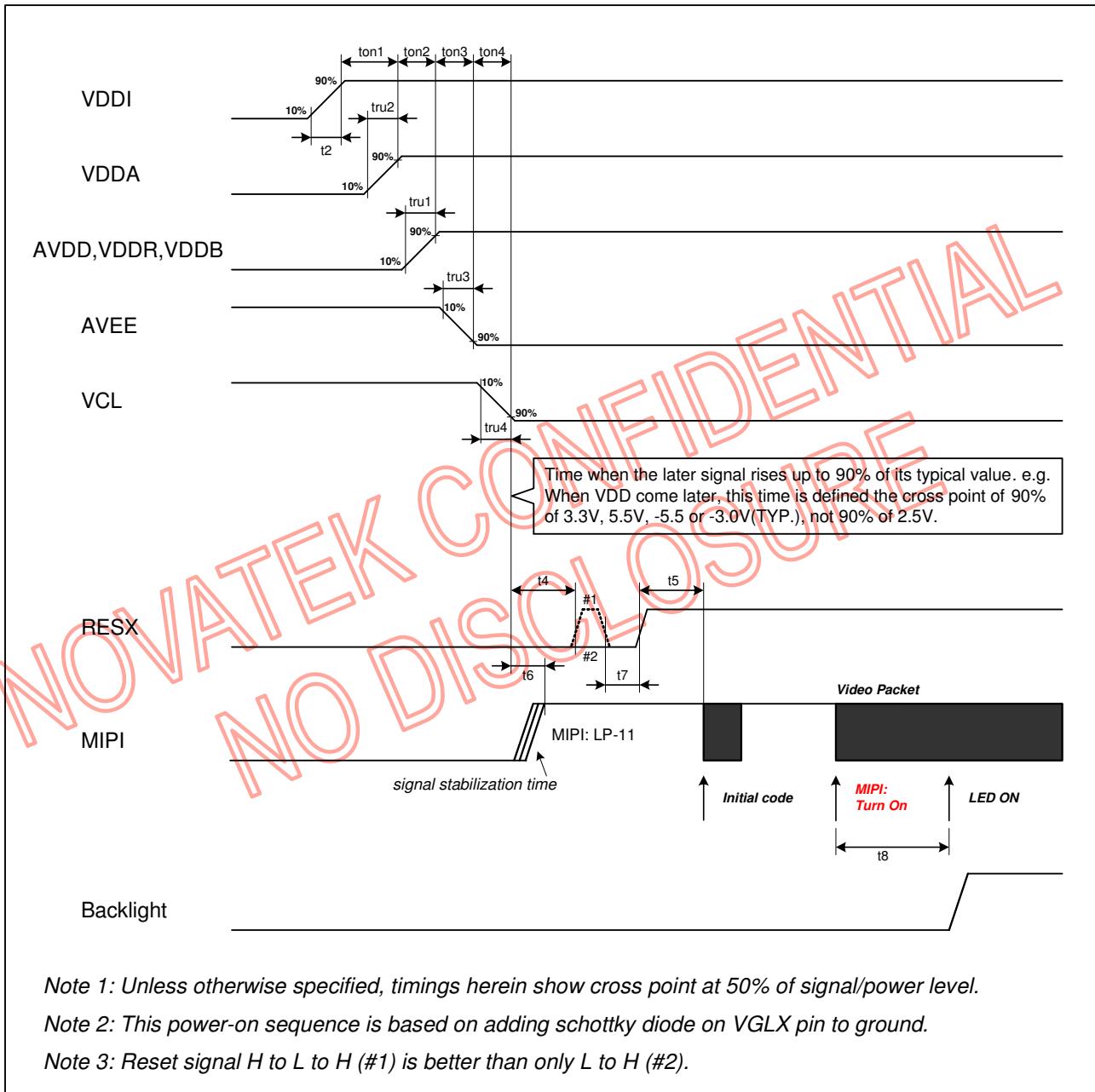
Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground.

Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

- 5 Input power (BTM[2:0] = "110"):

VDDI=1.65~3.6V, VDDA=2.5~3.6V, AVDD=VDDR=VDBB=4.5~6.0V, AVEE=-4.5~6.0V, VCL=-2.5~4.0V



5.6.2 Power Off Sequence

The power off sequence for different power input modes are shown below figures.

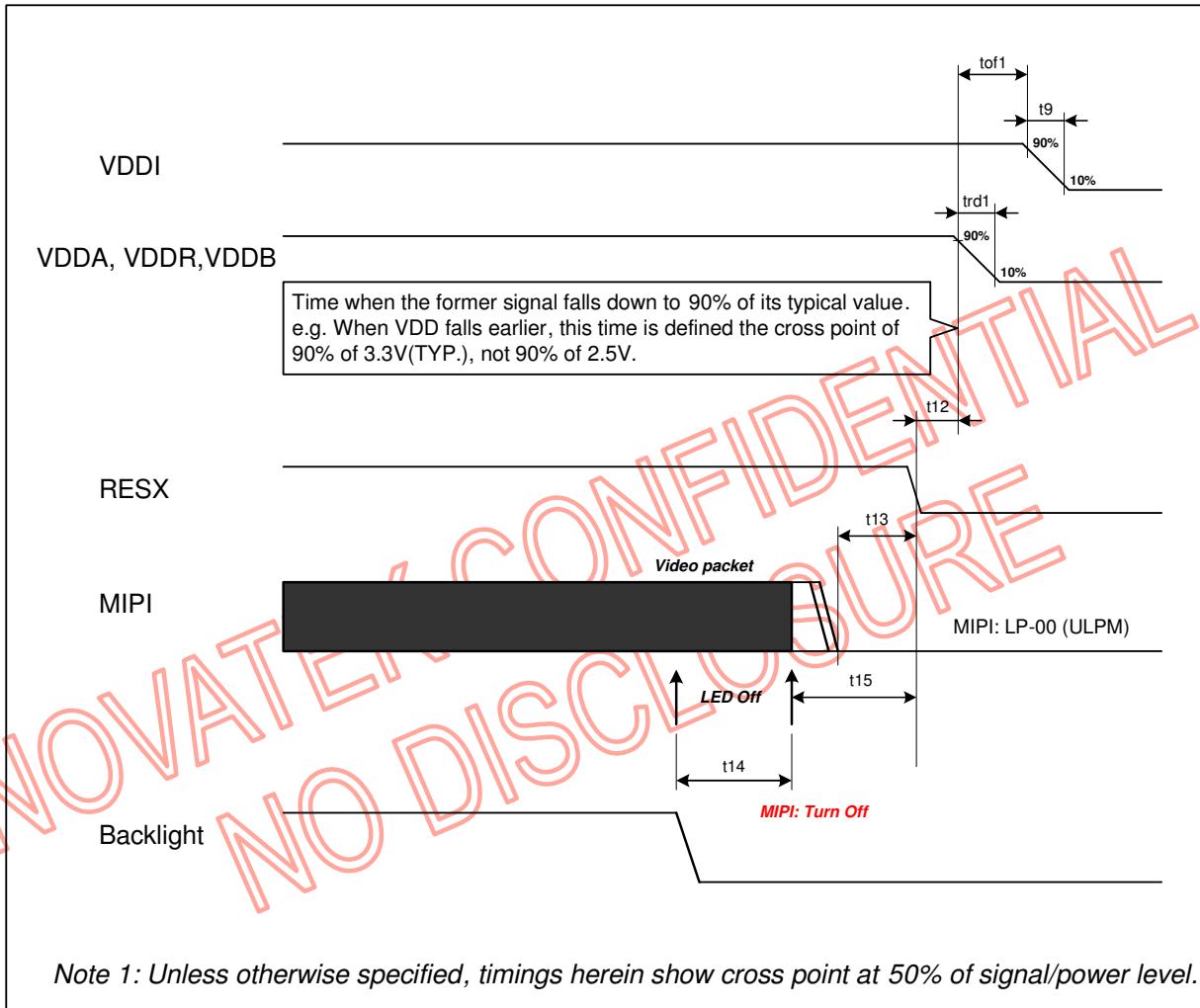
Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150	-	-	μs	
tof1	-	No limit	-	ms	
tof2	-	0 (Note)	-	ms	
tof3	-	No limit	-	ms	
tof4	-	No limit	-	ms	
trd1	150	-	-	μs	
trd2	150	-	-	μs	
trd3	150	-	-	μs	
trd4	150	-	-	μs	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	100			ms	

Note: VDDA and AVDD/VDDR/VDBB should be turned off simultaneous when using 4 Input Power mode (BTM[2:0] = "101") or 5 Input Power mode (BTM[2:0] = "110"). If VDDA and AVDD/VDDR/VDBB can not be turned off simultaneous, please change to use 3 Input Power mode (BTM[2:0] = "100").

**NOVATEK CONFIDENTIAL
NO DISCLOSURE**

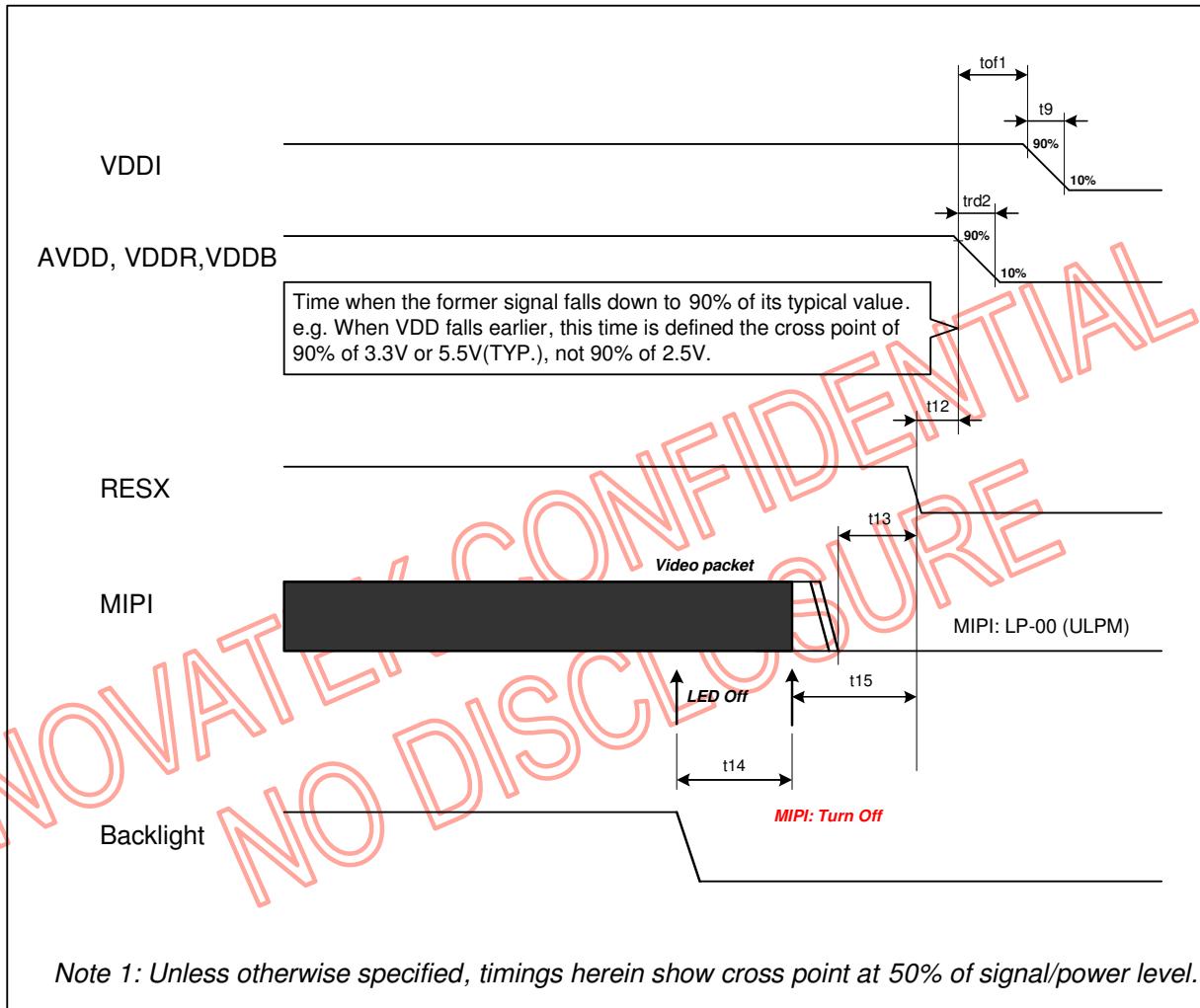
- 2 Input power (BTM[2:0] = "000" or "001"):

VDDI=1.65~3.6V, VDDA=VDDR=VDBB=2.5~3.6V



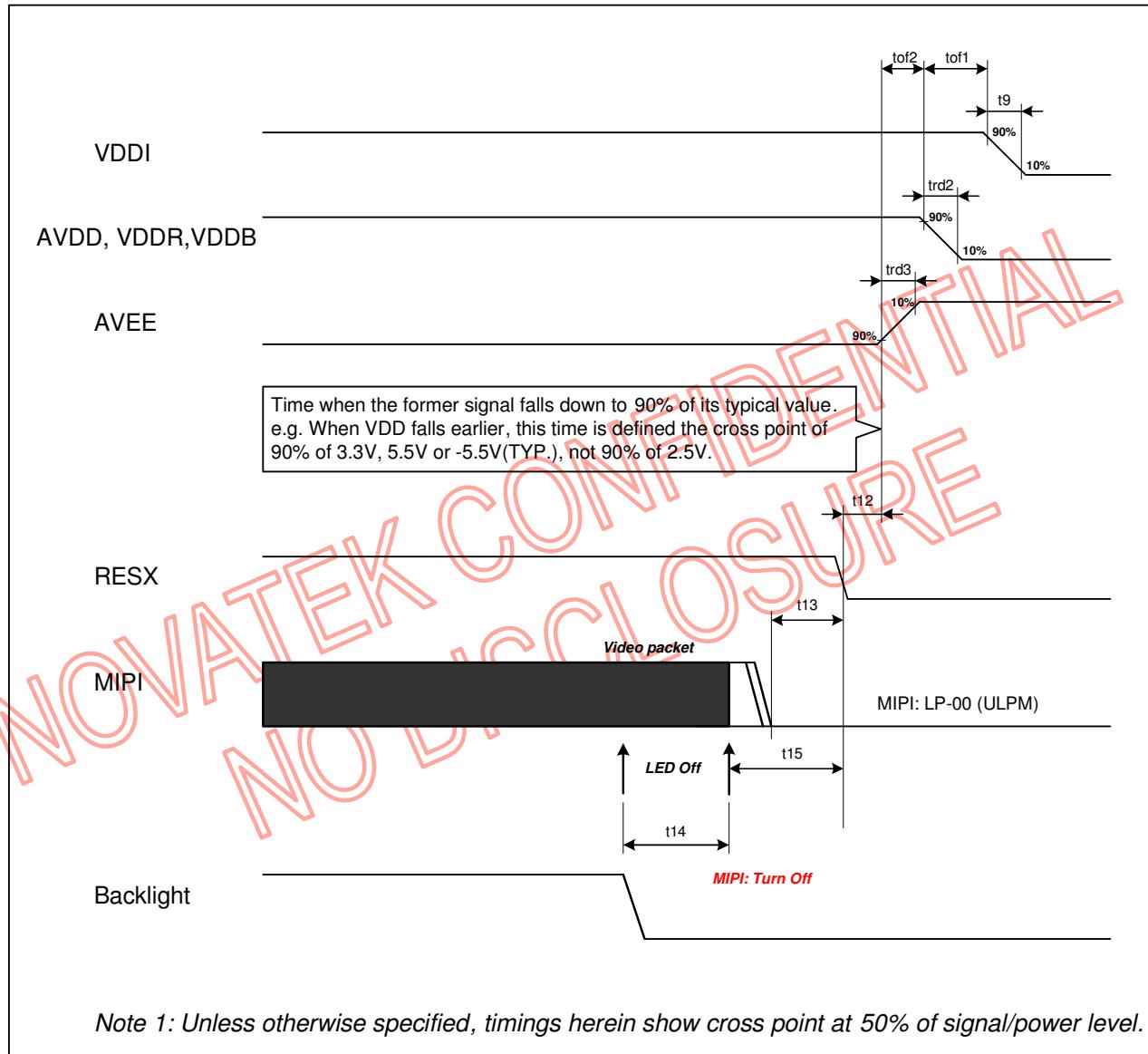
- 2 Input power (BTM[2:0] = "010" or "011"):

VDDI=1.65~3.6V, AVDD=VDDR=VDBB=4.5~6.0V



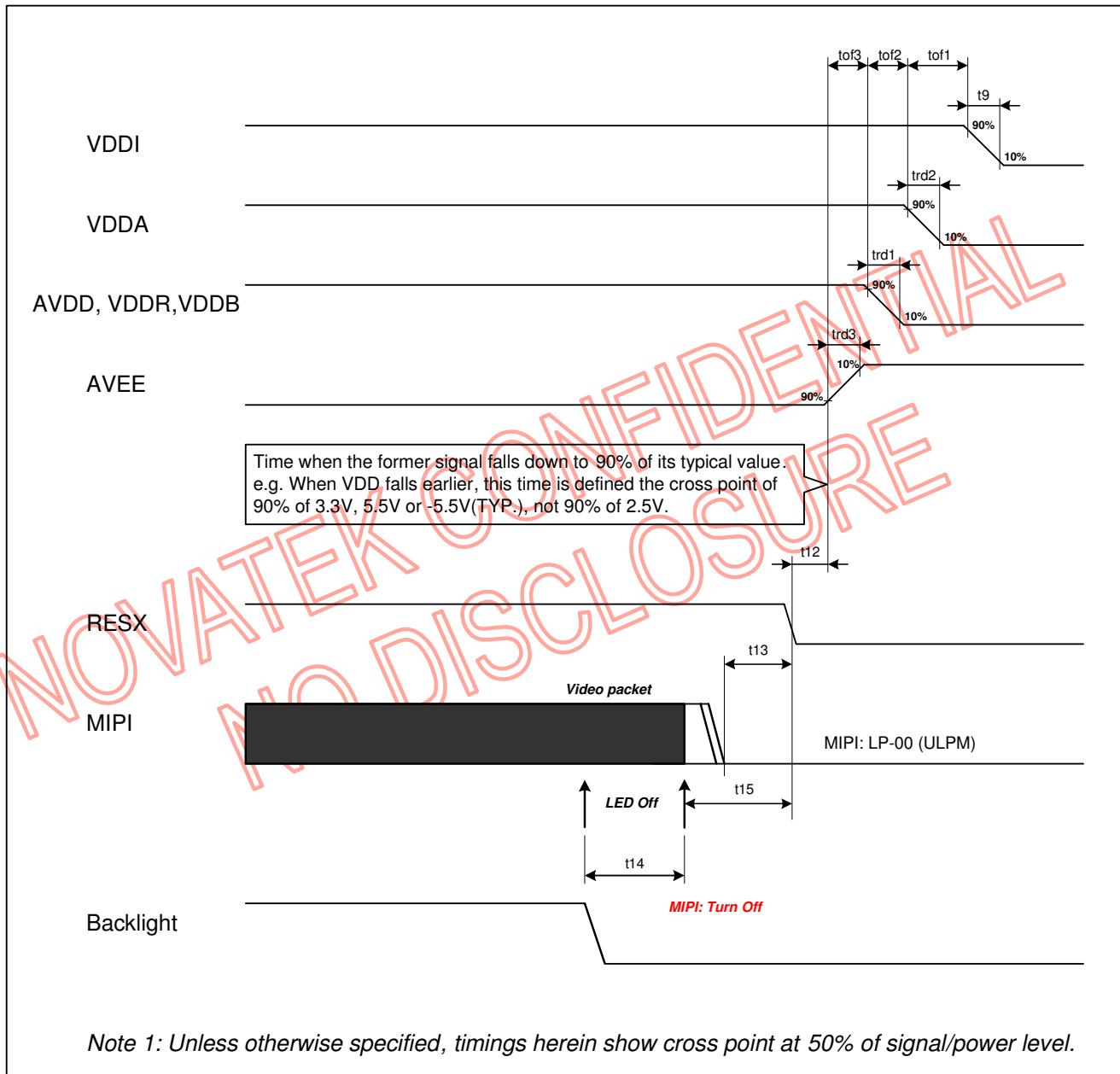
- 3 Input power (BTM[2:0] = "100"):

VDDI=1.65~3.6V, AVDD=VDDR=VDBB=4.5~6.0V, AVEE=-4.5~6.0V

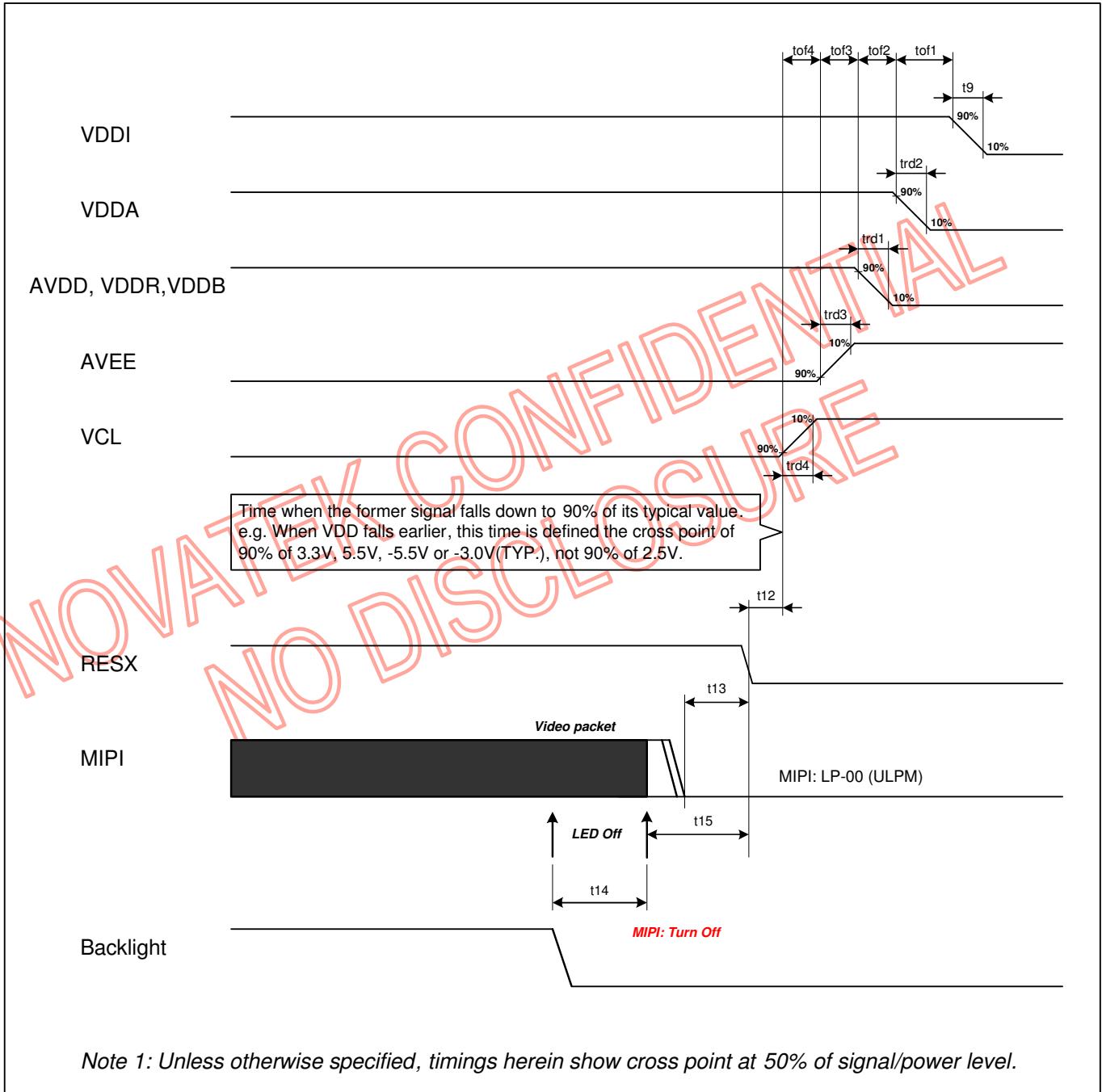


- 4 Input power (BTM[2:0] = "101"):

VDDI=1.65~3.6V, VDDA=2.5~3.6V, AVDD=VDDR=VDBB=4.5~6.0V, AVEE=-4.5~6.0V



- 5 Input power (BTM[2:0] = "110"):
 VDDI=1.65~3.6V, VDDA=2.5~3.6V, AVDD=VDDR=VDBB=4.5~6.0V, AVEE=-4.5~6.0V, VCL=-2.5~4.0V



5.6.3 Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

NOVATEK CONFIDENTIAL
NO DISCLOSURE

5.7 Power Level Modes

5.7.1 Definition

5 level modes are defined they are in order of maximum power consumption to minimum power consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 16.7M colors.

2. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display is used but with 8 colors.

3. Sleep In Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MPU interface and registers are working with VDDI power supply. Contents of the frame memory can be safe or random.

4. Deep Standby Mode.

In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. The MPU interface and registers are not working. Contents of the frame memory are random.

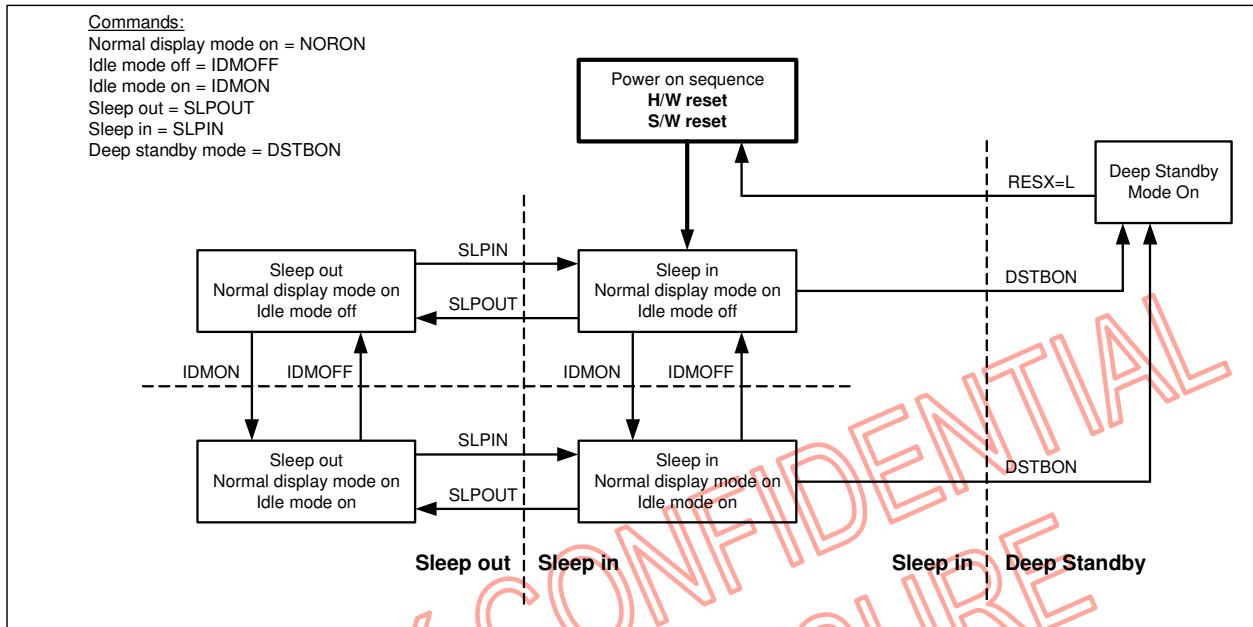
5. Power Off Mode

In this mode, VDDI and VDDA/VDDR/VDDB are removed.

Note: Transition between mode 1~3 is controllable by MPU commands. Mode 4 is entered for power saving with both power supplies for I/O and analog circuits and can be exited by hardware reset only (RESX=L). Mode 5 is entered only when both power supplies for I/O and analog circuits are removed.

NOVATEK CONFIDENTIAL
NO DISCLOSURE

5.7.2 Power Level Mode Flow Chart



Notes:

- 1) There is not any abnormal visual effect when there is changing from one power mode to another power mode.
- 2) There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode

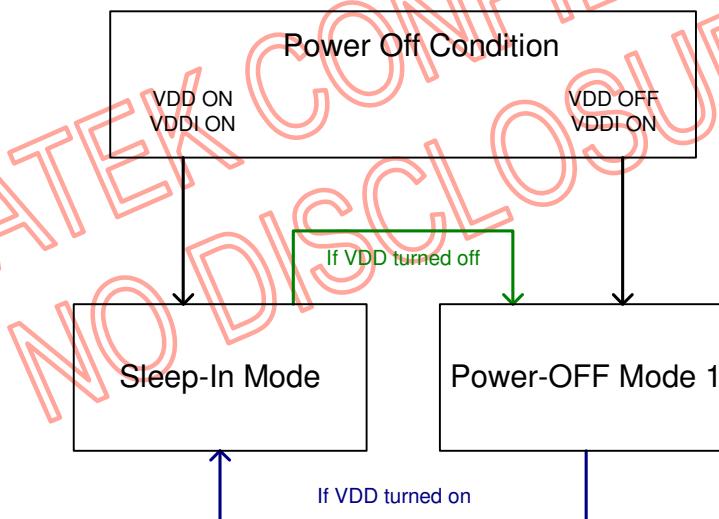
The following table represents the SRAM and Registers its mode state.

Mode	Register	Control	
		Enter	Exit
Sleep in mode	Keep	Command	
Deep-standby mode	Loss	Command	Reset pin
Reset=L	Keep (Default Value)	Reset (H/W)	

The condition for irregular power off mode is shown below.

Power Off Mode	VDD	VDDI	RESX	I/O
Mode 1	OFF	ON	High or Low	Low

Note: VDD means VDDA, VDDR and VDBB.



5.8 Reset function

5.8.1 Register Default Value

Table 5.8.1 Default Values for User Command Set

Item	After Power On	After Hardware Reset	After Software Reset
RDNUMED (05h)	00h	00h	No Changed
RDDPM (0Ah)	08h	08h	08h
RDDMADCTR (0Bh)	00h	00h	00h
RDDCOLMOD (0Ch)	70h	70h	70h
RDDIM (0Dh)	00h	00h	00h
RDDSM (0Eh)	00h	00h	00h (Bit D0 No Changed)
RDDSDR (0Fh)	00h	00h	00h
Sleep In/Out (10h/11h)	In	In	In
Normal/All Pixel Off/On (13h/22h/23h)	Normal	Normal	Normal
Display Inversion On/Off (21h/20h)	Off	Off	Off
All Pixel On/Off (23h/22h)	Off	Off	Off
Gamma setting (26h)	01h (GC0)	01h (GC0)	01h (GC0)
Display On/Off (29h/28h)	Off	Off	Off
Tearing: On/Off (35h/34h)	Off	Off	Off
Idle Mode On/Off (38h/39h)	Off	Off	Off
Interface Pixel Color Format (3Ah)	70h	70h	70h
Set Tearing Effect Scan Line (44h)	0000h	0000h	0000h
Get Scan Line (45h)	N/A	N/A	N/A
DSTB mode (4Fh)	00h	00h	00h
Display Brightness (51h, 52h)	00h	00h	00h
CTRL Display (53h, 54h)	00h	00h	00h
CABC Control (55h, 56h)	00h	00h	00h
Minimum Brightness (5Eh, 5Fh)	00h	00h	00h
DDB Start/Continue (A1h, A8h)	After MTP	MTP Value	MTP Value
	Before MTP	All 00h	All 00h
ID1 (04h, DAh) ID2 (04h, DBh) ID3 (04h, DCh)	After MTP	MTP Value	MTP Value
	Before MTP	ID1 = "00h" ID2 = "80h" ID3 = "00h"	ID1 = "00h" ID2 = "80h" ID3 = "00h"

5.8.2 Output or I/O Pins

Output pins	After Power On	After Hardware Reset	After Software Reset
HSSI_DATA0_P, HSSI_DATA0_N	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
TE, TE1	VSSI	VSSI	VSSI
LEDPWM	VSSI	VSSI	VSSI
Source Driver Output	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Note: There will be no output from TE, LEDPWM, HISS_CLK_P/N and HSSI_DATAn_P/N during Power On/Off sequences, H/W Reset and S/W Reset.

5.8.3 Input Pins

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See Section 5.6	Input Valid	Input Valid	Input Valid	See Section 5.6
HSSI_CLK_P, HSSI_CLK_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_DATA0_P, HSSI_DATA0_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_DATA1_P, HSSI_DATA1_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_DATA2_P, HSSI_DATA2_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid
HSSI_DATA3_P, HSSI_DATA3_N	Input Invalid	Input Valid	Input Valid	Input Valid	Input Invalid

Note: "Input Valid" means LP-Rx without instructions of the MCU.

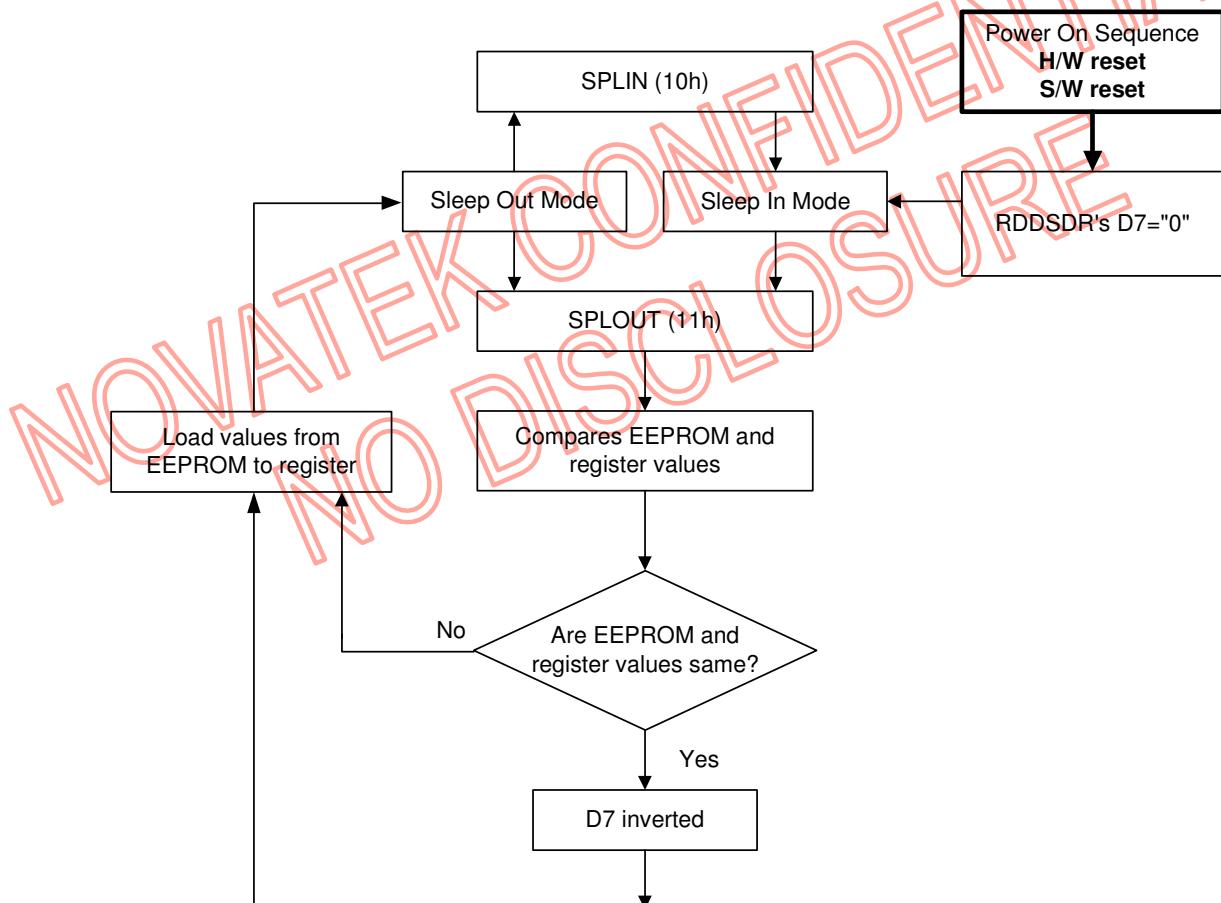
5.9 Sleep Out-Command and Self-Diagnostic Functions of the Display Module

5.9.1 Register loading Detection

Sleep Out-command (See "Sleep Out (11h)") is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller is working properly.

There are compared factory values of the EEPROM and register values of the display controller by the display controller (1st step: Compares register and EEPROM values, 2nd step: Loads EEPROM value to register). If those both values (EEPROM and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command "Read Display Self-Diagnostic Result (0Fh)" (=RDDSDR) (The used bit of these commands is D7). If those both values are not same, this bit (D7) is not inverted (= not increased by 1) and the used TE-line is set to low (Registers, what are set by "Tearing Effect Line On (35h)" command, are keeping their current values) when it can be reactivated by "Tearing Effect Line On (35h)" command.

The flow chart for this internal function is following:



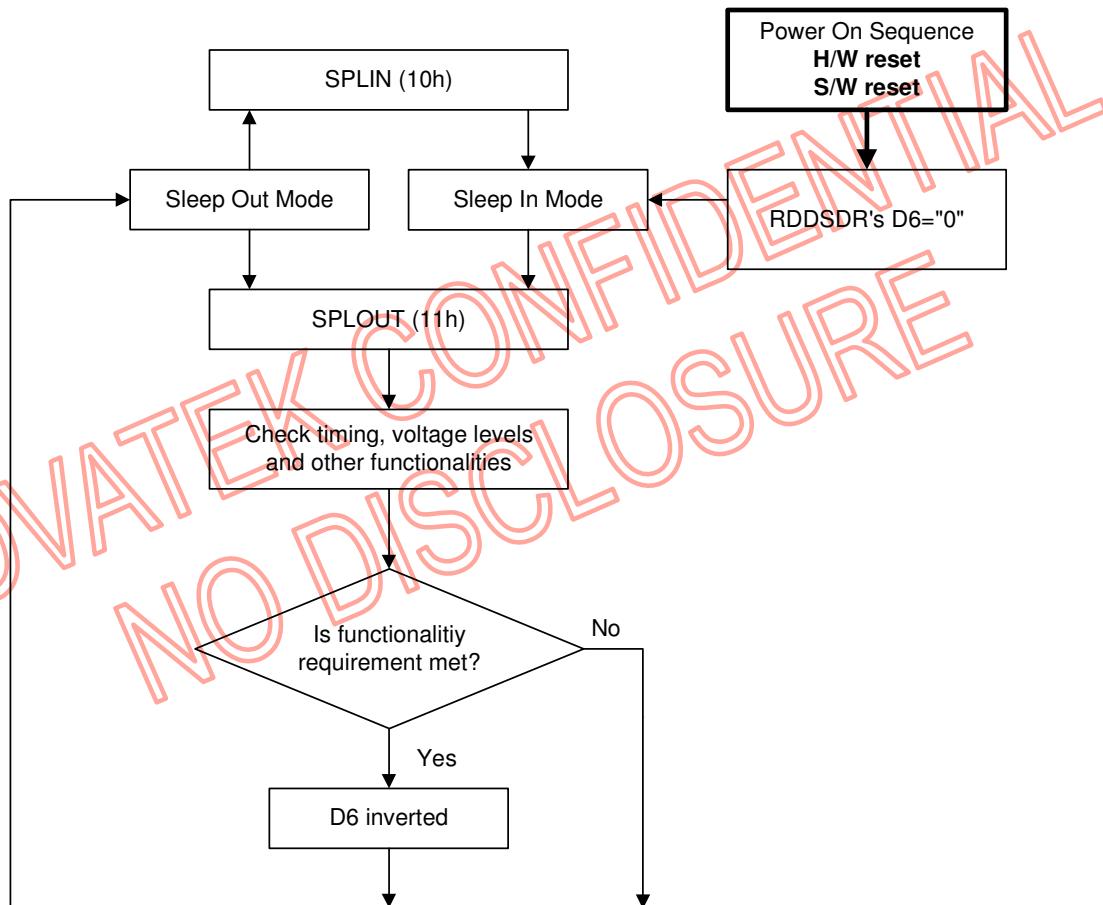
Note: There is not compared and loaded register values, which can be changed by user (00h to AFh and DAh to DCCh), by the display module.

5.9.2 Functionality Detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, there is inverted (= increased by 1) a bit, which defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of these commands is D6). If functionality requirement is not same, this bit (D6) is not inverted (= not increased by 1).

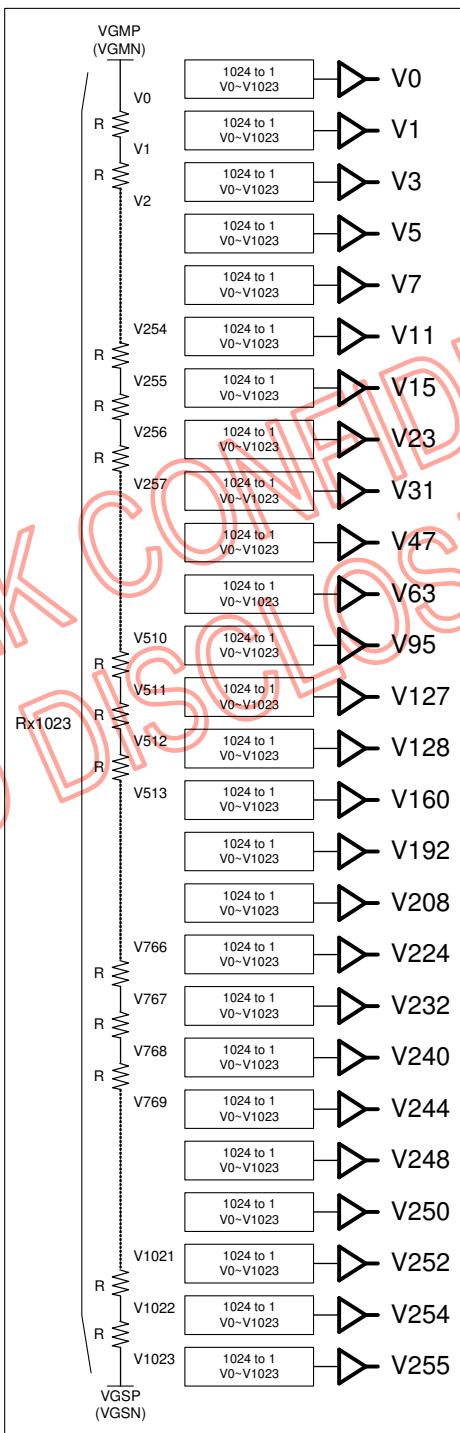
The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In -mode to Sleep Out -mode, before there is possible to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out -command is sent in Sleep Out -mode.

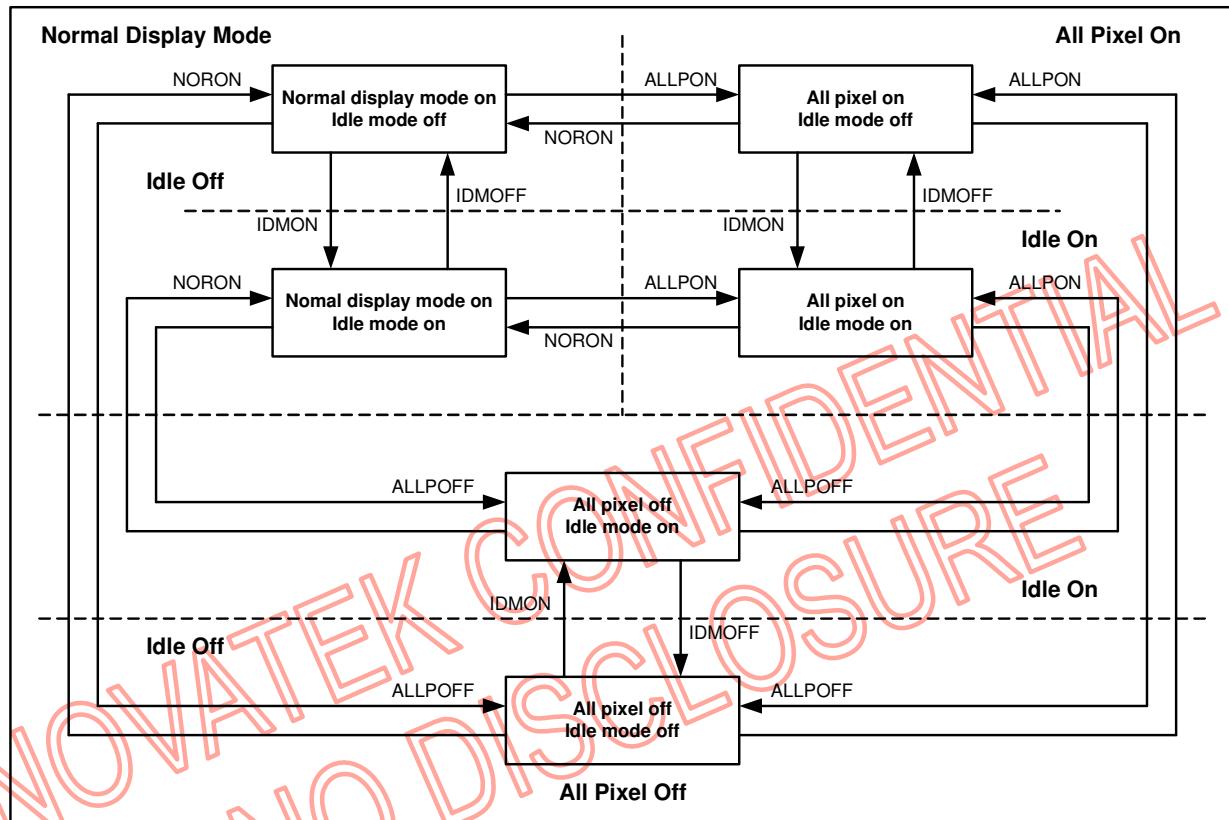
5.10 Gamma Function

The structure of grayscale amplifier is shown as below. The 26 voltage levels between VGMP and VGSP are determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment register and the micro-adjustment register.



5.11 Basic Display Mode

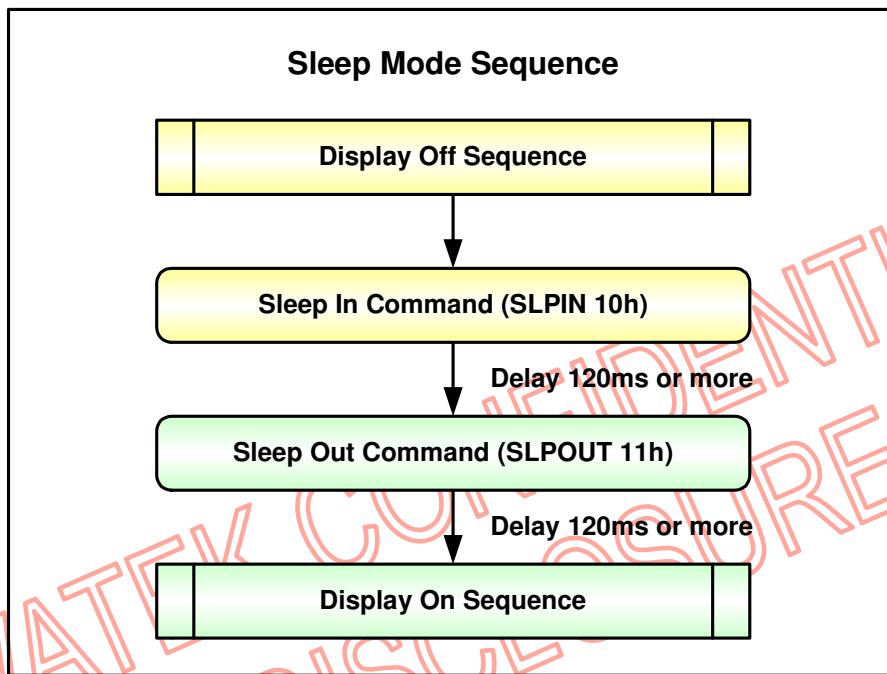
The NT35521 has some basic operation modes which are Normal Display Mode, Idle Mode, All Pixel On and All pixel Off for panel display. User can change these display modes for each other is illustrated below.



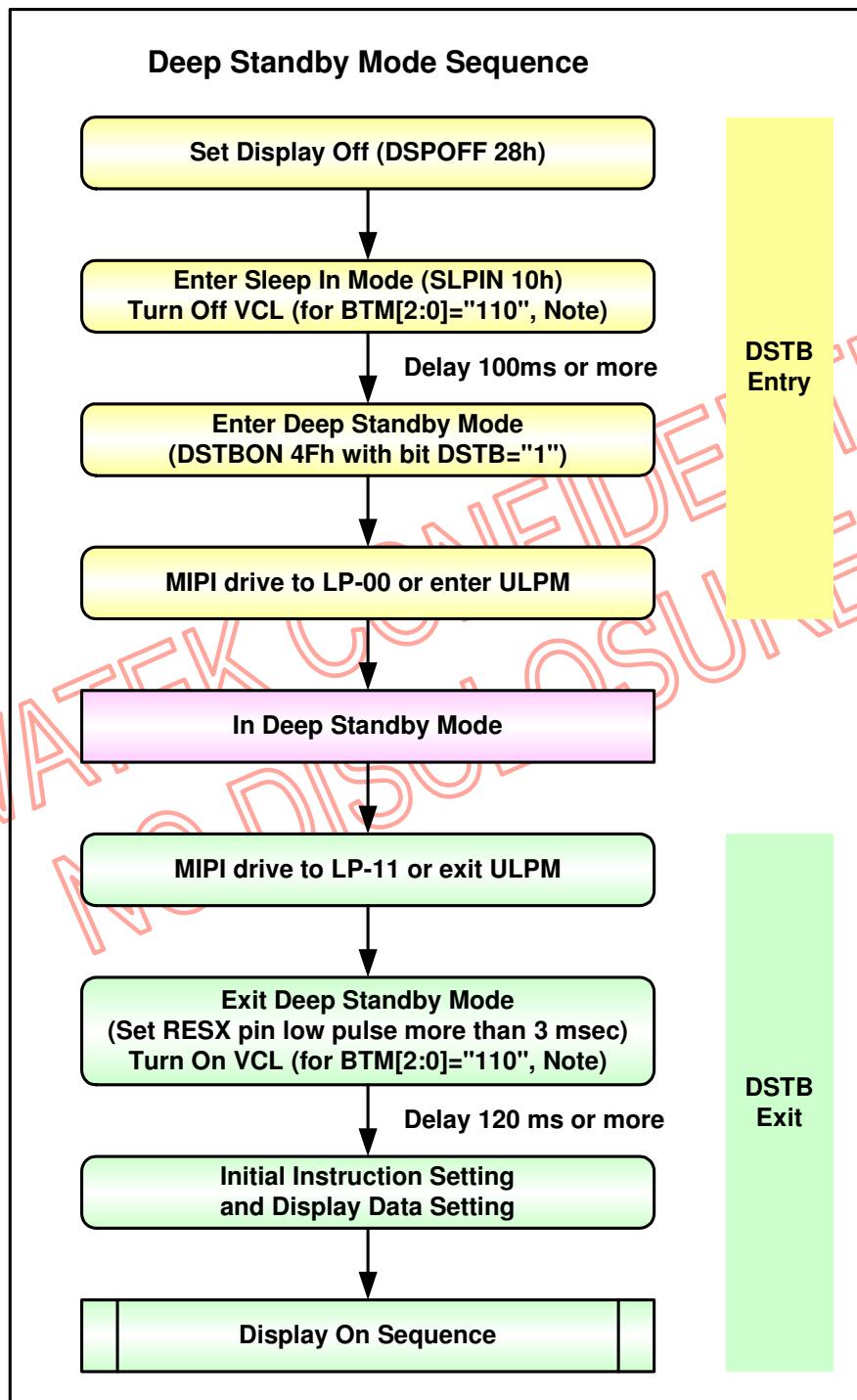
5.12 Instruction Setting Sequence

When setting instruction to the NT35521, the sequences shown in below figures must be followed to complete the instruction setting.

5.12.1 Sleep In/Out Sequence



5.12.2 Deep Standby Mode Enter/Exit Sequence



Note: The VCL should be turned off during DSTB to avoid the leakage current when using 5 power mode (BTM[2:0] = "110", VCL is external input power). User can skip the VCL off/on steps if using NT50198 power IC with NT35521 in 5 power mode because the VCL from NT50198 will be turned off by driver IC NT35521 after enter sleep-in.

5.13 Instruction Setup Flow

5.13.1 Initializing with the Built-in Power Supply Circuits

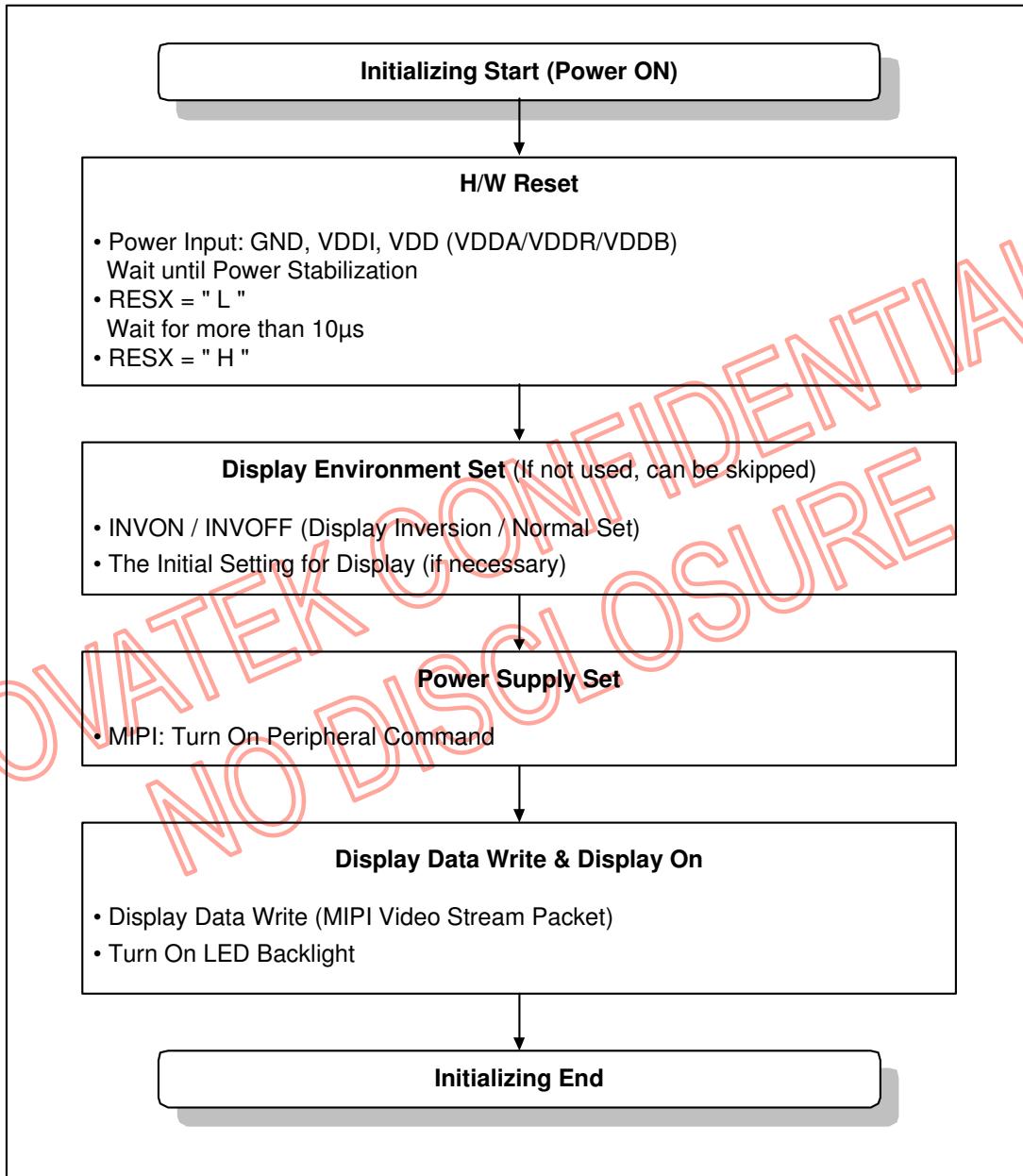


Fig. 5.13.1 Initializing with the built-in power supply circuit

Note: This figure is shown about initialization flow. Please see Section 5.6.1 for the detail of Power On Sequence.

5.13.2 Power OFF Sequence

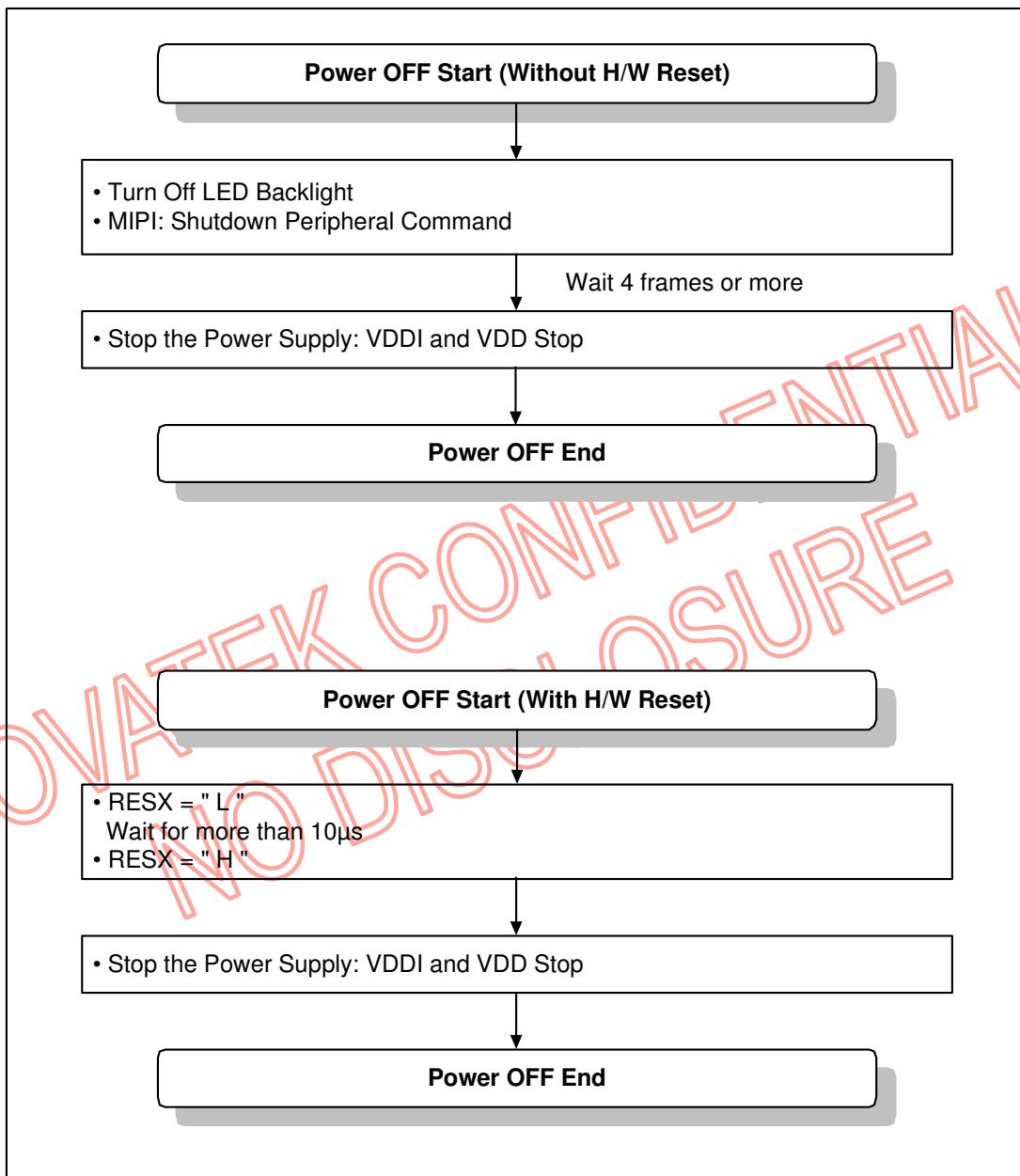
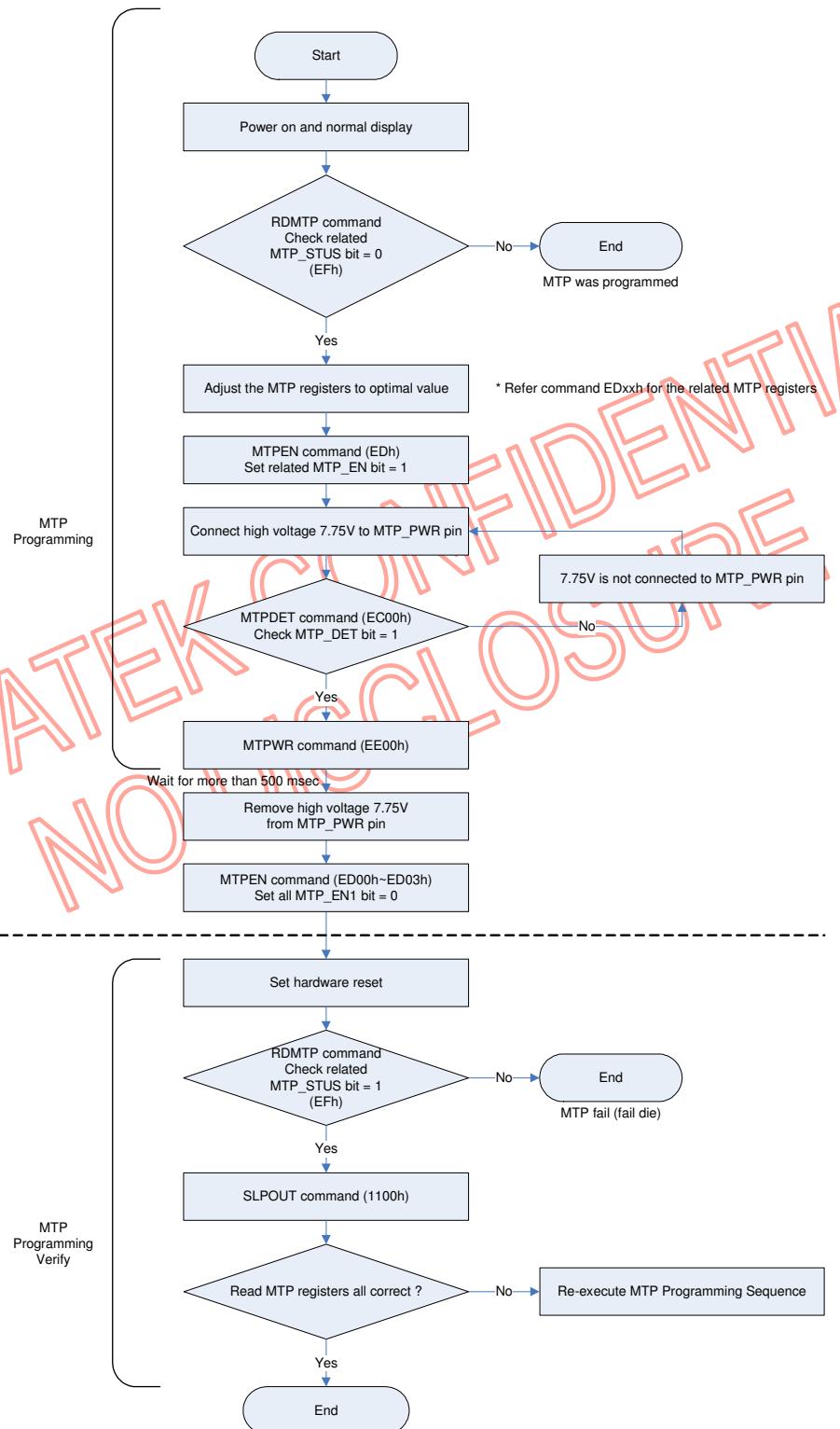


Fig. 5.13.2 Power off sequence

Note: This figure is shown about power off flow. Please see Section 5.6.2 for the detail of Power Off Sequence.

5.14 MTP Write Sequence



5.15 Column, 1-Dot, 2-Dot, 3-Dot, 4-Dot and Z Inversion (VCOM DC Drive)

The NT35521, in addition to the frame-inversion liquid crystal drive, supports the column, 1-dot, 2-dot, 3-dot, 4-dot and Z inversion driving methods to invert the polarity of liquid crystal. The column, 1-dot, 2-dot, 3-dot, 4-dot and Z inversion can provide a solution for improving display quality.

In determining the inversion drive for the inversion cycle, check the quality of display on the liquid crystal panel. Note that setting 1-dot inversion will raise the frequency of the liquid crystal polarity inversion and increase the charging/discharging current on liquid crystal cells.

NOVATEK CONFIDENTIAL
NO DISCLOSURE

5.16 Dynamic Backlight Control Function

The NT35521 embedded Content Adaptive Brightness Control (CABC) function. This function is used to generate a proper PWM signal based on internal CABC algorithm. User could apply this PWM signal to control other device(s) (Such as power IC or LED driver IC). When the CABC function is enabled and cooperate with external circuits (such as LED driver circuit), the power consumption of backlight will be reduced with keeping acceptable display quality.

The CABC function of NT35521 is used to reduce the power consumption of display backlight. Contents adaptation means that the average gray level scale of image contents is increased while simultaneously lowering brightness of the backlight to achieve same perceived brightness. The adjusted gray level scale and thus power consumption reduction depends on the contents of the image. The display image and brightness are dynamically processed by CABC block. The availability of this function ranges from moving picture such as TV image to still picture such as menu. However, in order to gain a better display quality and reduce the power consumption of the backlight, the NT35521 internally uses NOVATEK dynamic gamma algorithm to produce an optimal backlight control based on different image contents.

It is also available to control the brightness by adjusting PWM duty manually in NT35521. So combined the CABC with manual setting processed results, the display output brightness is:

$$\text{Display Backlight Brightness} = \text{Manual Setting Ratio} \times \text{CABC Brightness Ratio}$$

Table 5.16.1 Display Brightness Output When CABC Function are Enable

Example	A	B	A x B	Brightness Output of LEDPWM	Image Status
	Brightness Ratio (Manual)	Brightness Ratio (CABC)	Calculation Result		
Example 1	70%	50%	35%	35%	CABC Modified
Example 2	80%	100%	80%	80%	CABC Modified
Example 3	50%	30%	15%	15%	CABC Modified

One of ABC applications is simply illustrated in the **Fig. 5.16.1**. This application is used to dynamic control the backlight power consumption. The LEDPWM is an output-type pin which can output a PWM signal to control the display backlight brightness. The PWM duty cycle of “LEDPWM” is determined by CABC and manual setting processed results. The external LED driver ICs are necessary in order to transfer the PWM signal into driving power for LED backlight.

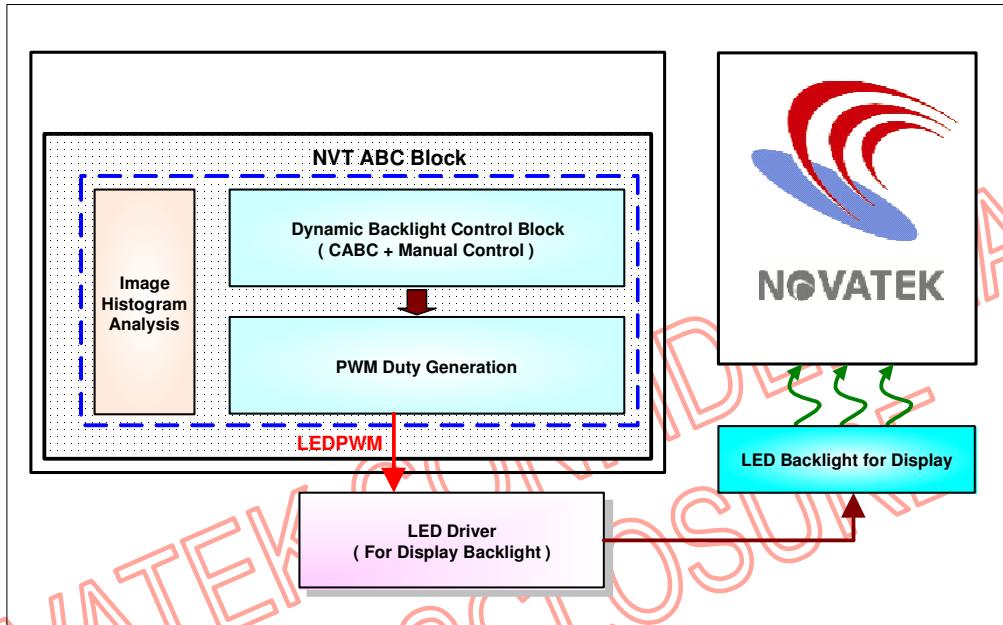


Fig. 5.16.1 One Application of ABC Dynamic Backlight Brightness Control

5.16.1 PWM Control Architecture

The below diagram illustrates the PWM duty combination architecture and its corresponding control registers for LED backlight control.

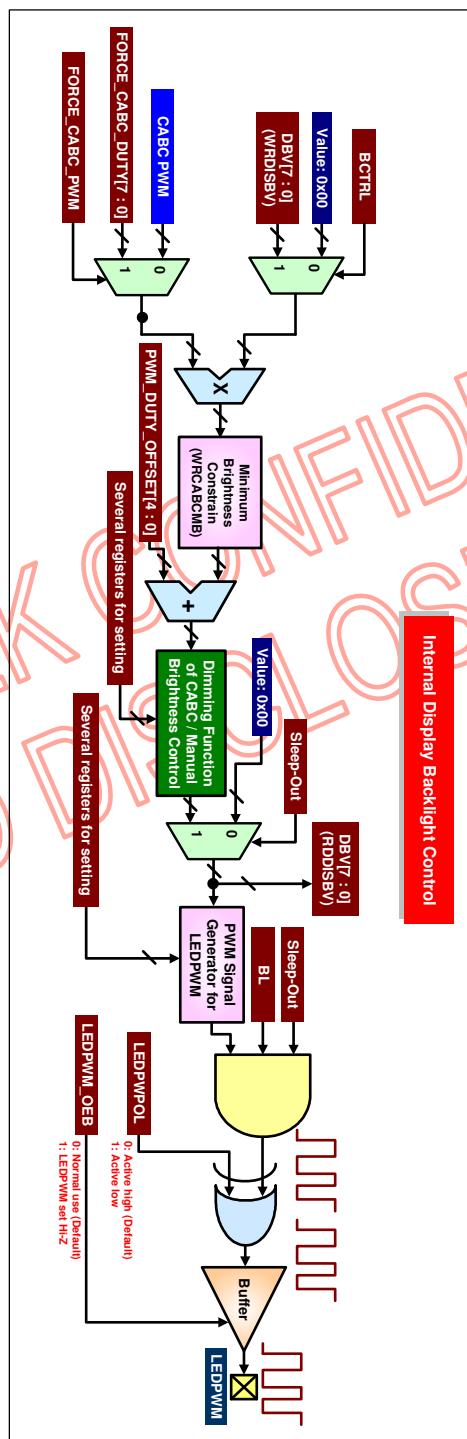


Fig. 5.16.2 Internal Display Backlight Control Combined with CABC

As shown in **Fig. 5.16.2**, the register bit “BL” is used to control the “LEDPWM” pin to output PWM signal. Normally, if user want to disable the display backlight completely and immediately, user can set “BL” = “0”. The below table shows some applications of register bit “LEDPWPOL”:

BL	LEDPWPOL	Status of LEDPWM Pin	Display Backlight Status
0	0	0 (Default)	Off
0	1	1	Off
1	0	Original polarity of PWM signal	On
1	1	Inversed polarity of PWM signal	On

The setting bit “BCTRL” is used to enable / disable the display backlight control functions (such as LEDPWM). When user set “BCTRL” = “0”, then the backlight will be turned off with dimming function, and the value of register DBV[7:0] (RDDISBV) will be “00h” after dimming period.

BCTRL	Value of DBV[7:0] (RDDISBV)	Display Backlight Status
0	00h	Off
1	Determined by CABC estimation	On

The display backlight brightness can be affected by setting register DBV[7:0] (here means WRDISBV) manually. Here are listed the application with register bits DBV[7:0] (WRDISBV), RDPWM[7:0], and RDPWM_L[7:0] in below table.

CABC Status: Off Mode (RDPWM[7:0] will be FFh) “FORCE_CABC_PWM”=“0”, WRCABCM[7:0] = 00h, PWM_DUTY_OFFSET[4:0]=00h, “BL”=“1”, “BCTRL”=“1”, Sleep-Out Mode		
Value of RDPWM_L[7:0]	Value of RDPWM [7:0]	Display Backlight Brightness
Determined by DBV[7:0] (Here means from WRDISBV)	FFh	Determined by DBV[7:0] manually (Here means from WRDISBV)

CABC Status: UI-Mode / Still-Mode / Moving-Mode “FORCE_CABC_PWM” = “0”, WRCABCM[7:0]=00h, PWM_DUTY_OFFSET[4:0]=00h, “BL”=“1”, “BCTRL”=“1”, Sleep-Out Mode		
Value of RDPWM_L[7: 0]	Value of RDPWM [7: 0]	Display Backlight Brightness
Determined by DBV[7:0] (Here means from WRDISBV)	Determined by CABC Function	Determined by DBV[7:0] x CABC Function (Here means DBV[7:0] from WRDISBV)

Writing the register DBV[7:0] (WRDISBV) in command address 51h is used to adjust the backlight brightness value. However, reading register DBV[7:0] (RDDISBV) from command address 52h is used to indicate the real PWM duty variation.

The register setting CMB[7:0] is used to limit the minimum PWM duty in order to prevent the backlight brightness too dark.

The register FORCE_CABC_DUTY[7:0] is used to perform a fixed PWM duty of CABC output while the register bit “FORCE_CABC_PWM” is set as “1”.

The “Sleep-Out” is a flag in order to indicate the driver IC is in “Sleep-Out” mode. Here are listed some conditions when driver IC is in Sleep-In or Sleep-Out status.

Driver IC Status	Sleep-Out Flag	CABC Function	Dimming Functions for CABC	Display Backlight Status
Sleep-In	0	Not Available	Not Available	Turn-Off
Sleep-Out	1	Available	Available	Controllable

5.16.2 Dimming Function for CABC/Force PWM Function and Manual Brightness Control

A dimming function (how fast to change the brightness from old to new level and what are brightness levels during the change) is used when changing from one brightness level to another. The dimming function curves for CABC /Force PWM Function and Manual Brightness Control can be configured the same or not the same in increment and decrement directions. The basic idea is described below.

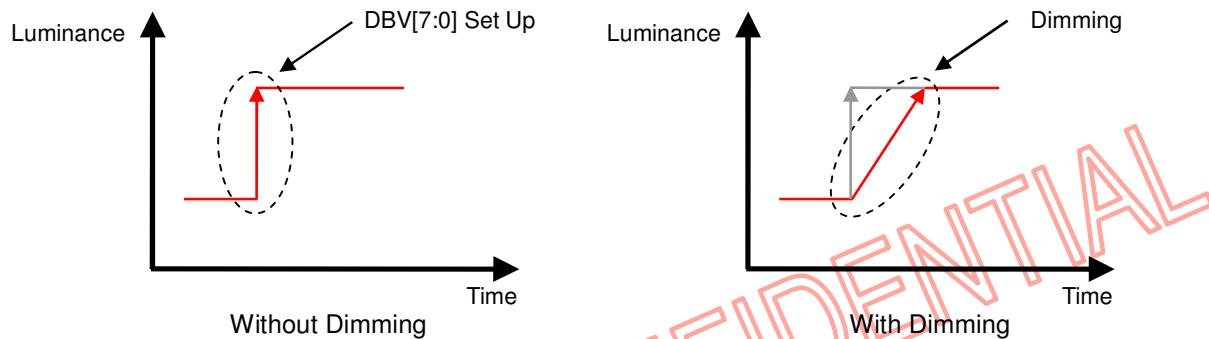


Fig. 5.16.3 Basic Concept of Dimming Function

The NT35521 provides PWM duty dimming mechanism for CABC/Force PWM Function and manual brightness control, and this dimming function can be enabled / disabled by register bit DD as the following table.

Enable Control for Dimming Function	
"DD" = "0"	Disable Dimming Function of CABC and Manual Brightness Control
"DD" = "1"	Enable Dimming Function of CABC and Manual Brightness Control

There are different register setting for rising dimming (increment dimming) and falling dimming (decrement dimming) in CABC Off-Mode, Still/UI-Mode and Moving-Mode respectively.

CABC Mode	Registers for Rising Dimming Setting	Registers for Falling Dimming Setting
Off-Mode	DIM_STEP_OFF[2:0] and DM_IN[3:0]	DIM_STEP_OFF[2:0] and DM_DE[3:0]
UI-Mode	DIM_STEP_STILL[2:0] and DM_IN[3:0]	DIM_STEP_STILL[2:0] and DM_DE[3:0]
Still-Mode	DIM_STEP_STILL[2:0] and DM_IN[3:0]	DIM_STEP_STILL[2:0] and DM_DE[3:0]
Moving-Mode	DIM_STEP_MOV[2:0] and DM_IN[3:0]	DIM_STEP_MOV[2:0] and DM_DE[3:0]

The total dimming steps and each step time can be set by registers DIM_STEP_OFF[2:0] / DIM_STEP_STILL[2:0] / DIM_STEP_MOV[2:0], DM_IN[3:0], and DM_DE[3:0], respectively. These three registers can determine some characteristics of dimming curves. The **Fig. 5.16.4** and **Fig. 5.16.5** illustrate the dimming curves for CABC Still-Mode and Moving-Mode respectively. The unit of registers DM_IN[3:0] and DM_DE[3:0] is “frames per step”. The unit of register DIM_STEP_OFF[2:0], DIM_STEP_STILL[2:0] and DIM_STEP_MOV[2:0] is “steps”.

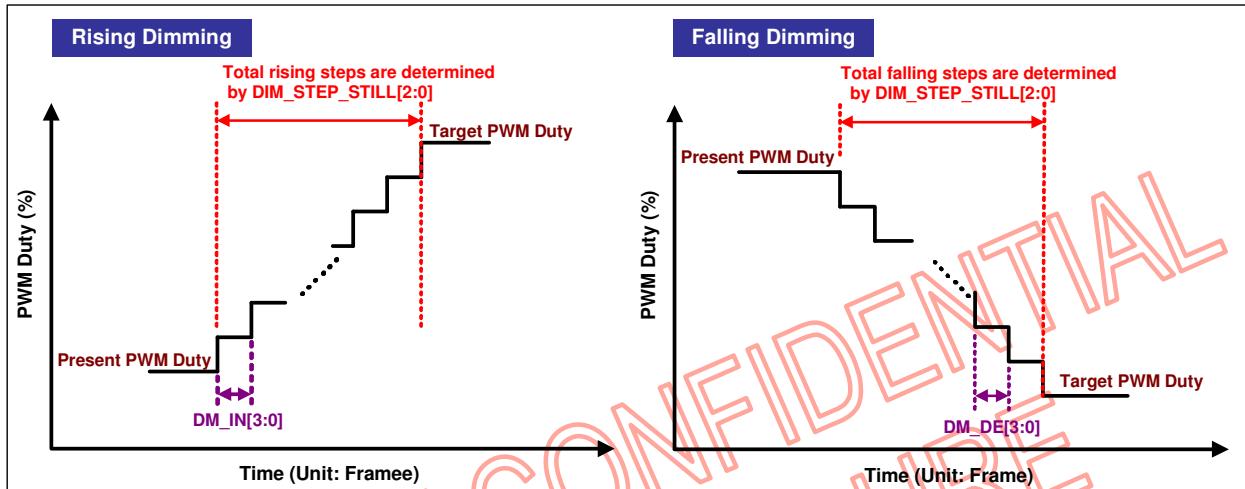


Fig. 5.16.4 Dimming Mechanism in CABC Still-Mode

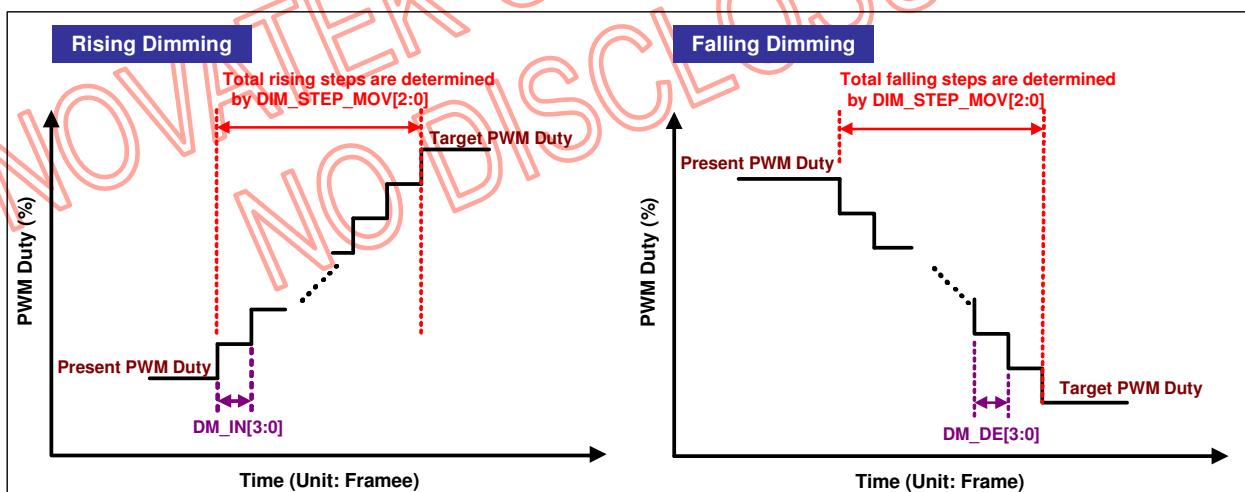


Fig. 5.16.5 Dimming Mechanism in CABC Moving-Mode

5.16.3 PWM Signal Setting for CABC

The registers PWMDIV[7:0] and PWM_DUTY_OFFSET[4:0] can change the frequency and duty compensation of the PWM signal. The PWM operation frequency “FOSC” is “not” the real PWM frequency, the “FOSC” is used to provide clock source for the internal PWM circuit. The PWM operation frequency can be chosen by setting register “PWMF”, and the real PWM frequency can be quickly estimated by the bellow formula.

PWMF[1:0]	PWM Operation Frequency (FOSC)	Real PWM Frequency of LEDPWM
00	5 MHz	PWM Frequency = $\frac{5 \text{ MHz}}{256 \times \text{PWMDIV}[7:0]}$
01	10 MHz	PWM Frequency = $\frac{10 \text{ MHz}}{256 \times \text{PWMDIV}[7:0]}$
1x	50 MHz	PWM Frequency = $\frac{50 \text{ MHz}}{256 \times \text{PWMDIV}[7:0]}$

For Example:

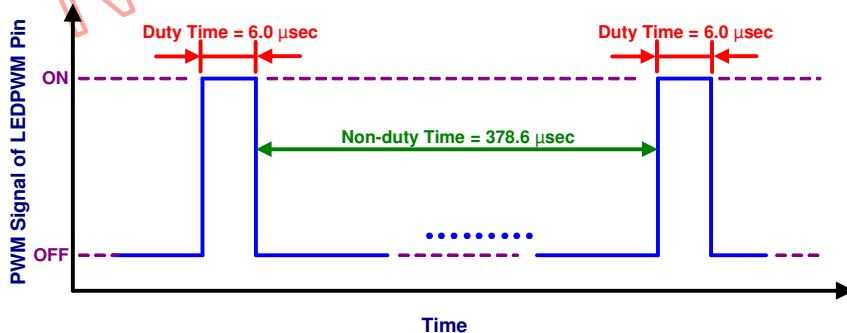
If the “PWMDIV[7:0]” = 0x0F, and “PWMF” = “1”, then

$$\text{PWM Frequency} = \frac{10 \text{ MHz}}{256 \times \text{PWMDIV}[7:0]} = \frac{10 \text{ MHz}}{256 \times 15} \approx 2.60 \text{ KHz}$$

In this condition, when PWM duty is estimated as “4” (Reading the register “DBV[7:0]” = 03h from RDDISBV), then the duty time of the PWM signal can be estimated as shown in below.

$$\text{PWM Duty Time} = \frac{4}{256} \times \frac{1}{2.60 \text{ KHz}} = 6.0 \mu\text{sec}$$

$$\text{PWM Non-Duty Time} = \frac{(256 - 4)}{256} \times \frac{1}{2.60 \text{ KHz}} = 378.6 \mu\text{sec}$$



The same, when PWM frequency is 2.60 KHz, and PWM duty of LEDPWM is 256 (Reading the register “DBV[7:0]” = FFh from RDDISBV), then the duty time can be estimated as shown in below.

$$\text{PWM Duty Time} = \frac{256}{256} \times \frac{1}{2.60 \text{ KHz}} = 384.6 \mu\text{sec}$$

Because the external LED driver needs some stable time to drive the LED backlight, this necessary stable time will reduce the effective PWM duty period, so the PWM_DUTY_OFFSET[4:0] is used to compensate effective PWM duty.

An example is shown in **Fig. 5.16.6**. When PWM duty of LEDPWM signal is 60%, the backlight brightness should be 60% of original. But user may find that the backlight brightness is 57% of original. So user can set PWM_DUTY_OFFSET[4:0] and let the backlight brightness becomes 60% of original.

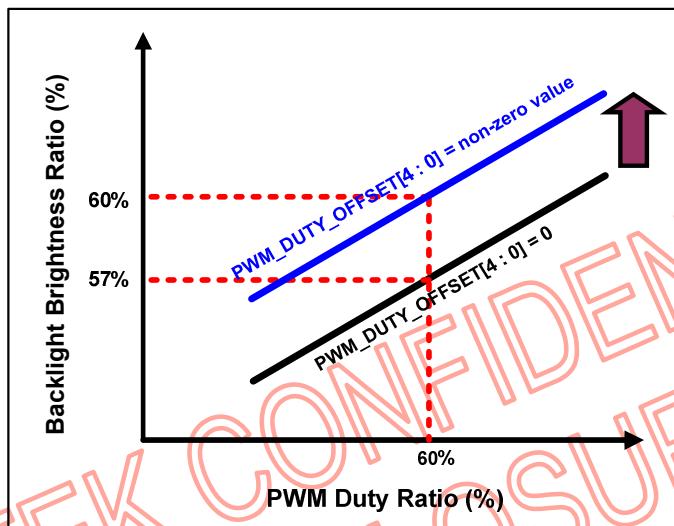
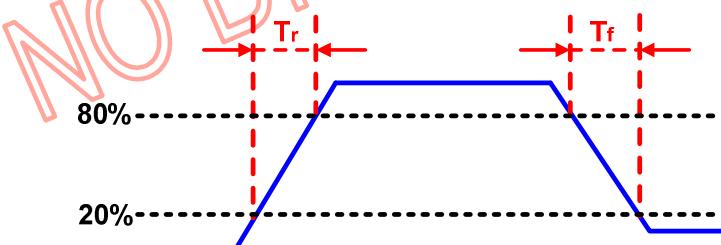


Fig. 5.16.6 Duty Compensation of PWMLED Signal

Note: The rising time (T_r) and falling time (T_f) of the "LEDPWM" signal are stipulated to be equal to or less than 15ns when maximum load is 30pF.



5.16.4 Content Adaptive Brightness Control (CABC)

A Content Adaptive Brightness Control (CABC) function can be used to reduce the power consumption of the luminance source. Content adaptation means that content grey level scale can be increased while simultaneously decreasing brightness of the backlight to achieve same perceived brightness. The adjusted grey level scale and thus the power consumption reduction depend on the content of the image. The NOVATEK CABC algorithm can adjust the brightness of each gray level without changing the original image contents.

The NOVATEK CABC function provides four operation modes, and these modes can be selected by the register 55h. See command "Write Content Adaptive Brightness Control (55h)" (bit C[1:0]) for more information. These four modes are described as below.

- Off Mode

Content Adaptive Brightness Control functionality is completely turn-off. In this mode, the NT35521 will use the original Gamma 2.2 registers setting for display. And if the function of "forced PWM duty" is turn-off (i.e. "FORCE_CABC_PWM" is set as "0"), the brightness ratio of CABC is 100% ("RDPWM[7:0]" = FFh).

- UI [User interface] Image Mode (UI-Mode)

This mode is applied to optimize for UI image. It is kept image quality as much as possible. Target power consumption reduction ratio is 10% or less. NT35521 provides flexible configuration for UI-Mode by setting the registers CABC_UI_PWM0[7:0] ~ CABC_UI_PWM3[7:0] to setting prefer brightness.

- Still Picture Mode (Still-Mode)

This mode is used to gain a better display quality for still picture. Some image quality degradation would be acceptable. Ideal power consumption reduction ratio is more than 30%. The NT35521 will automatically estimate a better gamma setting and PWM duty based on different image contents, so the reduction ratio of the power consumption of backlight is not a constant ratio, this ratio will vary between 10% ~ 40% with different image contents.

- Moving Image Mode (Moving-Mode)

User can select this mode to keep the moving image quality and reduce the power consumption of backlight. It is focused on the biggest power reduction with image quality degradation. Idea power consumption reduction ratio is more than 30%.

6 COMMAND DESCRIPTIONS

6.1 User Command Set

Table 6.1.1 User Command Set

Instruction	ACT	R/W	Address		Parameter										Function
			MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
NOP	Dir	W	00h	0000h	No Argument (0000h in Non-MIPI I/F)										No Operation
SWRESET	Cnd1	W	01h	0100h	No Argument (0000h in Non-MIPI I/F)										Software reset
RDDID	Dir	R	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read display ID	
				0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		
				0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		
RDNUMED	Dir	R	05h	X	X	P7	P6	P5	P4	P3	P2	P1	P0	Read No. of the Corrupted Packets on DSI	
RDDPM	Dir	R	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Power Mode	
RDDMADCTL	Dir	R	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display MADCTR	
RDDCOLMOD	Dir	R	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Pixel Format	
RDDIM	Dir	R	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Image Mode	
RDDSM	Dir	R	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Signal Mode	
RDDSDR	Dir	R	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read Display Self-diagnostic result	
SLPIN	DVS	W	10h	1000h	No Argument (0000h in Non-MIPI I/F)										Sleep in & booster off
SLPOUT	Dir	W	11h	1100h	No Argument (0000h in Non-MIPI I/F)										Sleep out & booster on
NORON	DVS	W	13h	1300h	No Argument (0000h in Non-MIPI I/F)										Normal mode on
INVOFF	DVS	W	20h	2000h	No Argument (0000h in Non-MIPI I/F)										Display inversion off (normal)
INVON	DVS	W	21h	2100h	No Argument (0000h in Non-MIPI I/F)										Display inversion on
ALLPOFF	DVS	W	22h	2200h	No Argument (0000h in Non-MIPI I/F)										All pixel off (black)
ALLPON	DVS	W	23h	2300h	No Argument (0000h in Non-MIPI I/F)										All pixel on (white)
GAMSET	DVS	W	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	Gamma curve select	
DISPOFF	DVS	W	28h	2800h	No Argument (0000h in Non-MIPI I/F)										Display off
DISPON	DVS	W	29h	2900h	No Argument (0000h in Non-MIPI I/F)										Display on
TEOFF	DVS	W	34h	3400h	No Argument (0000h in Non-MIPI I/F)										Tearing effect line off
TEON	DVS	W	35h	3500h	00h	-	-	-	-	-	-	-	M	Tearing effect mode set & on	
MADCTL	Cnd2	W	36h	3600h	00h	MY	MX	MV	ML	RGB	MH	RSMX	RSMY	Memory data access control	
IDMOFF	DVS	W	38h	3800h	No Argument (0000h in Non-MIPI I/F)										Idle mode off
IDMON	DVS	W	39h	3900h	No Argument (0000h in Non-MIPI I/F)										Idle mode on
COLMOD	Dir	W	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0	Interface pixel format	
STESL	DVS	W	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Set tearing effect scan line	
				4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0		
GSL	Dir	R	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8	Get scan line	
				4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0		
DSTBON	DVS	W	4Fh	4F00h	00h	-	-	-	-	-	-	-	DSTB	Deep standby mode on	
WRDISBV	DVS	W	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Write display brightness	
RDDISBV	Dir	R	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	Read display brightness value	

Table 6.1.1 User Command Set (Continued)

Instruction	ACT	R/W	Address		Parameter									Function
			MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRCTRLD	DVS	W	53h	5300h	00h	-	-	BCTRL	-	DD	BL	-	-	Write control display
RDCTRLD	Dir	R	54h	5400h	00h	-	-	BCTRL	-	DD	BL	-	-	Read control display value
WRCABC	DVS	W	55h	5500h	00h	C7	C6	C5	C4	C3	C2	C1	C0	Write CABC mode
RDCABC	Dir	R	56h	5600h	00h	C7	C6	C5	C4	C3	C2	C1	C0	Read CABC mode
WRCABCM	DVS	W	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Write CABC minimum brightness
RDCABCM	Dir	R	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	Read CABC minimum brightness
RDDDBS	Dir	R	A1h	A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	Read DDB start
				A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
				A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
				A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
				A104h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
				A105h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
				A106h	00h	1	1	1	1	1	1	1	1	
RDDDBC	Dir	R	A8h	A800h	00h	D7	D6	D5	D4	D3	D2	D1	D0	Read DDB continue
				:	00h	:	:	:	:	:	:	:	:	
				:	00h	1	1	1	1	1	1	1	1	
RDID1	Dir	R	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	Read ID1
RDID2	Dir	R	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	Read ID2
RDID3	Dir	R	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	Read ID3

Notes:

1. The following description is indicates the executing time of instructions.

No.	Symbol	Executing Time	
1	Dir (Direct)	At the received a completed instruction and parameter	
2	DVS (Display Vertical Sync.)	Synchronized with the next frame	
3	DHS (Display Horizontal Sync.)	Synchronized with the next line	
4	Cnd1 (By Conditional 1)	State	Executing time
		When Sleep In	Dir
		Other	DHS
5	Cnd2 (By Conditional 2)	State	Executing time
		B7, B6, B5	Dir
		B4, B3, B2, B1, B0	DVS

2. In MIPI interface, parameters of the command are stores onto registers when the last parameter of the command has been received. Also, parameters of the command are not stored onto registers if there has been happen a break. See more information on the section "DATA TRANSFER RECOVERY". This note is valid when a number of the parameters is equal or less than 32.

NOP (00h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	Write	00h	0000h	No Argument (0000h in Non-MIPI I/F)									

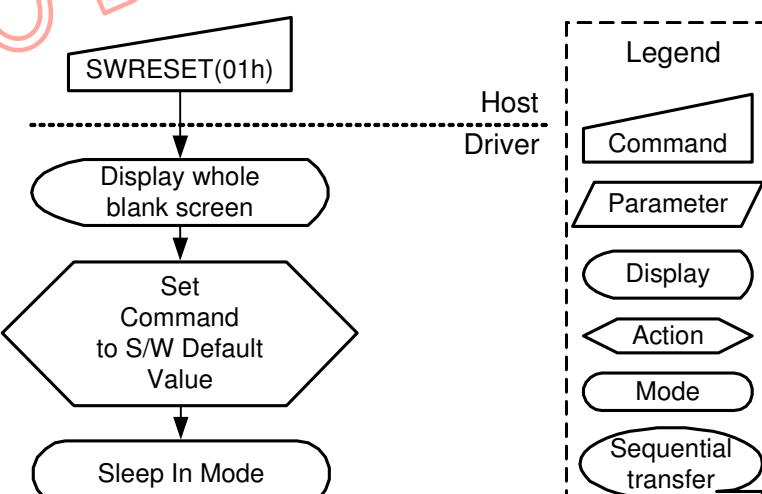
NOTE: “-” Don't care

Description	This command is empty command. It does not have effect on the display module. However it can be used to terminate RAM data write, RAM data read, RAM data write continue or RAM data read continue as described in RAMWR (Memory Write), RAMRD (Memory Read), RAMWRC (Memory Write Continue) and RAMRDC (Memory Read Continue) and parameter write commands.	
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
Default	Sleep In	Yes
	Status	Default Value
	Power On Sequence	N/A
	S/W Reset	N/A
Flow Chart	H/W Reset	N/A
	-	-

SWRESET: Software Reset (01h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
SWRESET	Write	01h	0100h	No Argument (0000h in Non-MIPI I/F)									

NOTE: “-” Don’t care

Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description) The display is blank immediately. <i>Note: The Frame Memory content is kept or not by this command.</i>									
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier’s factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A
Status	Default Value									
Power On Sequence	N/A									
S/W Reset	N/A									
H/W Reset	N/A									
Flow Chart	 <pre> graph TD SWRESET[SWRESET(01h)] --> Blank[Display whole blank screen] Blank --> Set[Set Command to S/W Default Value] Set --> Sleep[Sleep In Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 									

RDDID: Read Display ID (04h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDID	Read	04h	0400h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	
			0401h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	
			0402h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

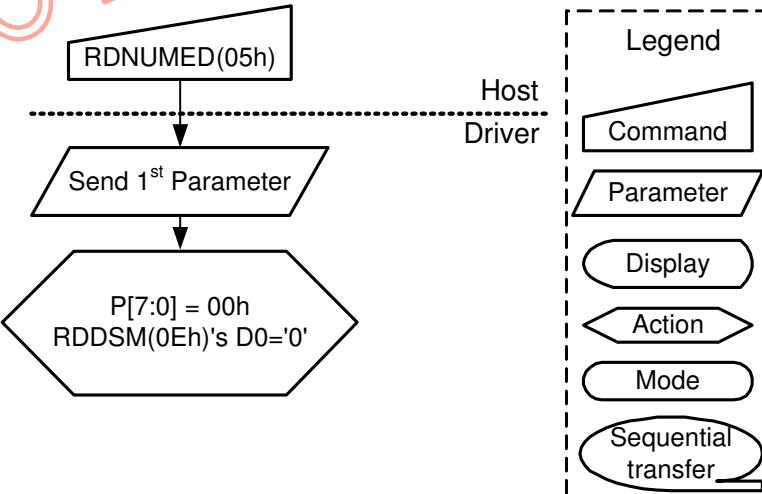
NOTE: “-” Don't care

Description	This read byte returns 24-bit display identification information. The 1 st parameter (ID1): the module's manufacture ID. The 2 nd parameter (ID2): the module/driver version ID. The 3 rd parameter (ID3): the module/driver ID. <i>Note: Commands RDID1/2/3 (DAh, DBh, DCh) read data correspond to the parameter 1, 2, 3 of the command 04h, respectively.</i>															
Restriction	-															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes					
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <th>After MTP</th> <th>Before MTP</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>MTP Values</td> <td>ID1=00h, ID2=80h, ID3=00h</td> </tr> <tr> <td>S/W Reset</td> <td>MTP Values</td> <td>ID1=00h, ID2=80h, ID3=00h</td> </tr> <tr> <td>H/W Reset</td> <td>MTP Values</td> <td>ID1=00h, ID2=80h, ID3=00h</td> </tr> </tbody> </table>			Status	Default Value	After MTP	Before MTP	Power On Sequence	MTP Values	ID1=00h, ID2=80h, ID3=00h	S/W Reset	MTP Values	ID1=00h, ID2=80h, ID3=00h	H/W Reset	MTP Values	ID1=00h, ID2=80h, ID3=00h
Status	Default Value															
After MTP	Before MTP															
Power On Sequence	MTP Values	ID1=00h, ID2=80h, ID3=00h														
S/W Reset	MTP Values	ID1=00h, ID2=80h, ID3=00h														
H/W Reset	MTP Values	ID1=00h, ID2=80h, ID3=00h														
Flow Chart	<pre> graph TD RDDID[RDDID(04h)] --> S1[/Send 1st Parameter ID1[7:0]/] S1 --> S2[/Send 2nd Parameter ID2[7:0]/] S2 --> S3[/Send 3rd Parameter ID3[7:0]/] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 															

RDNUMED: Read Number of Errors on DSI (05h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDNUMED	Read	05h	X	X	P7	P6	P5	P4	P3	P2	P1	P0	

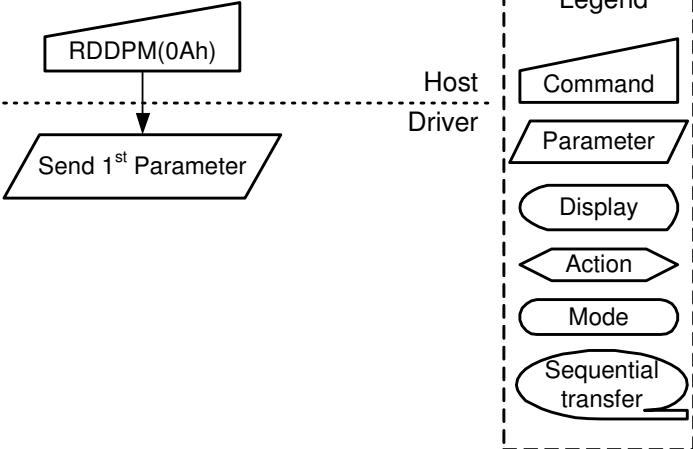
NOTE: “-“ Don't care

Description	<p>The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below.</p> <p>P[6..0] bits are telling a number of the parity errors.</p> <p>P[7] is set to “1” if there is overflow with P[6..0] bits.</p> <p>P[7..0] bits are set to “0”'s (as well as RDDSM(0Eh)'s D0 are set “0” at the same time) after there is sent the first parameter information (= The read function is completed).</p> <p>See also section “Acknowledge with Error Report (AwER)” and command RDDSM(0Eh).</p> <p>This command is used for MIPI DSI only. It is no function for others interface operation.</p>									
Restriction	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>No Changed</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	No Changed	H/W Reset	00h
Status	Default Value									
Power On Sequence	00h									
S/W Reset	No Changed									
H/W Reset	00h									
Flow Chart	 <pre> graph TD RDNUMED[RDNUMED(05h)] --> Send1st[Send 1st Parameter] Send1st --> Decision{P[7:0] = 00h RDDSM(0Eh)'s D0='0'} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 									

RDDPM: Read Display Power Mode (0Ah)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDPM	Read	0Ah	0A00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	

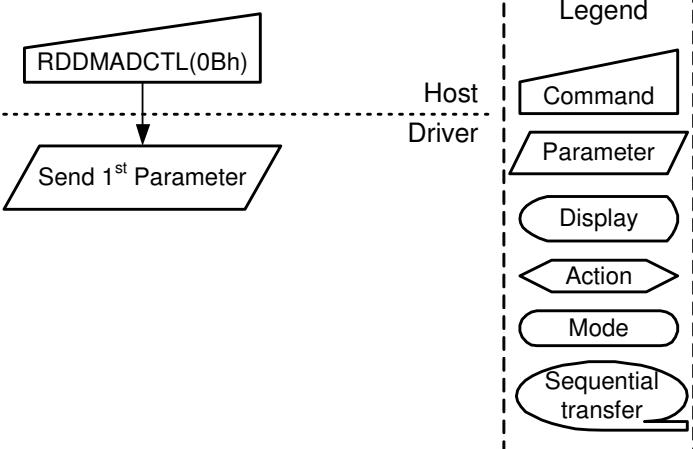
NOTE: “-“ Don't care

Description	This command indicates the current status of the display as described in the table below:	
	Bit	Description
	D7	Booster Voltage Status “1”=Booster On, “0”=Booster Off
	D6	Idle Mode On/Off “1”=Idle Mode On, “0”=Idle Mode Off
	D5	Partial Mode On/Off Set to “0” (not used)
	D4	Sleep In/Out “1” = Sleep Out Mode, “0” = Sleep In Mode
	D3	Display Normal Mode On/Off “1” = Display Normal On, “0” = Display Normal Off
	D2	Display On/Off “1” = Display is On, “0” = Display is Off
	D1	Not Defined Set to “0” (not used)
	D0	Not Defined Set to “0” (not used)
Restriction	-	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	08h
	S/W Reset	08h
	H/W Reset	08h
Flow Chart	 <pre> graph TD RDDPM[RDDPM(0Ah)] --> Send1st[Send 1st Parameter] Send1st --> HostDriver[Host Driver] HostDriver --> Legend[Legend] Legend --- Command[/Command/] Legend --- Parameter[/Parameter/] Legend --- Display([Display]) Legend --- Action([Action]) Legend --- Mode([Mode]) Legend --- SequentialTransfer([Sequential transfer]) </pre>	

RDDMADCTL: Read Display MADCTL (0Bh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDMADCTL	Read	0Bh	0B00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	

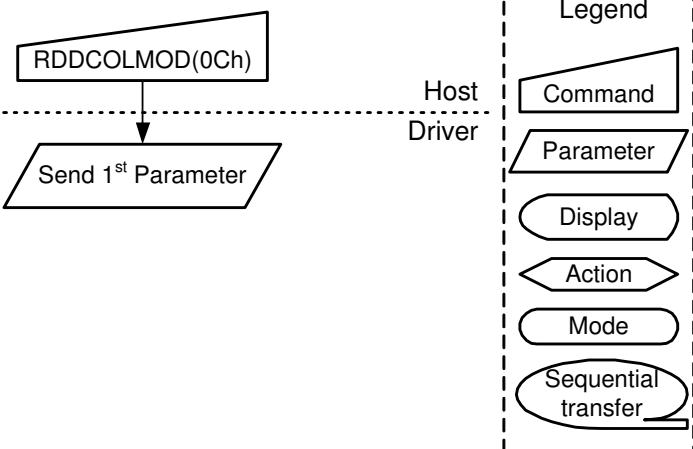
NOTE: “-“ Don’t care

Description	This command indicates the current status of the display as described in the table below:										
	Bit	Description	Value								
	D7	Row Address Order (MY)	Set to “0” (not used)								
	D6	Column Address Order (MX)	Set to “0” (not used)								
	D5	Row/Column Exchange (MV)	Set to “0” (not used)								
	D4	Vertical refresh Order (ML)	Set to “0” (not used)								
	D3	RGB-BGR Order	“0” = RGB color sequence “1” = BGR color sequence								
	D2	Horizontal refresh Order (MH)	Set to “0” (not used)								
	D1	Flip horizontal (RSMX)	“0” = Normal , “1” = Horizontal flip								
	D0	Flip vertical (RSMY)	“0” = Normal , “1” = Vertical flip								
Restriction	-										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability										
Normal Mode On, Idle Mode Off, Sleep Out	Yes										
Normal Mode On, Idle Mode On, Sleep Out	Yes										
Sleep In	Yes										
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>00h</td></tr> <tr> <td>S/W Reset</td><td>00h</td></tr> <tr> <td>H/W Reset</td><td>00h</td></tr> </tbody> </table>			Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value										
Power On Sequence	00h										
S/W Reset	00h										
H/W Reset	00h										
Flow Chart	 <pre> graph TD RDDMADCTL[RDDMADCTL(0Bh)] --> SD[Send 1st Parameter] SD --> HD[Host Driver] HD --> D[Display] style RDDMADCTL fill:none,stroke:none style SD fill:none,stroke:none style HD fill:none,stroke:none style D fill:none,stroke:none style L fill:none,stroke:none style P fill:none,stroke:none style A fill:none,stroke:none style M fill:none,stroke:none style ST fill:none,stroke:none L --- C[Command] L --- P[Parameter] L --- D[Display] L --- A[Action] L --- M[Mode] L --- ST[Sequential transfer] </pre>										

RDDCOLMOD: Read Display Pixel Format (0Ch)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDCOLMOD	Read	0Ch	0C00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	

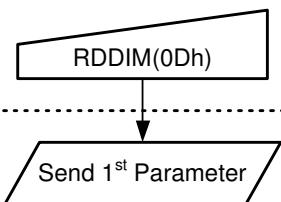
NOTE: “-“ Don't care

Description	This command indicates the current status of the display as described in the table below:									
	Bit	Description								
	D7	Not Defined								
	D6 ~ D4	RGB Interface Color Format “101” = 16-bit / pixel “110” = 18-bit / pixel “111” = 24-bit / pixel								
	D3	Not Defined								
	D2 ~ D0	Control Interface Color Format								
Restriction	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>70h</td> </tr> <tr> <td>S/W Reset</td> <td>70h</td> </tr> <tr> <td>H/W Reset</td> <td>70h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	70h	S/W Reset	70h	H/W Reset	70h
Status	Default Value									
Power On Sequence	70h									
S/W Reset	70h									
H/W Reset	70h									
Flow Chart	 <pre> graph TD RDDCOLMOD[RDDCOLMOD(0Ch)] --> Send1st[Send 1st Parameter] Send1st --> HostDriver[Host Driver] subgraph Legend [Legend] Command[Command] Parameter[Parameter] Display[Display] Action[Action] Mode[Mode] Sequential[Sequential transfer] end </pre>									

RDDIM: Read Display Image Mode (0Dh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDIM	Read	0Dh	0D00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	

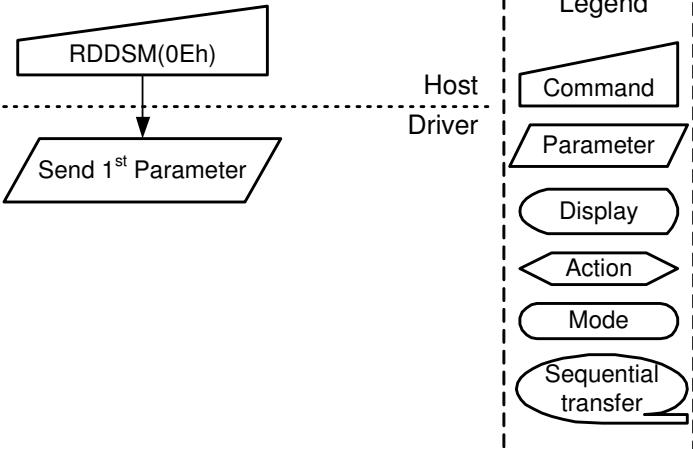
NOTE: “-” Don't care

Description	This command indicates the current status of the display as described in the table below:									
	Bit	Description								
	D7	Vertical Scrolling On/Off								
	D6	Horizontal Scrolling On/Off								
	D5	Inversion On/Off “1” = Inversion On, “0” = Inversion Off								
	D4	All Pixel On “1” = White display, “0” = Normal display								
	D3	All Pixel Off “1” = Black display, “0” = Normal display								
Restriction	D2 ~ D0 Gamma Curve Selection “000” = GC0, “001” = GC1 “010” = GC2, “011” = GC3 “100” to “111” = not defined									
	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value									
Power On Sequence	00h									
S/W Reset	00h									
H/W Reset	00h									
Flow Chart	 <pre> graph TD RDDIM["RDDIM(0Dh)"] --> SD[Send 1st Parameter] SD -.- HD[Host Driver] HD --> SD </pre>									
	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 									

RDDSM: Read Display Signal Mode (0Eh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDSM	Read	0Eh	0E00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	

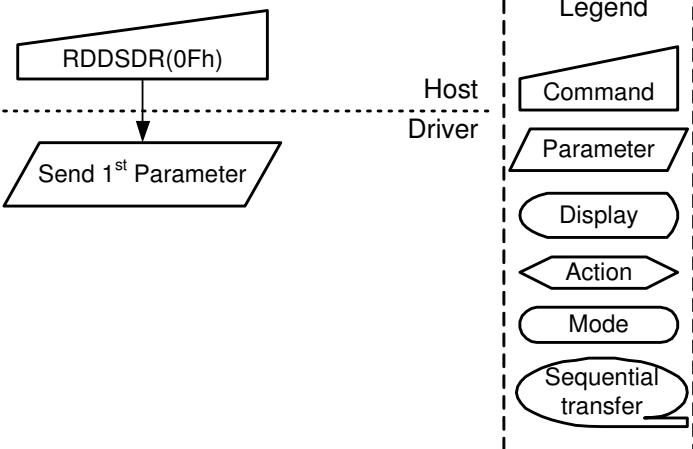
NOTE: “-“ Don't care

Description	This command indicates the current status of the display as described in the table below:									
	Bit	Description								
	D7	Tearing Effect Line On/Off								
	D6	Tearing Effect Line Mode								
	D5	Horizontal Sync. (HS, RGB I/F)On/Off								
	D4	Vertical Sync. (VS, RGB I/F)On/Off								
	D3	Pixel Clock (PCLK, RGB I/F)On/Off								
	D2	Data Enable (DE, RGB I/F)On/Off								
	D1	Not Defined								
	D0	Error on DSI								
Note: Bit D5 to D2 indicate current status of the lines when this command has been sent.										
Restriction	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h (Bit D0 No Changed)</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h (Bit D0 No Changed)	H/W Reset	00h
Status	Default Value									
Power On Sequence	00h									
S/W Reset	00h (Bit D0 No Changed)									
H/W Reset	00h									
Flow Chart	 <pre> graph TD RDDSM[RDDSM(0Eh)] --> Send1st[Send 1st Parameter] Send1st --> HostDriver[Host Driver] HostDriver --> Legend[Legend] Legend --- Command[Command] Legend --- Parameter[Parameter] Legend --- Display[Display] Legend --- Action[Action] Legend --- Mode[Mode] Legend --- Sequential[Sequential transfer] </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDSDR	Read	0Fh	0F00h	00h	D7	D6	D5	D4	D3	D2	D1	D0	

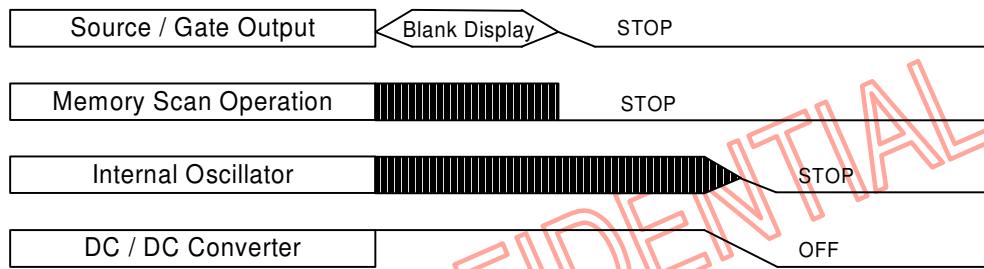
NOTE: “-“ Don’t care

Description	This command indicates the current status of the display as described in the table below:			
	Bit	Description	Value	
	D7	Register Loading Detection		
	D6	Functionality Detection		
	D5	Chip Attachment Detection		
	D4	Display Glass Break Detection		
	D3	Not Defined	Set to “0” (not used)	
	D2	Not Defined	Set to “0” (not used)	
	D1	Not Defined	Set to “0” (not used)	
Restriction	-			
	Register Availability	Status	Availability	
Default		Normal Mode On, Idle Mode Off, Sleep Out	Yes	
		Normal Mode On, Idle Mode On, Sleep Out	Yes	
		Sleep In	Yes	
		Status		
		Power On Sequence	00h	
		S/W Reset	00h	
		H/W Reset	00h	
Flow Chart	 <pre> graph TD RDDSDR[RDDSDR(0Fh)] --> Send1st[Send 1st Parameter] Send1st -.-> HostDriver[Host Driver] subgraph Legend [Legend] direction TB C[Command] --- P[Parameter] D[Display] --- A[Action] M[Mode] --- ST[Sequential transfer] end </pre>			

SLPIN: Sleep In (10h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
SLPIN	Write	10h	1000h	No Argument (0000h in Non-MIPI I/F)									

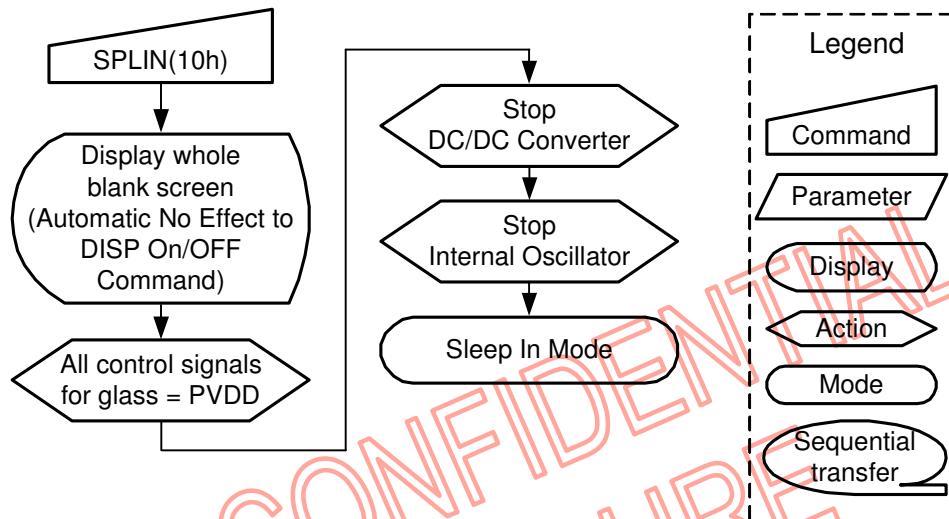
NOTE: “-“ Don't care

Description	<p>This command causes the TFT LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.</p>  <p>Control Interface as well as memory and registers are still working and the memory keeps (RAMKP="1") or loses (RAMKP="0") its contents. User can send PCLK, HS and VS information on RGB I/F for blank display after Sleep In command and this information is valid during 2 frames after Sleep In command if there is used Normal Mode On in Sleep Out-mode. Dimming function does not work when there is changing mode from Sleep Out to Sleep In. There is used an internal oscillator for blank display.</p>								
	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode
Status	Default Value								
Power On Sequence	Sleep In Mode								
S/W Reset	Sleep In Mode								
H/W Reset	Sleep In Mode								

It takes about 120 msec to get into Sleep In mode (booster off state) after SLPIN command issued.

The results of booster off can be check by RDDST (0Ah) command D7.

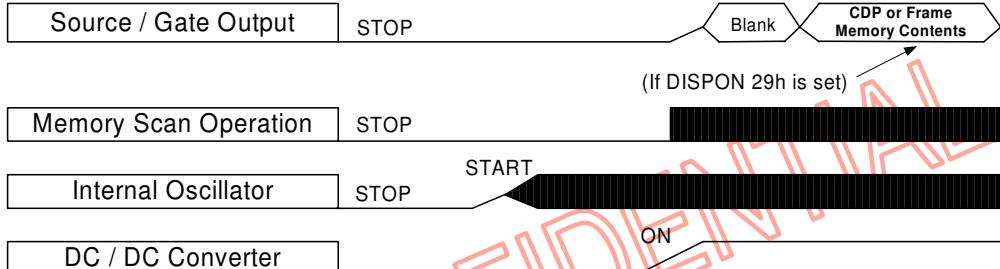
Flow Chart

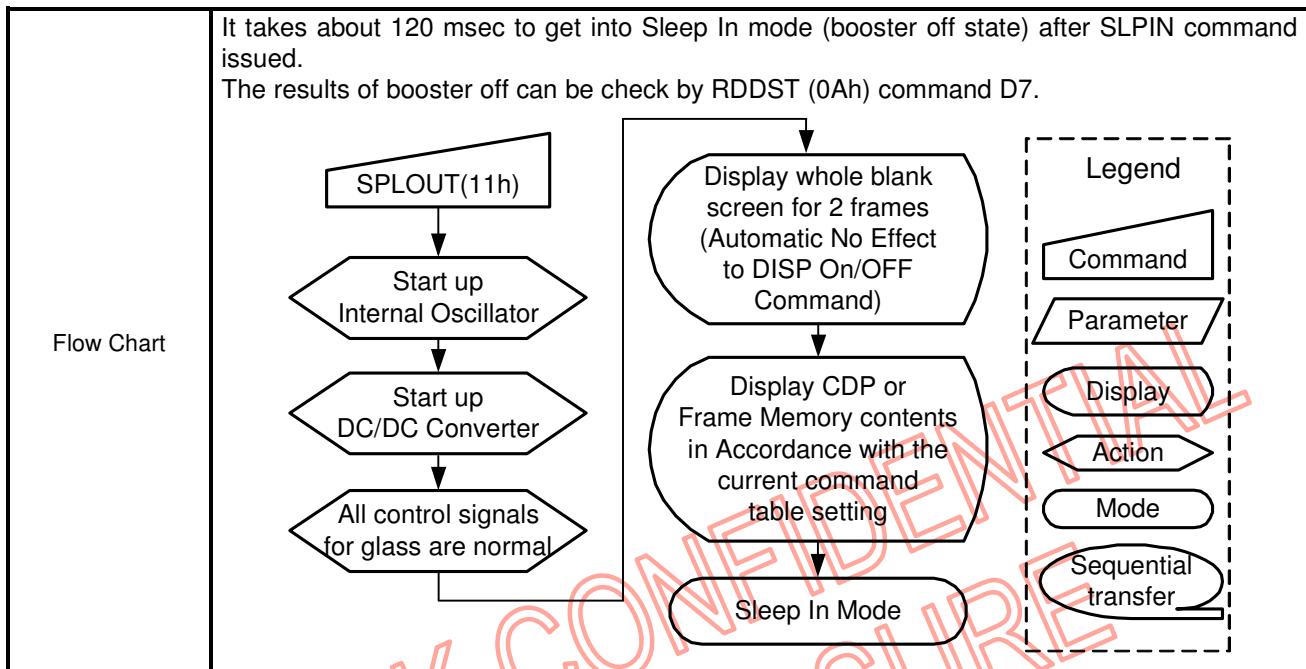


SLPOUT: Sleep Out (11h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
SLPOUT	Write	11h	1100h	No Argument (0000h in Non-MIPI I/F)									

NOTE: “-“ Don't care

Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.</p> 									
	<p>User can start to send PCLK, HS and VS information on RGB I/F before Sleep Out command and this information is valid at least 2 frames before Sleep Out command, if there is left Sleep In-mode to Sleep Out-mode in Normal Mode On. There is used an internal oscillator for blank display. NT35521 will do sequence control about gate control signals when sleep out.</p>									
	<p>Sleep Out Mode can only be exit by the Sleep In Command (10h), S/W reset command (01h) or H/W reset. It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. NT35521 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the NT35521 is already Sleep Out –mode. NT35521 is doing self-diagnostic functions during this 5msec. See also section 5.9. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>									
	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Sleep In Mode</td></tr> <tr> <td>S/W Reset</td><td>Sleep In Mode</td></tr> <tr> <td>H/W Reset</td><td>Sleep In Mode</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode
Status	Default Value									
Power On Sequence	Sleep In Mode									
S/W Reset	Sleep In Mode									
H/W Reset	Sleep In Mode									

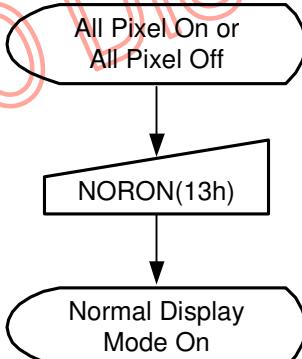


**NOVATEK CONFIDENTIAL
NO DISCLOSURE**

NORON: Normal Display Mode On (13h)

Inst / Para	R/W	Address		Parameter										
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0		
NORON	Write	13h	1300h		No Argument (0000h in Non-MIPI I/F)									

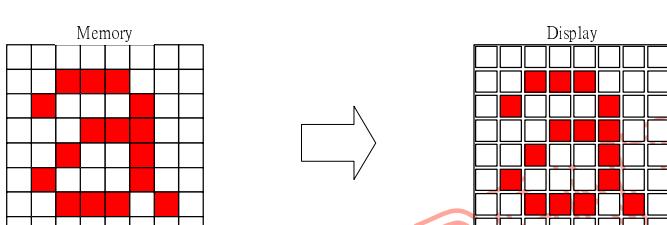
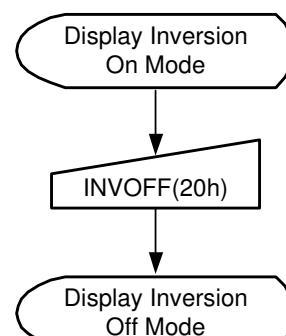
NOTE: “-“ Don't care

Description	This command returns the display to normal mode. Normal display mode on. Exit from NORON by the All Pixels On or All Pixels Off command. There is no abnormal visual effect during mode change.									
Restriction	This command has no effect when Normal Display mode is active.									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Mode On</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Mode On</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Mode On</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On
Status	Default Value									
Power On Sequence	Normal Mode On									
S/W Reset	Normal Mode On									
H/W Reset	Normal Mode On									
Flow Chart	 <pre> graph TD A([All Pixel On or All Pixel Off]) --> B[NORON(13h)] B --> C([Normal Display Mode On]) </pre>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

INVOFF: Display Inversion Off (20h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
INVOFF	Write	20h	2000h	No Argument (0000h in Non-MIPI I/F)									

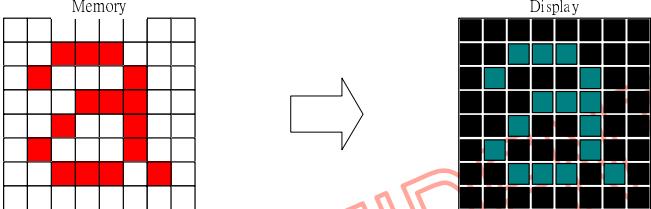
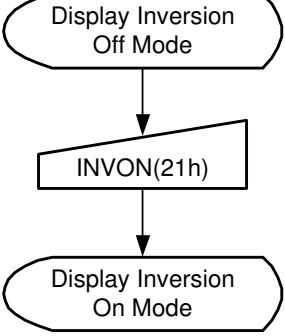
NOTE: “-“ Don’t care

Description	<p>This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status.</p> <p>(Example)</p> 									
Restriction	This command has no effect when module is already in Inversion Off mode.									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off
Status	Default Value									
Power On Sequence	Display Inversion off									
S/W Reset	Display Inversion off									
H/W Reset	Display Inversion off									
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 									

INVON: Display Inversion On (21h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
INVON	Write	21h	2100h	No Argument (0000h in Non-MIPI I/F)									

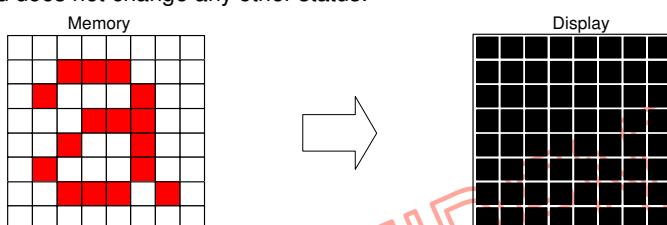
NOTE: “-“ Don't care

Description	<p>This command is used to enter display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.</p> <p>(Example)</p> 								
Restriction	This command has no effect when module is already in Inversion On mode.								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Inversion off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Inversion off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off
Status	Default Value								
Power On Sequence	Display Inversion off								
S/W Reset	Display Inversion off								
H/W Reset	Display Inversion off								
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

ALLPOFF: All Pixel Off (22h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
ALLPOFF	Write	22h	2200h	No Argument (0000h in Non-MIPI I/F)									

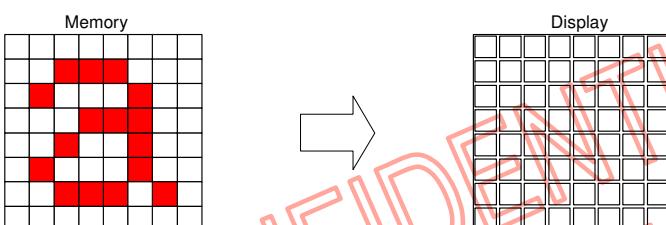
NOTE: “-“ Don’t care

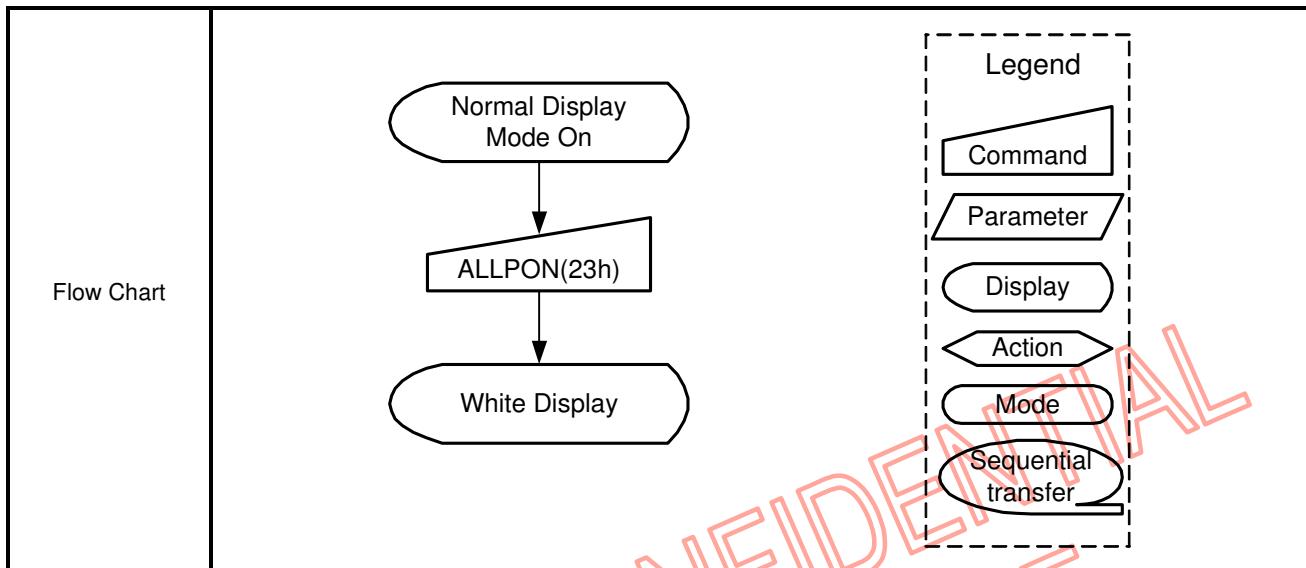
Description	<p>This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p>  <p>(Example)</p> <p>“All Pixels On”, “Normal Display Mode On” commands are used to leave this mode. The display panel is showing the content of the frame memory after “Normal Display On” command.</p>								
Restriction	This command has no effect when module is already in All Pixel Off mode.								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All pixel off</td> </tr> <tr> <td>S/W Reset</td> <td>All pixel off</td> </tr> <tr> <td>H/W Reset</td> <td>All pixel off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	All pixel off	S/W Reset	All pixel off	H/W Reset	All pixel off
Status	Default Value								
Power On Sequence	All pixel off								
S/W Reset	All pixel off								
H/W Reset	All pixel off								
Flow Chart	<pre> graph TD A([Normal Display Mode On]) --> B[/ALLPOFF(22h)] B --> C([Black Display]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

ALLPON: All Pixel On (23h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
ALLPON	Write	23h	2300h	No Argument (0000h in Non-MIPI I/F)									

NOTE: “-“ Don't care

Description	<p>This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>(Example)</p>  <p>“All Pixels Off”, “Normal Display Mode On” commands are used to leave this mode. The display panel is showing the content of the frame memory after “Normal Display On” command.</p>								
Restriction	This command has no effect when module is already in all Pixel On mode.								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>All pixel off</td> </tr> <tr> <td>S/W Reset</td> <td>All pixel off</td> </tr> <tr> <td>H/W Reset</td> <td>All pixel off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	All pixel off	S/W Reset	All pixel off	H/W Reset	All pixel off
Status	Default Value								
Power On Sequence	All pixel off								
S/W Reset	All pixel off								
H/W Reset	All pixel off								

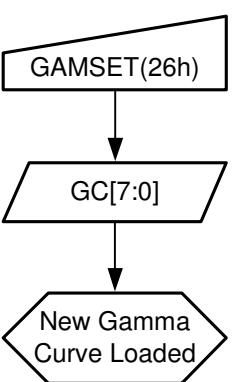


**NOVATEK CONFIDENTIAL
NO DISCLOSURE**

GAMSET: Gamma Set (26h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GAMSET	Write	26h	2600h	00h	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	

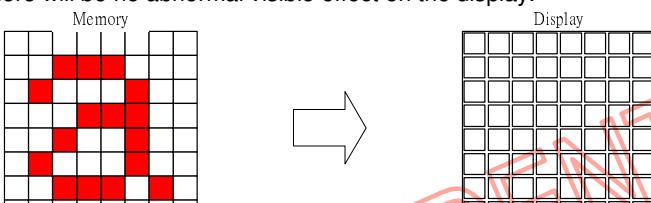
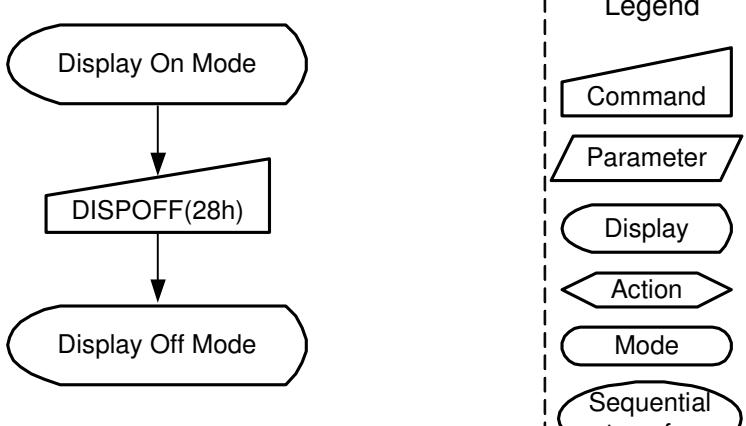
NOTE: “-“ Don't care

Description	<p>This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.</p> <table border="1"> <thead> <tr> <th>GC[7:0]</th><th>Parameter</th><th>Curve Selected</th></tr> </thead> <tbody> <tr> <td>01h</td><td>GC0</td><td>Gamma Curve 1 (G=2.2)</td></tr> <tr> <td>02h</td><td>GC1</td><td>Reserved</td></tr> <tr> <td>04h</td><td>GC2</td><td>Reserved</td></tr> <tr> <td>08h</td><td>GC3</td><td>Reserved</td></tr> </tbody> </table> <p><i>Note: All other values are undefined.</i></p>	GC[7:0]	Parameter	Curve Selected	01h	GC0	Gamma Curve 1 (G=2.2)	02h	GC1	Reserved	04h	GC2	Reserved	08h	GC3	Reserved
GC[7:0]	Parameter	Curve Selected														
01h	GC0	Gamma Curve 1 (G=2.2)														
02h	GC1	Reserved														
04h	GC2	Reserved														
08h	GC3	Reserved														
Restriction	<p>Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma curve until valid is received.</p>															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h							
Status	Default Value															
Power On Sequence	01h															
S/W Reset	01h															
H/W Reset	01h															
Flow Chart	 <pre> graph TD A[GAMSET(26h)] --> B[GC[7:0]] B --> C{New Gamma Curve Loaded} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 															

DISPOFF: Display Off (28h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
DISPOFF	Write	28h	2800h	No Argument (0000h in Non-MIPI I/F)									

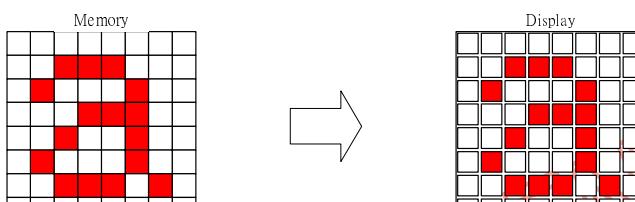
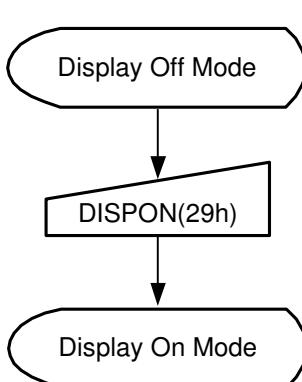
NOTE: “-“ Don’t care

Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.</p> <p>(Example)</p> 								
Restriction	This command has no effect when module is already in Display Off mode.								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value								
Power On Sequence	Display off								
S/W Reset	Display off								
H/W Reset	Display off								
Flow Chart	 <pre> graph TD A([Display On Mode]) --> B[DISPOFF(28h)] B --> C([Display Off Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

DISPON: Display On (29h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
DISPON	Write	29h	2900h	No Argument (0000h in Non-MIPI I/F)									

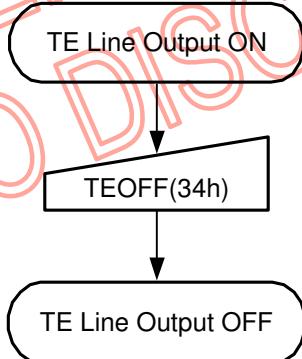
NOTE: “-“ Don't care

Description	<p>This command is used to recover from DISPLAY OFF mode. Output from Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status.</p> <p>(Example)</p> 								
Restriction	This command has no effect when module is already in Display On mode.								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Display off</td></tr> <tr> <td>S/W Reset</td><td>Display off</td></tr> <tr> <td>H/W Reset</td><td>Display off</td></tr> </tbody> </table>	Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value								
Power On Sequence	Display off								
S/W Reset	Display off								
H/W Reset	Display off								
Flow Chart	 <pre> graph TD A([Display Off Mode]) --> B[DISPON(29h)] B --> C([Display On Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

TEOFF: Tearing Effect Line OFF (34h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
TEOFF	Write	34h	3400h	No Argument (0000h in Non-MIPI I/F)									

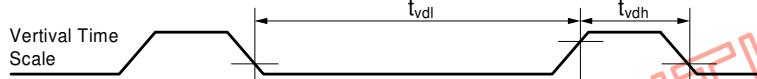
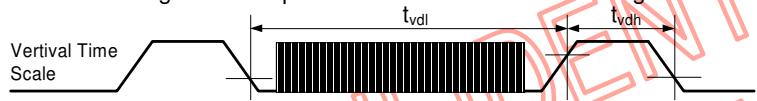
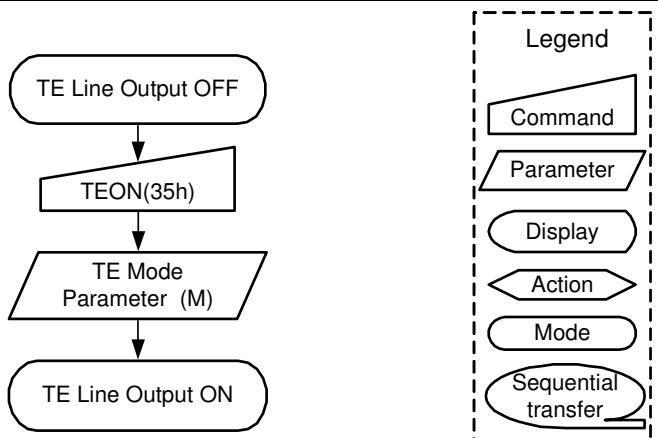
NOTE: “-“ Don't care

Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.	
Restriction	This command has no effect when Tearing Effect output is already OFF.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Tearing Effect off
	S/W Reset	Tearing Effect off
	H/W Reset	Tearing Effect off
Flow Chart	 <pre> graph TD A([TE Line Output ON]) --> B[TEOFF(34h)] B --> C([TE Line Output OFF]) </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

TEON: Tearing Effect Line ON (35h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
TEON	Write	35h	3500h	00h	-	-	-	-	-	-	-	-	M

NOTE: “-“ Don’t care

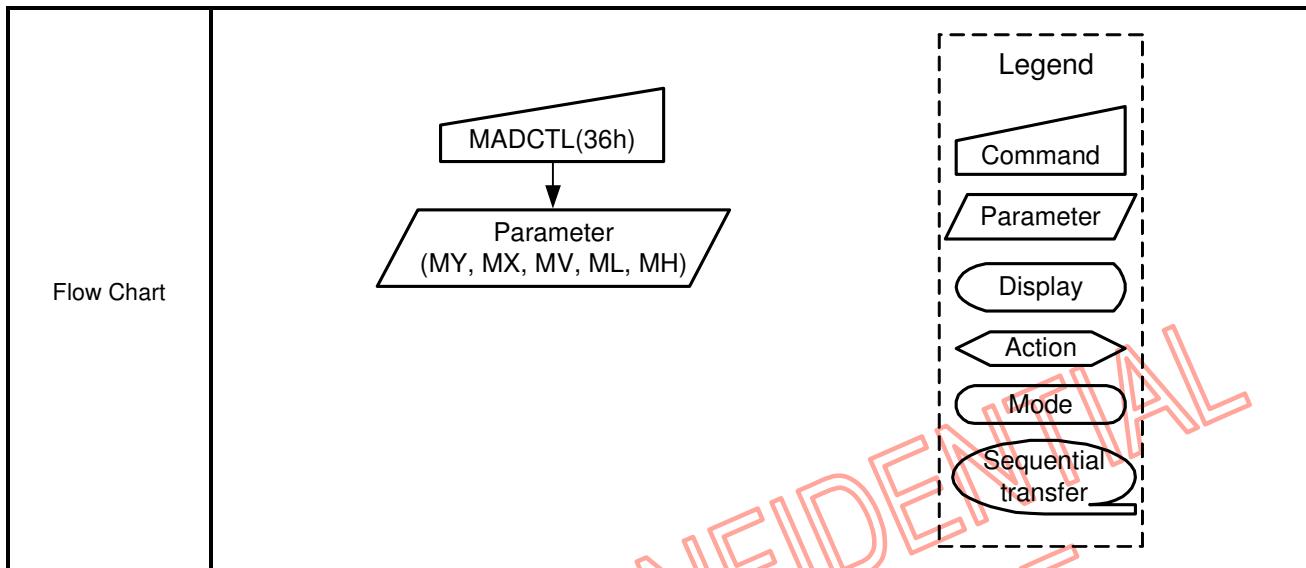
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.</p> <p>The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line. (“-“ = Don’t Care).</p> <p>When M = “0”: The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>When M = “1”: The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.</p>  <p><i>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</i></p>								
Restriction	This command has no effect when Tearing Effect output is already ON.								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Tearing Effect off</td> </tr> <tr> <td>S/W Reset</td> <td>Tearing Effect off</td> </tr> <tr> <td>H/W Reset</td> <td>Tearing Effect off</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	Tearing Effect off	S/W Reset	Tearing Effect off	H/W Reset	Tearing Effect off
Status	Default Value								
Power On Sequence	Tearing Effect off								
S/W Reset	Tearing Effect off								
H/W Reset	Tearing Effect off								
Flow Chart	 <pre> graph TD A([TE Line Output OFF]) --> B[/TEON(35h)/] B --> C{TE Mode Parameter (M)} C --> D([TE Line Output ON]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

MADCTL: Memory Data Access Control (36h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
MADCTL	Write	36h	3600h	00h	MY	MX	MV	ML	RGB	MH	RSMX	RSMY	

NOTE: “-“ Don’t care

Description	This command defines display direction of image. This command makes no change on the other driver status.													
	Bit	NAME												
	MY	Row Address Order												
	MX	Column Address Order												
	MV	Row/Column Exchange												
	ML	Vertical Refresh Order												
	RGB	RGB-BGR Order												
	MH	Horizontal Refresh Order												
	RSMX	Flip Horizontal												
	RSMY	Flip Vertical												
Restriction	-													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value													
Power On Sequence	00h													
S/W Reset	00h													
H/W Reset	00h													

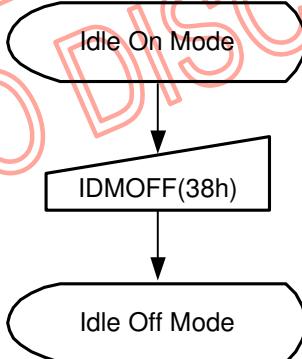


NOVATEK CONFIDENTIAL
NO DISCLOSURE

IDMOFF: Idle Mode Off (38h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
IDMOFF	Write	38h	3800h	No Argument (0000h in Non-MIPI I/F)									

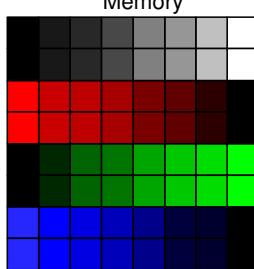
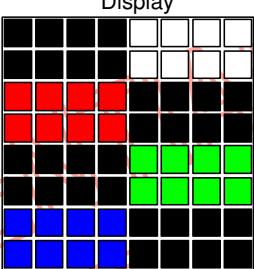
NOTE: “-“ Don't care

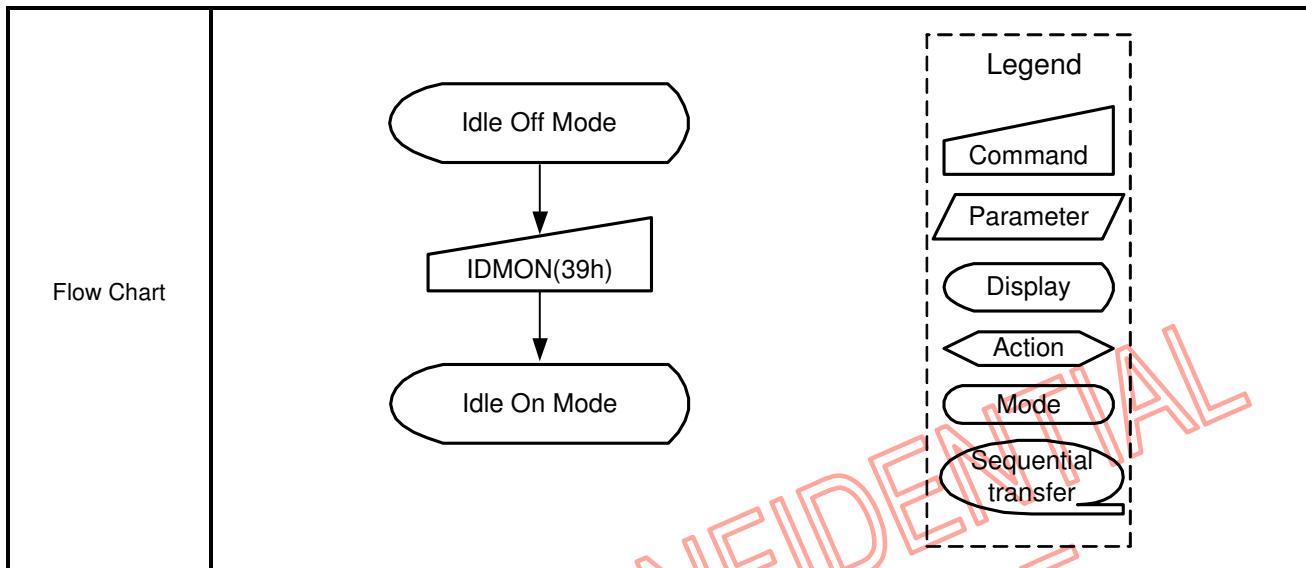
Description	This command is used to recover from Idle mode on. In the idle off mode, display panel can display maximum 16.7M colors.	
Restriction	This command has no effect when module is already in Idle Off mode.	
Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In	Yes
Default	Status	Default Value
	Power On Sequence	Idle Mode off
	S/W Reset	Idle Mode off
	H/W Reset	Idle Mode off
Flow Chart	 <pre> graph TD A([Idle On Mode]) --> B[IDMOFF(38h)] B --> C([Idle Off Mode]) </pre> <p>The flowchart illustrates the process of transitioning from 'Idle On Mode' to 'Idle Off Mode'. It starts with an oval labeled 'Idle On Mode', followed by a trapezoid labeled 'IDMOFF(38h)', and ends with an oval labeled 'Idle Off Mode'. Arrows indicate the sequential flow between these states.</p>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer

IDMON: Idle Mode On (39h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
IDMON	Write	39h	3900h	No Argument (0000h in Non-MIPI I/F)									

NOTE: “-“ Don’t care

Description	<p>This command is used to enter into Idle mode on. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G, and B in Frame Memory, 8 color depth data is displayed.</p> <div style="display: flex; align-items: center; justify-content: space-around;"> <div style="text-align: center;"> <p>Memory</p>  </div> <div style="text-align: center;">  </div> </div>																																									
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th colspan="4">Memory Contents vs. Display Colors</th> </tr> <tr> <th></th> <th>R₇R₆R₅R₄R₃R₂R₁R₀</th> <th>R₇G₆G₅G₄G₃G₂G₁G₀</th> <th>B₇B₆B₅B₄B₃B₂B₁B₀</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXXXX</td> <td>0XXXXXXX</td> <td>0XXXXXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXXXXX</td> <td>0XXXXXXX</td> <td>1XXXXXXX</td> </tr> <tr> <td>Red</td> <td>1XXXXXXX</td> <td>0XXXXXXX</td> <td>0XXXXXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXXXXXX</td> <td>0XXXXXXX</td> <td>1XXXXXXX</td> </tr> <tr> <td>Green</td> <td>0XXXXXXXX</td> <td>1XXXXXXXX</td> <td>0XXXXXXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXXXXXX</td> <td>1XXXXXXXX</td> <td>1XXXXXXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXXXXXX</td> <td>1XXXXXXXX</td> <td>0XXXXXXXX</td> </tr> <tr> <td>White</td> <td>1XXXXXXXX</td> <td>1XXXXXXXX</td> <td>1XXXXXXXX</td> </tr> </tbody> </table>			Memory Contents vs. Display Colors					R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	R ₇ G ₆ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀	Black	0XXXXXXX	0XXXXXXX	0XXXXXXX	Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX	Red	1XXXXXXX	0XXXXXXX	0XXXXXXX	Magenta	1XXXXXXXX	0XXXXXXX	1XXXXXXX	Green	0XXXXXXXX	1XXXXXXXX	0XXXXXXXX	Cyan	0XXXXXXXX	1XXXXXXXX	1XXXXXXXX	Yellow	1XXXXXXXX	1XXXXXXXX	0XXXXXXXX	White	1XXXXXXXX	1XXXXXXXX
Memory Contents vs. Display Colors																																										
	R ₇ R ₆ R ₅ R ₄ R ₃ R ₂ R ₁ R ₀	R ₇ G ₆ G ₅ G ₄ G ₃ G ₂ G ₁ G ₀	B ₇ B ₆ B ₅ B ₄ B ₃ B ₂ B ₁ B ₀																																							
Black	0XXXXXXX	0XXXXXXX	0XXXXXXX																																							
Blue	0XXXXXXX	0XXXXXXX	1XXXXXXX																																							
Red	1XXXXXXX	0XXXXXXX	0XXXXXXX																																							
Magenta	1XXXXXXXX	0XXXXXXX	1XXXXXXX																																							
Green	0XXXXXXXX	1XXXXXXXX	0XXXXXXXX																																							
Cyan	0XXXXXXXX	1XXXXXXXX	1XXXXXXXX																																							
Yellow	1XXXXXXXX	1XXXXXXXX	0XXXXXXXX																																							
White	1XXXXXXXX	1XXXXXXXX	1XXXXXXXX																																							
Restriction	This command has no effect when module is already in Idle On mode																																									
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																															
Status	Availability																																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																																									
Sleep In	Yes																																									
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle Mode off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle Mode off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle Mode off</td> </tr> </tbody> </table>			Status	Default Value	Power On Sequence	Idle Mode off	S/W Reset	Idle Mode off	H/W Reset	Idle Mode off																															
Status	Default Value																																									
Power On Sequence	Idle Mode off																																									
S/W Reset	Idle Mode off																																									
H/W Reset	Idle Mode off																																									

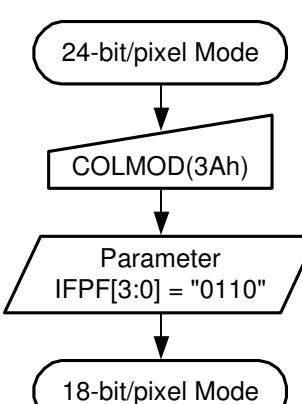


NOVATEK CONFIDENTIAL
NO DISCLOSURE

COLMOD: Interface Pixel Format (3Ah)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
COLMOD	Write	3Ah	3A00h	00h	VIPF3	VIPF2	VIPF1	VIPF0	IFPF3	IFPF2	IFPF1	IFPF0	

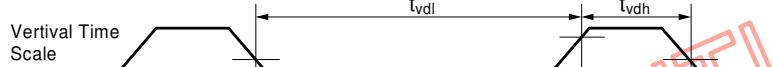
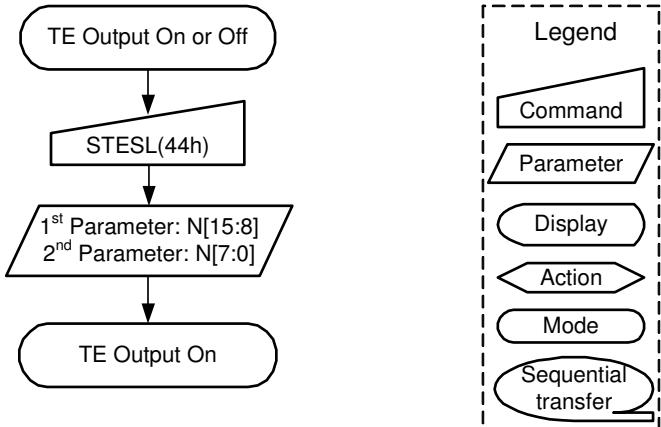
NOTE: “-” Don't care

Description	This command is used to define the format of RGB picture data, which is to be transferred via the RGB or MCU interface. The formats are shown in the table:									
	<table border="1"> <thead> <tr> <th>Bit</th> <th>NAME</th> <th>DESCRIPTION</th> </tr> </thead> <tbody> <tr> <td>VIPF[3:0]</td> <td>Pixel Format for RGB Interface</td> <td>“0101” = 16-bit/pixel “0110” = 18-bit/pixel “0111” = 24-bit/pixel The others = not defined</td> </tr> <tr> <td>IFPF[3:0]</td> <td>Pixel Format for MCU Interface</td> <td>Set to “0” (not used)</td> </tr> </tbody> </table>		Bit	NAME	DESCRIPTION	VIPF[3:0]	Pixel Format for RGB Interface	“0101” = 16-bit/pixel “0110” = 18-bit/pixel “0111” = 24-bit/pixel The others = not defined	IFPF[3:0]	Pixel Format for MCU Interface
Bit	NAME	DESCRIPTION								
VIPF[3:0]	Pixel Format for RGB Interface	“0101” = 16-bit/pixel “0110” = 18-bit/pixel “0111” = 24-bit/pixel The others = not defined								
IFPF[3:0]	Pixel Format for MCU Interface	Set to “0” (not used)								
Restriction	There is no visible effect until the Frame Memory is written to.									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>70h</td> </tr> <tr> <td>S/W Reset</td> <td>70h</td> </tr> <tr> <td>H/W Reset</td> <td>70h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	70h	S/W Reset	70h	H/W Reset	70h
Status	Default Value									
Power On Sequence	70h									
S/W Reset	70h									
H/W Reset	70h									
Flow Chart	 <pre> graph TD A([24-bit/pixel Mode]) --> B[COLMOD(3Ah)] B --> C{Parameter IFPF[3:0] = "0110"} C --> D([18-bit/pixel Mode]) </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

STESL: Set Tearing Effect Scan Line (44h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
STESL	Write	44h	4400h	00h	N15	N14	N13	N12	N11	N10	N9	N8	
			4401h	00h	N7	N6	N5	N4	N3	N2	N1	N0	

NOTE: “-“ Don’t care

Description	<p>This command turns on the display module’s Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MADCTL bit ML.</p> <p>The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line mode. The Tearing Effect Output line consists of V-Blanking information only.</p>  <p>Note that STESL with N[15:0] = "000h" is equivalent to TEON with M = "0".</p> <p>The Tearing Effect Output line shall be active low when the display module is in Sleep in mode.</p> <p>This command takes effect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON (35h)" or "STESL (44h) command" until the end of the frame.</p>									
Restriction	Parameter range $0 \leq N[15:0] \leq 1280 + \text{Porch Line}$									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0000h</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	0000h	S/W Reset	0000h	H/W Reset	0000h
Status	Default Value									
Power On Sequence	0000h									
S/W Reset	0000h									
H/W Reset	0000h									
Flow Chart	 <pre> graph TD A([TE Output On or Off]) --> B[STESL(44h)] B --> C{1st Parameter: N[15:8] / 2nd Parameter: N[7:0]} C --> D([TE Output On]) </pre>									

GSL: Get Scan Line (45h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
GSL	Read	45h	4500h	00h	N15	N14	N13	N12	N11	N10	N9	N8	
			4501h	00h	N7	N6	N5	N4	N3	N2	N1	N0	

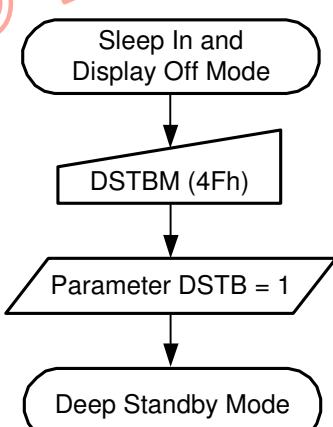
NOTE: “-“ Don’t care

Description	This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as VSYNC + VBP + VADR + VFP. The first scan line is defined as the first line of V Sync and is denoted as Line 0. When in Sleep mode, the returned value is undefined.									
Restriction	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>XXXXh</td> </tr> <tr> <td>S/W Reset</td> <td>XXXXh</td> </tr> <tr> <td>H/W Reset</td> <td>XXXXh</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	XXXXh	S/W Reset	XXXXh	H/W Reset	XXXXh
Status	Default Value									
Power On Sequence	XXXXh									
S/W Reset	XXXXh									
H/W Reset	XXXXh									
Flow Chart	<pre> graph TD A[GSL(45h)] --> B[/Send Parameter N[15:8]/] B --> C[/Send Parameter N[7:0]/] </pre> <p>The flowchart illustrates the sequence of operations. It starts with the command GSL(45h), followed by the transmission of parameter N[15:8], and finally the transmission of parameter N[7:0]. The entire process is labeled as Host Driver.</p>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

DSTBON: Deep Standby Mode On (4Fh)

Inst / Para	R/W	Address		Parameter								
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
DSTBON	Write	4Fh	4F00h	00h	-	-	-	-	-	-	-	DSTB

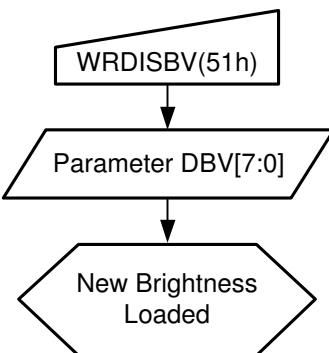
NOTE: “-“ Don't care

Description	This command is used to enter deep standby mode. DSTB=“1”, enter deep standby mode. Notes: 1. Before setting this command, enter Sleep In Mode (1000h) and Display Off (2800h) first. User can not write this register in Sleep-Out and Display-On mode. 2. It can not exit Deep Standby Mode while setting bit DSTB from “1” to “0”. 3. To exit Deep Standby Mode, input low pulse more than 3 msec to pin RESX.									
Restriction	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>DSTB = “0”</td> </tr> <tr> <td>S/W Reset</td> <td>DSTB = “0”</td> </tr> <tr> <td>H/W Reset</td> <td>DSTB = “0”</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	DSTB = “0”	S/W Reset	DSTB = “0”	H/W Reset	DSTB = “0”
Status	Default Value									
Power On Sequence	DSTB = “0”									
S/W Reset	DSTB = “0”									
H/W Reset	DSTB = “0”									
Flow Chart	 <pre> graph TD A([Sleep In and Display Off Mode]) --> B[/DSTBM (4Fh)/] B --> C[/Parameter DSTB = 1/] C --> D([Deep Standby Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 									

WRDISBV: Write Display Brightness (51h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRDISBV	Write	51h	5100h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0	

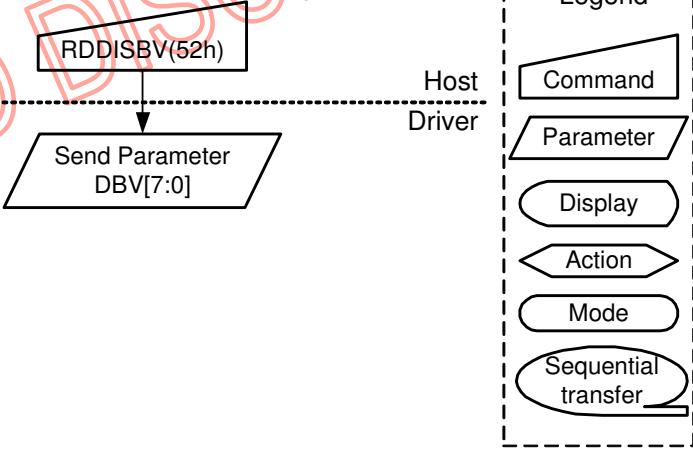
NOTE: “-“ Don't care

Description	This command is used to adjust brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.										
	DBV[7:0]	Brightness (Ratio)	Brightness (%)								
	00h	0/256	0%								
	01h	2/256	0.78125%								
	:	:	:								
	FEh	255/256	99.609375%								
	FFh	256/256	100%								
Restriction	The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability										
Normal Mode On, Idle Mode Off, Sleep Out	Yes										
Normal Mode On, Idle Mode On, Sleep Out	Yes										
Sleep In	Yes										
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>			Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value										
Power On Sequence	00h										
S/W Reset	00h										
H/W Reset	00h										
Flow Chart	 <pre> graph TD A[WRDISBV(51h)] --> B{Parameter DBV[7:0]} B --> C{New Brightness Loaded} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 										

RDDISBV: Read Display Brightness (52h)

Inst / Para	R/W	Address		Parameter								
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0
RDDISBV	Read	52h	5200h	00h	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

NOTE: “-“ Don't care

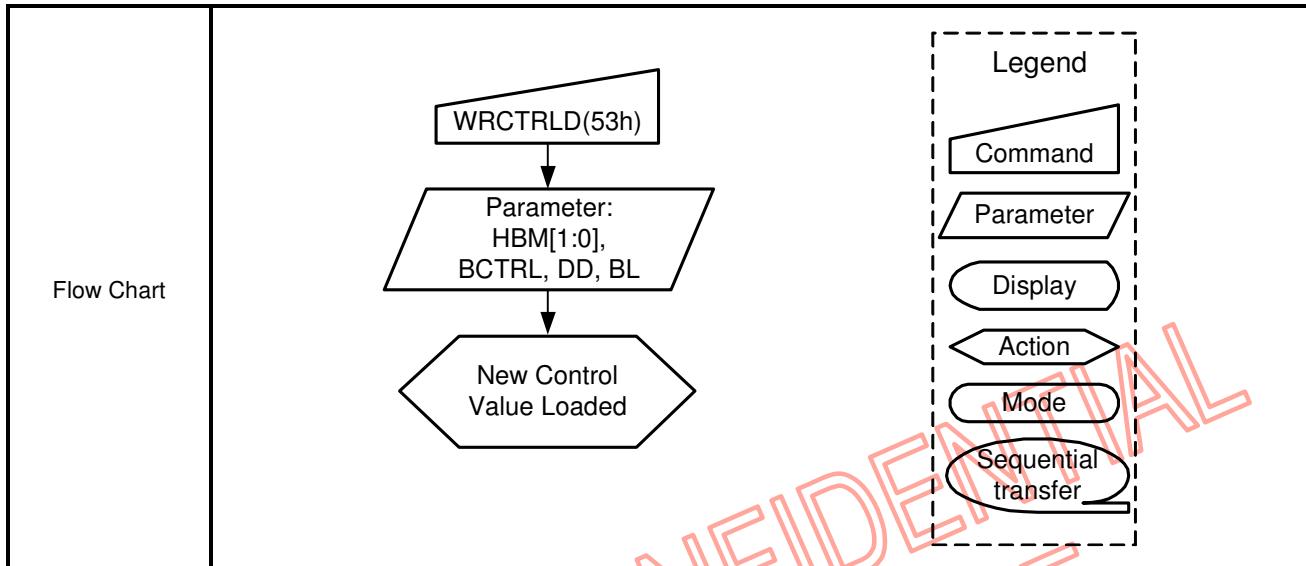
Description	This command returns brightness value. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.									
Restriction	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value									
Power On Sequence	00h									
S/W Reset	00h									
H/W Reset	00h									
Flow Chart	 <pre> graph TD RDDISBV["RDDISBV(52h)"] --> SendParam["Send Parameter DBV[7:0]"] subgraph HostDriver [Host Driver] SendParam end subgraph Legend [Legend] direction TB C[Command] --- P[Parameter] D[Display] --- A[Action] M[Mode] --- ST[Sequential transfer] end </pre>									

WRCTRLD: Write CTRL Display (53h)

Inst / Para	R/W	Address		Parameter								
		MiPI	Non-MiPI	D[15:8] (Non-MiPI)	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	Write	53h	5300h	00h	-	-	BCTRL	-	DD	BL	-	-

NOTE: “-“ Don't care

Description	<p>This command is used to control display brightness. BCTRL: Brightness Control Block On/Off The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).</p> <table border="1"> <thead> <tr> <th>BCTRL</th><th>DESCRIPTION</th><th>LEDPWM Pin</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off, DBV[7:0] are 00h.</td><td>LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)</td></tr> <tr> <td>1</td><td>On, DBV[7:0] are active</td><td>LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)</td></tr> </tbody> </table> <p>DD: Display Dimming Control On/Off</p> <table border="1"> <thead> <tr> <th>DD</th><th>DESCRIPTION</th></tr> </thead> <tbody> <tr> <td>0</td><td>Display dimming is off</td></tr> <tr> <td>1</td><td>Display dimming is on</td></tr> </tbody> </table> <p>BL: Backlight Control On/Off without Dimming Effect When BL bit change from “On” to “Off”, display brightness is turned off without gradual dimming, even if dimming on (DD=“1”) is selected.</p> <table border="1"> <thead> <tr> <th>BL</th><th>DESCRIPTION</th><th>LEDPWM Pin</th></tr> </thead> <tbody> <tr> <td>0</td><td>Off</td><td>LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)</td></tr> <tr> <td>1</td><td>On</td><td>LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)</td></tr> </tbody> </table> <p>The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=“1”, e.g. BCTRL: 0→1 or 1→0.</p> <p><i>Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.</i></p>	BCTRL	DESCRIPTION	LEDPWM Pin	0	Off, DBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)	1	On, DBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)	DD	DESCRIPTION	0	Display dimming is off	1	Display dimming is on	BL	DESCRIPTION	LEDPWM Pin	0	Off	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)	1	On	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)
BCTRL	DESCRIPTION	LEDPWM Pin																							
0	Off, DBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)																							
1	On, DBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)																							
DD	DESCRIPTION																								
0	Display dimming is off																								
1	Display dimming is on																								
BL	DESCRIPTION	LEDPWM Pin																							
0	Off	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)																							
1	On	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)																							
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h							
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h							
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h							
Status	Default Value																								
Power On Sequence	00h																								
S/W Reset	00h																								
H/W Reset	00h																								



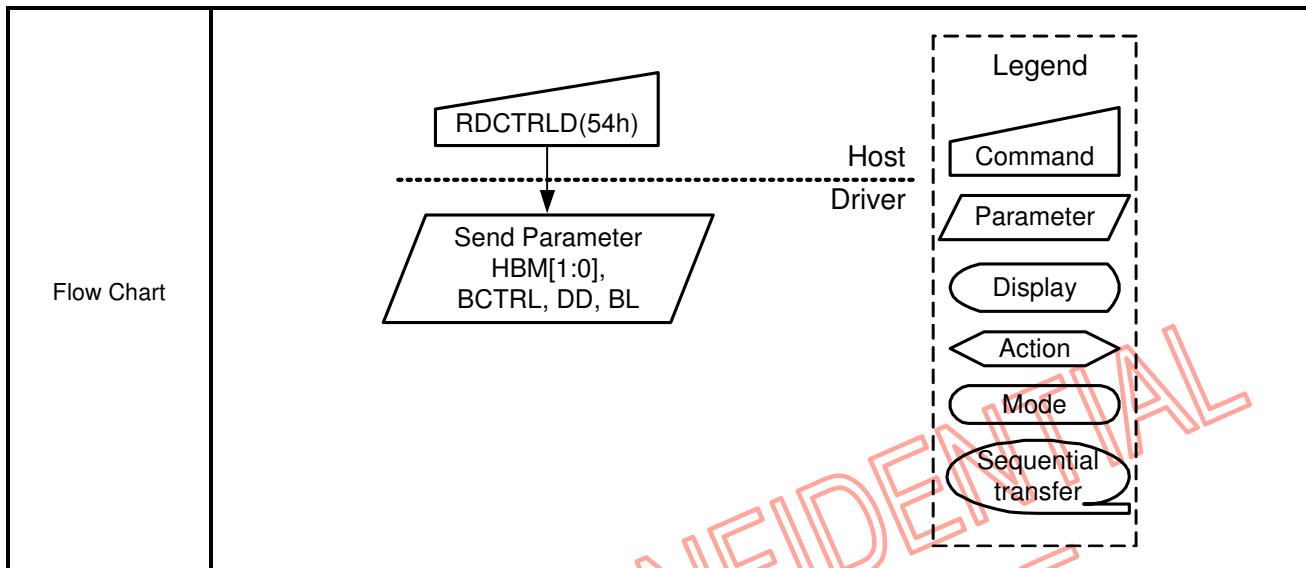
NOVATEK CONFIDENTIAL
NO DISCLOSURE

RDCTRLD: Read CTRL Display Value (54h)

Inst / Para	R/W	Address		Parameter								
		MiPi	Non-MiPi	D[15:8] (Non-MiPi)	D7	D6	D5	D4	D3	D2	D1	D0
RDCTRLD	Read	54h	5400h	00h			BCTRL		DD	BL		

NOTE: “-“ Don't care

Description	This command returns display brightness control. BCTRL: Brightness Control Block On/Off The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).										
	BCTRL	DESCRIPTION	LEDPWM Pin								
	0	Off, DBV[7:0] are 00h.	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)								
	1	On, DBV[7:0] are active	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)								
	DD: Display Dimming Control On/Off										
	DD	DESCRIPTION									
	0	Display dimming is off									
	1	Display dimming is on									
	BL: Backlight Control On/Off without Dimming Effect When BL bit change from “On” to “Off”, display brightness is turned off without gradual dimming, even if dimming on (DD=“1”) is selected.										
	BL	DESCRIPTION	LEDPWM Pin								
	0	Off	LEDPWPOL="0": keep low (0%, high level is duty) LEDPWPOL="1": keep high (0%, low level is duty)								
	1	On	LEDPWPOL="0": PWM output (high level is duty) LEDPWPOL="1": PWM output (low level is duty)								
The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=“1”, e.g. BCTRL: 0→1 or 1→0.											
Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.											
Restriction	-										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability										
Normal Mode On, Idle Mode Off, Sleep Out	Yes										
Normal Mode On, Idle Mode On, Sleep Out	Yes										
Sleep In	Yes										
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>			Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value										
Power On Sequence	00h										
S/W Reset	00h										
H/W Reset	00h										



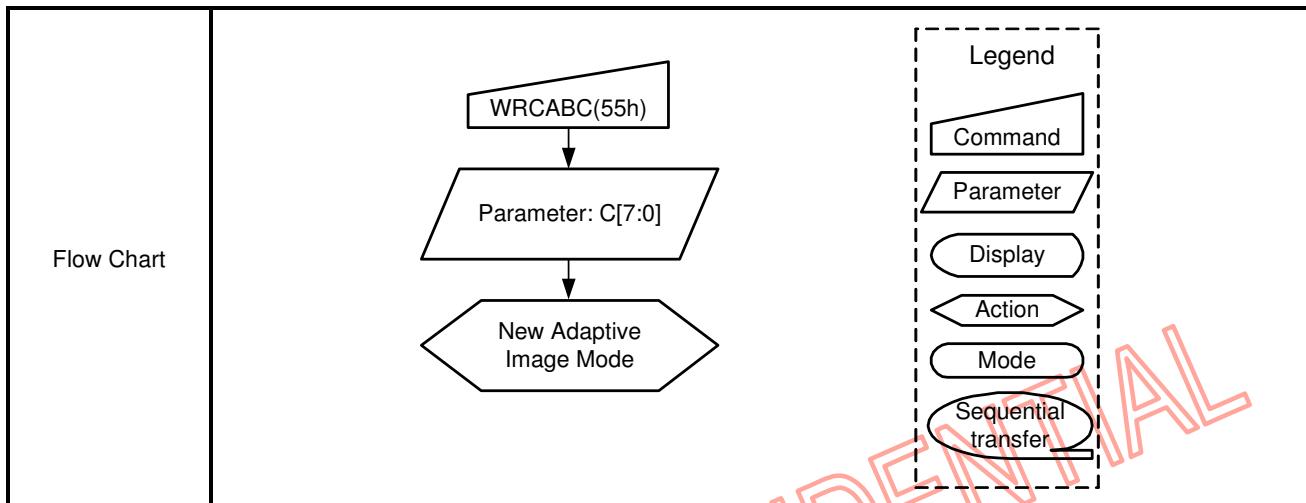
NOVATEK CONFIDENTIAL
NO DISCLOSURE

WRCABC: Write Content Adaptive Brightness Control (55h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRCABC	Write	55h	5500h	00h	C7	C6	C5	C4	C3	C2	C1	C0	

NOTE: “-“ Don't care

Description	This command is used to set parameters for image content based adaptive brightness control and image enhancement functionality. There is possible to use 4 different modes for content adaptive image functionality, 3 different modes for image enhancement functionality and 3 different modes for sunlight readability enhancement functionality, which are defined on a table below. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>C[7:0]</th><th>Function</th></tr> </thead> <tbody> <tr><td>00h</td><td>CABC Off</td></tr> <tr><td>01h</td><td>CABC User Interface Image (UI-Mode)</td></tr> <tr><td>02h</td><td>CABC Still Picture Image (Still-Mode)</td></tr> <tr><td>03h</td><td>CABC Moving Picture Image (Moving-Mode)</td></tr> <tr><td>4xh</td><td>SRE - Low Enhancement</td></tr> <tr><td>5xh</td><td>SRE - Medium Enhancement</td></tr> <tr><td>6xh</td><td>SRE - High Enhancement</td></tr> <tr><td>7xh</td><td>reserved</td></tr> <tr><td>8xh</td><td>IE - Low Enhancement</td></tr> <tr><td>9xh</td><td>IE - Medium Enhancement</td></tr> <tr><td>Bxh</td><td>IE - High Enhancement</td></tr> </tbody> </table> <p>Note: The setting values which not in above table are invalid.</p>													C[7:0]	Function	00h	CABC Off	01h	CABC User Interface Image (UI-Mode)	02h	CABC Still Picture Image (Still-Mode)	03h	CABC Moving Picture Image (Moving-Mode)	4xh	SRE - Low Enhancement	5xh	SRE - Medium Enhancement	6xh	SRE - High Enhancement	7xh	reserved	8xh	IE - Low Enhancement	9xh	IE - Medium Enhancement	Bxh	IE - High Enhancement
C[7:0]	Function																																				
00h	CABC Off																																				
01h	CABC User Interface Image (UI-Mode)																																				
02h	CABC Still Picture Image (Still-Mode)																																				
03h	CABC Moving Picture Image (Moving-Mode)																																				
4xh	SRE - Low Enhancement																																				
5xh	SRE - Medium Enhancement																																				
6xh	SRE - High Enhancement																																				
7xh	reserved																																				
8xh	IE - Low Enhancement																																				
9xh	IE - Medium Enhancement																																				
Bxh	IE - High Enhancement																																				
Restriction	This register is synchronized with V-sync by internal circuit.																																				
Register Availability	<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																	
Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																				
Sleep In	Yes																																				
<table border="1" style="width: 100%;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>00h</td></tr> <tr><td>S/W Reset</td><td>00h</td></tr> <tr><td>H/W Reset</td><td>00h</td></tr> </tbody> </table>												Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h																		
Status	Default Value																																				
Power On Sequence	00h																																				
S/W Reset	00h																																				
H/W Reset	00h																																				
												Default																									



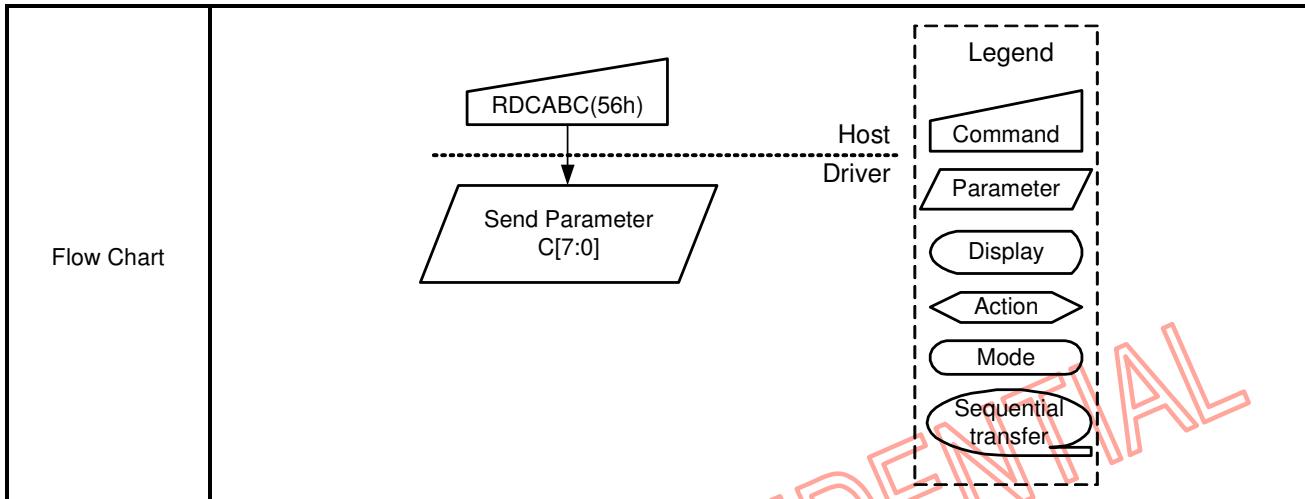
NOVATEK CONFIDENTIAL
NO DISCLOSURE

RDCABC: Read Content Adaptive Brightness Control (56h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDCABC	Read	56h	5600h	00h	C7	C6	C5	C4	C3	C2	C1	C0	

NOTE: “-“ Don't care

Description	This command is used to set parameters for image content based adaptive brightness control and image enhancement functionality. There is possible to use 4 different modes for content adaptive image functionality, 3 different modes for image enhancement functionality and 3 different modes for sunlight readability enhancement functionality, which are defined on a table below. <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>C[7:0]</th><th>Function</th></tr> </thead> <tbody> <tr><td>00h</td><td>CABC Off</td></tr> <tr><td>01h</td><td>CABC User Interface Image (UI-Mode)</td></tr> <tr><td>02h</td><td>CABC Still Picture Image (Still-Mode)</td></tr> <tr><td>03h</td><td>CABC Moving Picture Image (Moving-Mode)</td></tr> <tr><td>4xh</td><td>SRE - Low Enhancement</td></tr> <tr><td>5xh</td><td>SRE - Medium Enhancement</td></tr> <tr><td>6xh</td><td>SRE - High Enhancement</td></tr> <tr><td>7xh</td><td>reserved</td></tr> <tr><td>8xh</td><td>IE - Low Enhancement</td></tr> <tr><td>9xh</td><td>IE - Medium Enhancement</td></tr> <tr><td>Bxh</td><td>IE - High Enhancement</td></tr> </tbody> </table> <p>Note: The setting values which not in above table are invalid.</p>													C[7:0]	Function	00h	CABC Off	01h	CABC User Interface Image (UI-Mode)	02h	CABC Still Picture Image (Still-Mode)	03h	CABC Moving Picture Image (Moving-Mode)	4xh	SRE - Low Enhancement	5xh	SRE - Medium Enhancement	6xh	SRE - High Enhancement	7xh	reserved	8xh	IE - Low Enhancement	9xh	IE - Medium Enhancement	Bxh	IE - High Enhancement
C[7:0]	Function																																				
00h	CABC Off																																				
01h	CABC User Interface Image (UI-Mode)																																				
02h	CABC Still Picture Image (Still-Mode)																																				
03h	CABC Moving Picture Image (Moving-Mode)																																				
4xh	SRE - Low Enhancement																																				
5xh	SRE - Medium Enhancement																																				
6xh	SRE - High Enhancement																																				
7xh	reserved																																				
8xh	IE - Low Enhancement																																				
9xh	IE - Medium Enhancement																																				
Bxh	IE - High Enhancement																																				
Restriction	-																																				
Register Availability	<table border="1" style="margin-top: 10px;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																	
Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																				
Sleep In	Yes																																				
<table border="1" style="margin-top: 10px;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>00h</td></tr> <tr><td>S/W Reset</td><td>00h</td></tr> <tr><td>H/W Reset</td><td>00h</td></tr> </tbody> </table>												Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h																		
Status	Default Value																																				
Power On Sequence	00h																																				
S/W Reset	00h																																				
H/W Reset	00h																																				
												Default																									

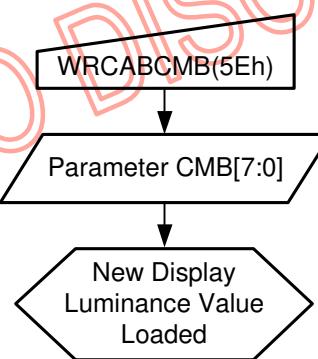


NOVATEK CONFIDENTIAL
NO DISCLOSURE

WRCABCMB: Write CABC minimum brightness (5Eh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
WRCABCMB	Write	5Eh	5E00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	

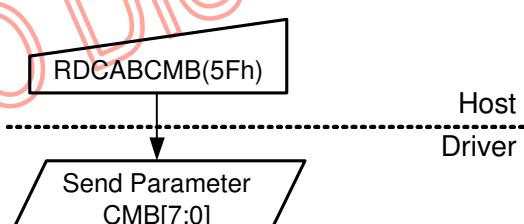
NOTE: “-“ Don't care

Description	This command is used to set the minimum brightness value of the display for CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.									
Restriction	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value									
Power On Sequence	00h									
S/W Reset	00h									
H/W Reset	00h									
Flow Chart	 <pre> graph TD A[WRCABCMB(5Eh)] --> B[Parameter CMB[7:0]] B --> C{New Display Luminance Value Loaded} </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

RDCABCMB: Read CABC minimum brightness (5Fh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDCABCMB	Read	5Fh	5F00h	00h	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	

NOTE: “-“ Don't care

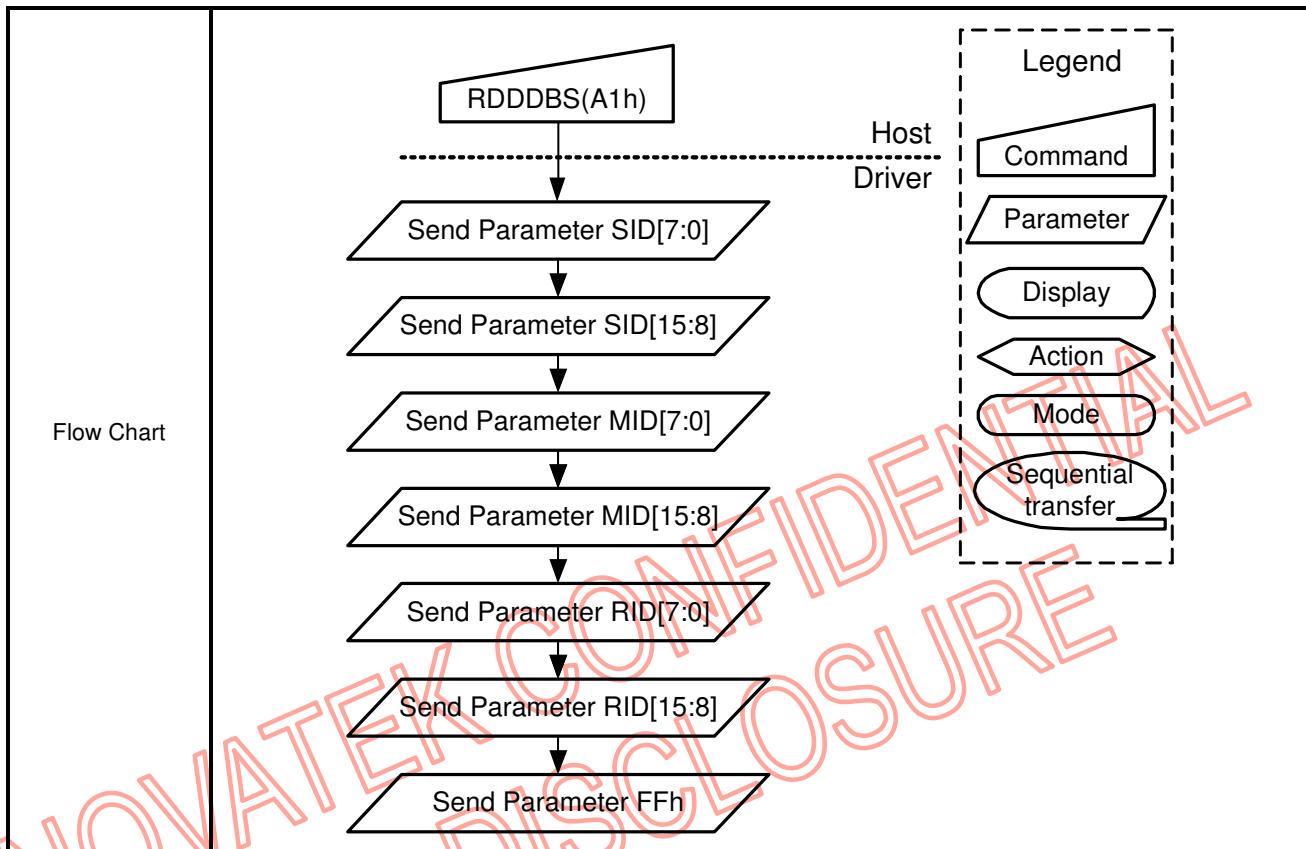
Description	This command return the minimum brightness value of CABC function In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. CMB[7:0] is the minimum brightness for CABC specified with “WRCABCMB Write CABC minimum brightness (5Eh)” command.									
Restriction	-									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability									
Normal Mode On, Idle Mode Off, Sleep Out	Yes									
Normal Mode On, Idle Mode On, Sleep Out	Yes									
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value									
Power On Sequence	00h									
S/W Reset	00h									
H/W Reset	00h									
Flow Chart	 <pre> graph TD A[RDCABCMB(5Fh)] --> B{Send Parameter CMB[7:0]} B --> C[Host Driver] </pre> <p>The flowchart illustrates the command sequence. It starts with the command RDCABCMB(5Fh), which triggers the action "Send Parameter CMB[7:0]". This action is then sent to the Host Driver.</p>	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

RDDDBS: Read DDB Start (A1h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDDBS	Read	A1h	A100h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	
			A101h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
			A102h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
			A103h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
			A104h	00h	RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0	
			A105h	00h	RID15	RID14	RID13	RID12	RID11	RID10	RID9	RID8	
			A106h	00h	1	1	1	1	1	1	1	1	

NOTE: “-” Don't care

Description	<p>This command returns the supplier identification and display module mode/revision information.</p> <p><i>Note: This information is not the same what “Read ID1 (DAh)”, “Read ID2 (DBh)” and “Read ID3 (DCh)” commands are returning.</i></p> <p><i>Note: Parameter 0xFF is an “Exit Code”, this means that there is no more data in the DDB block.</i></p> <p>This read sequence can be interrupted by any command and it can be continued by “Read DDB Continue (A8h)” command when the first parameter, what has been transferred, is the parameter, which has not been sent e.g. RDDDBS => 1st parameter has been sent => 2nd parameter has been sent=> interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.</p> <p>SID[7:0]: LS byte of Supplier ID SID[15:8]: MS byte of Supplier ID MID[7:0]: LS byte of Supplier Elective Data such as model number MID[15:8]: MS byte of Supplier Elective Data such as model number RID[7:0]: LS byte of Supplier Elective Data such as revision number RID[15:8]: MS byte of Supplier Elective Data such as revision number</p>															
Restriction	-															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>After MTP</th> <th>Before MTP</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>MTP Value</td> <td>All 00h</td> </tr> <tr> <td>S/W Reset</td> <td>MTP Value</td> <td>All 00h</td> </tr> <tr> <td>H/W Reset</td> <td>MTP Value</td> <td>All 00h</td> </tr> </tbody> </table>		Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP Value	All 00h	S/W Reset	MTP Value	All 00h	H/W Reset	MTP Value	All 00h
Status	Default Value															
	After MTP	Before MTP														
Power On Sequence	MTP Value	All 00h														
S/W Reset	MTP Value	All 00h														
H/W Reset	MTP Value	All 00h														

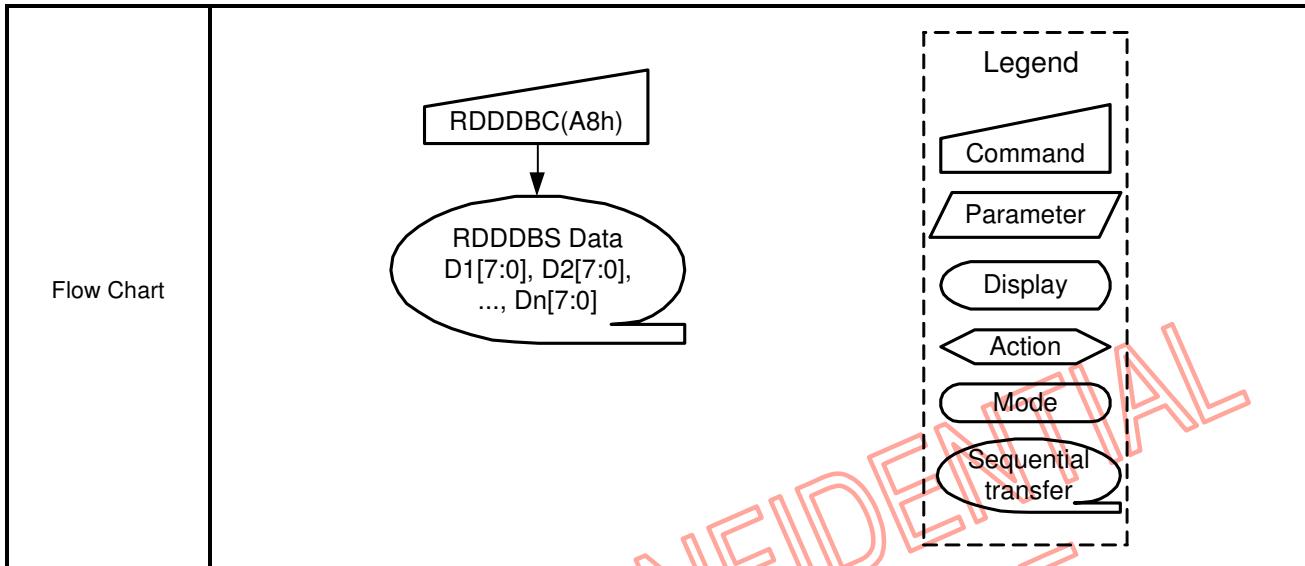


RDDDBC: Read DDB Continue (A8h)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDDDBC	Read	A8h	A800h	00h	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	
			A801h	00h	SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	
			A802h	00h	MID7	MID6	MID5	MID4	MID3	MID2	MID1	MID0	
			A803h	00h	MID15	MID14	MID13	MID12	MID11	MID10	MID9	MID8	
			A804h	00h	RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0	
			A805h	00h	RID15	RID14	RID13	RID12	RID11	RID10	RID9	RID8	
			A806h	00h	1	1	1	1	1	1	1	1	

NOTE: “-“ Don't care

Description	This command returns the supplier identification and display module mode/revision information from the point where RDDDBS command was interrupted by an other command. <i>Note: Parameter 0xFF is an “Exit Code”, this means that there is no more data in the DDB block.</i> <i>Note: For use example,</i> 1. Set maximum return packet size=3 2. Read 0xA1, return 3 bytes SID[7:0], SID[15:8], MID[7:0] 3. Read 0xA8, return 4 bytes MID[15:8], RID[7:0], RID[15:8] and 0xFF															
Restriction	A Read DDB Start command (RDDDBS) should be executed at least once before a Read DDB Continue command (RDDDBC) to define the read location. Otherwise, data read with a Read DDB Continue command is undefined.															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability															
Normal Mode On, Idle Mode Off, Sleep Out	Yes															
Normal Mode On, Idle Mode On, Sleep Out	Yes															
Sleep In	Yes															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>After MTP</th> <th>Before MTP</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>MTP Value</td> <td>All 00h</td> </tr> <tr> <td>S/W Reset</td> <td>MTP Value</td> <td>All 00h</td> </tr> <tr> <td>H/W Reset</td> <td>MTP Value</td> <td>All 00h</td> </tr> </tbody> </table>	Status	Default Value		After MTP	Before MTP	Power On Sequence	MTP Value	All 00h	S/W Reset	MTP Value	All 00h	H/W Reset	MTP Value	All 00h	
Status	Default Value															
	After MTP	Before MTP														
Power On Sequence	MTP Value	All 00h														
S/W Reset	MTP Value	All 00h														
H/W Reset	MTP Value	All 00h														



NOVATEK CONFIDENTIAL
NO DISCLOSURE

RDID1: Read ID1 Value (DAh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDID1	Read	DAh	DA00h	00h	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	

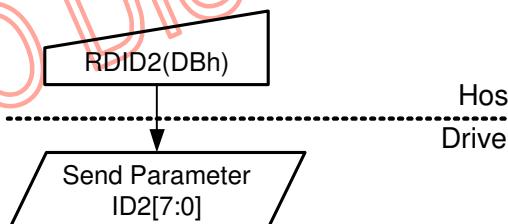
NOTE: “-“ Don't care

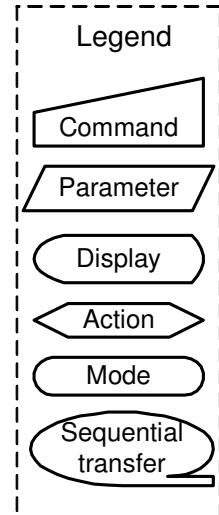
Description	This read byte identifies the TFT LCD module's manufacture ID.														
Restriction	-														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Sleep In</td> <td colspan="2">Yes</td> </tr> </tbody> </table>			Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Sleep In	Yes	
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>After MTP</td> <td>Before MTP</td> </tr> <tr> <td>S/W Reset</td> <td>MTP Value</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>MTP Value</td> <td>00h</td> </tr> </tbody> </table>			Status	Default Value		Power On Sequence	After MTP	Before MTP	S/W Reset	MTP Value	00h	H/W Reset	MTP Value	00h
Status	Default Value														
Power On Sequence	After MTP	Before MTP													
S/W Reset	MTP Value	00h													
H/W Reset	MTP Value	00h													
Flow Chart	<pre> graph TD RDID1["RDID1(DAh)"] --> SendParam["Send Parameter ID1[7:0]"] SendParam -.-> HostDriver["Host Driver"] </pre> <p>The flowchart illustrates the process of reading the ID1 value. It starts with the command RDID1(DAh), which is then used to send the parameter ID1[7:0]. This interaction occurs between the Host and the Driver.</p>														
	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 														

RDID2: Read ID2 Value (DBh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDID2	Read	DBh	DB00h	00h	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	

NOTE: “-“ Don't care

Description	This read byte is used to track the TFT LCD module/driver version. It is changed each time a version is made to the display, material or construction specifications. Parameter Range: ID2 = 80h to FFh														
Restriction	-														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Sleep In</td> <td colspan="2">Yes</td> </tr> </tbody> </table>			Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Sleep In	Yes	
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>After MTP</td> <td>Before MTP</td> </tr> <tr> <td>S/W Reset</td> <td>MTP Value</td> <td>80h</td> </tr> <tr> <td>H/W Reset</td> <td>MTP Value</td> <td>80h</td> </tr> </tbody> </table>			Status	Default Value		Power On Sequence	After MTP	Before MTP	S/W Reset	MTP Value	80h	H/W Reset	MTP Value	80h
Status	Default Value														
Power On Sequence	After MTP	Before MTP													
S/W Reset	MTP Value	80h													
H/W Reset	MTP Value	80h													
Flow Chart	 <pre> graph TD RDID2[RDID2(DBh)] --> SendParam[/Send Parameter ID2[7:0]/] SendParam --> HostDriver[Host Driver] </pre> <p>The flowchart illustrates the process of reading the ID2 value. It starts with the RDID2 command (DBh), which is then converted into a parameter (ID2[7:0]). This parameter is then sent from the Host to the Driver.</p>														



RDID3: Read ID3 Value (DCh)

Inst / Para	R/W	Address		Parameter									
		MIPI	Non-MIPI	D[15:8] (Non-MIPI)	D7	D6	D5	D4	D3	D2	D1	D0	
RDID3	Read	DCh	DC00h	00h	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	

NOTE: “-“ Don't care

Description	This parameter read byte identifies the TFT LCD module/driver.														
Restriction	-														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td colspan="2">Yes</td> </tr> <tr> <td>Sleep In</td> <td colspan="2">Yes</td> </tr> </tbody> </table>			Status	Availability		Normal Mode On, Idle Mode Off, Sleep Out	Yes		Normal Mode On, Idle Mode On, Sleep Out	Yes		Sleep In	Yes	
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th colspan="2">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>After MTP</td> <td>Before MTP</td> </tr> <tr> <td>S/W Reset</td> <td>MTP Value</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>MTP Value</td> <td>00h</td> </tr> </tbody> </table>			Status	Default Value		Power On Sequence	After MTP	Before MTP	S/W Reset	MTP Value	00h	H/W Reset	MTP Value	00h
Status	Default Value														
Power On Sequence	After MTP	Before MTP													
S/W Reset	MTP Value	00h													
H/W Reset	MTP Value	00h													
Flow Chart	<pre> graph TD RDID3[DID3(DCh)] --> SendParam[Send Parameter ID3[7:0]] subgraph Legend [Legend] Command[/\] Parameter[Parameter] Display[Display] Action[Action] Mode[Mode] Sequential[Sequential transfer] end </pre> <p>The flowchart illustrates the communication between the Host and the Driver. The Host sends a command (RDID3(DCh)) to the Driver, which then responds with a parameter (ID3[7:0]). A legend on the right defines the symbols: Command (triangular box), Parameter (rectangle), Display (oval), Action (diamond), Mode (trapezoid), and Sequential transfer (horizontal bar).</p>														

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage (Logic)	VDDI	-0.3 ~ +5.5	V
Supply voltage	VCI	-0.3 ~ +5.5	V
Supply voltage (MV)	AVDD	-0.3 ~ +6.6	V
	AVEE	+0.3 ~ -6.6	V
Supply voltage (HV)	VGH	-0.3 ~ +22	V
	VGLX	+0.3 ~ -18	
	VGH-VGLX	-0.3 ~ +33	
Logic Input voltage range	VIN	-0.3 ~ VDDI + 0.3	V
Logic Output voltage range	VO	-0.3 ~ VDDI + 0.3	V
Differential Input Voltage	HSSI_CLK_P/N HSSI_DATA0_P/N HSSI_DATA1_P/N HSSI_DATA2_P/N HSSI_DATA3_P/N	-0.3 ~ +1.8	V
Operating temperature range	TOPR	-40 ~ +85	°C
Storage Temperature range	TSTG	-55 ~ +125	°C

Note:

1. If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.
2. VCI means VDDA, VDDR and VDBB when BTM[2:0] = "000" or "001".
VCI means VDDA and AVDD means AVDD, VDDR and VDBB when BTM[2:0] = "010", "011", "100", "101" or "110".

7.2 DC Characteristics

7.2.1 Basic Characteristics

Parameter	Symbol	Conditions	Specification			Unit	Related Pins
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Operating voltage	VDD	Operating Voltage	2.5	3.3	3.6	V	Note 1, 2
Logic Operating voltage	VDDI	I/O supply voltage	1.65	1.8	3.6	V	Note 1, 2
Input / Output							
Logic High level input voltage	VIH	VDDI=1.65~3.6	0.7 VDDI	-	VDDI	V	Note 1, 2, 3
Logic Low level input voltage	VIL		VSSI	-	0.3 VDDI	V	Note 1, 2, 3
Logic High level output voltage	VOH	VDDI=1.65~3.6 IOH = -1.0mA	0.8 VDDI	-	VDDI	V	Note 1, 2, 5
Logic Low level output voltage	VOL		VSSI	-	0.2 VDDI	V	Note 1, 2, 5
Logic High level leakage (Except MIPI)	ILIH	Vin=0~VDDI	-	-	1	µA	Note 1, 2, 3
Logic Low level leakage (Except MIPI)	ILIL	Vin=0~VDDI	-1	-	-	µA	Note 1, 2, 3
Logic High level leakage (MIPI)	ILIH	Vin=0~VDDA	-	-	1	µA	Note 2, 8
Logic Low level leakage (MIPI)	ILIL	Vin=0~VDDA	-1	-	-	µA	Note 2, 8
DC/DC Converter Operation							
AVDD booster voltage	AVDD	-	4.5	-	6.3	V	Note 2, 7
AVEE booster voltage	AVEE	-	-6.3	-	-4.5	V	Note 2, 7
VCL booster voltage	VCL	-	-2.5	-	-4.0	V	Note 2, 7
VGH booster voltage	VGH	-	AVDD -VCL	-	2AVDD -2AVEE	V	Note 2, 6
VGLX booster voltage	VGLX	-	AVEE +VCL	-	2AVEE -AVDD	V	Note 2, 6
Voltage difference between VGH and VGLX	VGHL	VGH-VGLX	-	-	30	V	Note 2
Oscillator tolerance	ΔOSC	25 °C	-5	-	5	%	
Source Driver							
Gamma reference voltage	VGMP	-	3.0	-	6.0	V	Note 2
	VGSP	-	0.0	-	3.3	V	Note 2
	VGMN	-	-6.0	-	-3.0	V	Note 2
	VGSN	-	-3.3	-	0.0	V	Note 2
Output offset voltage	VOFSET	-	-	-	45	mV	Note 4
Output deviation voltage	Vdev	VGMP-0.2V≥Sout≥4.0V (0.2-VGMN≥Sout≥4.0V) 0.2V≤Sout≤1.0V	-	20	30	mV	Note 4 Fig.7.2.2
		1.0V<Sout<4.0V	-	10	15	mV	

Note 1) $VDDI=1.65$ to $3.6V$, $VDD=2.5$ to $3.6V$, $VSSI=VSS=DVSS=0V$, $Ta=-30$ to $70\text{ }^{\circ}\text{C}$ (to $+85\text{ }^{\circ}\text{C}$ no damage)

VDD means $VDDA$, $VDDR$, $VDBB$ and VSS means $VSSA$, $VSSR$, $VSSB$, $AVSS$, $VSSAM$.

$VDBB$, $VDDA$ and $VDDR$ should be the same input voltage level and larger than $VDDI$ voltage.

Note 2) When the measurements are performed with module, measurement points are like below.

Note 3) $DSWAP[1:0]$, $PSWAP$, $LANSEL[1:0]$, $IM[1:0]$, $VGSW[3:0]$, CSX , D/CX , SCL , SDI pins.

Note 4) Channel loading = 40pF / channel, $Ta=25\text{ }^{\circ}\text{C}$.

Note 5) SDO , EN_PWR , $HSOUT$, TE , $TE1$, $LEDPWM$ pins

Note 6) $VDBB=3.3V$, $Ta=25\text{ }^{\circ}\text{C}$, no load on panel and $Iload=2mA$, $|Output\text{ Voltage} - Target\text{ Voltage}| < 100mV$.

Note 7) $VDBB=3.3V$, $Ta=25\text{ }^{\circ}\text{C}$, no load on panel and $Iload=TBDmA$, power pad serial resistor is smaller than maximum value.

Note 8) $Vin = 0$ to $VDDA$, $VDD=2.5$ to $3.6V$, $VDDI=1.65$ to $3.6V$, $VSSAM=VSS=0V$, $Ta=-30$ to $70\text{ }^{\circ}\text{C}$ (to $+85\text{ }^{\circ}\text{C}$ no damage).

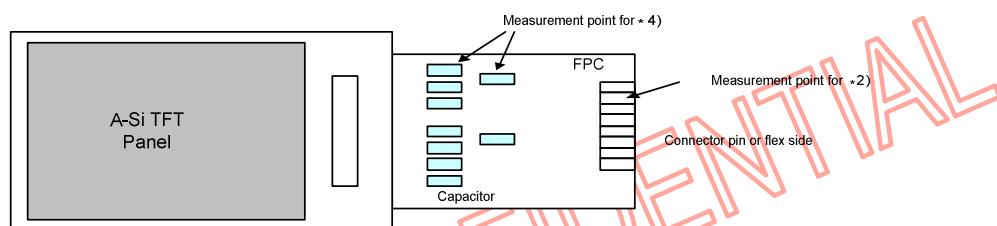


Fig. 7.2.1 Measurement Points for All Characteristics.

-When $4.0 \leq Sout \leq VGMP-0.2V$ ($4.0 \leq Sout \leq 0.2V-VGMN$), $0.2V \leq Sout \leq 1.0V$

$$|(S1, S2, S3, \dots, S2400) - Average(S1, S2, S3, \dots, S2400)| \leq 30mV$$

-When $1.0V < Sout < 4.0V$

$$|(S1, S2, S3, \dots, S2400) - Average(S1, S2, S3, \dots, S2400)| \leq 15mV$$

- $Sout=V0 \sim V255$

$$|S_{Target} - Average(S1, S2, S3, \dots, S2400)| \leq 45mV$$

7.2.2 MIPI Characteristics

7.2.2.1 DC Characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-CD, LP-RX	-	-	10	μ A
Logic low level input current	I_{IL}	LP-CD, LP-RX	-10	-	-	μ A
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) $VDD=1.65\sim3.6V$, $VDD=2.5$ to $3.6V$, $VSS=VSSAM=0V$, $T_a=-30$ to $70^{\circ}C$ (to $+85^{\circ}C$ no damage). VDD means $VDDA$, $VDDR$, $VDBB$ and VSS means $VSSAM$, $VSSA$, $VSSR$, $VSSB$, $AVSS$.

Note 2) DSI high speed is off.

Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

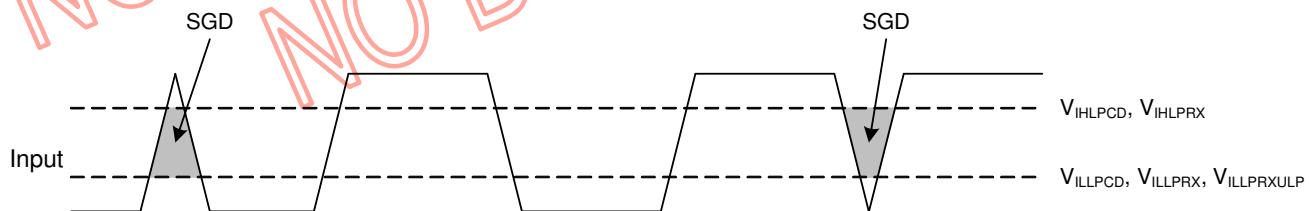


Fig. 7.2.2 Spike/Glitch rejection-DSI

7.2.2.2 DC Characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450 MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450 MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERM_EN}	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) $VDDI=1.65\sim3.6V$, $VDD=2.5$ to $3.6V$, $VSSI=VSS=VSSAM=0V$, $T_a=-30$ to $70^{\circ}C$ (to $+85^{\circ}C$ no damage). VDD means $VDDA$, $VDDR$, $VDBB$ and VSS means $VSSAM$, $VSSA$, $VSSR$, $VSSB$, $AVSS$.

Note 2) Includes 50mV (-50mV to 50mV) ground difference.

Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$.

Note 4) Without 50mV (-50mV to 50mV) ground difference.

Note 5) $Dn=D0$, $D1$, $D2$ and $D3$.

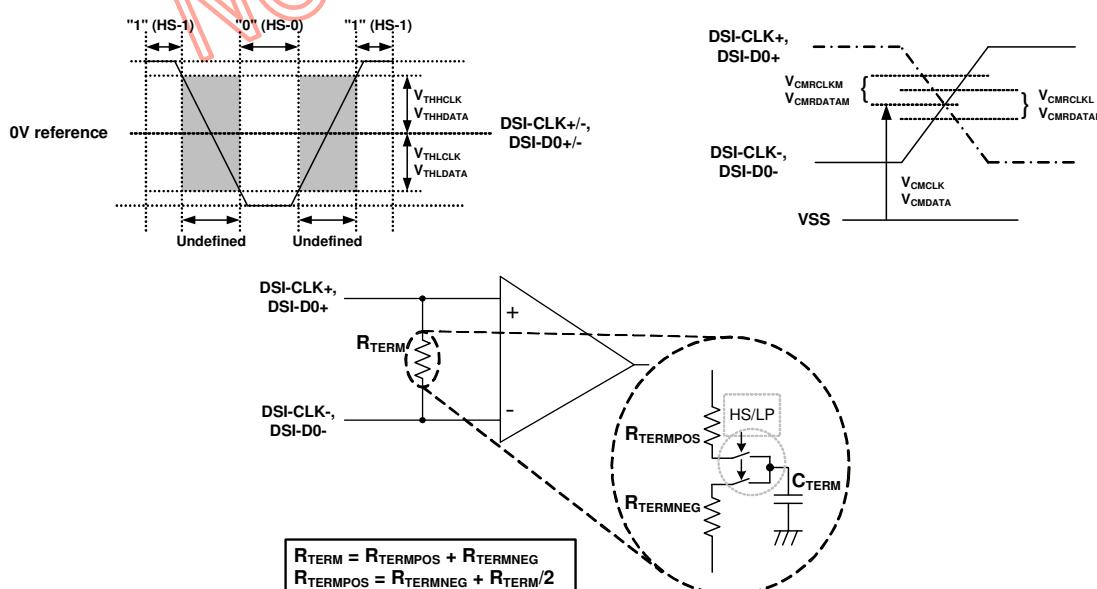


Fig. 7.2.3 Differential voltage range, termination resistor and Common mode voltage

7.3 AC Characteristics

7.3.1 MIPI DSI Timing Characteristics

7.3.1.1 High Speed Mode

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	2xUIINST	Double UI instantaneous	4	-	8	ns	4 Lane (Note 2)
			3	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UIINSTA UIINSTB	UI instantaneous halfs (UI = UIINSTA = UIINSTB)	2	-	4	ns	4 Lane (Note 2)
			1.5	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	t _{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t _{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t _{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	t _{DRTDATA}	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t _{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	t _{DFTDATA}	Differential fall time for data	150	-	0.3xUI	ps	

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2Gbps for 24-bit data format, 1.5Gbps for 18-bit data format and 1.33Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.

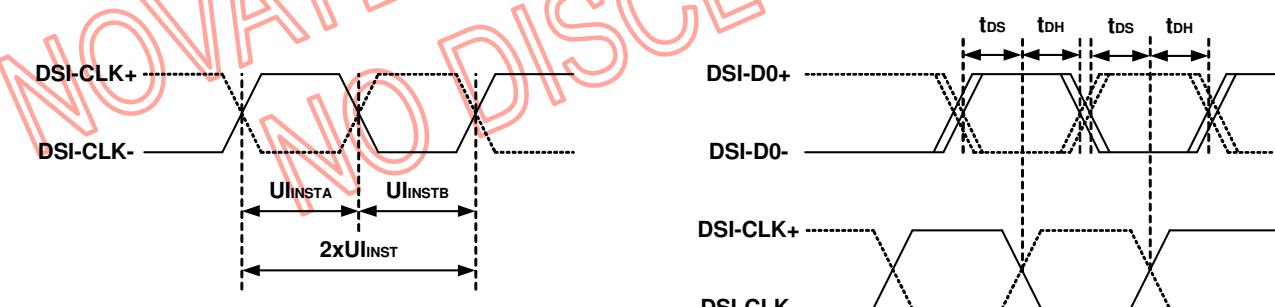


Fig. 7.3.1 DSI clock channel timing

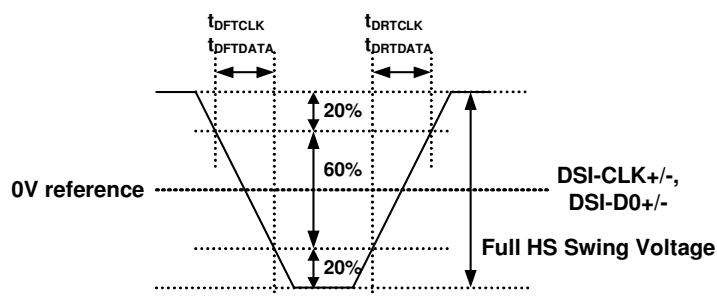


Fig. 7.3.2 Rising and fall time on clock and data channel

7.3.1.2 Low Power Mode

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2 \times T_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5 \times T_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4 \times T_{LPXD}$	-	-	ns	Output

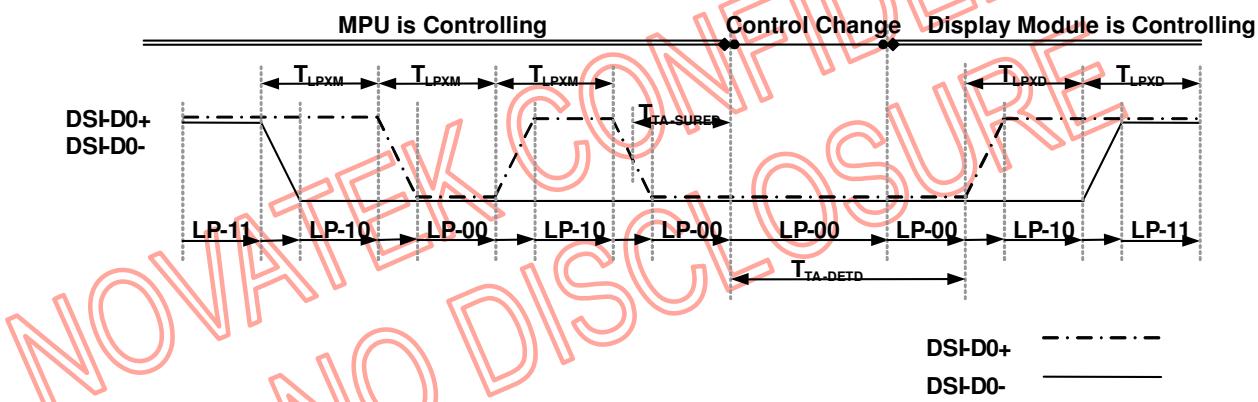


Fig. 7.3.3 Bus Turnaround (BAT) from MPU to display module Timing

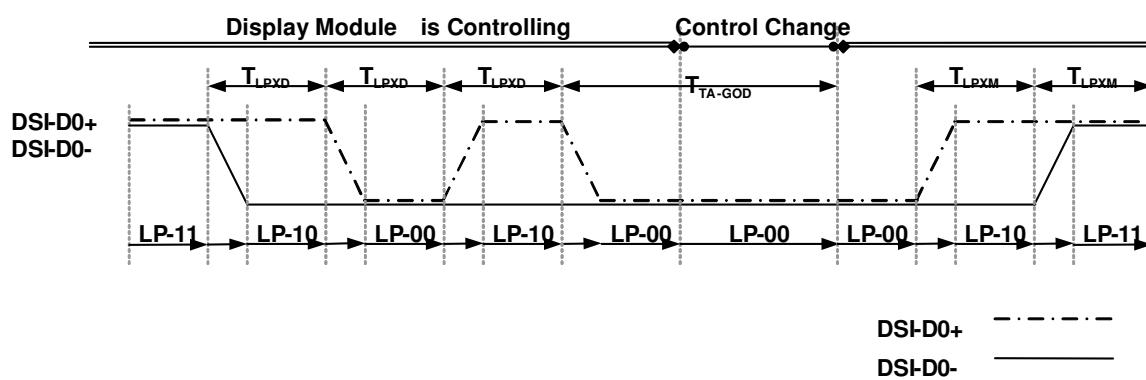


Fig. 7.3.4 Bus Turnaround (BAT) from display module to MPU Timing

7.3.1.3 DSI Bursts

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T _{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	T _{HS-TERM-EN}	Time to enable data receiver line termination measured from when Dn crosses V _{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	T _{HS-SKIP}	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	T _{HS-TRAIL}	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	T _{CLK-POS}	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	T _{CLK-TERM-EN}	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	T _{CLK-PREPARE + T_{CLK-ZERO}}	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as T_{HS-EXIT} from each other in continuous clock mode. In discontinuous mode, the break is longer which account T_{CLK-POS}, T_{CLK-TRAIL} and T_{HS-EXIT}, before activity in clock and data lanes again.

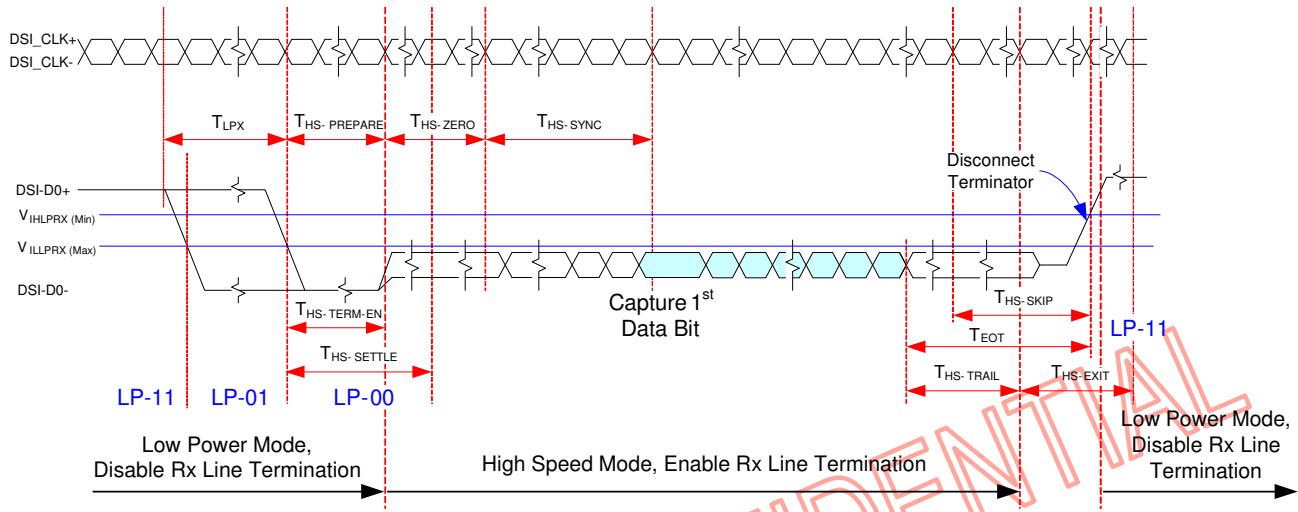


Fig. 7.3.5 Data lanes-Low Power Mode to/from High Speed Mode Timing

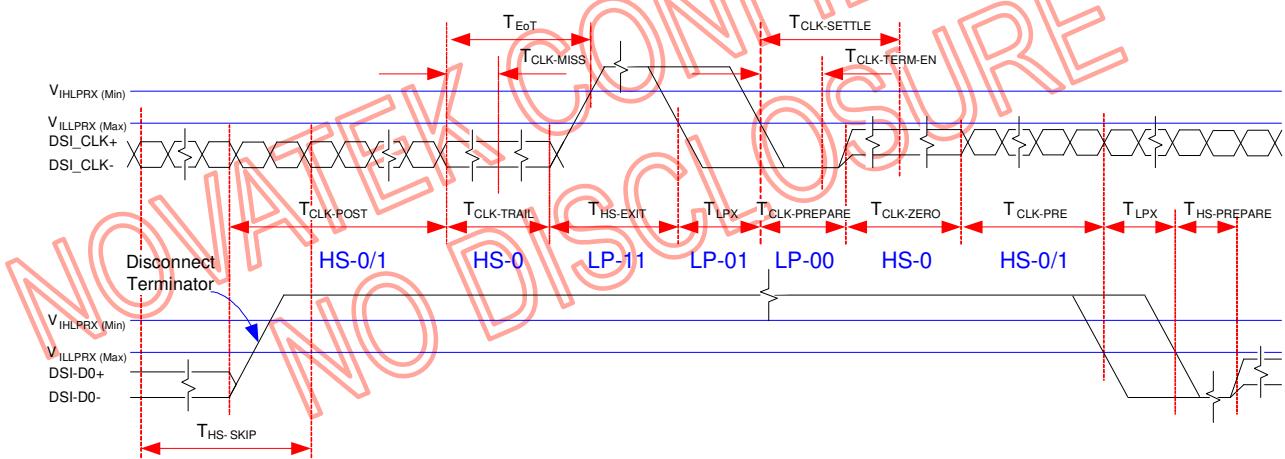


Fig. 7.3.6 Clock lanes- High Speed Mode to/from Low Power Mode Timing

7.3.2 Reset Input Timing

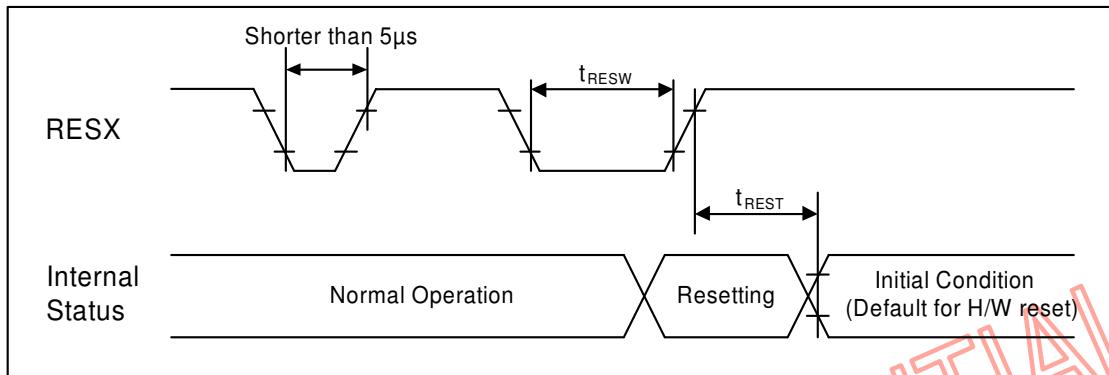


Fig. 7.3.7 Reset input timing

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	μs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

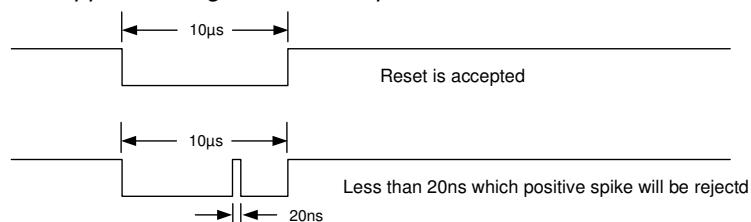
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5μs	Reset Rejected
Longer than 10μs	Reset
Between 5μs and 10μs	Reset Start

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In-mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

7.3.3 Deep Standby Mode Timing

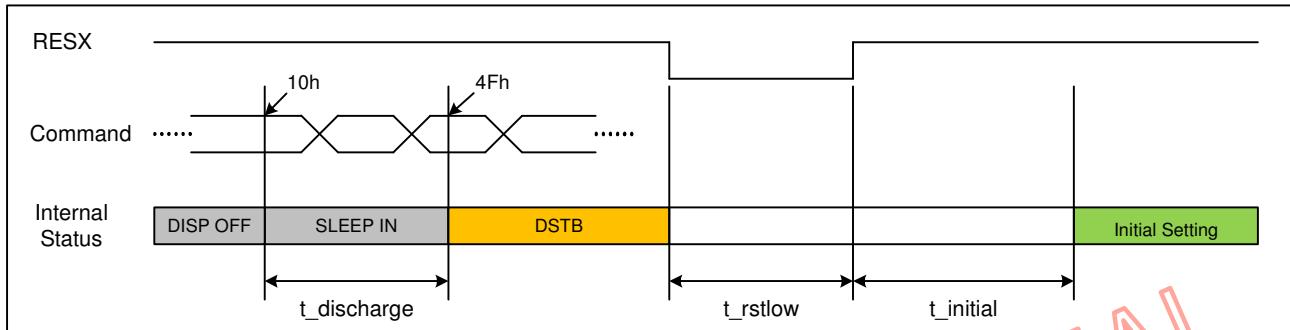


Fig. 7.3.8 Deep standby timing

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V, Ta = -30 to 70 °C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_discharge	Sleep in into DSTB delay time	-	-	100	ms	
	t_rstlow	Reset low pulse	3	-	-	ms	
	t_initial	Reset high to initial setting delay time	-	-	120	ms	

Note 1) $t_{\text{discharge}}$ suggested delay time over 100ms.

Note 2) t_{initial} suggested delay time over 120ms..

8 REFERENCE APPLICATIONS

8.1 Microprocessor Interface

The display, which is using MIPI DSI, is connected to the MPU as it is illustrated below.

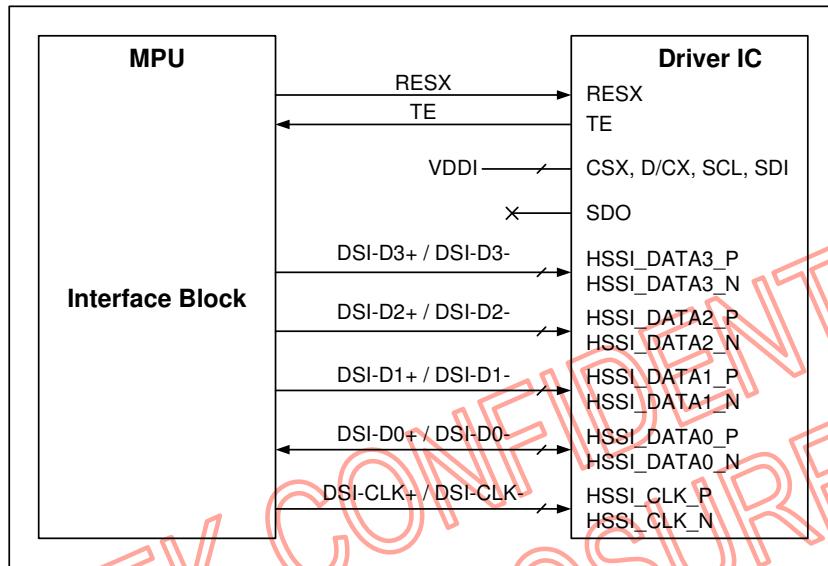


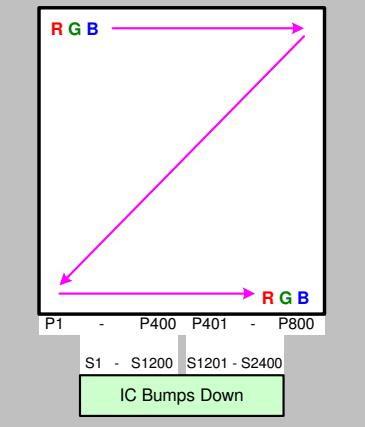
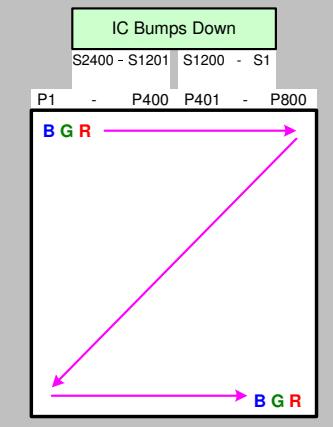
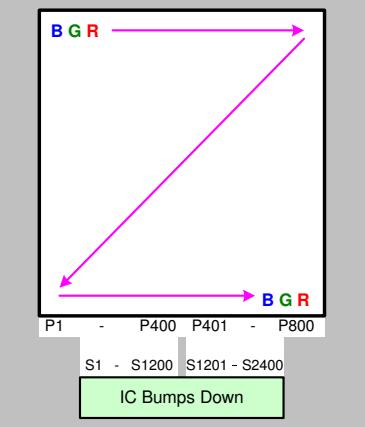
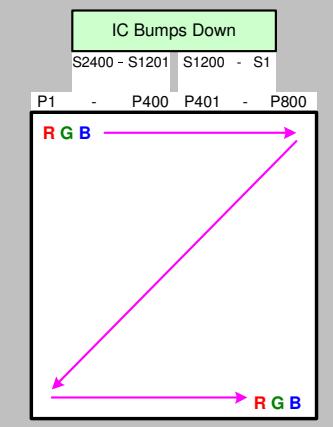
Fig. 8.1.1 Interfacing for MIPI by Connecting IM[1:0] = "11"

Notes:

1. When TE is not in use, please let it open.
2. Connect HSSI_DATA3_P/N to VSSAM in 3 data lanes application (LANSEL[1:0] = "10").
3. Connect HSSI_DATA3_P/N and HSSI_DATA2_P/N to VSSAM in 2 data lanes application (LANSEL[1:0] = "01").

8.2 Connections with Panel

8.2.1 Connection for Panel with Column/Dot Inversion

 <p>CRL = 0 CRGB = 0</p>	 <p>CRL = 1 CRGB = 0</p>
 <p>CRL = 0 CRGB = 1</p>	 <p>CRL = 1 CRGB = 1</p>
IC on Bottom Side of Module	IC on Top Side of Module

The relationship between Sn output sequence and CRL/CRGB is shown below.

CGM	Display Resolution	CRL	CRGB	Sn Output Sequence	Note
000	800RGB	0	0	S1 _(R) → S2 _(G) → S3 _(B) → ... → S2398 _(R) → S2399 _(G) → S2400 _(B)	All S1 to S2400 are used
		0	1	S1 _(B) → S2 _(G) → S3 _(R) → ... → S2398 _(B) → S2399 _(G) → S2400 _(R)	
		1	0	S2400 _(B) → S2399 _(G) → S2398 _(R) → ... → S3 _(B) → S2 _(G) → S1 _(R)	
		1	1	S2400 _(R) → S2399 _(G) → S2398 _(B) → ... → S3 _(R) → S2 _(G) → S1 _(B)	
001	768RGB	0	0	S1 _(R) → S2 _(G) → S3 _(B) → ... → S1152 _(B) → S1249 _(R) → ... → S2398 _(R) → S2399 _(G) → S2400 _(B)	S1~S1152 and S1249~S2400 are used
		0	1	S1 _(B) → S2 _(G) → S3 _(R) → ... → S1152 _(R) → S1249 _(B) → ... → S2398 _(B) → S2399 _(G) → S2400 _(R)	
		1	0	S2400 _(B) → S2399 _(G) → S2398 _(R) → ... → S1249 _(R) → S1152 _(B) → ... → S3 _(B) → S2 _(G) → S1 _(R)	
		1	1	S2400 _(R) → S2399 _(G) → S2398 _(B) → ... → S1249 _(B) → S1152 _(R) → ... → S3 _(R) → S2 _(G) → S1 _(B)	
010	720RGB	0	0	S1 _(R) → S2 _(G) → S3 _(B) → ... → S1080 _(B) → S1321 _(R) → ... → S2398 _(R) → S2399 _(G) → S2400 _(B)	S1~S1080 and S1321~S2400 are used
		0	1	S1 _(B) → S2 _(G) → S3 _(R) → ... → S1080 _(R) → S1321 _(B) → ... → S2398 _(B) → S2399 _(G) → S2400 _(R)	
		1	0	S2400 _(B) → S2399 _(G) → S2398 _(R) → ... → S1321 _(R) → S1080 _(B) → ... → S3 _(B) → S2 _(G) → S1 _(R)	
		1	1	S2400 _(R) → S2399 _(G) → S2398 _(B) → ... → S1321 _(B) → S1080 _(R) → ... → S3 _(R) → S2 _(G) → S1 _(B)	
011	640RGB	0	0	S1 _(R) → S2 _(G) → S3 _(B) → ... → S960 _(B) → S1441 _(R) → ... → S2398 _(R) → S2399 _(G) → S2400 _(B)	S1~S960 and S1441~S2400 are used
		0	1	S1 _(B) → S2 _(G) → S3 _(R) → ... → S960 _(R) → S1441 _(B) → ... → S2398 _(B) → S2399 _(G) → S2400 _(R)	
		1	0	S2400 _(B) → S2399 _(G) → S2398 _(R) → ... → S1441 _(R) → S960 _(B) → ... → S3 _(B) → S2 _(G) → S1 _(R)	
		1	1	S2400 _(R) → S2399 _(G) → S2398 _(B) → ... → S1441 _(B) → S960 _(R) → ... → S3 _(R) → S2 _(G) → S1 _(B)	
100	600RGB	0	0	S1 _(R) → S2 _(G) → S3 _(B) → ... → S900 _(B) → S1501 _(R) → ... → S2398 _(R) → S2399 _(G) → S2400 _(B)	S1~S900 and S1501~S2400 are used
		0	1	S1 _(B) → S2 _(G) → S3 _(R) → ... → S900 _(R) → S1501 _(B) → ... → S2398 _(B) → S2399 _(G) → S2400 _(R)	
		1	0	S2400 _(B) → S2399 _(G) → S2398 _(R) → ... → S1501 _(R) → S900 _(B) → ... → S3 _(B) → S2 _(G) → S1 _(R)	
		1	1	S2400 _(R) → S2399 _(G) → S2398 _(B) → ... → S1501 _(B) → S900 _(R) → ... → S3 _(R) → S2 _(G) → S1 _(B)	
101	540RGB	0	0	S1 _(R) → S2 _(G) → S3 _(B) → ... → S810 _(B) → S1591 _(R) → ... → S2398 _(R) → S2399 _(G) → S2400 _(B)	S1~S810 and S1591~S2400 are used
		0	1	S1 _(B) → S2 _(G) → S3 _(R) → ... → S810 _(R) → S1591 _(B) → ... → S2398 _(B) → S2399 _(G) → S2400 _(R)	
		1	0	S2400 _(B) → S2399 _(G) → S2398 _(R) → ... → S1591 _(R) → S810 _(B) → ... → S3 _(B) → S2 _(G) → S1 _(R)	
		1	1	S2400 _(R) → S2399 _(G) → S2398 _(B) → ... → S1591 _(B) → S810 _(R) → ... → S3 _(R) → S2 _(G) → S1 _(B)	