

EEE205 – Digital Electronics (II)

Lectures 1-2

Dr. Ming Xu

Dept of Electrical & Electronic Engineering

XJTLU

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This Module

Textbooks:

1. A. Marcovitz, *Introduction to Logic Design*, McGraw Hill, 2005.
2. R. Tocci, N. Widmer and G. Moss, *Digital Systems: Principles and Applications*, Pearson Education, 2007.
3. T. Floyd, *Digital Fundamentals*, Pearson Education, 2000.

Assessment:

Final exam (70%), Mid-Term Class Test (10%),
Lab (10%), Assignments (10%)

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This Module

Contents:

1. Programmable Logics Devices (PLDs)
2. Hardware Design Languages (HDLs)
3. Large Combinational and Sequential Circuits
4. Algorithmic State Machines (ASMs)
5. Processor Interface Circuits

Office Hours:

1-3 pm on every Tuesday and Thursday

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In This Session

- Introduction to Programmable Logic Devices (PLDs)
- Programmable Array Logic (PAL)
- Generic Array Logic (GAL)

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Programmable Logic Devices (PLDs)

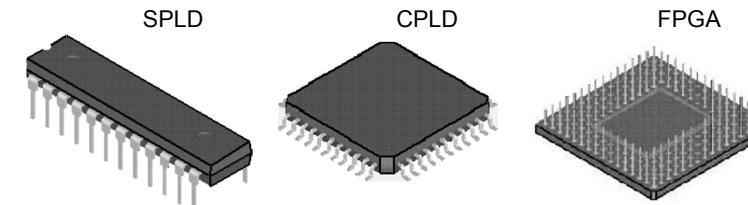
- PLDs can be used to implement combinational and sequential logic circuits.
- They can replace logic devices, resulting in fewer parts, lower cost and less space.
- The logic design in PLDs are implemented with programming software.

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Programmable Logic Devices (PLDs)

Types (*equivalent gates*: 2-input NAND gates)

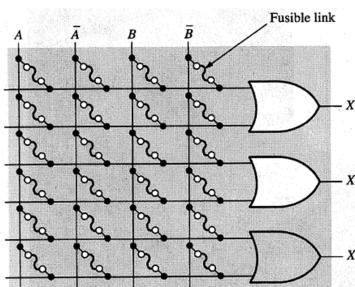
- SPLDs — Simple Programmable Logic Devices, up to 600 *equivalent gates* each.
- CPLDs — Complex Programmable Logic Devices, up to thousands of *equivalent gates* each.
- FPGAs — Field Programmable Gate Arrays, hundreds of thousands of *equivalent gates* each.



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Programmable Arrays

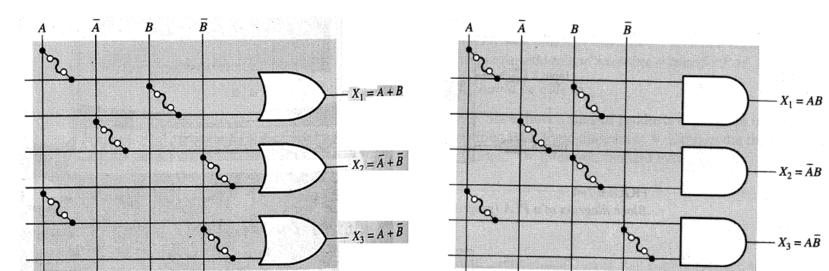
- All SPLDs consist of programmable arrays.
- A *programmable array* is a grid of conductors that form rows and columns with a fusible link at each cross point.



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Programmable Arrays

- The array is programmed by blowing fuses to eliminate selected variables from the output.
- An array can be fixed, one-time programmable or re-programmable.

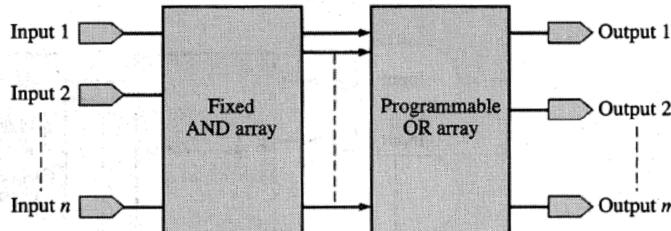


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Classifications of SPLDs

1. Programmable Read-Only Memory (PROM)

It consists of a fixed AND array and a programmable OR array.

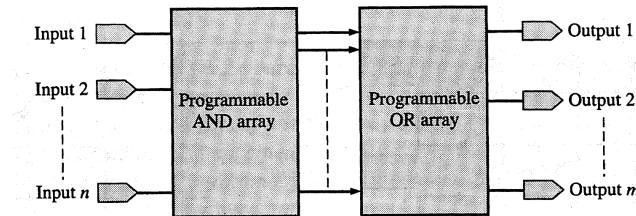


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Classifications of SPLDs

2. Programmable Logic Array (PLA)

It consists of a programmable AND array and a programmable OR array.

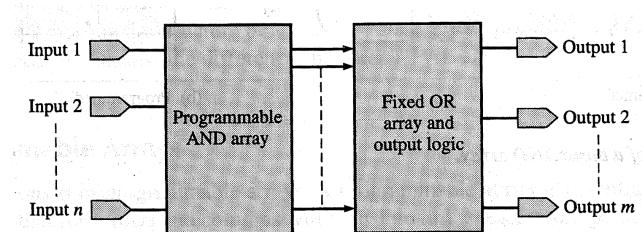


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Classifications of SPLDs

3. Programmable Array Logic (PAL)

It consists of a one-time programmable AND array and a fixed OR array with output logic.

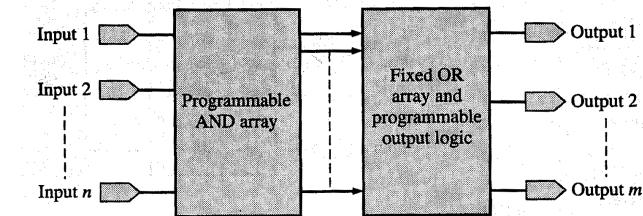


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Classifications of SPLDs

4. Generic Array Logic (GAL)

It consists of a reprogrammable AND array and a fixed OR array with programmable output logic.



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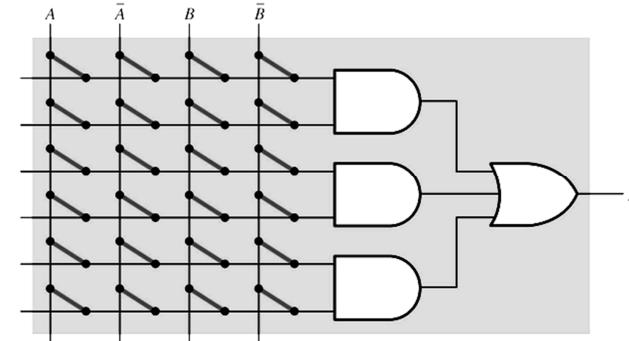
Classifications of SPLDs

- The PAL and the GAL are the most common PLDs used for logic implementation.
- The main differences between them lie in:
 - The GAL is reprogrammable.
 - The GAL has programmable output logic.

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Programmable Array Logic (PAL)

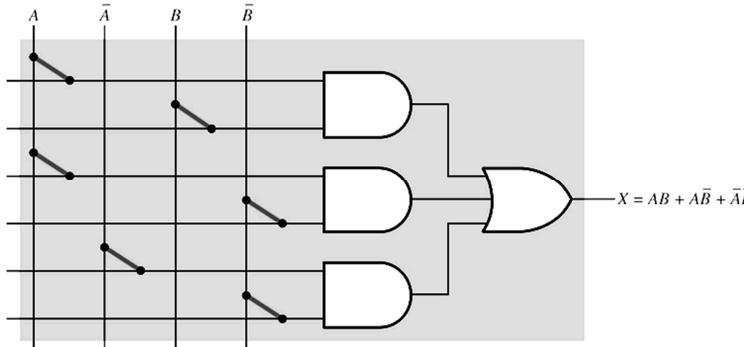
- Its AND/OR structure allows any sum-of-products (SOP) logic expression, not limited to 2 input variables as shown here.
- Any logic function can be expressed in SOP form.



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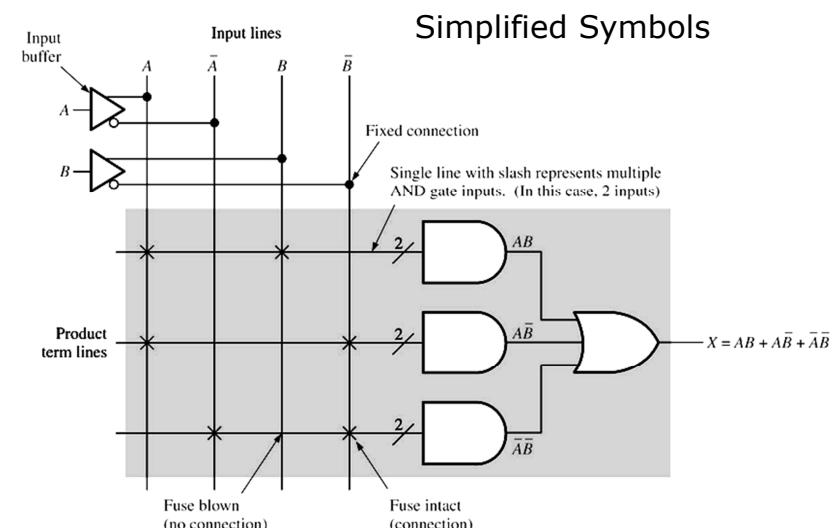
Programmable Array Logic (PAL)

- When the connection is required, the fuse is left intact.
- Otherwise it is blown open during programming.



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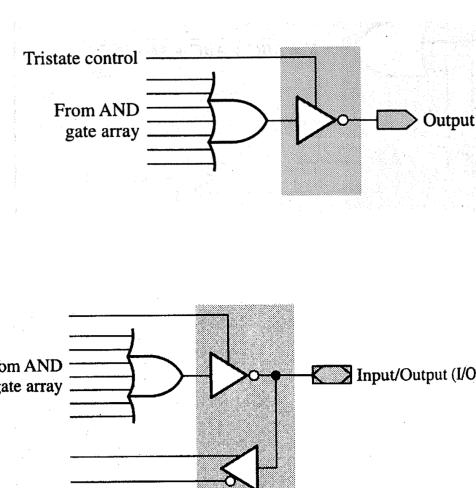
Programmable Array Logic (PAL)



Programmable Array Logic (PAL)

PAL Output Combinational Logic

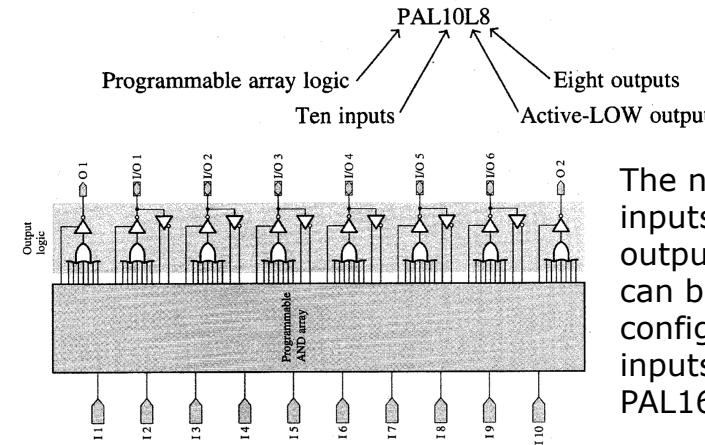
- The output is buffered and can be either active-LOW or active-HIGH.
 - The I/O pin can be used as an input or the feedback of an output.



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Programmable Array Logic (PAL)

Standard PAL Numbering



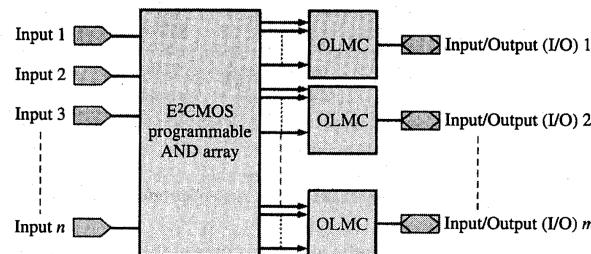
The number of inputs includes outputs that can be configured as inputs, e.g. PAL16L8.

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Generic Array Logic (GAL)

The GAL consists of:

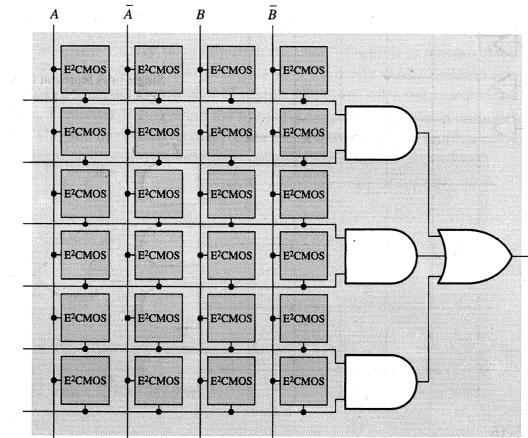
- A reprogrammable AND array
 - Output logic macrocells (OLMC), which contain the OR gates and programmable output logic.



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Generic Array Logic (GAL)

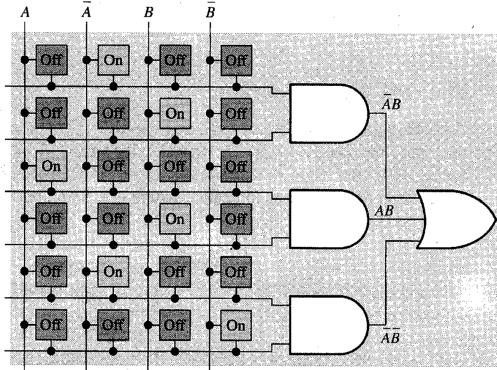
- The reprogrammable AND array is made up of electrically erasable CMOS (E2CMOS) cells.



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Generic Array Logic (GAL)

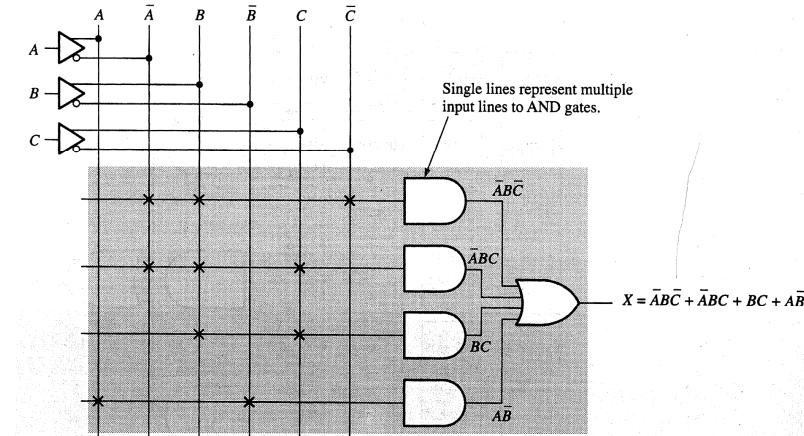
- A cell that is on connects its row and column, and a cell that is off disconnects the row and column.



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Generic Array Logic (GAL)

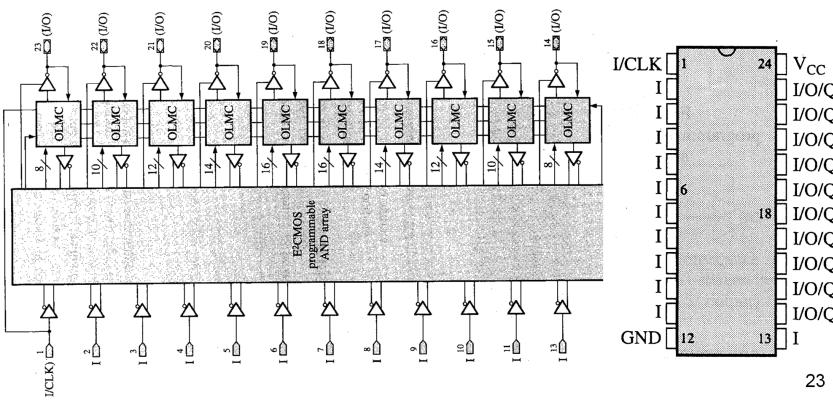
- Simplified symbols: a single line represents multiple input lines to AND gates.



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The GAL22V10

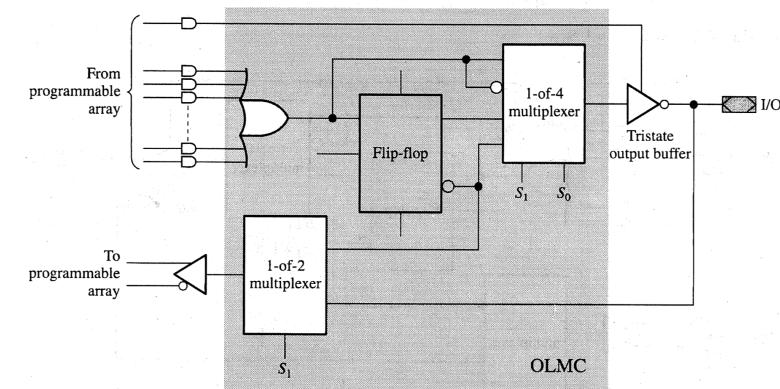
- The GAL22V10 contains 12 dedicated inputs and 10 input/outputs (I/Os). So it has up to 22 inputs and up to 10 outputs. Hence the name.



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The GAL22V10

- The OLMC can be configured as a combinational output, an input or a registered output.



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The GAL22V10

There are four inputs to the 1-of-4 multiplexer:

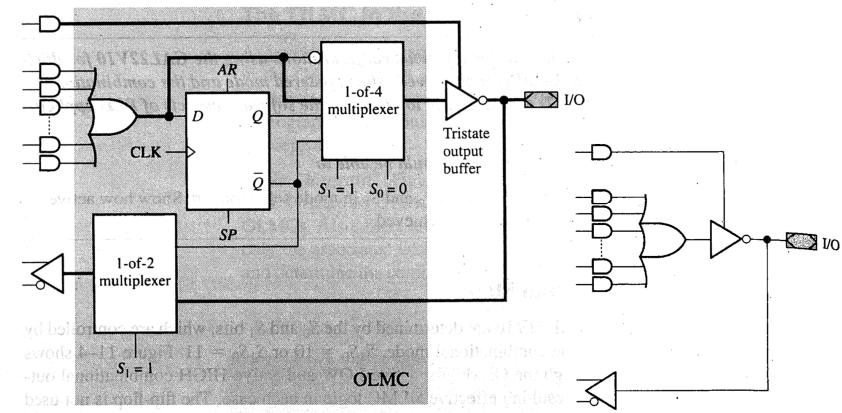
1. The OR gate output.
2. The complement of the OR gate output.
3. The registered OR gate output.
4. The complement of the registered OR gate output.

which corresponds to the four OLMC configurations.

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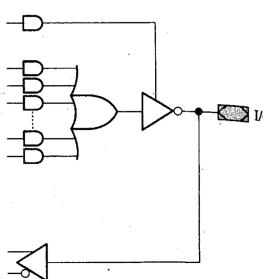
The GAL22V10

1. OLMC in the active-LOW combinational mode



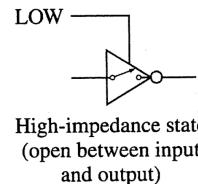
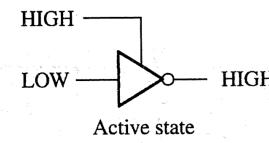
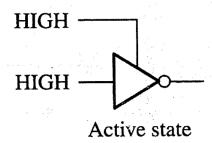
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The GAL22V10



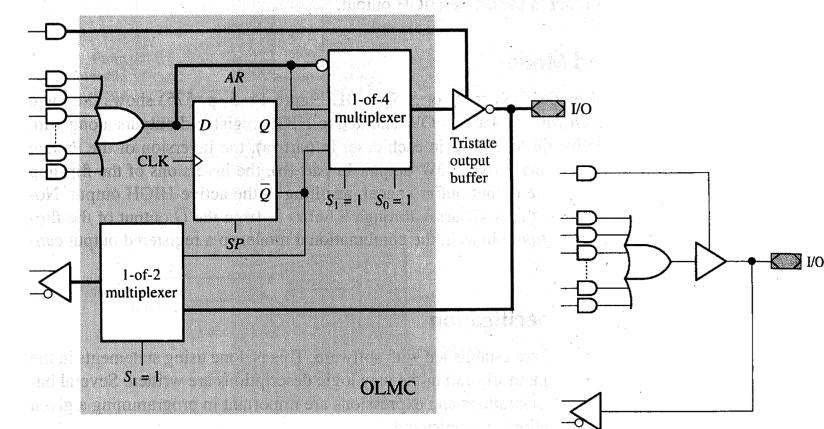
The tristate buffer:

- When the control line is HIGH, the I/O pin is an output which is fed back to the AND array.
- When the control line is LOW, the I/O pin is an input.



The GAL22V10

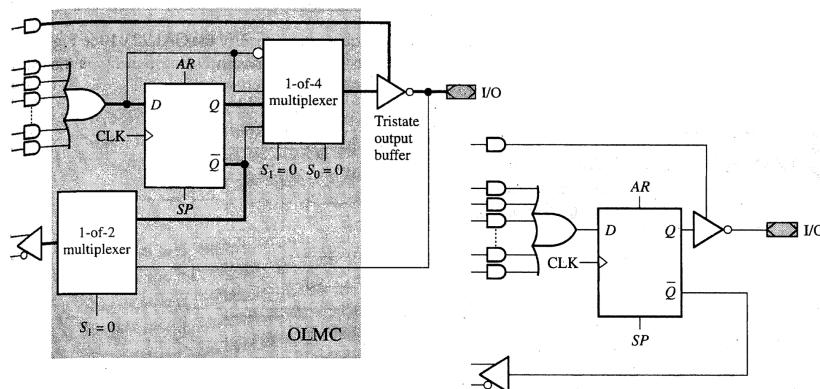
2. OLMC in the active-HIGH combinational mode



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The GAL22V10

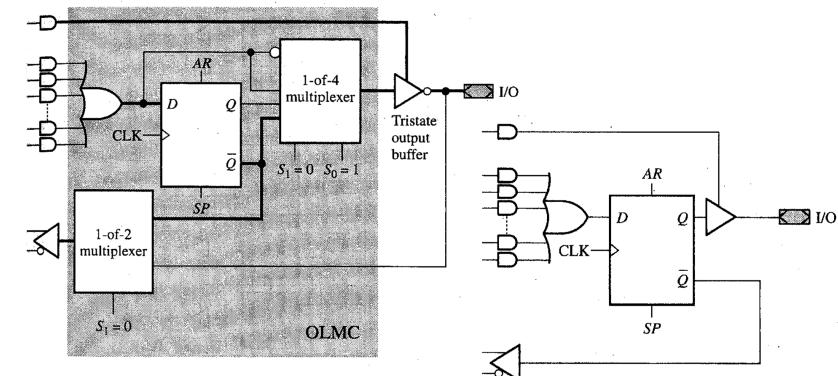
3. OLMC in the active-LOW registered mode



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The GAL22V10

4. OLMC in the active-HIGH registered mode

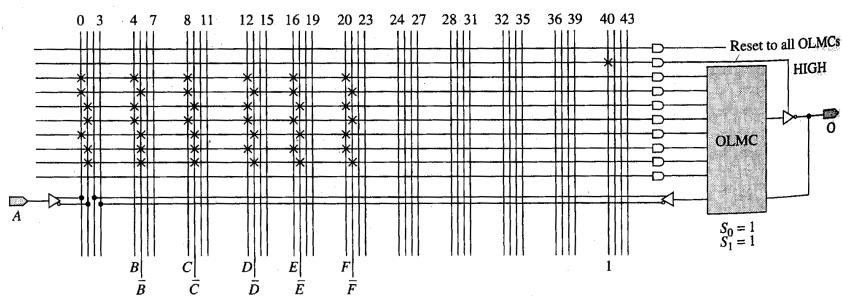


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The GAL22V10

An example to show how an SOP function is implemented.

$$X = ABCDEF + \bar{A}\bar{B}C\bar{D}\bar{E}\bar{F} + \bar{A}\bar{B}\bar{C}D\bar{E}\bar{F} + \bar{A}\bar{B}C\bar{D}\bar{E}F + A\bar{B}\bar{C}\bar{D}\bar{E}F + \bar{A}\bar{B}\bar{C}D\bar{E}F + \bar{A}\bar{B}\bar{C}\bar{D}\bar{E}\bar{F}$$



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