



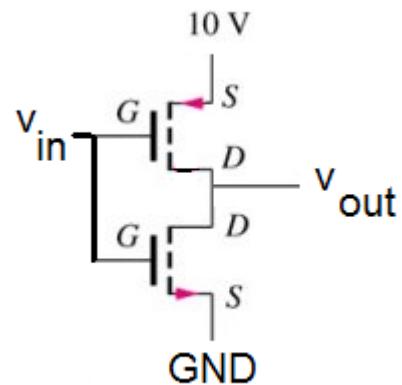
Xi'an Jiaotong-Liverpool University

西交利物浦大学

CMOS logic family

- **Inverters**
 - understanding with switch models
 - basic CMOS layouts
- **NAND gates** (materials developed by Prof. C. Z. Zhao)
- **NOR gates** (materials developed by Prof. C. Z. Zhao)
- **Design exercise**
- **General gates**
 - complicated gates

Logic gates



Circuit
schematic

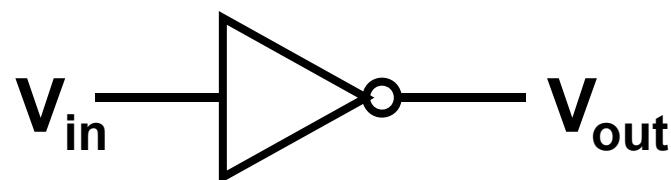
Circuit layout??

V_{in}	V_{out}
0 (0V)	1 (10V)
1 (10V)	0 (0V)

Truth table

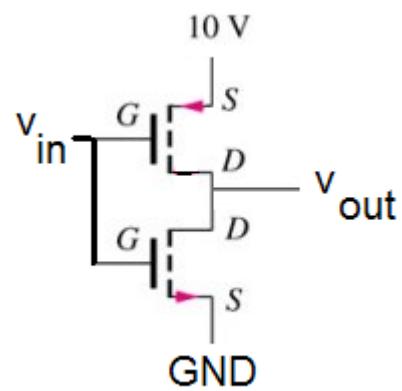
Output function

$$V_{out} = \overline{V}_{in}$$



Logic symbol

A CMOS Inverter



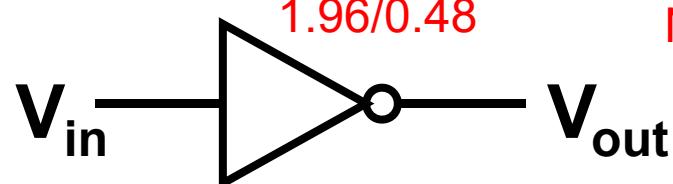
$V_{in} = 0V$ causes the NMOS transistor to be off (cut-off mode) and PMOS to be on (triode mode). A low source-to-drain resistance of the PMOS and high drain-to-source resistance of the NMOS results in voltage divider with V_{out} nearly 10V.

$V_{in} = 10V$ causes the PMOS transistor to be off (cutoff mode) and NMOS transistor to be on (triode mode). A high source-to-drain resistance of the PMOS and a low drain-to-source resistance of the NMOS results in voltage divider with V_{out} near 0V.

V_{in}	V_{out}
0 (0V)	1 (10V)
1 (10V)	0 (0V)

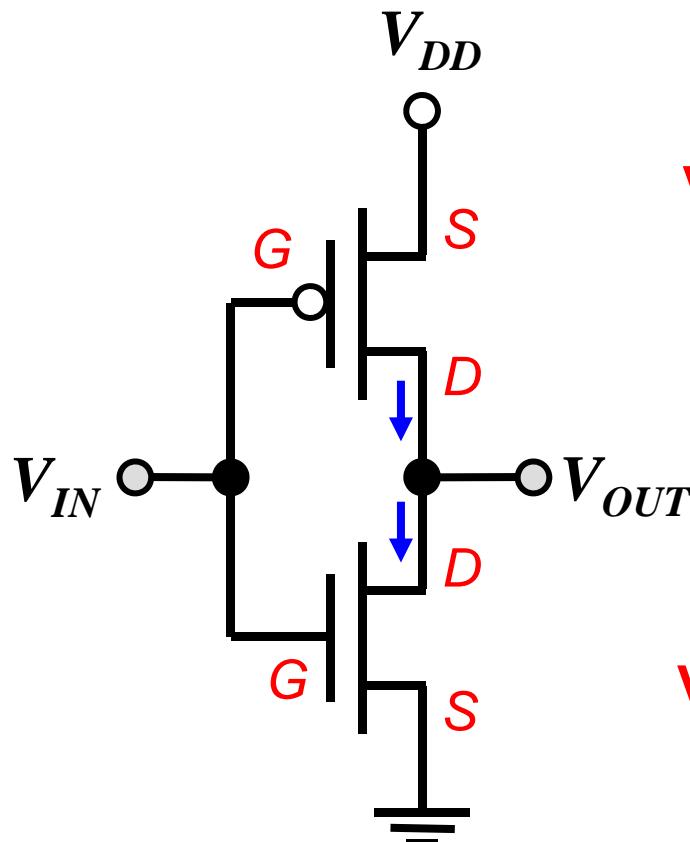
P 1.96
N 0.48

$$V_{out} = \bar{V}_{in}$$

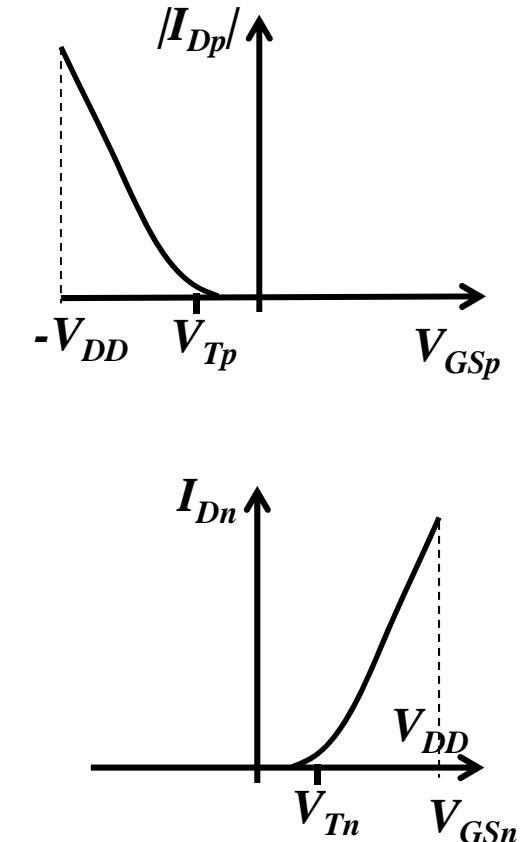
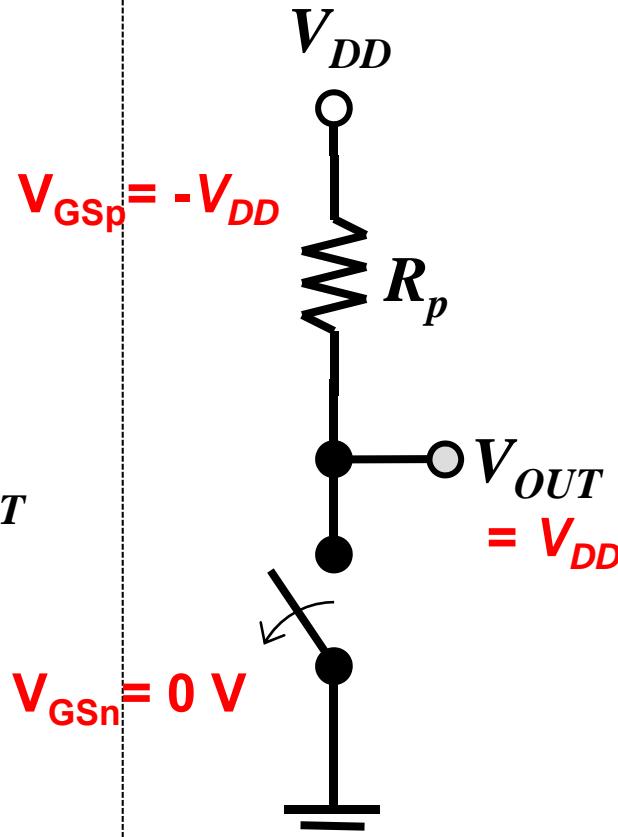


The CMOS Inverter: Intuitive Perspective

CIRCUIT

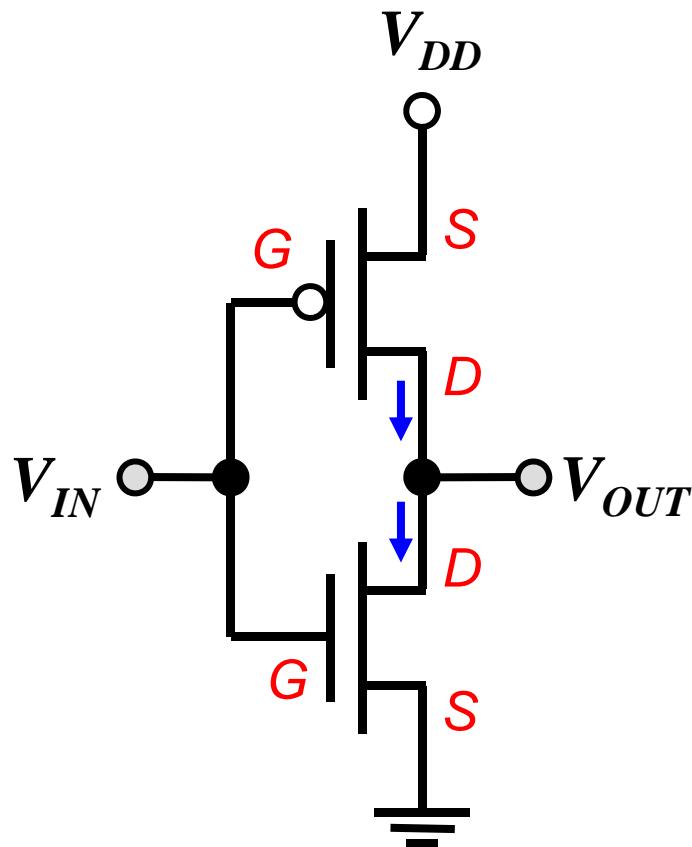


SWITCH MODELS

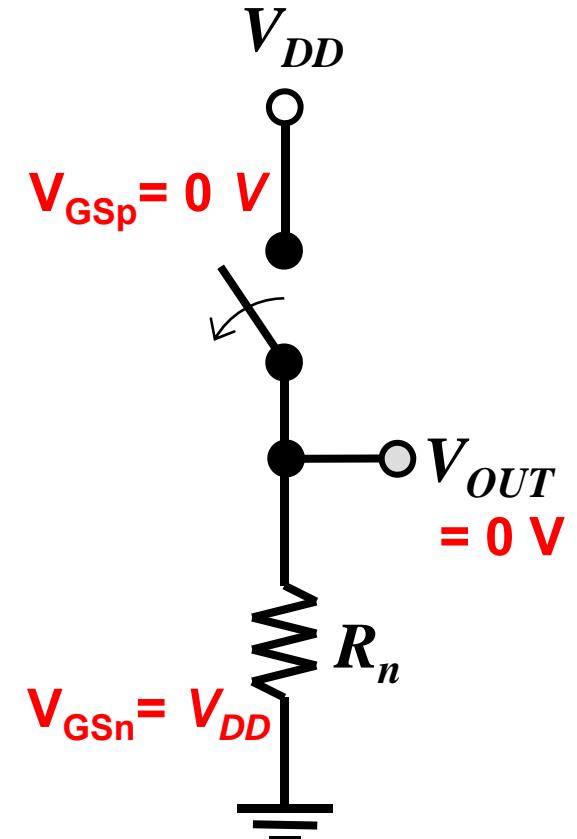
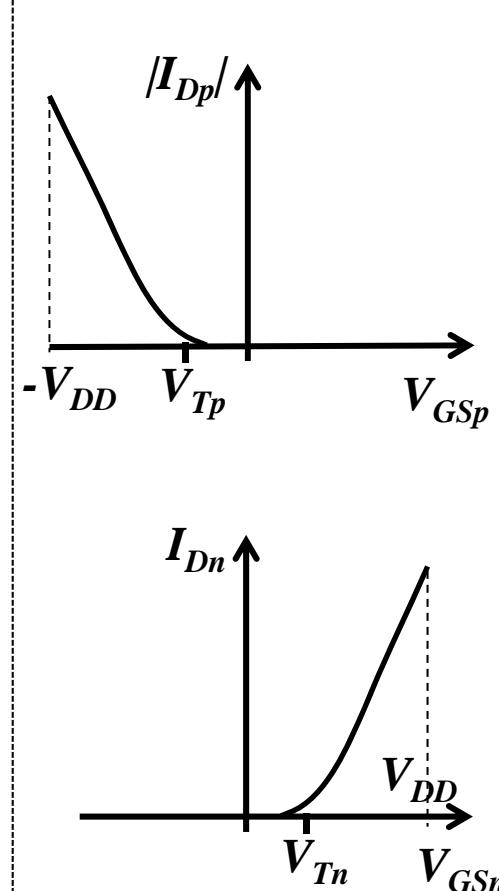


The CMOS Inverter: Intuitive Perspective

CIRCUIT



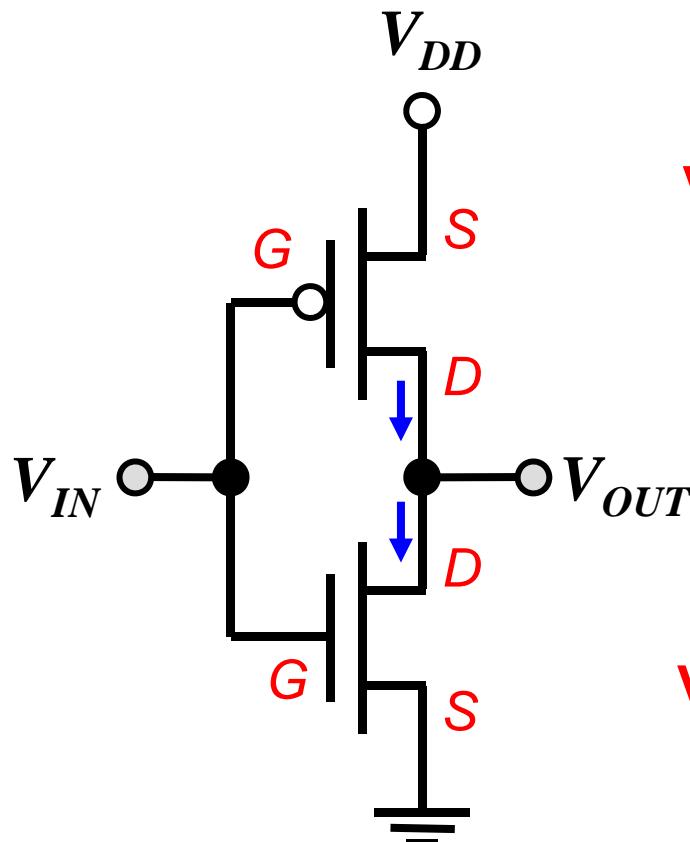
SWITCH MODELS



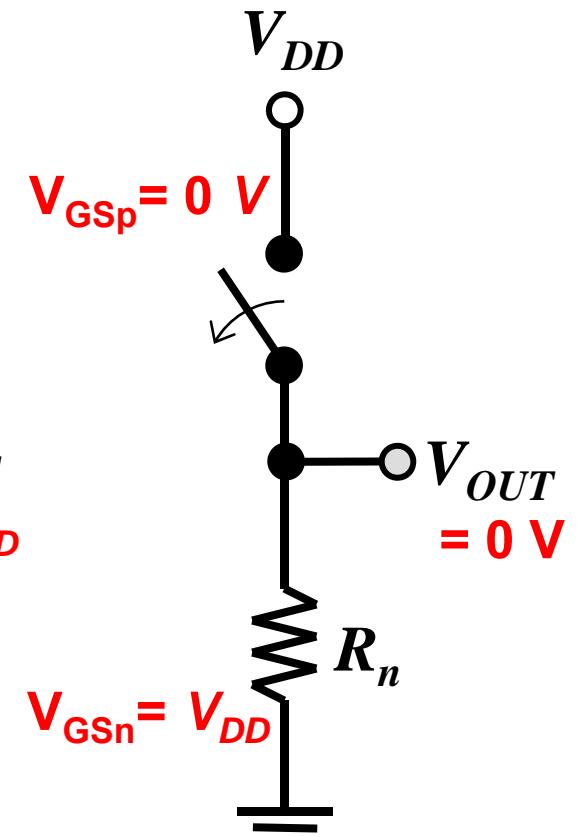
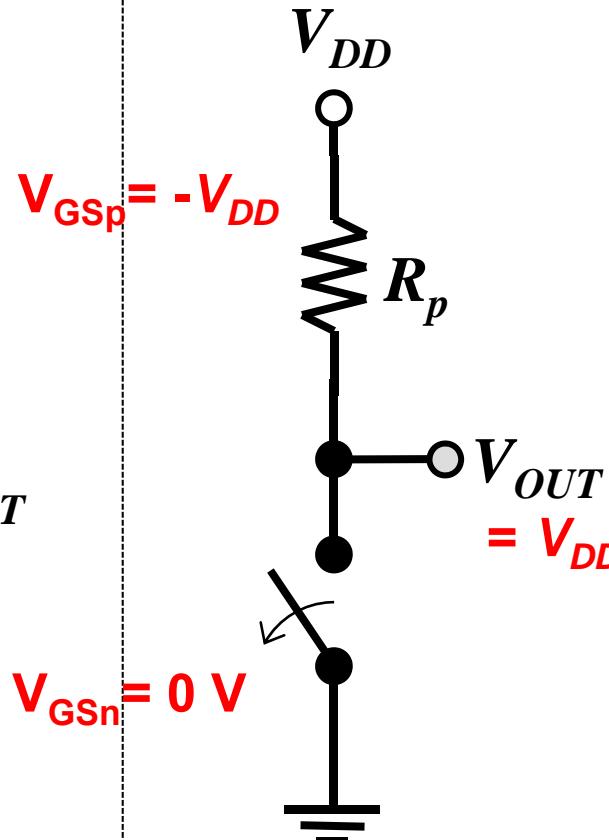
$$V_{IN} = V_{DD}$$

The CMOS Inverter: Intuitive Perspective

CIRCUIT



SWITCH MODELS

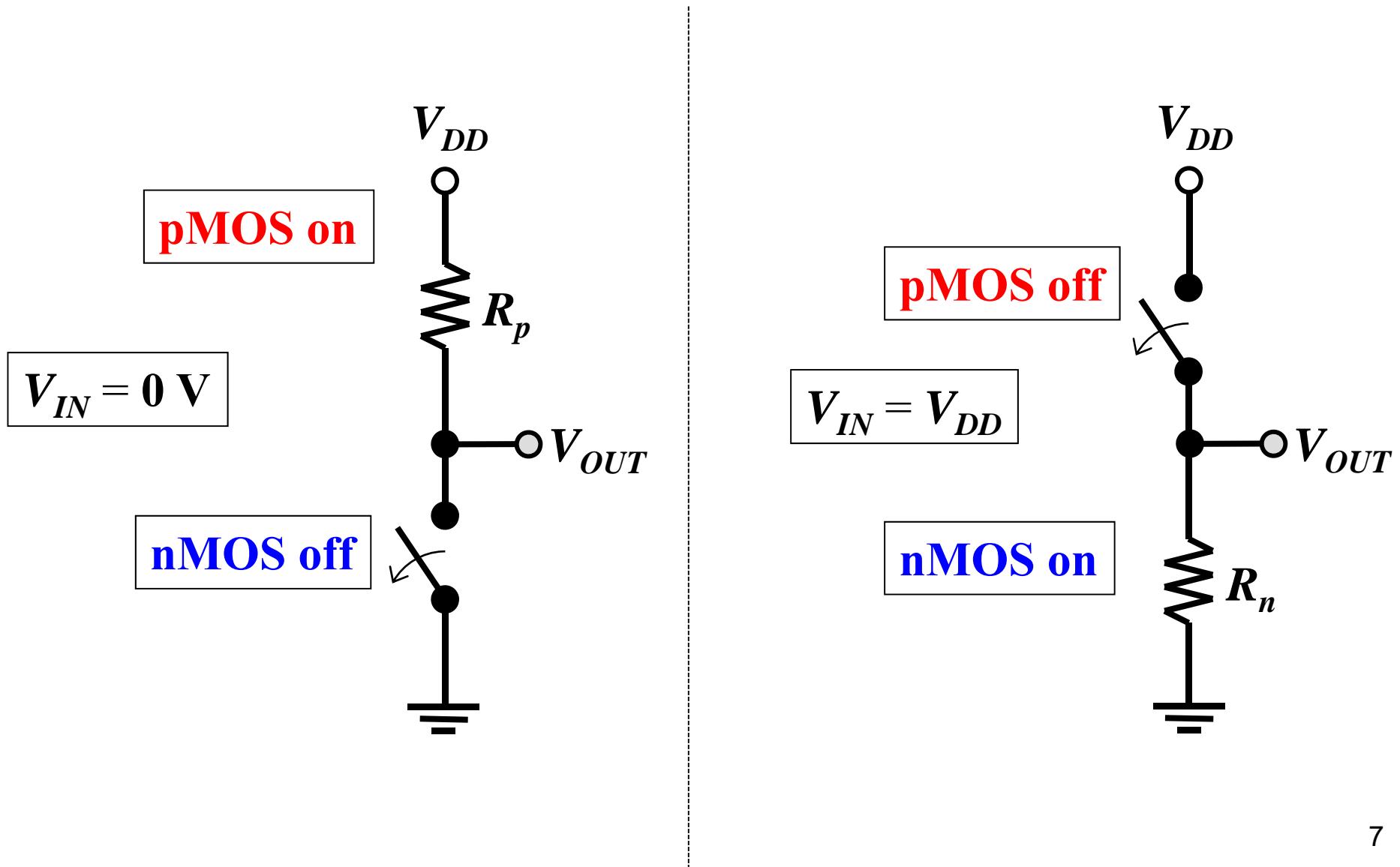


Low static power consumption, since one MOSFET is always off in steady state

$$V_{IN} = 0 \text{ V}$$

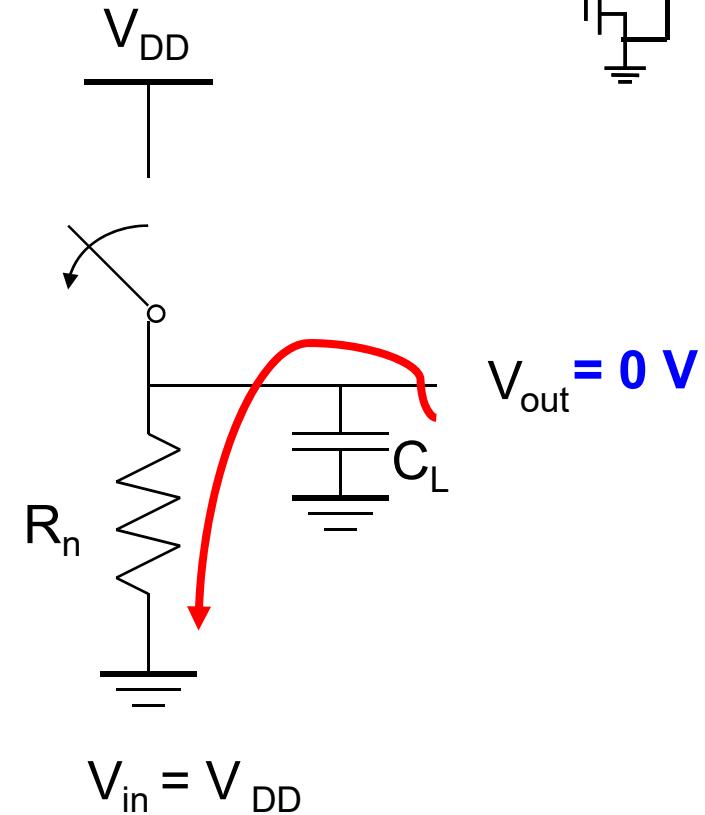
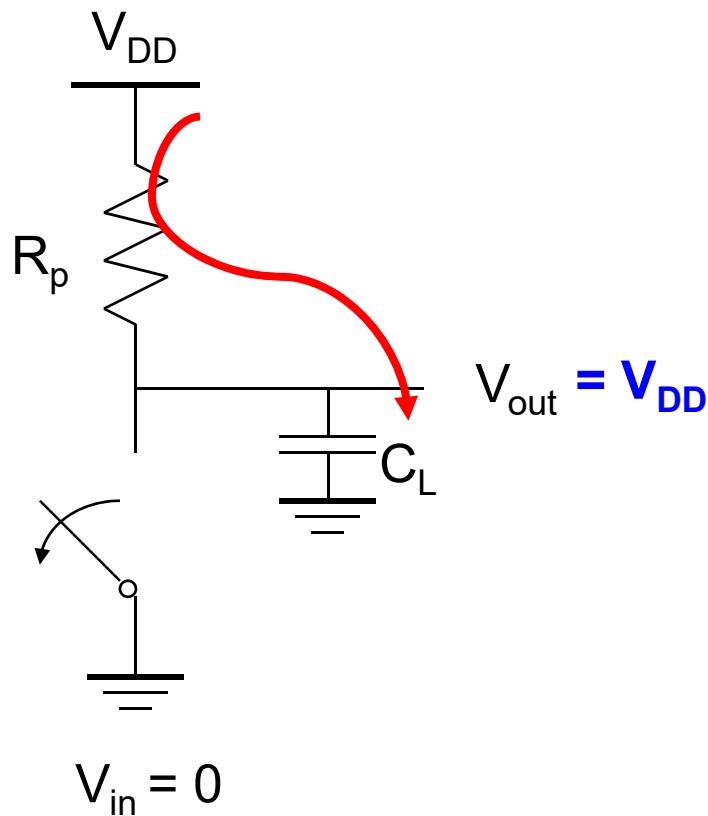
$$V_{IN} = V_{DD}$$

The CMOS Inverter: Intuitive Perspective



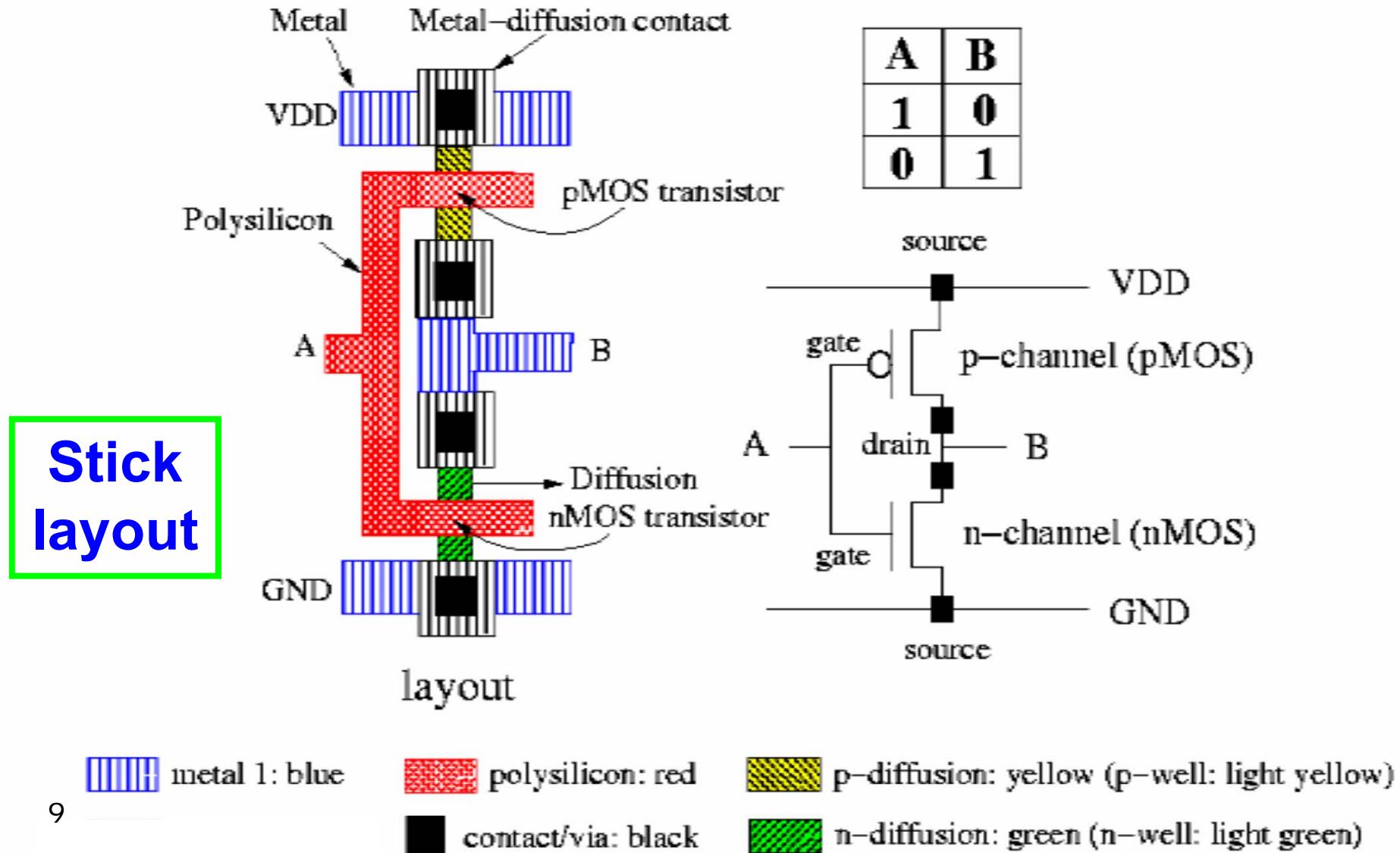
CMOS Inverter:

Switch Model of Dynamic Behaviour

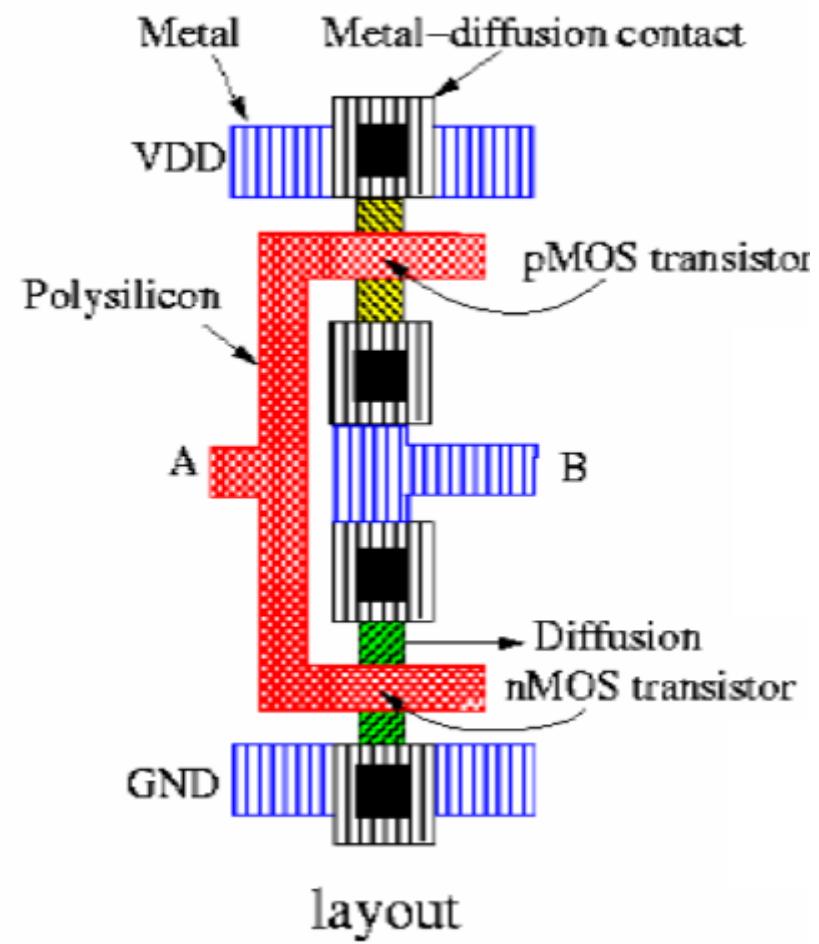
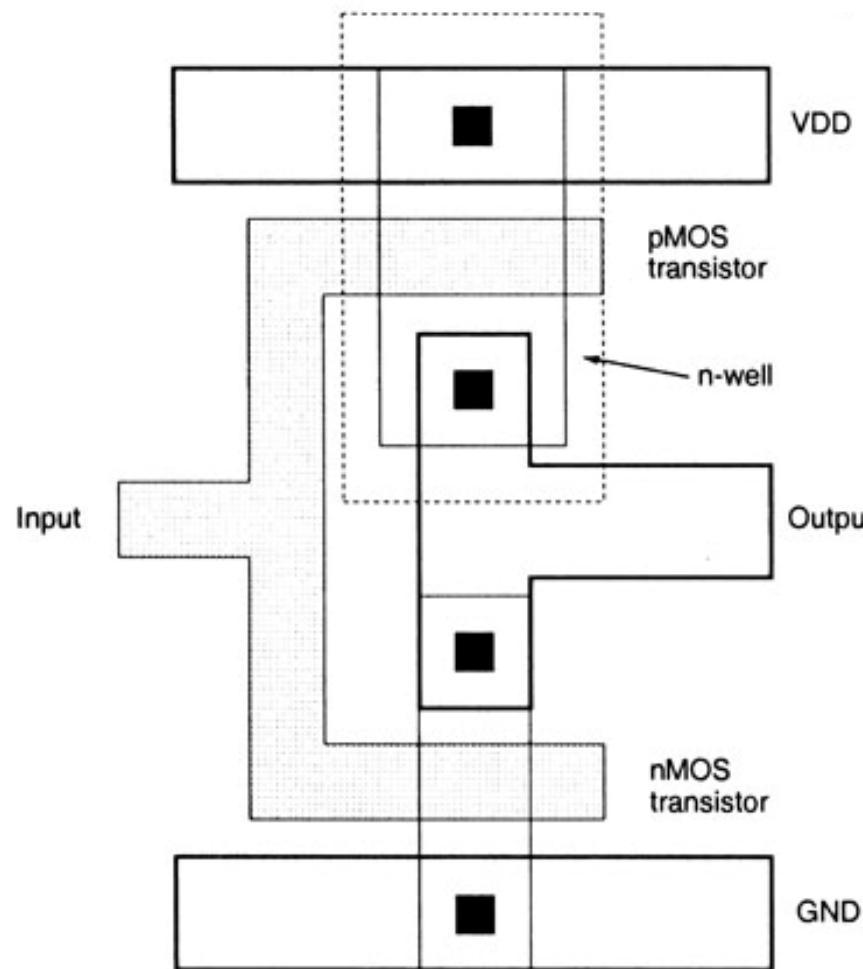


- The gate response time is determined by the time to **charge** C_L through R_p (**discharge** C_L through R_n).

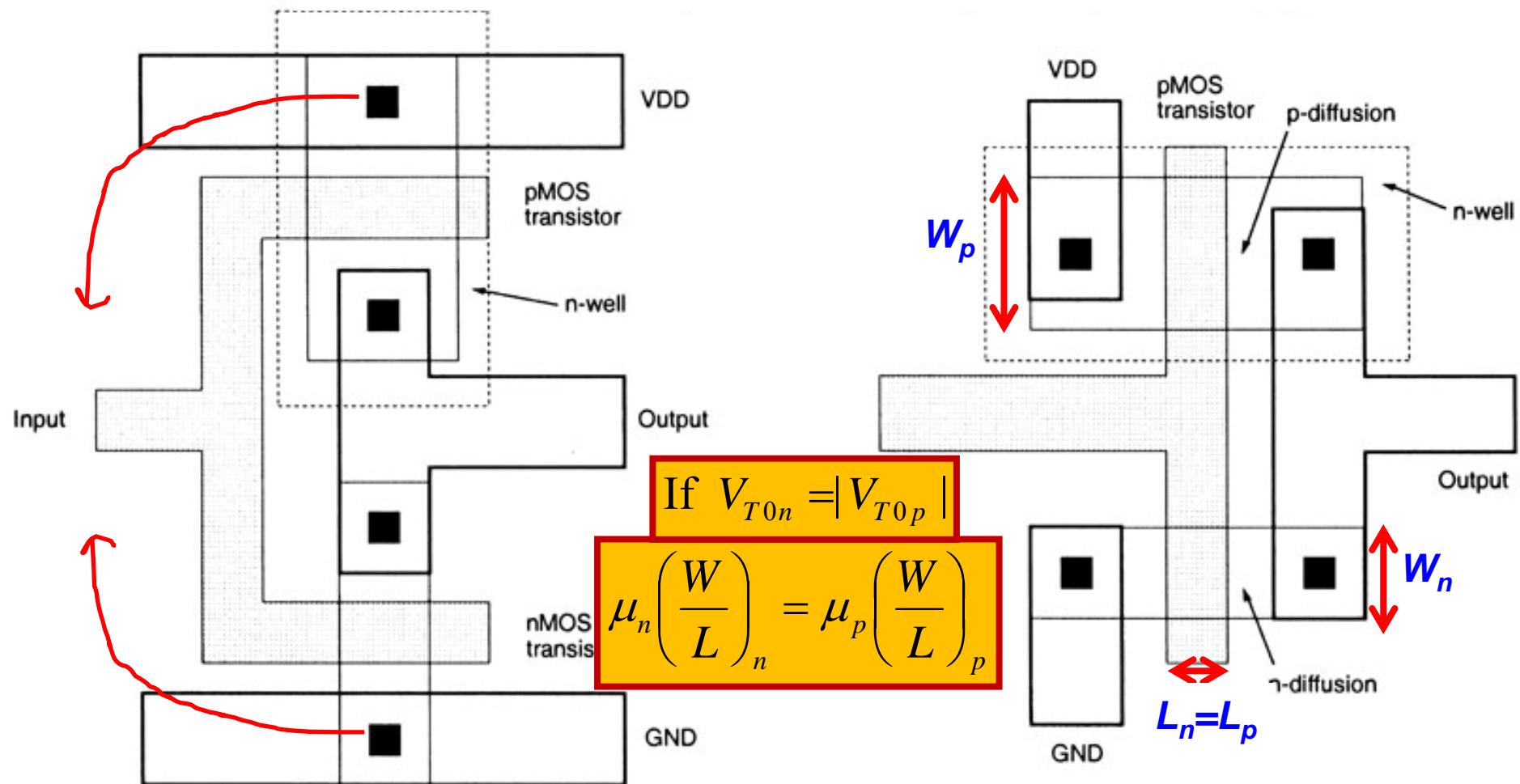
A CMOS Inverter



A CMOS Inverter Layout



A CMOS Inverter Layout





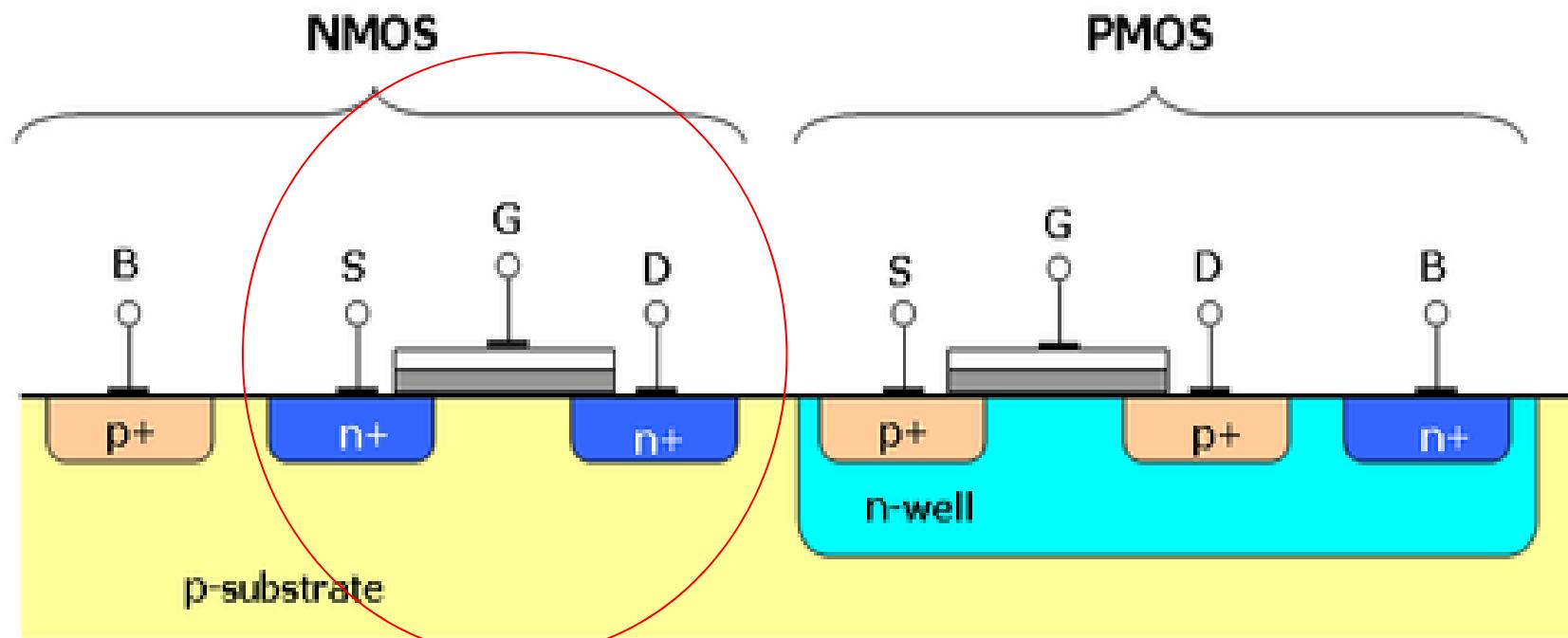
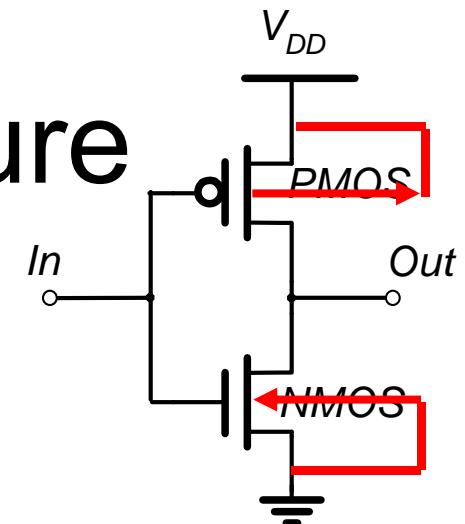
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CMOS logic family

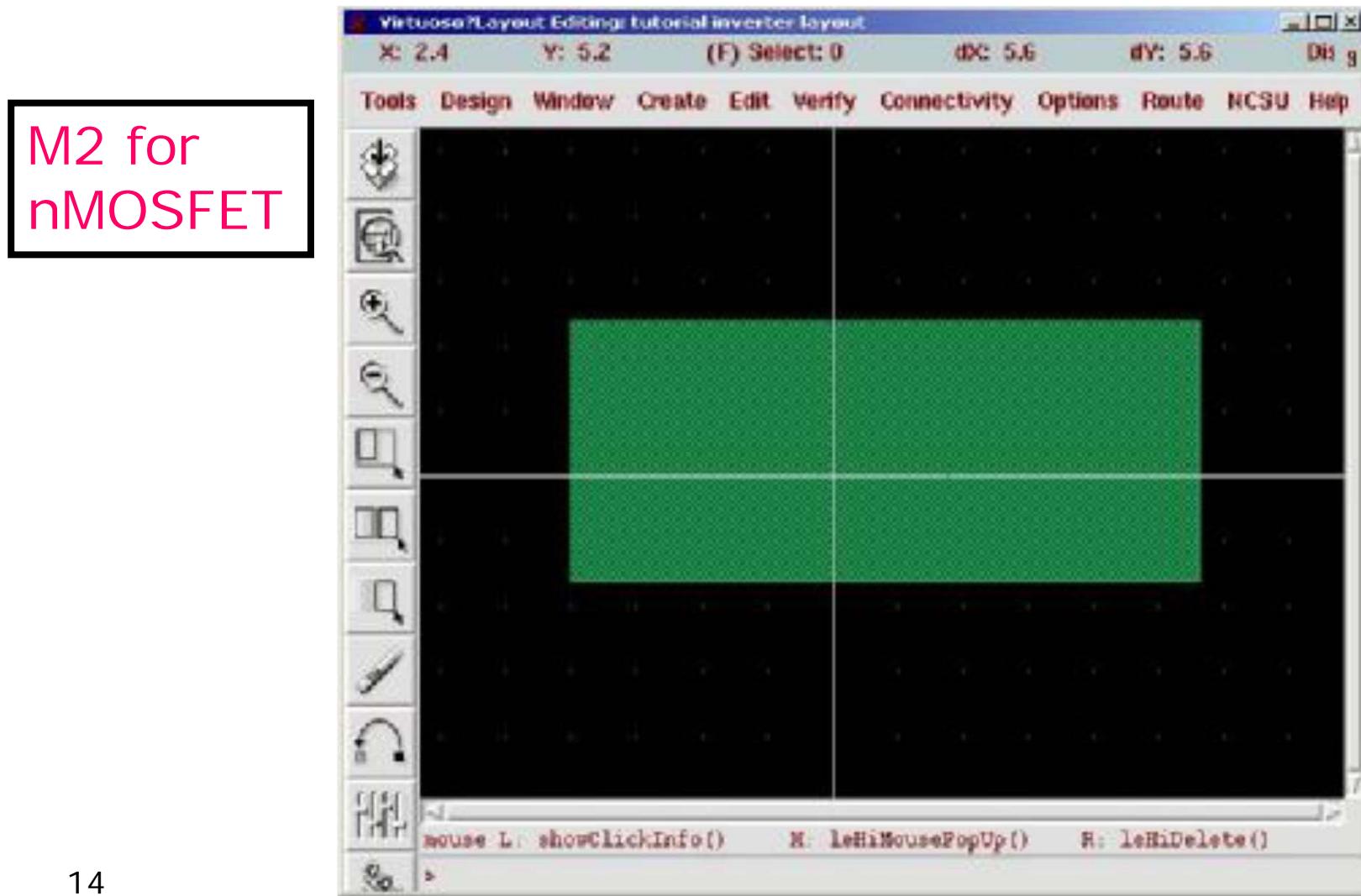
- Inverters
 - Switch models
 - Basic CMOS layouts
- NAND gates
- NOR gates
- Design exercise
- General gates
 - Complicated gates

CMOS basic structure

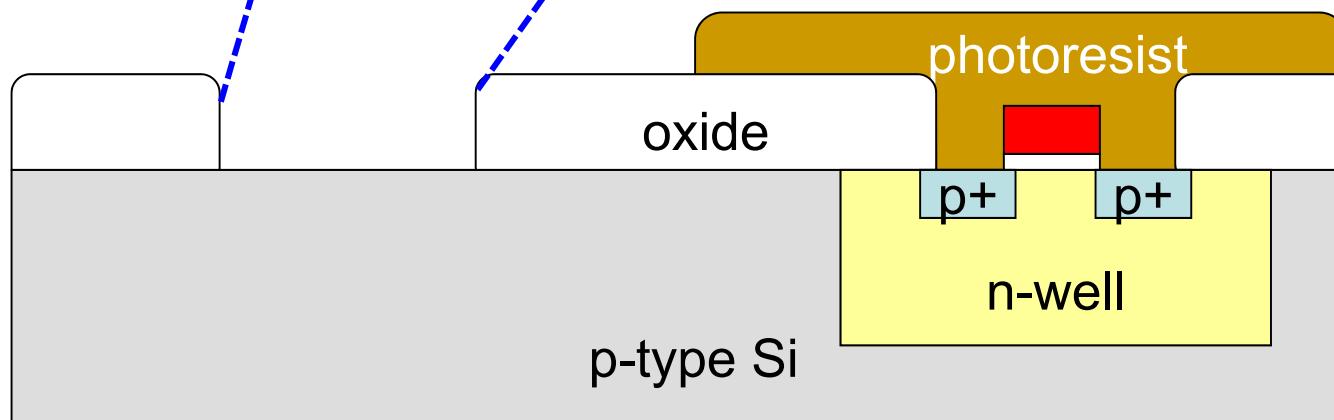
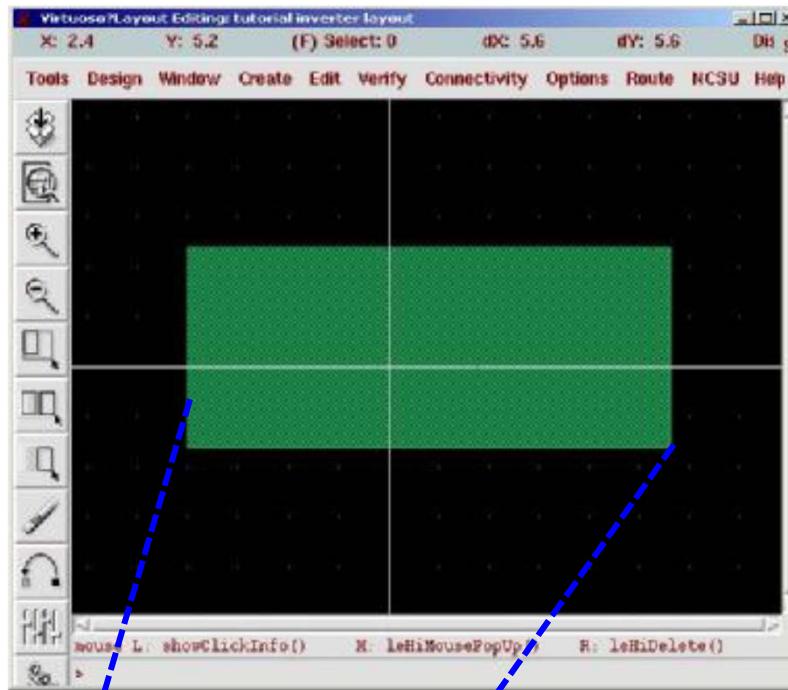


How to draw layouts:

1. Drawing the *n active* after calculation W/L



M2 for
nMOSFET

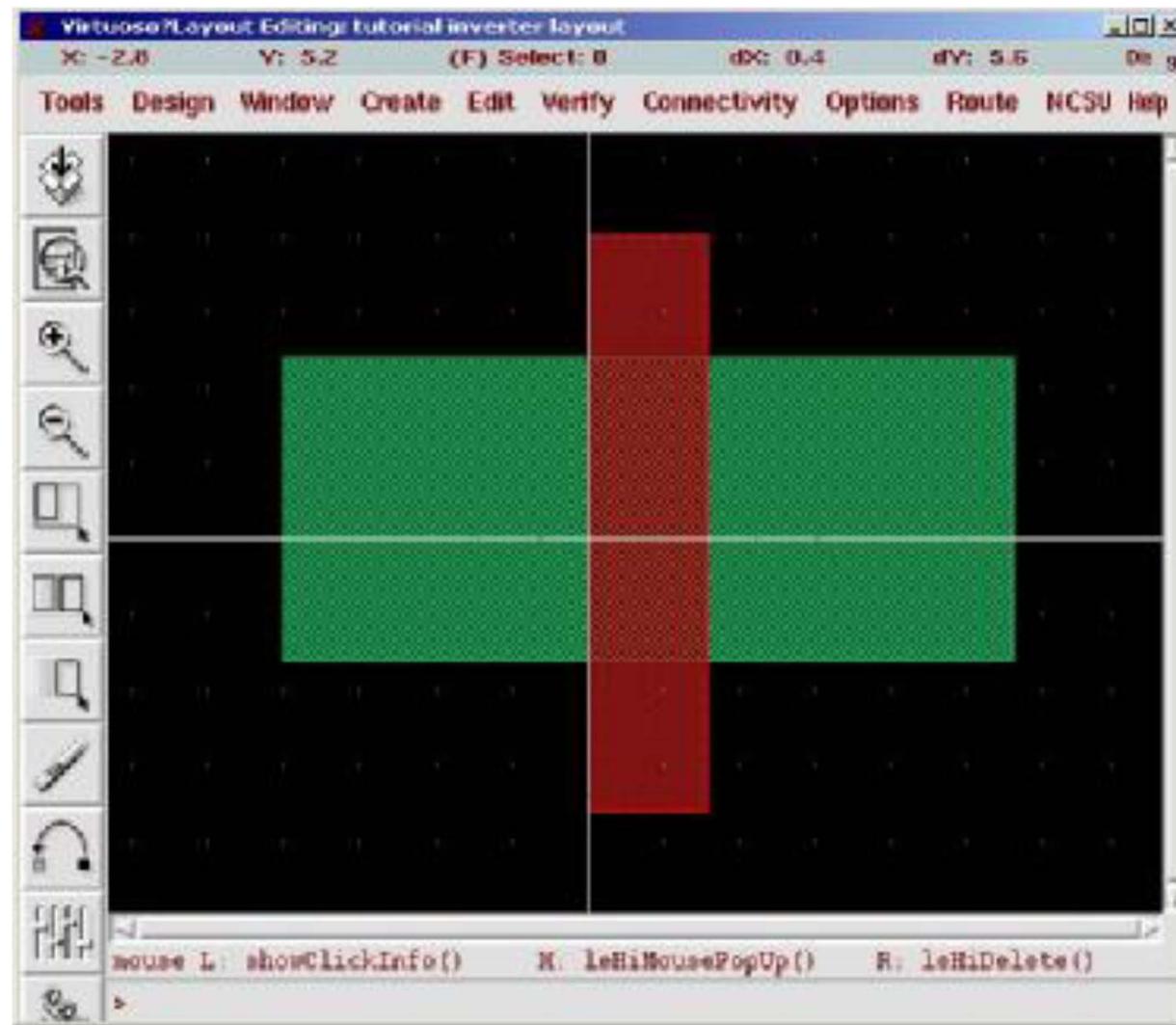


How to draw layouts:

2. Drawing poly-Si Gate (*poly*)

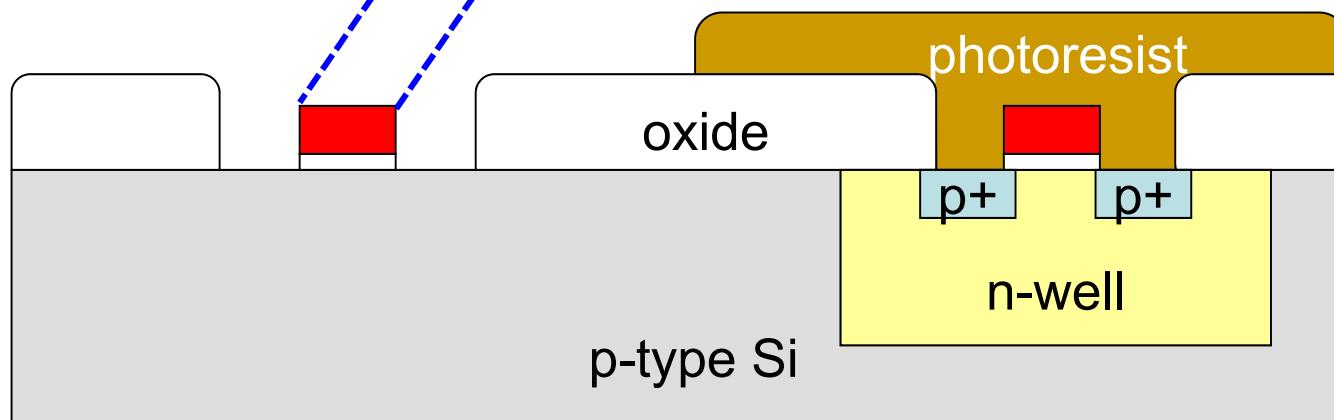
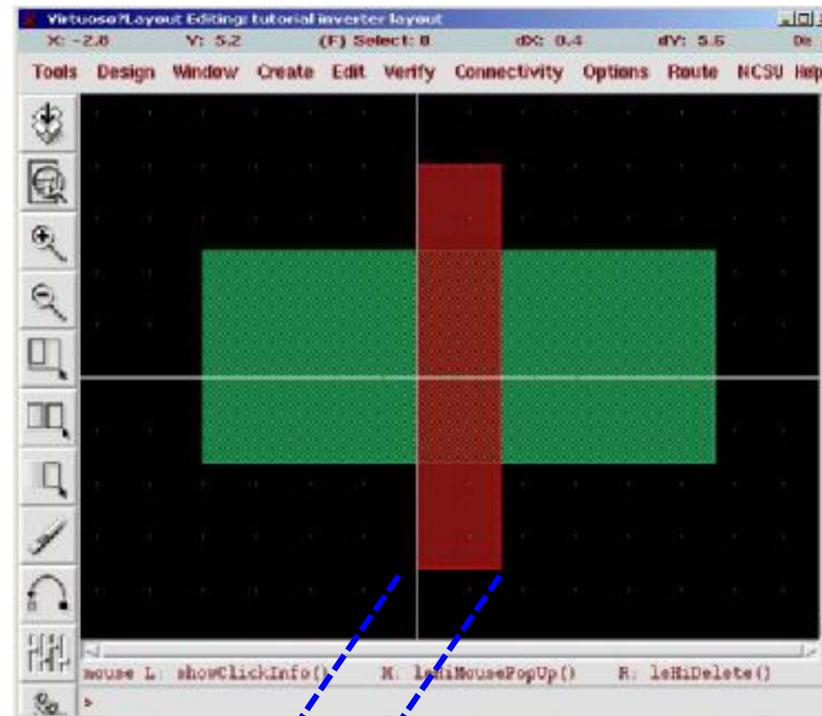
M3: poly

nMOSFET



M3: poly

nMOSFET

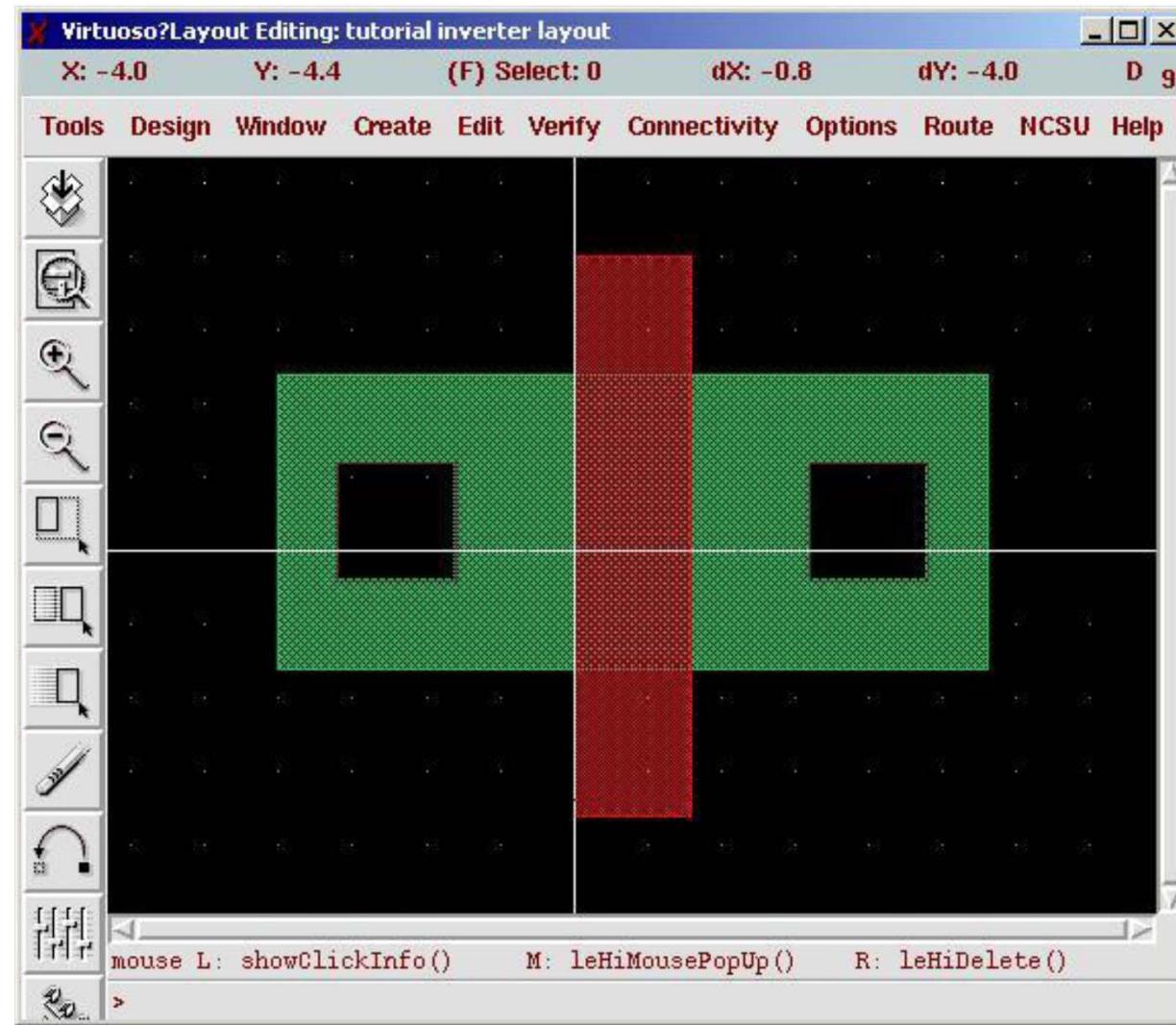


How to draw layouts:

3. Making active contact

M6: contact

nMOSFET



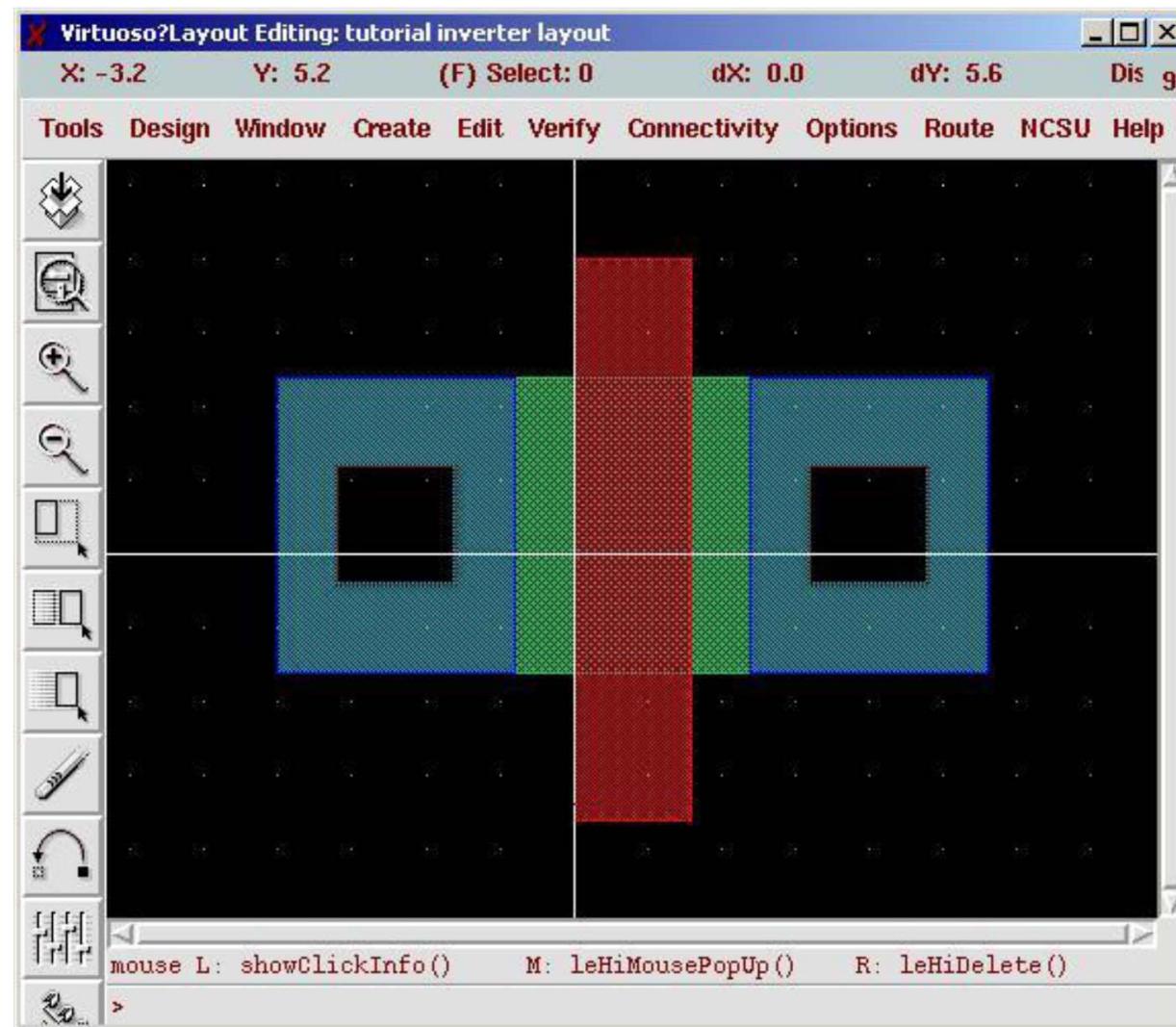
How to draw layouts:

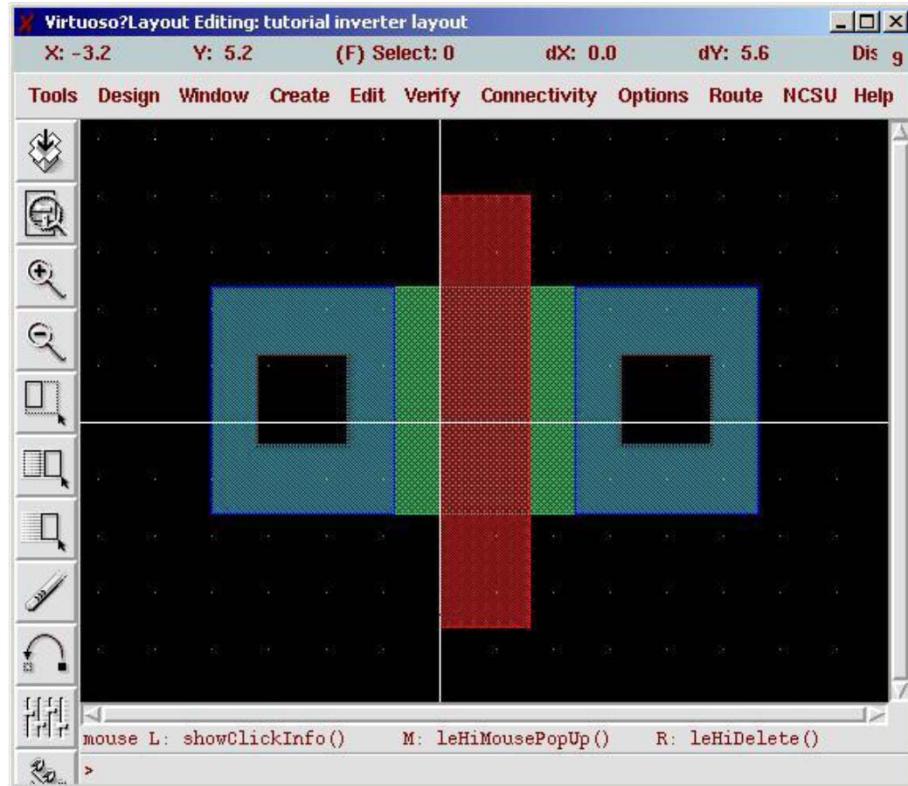
4. Covering the contacts with Metal

M7: metal

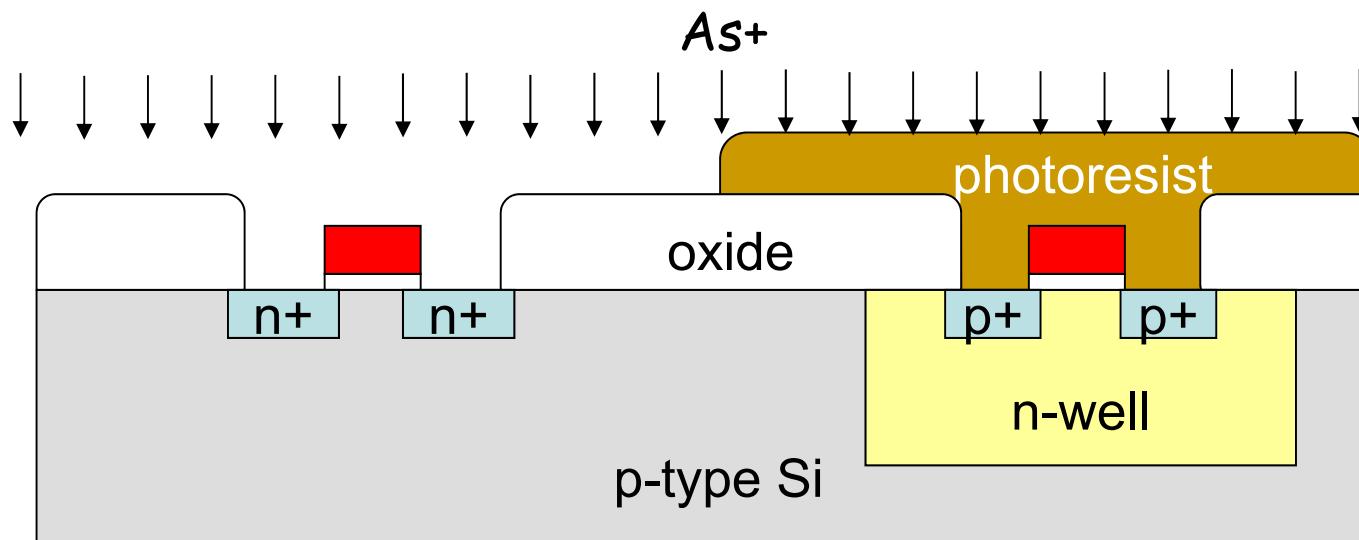
(every
contact
holes must
be covered)

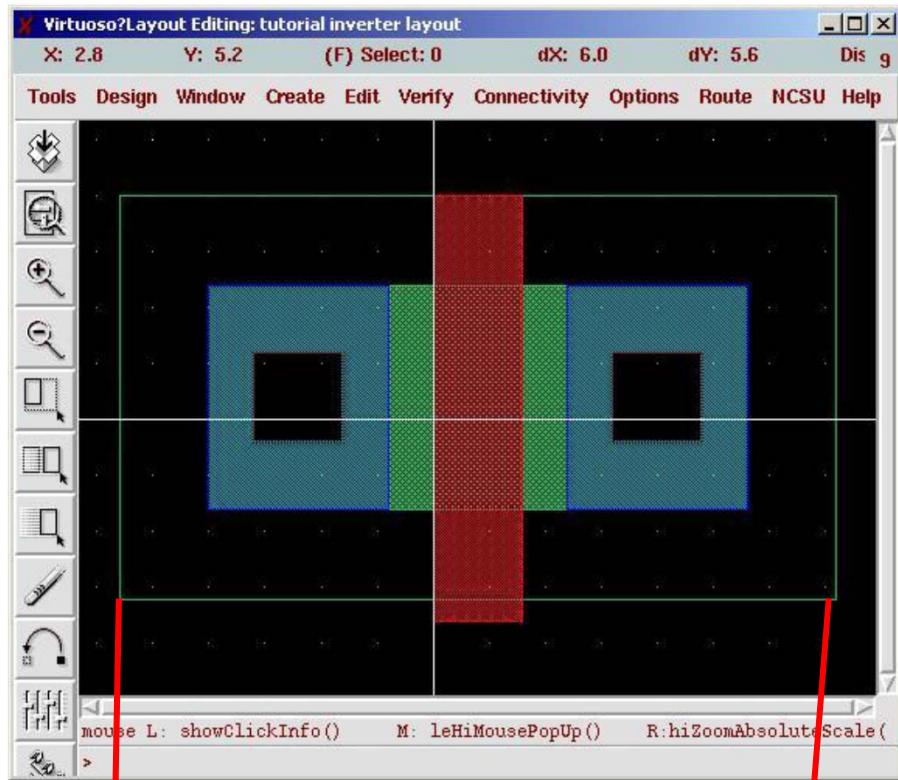
nMOSFET



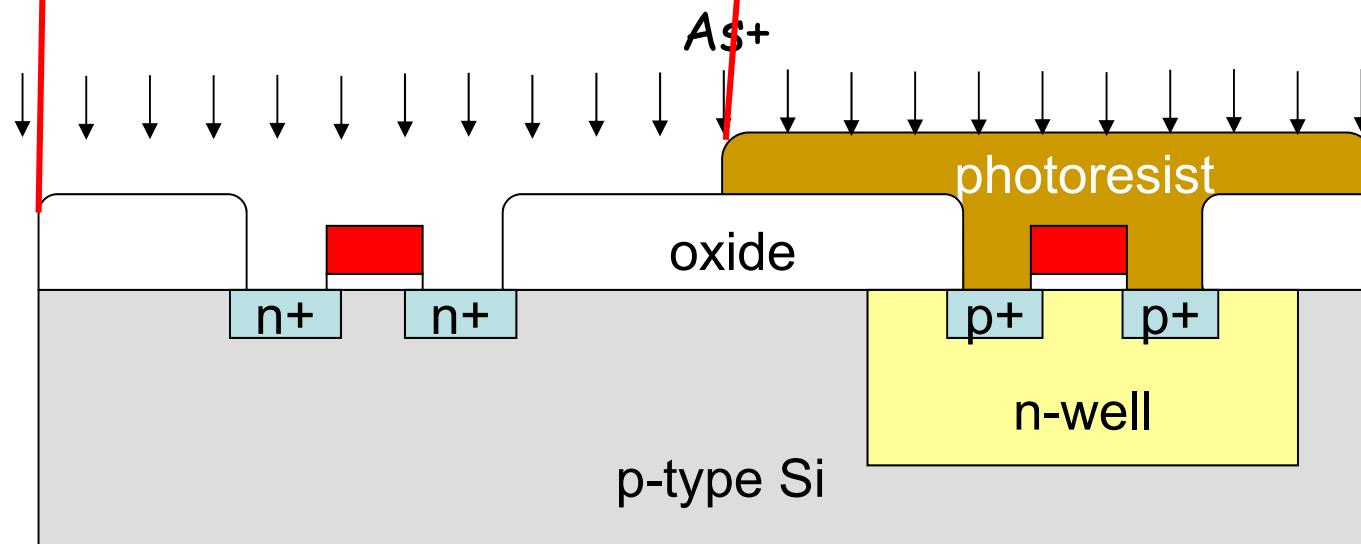


nMOSFET





M5: As⁺ implantation



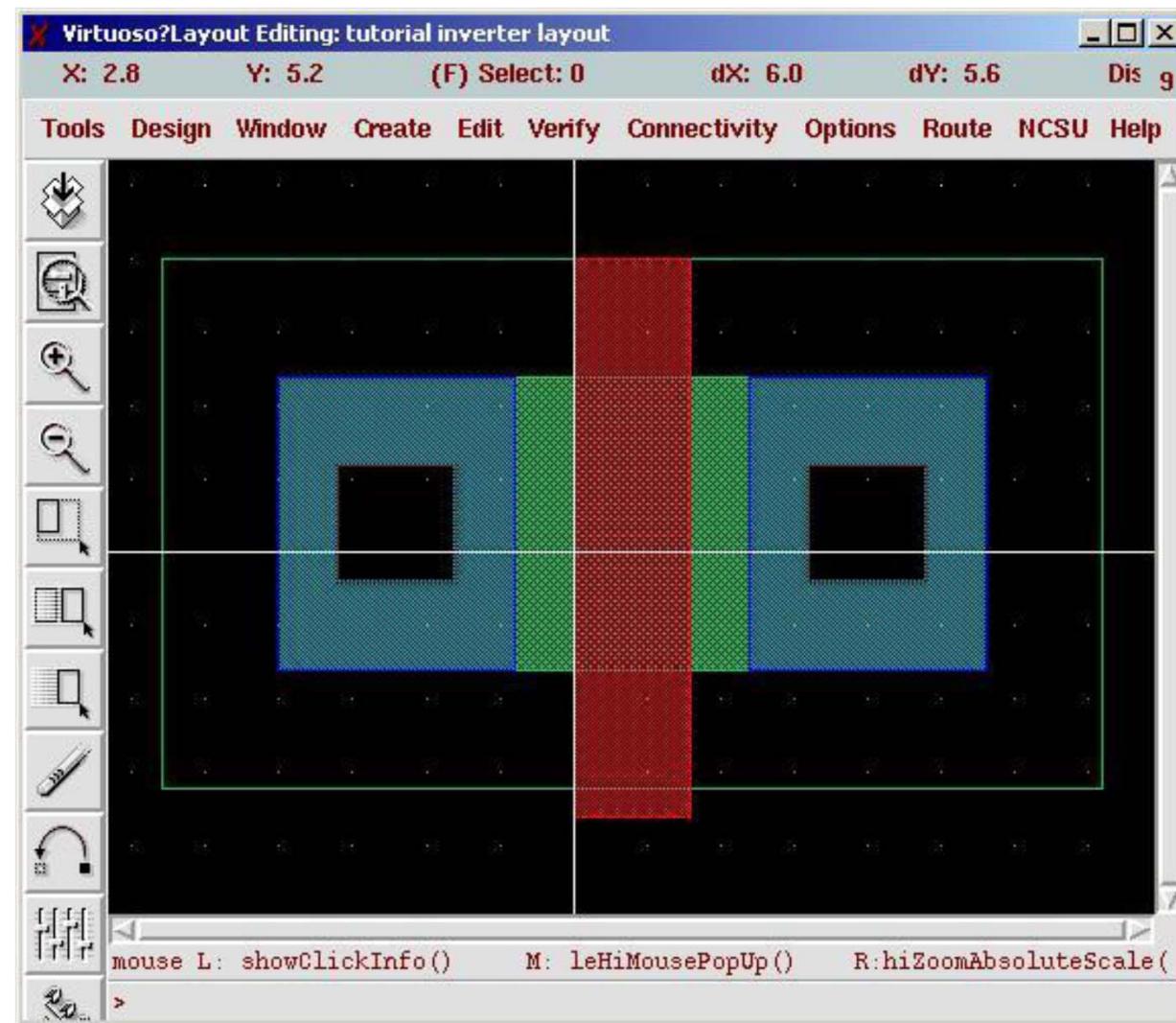
How to draw layouts:

5. Drawing the N-select layer

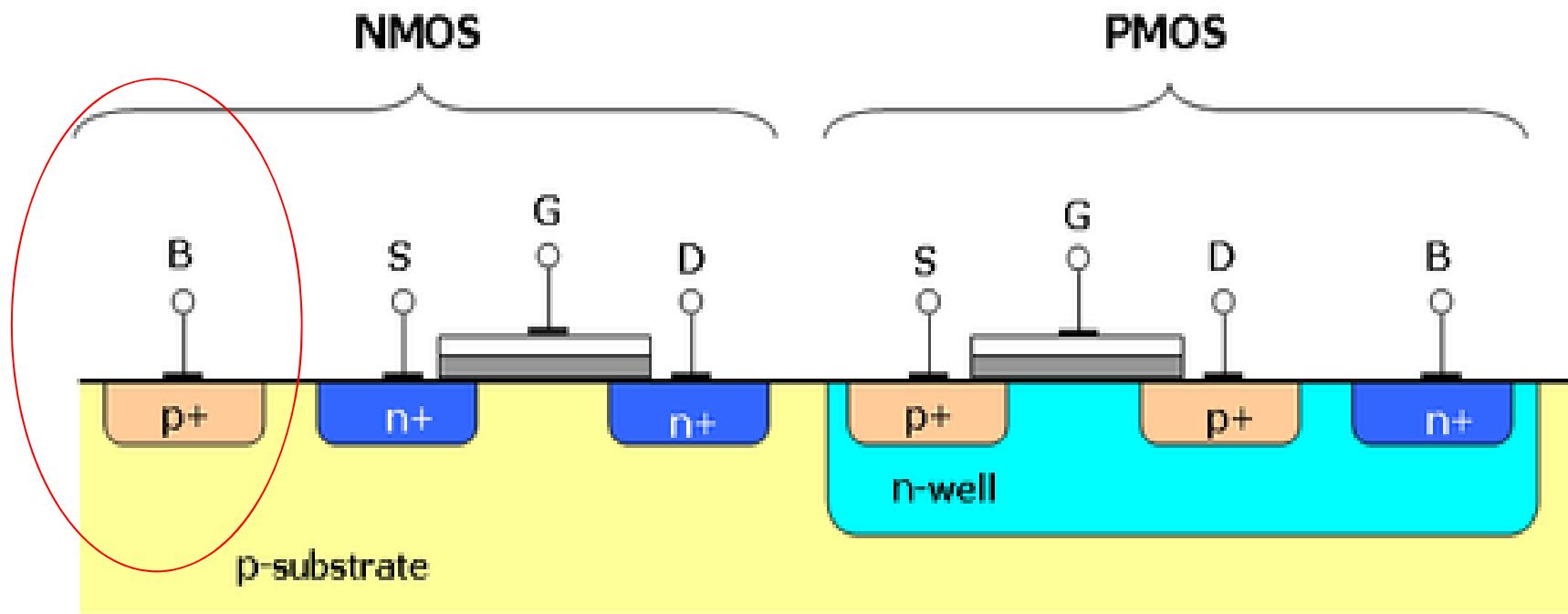
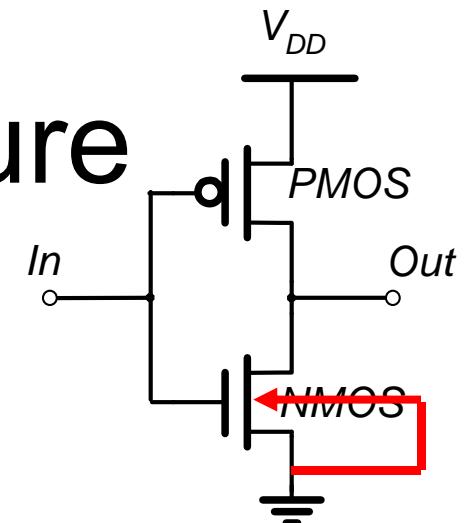
M5: As⁺
implantation

nMOSFET

M2
M3
M5
M6
M7



CMOS basic structure



How to draw layouts:

6. p-select layer, p-active layer, p-substrate contact & metal

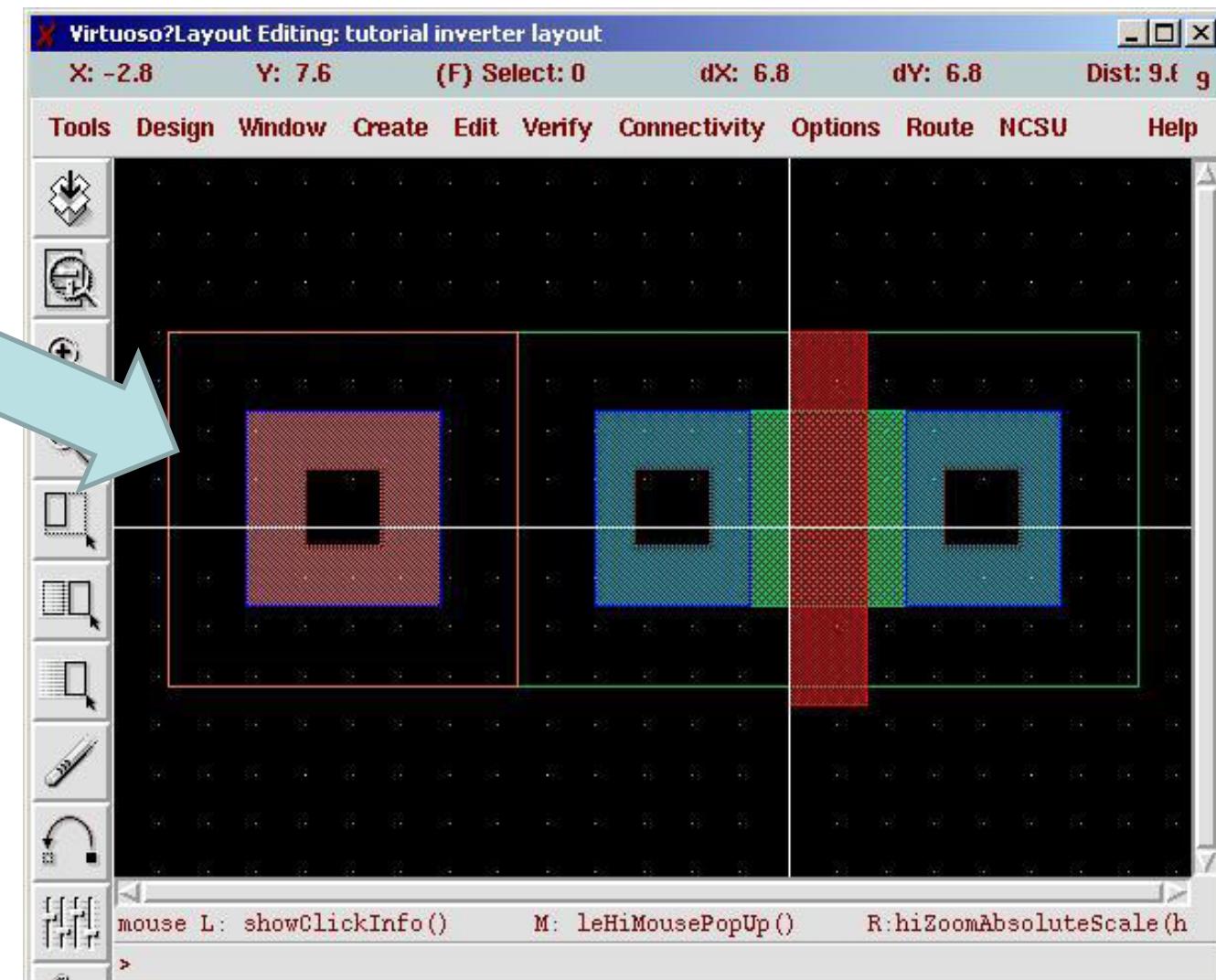
M4: B⁺

M2: active

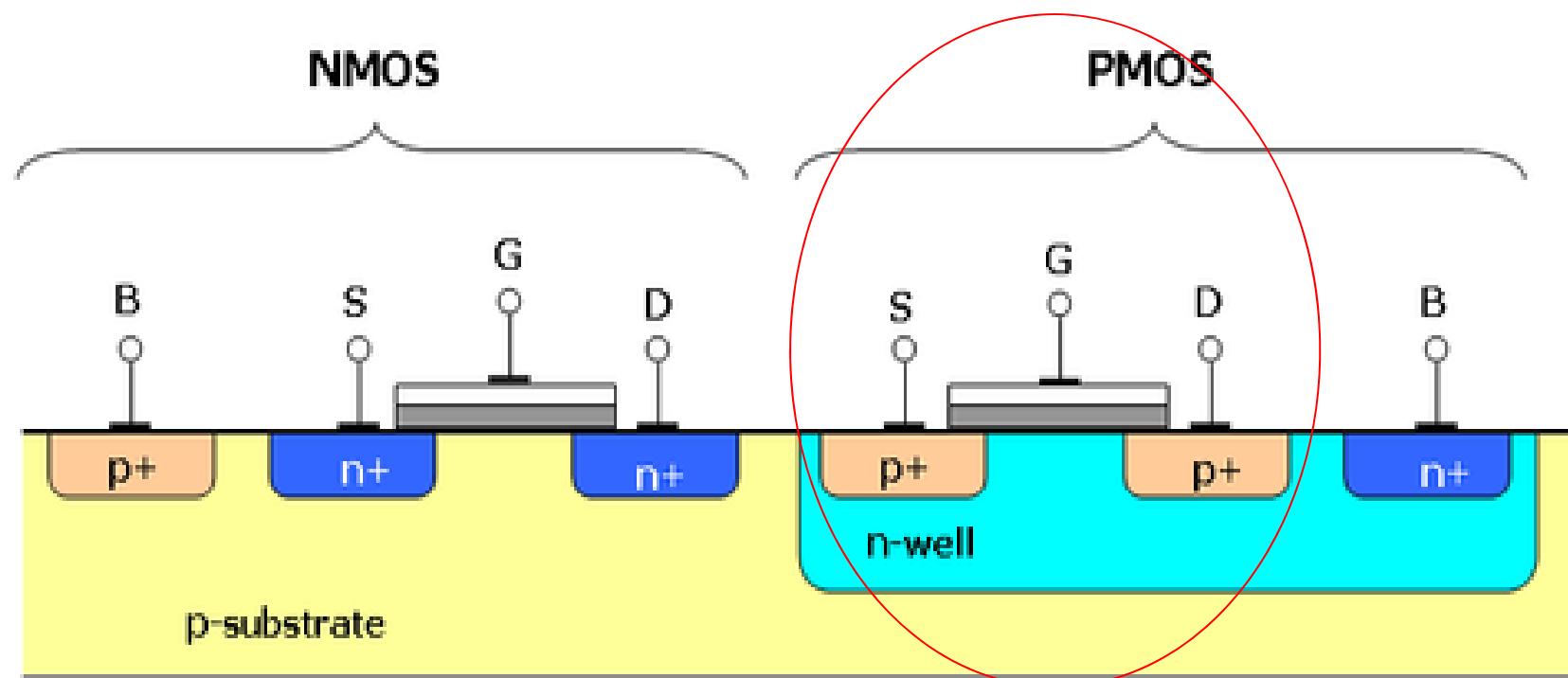
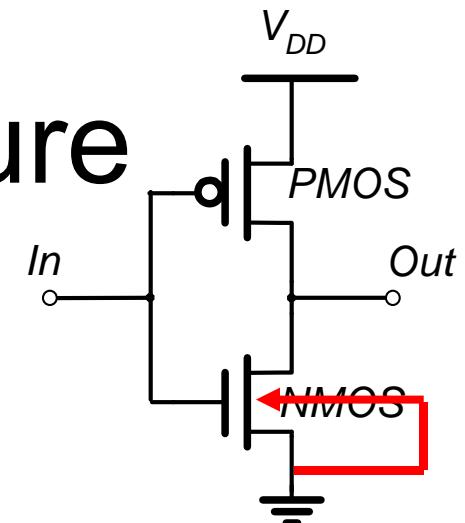
M6: contact

M7: metal

nMOSFET



CMOS basic structure



How to draw layouts:

7. Drawing a *p-active* layer **after calculation W/L**

M2: for
pMOSFET

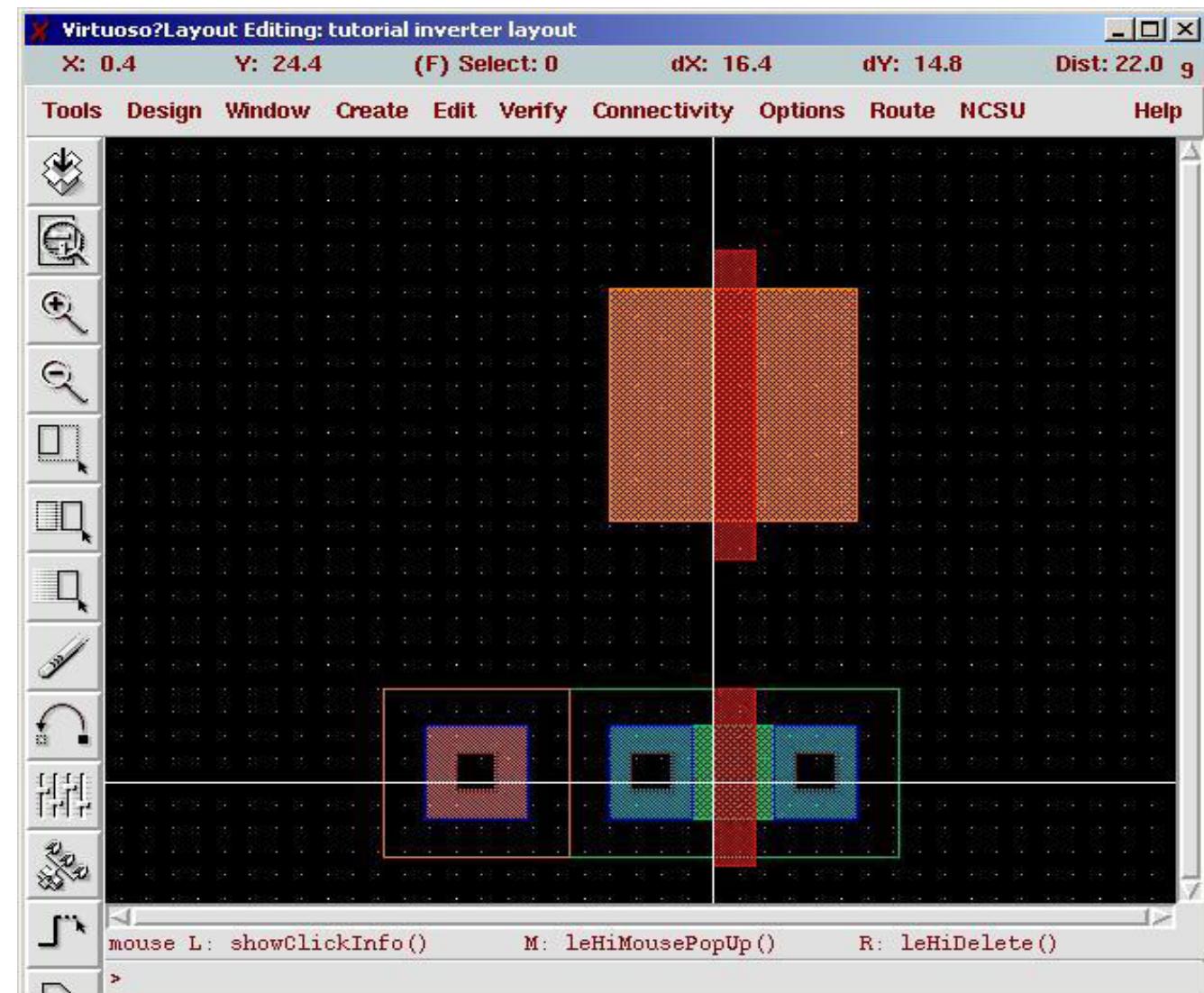


How to draw layouts:

8. Drawing Gate poly

M3: poly

pMOSFET

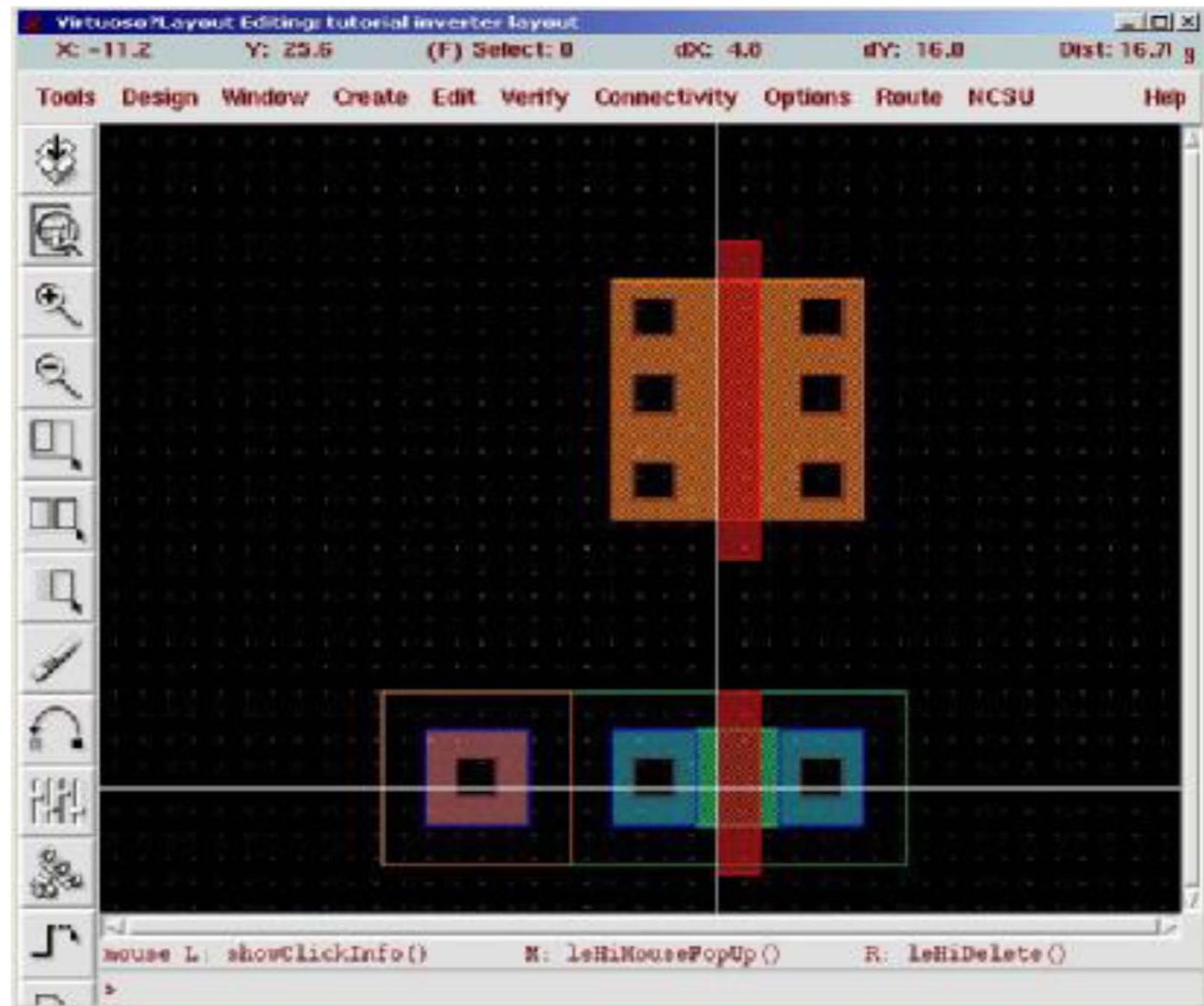


How to draw layouts:

9. Making active contacts (**cc**)

M6: contact

pMOSFET

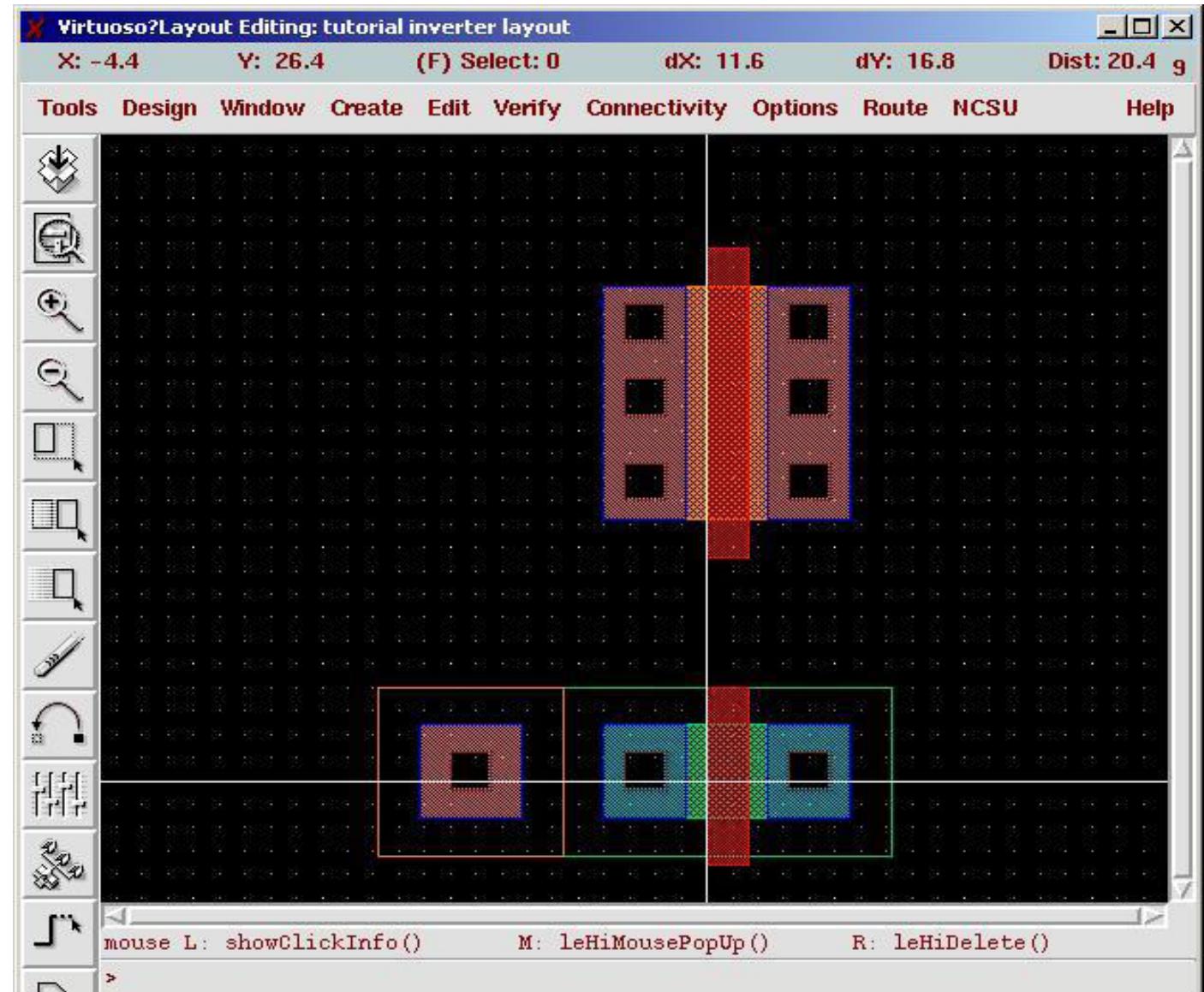


How to draw layouts:

10. Covering the contacts with metal-1

M7: metal

pMOSFET

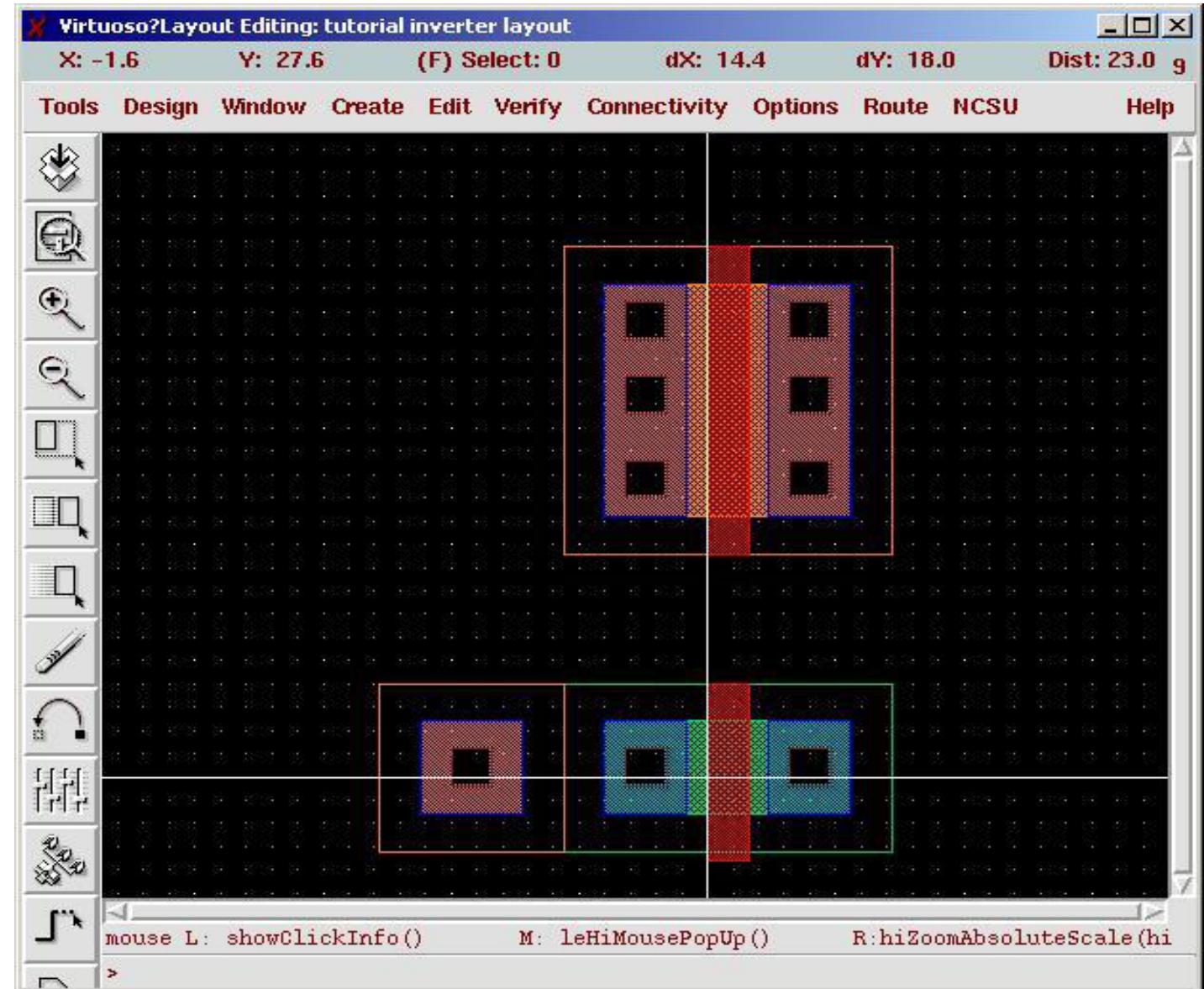


How to draw layouts:

11. Drawing p-select layer

M4: B⁺
implantation

pMOSFET

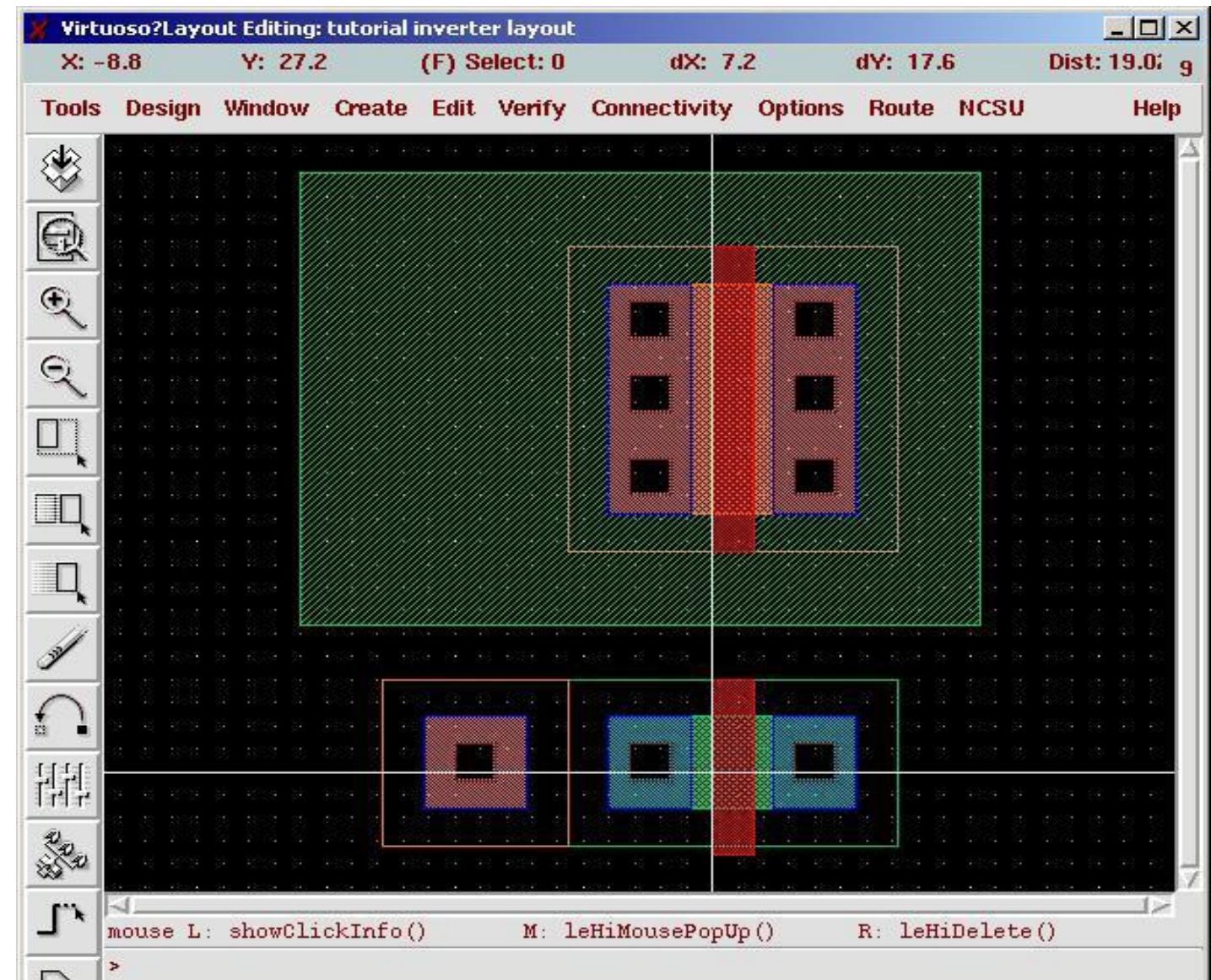


How to draw layouts:

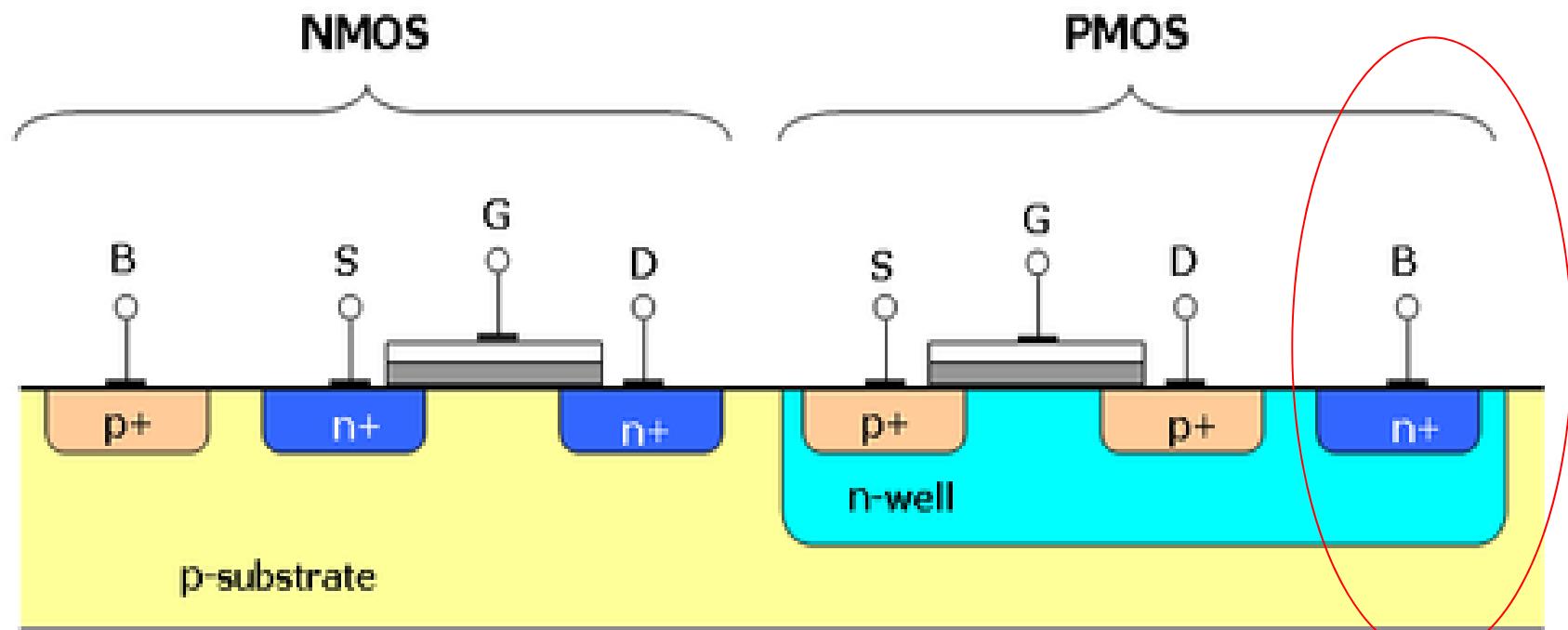
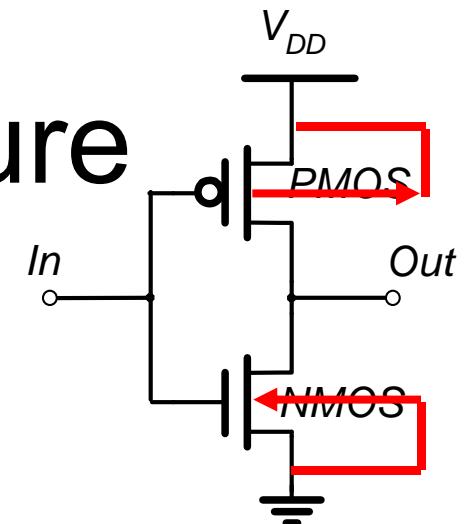
12. Drawing n-well layer

M1: n-well

pMOSFET



CMOS basic structure



How to draw layouts:

13. Drawing n-well contact

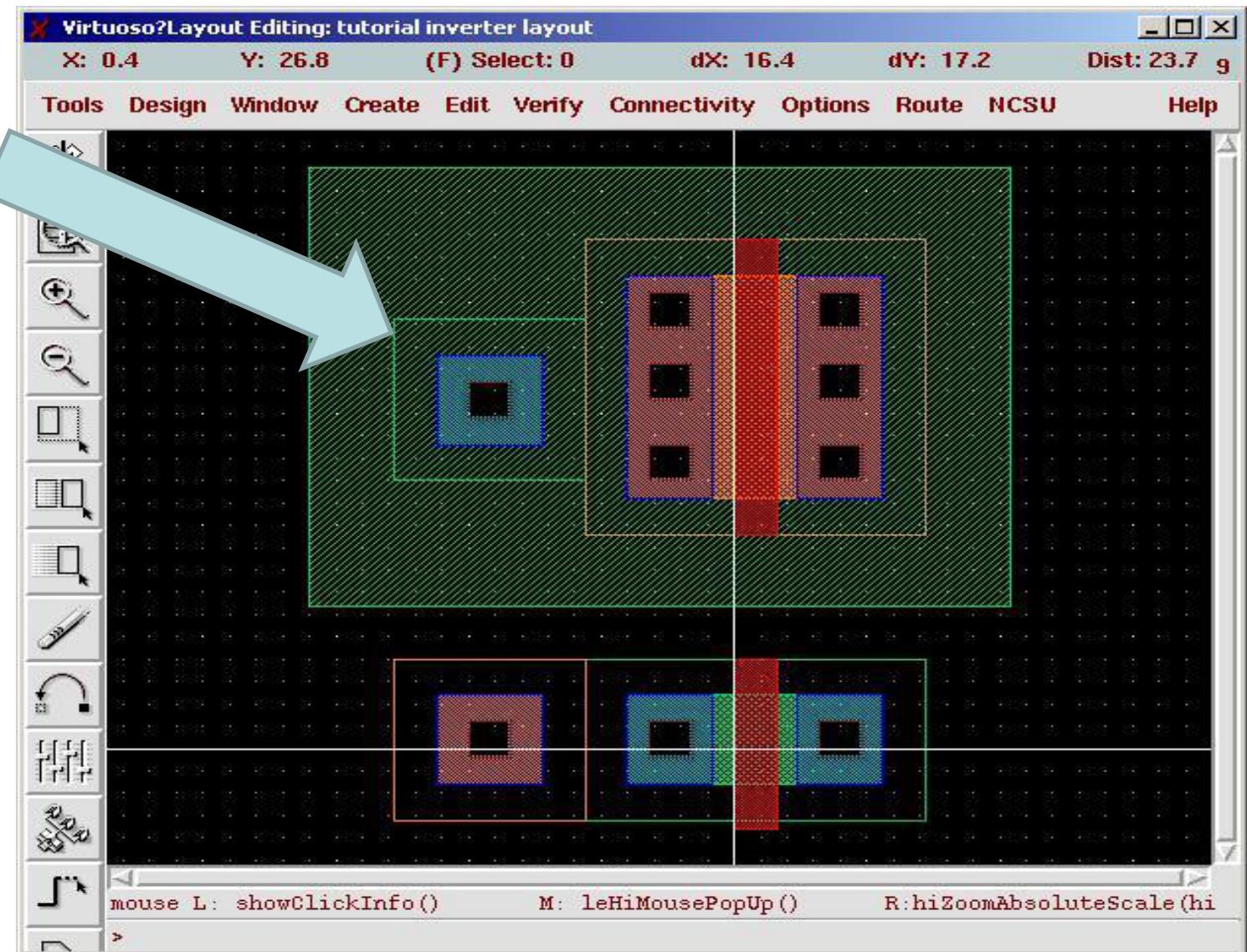
M5: As⁺

M2: active

M6: contact

M7: metal

pMOSFET

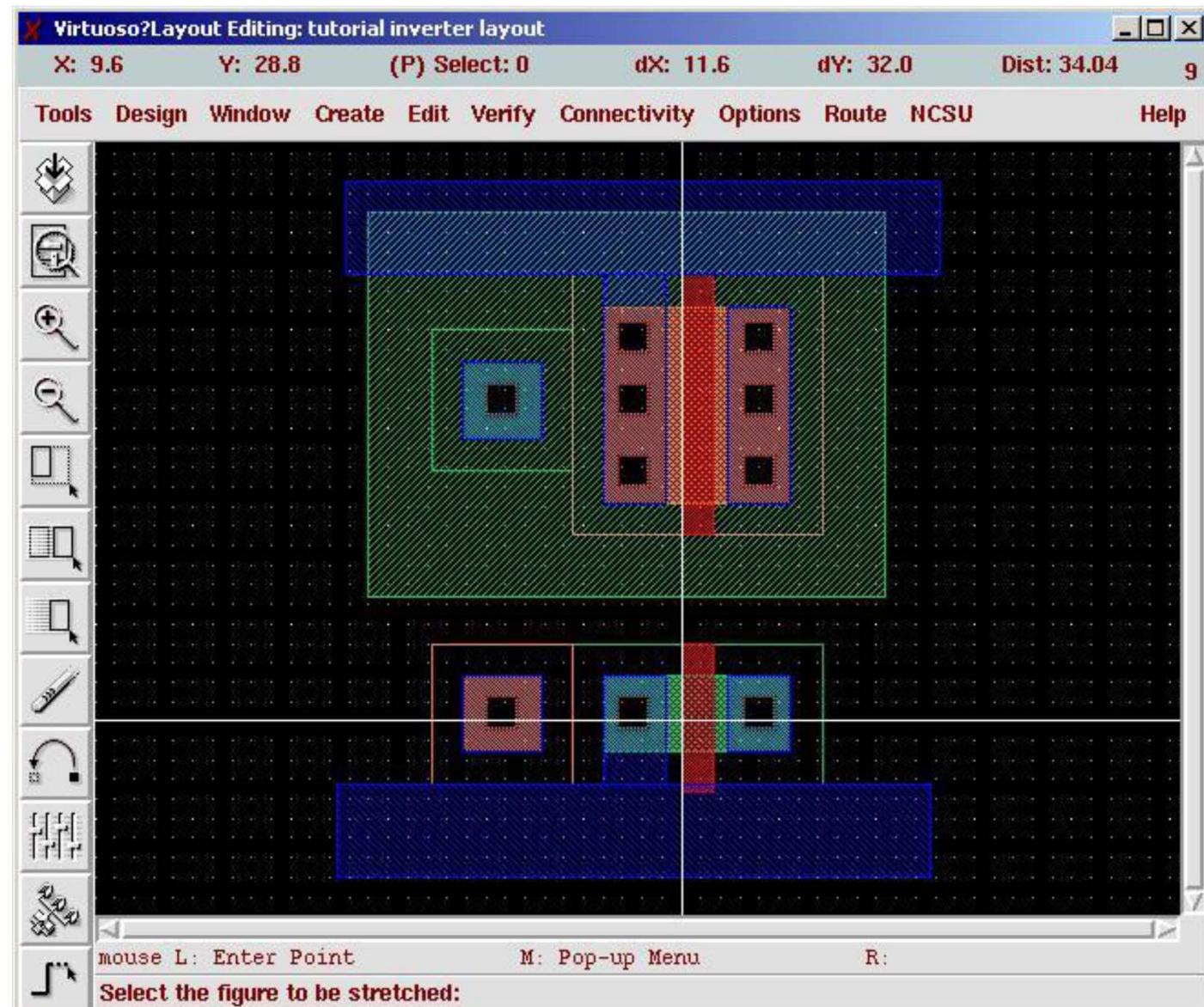


How to draw layouts:

14. Power Rails

M7: metal

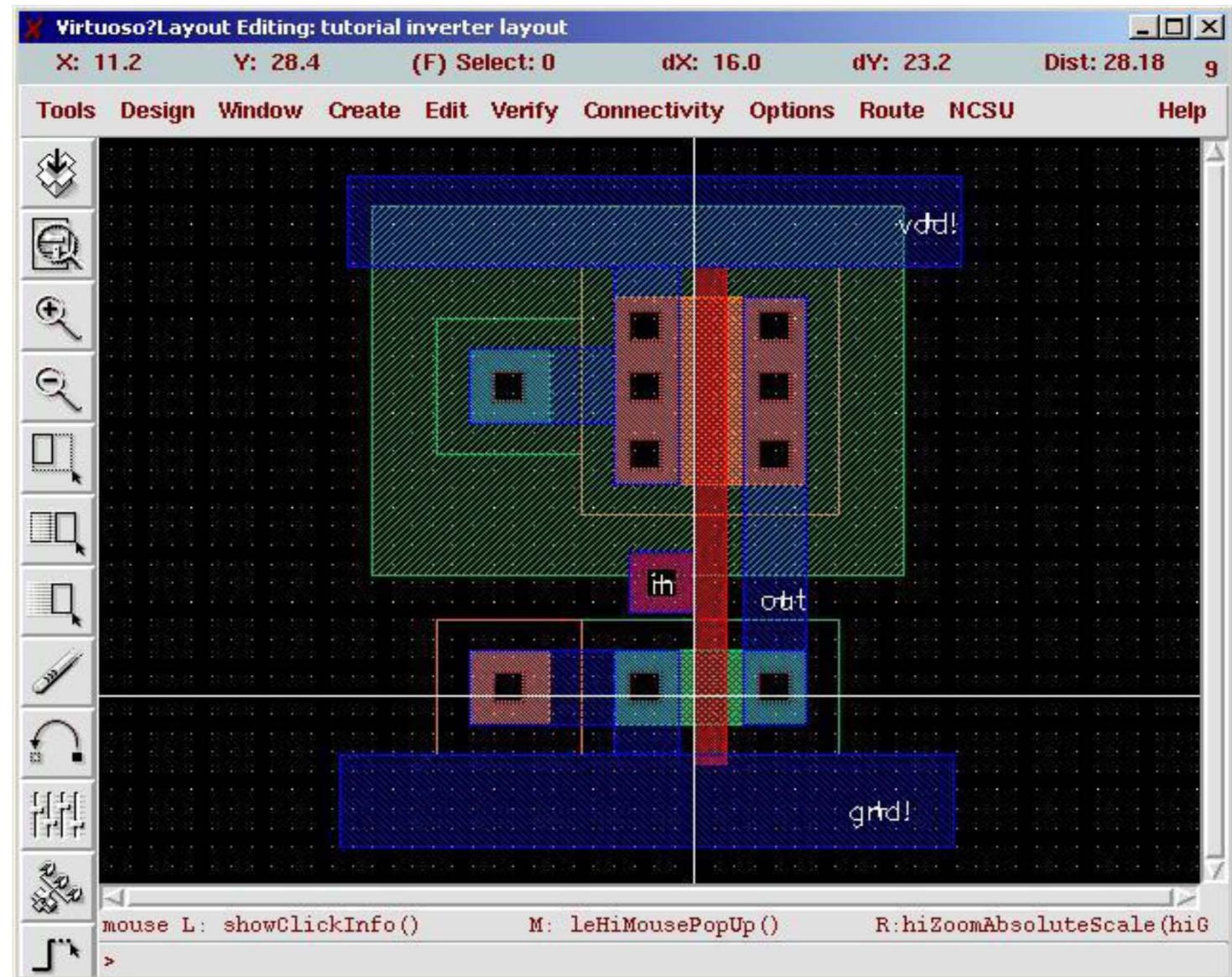
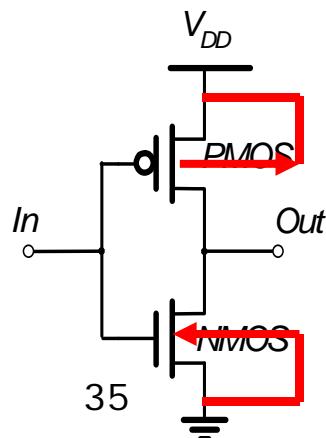
CMOS IC

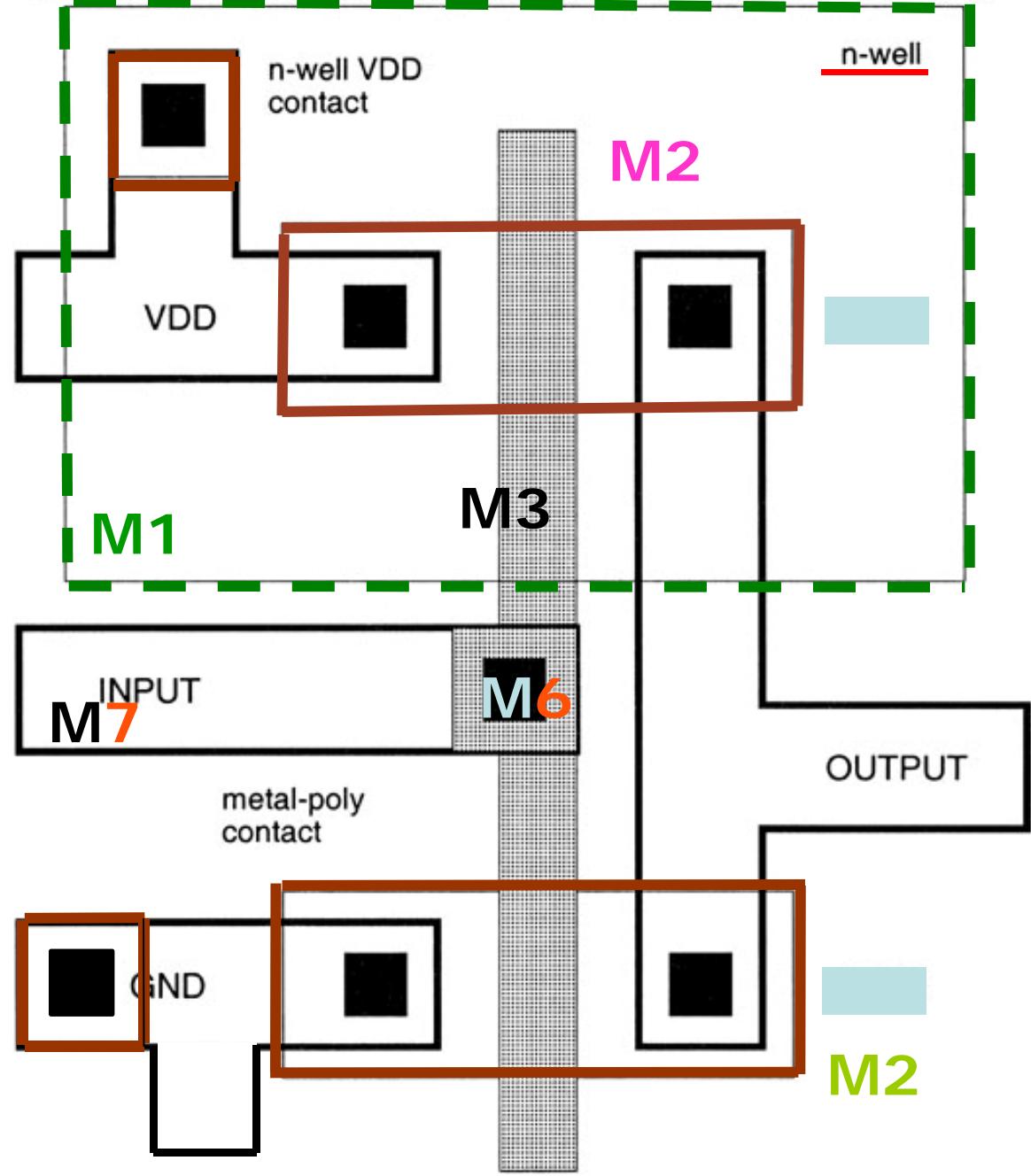
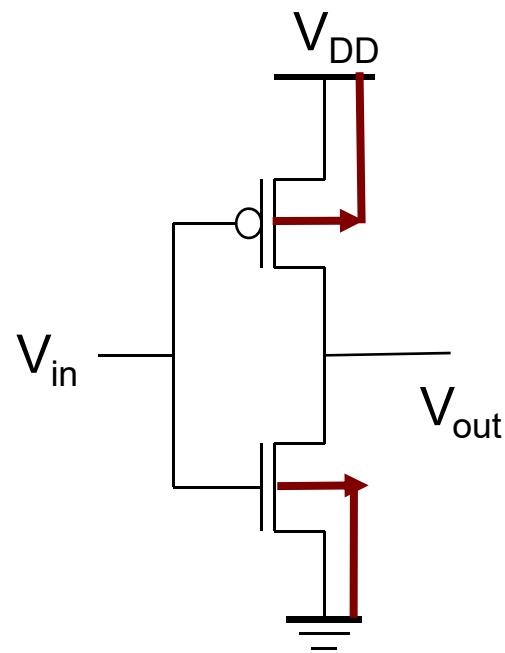


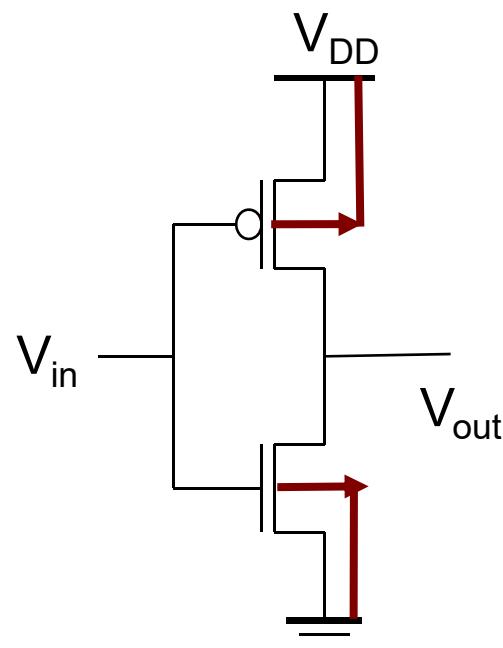
How to draw layouts:

14. Connections and Labels

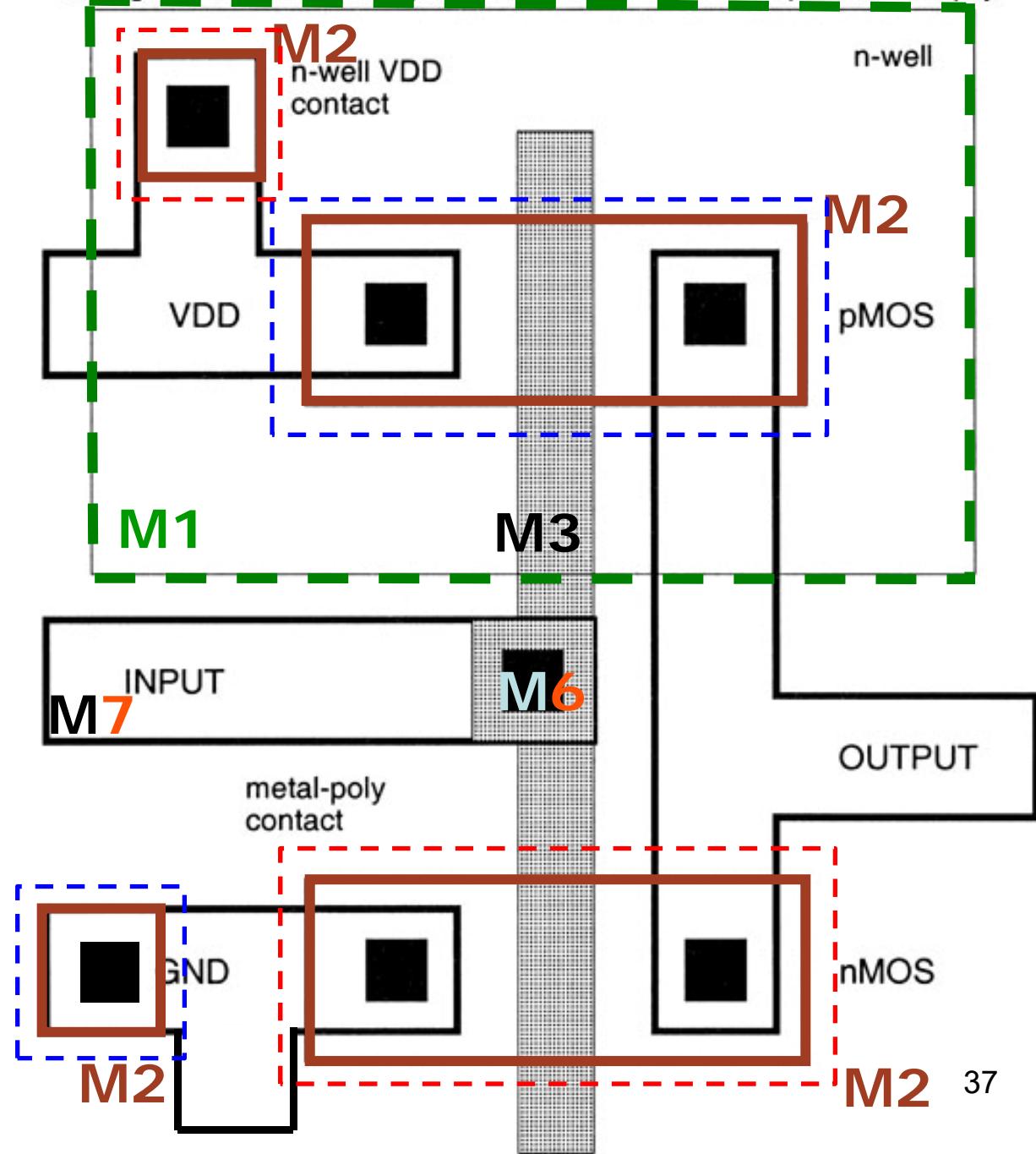
M3: poly
M6: contact
M7: metal







M4, M5





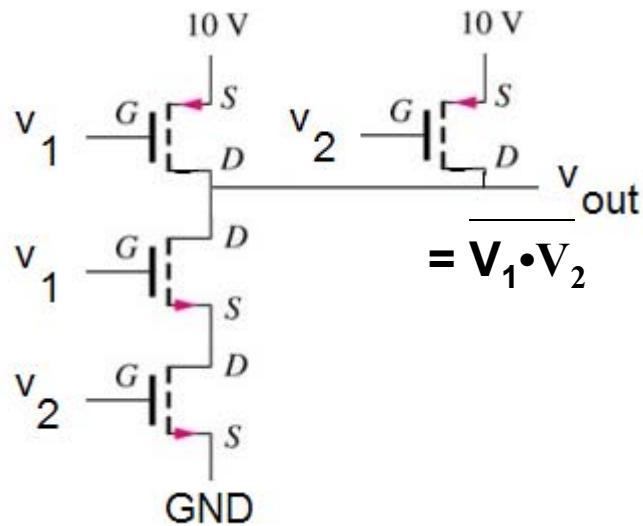
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CMOS logic family

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- NOR gates
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- General gates
 - Complicated gates

A CMOS NAND2 Gate

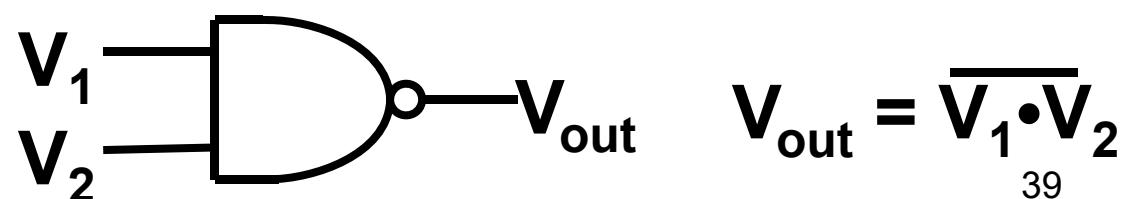


$V_1 = V_2 = 10V$ causes both NMOS transistors to be on and both PMOS transistors to be off. The high source-to-drain resistance of the parallel PMOS and the low drain-to-source resistance of the two NMOS in series form a voltage divider making V_{out} **nearly** 0V.

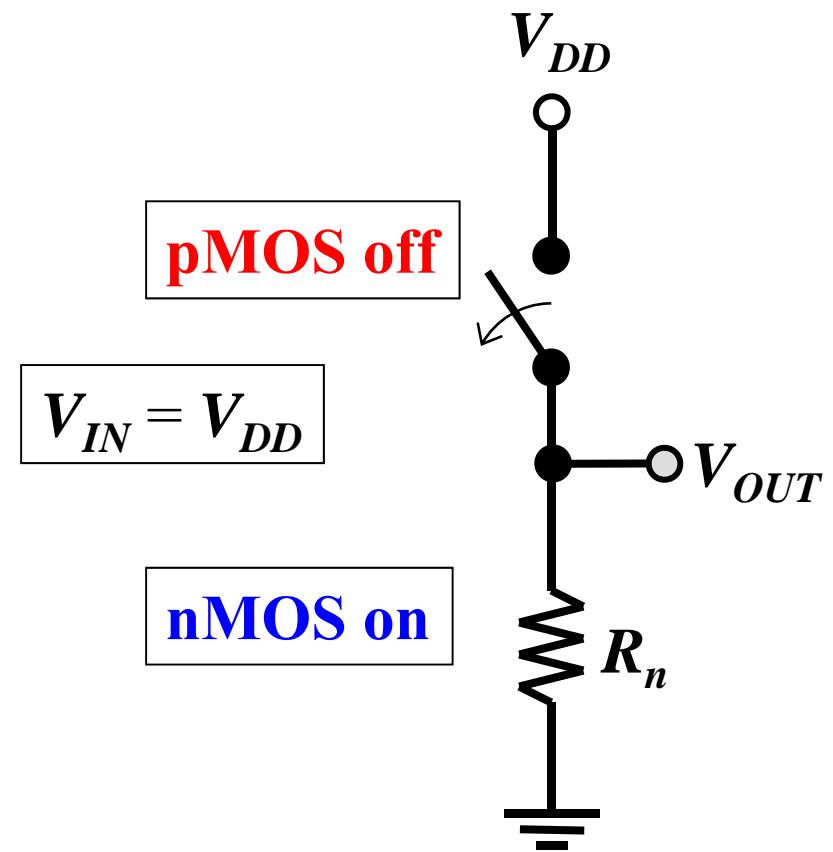
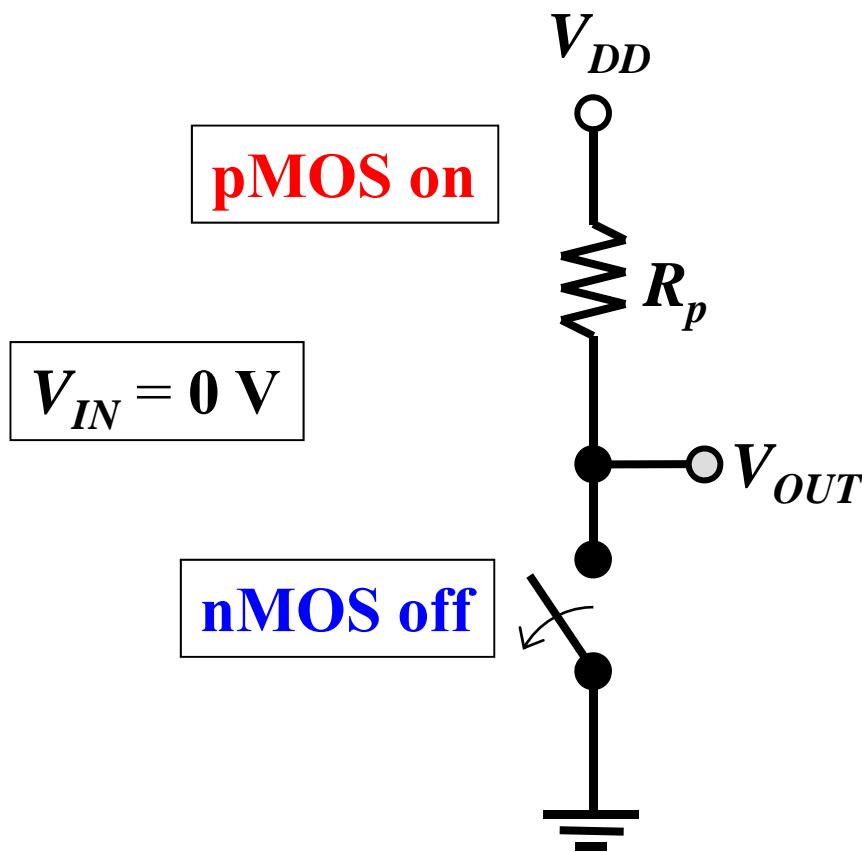
$V_1 = 0V$ or $V_2 = 0V$ (or both) cause one or both NMOS transistors to be off and one or both PMOS transistors to be on. The low resistance of the parallel PMOS and the high resistance of series NMOS cause a voltage divider to give V_{out} nearly 10V.

P 1.92

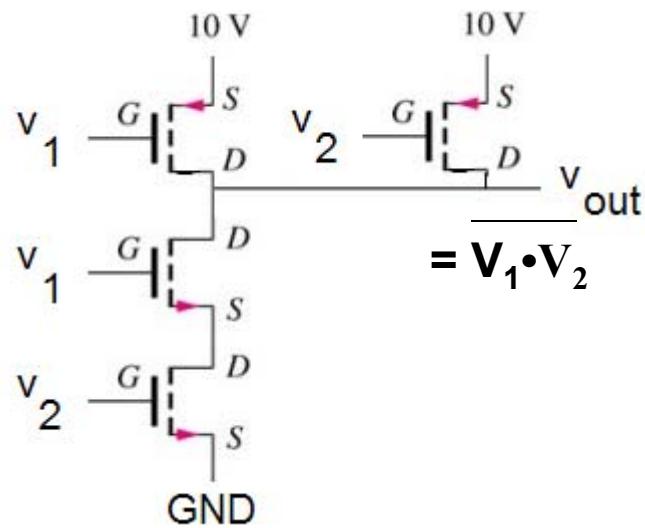
N 0.48



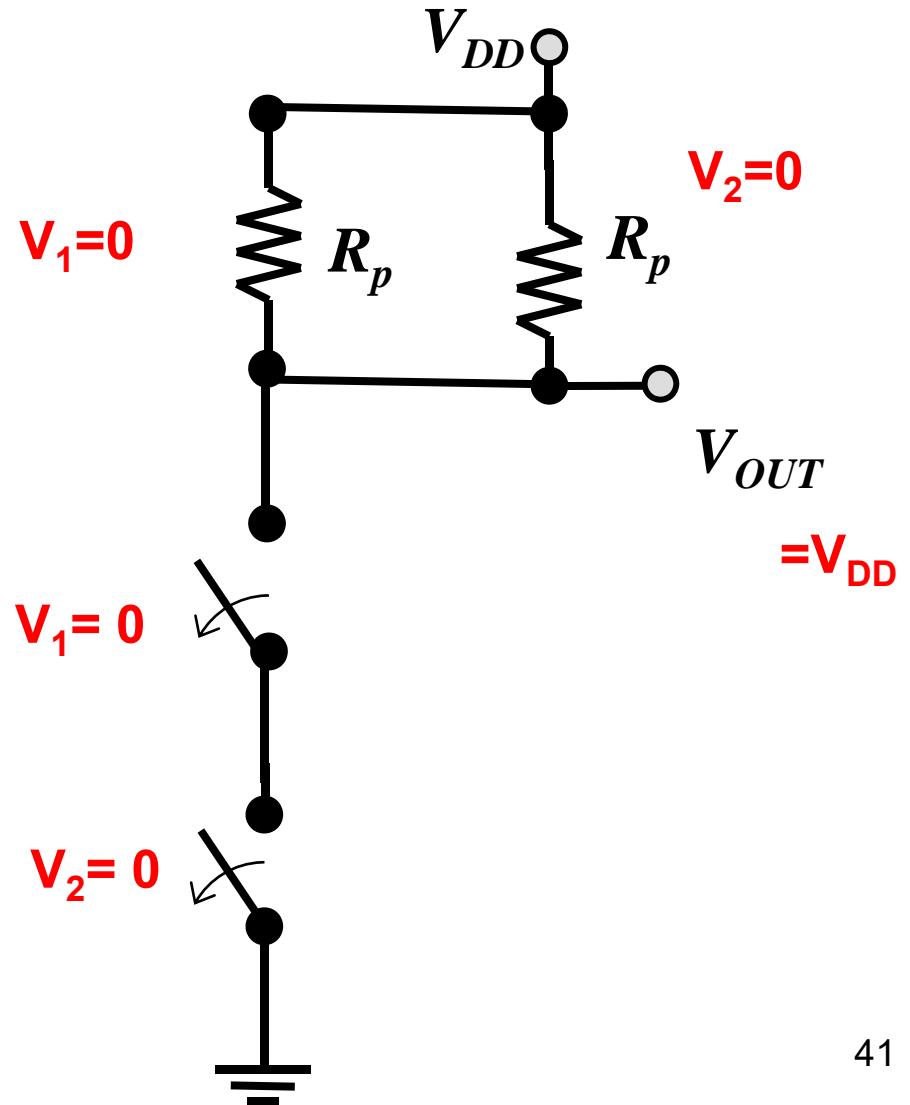
The CMOS Inverter: Intuitive Perspective



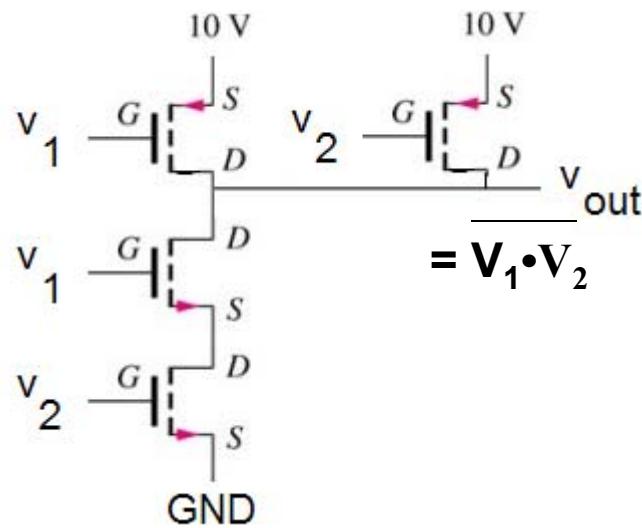
A CMOS NAND2 Gate



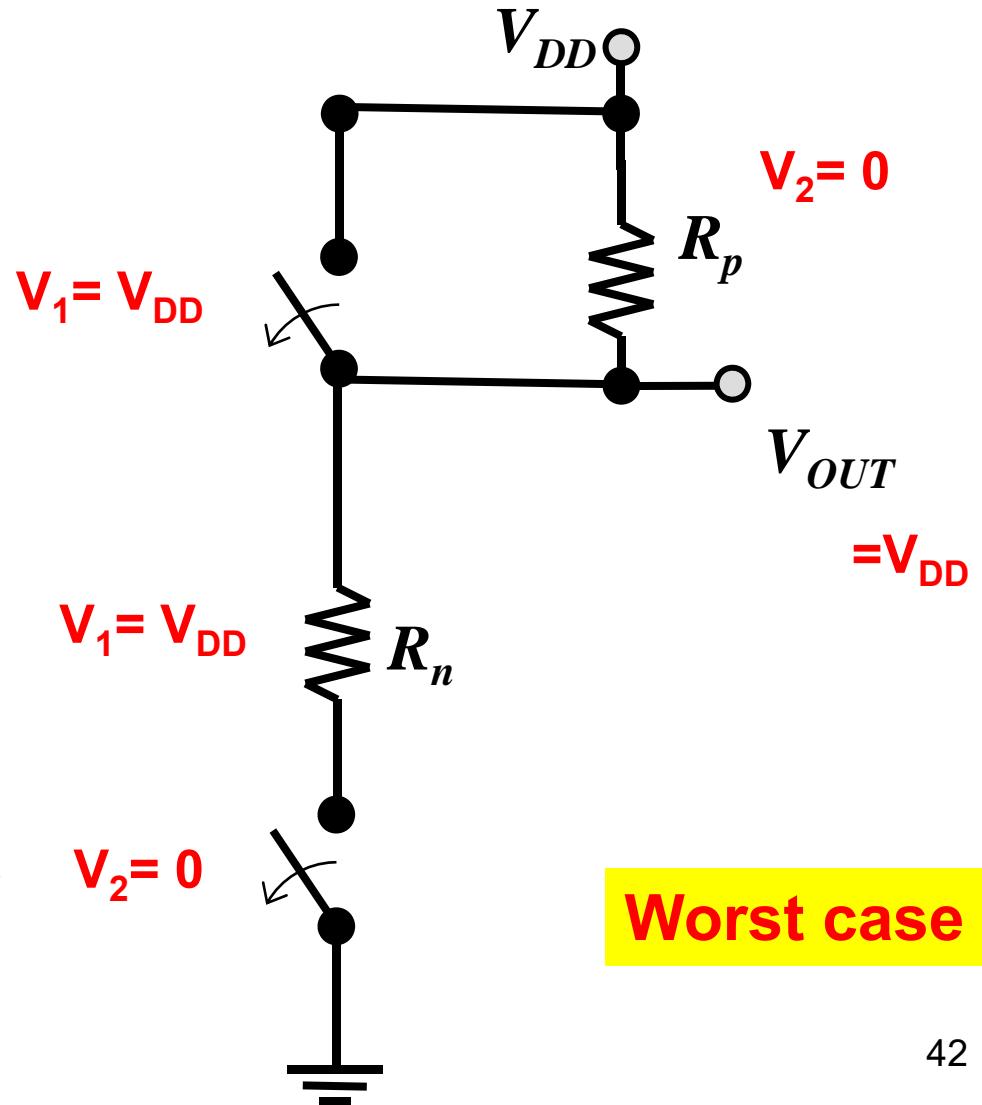
V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0



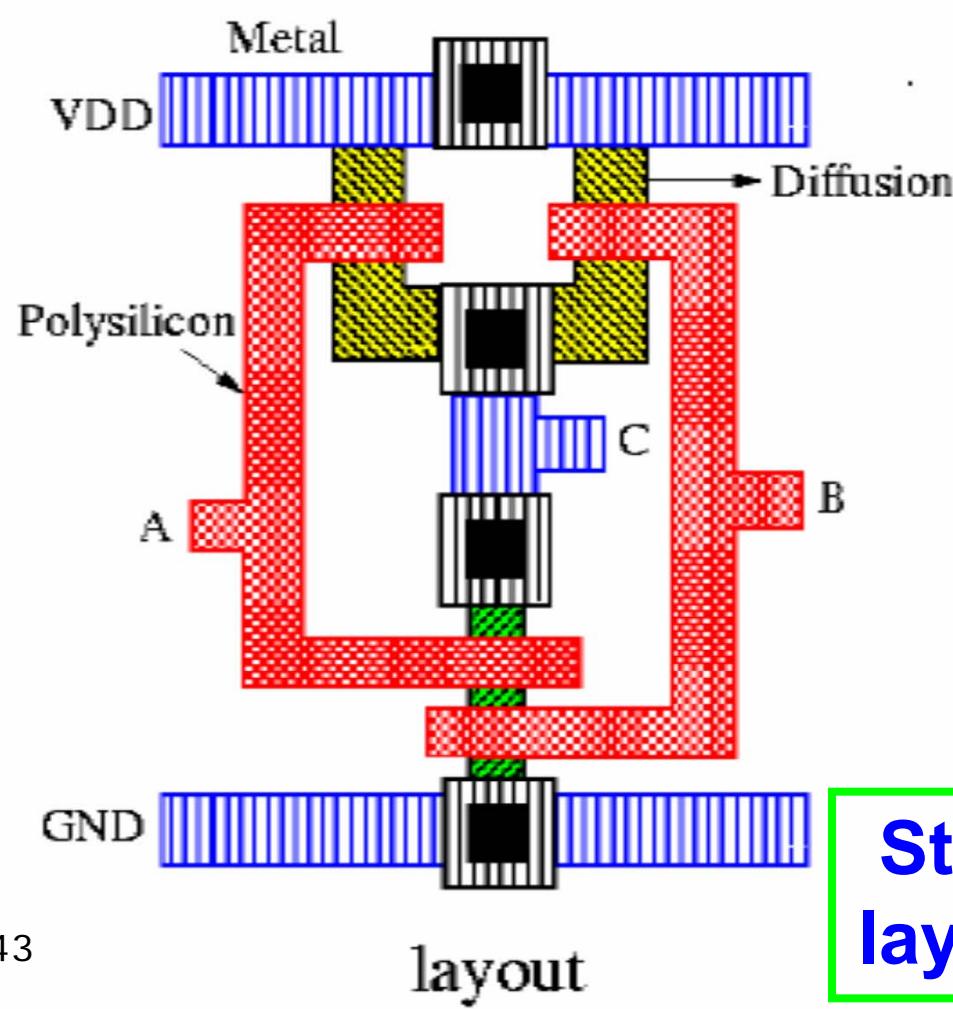
A CMOS NAND2 Gate



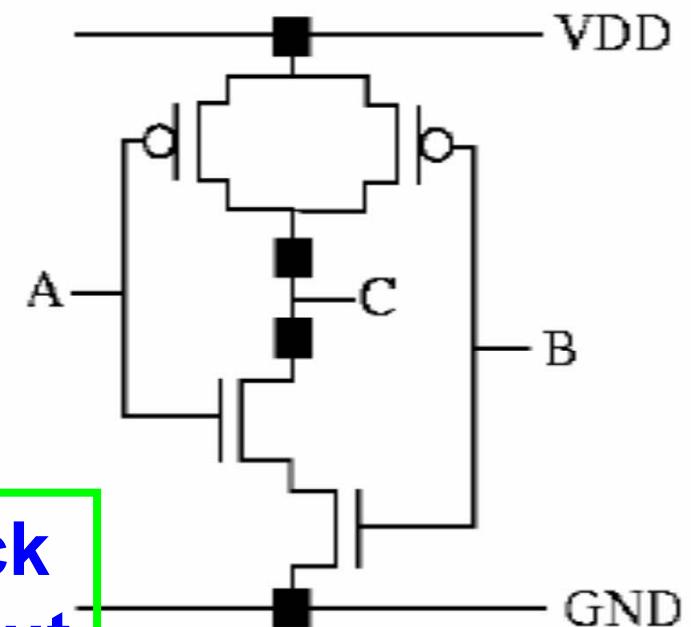
V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0



A CMOS NAND2 Gate: layout



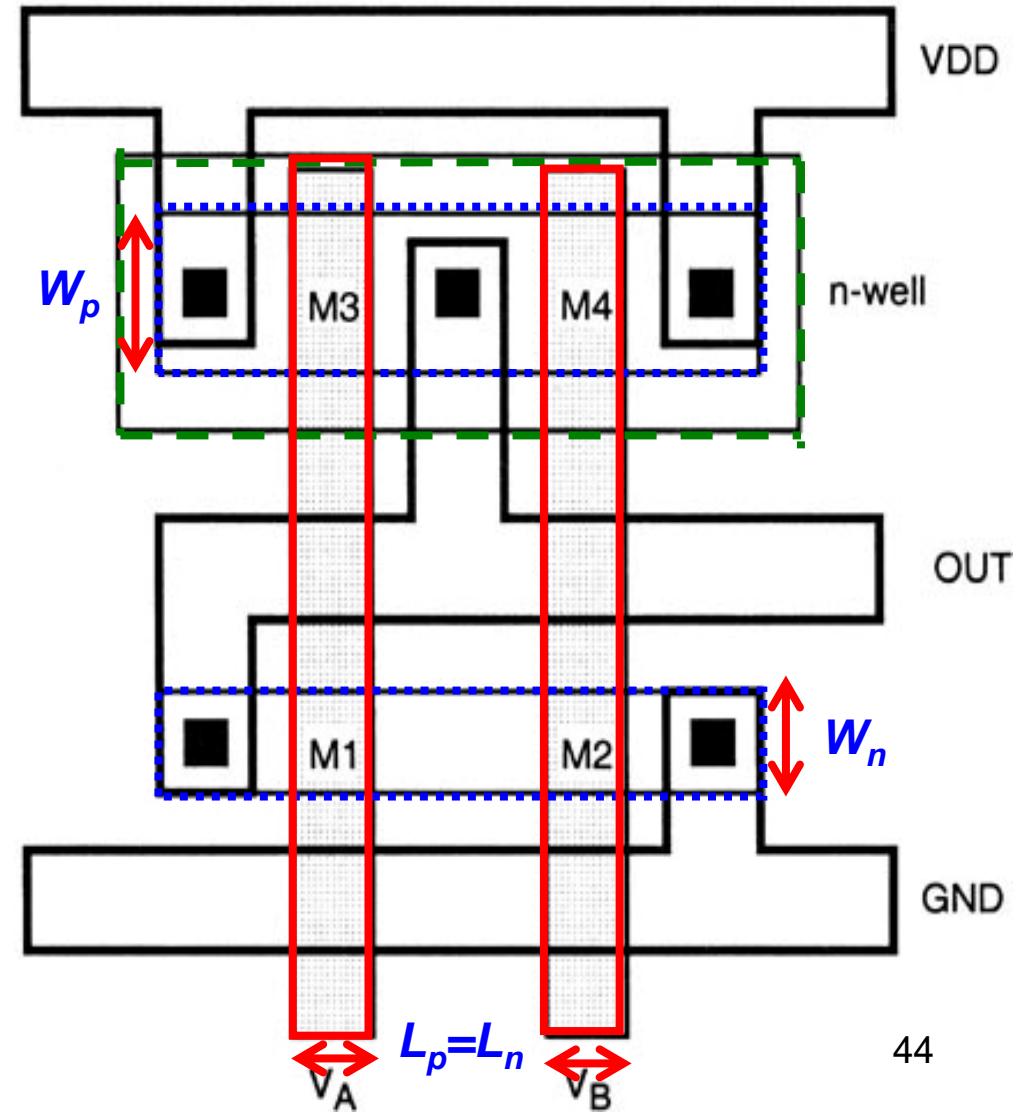
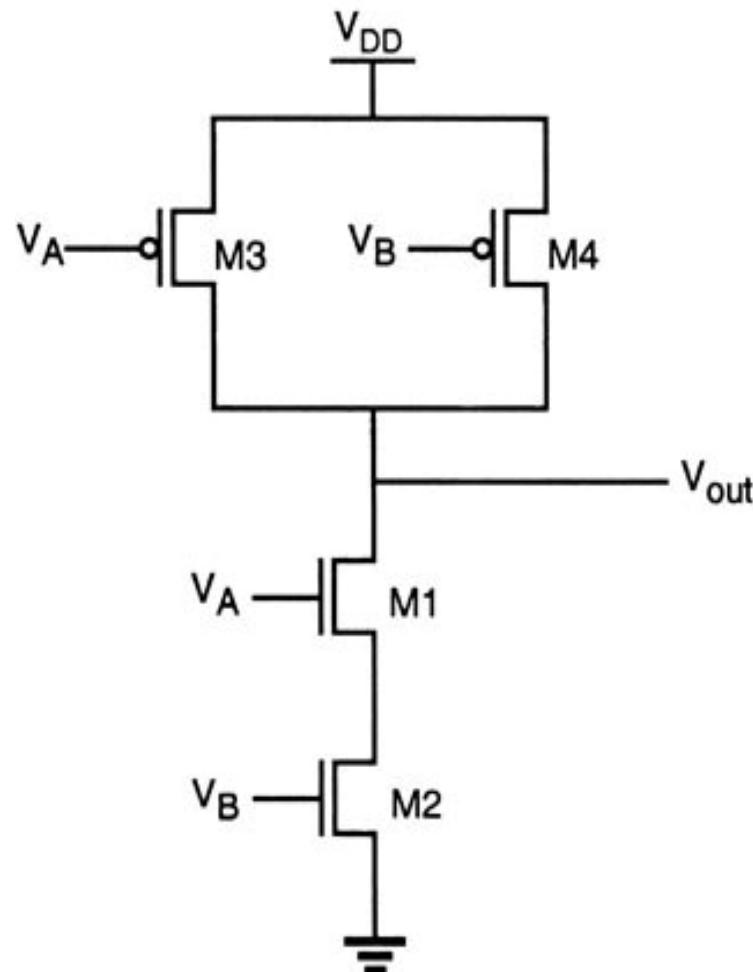
in1	in2	out
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0



Stick
layout

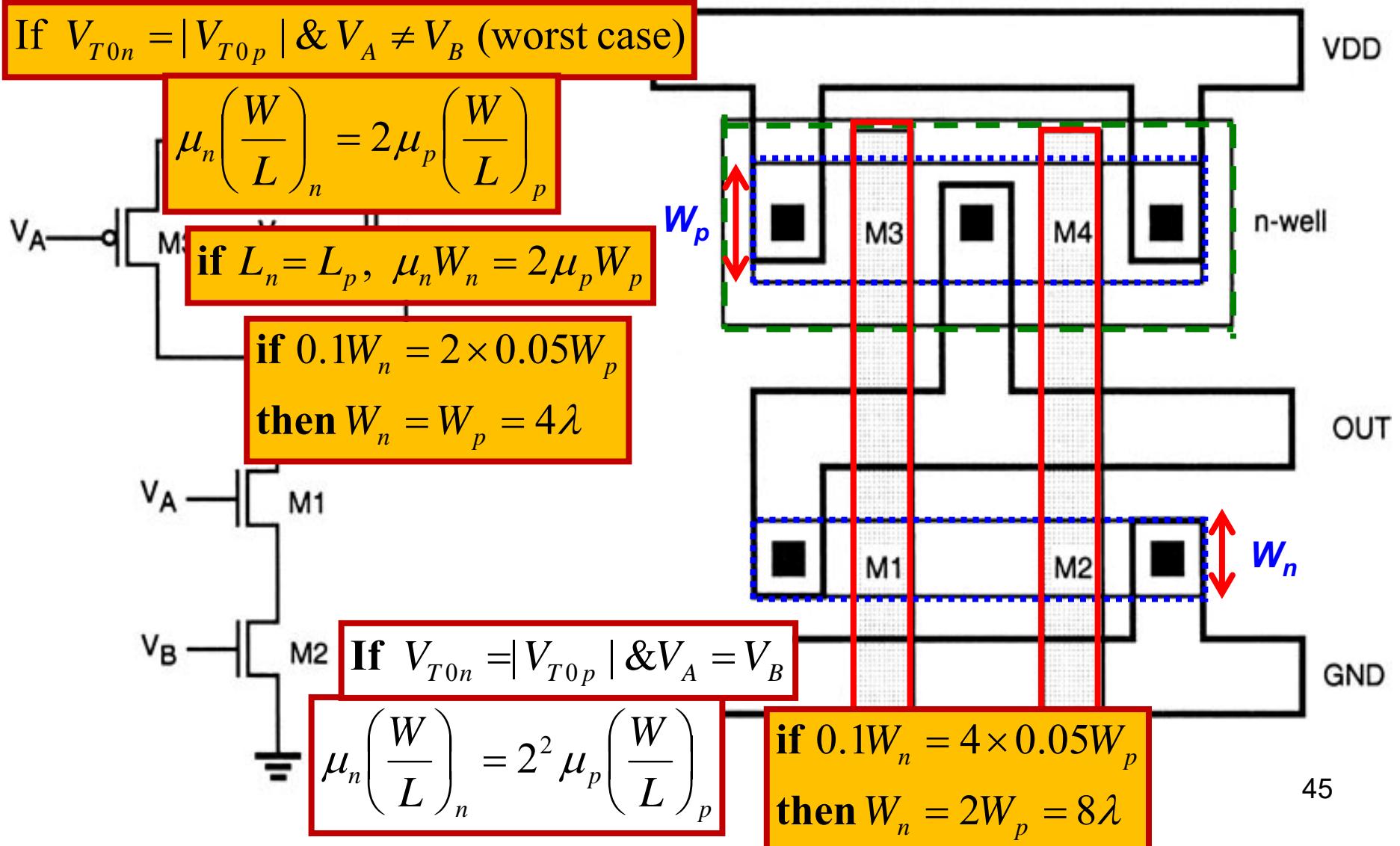
A CMOS NAND2 Gate: layout

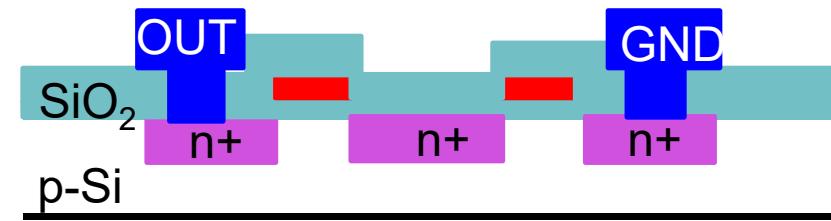
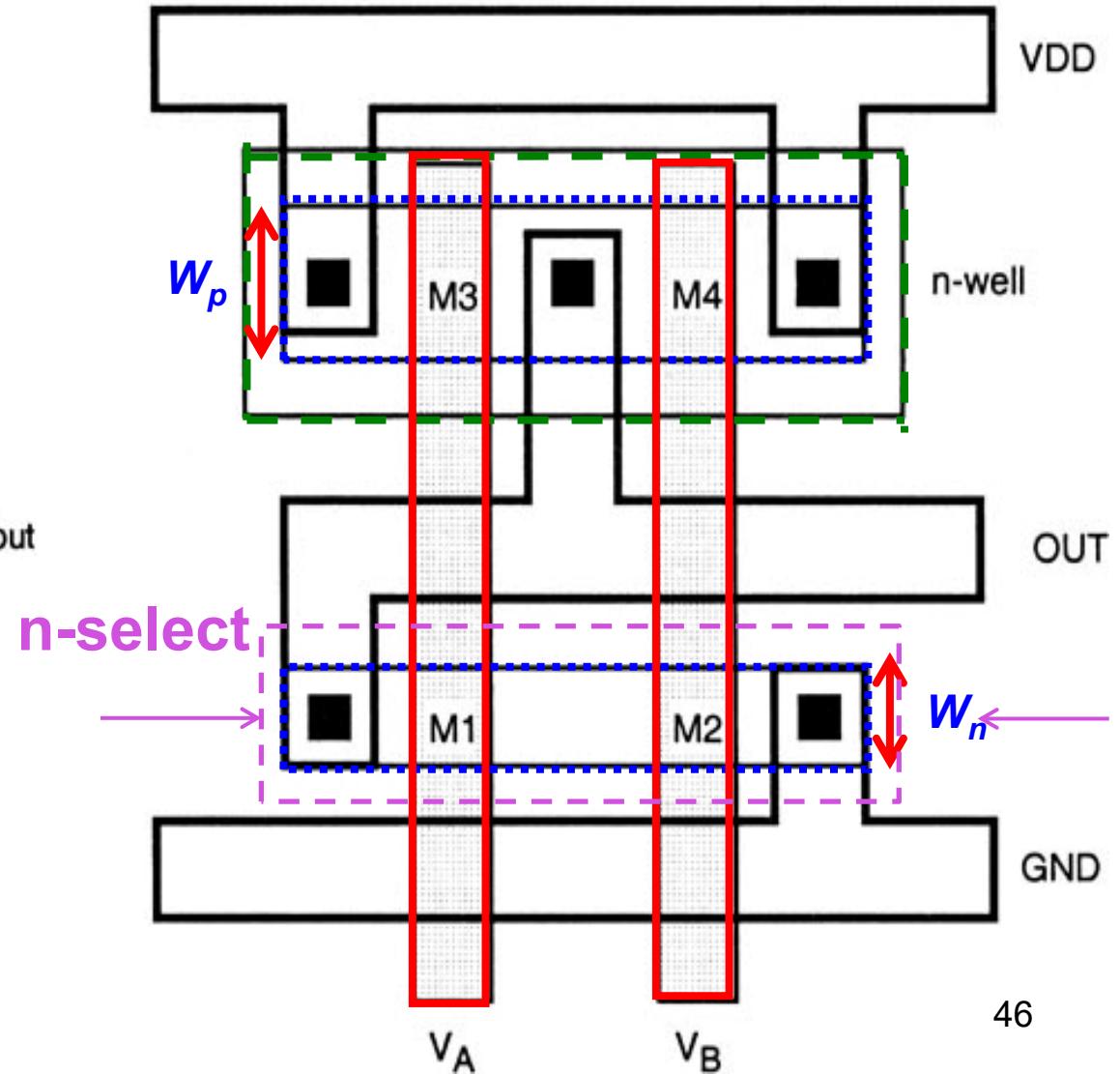
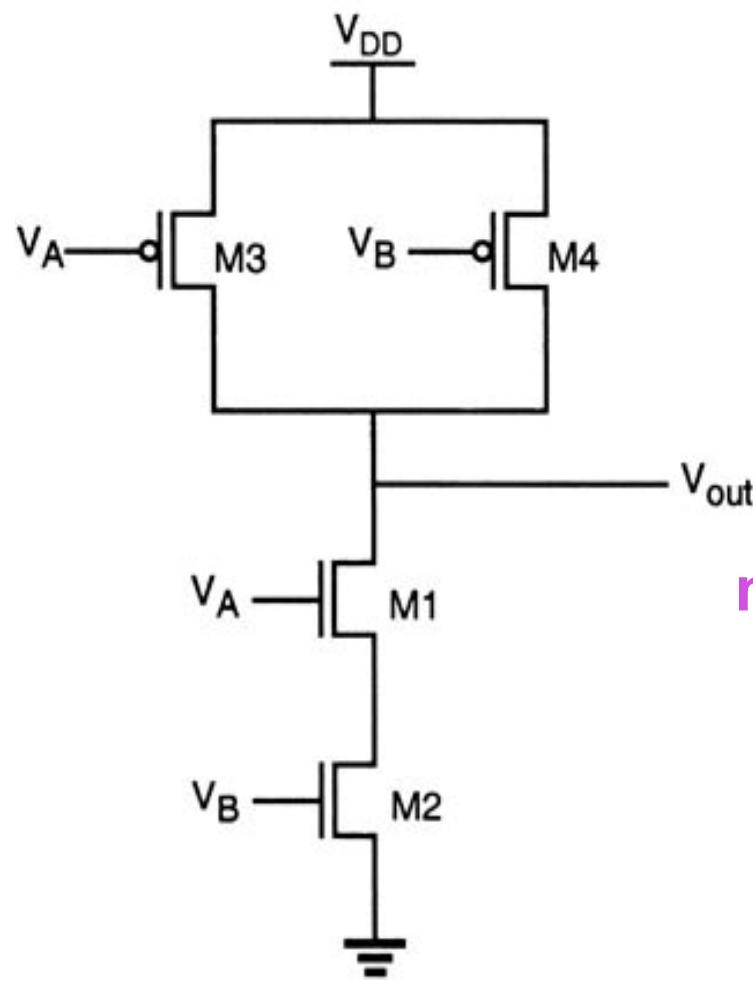
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A CMOS NAND2 Gate: layout

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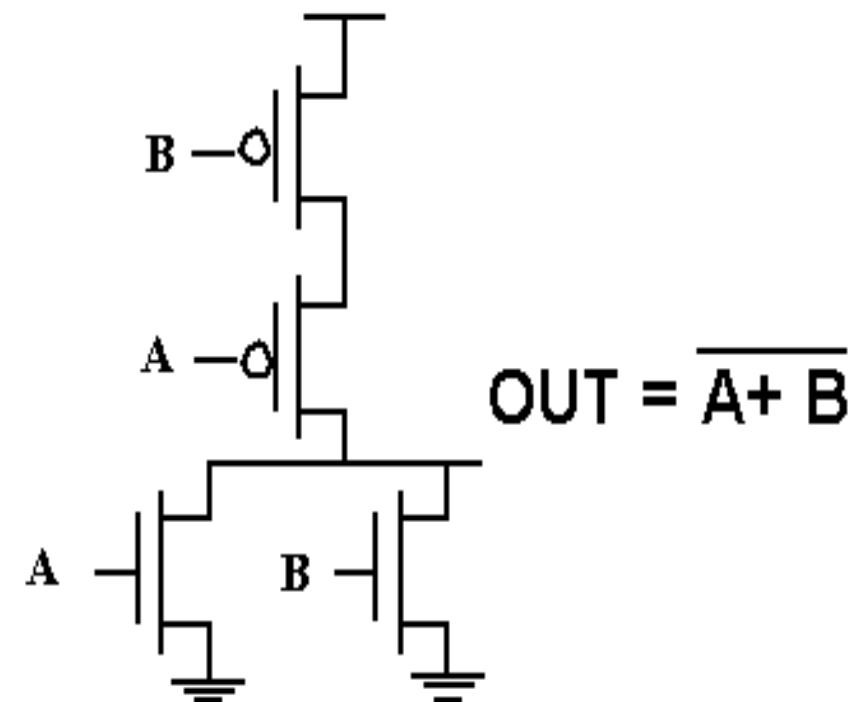


46

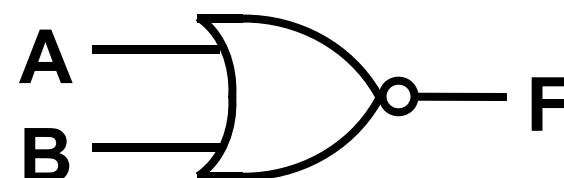
A CMOS NOR2 Gate

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

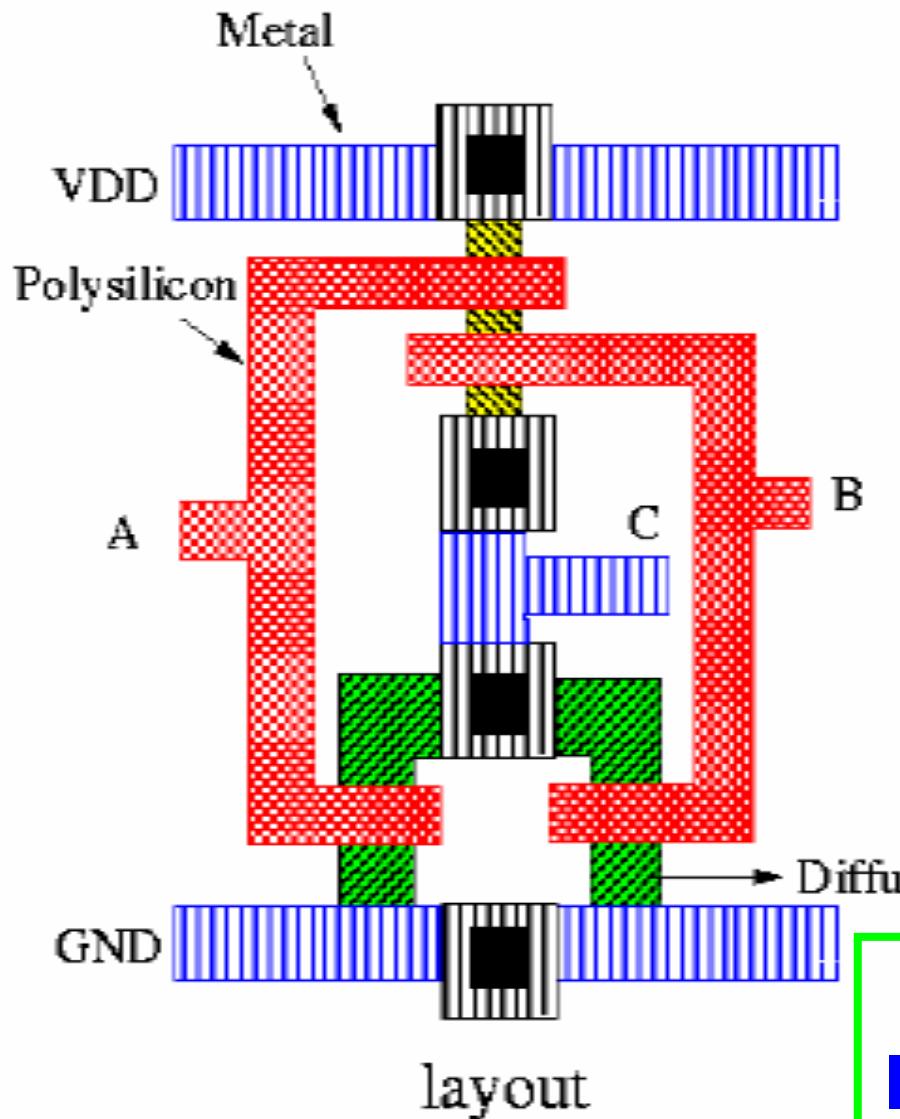
Truth Table of a 2 input NOR gate



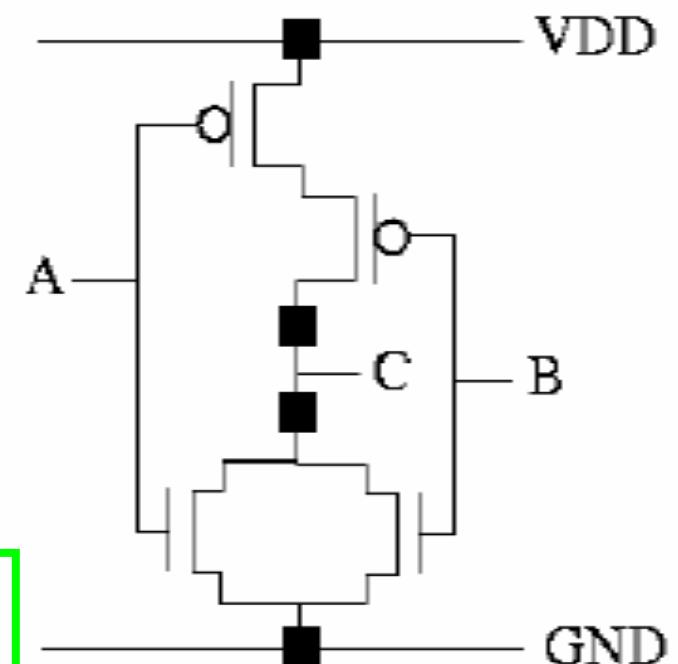
$$F = \overline{A+B}$$



A CMOS NOR2 Gate

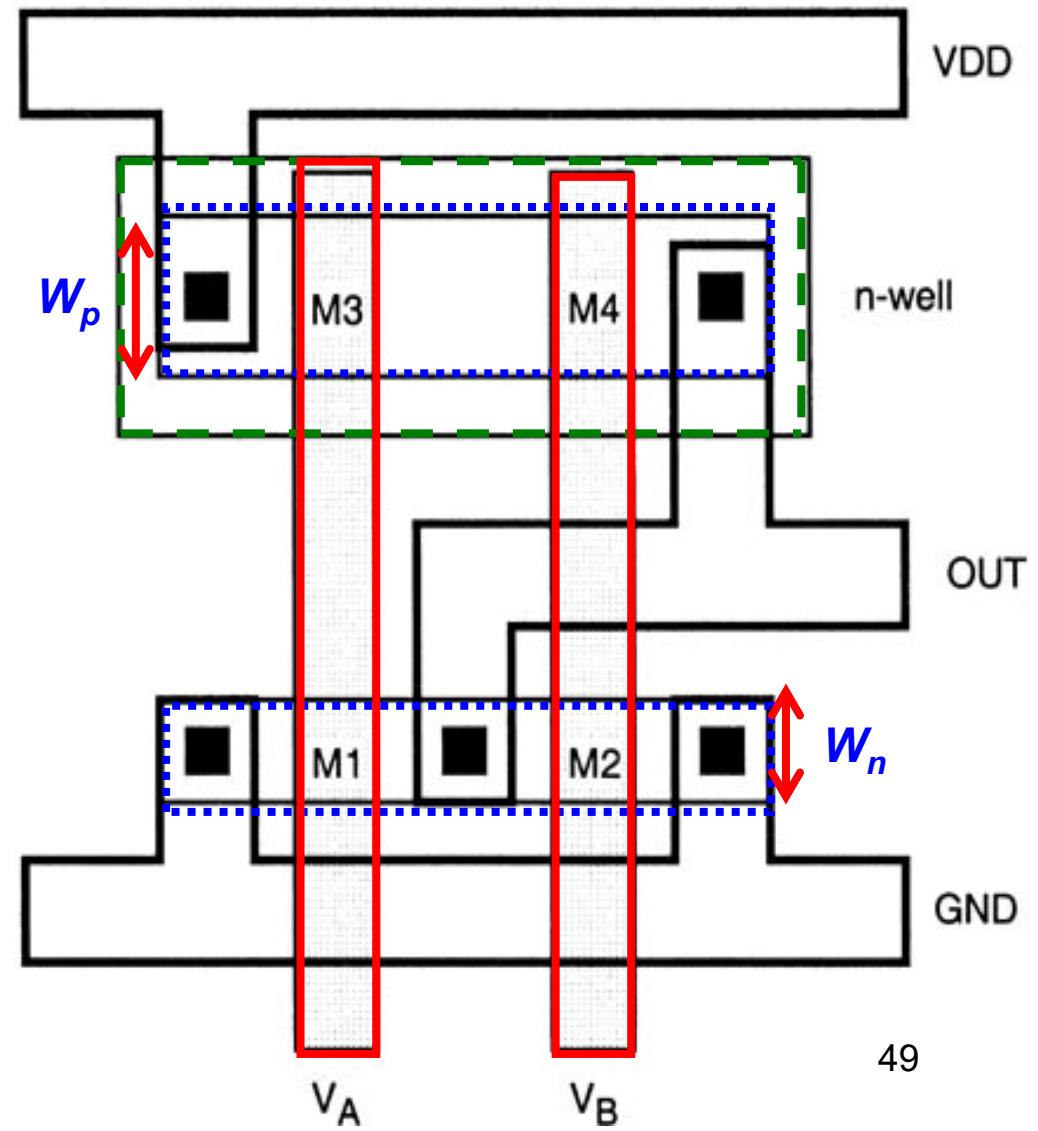
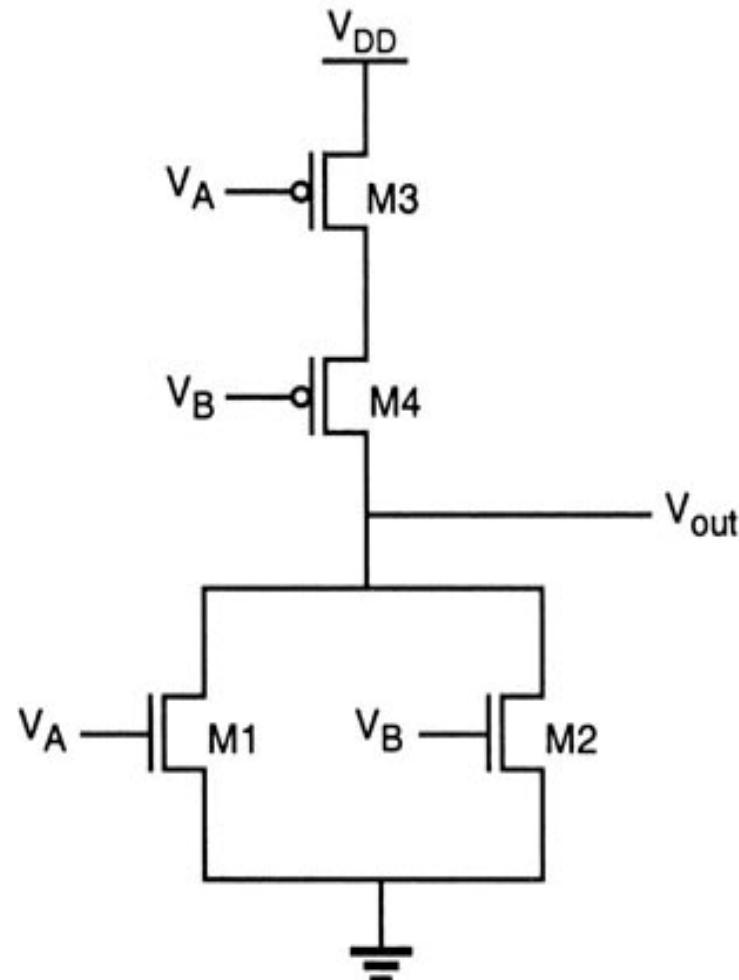


A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



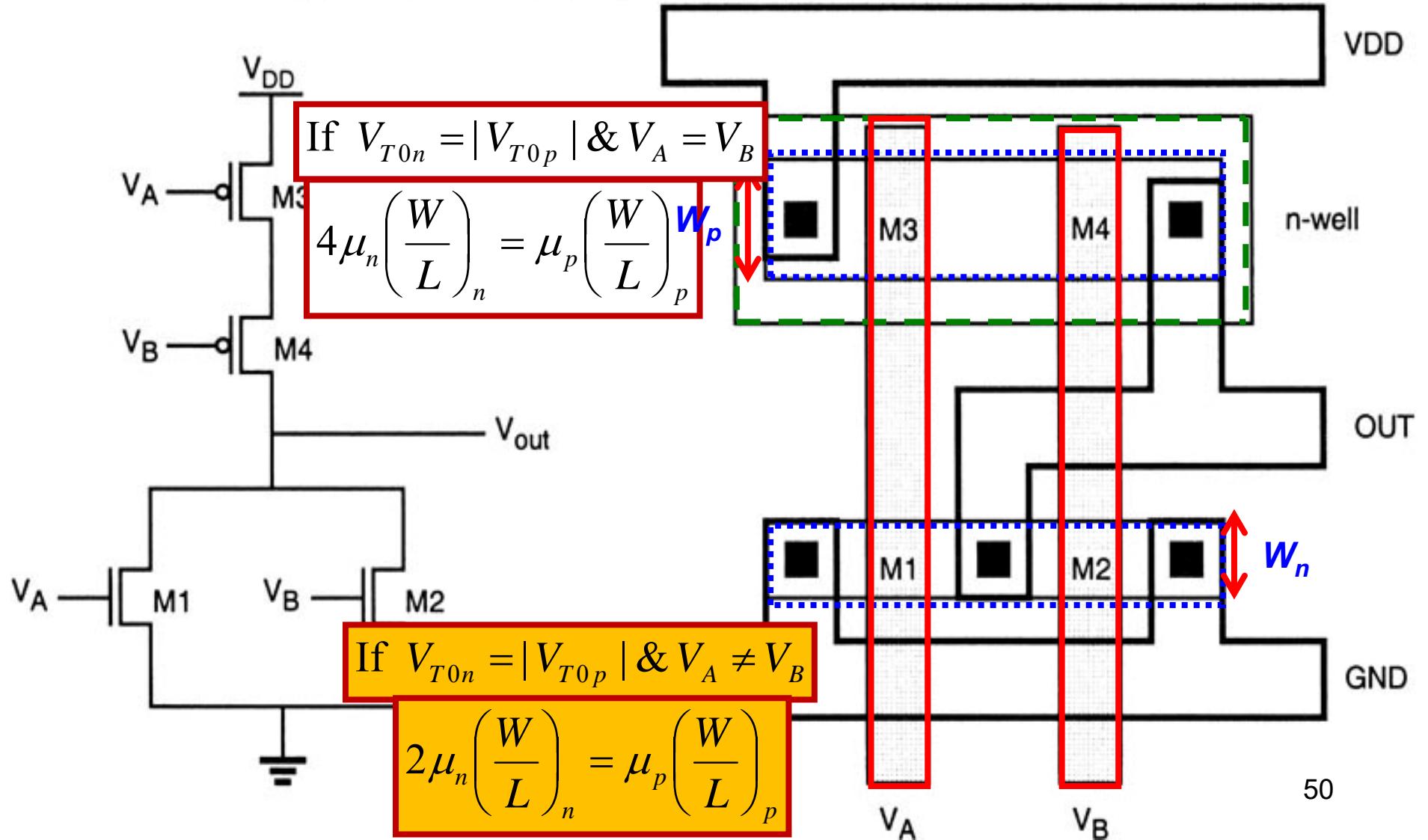
A CMOS NOR2 Gate

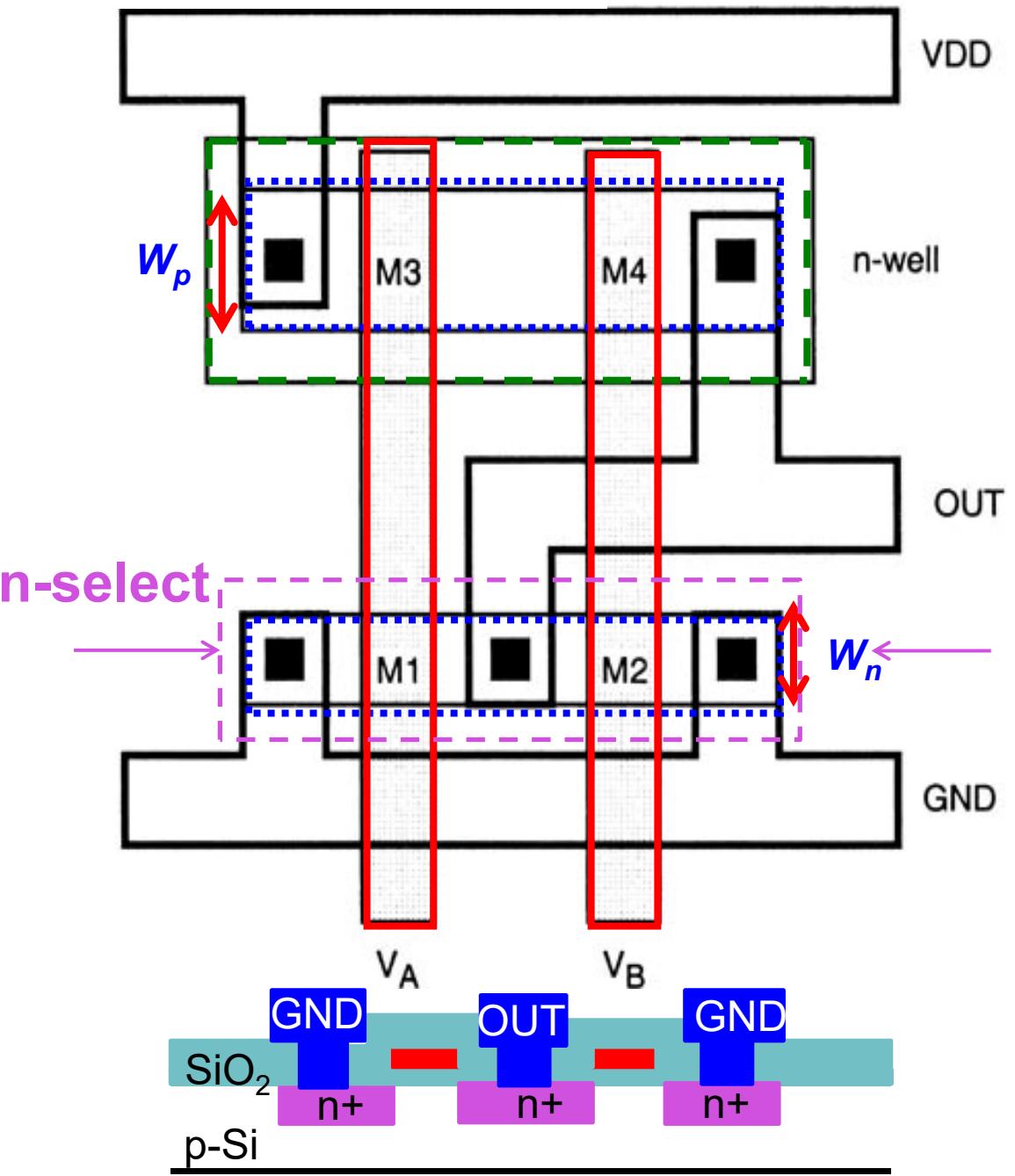
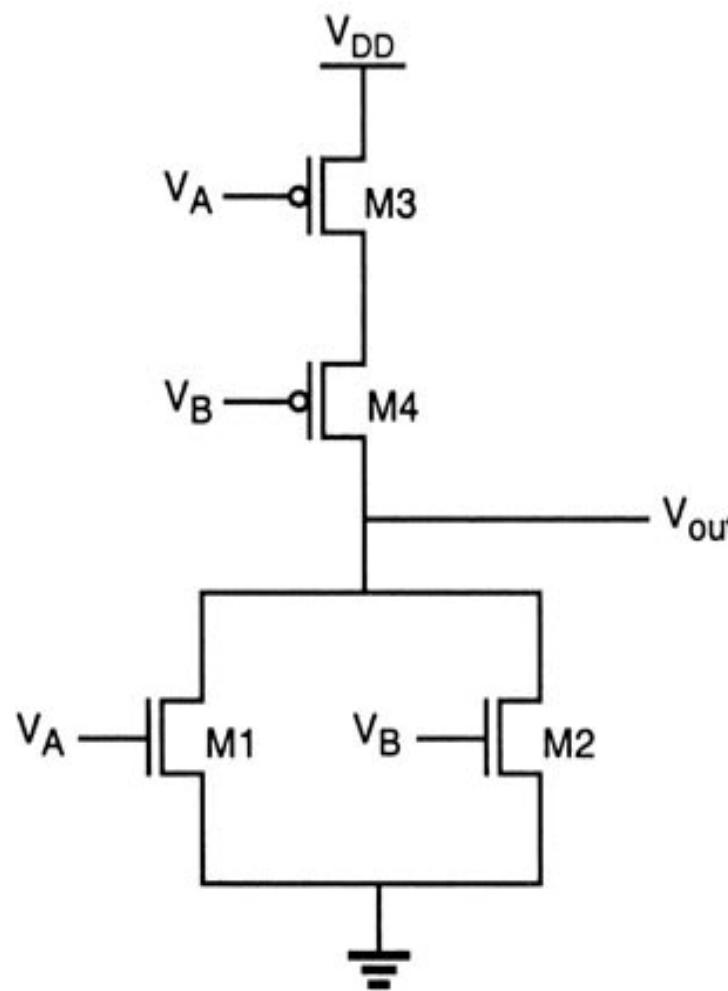
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A CMOS NOR2 Gate

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CMOS logic family

- Inverters
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- NOR gates
- Design exercise
- General gates
 - Complicated gates

CMOS IC Design Exercise

2018

Design Assignment

You are required to design a simple CMOS circuit consisting of a CMOS NOR2 gate. You are required to show the layout of the circuit, on cm graph paper, after calculating the aspect ratio of the transistors. The layout (i.e. plan view) of the circuit should include the V_{DD} and ground lines but not bond pads. Marks will be awarded for the report (including calculations and explanation of the calculations), the layout, and the quality of the drawing of the layout. You must also hand in, with the layout, a report in addition to the electronic submission on ICE.

Specification:

$V_{DD} = 3V$, $V_T = 0.3V$, $C_{ox} = 3 \times 10^{-4} Fm^{-2}$, electron mobility $0.1 \text{ m}^2 V^{-1} s^{-1}$, hole mobility $0.05 \text{ m}^2 V^{-1} s^{-1}$, **minimum feature size $0.3 \mu\text{m}$** , maximum alignment error $0.3\mu\text{m}/2$. The area of the circuit should be a minimum.

Your exercise: $2\lambda = 0.3 \mu\text{m}$

CMOS IC Design Check Points (2018)

Layout (50%):

Check point 1: Design rules' application for the 1st – 6th masks (patterns' size and spacing, such as minimum poly width is 2 lambdas and minimum poly spacing is 2 lambdas)

Check point 2: Design rules' application for the metal mask, interconnection width and spacing are 3 lambdas, VDD and ground > 3 lambdas, regular patterns (>1 lambda).

Check point 3: Design rules' application for the alignment error (such as all holes are covered by metal and minimum gate extension of poly over active is 2 lambdas)

Check point 4: All 7 masks have the same size (chip area). One body contact for each transistor at least (because of series resistance).

Check point 5: You should minimize chip area.

Report (50%):

Check point 1: Report format (cover page, contents, abstract, introduction, main body, conclusion, references)

Check point 2: main body 1: design rules' description

Check point 3: main body 2: theory of an **NOR** gate [VOH, VOL, VIH, VIL, Vth and why choose $k_p = 4k_n$ and what is the “worst case”?]

Check point 4: main body 3: results (design rules application on the 7 masks)

Check point 5: main body 4: discussion [such as how to reduce the chip area, how the $(W/L)_n/(W/L)_p$ ratio is affected by the two inputs “1,1” or “1, 0” or “0, 0”]

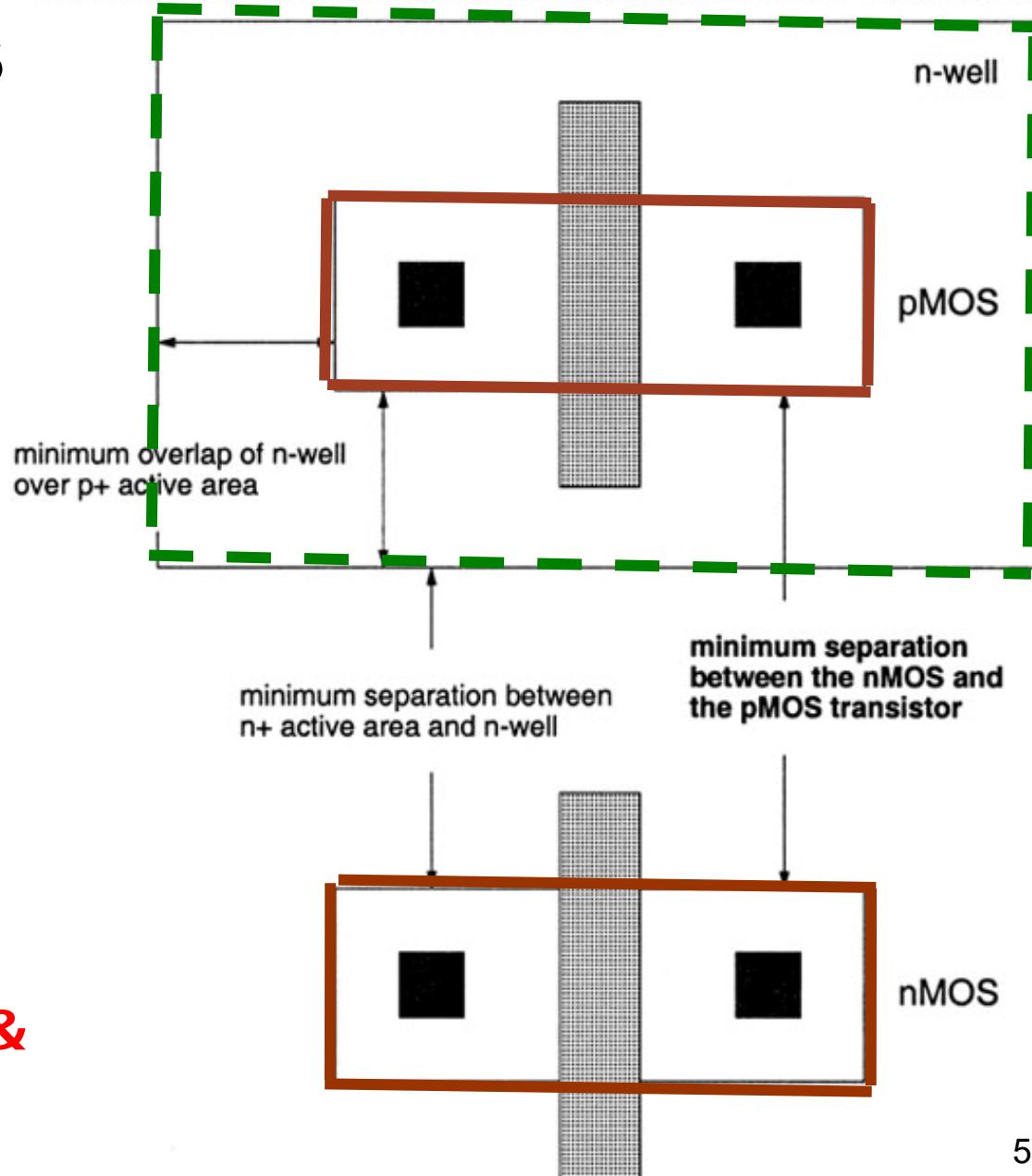
This is a paper design

- This is a paper design, get the graph paper with a stipulated scale from Lab EE215.
- **Deadline: 5:00 pm, 12nd December 2018**
 - 1) Report (submission on ICE as well)
 - 2) Layout (submission on ICE as well)
- You must also hand in them in class on 13/12.
- Late submission of the hard copies will be noted₅₅ down.

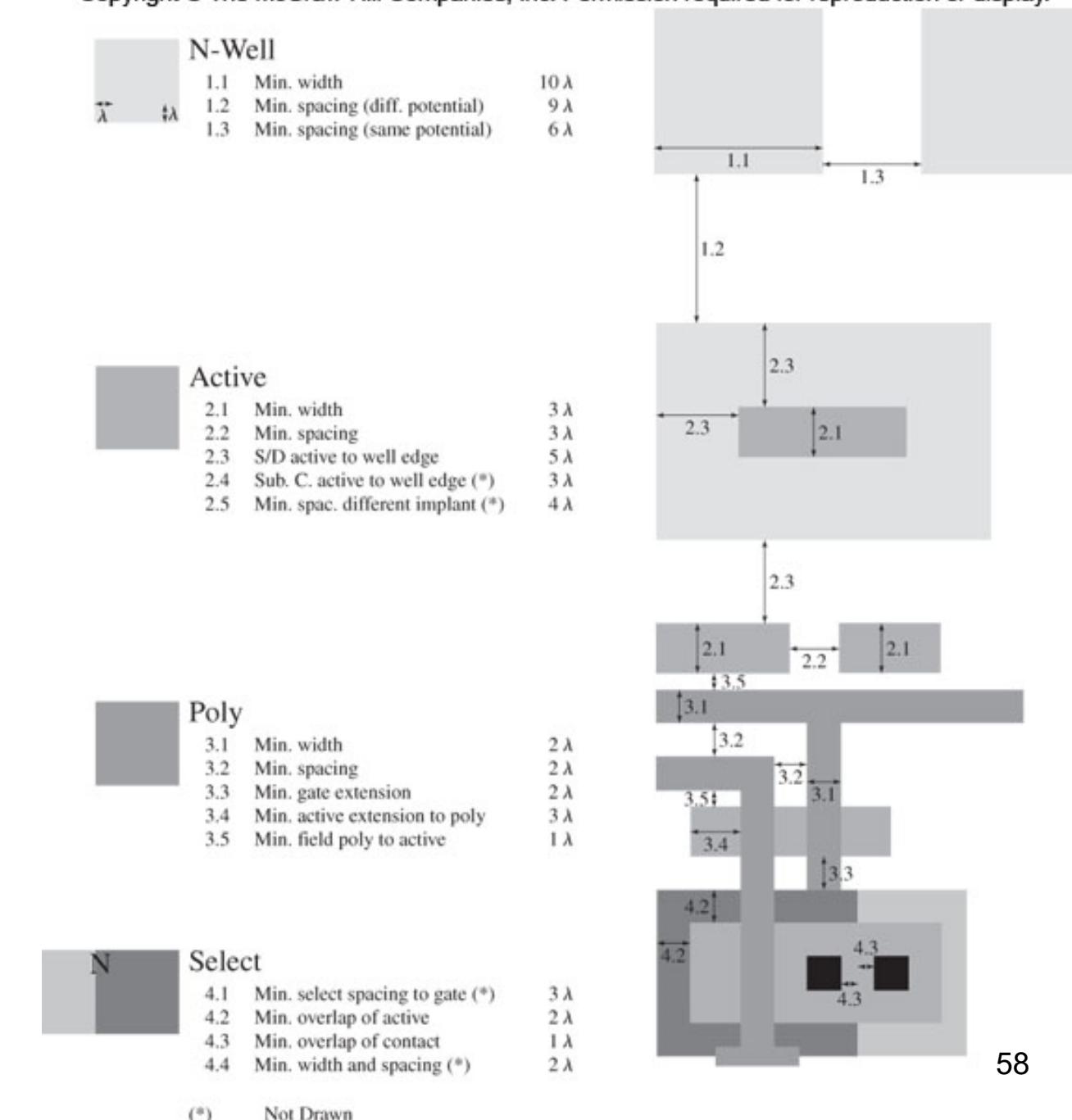
CMOS IC Design Exercise

- Understanding alignment and minimum feature size:
 - The minimum feature size is the smallest dimension that can be defined on a chip. This will often be the channel length L.
 - The various layers have to be aligned (registered) with each other. This involves some error in placing any mask relative to the pattern already on the silicon wafer. It is necessary to know how large (in microns) the error can be. You must allow for this in the design.
- Understanding difference between the *n*- and *p*-MOSFETs

Using rules

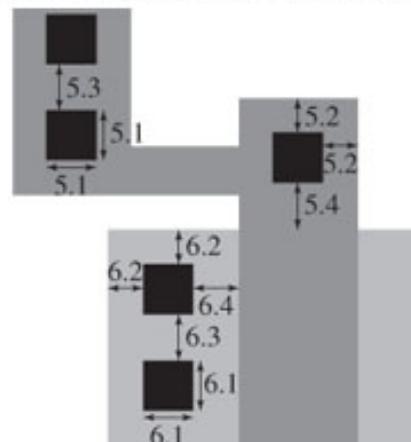


M2: pMOS active &
nMOS active



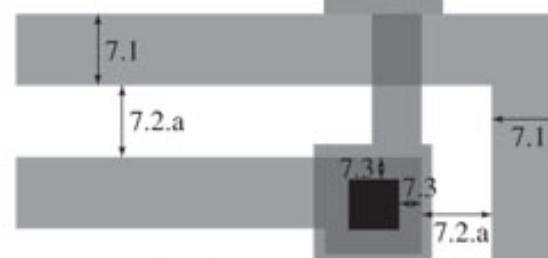
Contact

5.1	Exact contact size	2λ
5.2	Min. poly overlap	1.5λ
5.3	Min. spacing	2λ
5.4	Min. spacing to gate	2λ



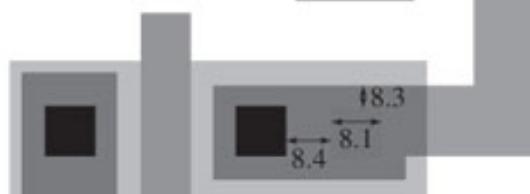
Metal1

7.1	Min. width	3λ
7.2.a	Min. spacing	3λ
7.3	Min. overlap of any contact	1λ



Via1

8.1	Exact size	2λ
8.2	Min. spacing	3λ
8.3	Min. overlap by metal1	1λ
8.4	Min. spacing to contact	2λ
8.5	Min. spac. to poly or act. edge	2λ



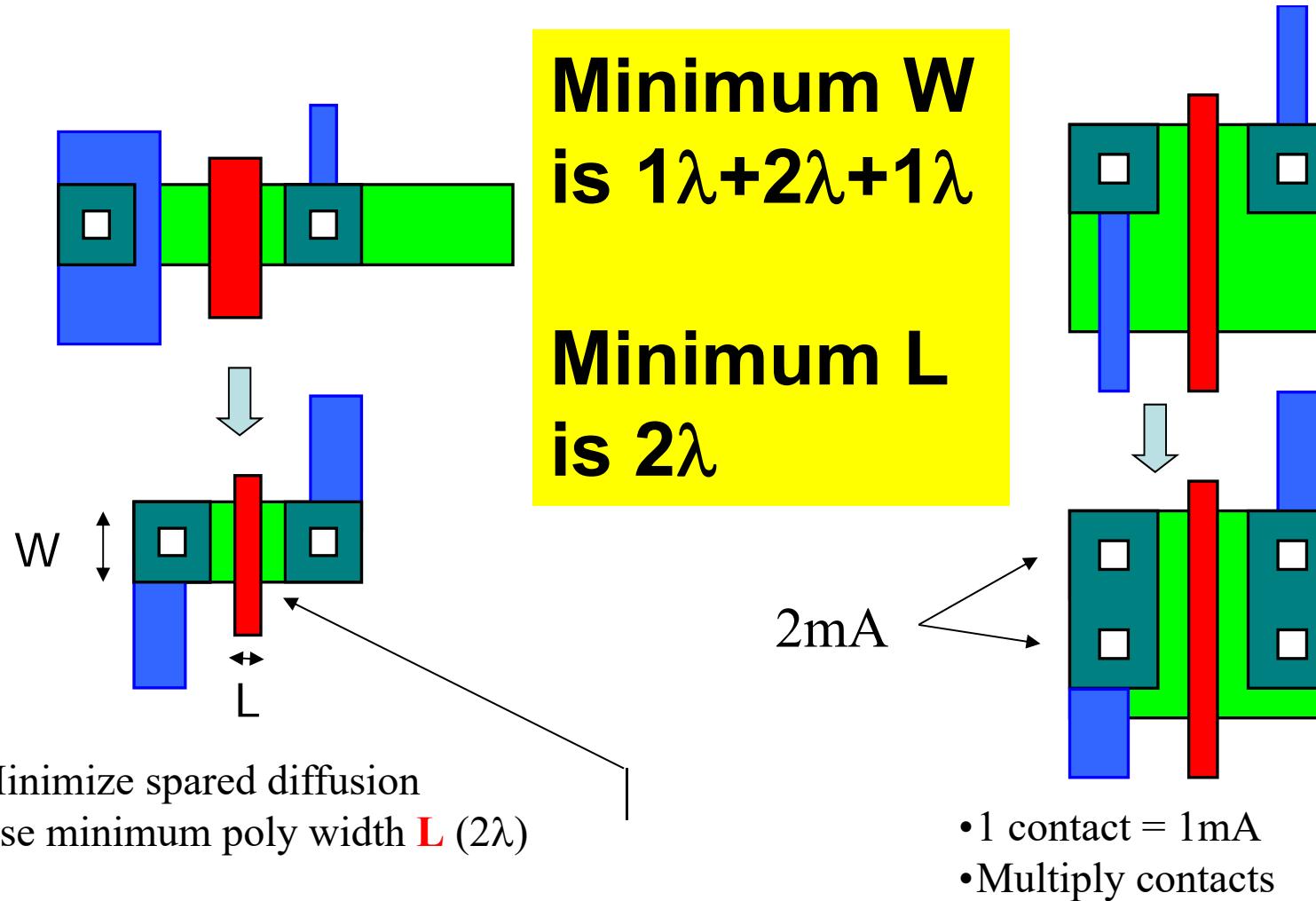
Metal2

9.1	Min. width	3λ
9.2.a	Min. spacing	4λ
9.3	Min. overlap to vial	1λ

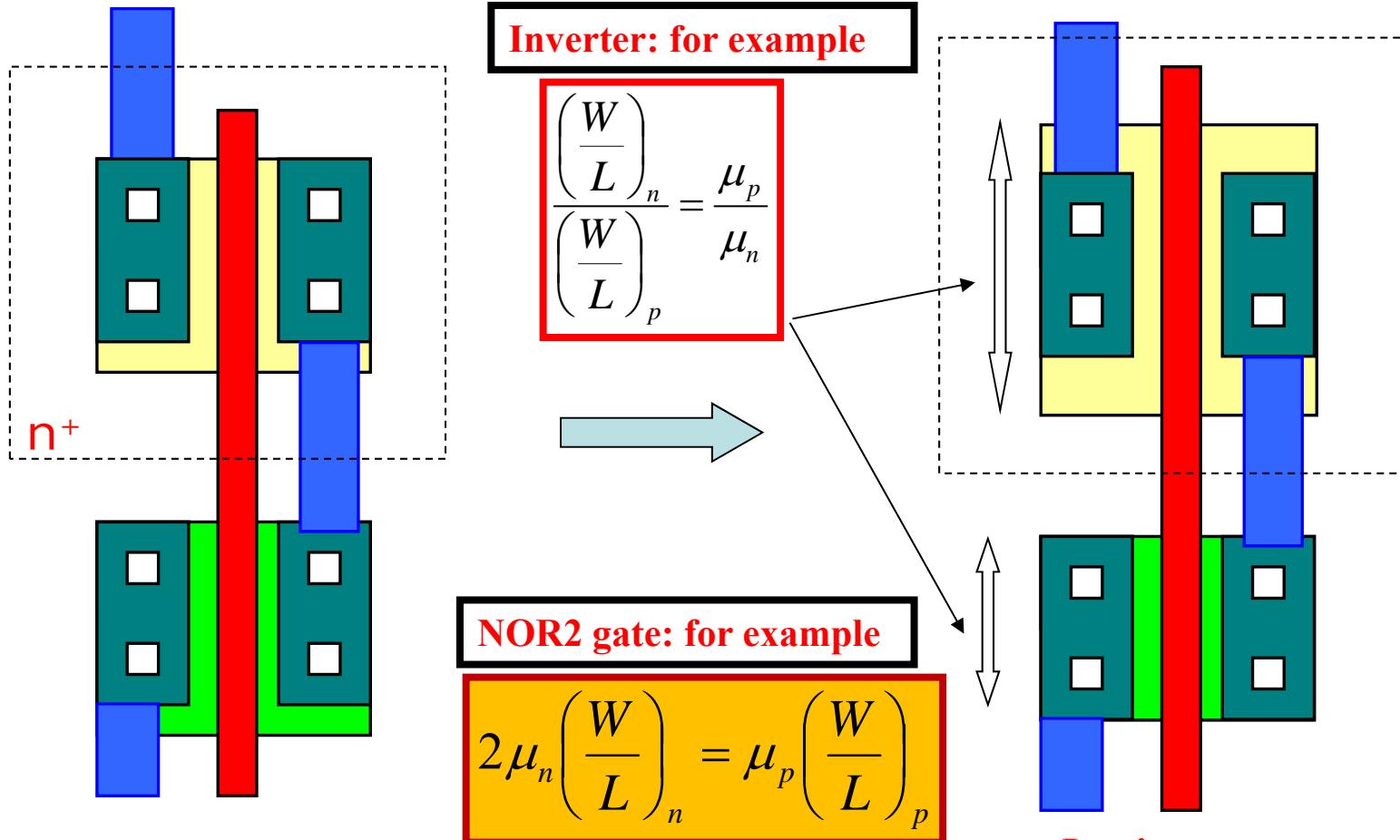


(*) Not Drawn

Basic design rules

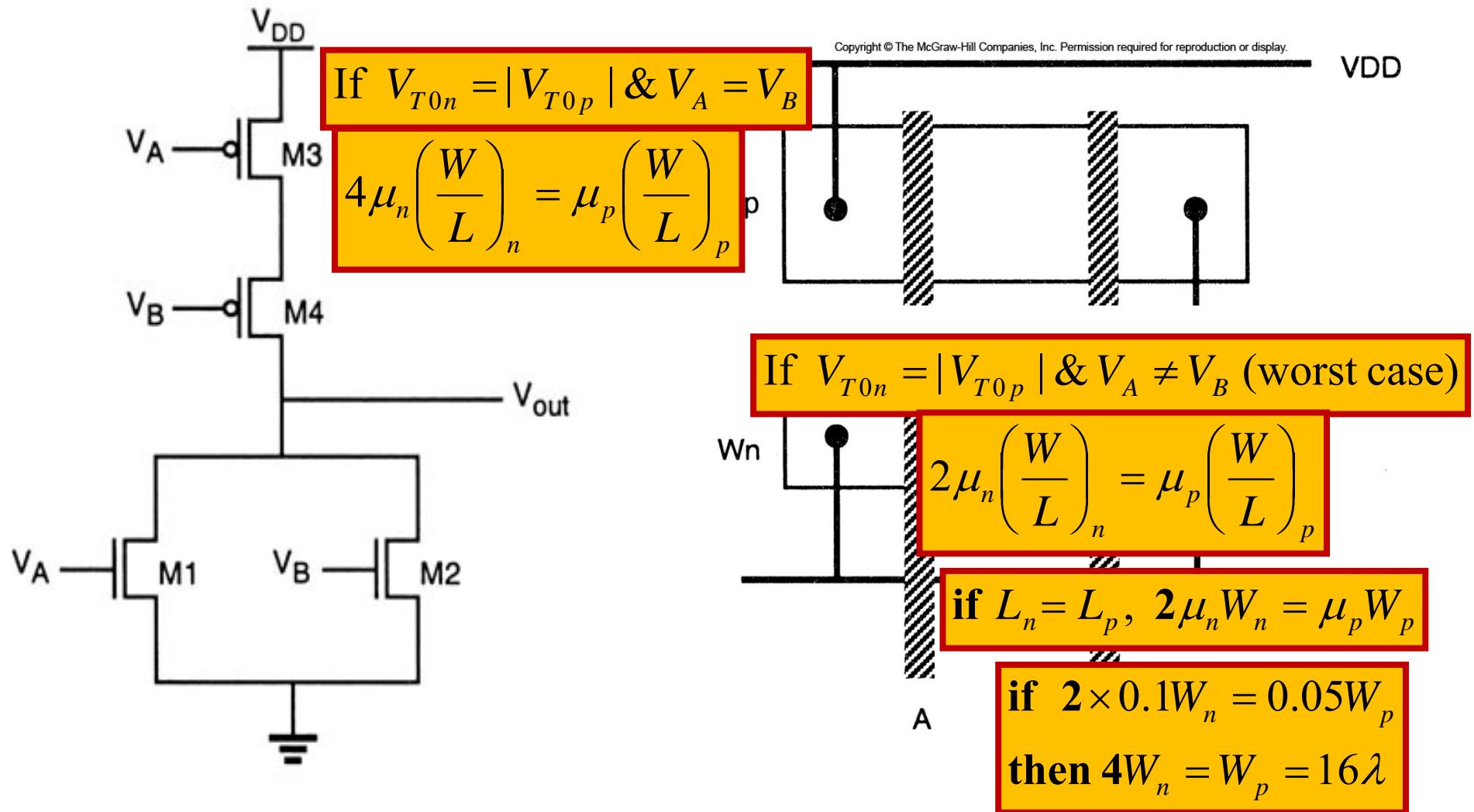


Basic design rules



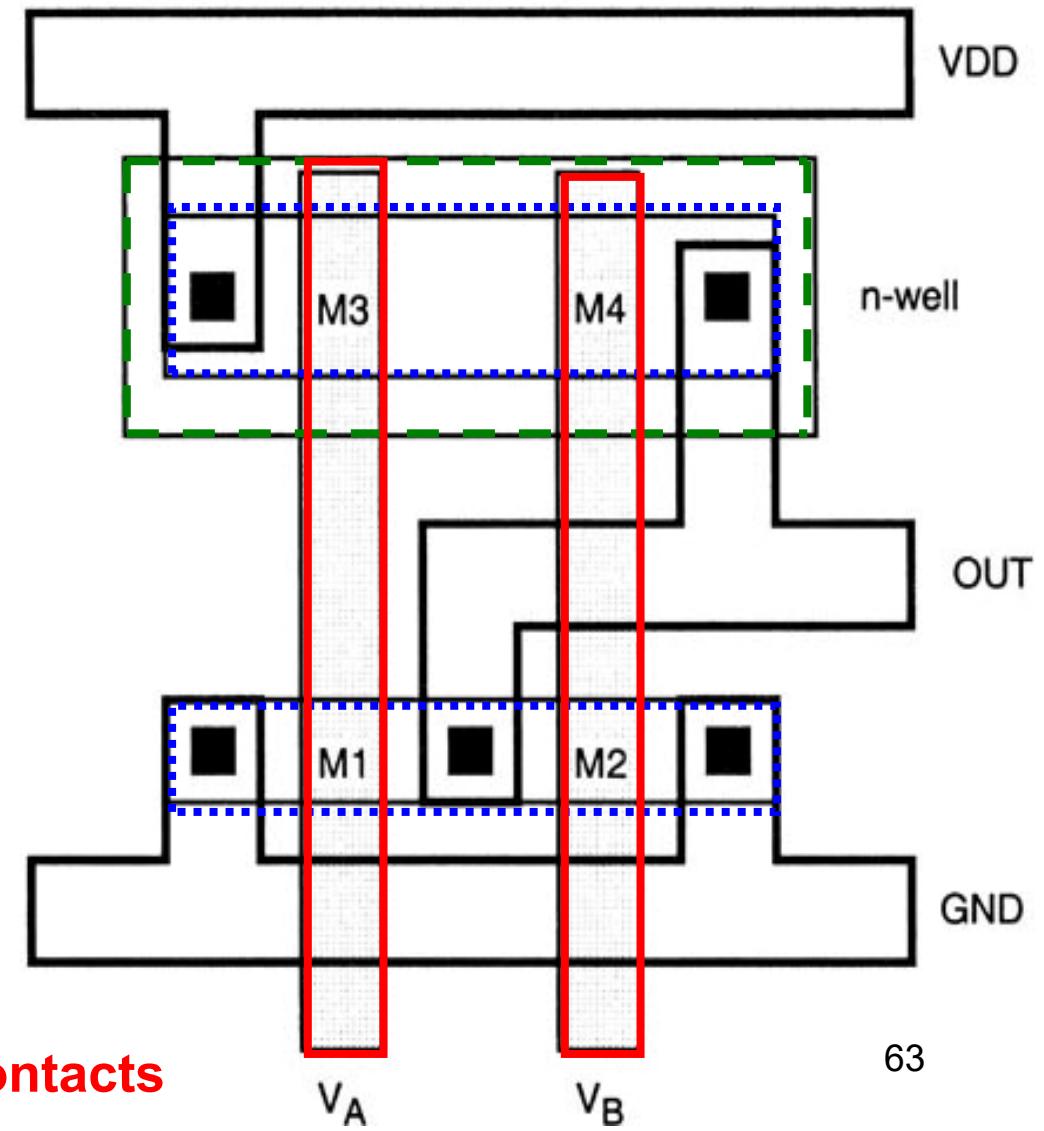
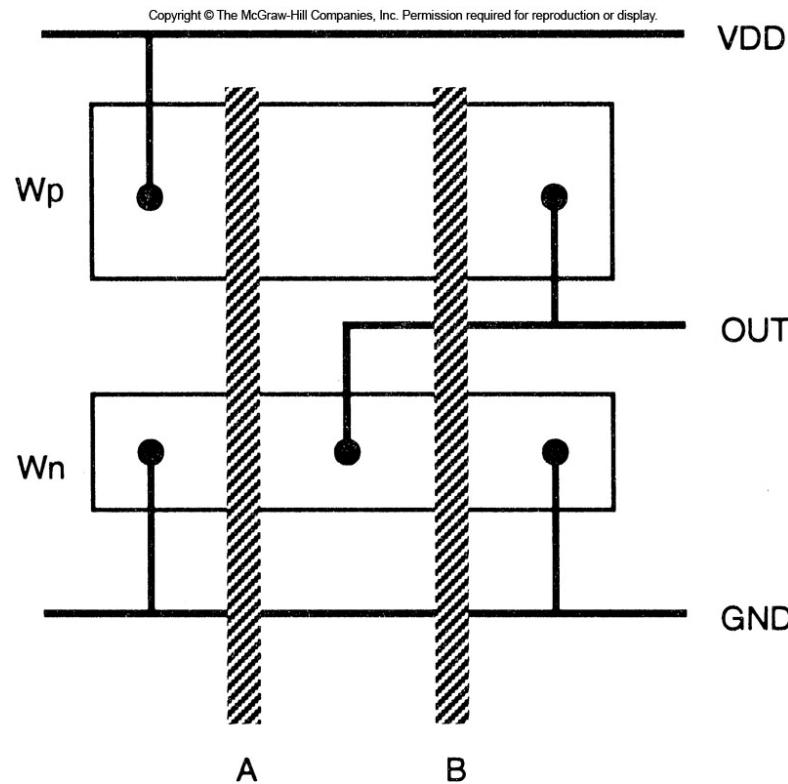
Design Exercise: CMOS NOR2

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Design Exercise: CMOS NOR2

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Design Exercise: CMOS NOR2

Contact

Poly

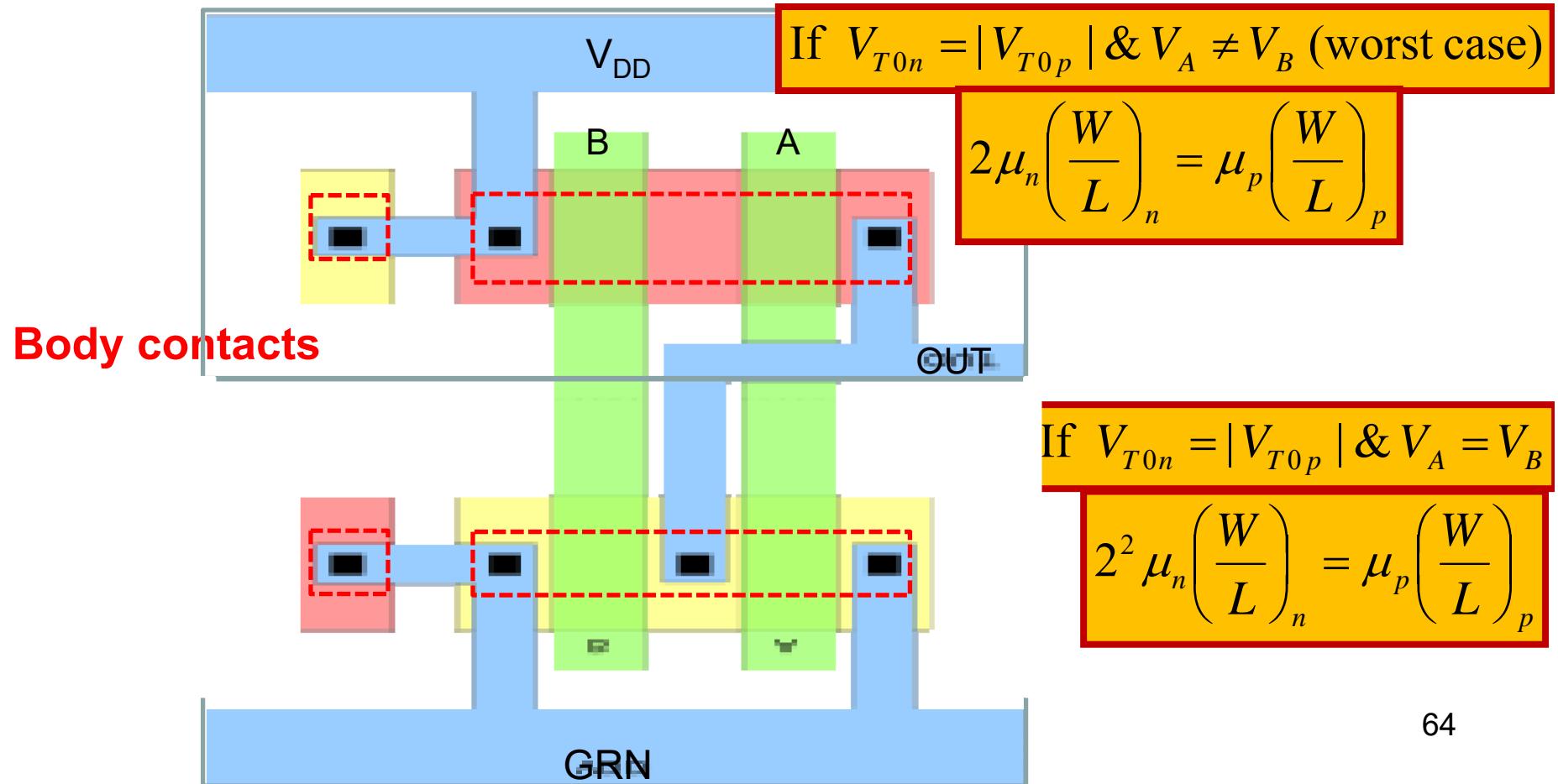
Metal

N-well

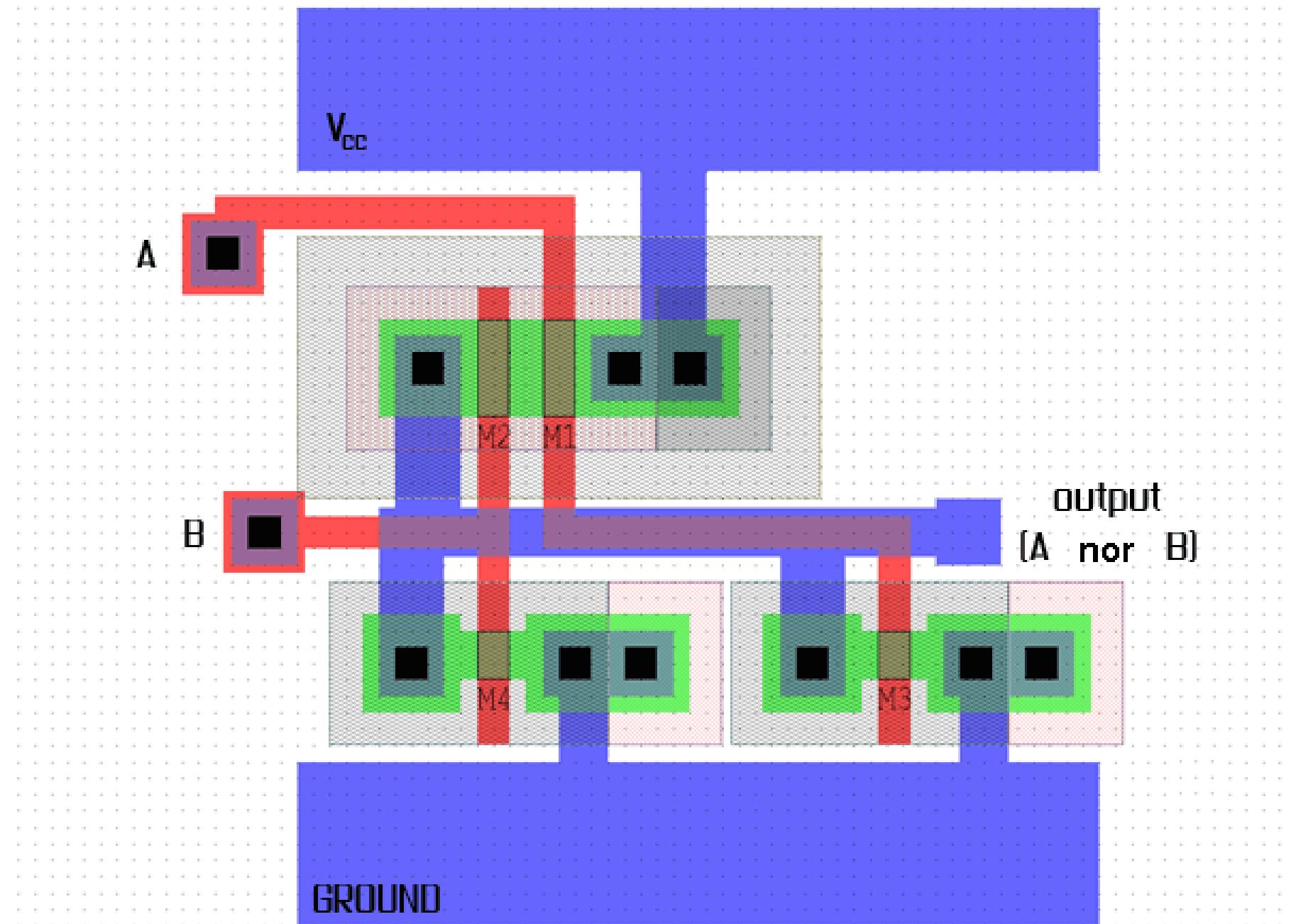
N-select

P-select

Active



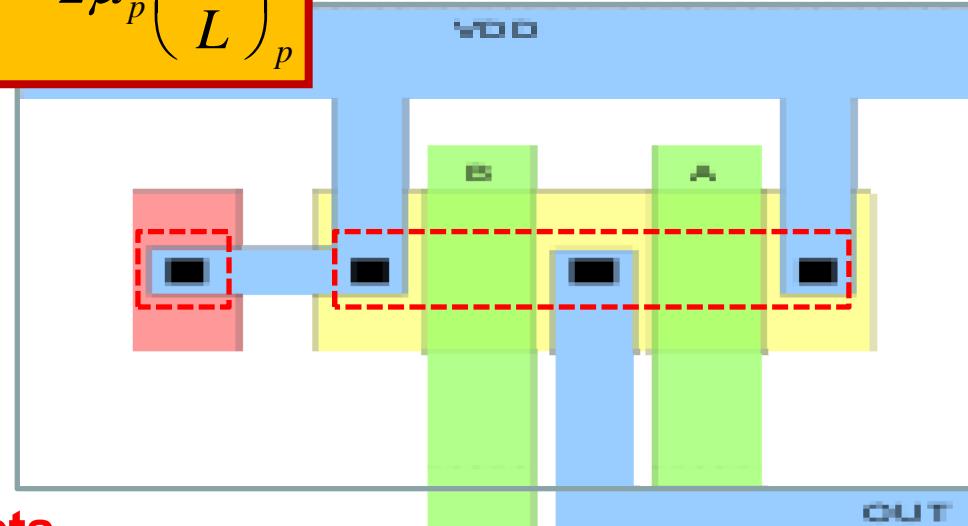
Design Exercise: CMOS NOR2



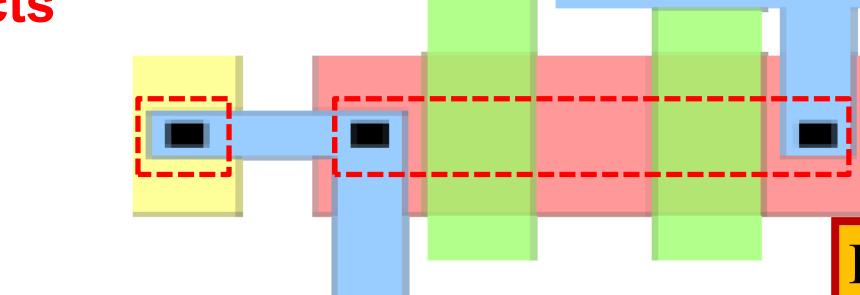
If $V_{T0n} = |V_{T0p}|$ & $V_A \neq V_B$ (worst case)

Example: CMOS NAND2

$$\mu_n\left(\frac{W}{L}\right)_n = 2\mu_p\left(\frac{W}{L}\right)_p$$



Body contacts



If $V_{T0n} = |V_{T0p}|$ & $V_A = V_B$

$$\mu_n\left(\frac{W}{L}\right)_n = 2^2 \mu_p\left(\frac{W}{L}\right)_p$$

Metal

N-select

Poly

P-select

Contact

N-well Active

Design Exercise: CMOS NOR2

Practical IC Layout Design Sessions

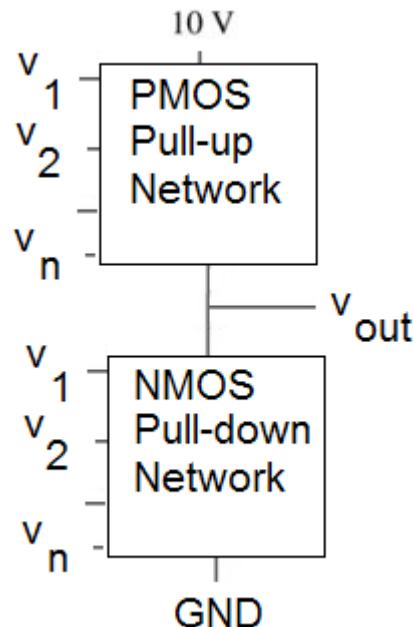
Week	Date	Time	Venue	TAs
Week 10	Friday, 23 rd Nov.	9:00am-	P202,	Yuxiao FANG
		1:00pm	P203	Yutao CAI
Week 11	Friday, 30 th Nov.	9:00am-	P202,	Yuxiao FANG
		1:00pm	P203	Miao CUI
Week 12	Friday, 7 th Nov.	9:00am-	TBD	Yuxiao FANG
		1:00pm		Yutao CAI



CMOS logic family

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- General gates
 - Complicated gates

CMOS Logic (General)



Any combination of inputs $V_1 V_2 \dots V_n$ that should result in an output of a logic state “1” should produce a low-resistance path from V_{out} to V_{DD} in the pull-up network (otherwise, the PMOS network should be of a high resistance).

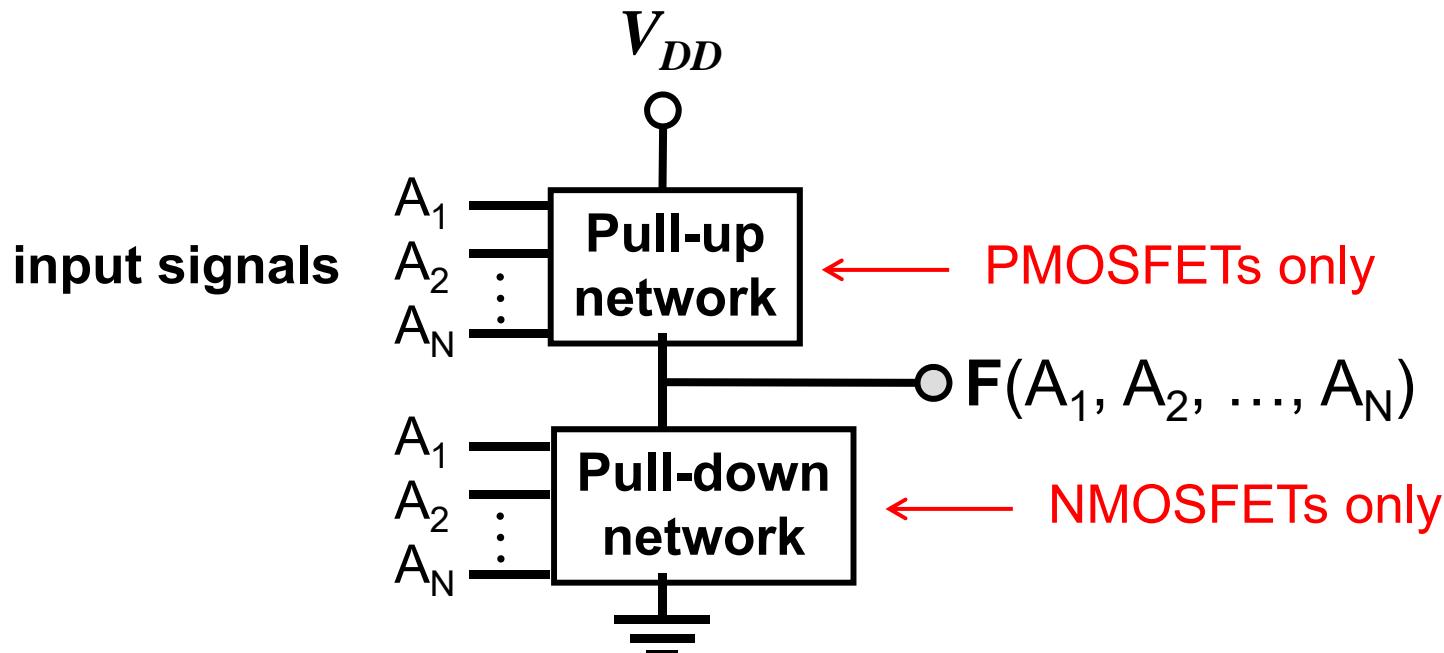
Any combination of inputs $V_1 V_2 \dots V_n$ that should result in an output of a logic state “0” should produce a low-resistance path from V_{out} to GND in the pull-down network (otherwise, the NMOS network should be of low resistance).

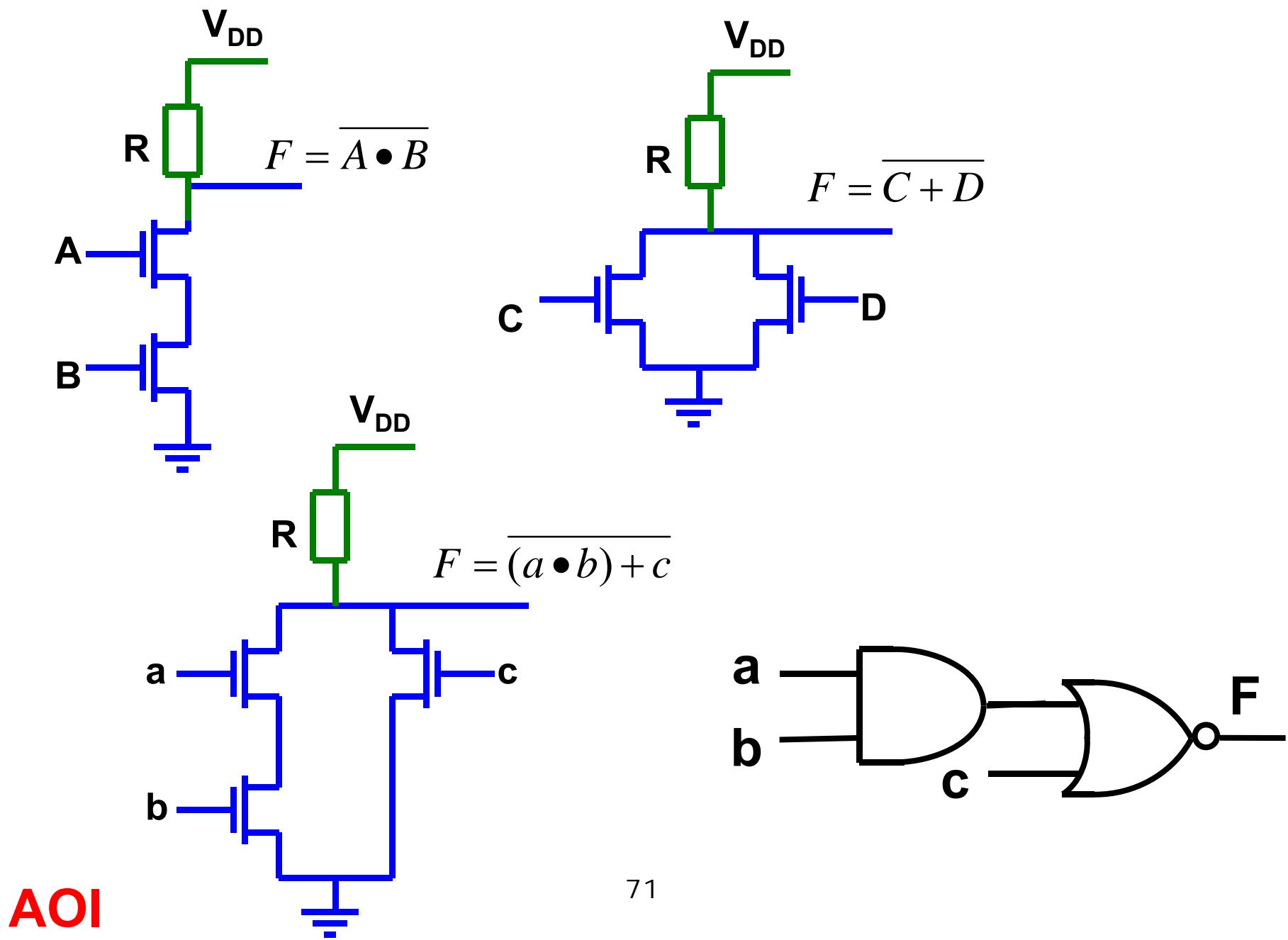
CMOS logic draws little current when V_{out} is a constant high or low (it does draw current when the output switches).

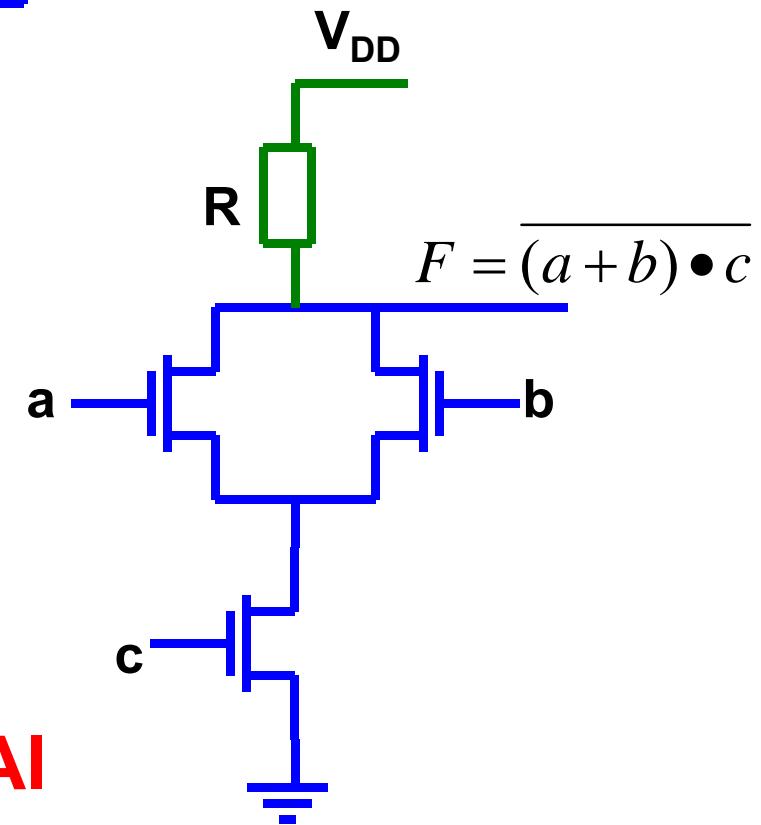
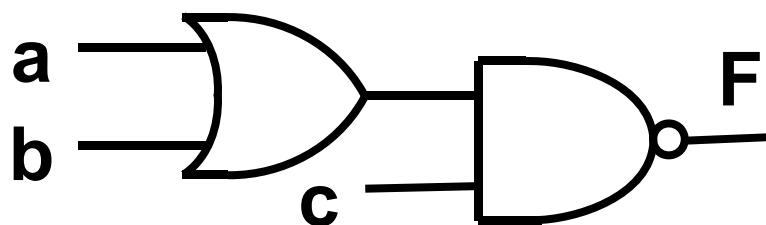
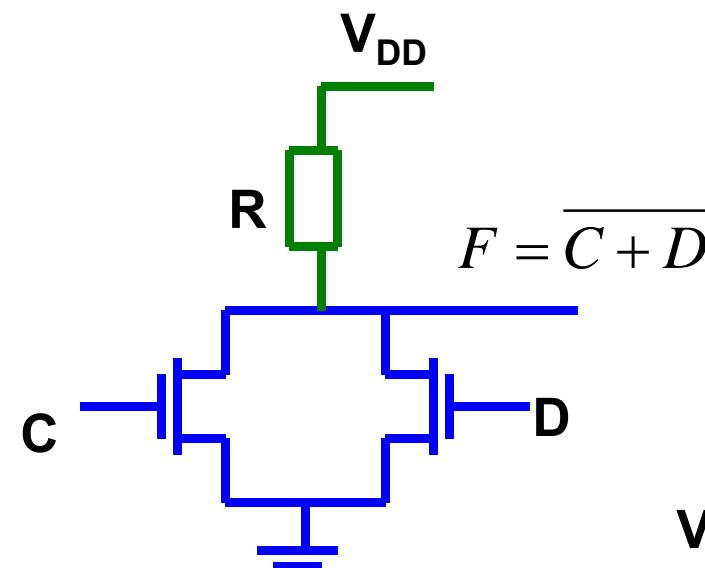
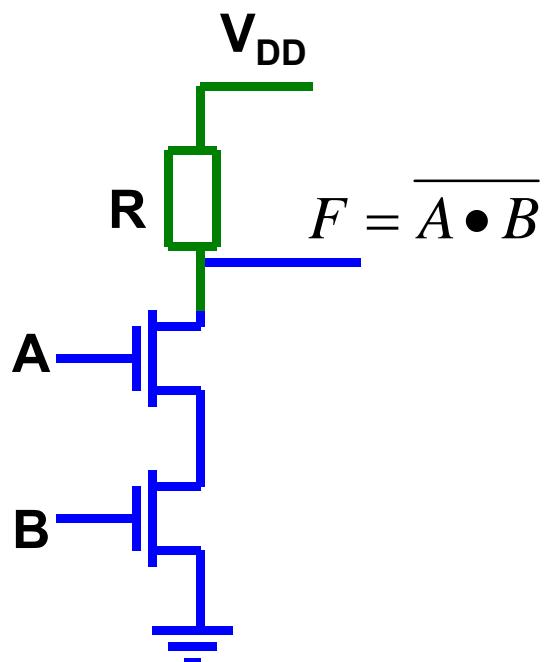
DC power consumption is low !

Pull-Down and Pull-Up Devices

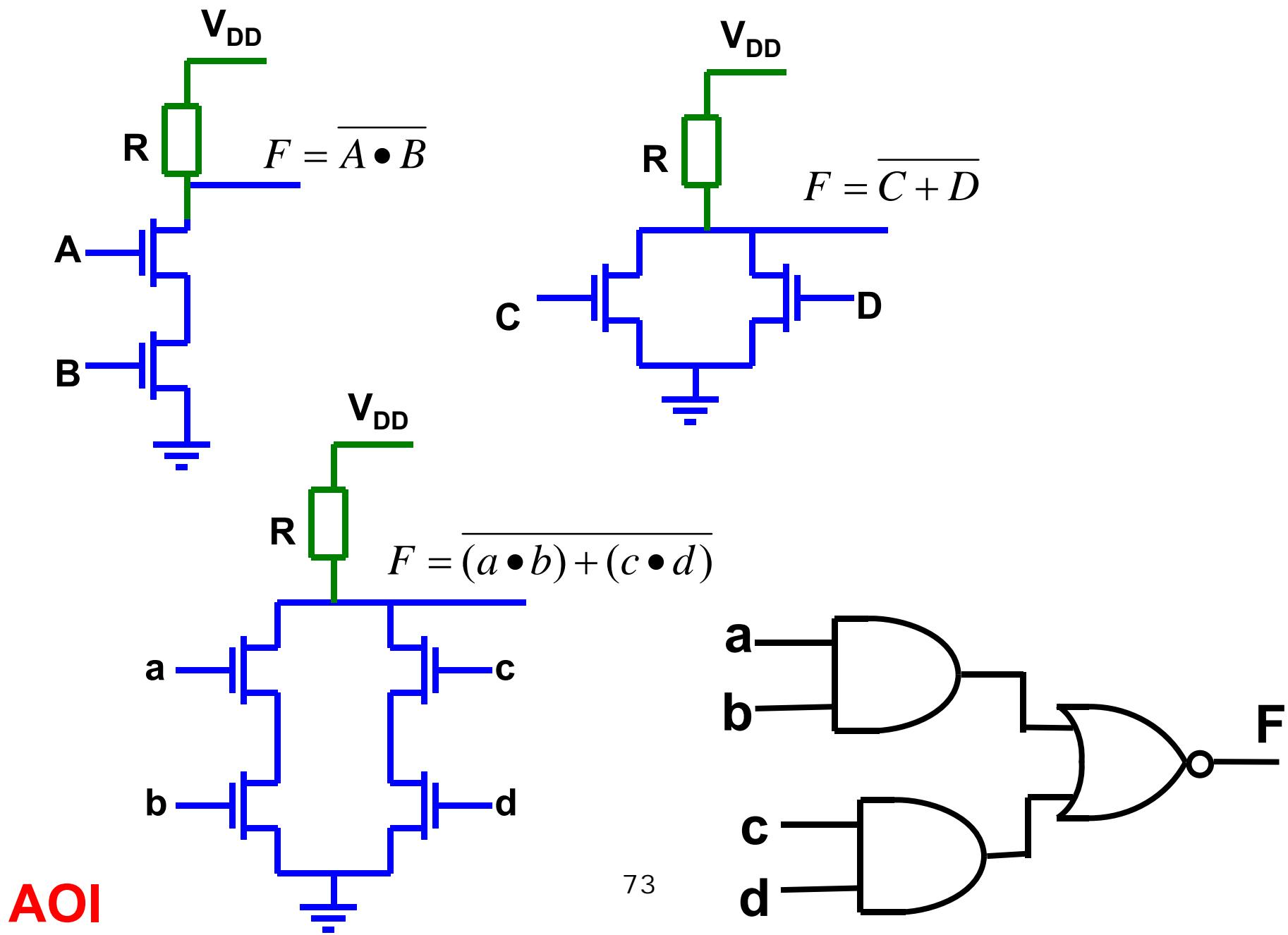
- In CMOS logic gates, NMOSFETs are used to connect the output to GND, whereas PMOSFETs are used to connect the output to V_{DD} .
 - An NMOSFET functions as a ***pull-down device*** when it is turned on (gate voltage = GND)
 - A PMOSFET functions as a ***pull-up device*** when it is turned on (gate voltage = V_{DD})

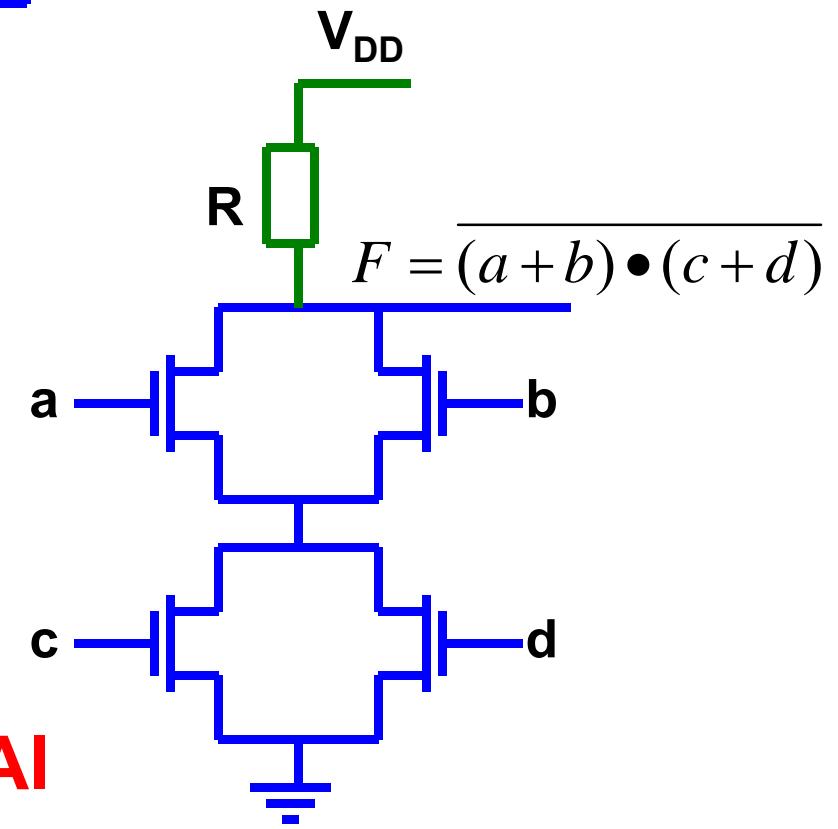
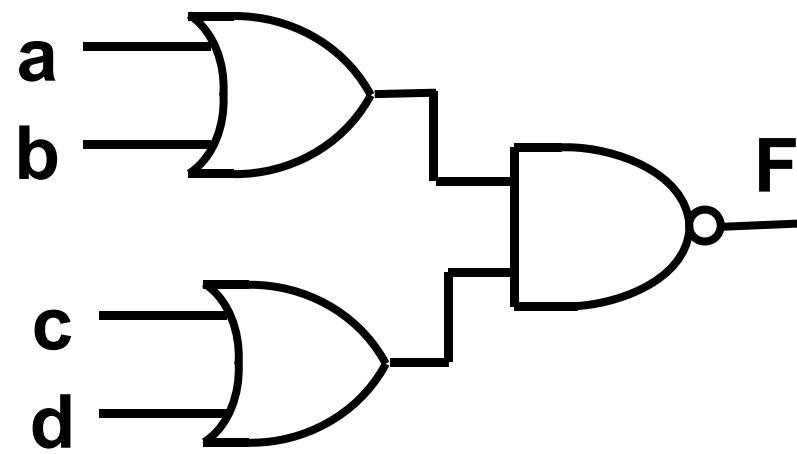
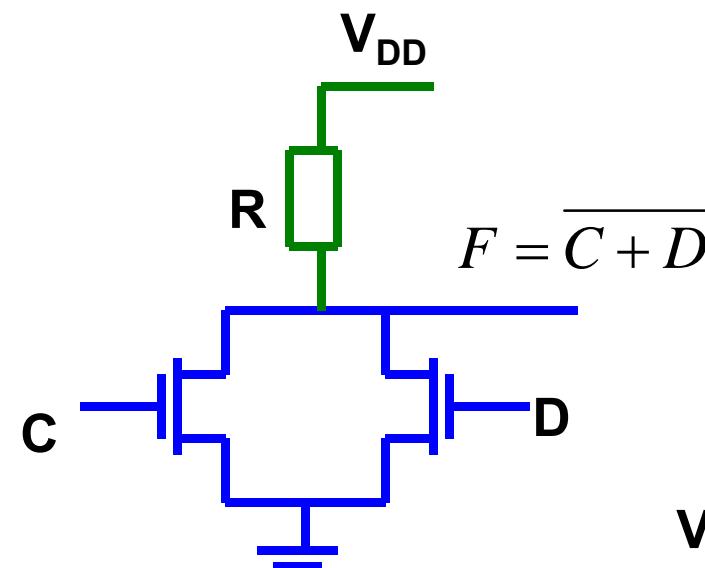
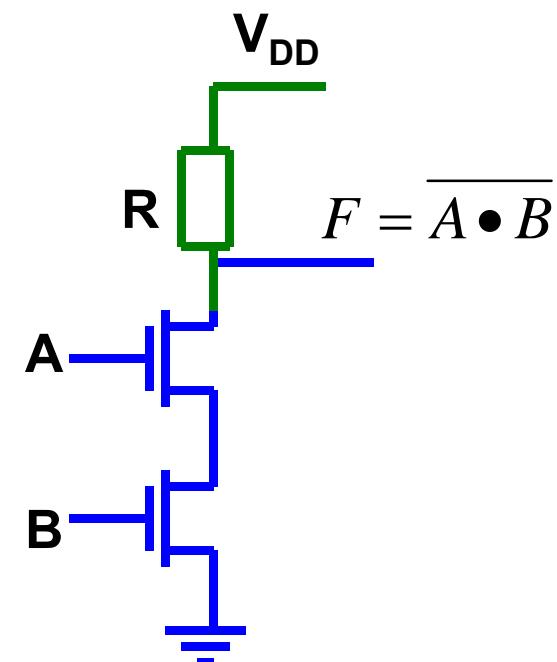




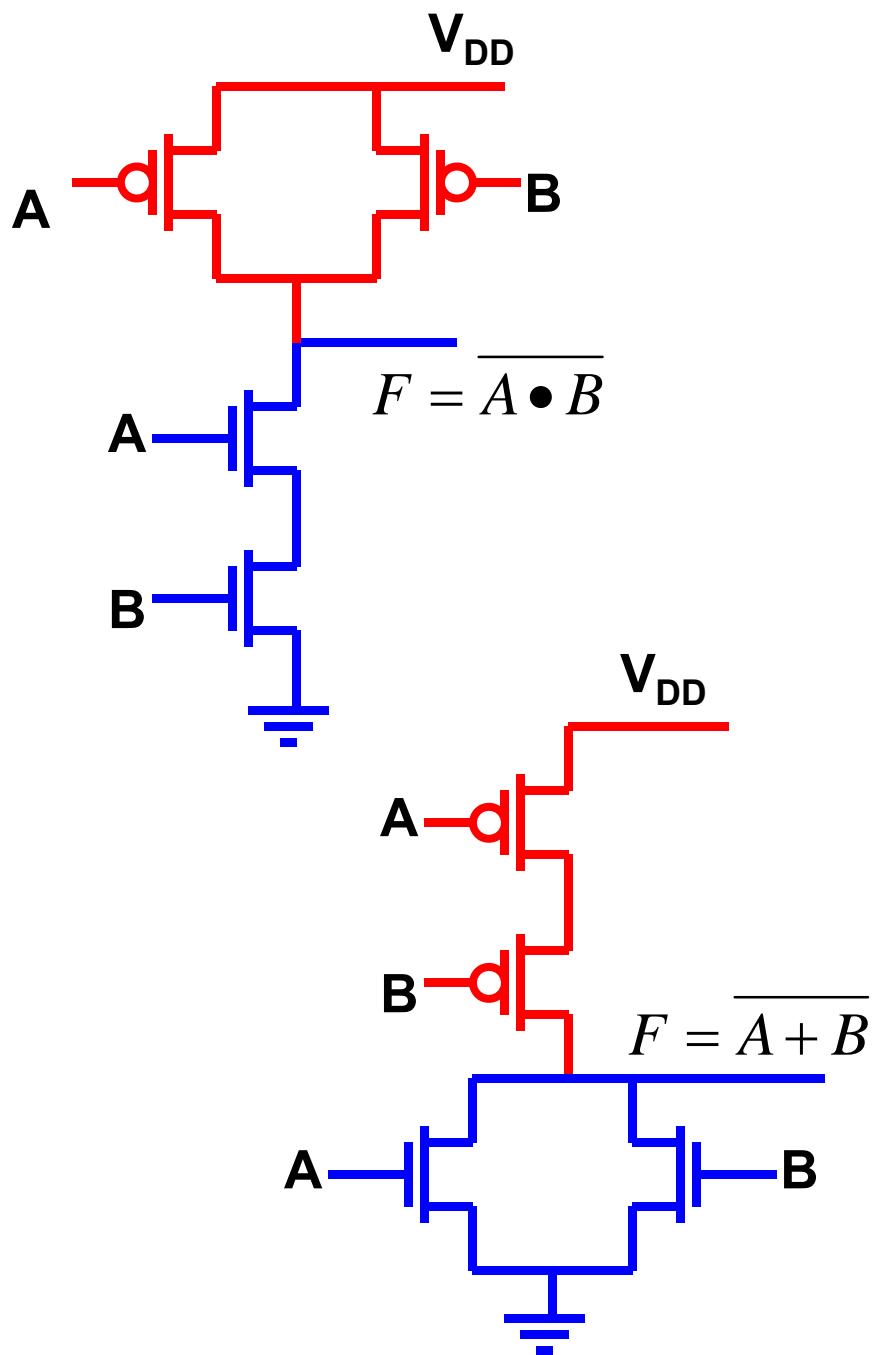


72 OAI

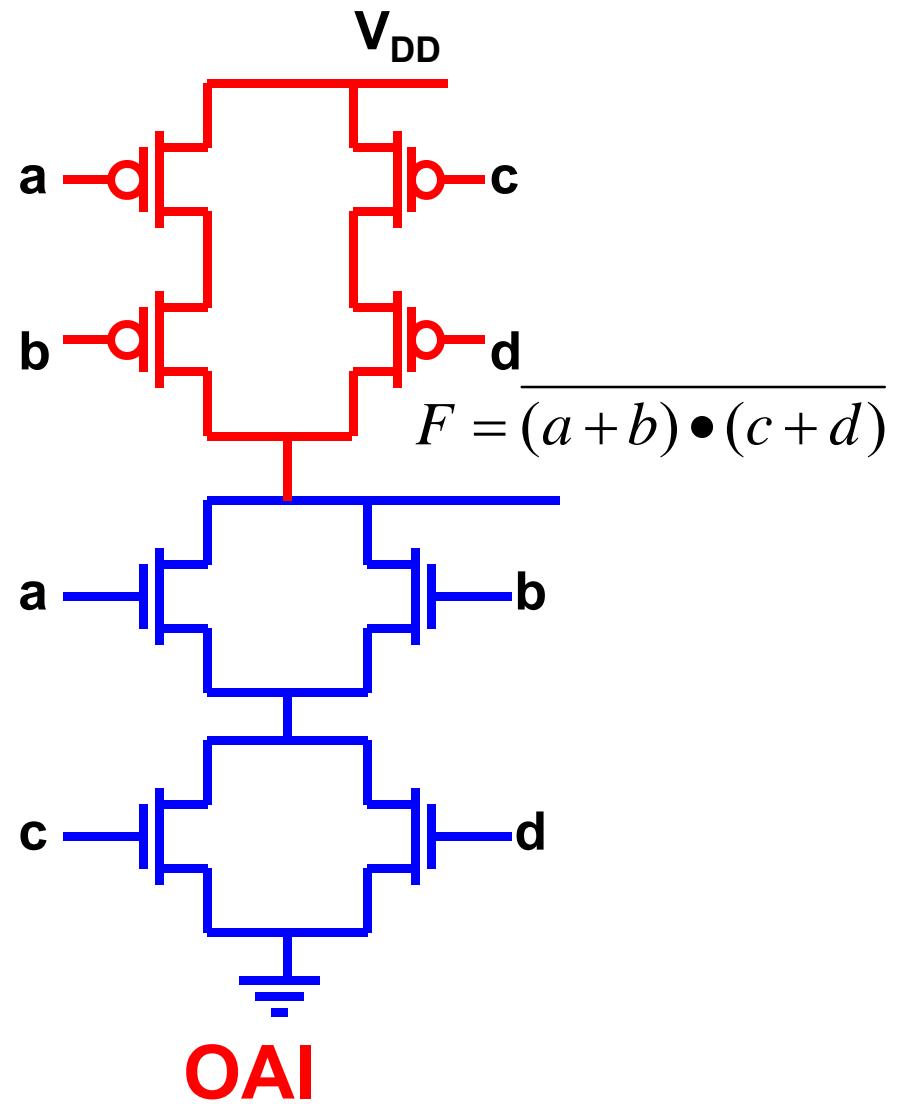




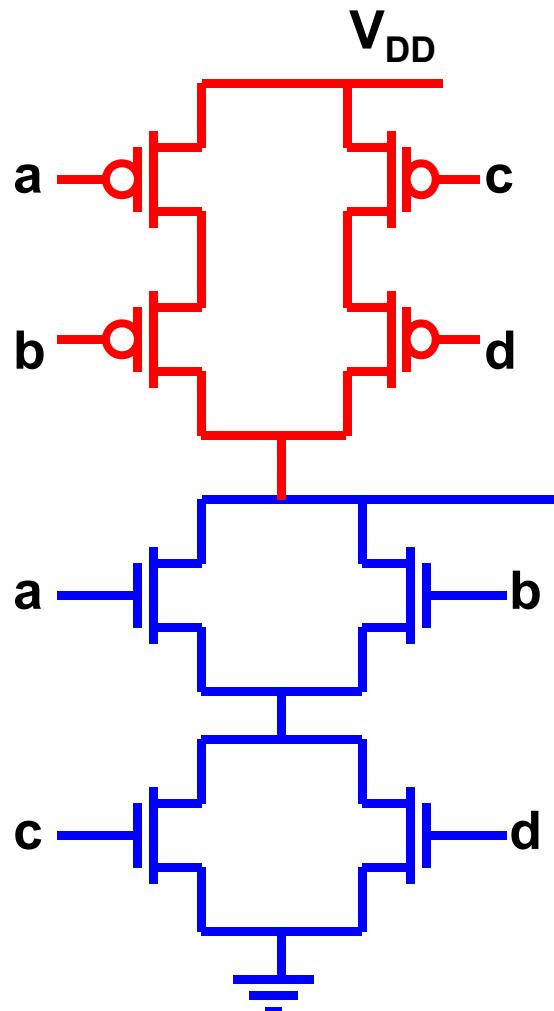
74
OAI



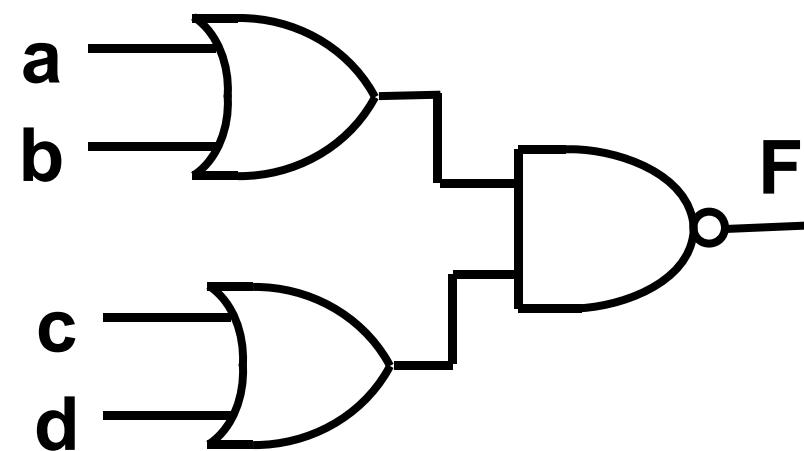
75



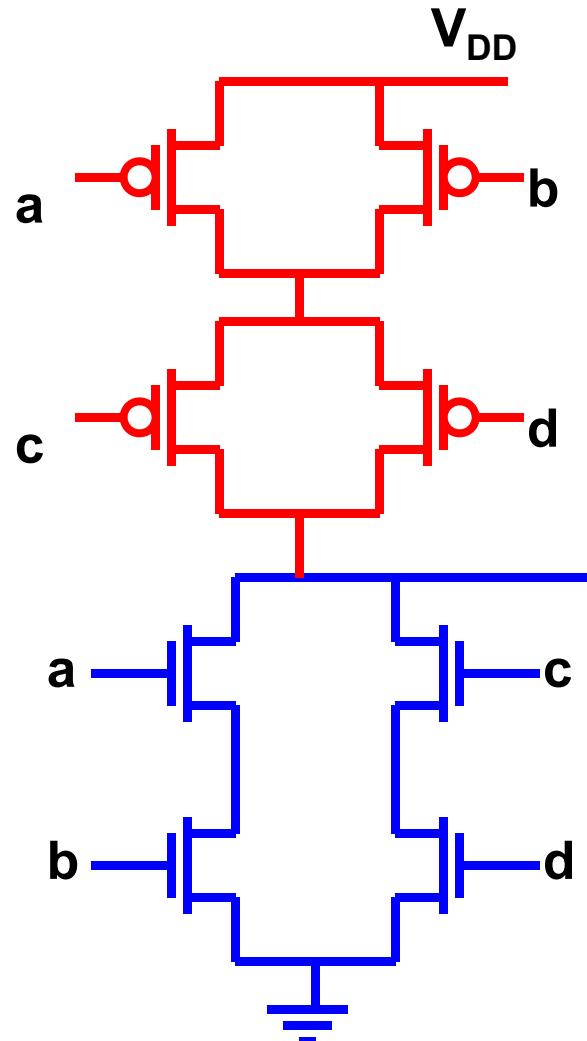
OAI



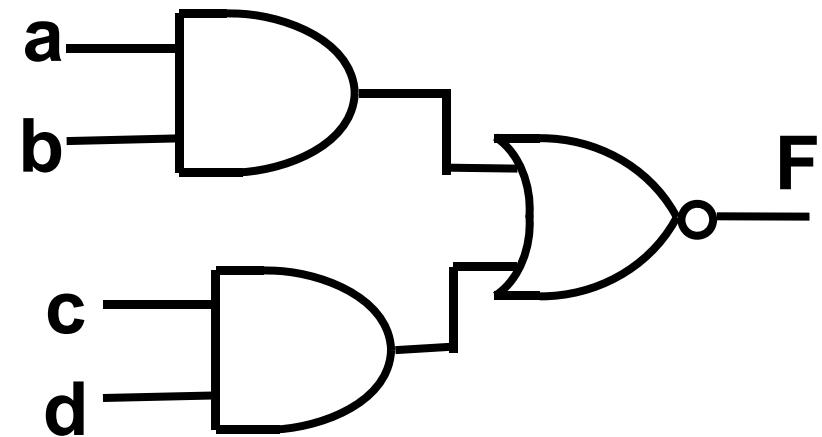
$$F = \overline{(a+b) \bullet (c+d)}$$



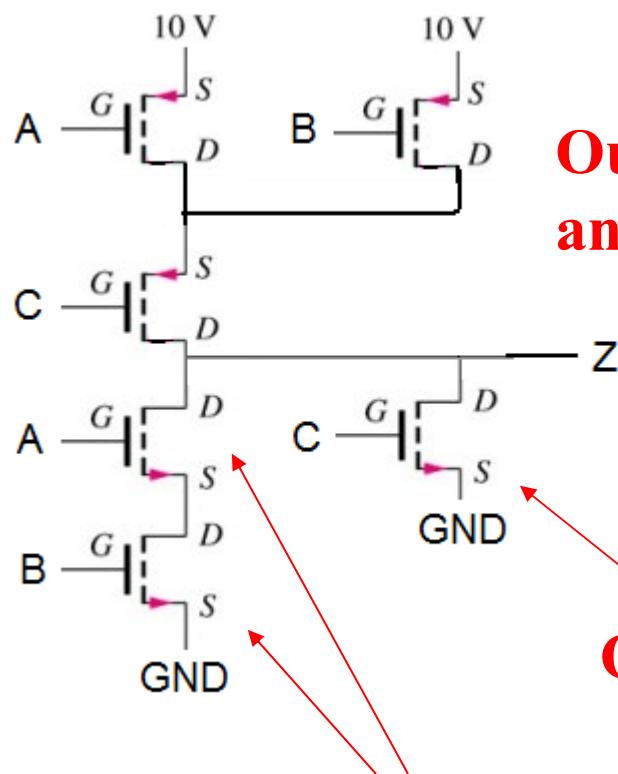
AOI



$$F = \overline{(a \bullet b) + (c \bullet d)}$$



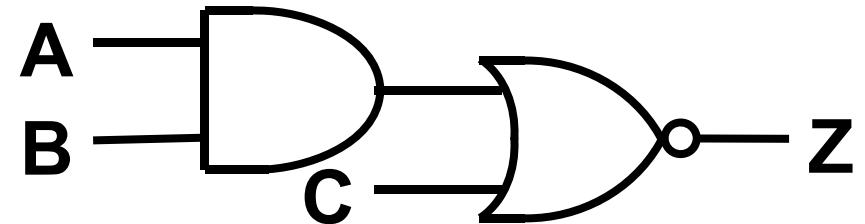
Example: Complex Function



**Output 1 if $C = 0$
and ($A = 0$ or $B = 0$)**

Output 0 if $A = 1$ and $B = 1$

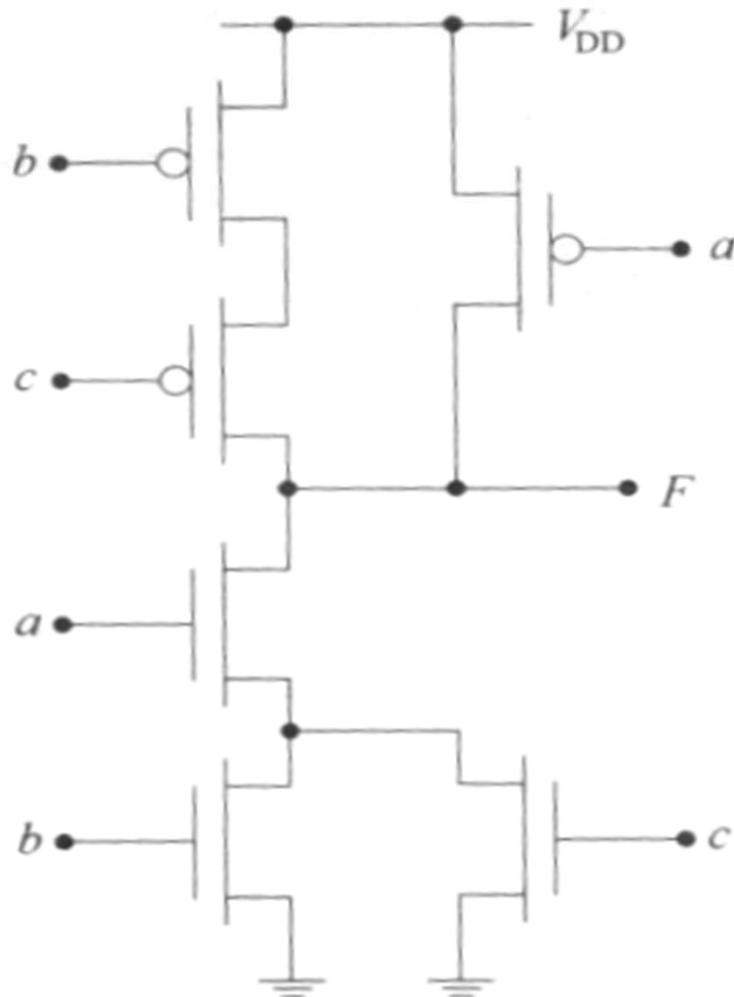
Logic function = ?



A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Example: Complex Function

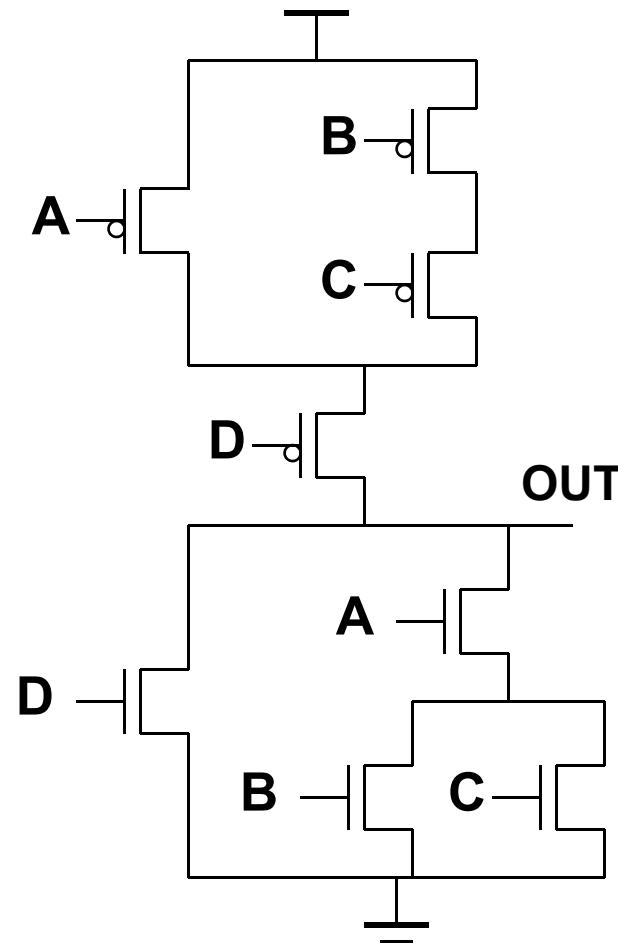
Logic Function, Symbol, & Circuit



Logic function = ?

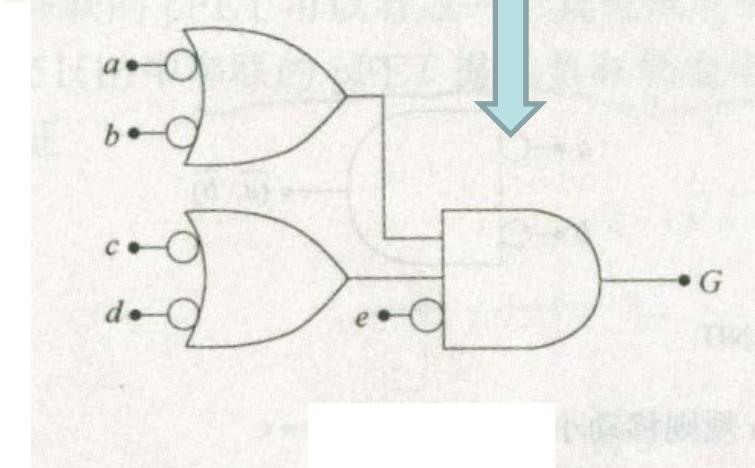
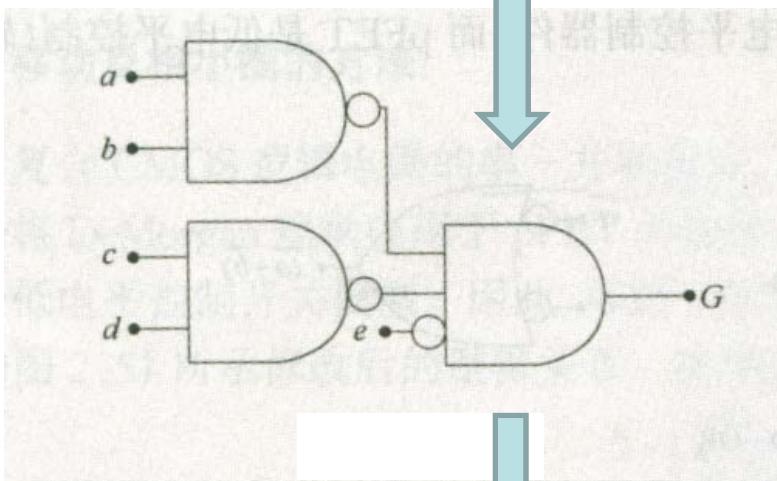
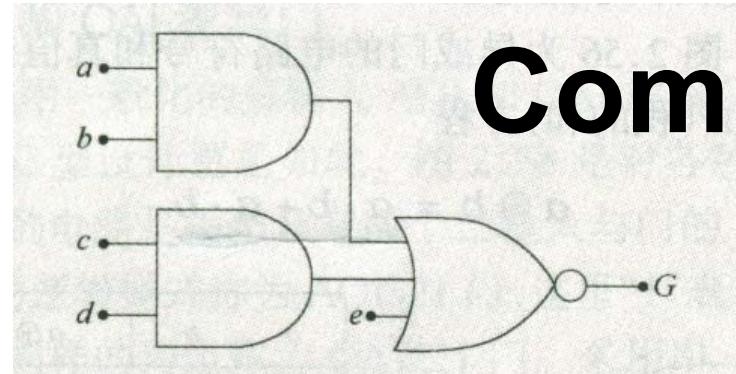


Complex CMOS Gate



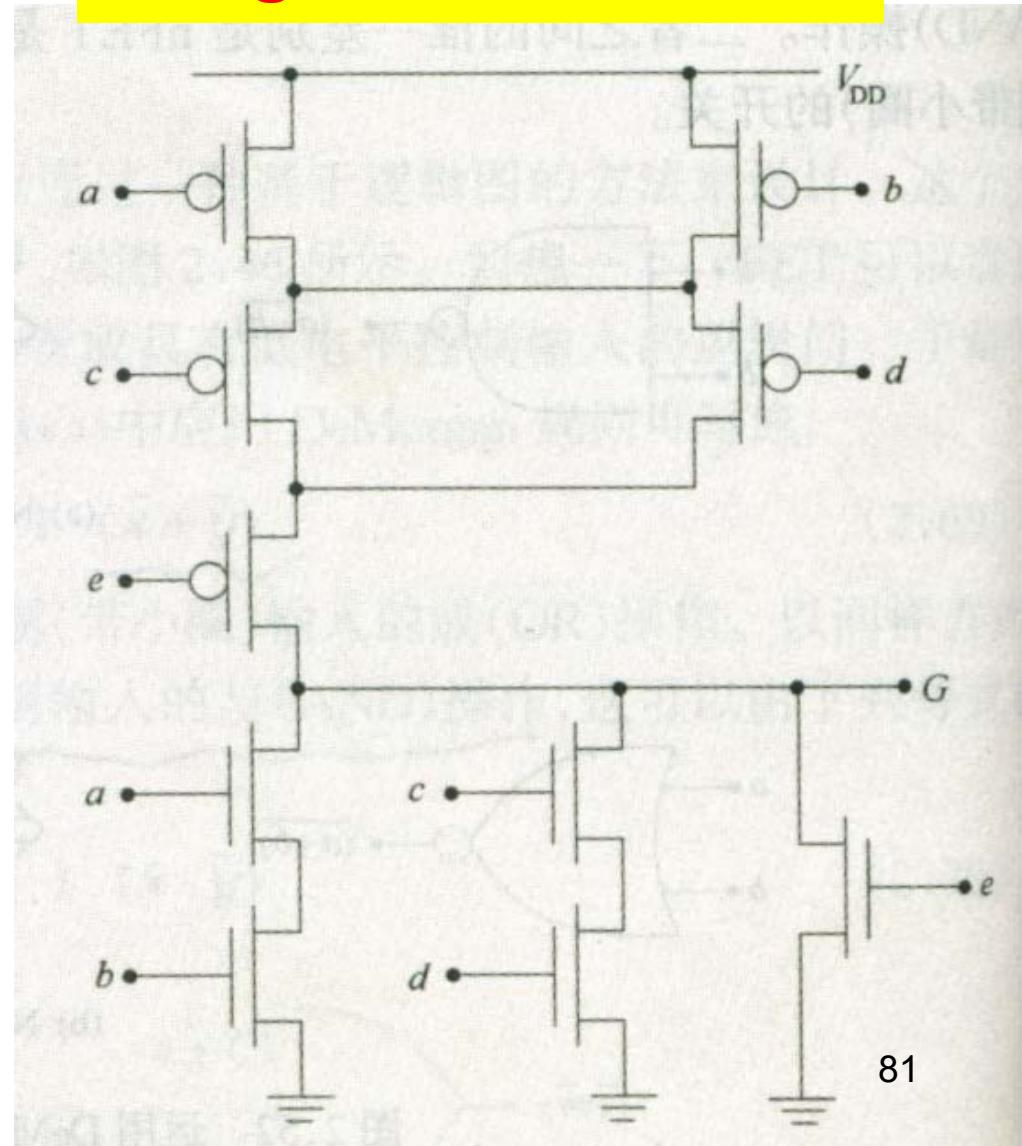
$$\text{OUT} = \overline{D + [A \cdot (B + C)]}$$

Logic symbols = ?



Complex CMOS Gate

Logic function = ?



Layout Example: NAND3

- Horizontal N-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top, Metal1 GND rail at bottom
- 32λ by 40λ

