



Xi'an Jiaotong-Liverpool University
西交利物浦大学

Integrated Electronics & Design

Lecture 1: Introduction

**Department of Electronics and
Electrical Engineering**

Dr. Gary, Chun ZHAO

Feb. 2018



On all slides of this Module

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- Semiconductor integrated optics and solar cells
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outline

- On the Module
- History of semiconductor devices and ICs
- **Moore's law**
 - Transistor scaling
- **Yield**
- 45nm node and ALD

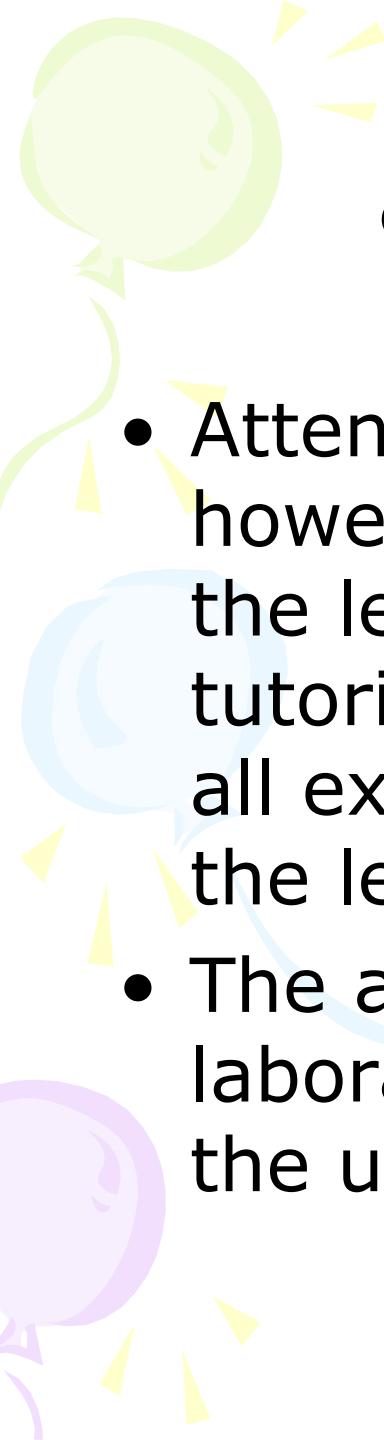
the state-of-the-art tech.



assessment system

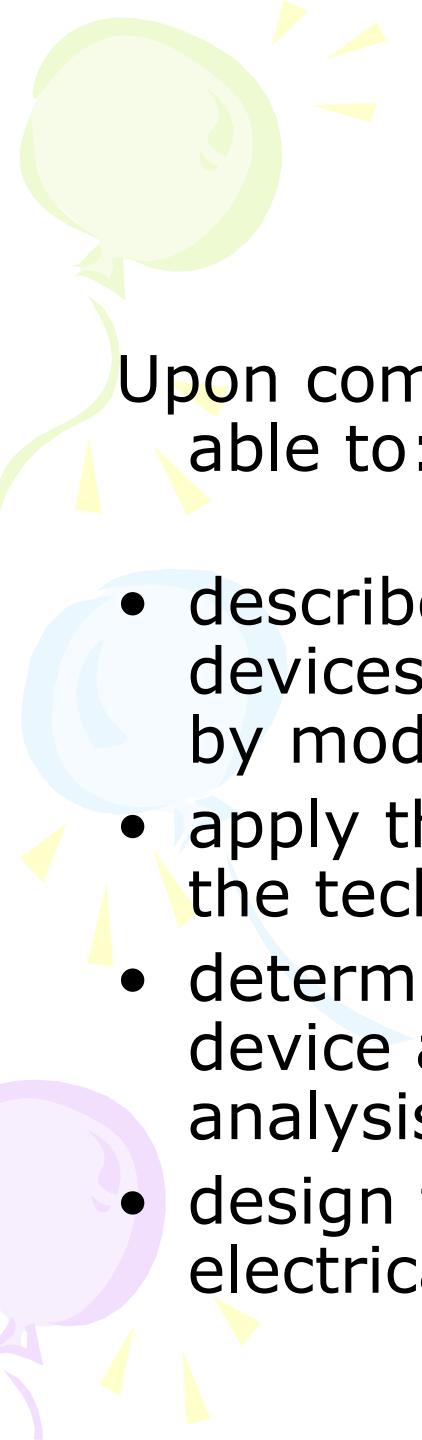
| method | % | distribution |
|---|------------|-----------------|
| assignment (homework, but class check) | 5% | 2 x 2.5% |
| Mid-term test | 10% | Week 7 |
| IC Design project | 15% | Paper design |
| Final exam | 70% | After week14 |

Randomly



attendance policy

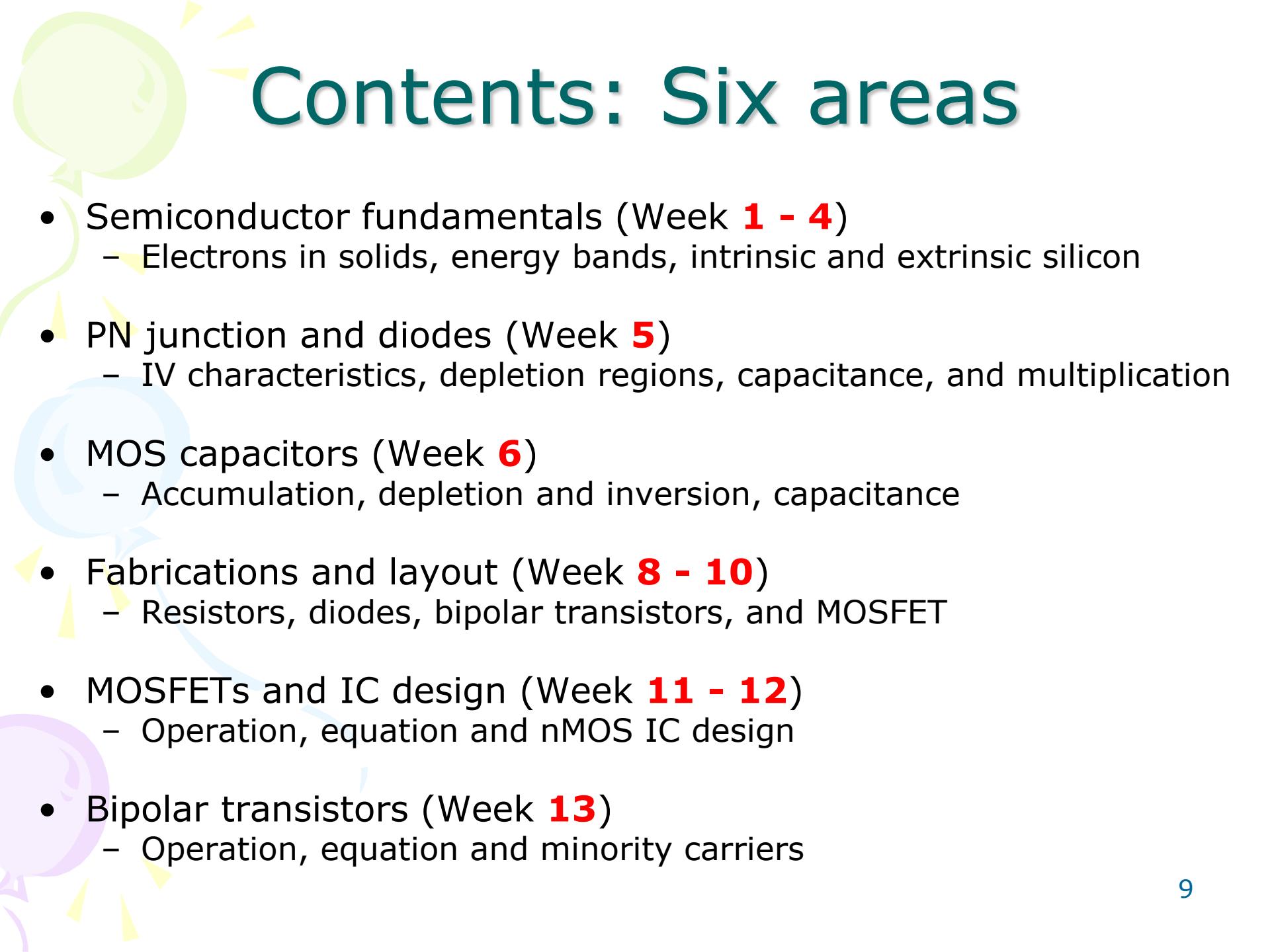
- Attending the lectures is not obligatory, however note that the material covered in the lectures will not be repeated in tutorials, and that it is not possible to put all explanations and comments made in the lecture on the web page or in script.
- The attendance policy for the tutorial and laboratory and the dropping policy follow the university rules and policies.



Module objective

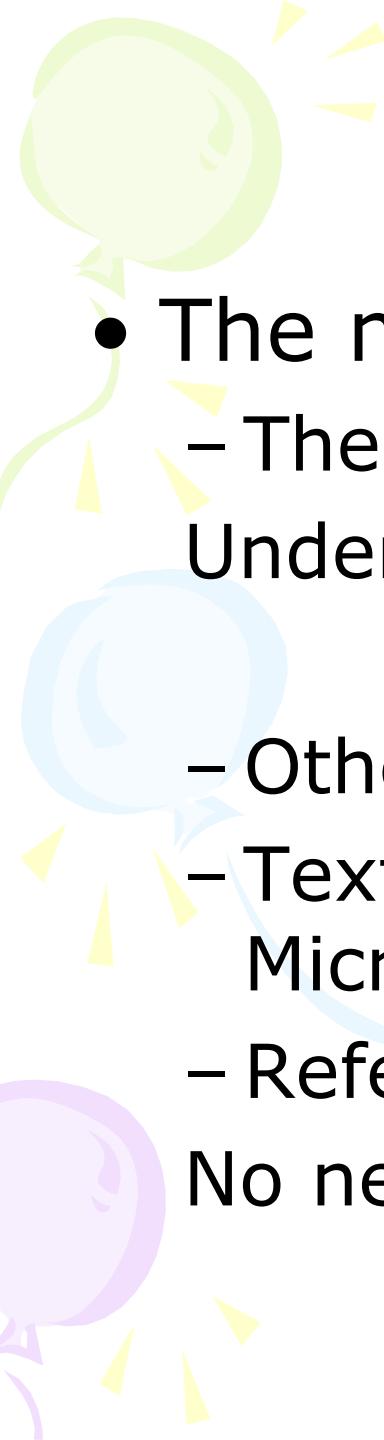
Upon completing this Module, the student shall be able to:

- describe the operation of basic semiconductor devices in words, by mathematical equations and by models
- apply the proper semiconductor device to solve the technical problem,
- determine the electrical characteristics of the device and apply them for electronic circuit analysis,
- design the semiconductor structure fulfilling the electrical parameter specifications.



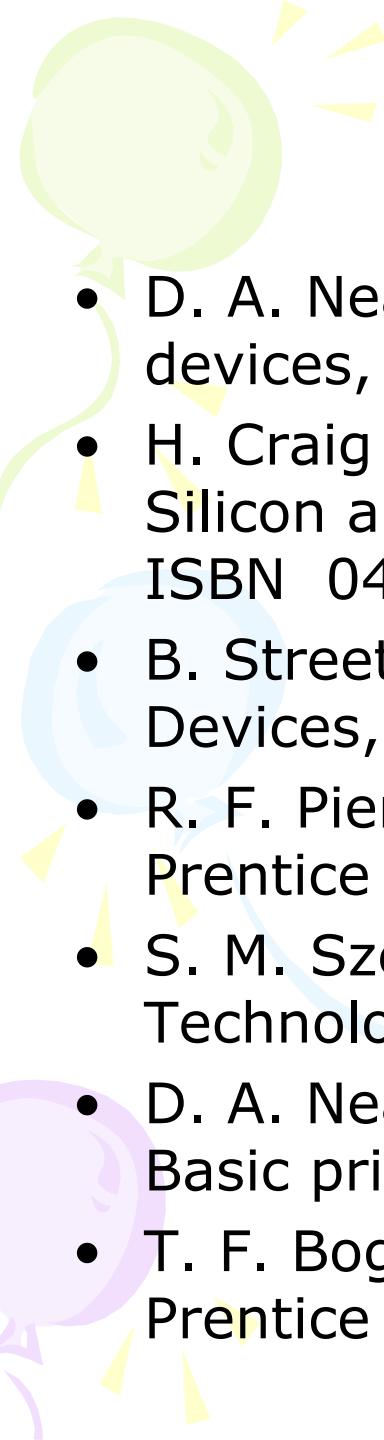
Contents: Six areas

- Semiconductor fundamentals (Week **1 - 4**)
 - Electrons in solids, energy bands, intrinsic and extrinsic silicon
- PN junction and diodes (Week **5**)
 - IV characteristics, depletion regions, capacitance, and multiplication
- MOS capacitors (Week **6**)
 - Accumulation, depletion and inversion, capacitance
- Fabrications and layout (Week **8 - 10**)
 - Resistors, diodes, bipolar transistors, and MOSFET
- MOSFETs and IC design (Week **11 - 12**)
 - Operation, equation and nMOS IC design
- Bipolar transistors (Week **13**)
 - Operation, equation and minority carriers



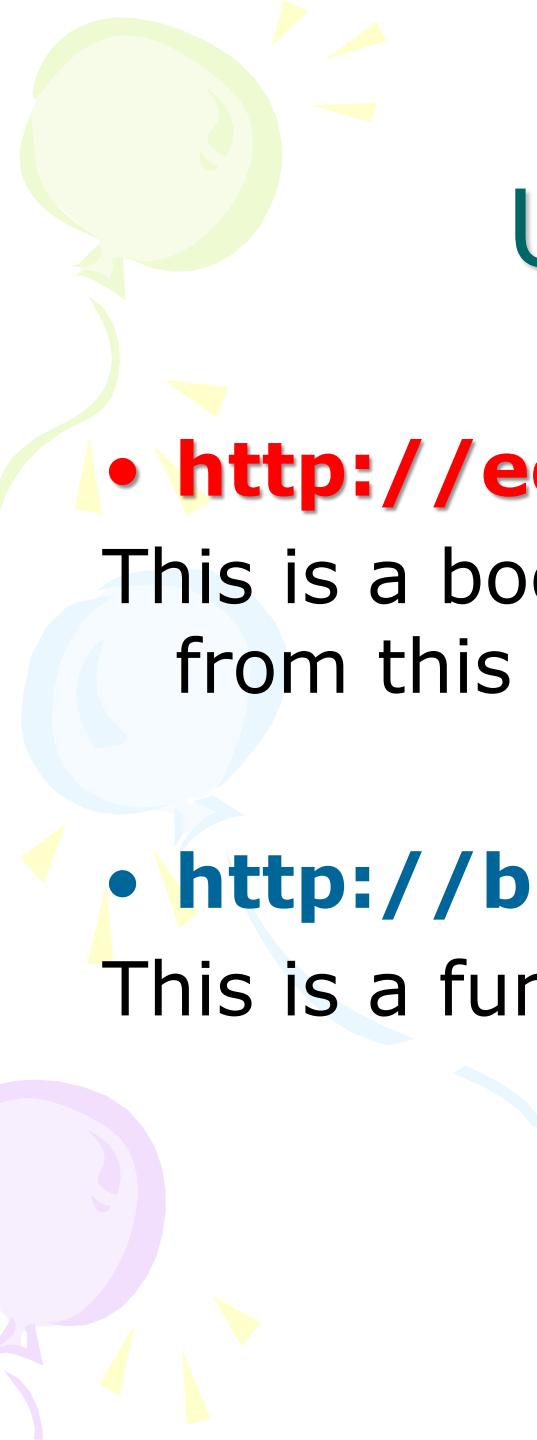
References

- The most important one
 - The handouts!
Understand them from cover to cover
 - Others
 - Textbook (An Introduction to Microelectronics, by C.Z. ZHAO et al.)
 - Reference books (see next slide)
- No need for reading from cover to cover



Reference books

- D. A. Neamen (2006). An introduction to semiconductor devices, 清华大学出版社. ISBN 978 7 302 12451 1.
- H. Craig Casey (1998). Devices for Integrated Circuits: Silicon and III-V Compound Semiconductors, Wiley & So., ISBN 0471171344.
- B. Streetman, S. Banerjee (1999). Solid State Electronic Devices, Prentice Hall, ISBN 0130255386.
- R. F. Pierret (1995). Semiconductor Device Fundamentals, Prentice Hall, ISBN 0201543931.
- S. M. Sze (2001). Semiconductor Devices: Physics and Technology, Wiley & So., ISBN 0471333727.
- D. A. Neamen (2003). Semiconductor physics and devices: Basic principles, McGraw-Hill, ISBN 0072321075.
- T. F. Bogart (1997). Electronic devices and circuits, Prentice Hall, ISBN 0133937607.



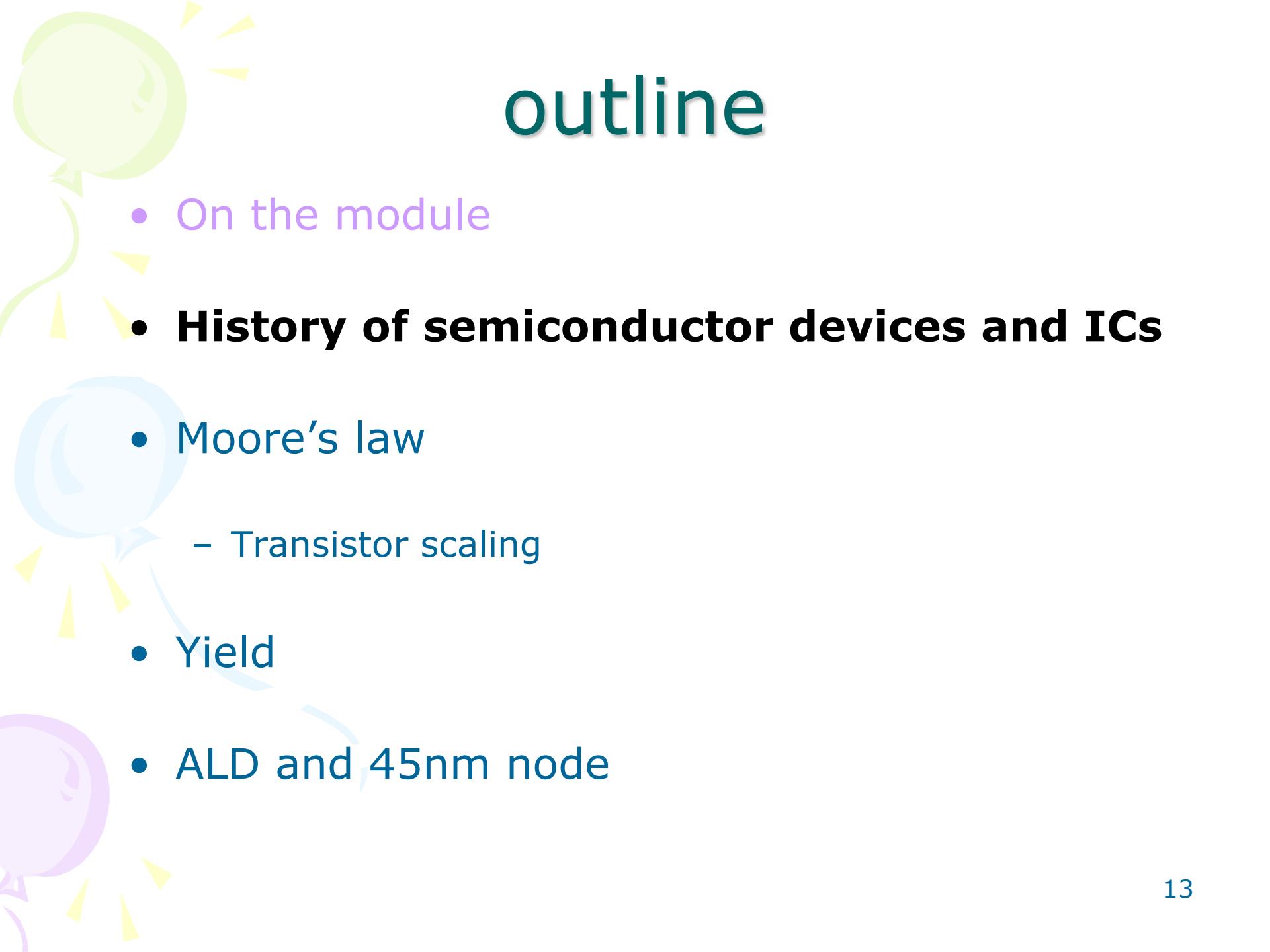
Useful Web Sites

- **<http://ece.colorado.edu/~bart/book/>**

This is a book. You can get almost everything from this book

- **<http://britneyspears.ac/lasers.htm>**

This is a funny website.



outline

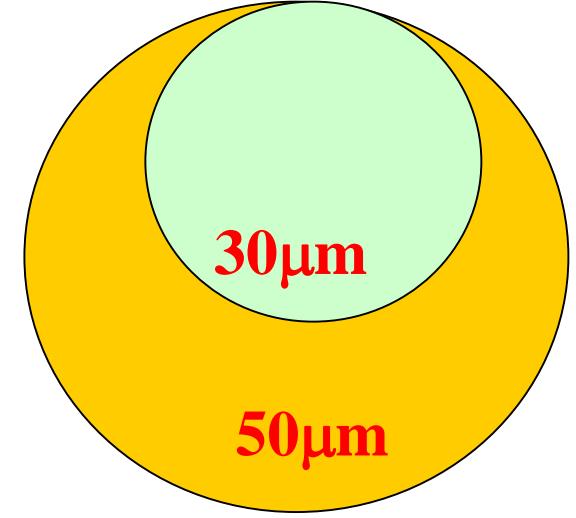
- On the module
- **History of semiconductor devices and ICs**
- Moore's law
 - Transistor scaling
- Yield
- ALD and 45nm node

What is the size of a transistor nowadays?



100 μ m

The size of a human
hair



30 μ m

50 μ m

30~50 μ m
(the size of a skin cell)

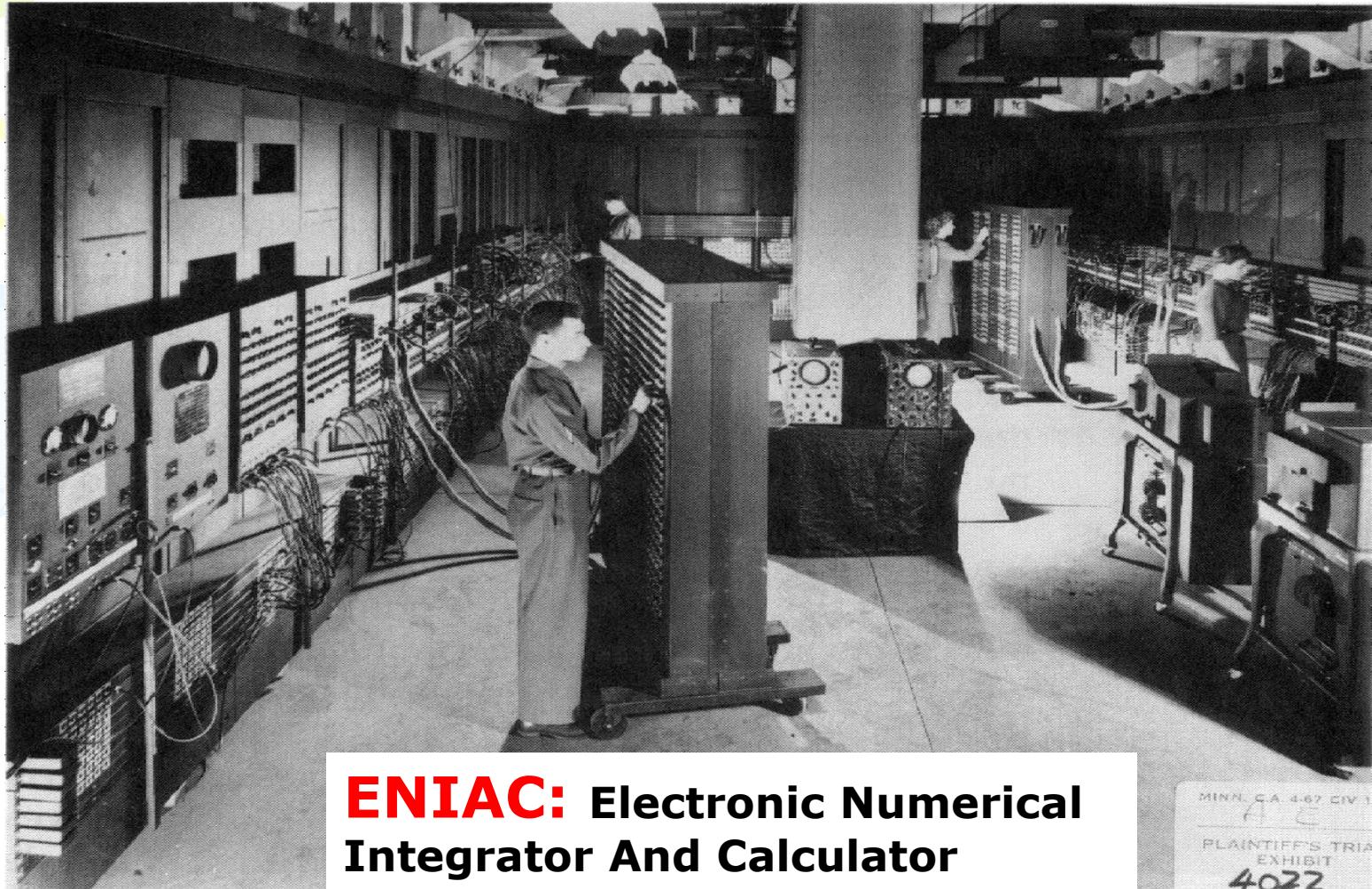
- 1 μ m × 1 μ m
(in 1990s, the size
of a transistor)

1940's: Vacuum tube era

- Vacuum tubes were used for radios, television, telephone equipment, and computers
- ... but they were expensive, bulky, fragile, and energy-hungry



1946: First electronic computer



ENIAC: Electronic Numerical Integrator And Calculator

Real size: 3000 cubic foot

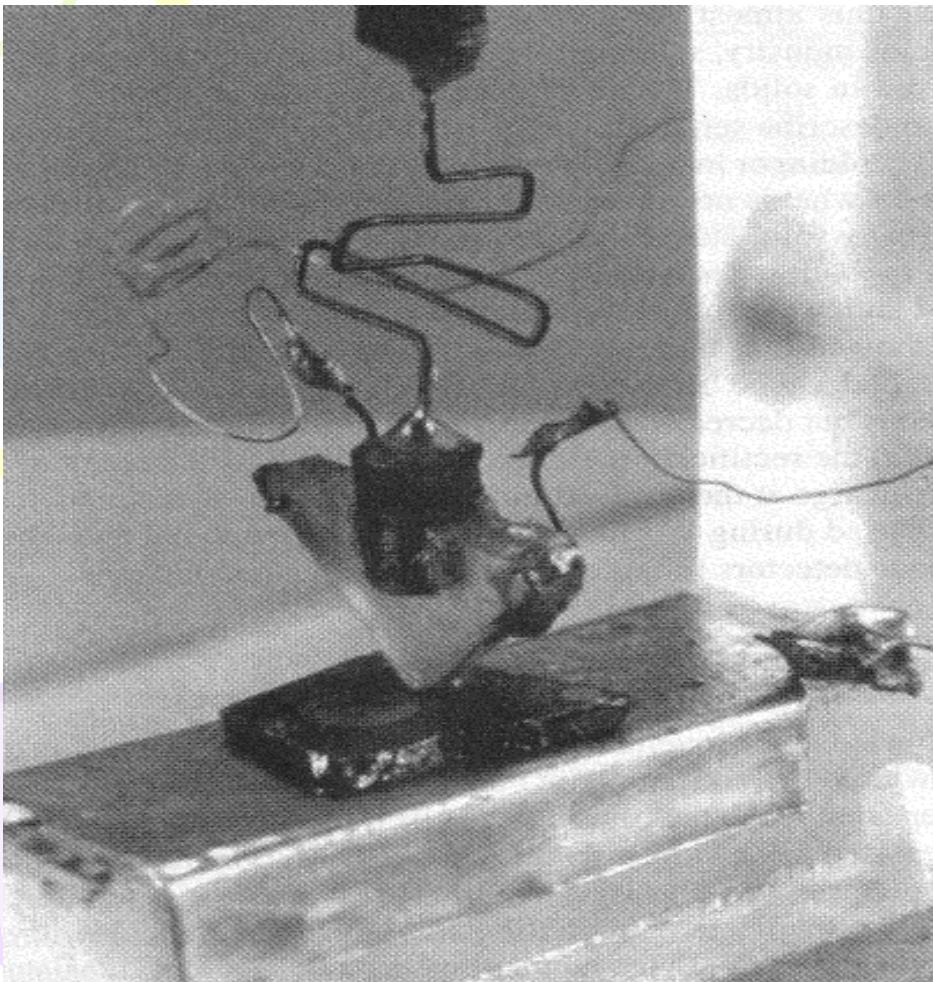
(1 foot =0.3048m) ¹⁶

ENIAC - The first electronic computer (1946)

- **1945**
- ENIAC filled an entire room!
17,468 vacuum tubes,
70,000 resistors, and
10,000 capacitors
6,000 manual switches
and many blinking lights!
- could add 5,000 numbers in
a single second



1947: First transistor



Picture shows a **point-contact transistor** structure comprising the plate of n-type **germanium** and two line-contacts of gold supported on a plastic wedge.

Source:

W. Shockley,
“The path to the conception of
the junction transistor”,
IEEE Tr. on Electron Devices
ED-23, 597 (1976).

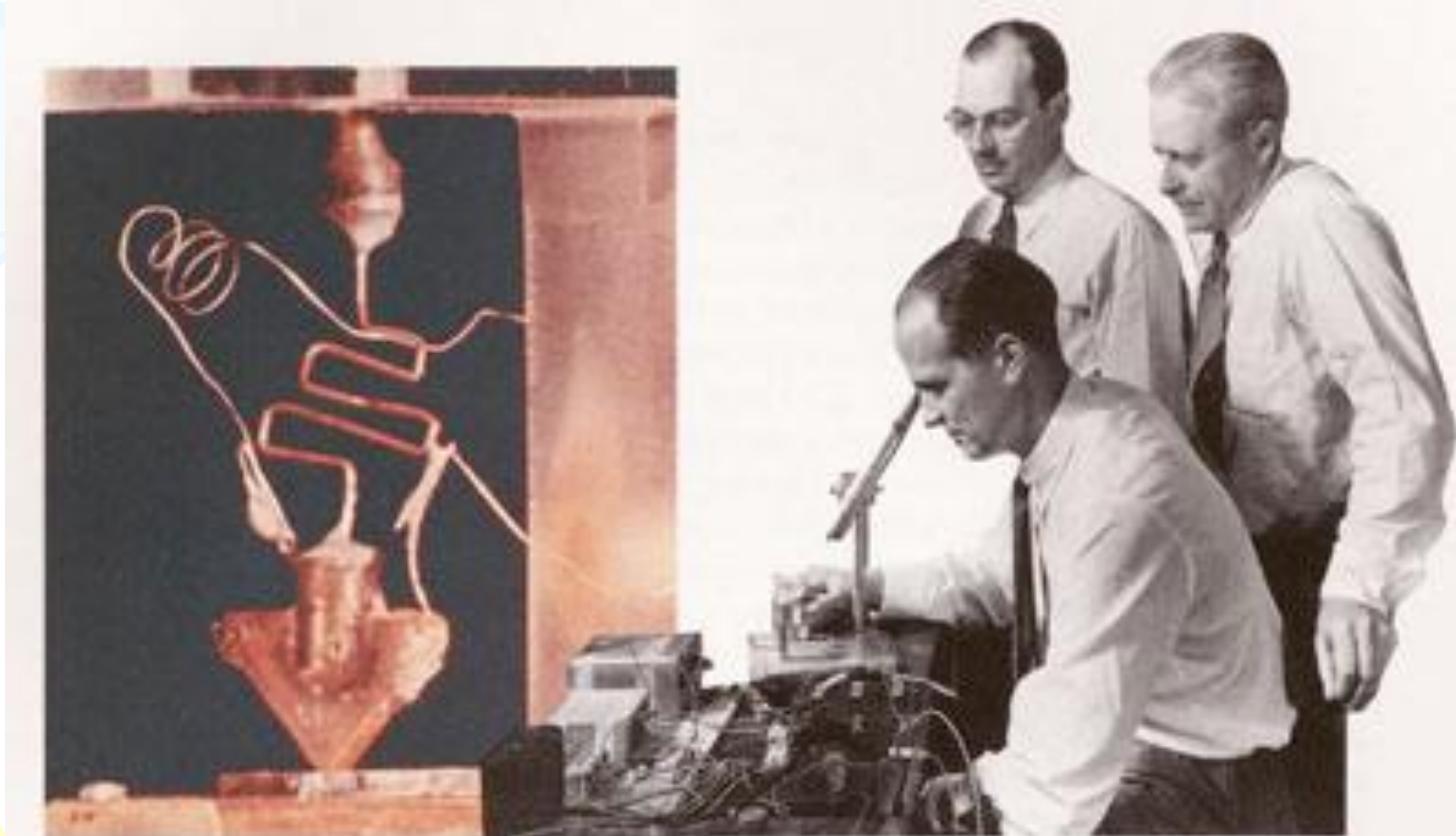


New York Times: Dec. 23rd 1947

"A device called a transistor, which has several applications in radio where a vacuum tube ordinarily is employed, was demonstrated for the first time yesterday at Bell Telephone Laboratories, 463 West Street, where it was invented."

The transistor is the defining invention of the 20th Century

- **First transistor (by Bardeen, Shockley and Brattain 1947): The Transistor Revolution**



The Nobel Prize in Physics: 1956



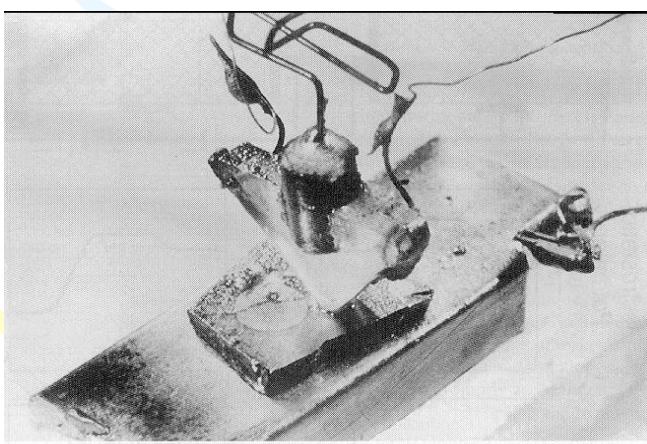
William Shockley



John Bardeen



Walter Brattain



- reproducibility was an issue, however.

1950: First Si BJT

- Invention of the bipolar junction transistor (BJT)
 - William Shockley, *Bell Labs, 1950*
 - more stable and reliable; easier and cheaper to make

1954: First commercial BJT

- In 1954, **Texas Instruments** produced the first commercial silicon transistor.
- **Discrete Electronic Circuits**

分离器件

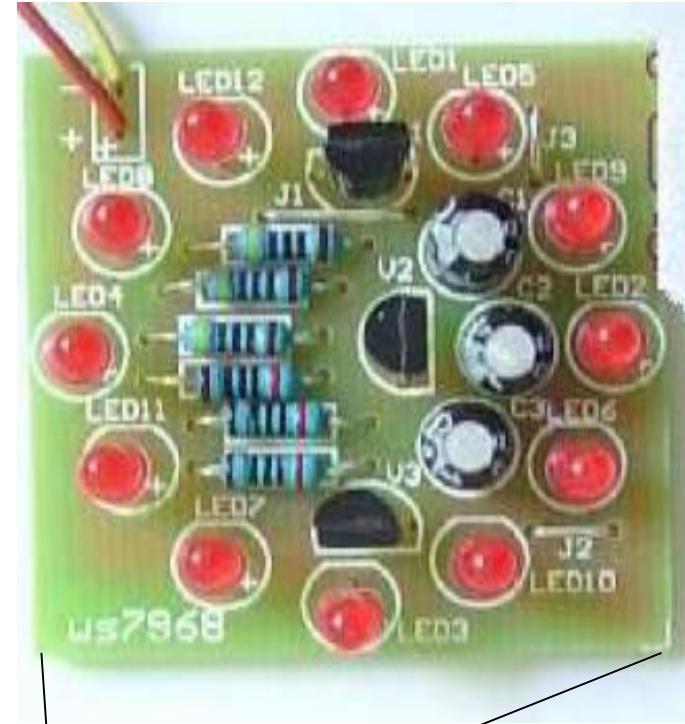
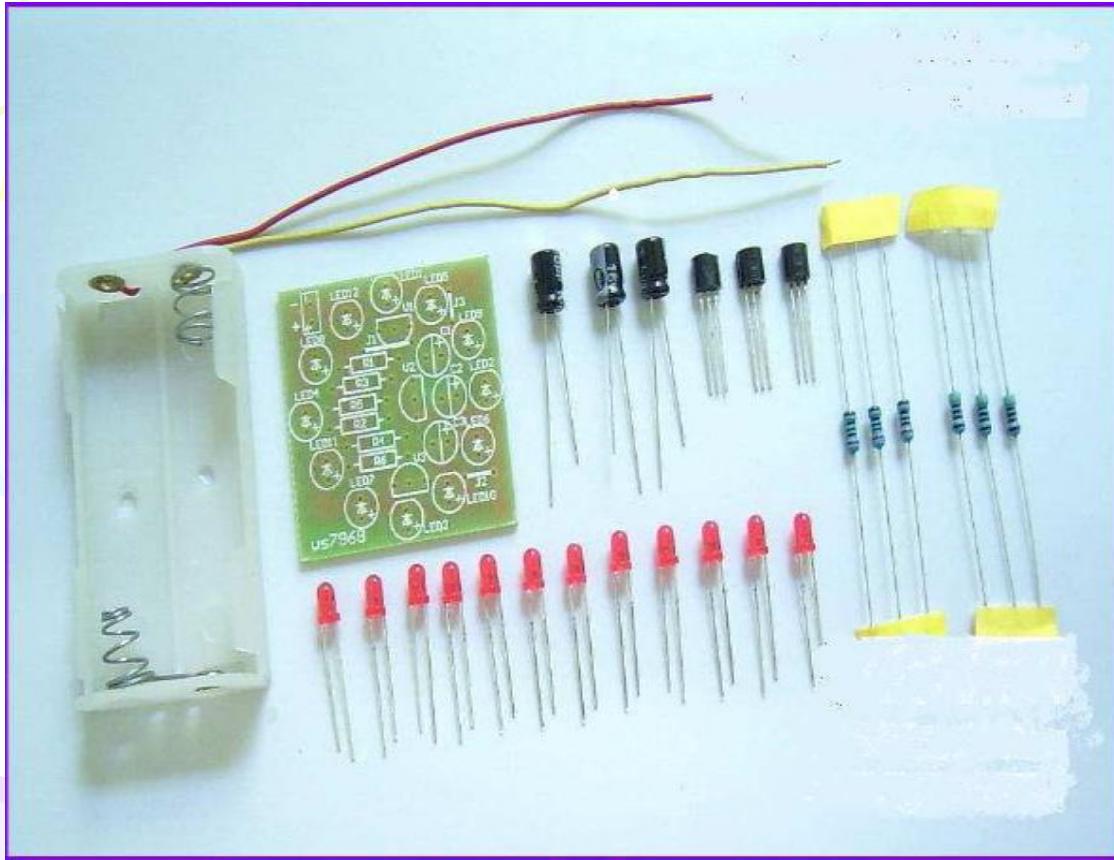
~\$2.50 each



- Before the invention of the integrated circuit, electronic equipment was composed of discrete components such as transistors, resistors, and capacitors. These components, often simply called “discretes”, were manufactured separately and were wired or soldered together onto circuit boards. Discretes took up a lot of room and were expensive and cumbersome to assemble, so engineers began, in the mid-1950s, to search for a simpler approach...

1) Discrete Electronic Circuits

- PCB circuits will not be discussed.



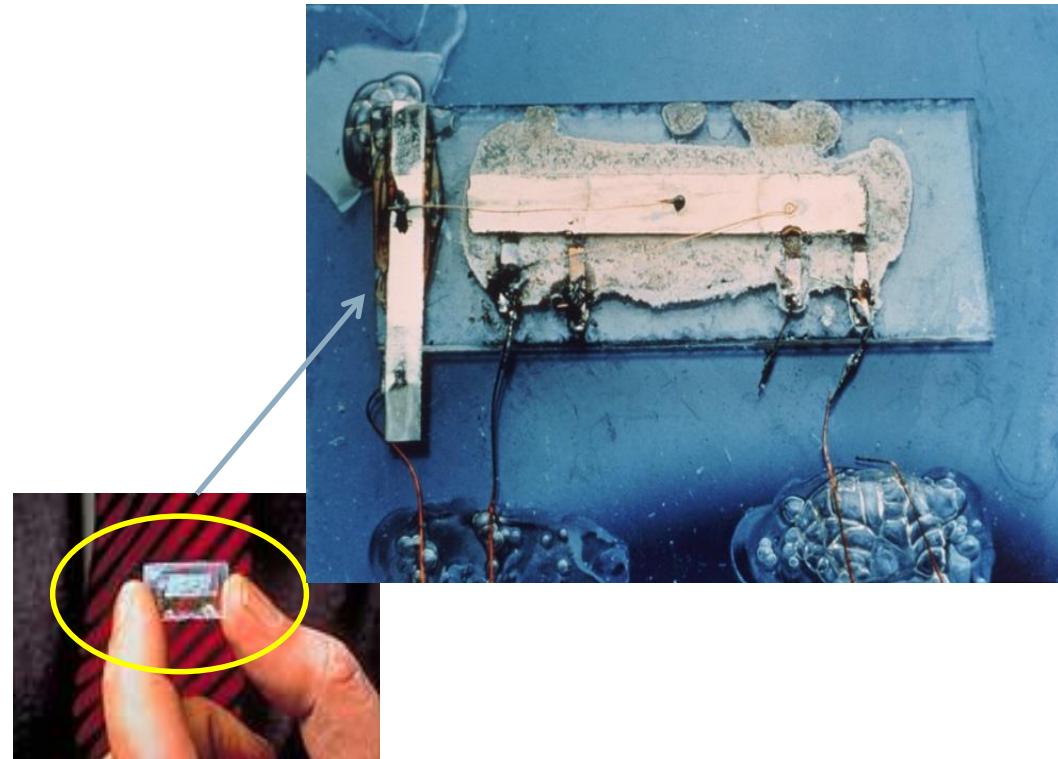
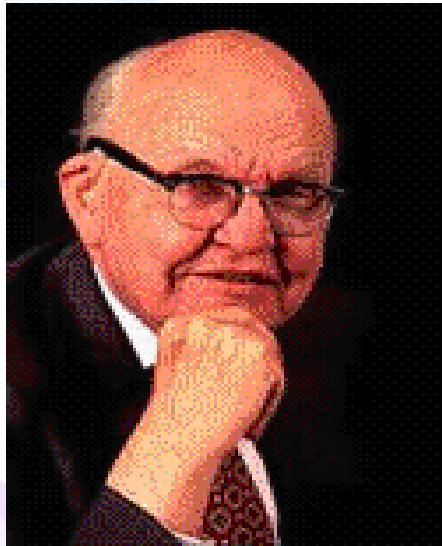
2) Integrated Circuits

- this is the module's issue

$1\mu\text{m} \times 1\mu\text{m}$
(in 1990s, the size
of a transistor)²⁴

1958: 1st Integrated Circuit

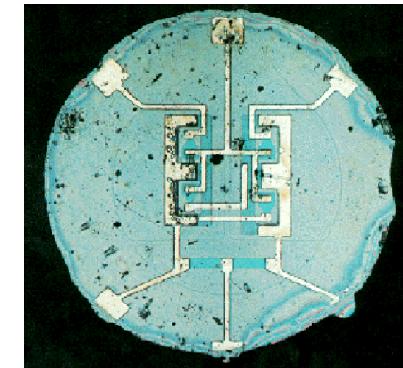
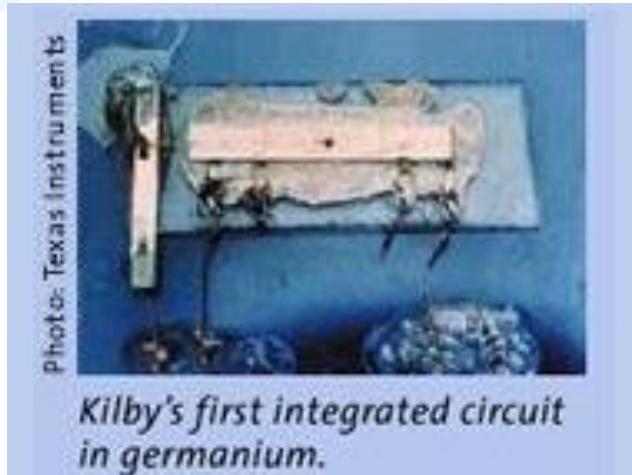
- A British idea: 1952 G. Dummer
- American fabrication: 1958 Jack Kilby
- No. of components: 12



(1923-2005), received the Nobel Prize in 2000 in Physics

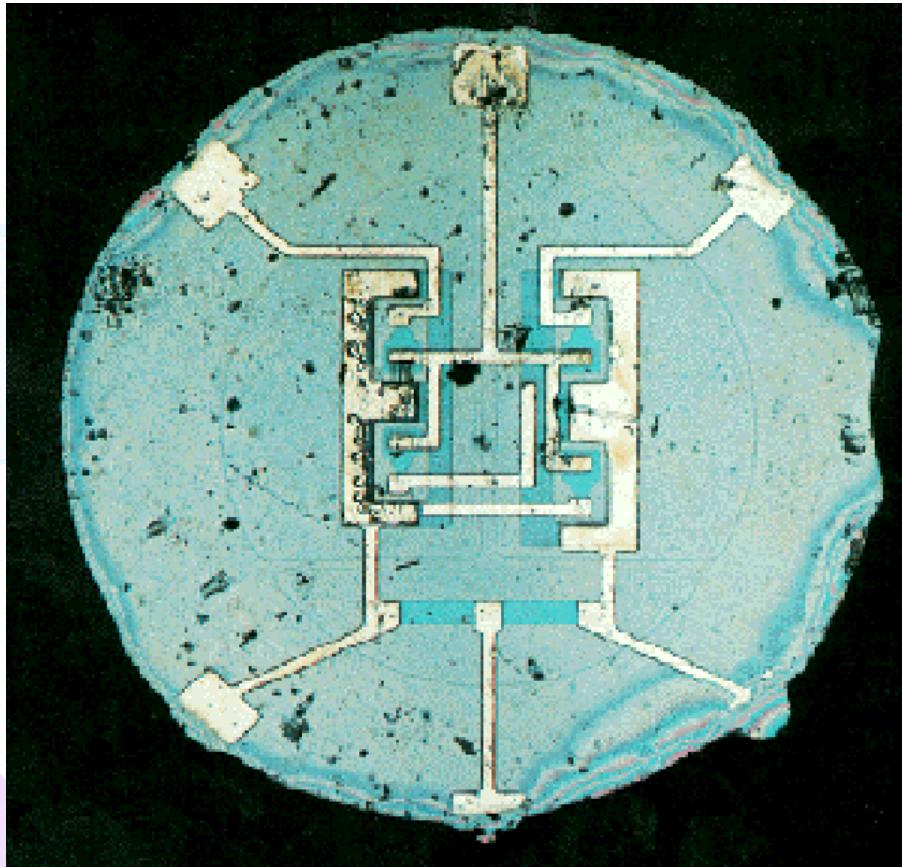
The Integrated Circuit (IC)

- An IC consists of interconnected electronic components in a single piece ("chip") of semiconductor material.
- In 1958, Jack S. Kilby (*Texas Instruments*) showed that it was possible to fabricate a simple IC in germanium.
- In 1959, Robert Noyce (*Fairchild Semiconductor*) demonstrated an IC made in silicon using SiO_2 as the insulator and Al for the metallic interconnects.



The first planar IC
(actual size: 0.06 in. diameter)

1959: First Monolithic IC



Picture shows a flip-flop circuit containing 6 devices, produced in **planar technology**.

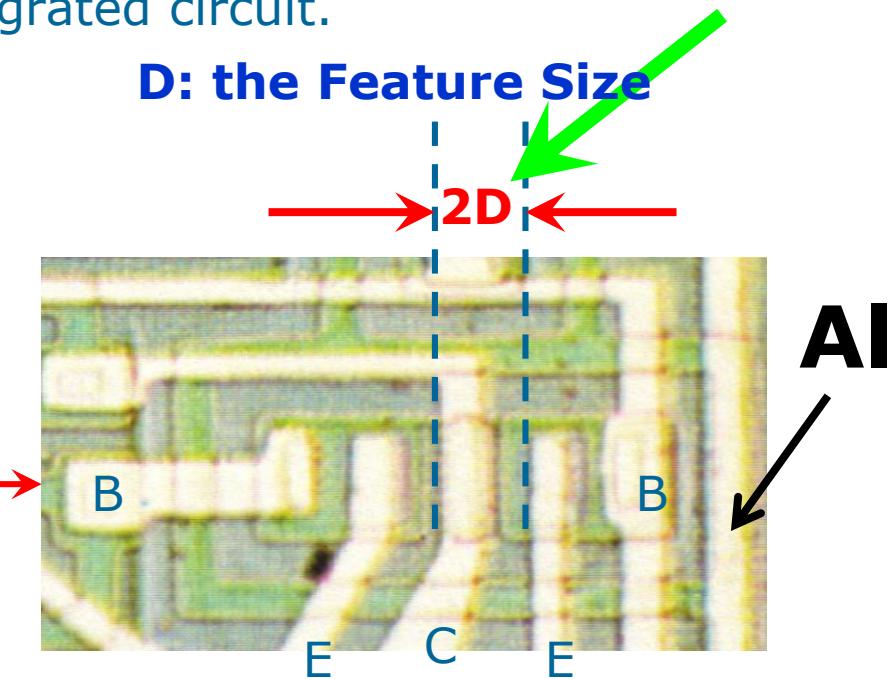
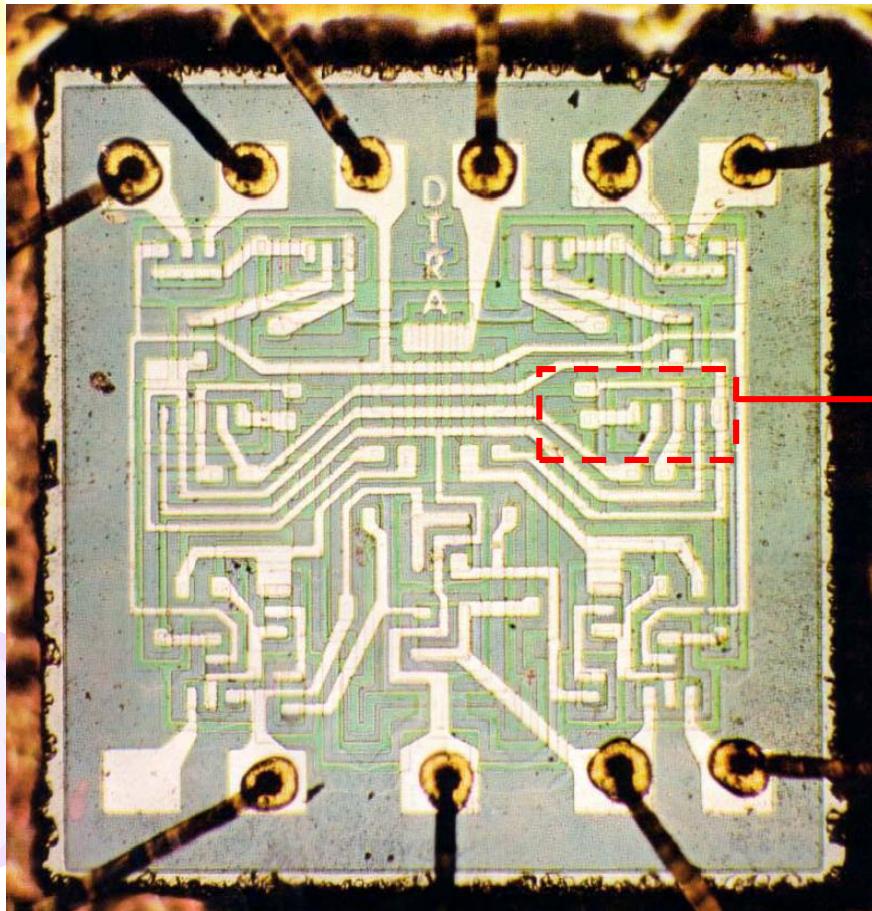
Source:

R. N. Neyce, "Semiconductor device-and-lead structure",
U.S.Patent 2,981,877

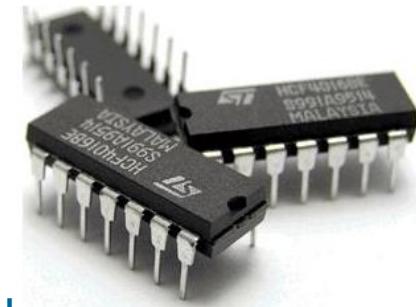
<http://www.computerhistory.org/semiconductor/timeline/1960-FirstIC.html>

A Fairchild Semiconductor digital (DTL) IC from 1964

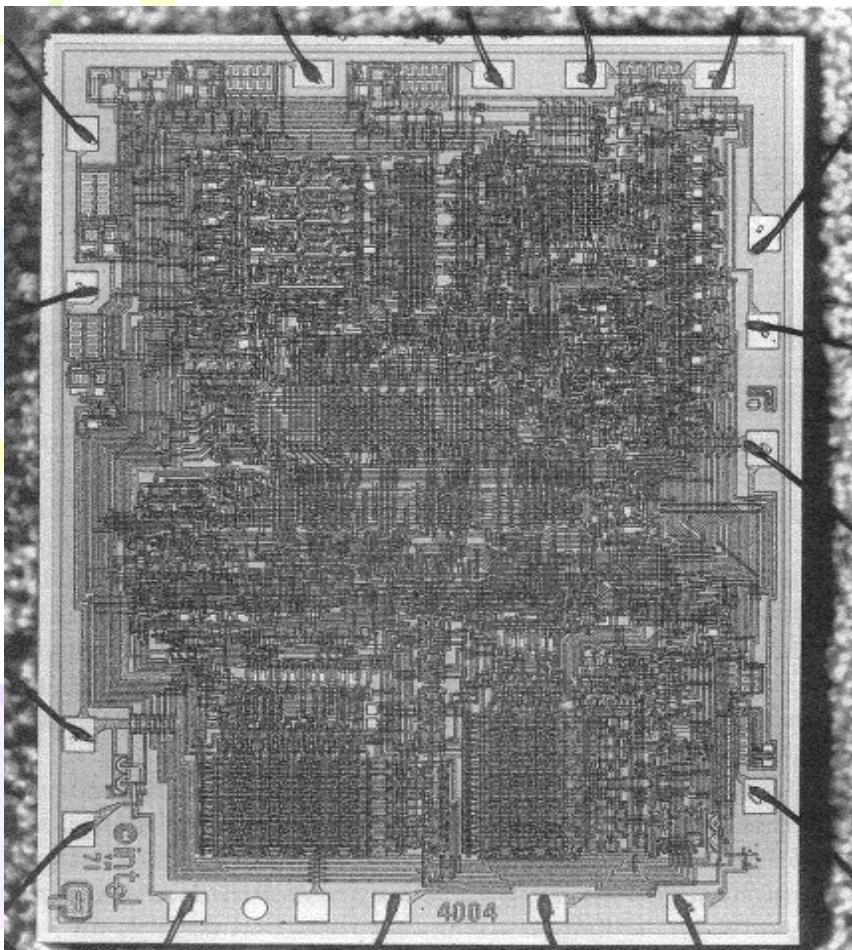
- Images courtesy of Fairchild Semiconductor. Used without permission. An early bipolar integrated circuit.



"D" represents IC technology level.
The names of "D", nowadays:
"D technology", or
"Generation D", or "D node"



1971: first microprocessor

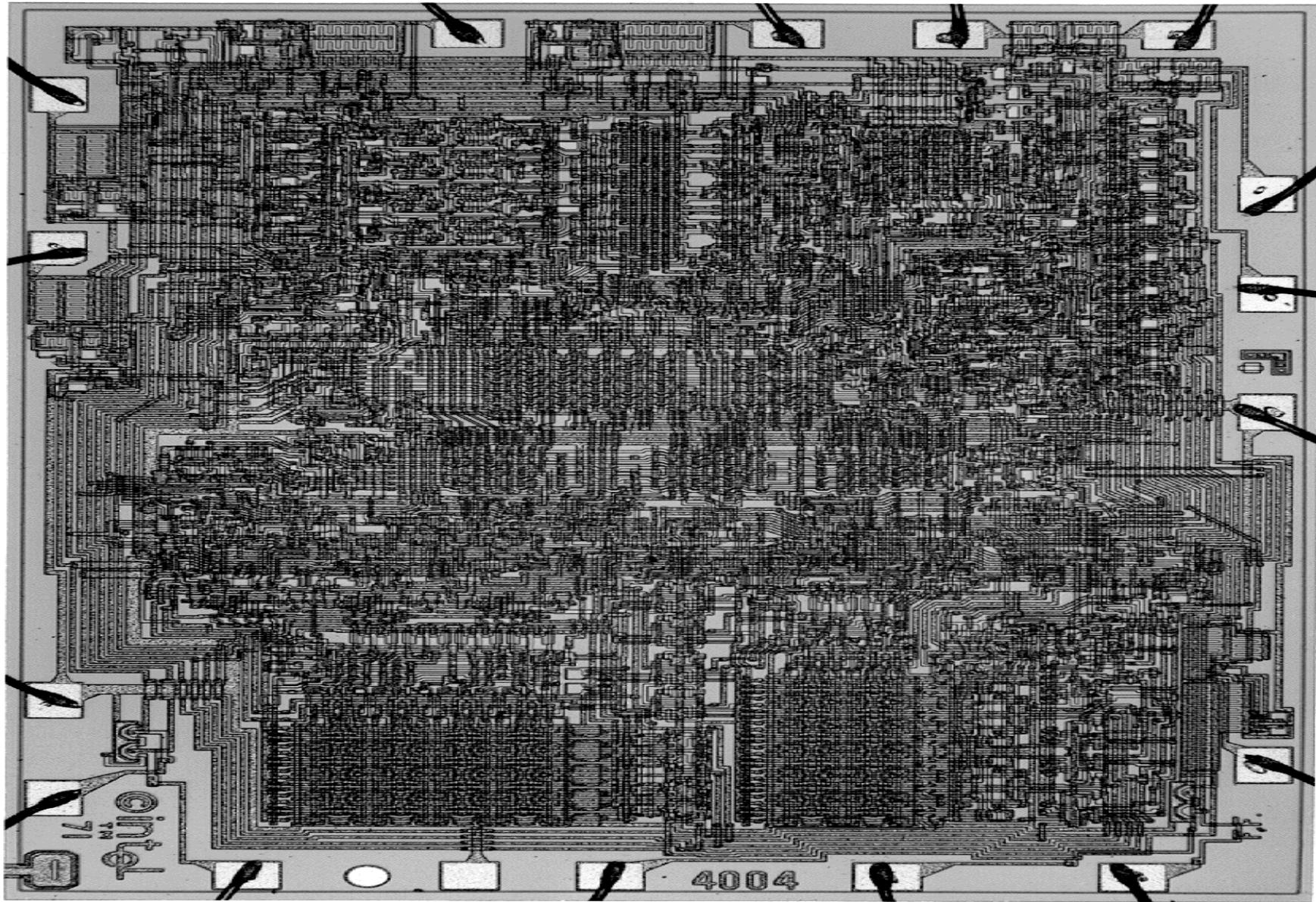


Picture shows a four-bit microprocessor **Intel 4004**.

- **10 μm technology**
- 3 mm \times 4 mm
- 2300 MOSFETs
- 108 kHz clock frequency

Source:
Intel Corporation

Intel 4004 Micro-Processor

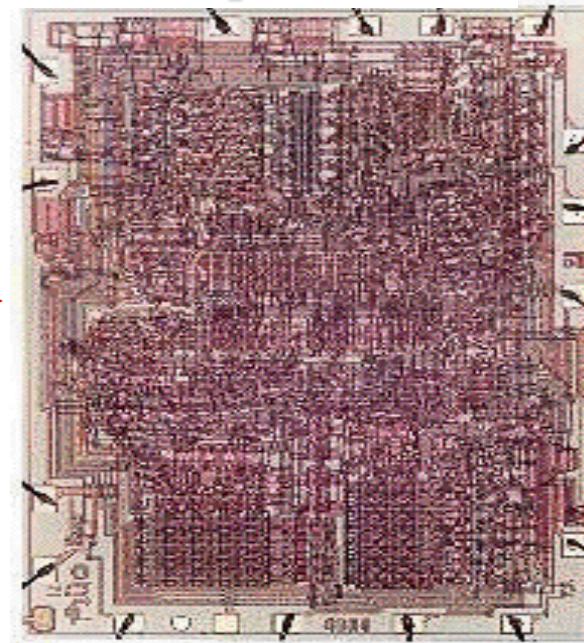


History: The 1st microprocessor

- Invented by Intel in 1971, 4004
- The basic structure for 'computing'

“Honey, I shrank the computer”

1 foot
=0.3048m



ENIAC --- 1946

Real size: 3000 cubic foot

4004 --- 1971

Real size: Thumbnail

1 μm technology at XJTLU

Semiconductor
manufacturing
processes

- 10 μm – 1971
- 3 μm – 1975
- 1.5 μm – 1982
- 1 μm – 1985
- .80 μm – 1989
- .60 μm – 1994
- .35 μm – 1995
- .25 μm – 1998
- .18 μm – 1999
- .13 μm – 2000
- 90 nm – 2002
- 65 nm – 2006
- 45 nm – 2008
- 32 nm – 2010
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018
- 5 nm – 2020



1997: Pentium II processor

Intel Pentium II

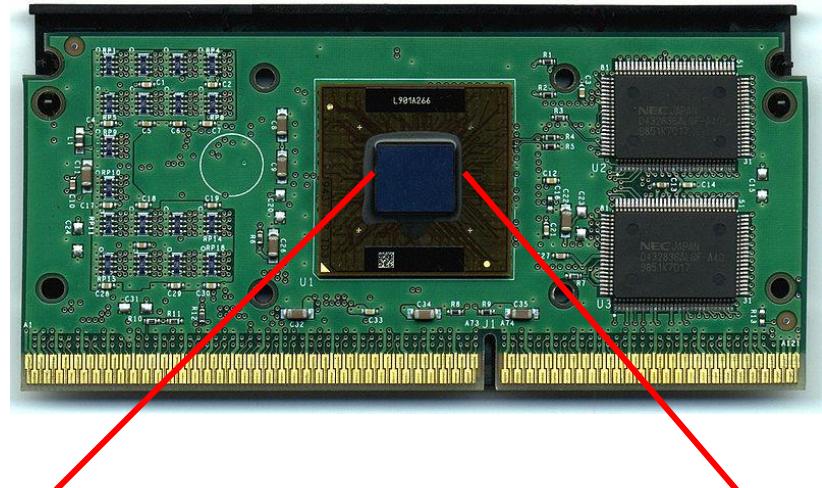
100's MHz

➤ 3 million transistors

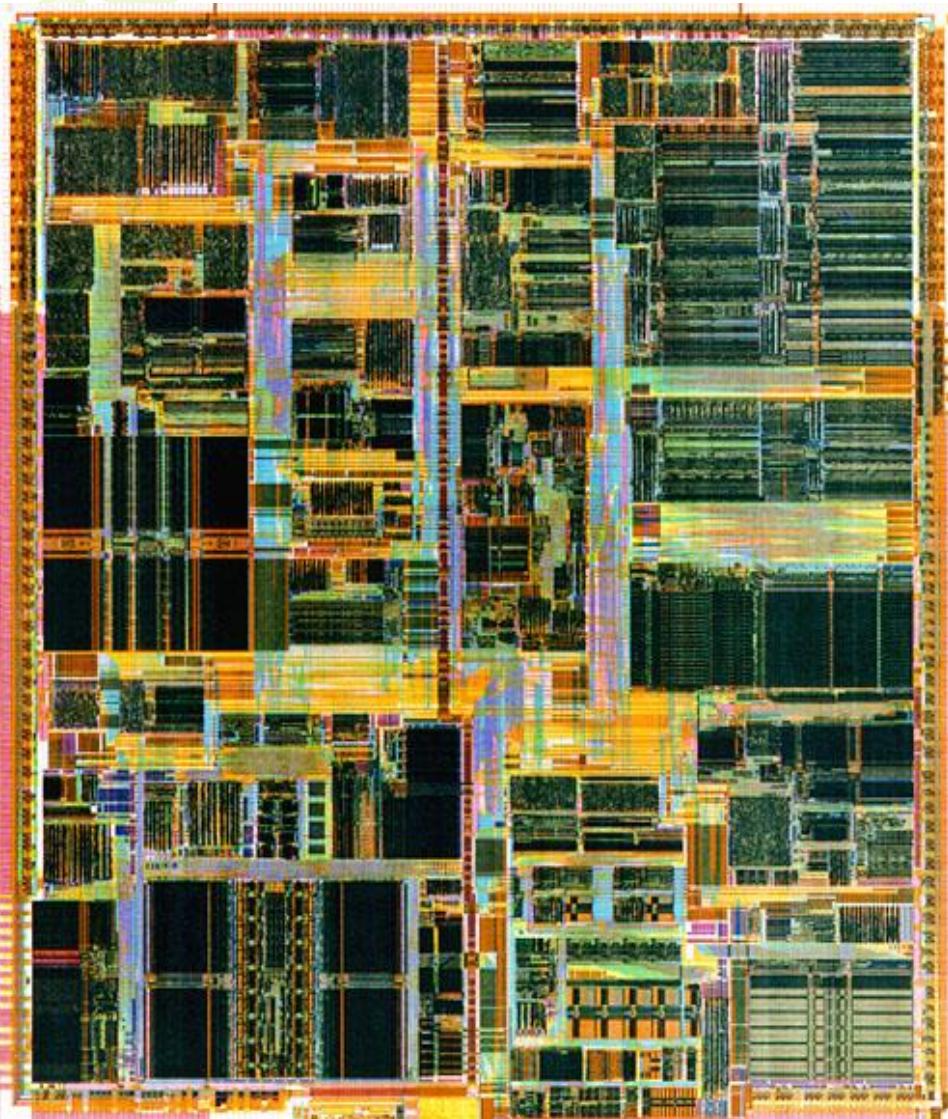
163mm² chip

0.6 µm technology

8W power consumption



2001: Pentium IV processor



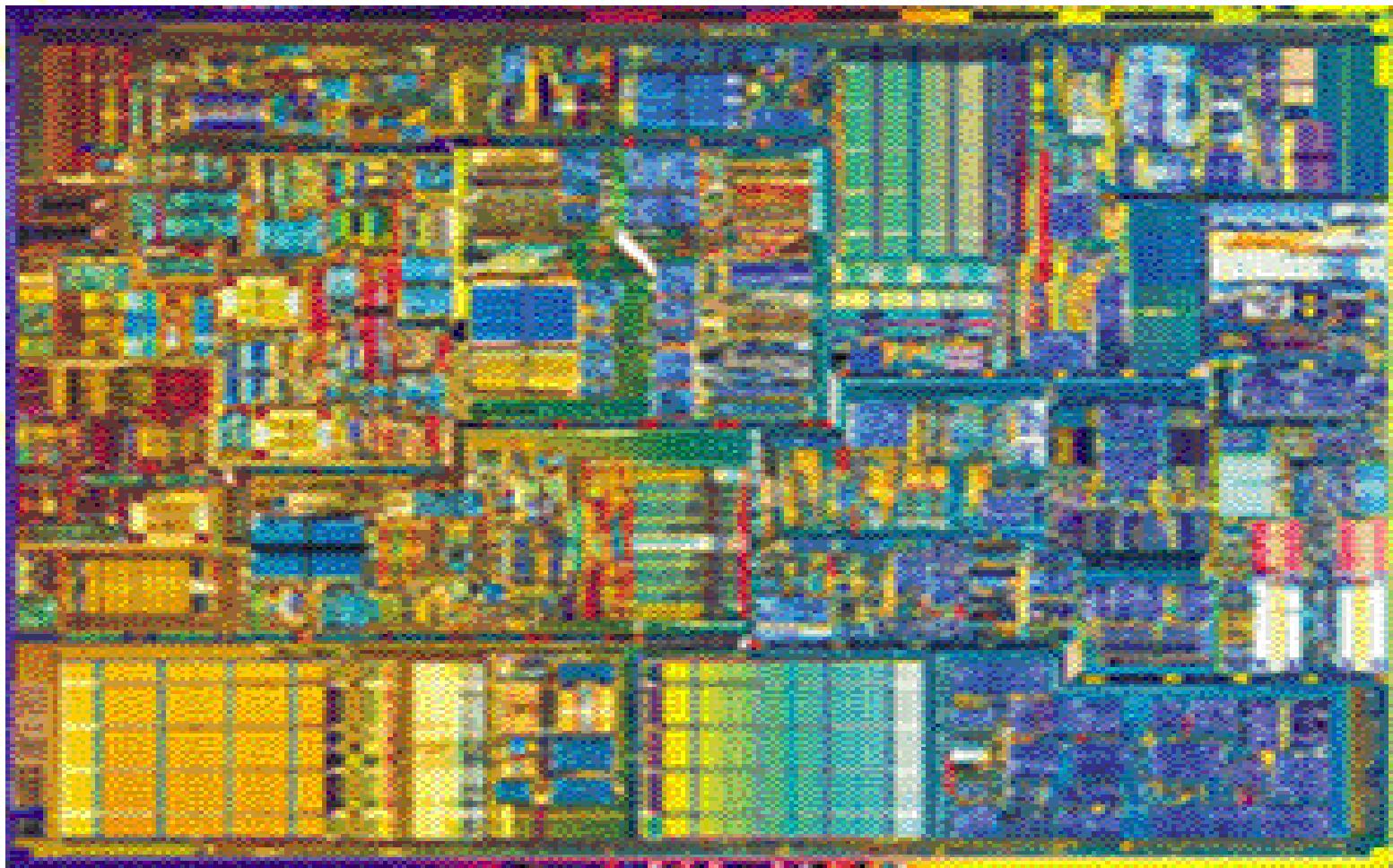
Picture shows a ULSI chip with 32-bit processor
Intel Pentium 4.

- 0.18 μ m CMOS technology
- 17.5 mm × 19 mm
- 42 000 000 components
- 1.6 GHz clock frequency

Source:
Intel Corporation

2002: Pentium IV processor

- Pentium 4: Intel---April 2, 2002
 - 0.13um; 2.4GHz; 55million transistors



2009-01-18: Intel Core™ i7 processor



Picture shows a ULSI chip with single core processor

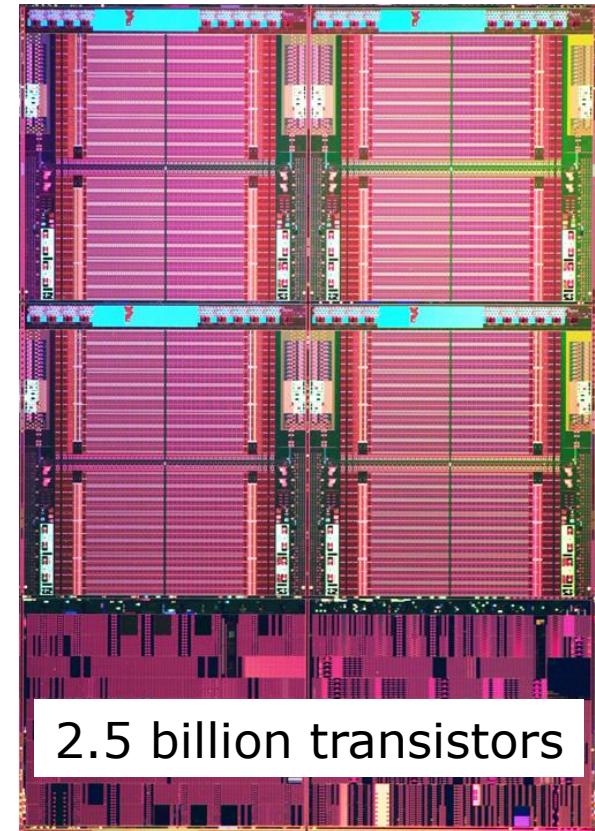
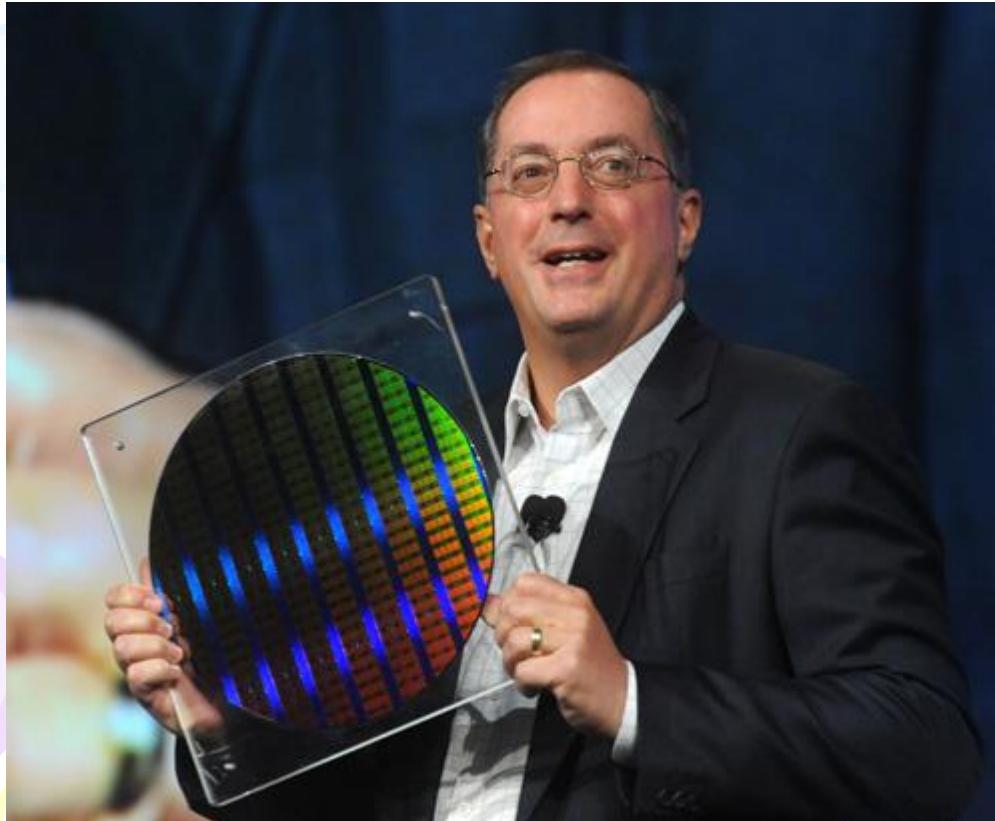
- **45nm** CMOS technology
- For a **8** core processor:
3.2 GHz clock frequency

Source:
Intel Corporation

45 nm feature size
Over 1 billion transistors

2009-09-22: Intel shows 22nm processor technology

- 32nm entered full scale production in 2010 and made **22nm** in **2011** and will make 14nm in 2013.





IMEC

<http://www2.imec.be/>

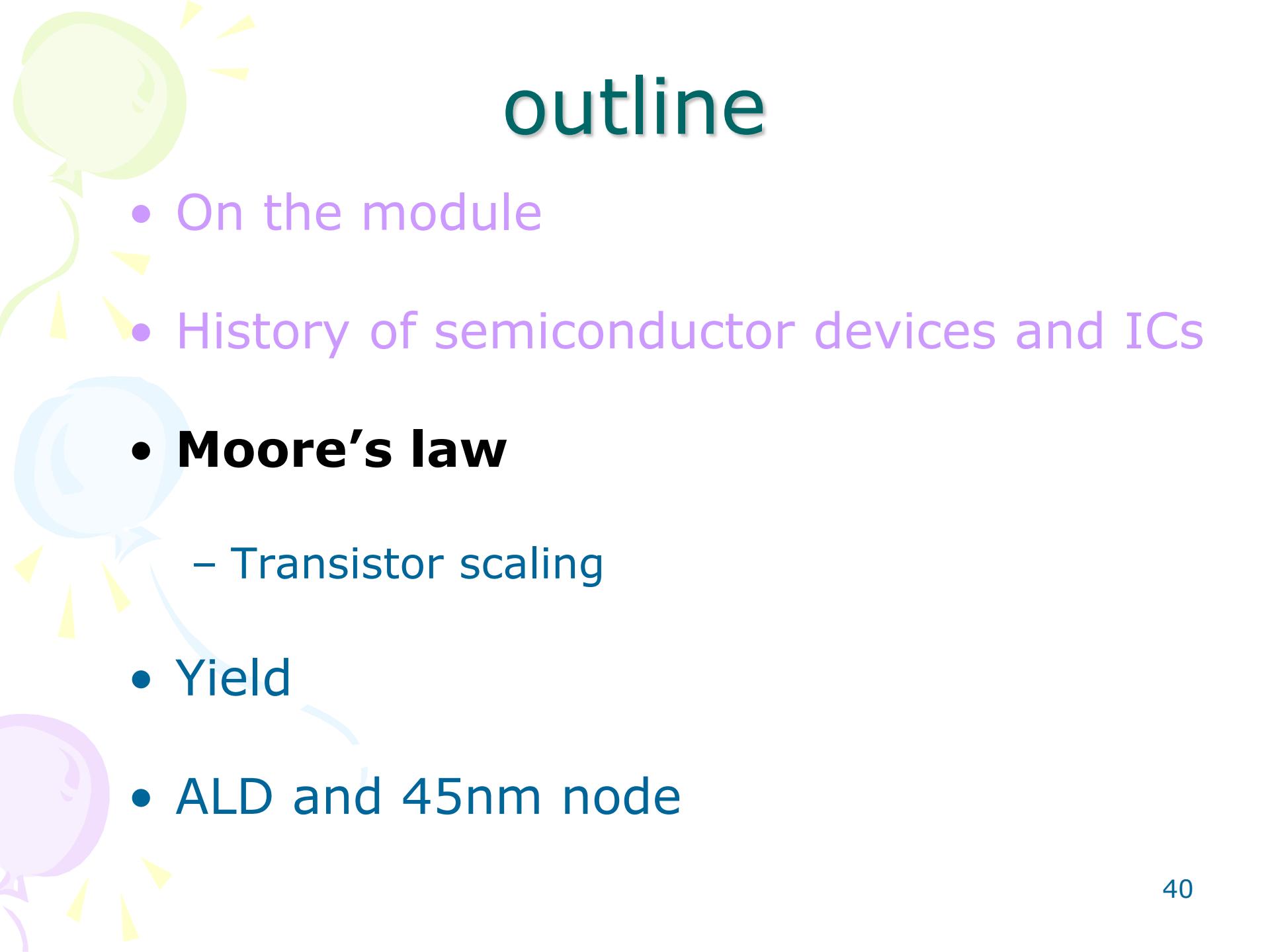
- IMEC is Europe's largest independent research center in nano-electronics and nano-technology. Over 1,600 employees coming from all over the world work at IMEC's campus.
- IMEC's research is applied in better healthcare, smart electronics, sustainable energy, and safer transport.

http://www.smics.com/website/cnVersion/About_SMIC/aboutUs.htm



中芯国际集成电路制造有限公司
Semiconductor Manufacturing International Corporation

- Semiconductor Manufacturing International Corporation is one of the leading semiconductor foundries in the world and the largest and most advanced foundry in Mainland China (Shanghai).



outline

- On the module
- History of semiconductor devices and ICs
- **Moore's law**
 - Transistor scaling
- Yield
- ALD and 45nm node



Moore's Law

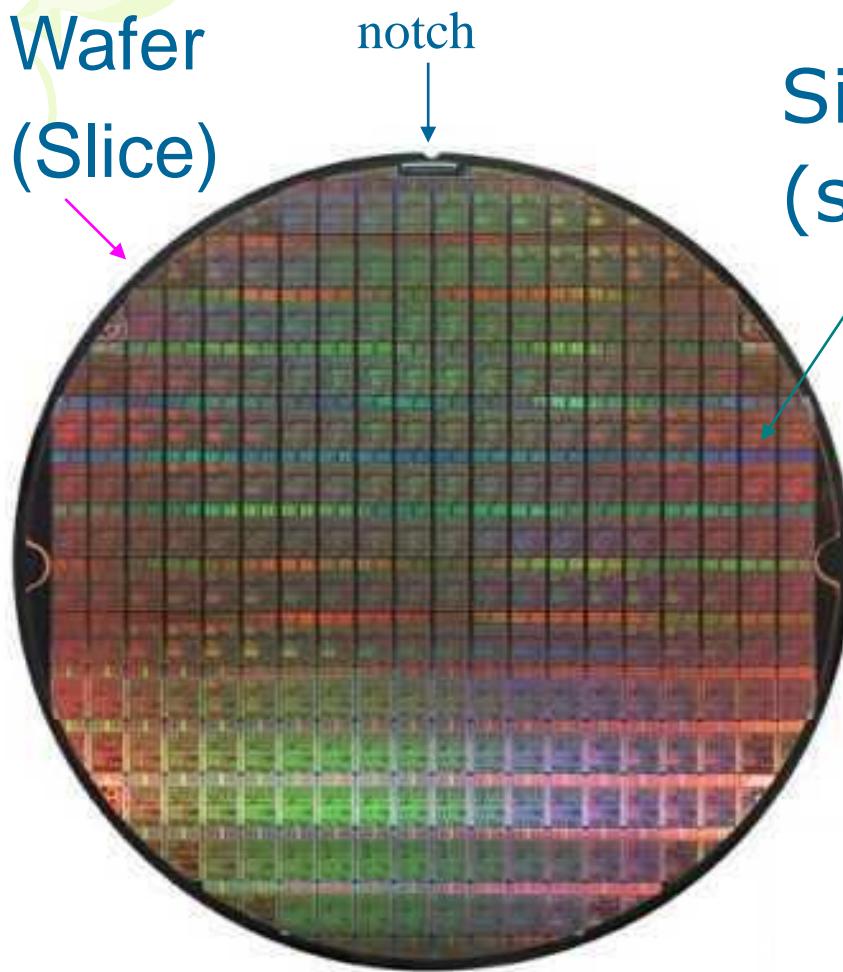
Gordon Moore: co-founder of Intel. "Density of IC devices is doubling with each new **generation**" (in 1965)

In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

- He made a prediction that semiconductor technology will double its effectiveness every 18 months

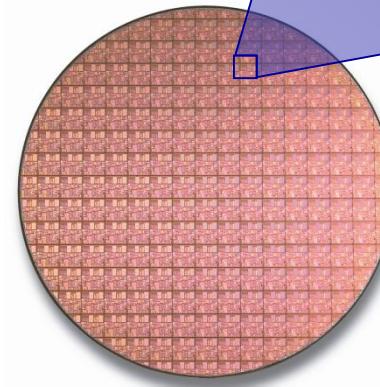
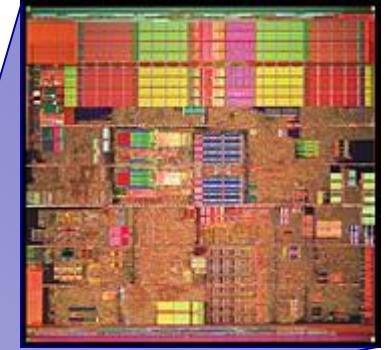
Wafer and Die

Wafer
(Slice)



Single die
(single chip)

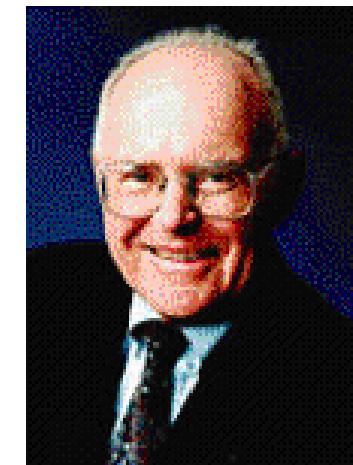
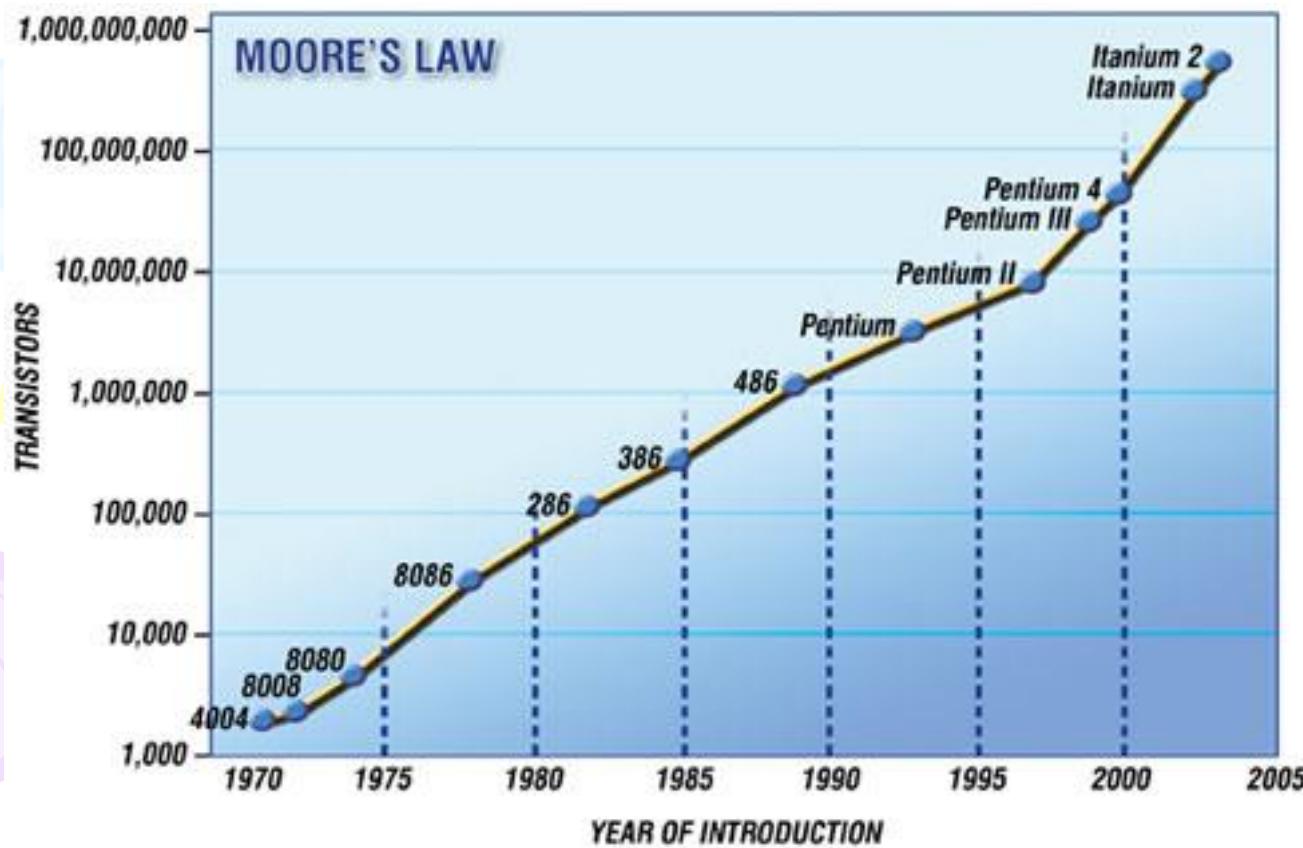
Intel Pentium®4 Processor



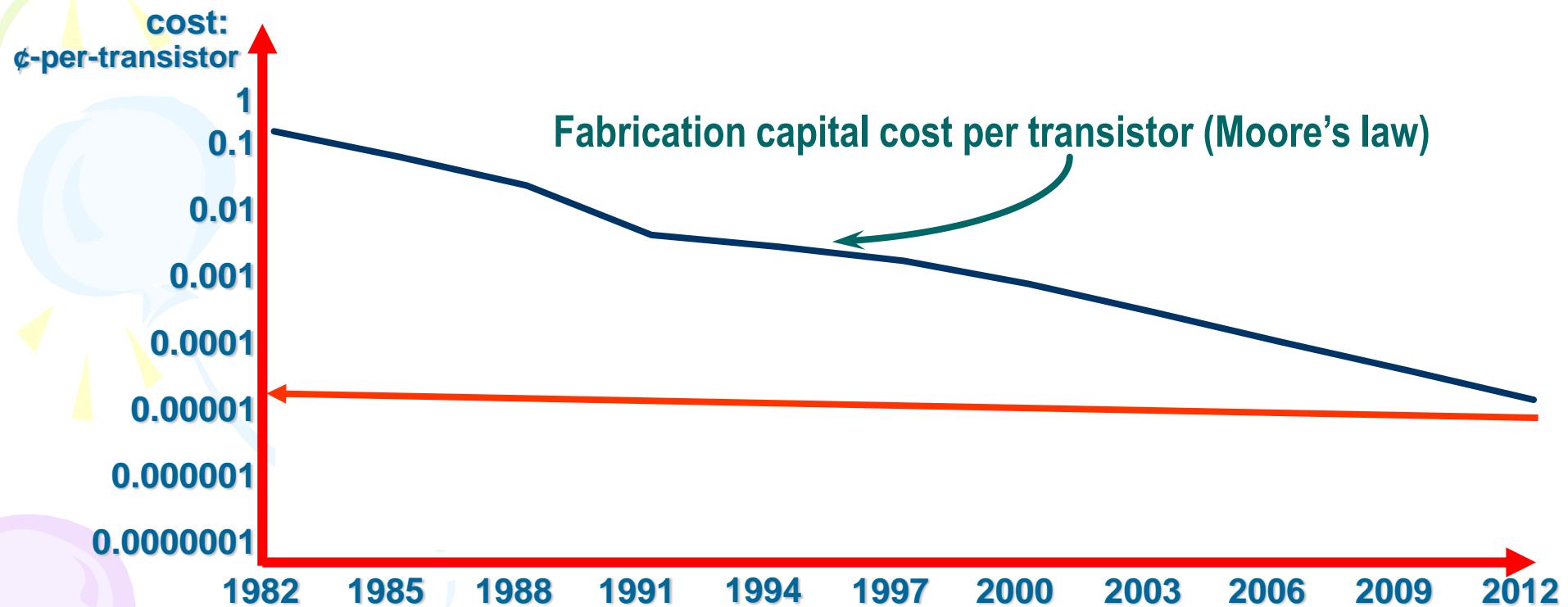
300mm Si wafer

Why the success: Moore's law

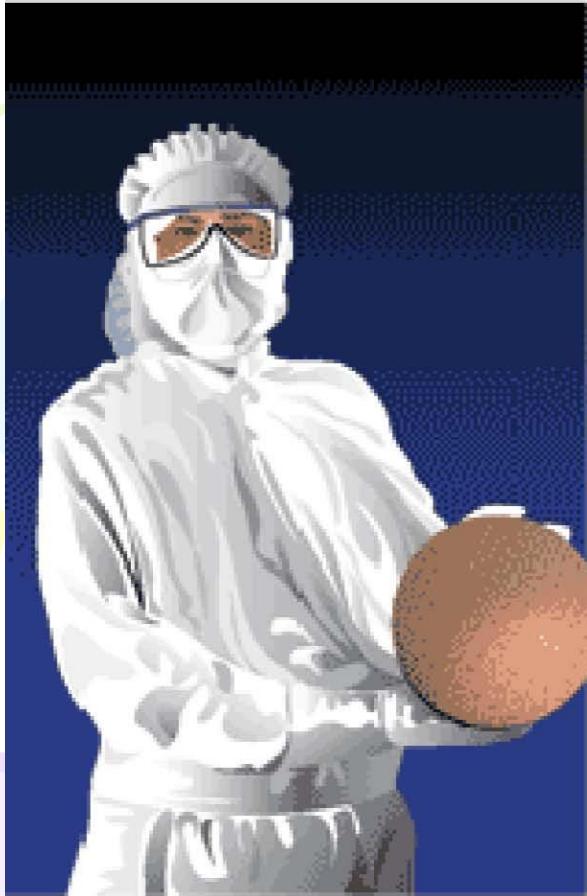
- **Moore's Law:**
 - Components per chip
 - double every 1.5 - 2 years



Moore's law in Cost per Transistor



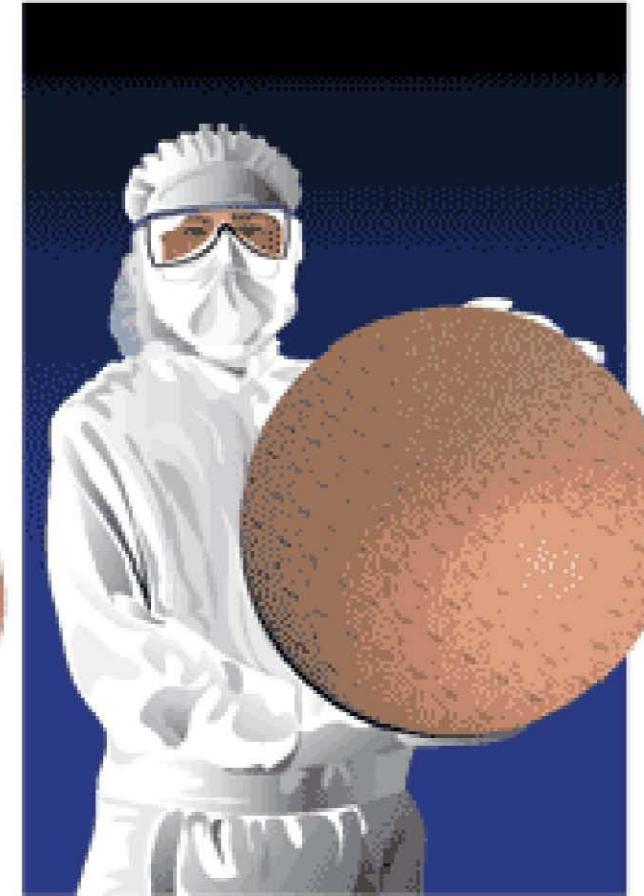
Processing is performed at die-level or wafer-level



200 mm/1990

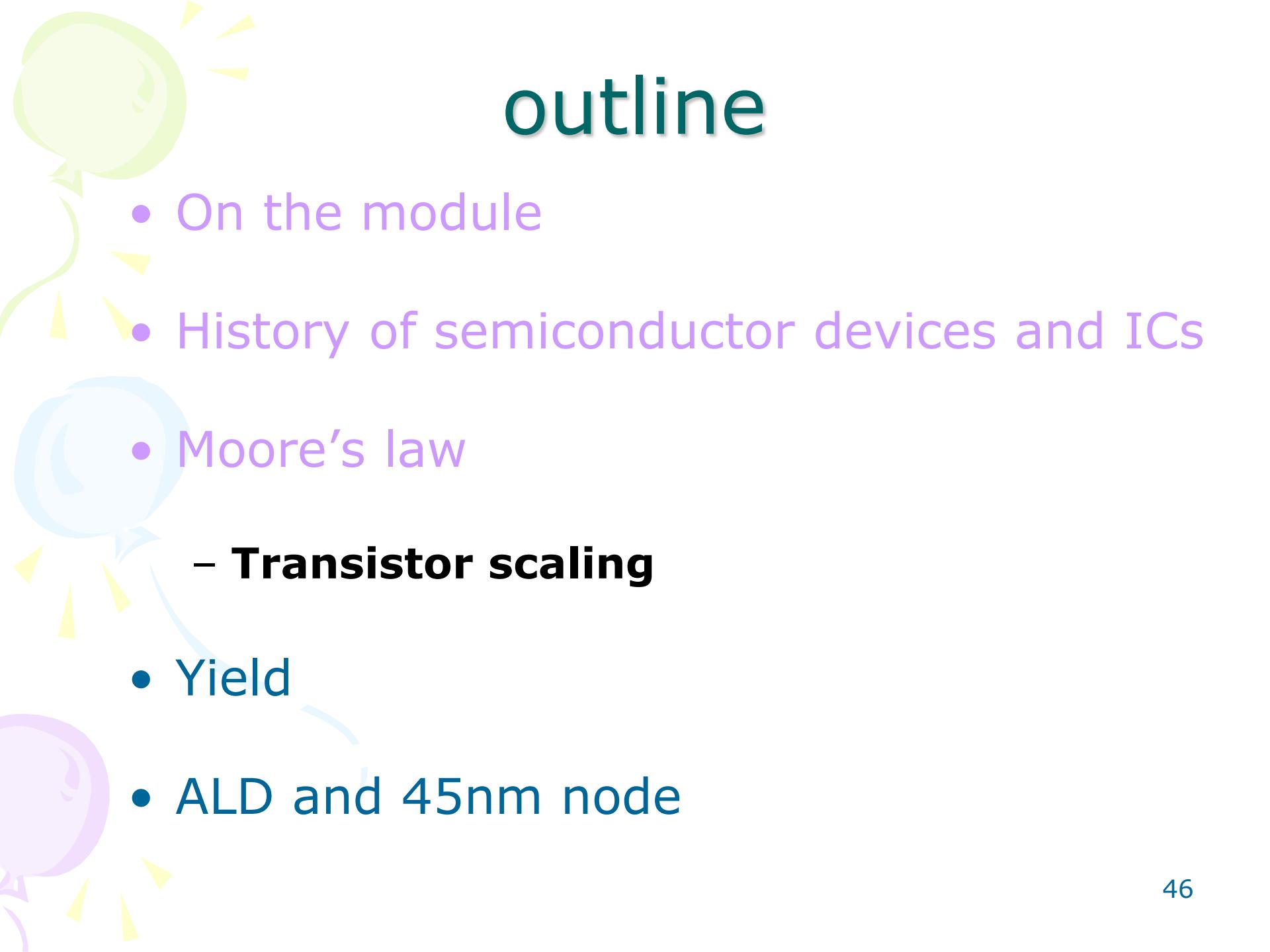


300 mm/2001



450 mm/2012?

Every 10-11 years wafer size increases. Will history repeat itself?



outline

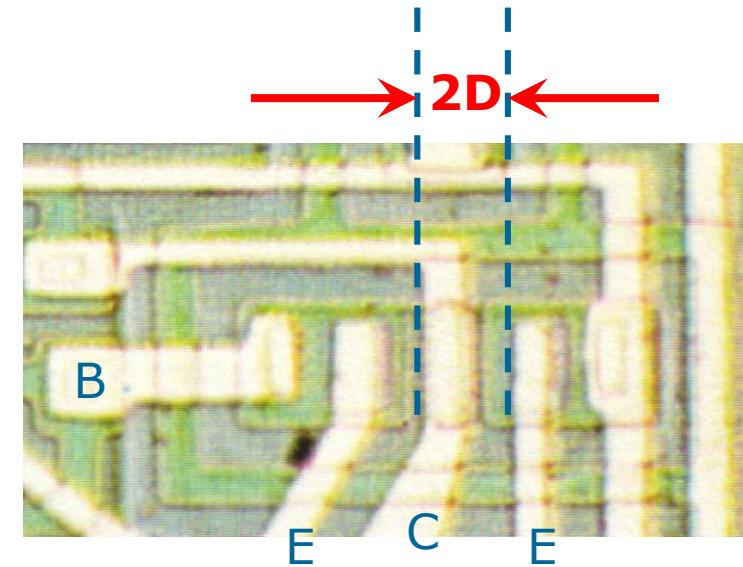
- On the module
- History of semiconductor devices and ICs
- Moore's law
 - **Transistor scaling**
- Yield
- ALD and 45nm node

Why Scaling?

- Technology shrinks by **0.7**/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x

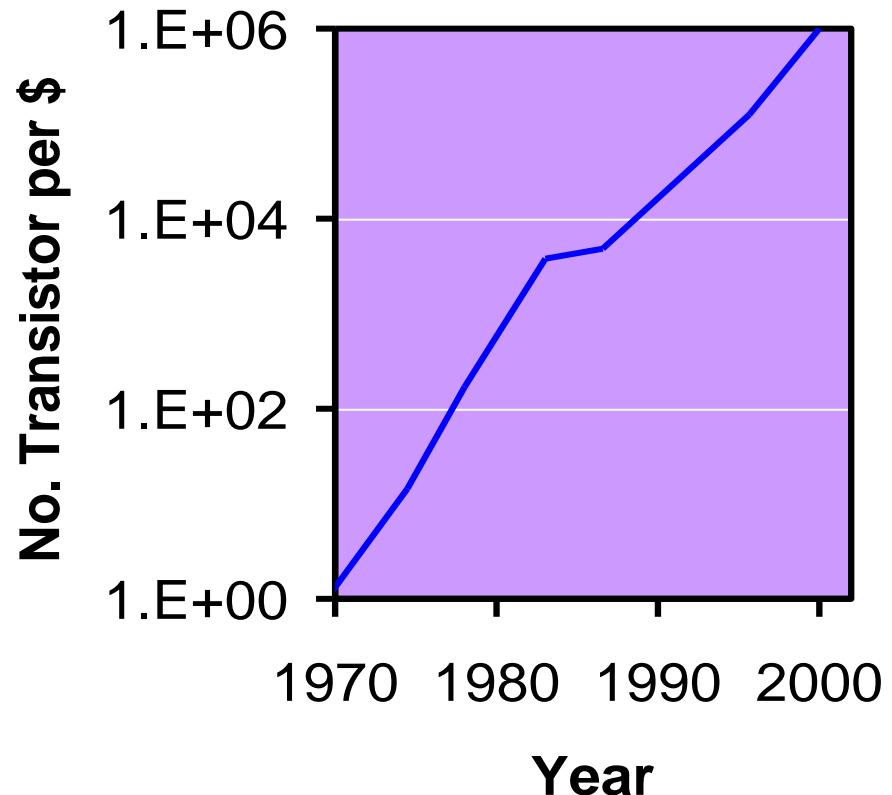


- 1) Cheaper**
- 2) Better (faster and more functional)**



Why is small beautiful?

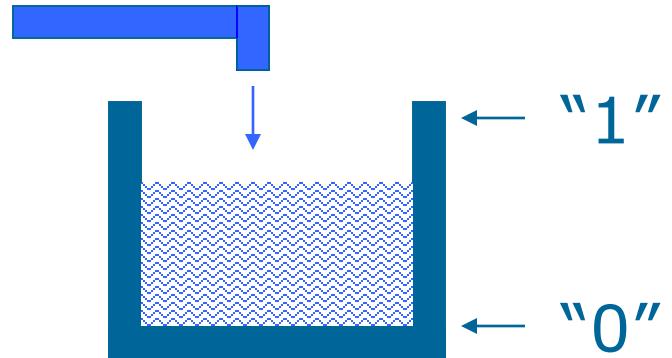
- Price reduction: A million to one
- “Nothing had ever done that for anything before”
--- J. Kilby



“If this happens in auto industry, a car can only worth less than a penny.”

Not only cheaper, but also better

- Binary: “0” and “1”
- “0”=Empty
“1”=Full
- Delay:
 - Filling the tank

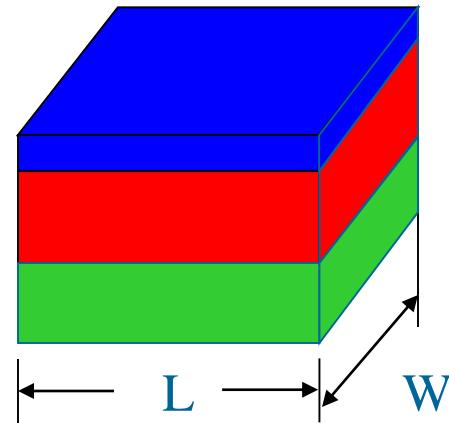


The smaller, the faster !

- Capacitors between gate and silicon
- Capacitor \Leftrightarrow Electronic tank
- Electronic charges \Leftrightarrow Water

- MOS

Metal
Oxide
Silicon



Delay
= RC

- Smaller devices \Leftrightarrow Smaller tank

Benefit of Transistor Scaling

Generation:

1.5 μ

1.0 μ

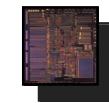
0.8 μ

0.6 μ

0.35 μ

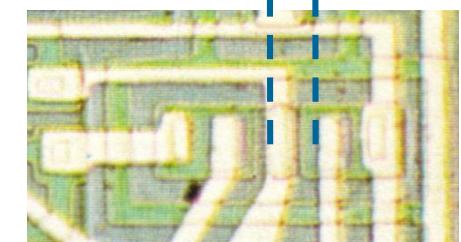
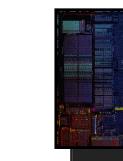
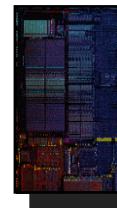
0.25 μ

Intel386™ DX
Processor

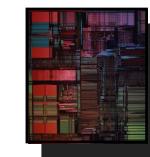
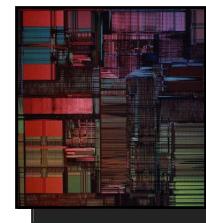


smaller chip area → lower cost

Intel486™ DX
Processor



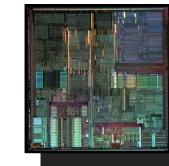
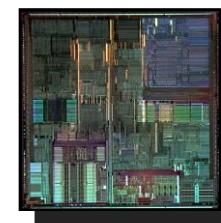
Pentium®
Processor



Pentium® II
Processor

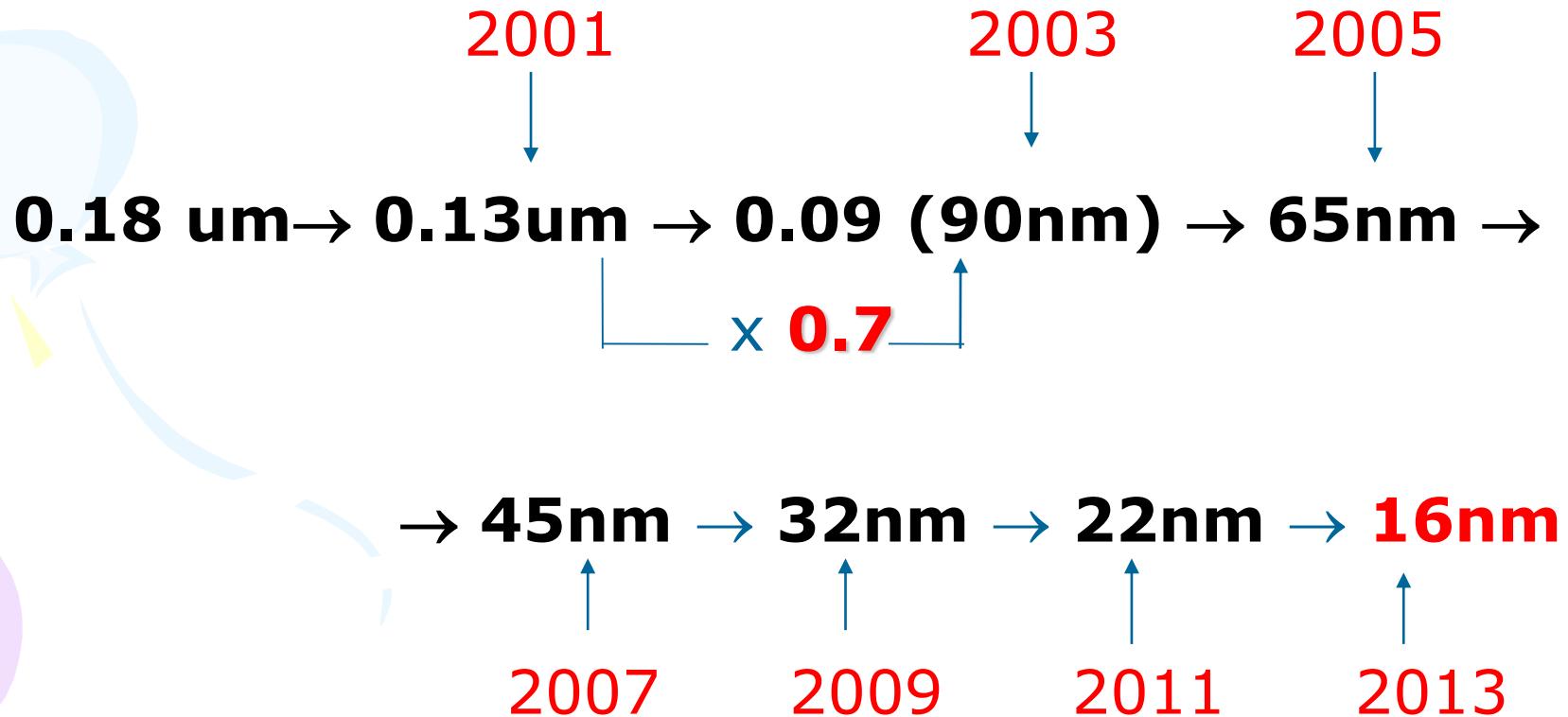


more functionality on a chip
→ better system performance



The state-of-the-art CMOS process

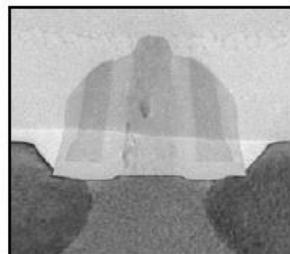
- $0.13\mu\text{m}$: 1000 trans. per hair



On-Time 2 Year Cycles

90 nm

2003



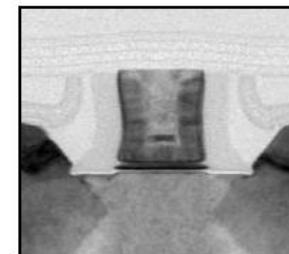
65 nm

2005



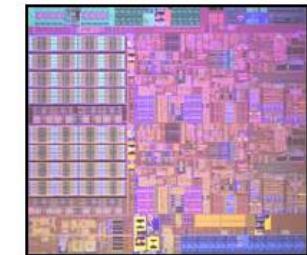
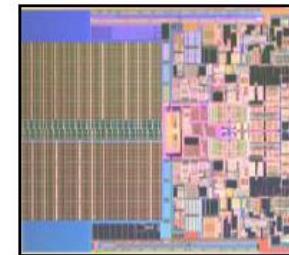
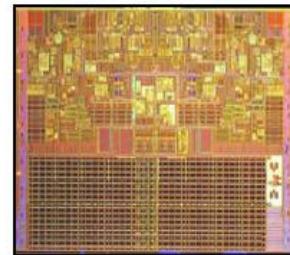
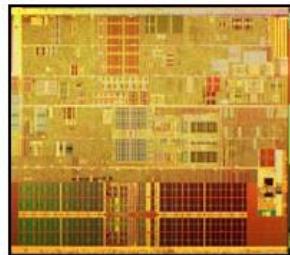
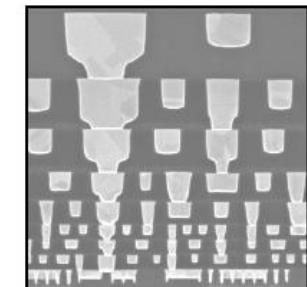
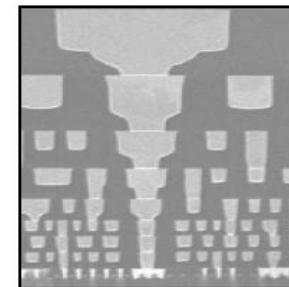
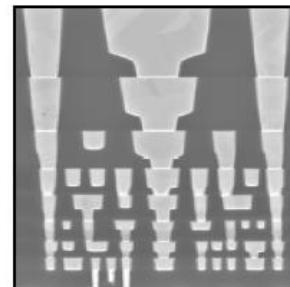
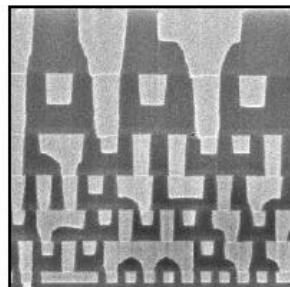
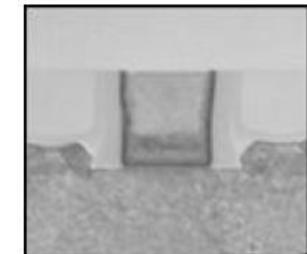
45 nm

2007

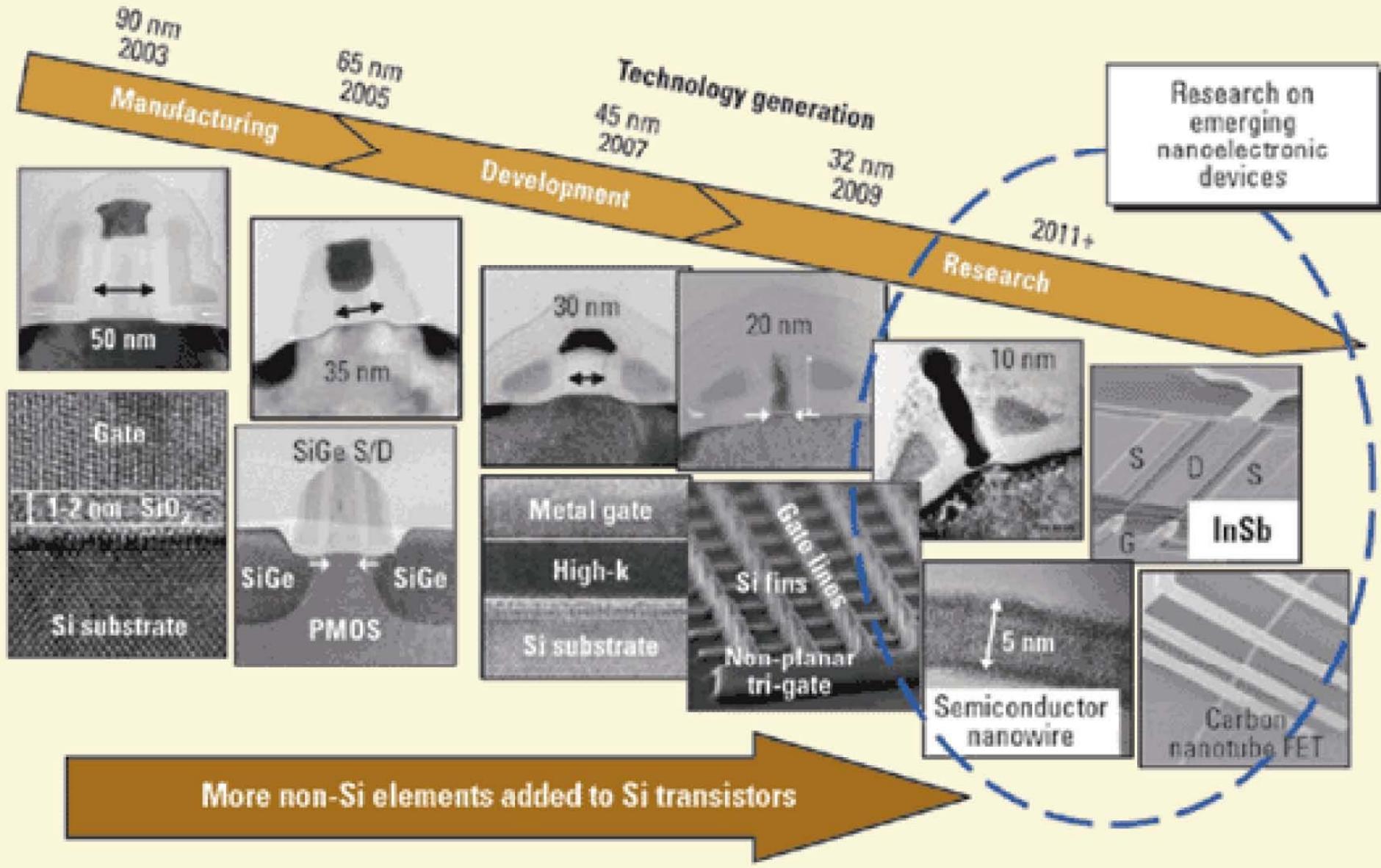


32 nm

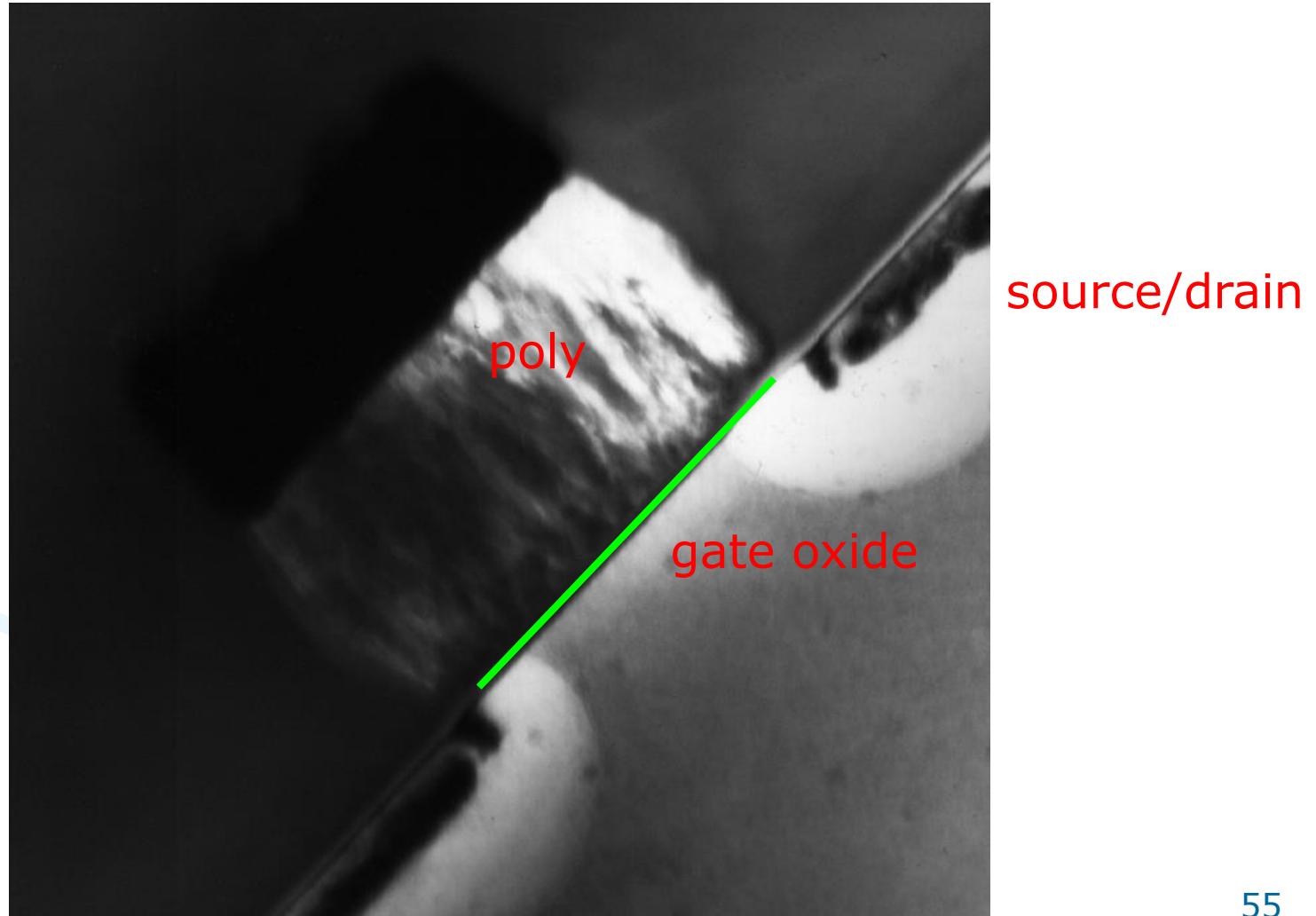
2009



NON-SILICON MATERIALS RESEARCH

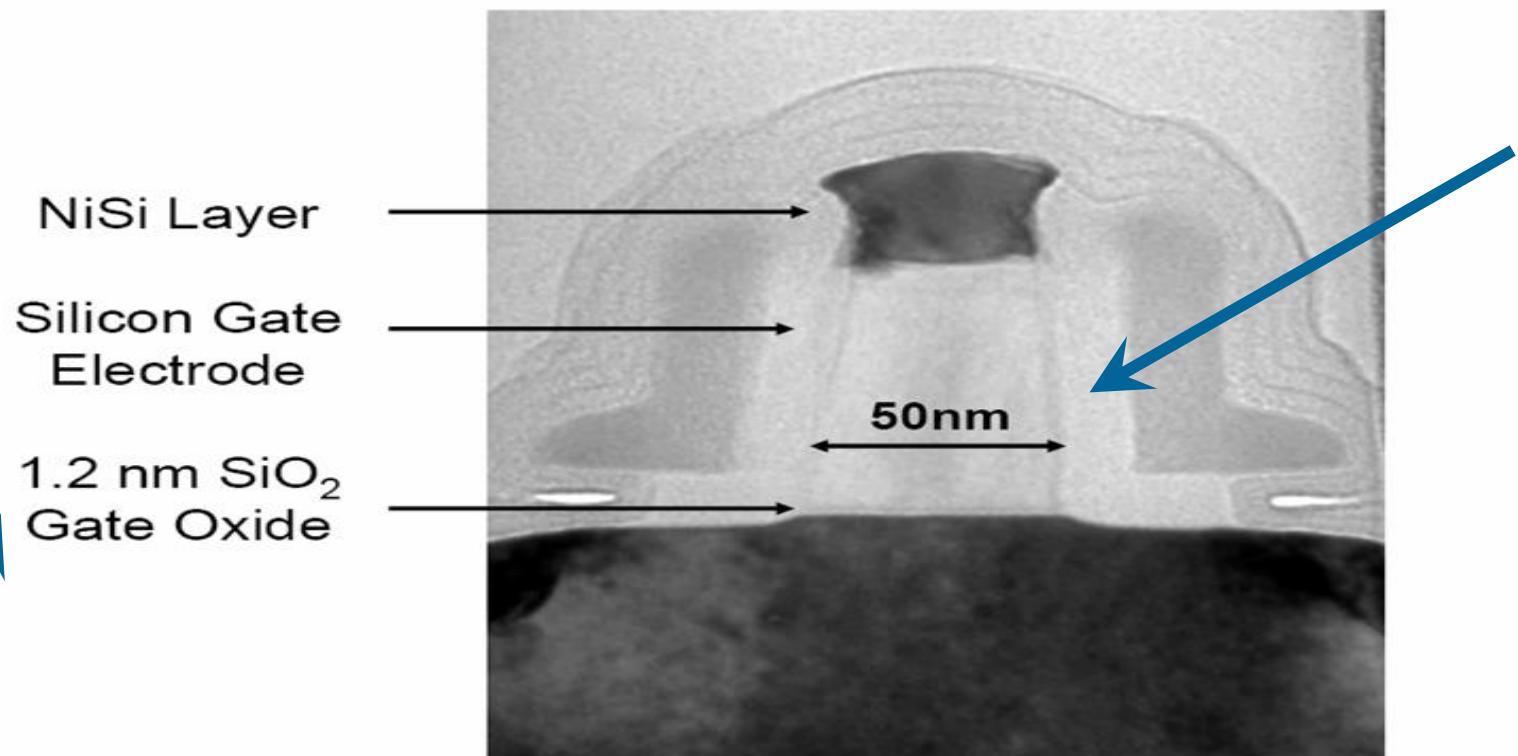


0.25 um transistor (Bell Labs)



90 nm NMOS

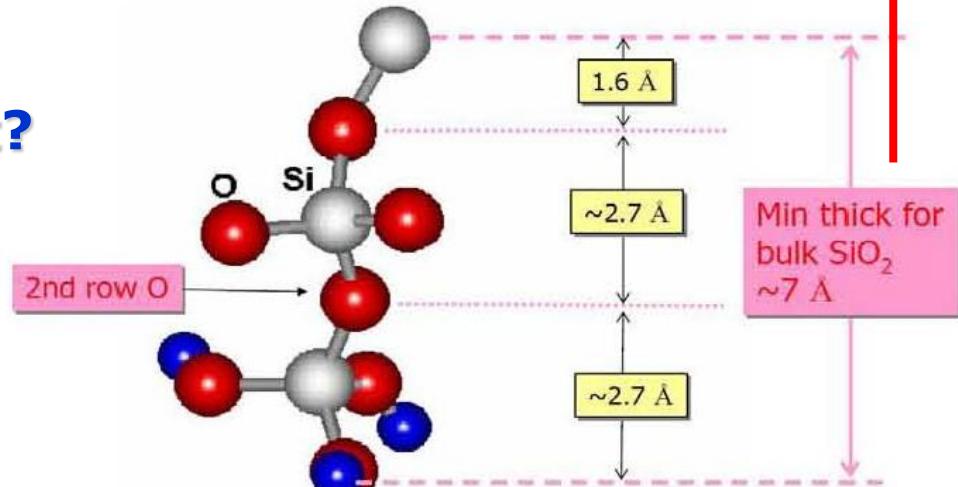
- Courtesy of Intel Corporation. Used with permission
- Picture from: <http://www.intel.com/technology/silicon/micron.htm>



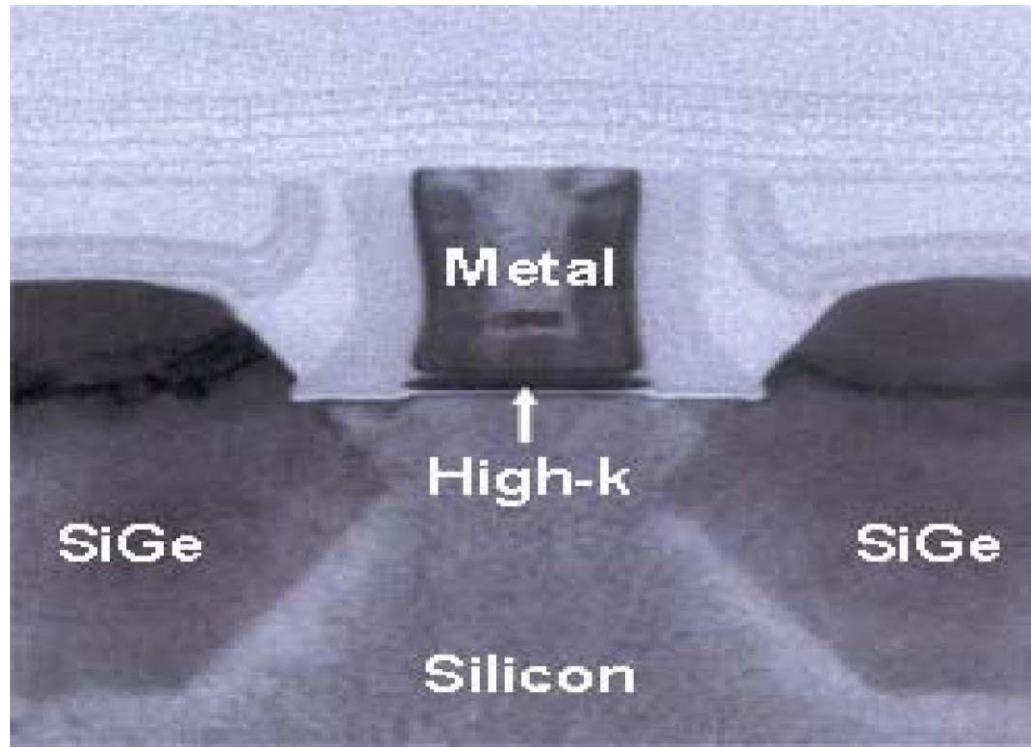
Min. thickness for bulk SiO₂

| CMOS (μm) | 0.5 | 0.18 | 0.13 | 0.1 | 0.07 | 0.05 | 0.035 | 0.025 |
|--------------------------------------|------|------|------|-----|------|------|-------|-------|
| L (nm) | 500 | 180 | 130 | 100 | 70 | 50 | 35 | 25 |
| V _{DD} (V) | 5 | 1.8 | 1.3 | 1 | 0.7 | 0.5 | 0.35 | 0.25 |
| T _{ox} (nm) | 10 | 3.5 | 2.2 | 1.5 | 1.0 | 0.7 | 0.5 | 0.35 |
| X _j (nm) | 120 | 50 | 40 | 33 | 22 | 15 | 11 | 8 |
| N, 10 ¹⁸ /cm ³ | 0.14 | 0.49 | 0.85 | 1.3 | 1.75 | 2.4 | 3.3 | 5.0 |

What can we do on this limit?



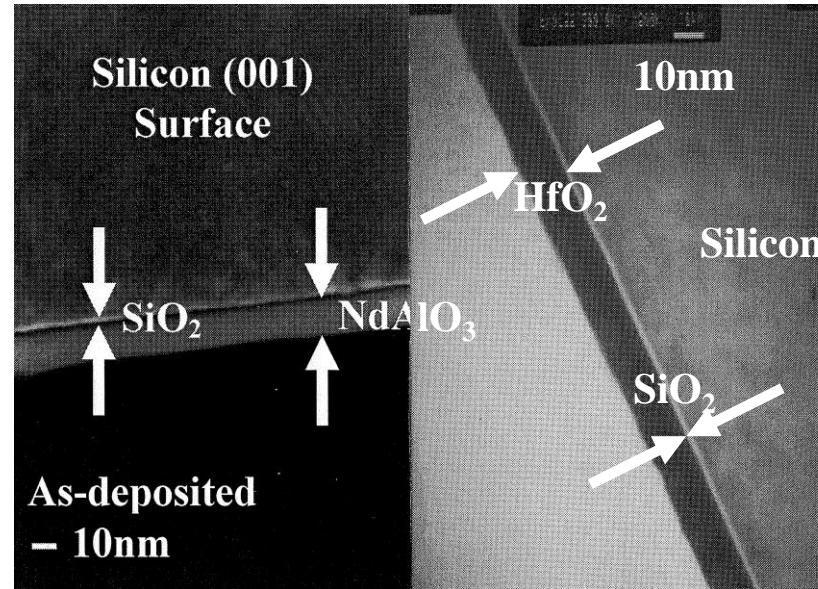
45 nm transistor with high-k metal



- Intel 45nm Hi-k metal gate silicon technology: One of the "Best inventions of the year."
- *TIME* Magazine, 2007

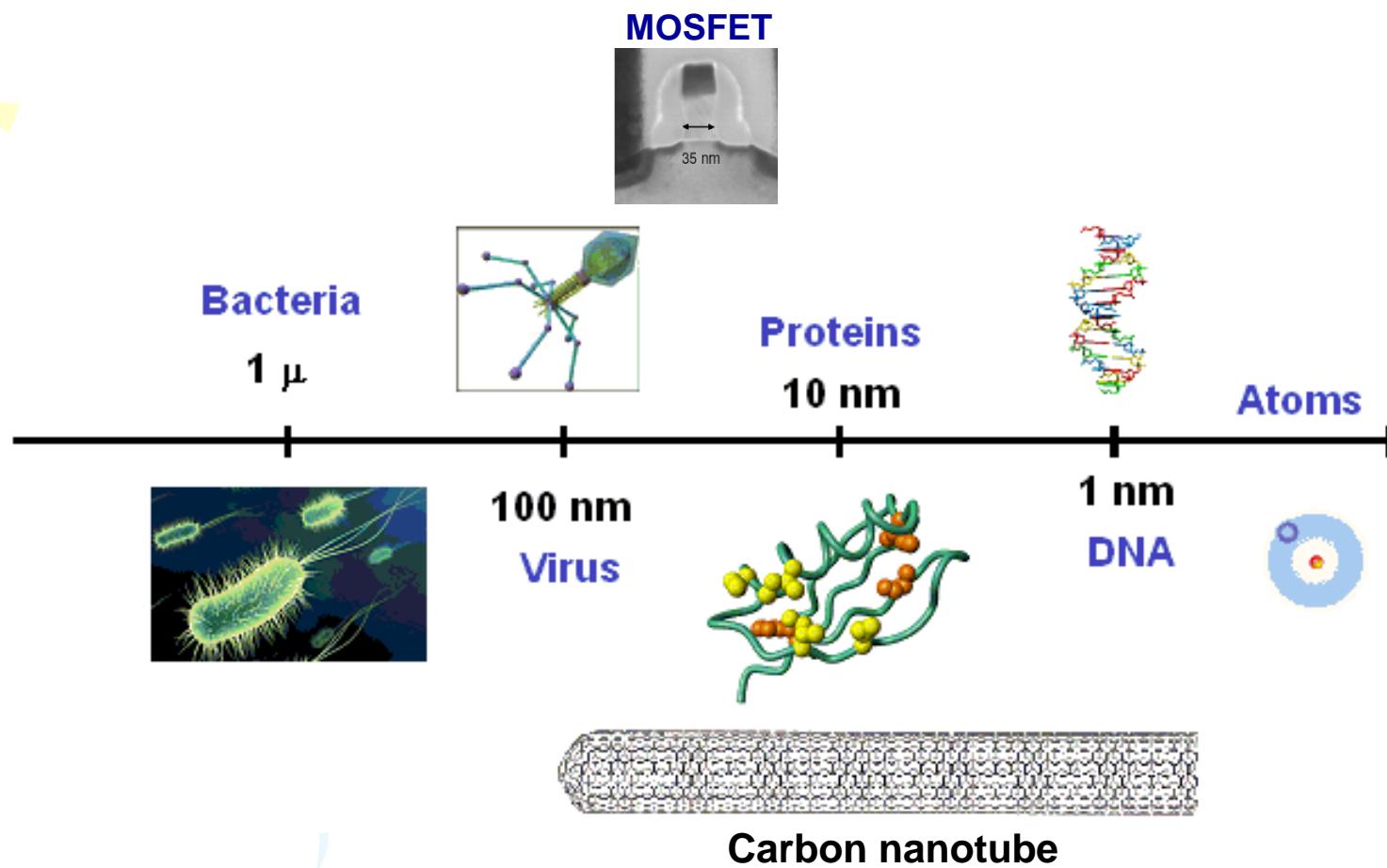
High-k dielectrics in Liverpool

- My TEM pictures (in 2008)



- Equipment I used: ALD (see the video)

The Nanometer Size Scale

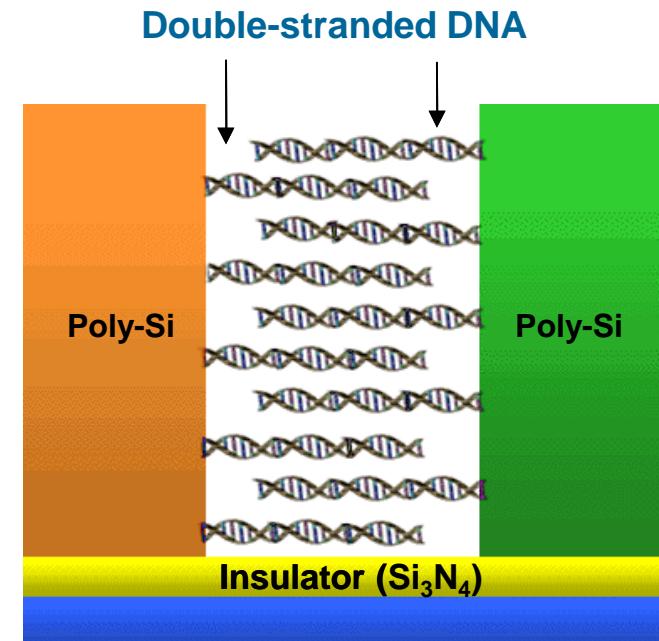
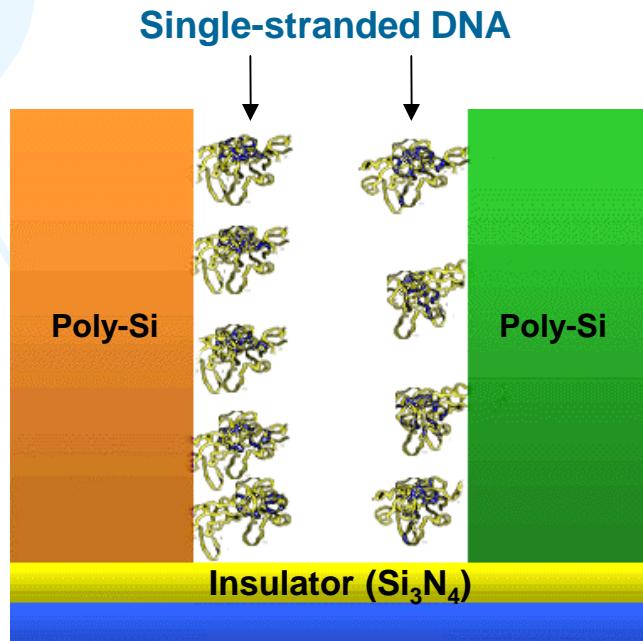
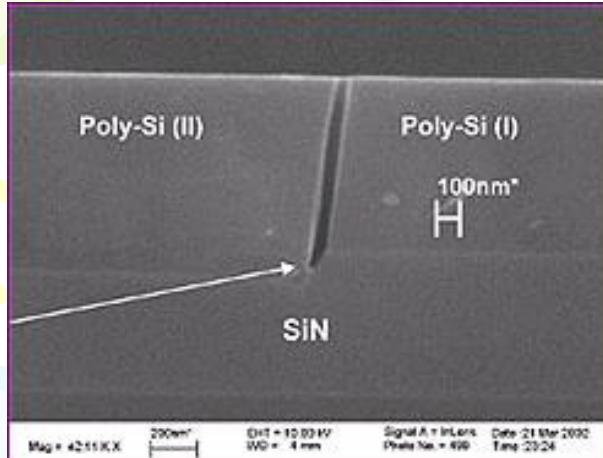




“More than Moore”

- Find the meaning from the internet yourself and tell the lecturer what is the future of IC.

Nanogap DNA Detector



Prof. Luke Lee, BioEngineering Dept.
<http://www-biopoems.berkeley.edu/>



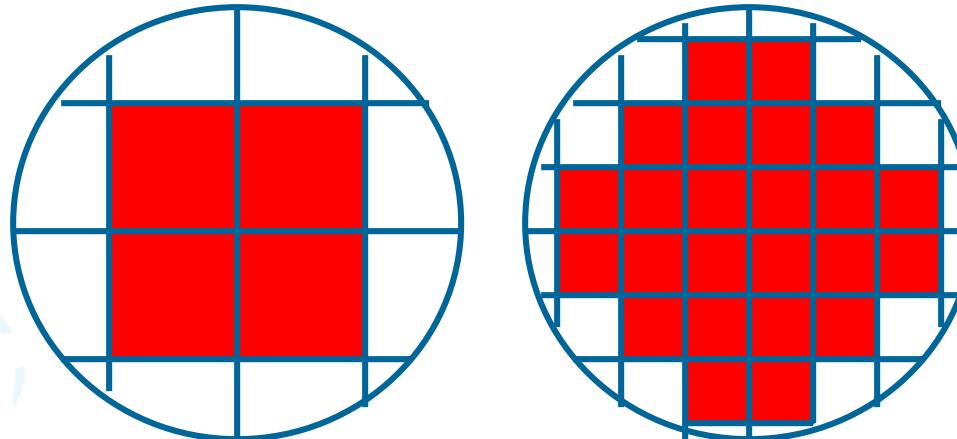
outline

- On the module
- History of semiconductor devices and IC
- Moore's law
 - Transistor scaling
- **Yield**
- ALD and 45nm node

Yield

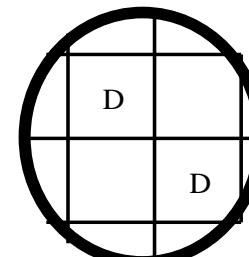
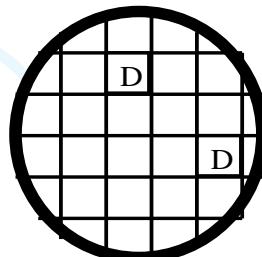
Die yield = $\frac{\text{No. of good chips per wafer}}{\text{Total number of chips per wafer}} \times 100\%$

Die cost = $\frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}}$



Example

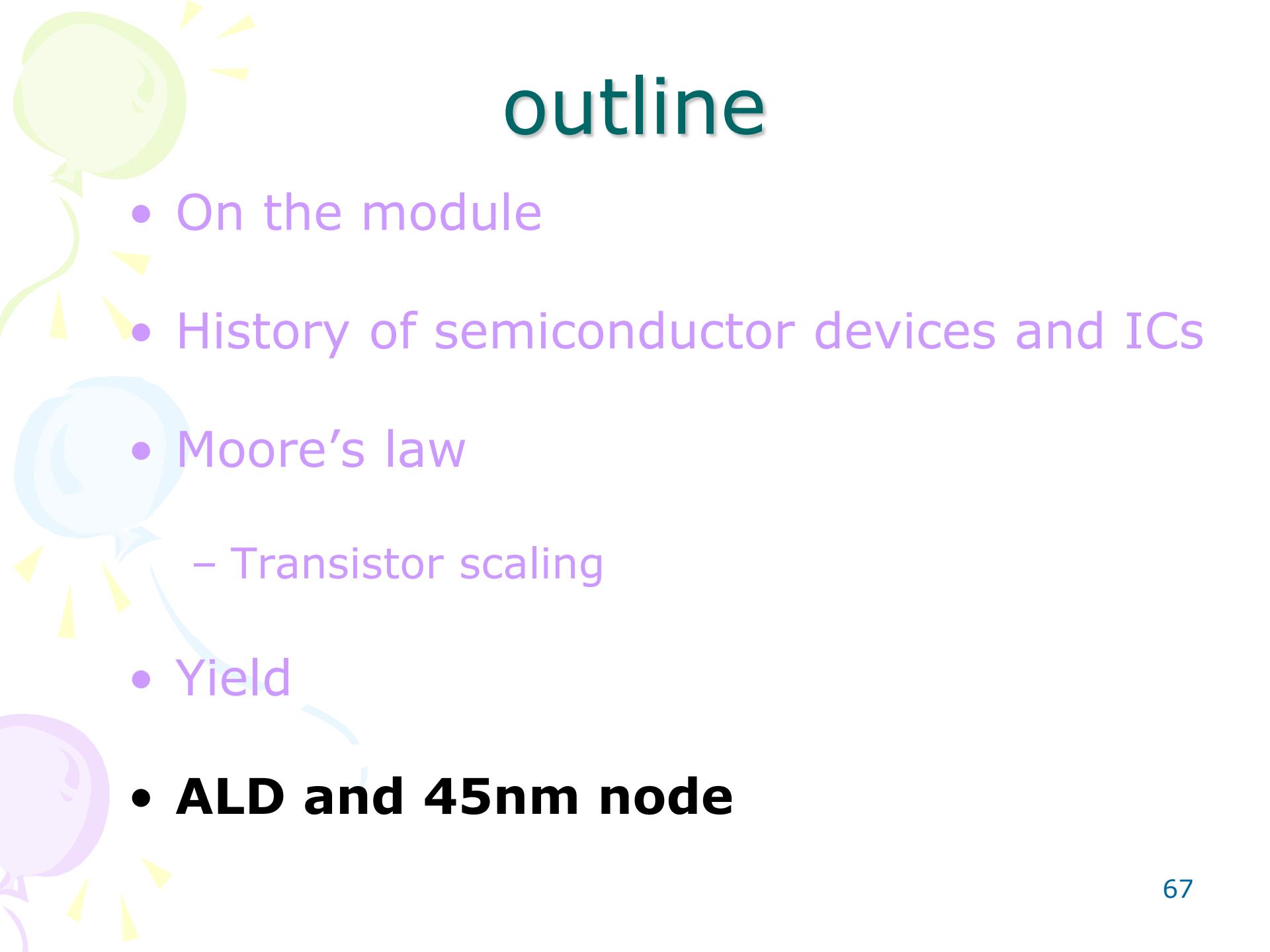
- Each '**chip**' consists of a large number transistors interconnected to make a circuit. Some of the silicon chips will contain defects such as those marked with D.
- Of 16 circuits in the example, 14 are working, so the **yield** is 87%. So if this slice were to cost £500 to make, the net cost of each chip would be $500/14=\text{£}36$.
- But much depends on how small each transistor is, and there is a relationship between this size and the size of the chip.
- Only two chips are working so that the **yield** is 50% and the cost would be £250.
- The smallest dimension that can be produced is called the minimum feature size(λ). It has changed from $10\mu\text{m}$ to $0.3\mu\text{m}$ in 25 years a factor of 35. The above example, which corresponds to a minimum feature size reduction of two leads to a reduction of cost from £250 to £36.



The largest silicon wafer

- Not only small chips, but also large wafers
- 12 inch --- 300mm
- With 90nm CMOS: 120b per wafer

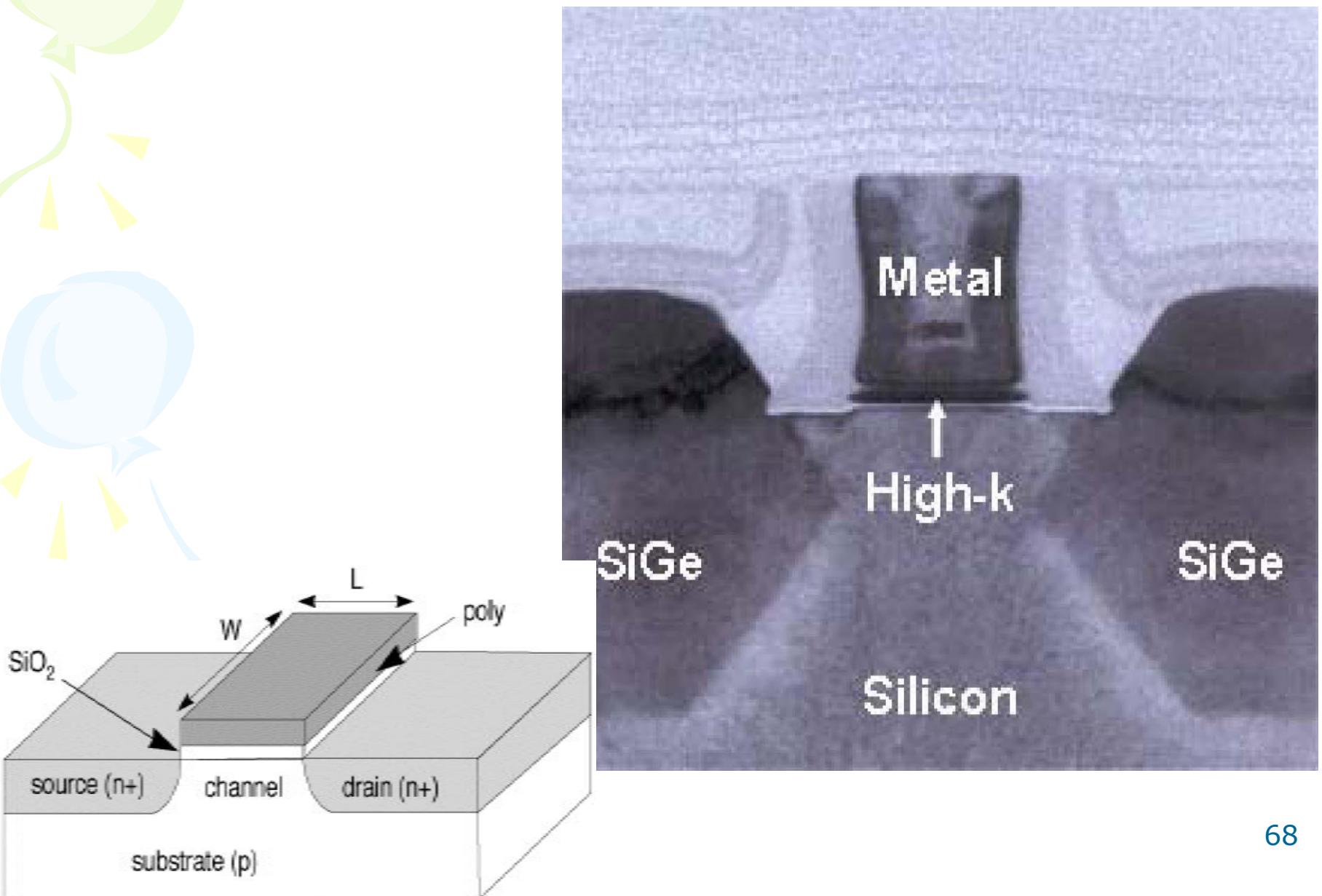




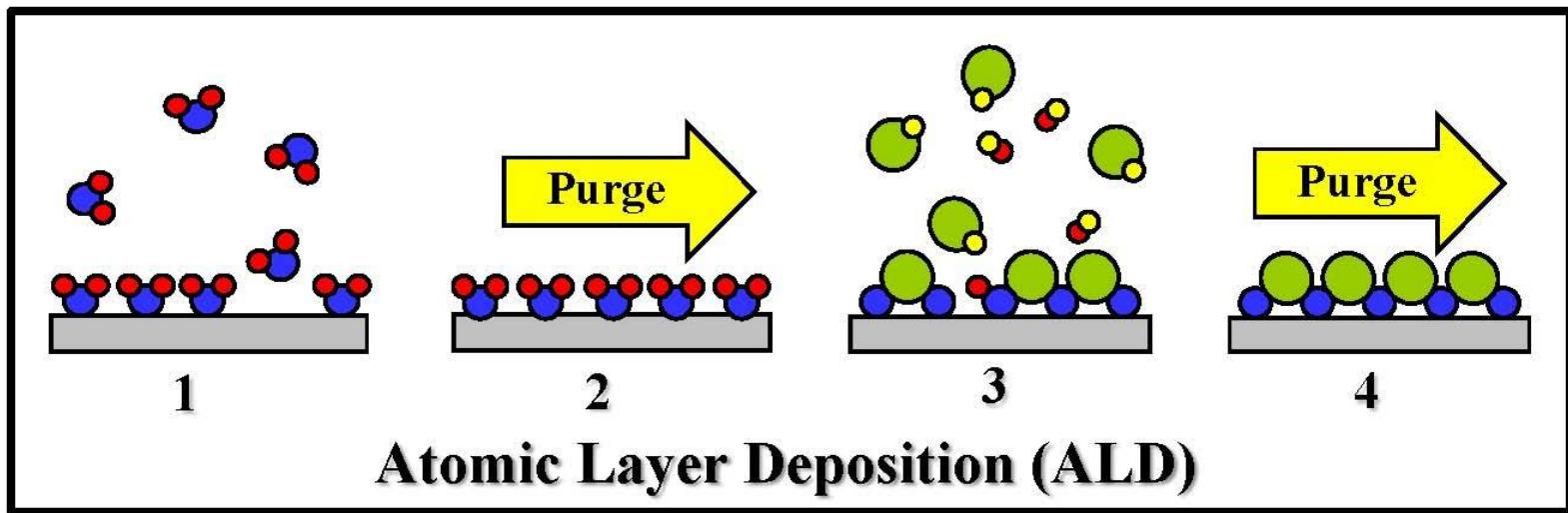
outline

- On the module
- History of semiconductor devices and ICs
- Moore's law
 - Transistor scaling
- Yield
- **ALD and 45nm node**

45 nm transistor with high-k metal

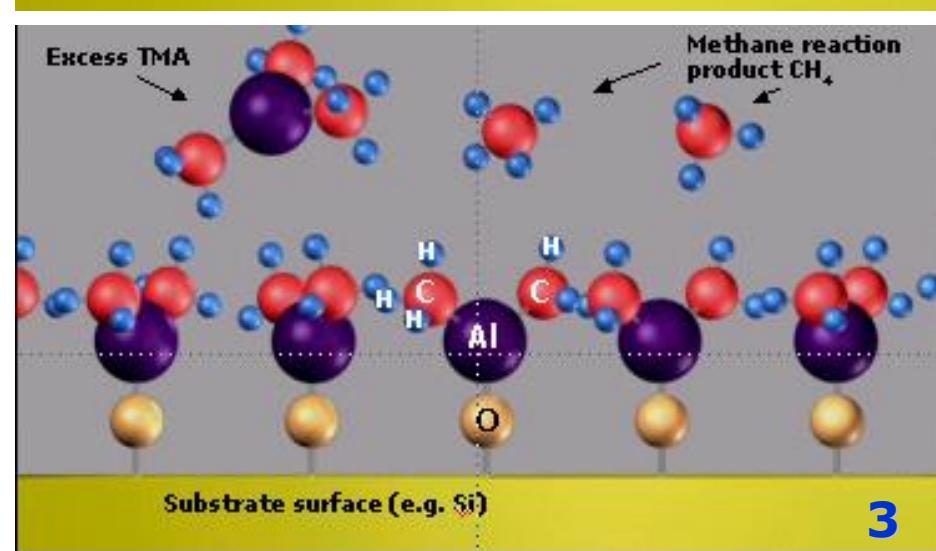
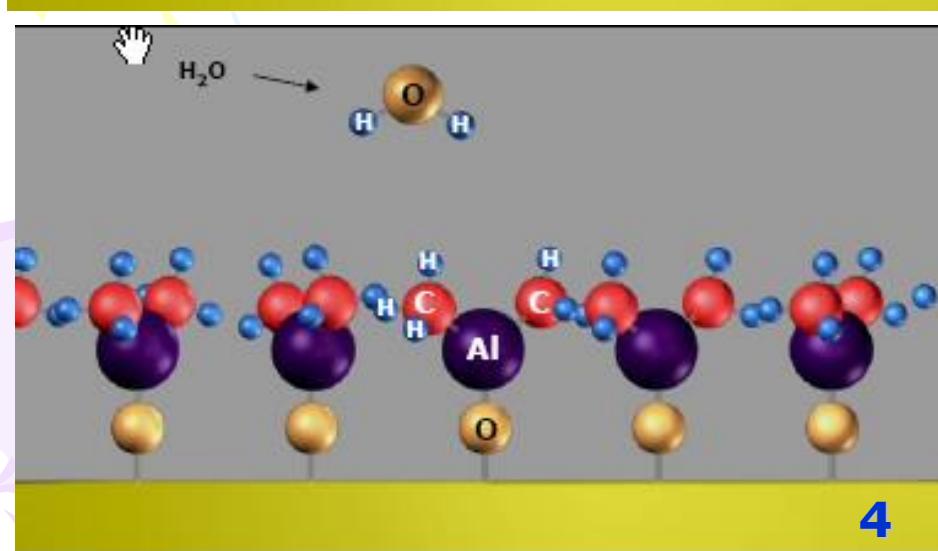
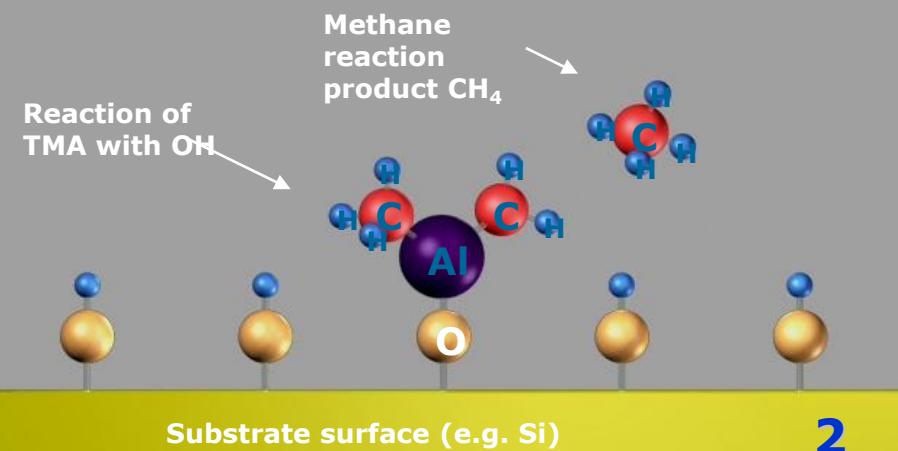
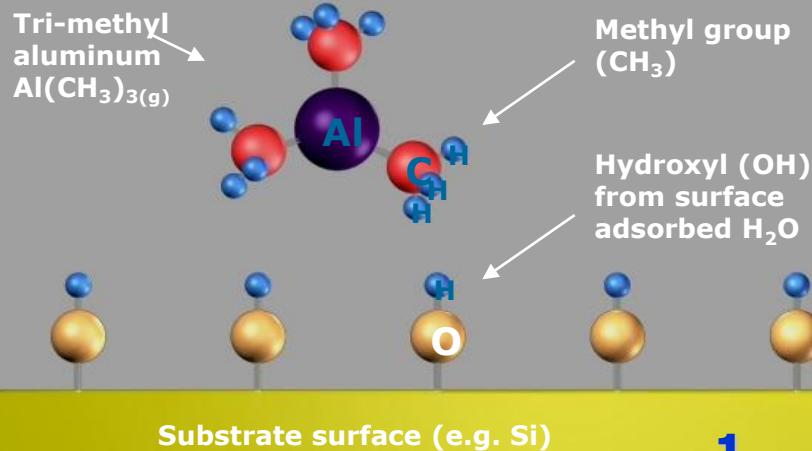


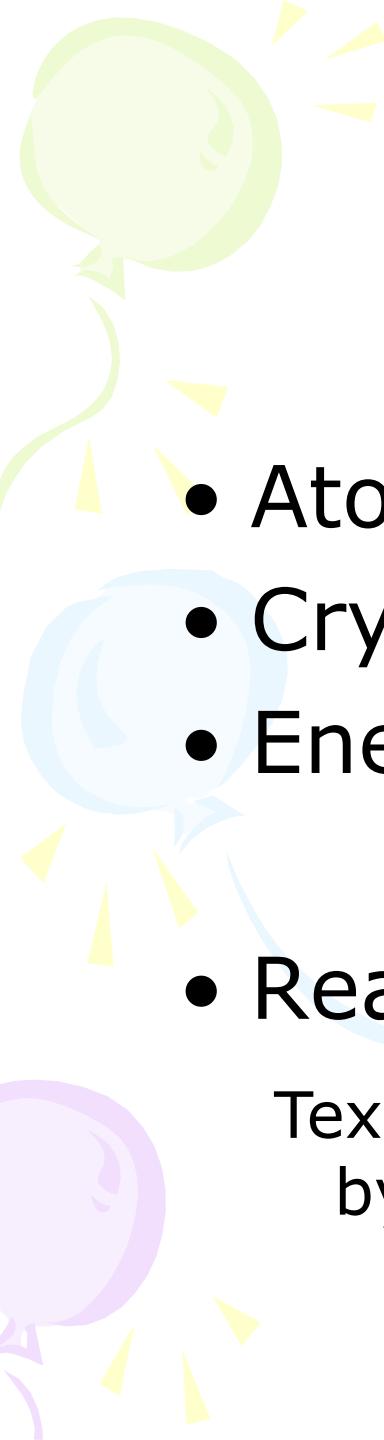
What is ALD?



ALD Video

• <http://www.cambridgenanotech.com/>





Next Lecture

- Atomic Structures
- Crystal structure
- Energy Bands
- Read: Chapter 1 – 2.1, 2.2 & 2.3

Textbook (An Introduction to Microelectronics,
by Cezhou ZHAO, Zhou FANG and Qifeng LU