

BACKSIDE DEFECT MONITORING STRATEGY AND IMPROVEMENT IN THE ADVANCED SEMICONDUCTOR MANUFACTURING

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ABSTRACT

Traditionally, control the defect on the front of wafer can improve equal yield because all chips located wafer's upper part. That's why wafer manufacturing engineers always focus on front side and bevel of wafer. However, with the rapid development of semiconductor technology, slight variation of backside condition may induce yield loss. Against this backdrop, monitoring the backside of wafer will be extremely important. Monitoring method include visual inspection (VI), macroscopic inspection (MAI), microscopically inspection (MII) and hyper fine inspection (HFI). All the above methods cross banded by different process characteristic build a multi-stage monitor system. There are a lot of challenges in backside inspection result from scanning algorithm. Monitor arrangement scientifically was elaborated in this paper. Meanwhile, graphic recognition system was introduced which can quantify the backside scan image and distinguish exceptions. Finally, the scan result can check and clear a fault after compare with the Backside Database (BDB). Certainly, use ingenious printing to collect the BDB was also discussed in this content.

Key words: backside scan; monitor network; graphic recognition

INTRODUCTION

Considerable resource is devoted to purchase lots of pieces of measurement and inspection equipment in today's semiconductor manufacturing industry. Most of inspection tools focus on wafer's front side, however, the extremely tight control of SPC and small tolerance of defects even the defects in wafer backside could cause the failure of front side chips while technologies entered nanometer node [1,2]. As fig.1 shows, only less than one percent of total capital is used for backside inspection.

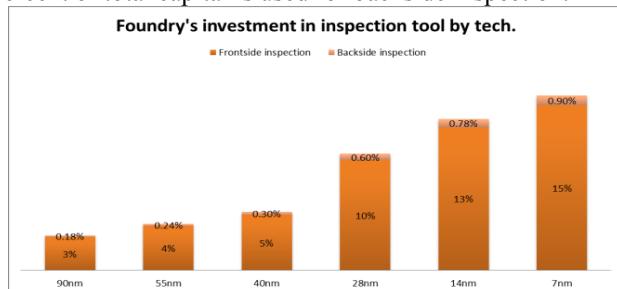


Fig.1 foundry's investment ratio in inspection tool by technology node

There are many different methods of defecting backside. The main detecting techniques were listed as below:

Detect method	Accuracy
Visual inspection	>10mm
Macroscopic inspection	3000um
Microcosmic inspection	20um
Hyper fine inspection	2um

Fig.2 shows images taken under different detection methods.

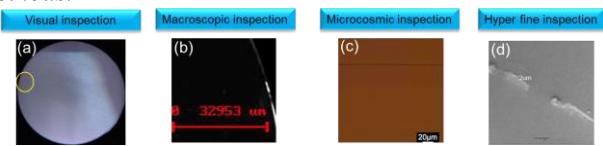


Fig.2. Images taken under different detection methods: (a) manual inspection; (b) Macroscopic inspection; (c) Microcosmic inspection;(d) Hyper fine inspection

Current primary testing and characterizing method of backside is defect count, more straightforward, visual inspection instead.

Nevertheless, taking defect count as the backside condition index not fit any more in the following situation.

① Mass Noise Interference

In the wafer manufacturing process, with the procedure increasing, the tool's parts such as aligner, e-chuck have more touching with the wafer's backside. Under the circumstances, the map scanned by inspection too worse to tell the deference between baseline and excursion.

As the Fig.3 shows, (a) and (b) is the same wafer scanned at different process stage. Scratch is obviously observed at stage A. Through a series of manufacturing steps, wafer with the scratch was inspected again; Fig(a) shows that the scratch cannot be highlighted easily for worse background noise.

For the same reason, only take defect count trend chart as backside condition index is not credible at BEOL.

Fig.4 shows that the same scratch's position at different stage trend chart. Stage A have a stronger signal than B.

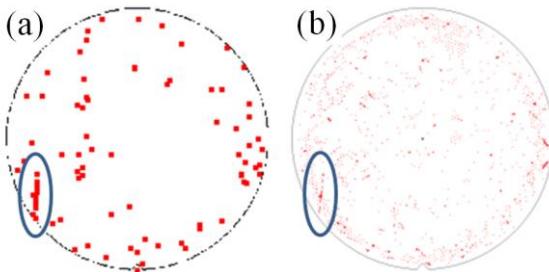


Fig. 3 The same wafer scanned at different stage; (a) scanned at FEOL, (b) scanned at BEOL

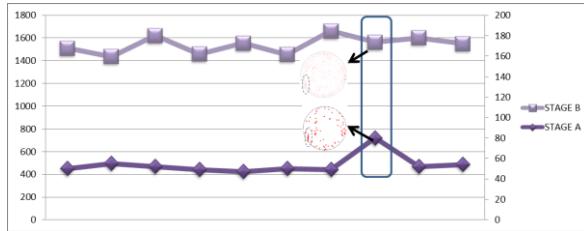


Fig. 4 the same scratch's signal position at different stage trend chart.

② Large Discolor

Fig.5 shows that Die to Die compare is used for front side where has information of reticle and Die. Backside inspection scanning principle is similar with front side. There is no pattern at backside, so the scan arithmetic cut bare wafer into fixed Pixel Blocks (PB). Fig.6 shows PB to PB compare and subtract is the backside inspection principal theory.



Fig. 5 The scan principle of wafer's frontside

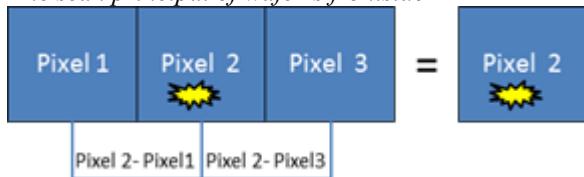


Fig. 6 The scan principle of wafer's backside

Like front side inspection, we're going to have the same problem. Once a large area discolors which across two or more PBs, Use the algorithm introduced above cannot work anymore.

1	1	1	1	1
1	2	2	2	1
1	1	2	1	1
1	1	1	1	1

Fig. 7 large area discolor schematic diagram of PB

As Fig 7 shows, PB1 represent good area, oppositely, PB2 represent defect area. Black PB2 which was surrounded by PB1 was incorrectly marked good area.

From Fig.8 (b) is an obviously ring map image which filled by white slash symbol. But the map Fig.8 (a) exhibits didn't reflect the defect (large area discolors) cause the area where filled black slash symbol is blank.

So, in this case, defect count cannot characterize the backside's worse condition.

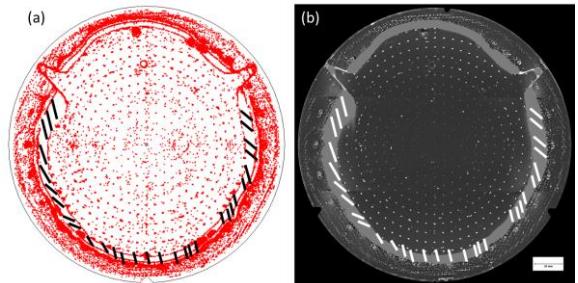


Fig. 8(a) defect map with large discolor; (b) defect image of large discolor.

Here is another challenge. The same scratch defect scanned by different accuracy may lead to different effects. We must introduce DC/TC (Defect Count/Total Count) which can characterize the capture rate of inline backside monitor. Fig.9 shows high accuracy is no longer applicable because DC/TC value is shape drop when the process runs to poly loop.

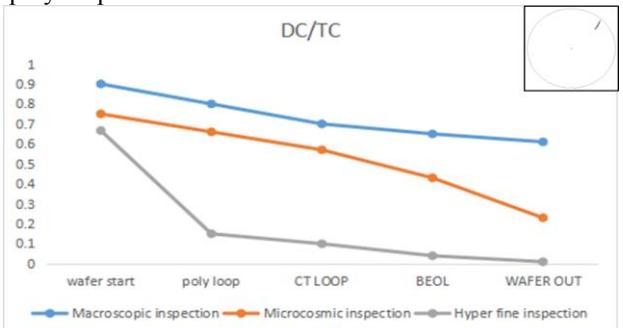


Fig.9 DC/TC under different accuracy and different process stage

As shown in the fig.10, it's readily comprehensible that the more accuracy tool is the higher defect count can be scanned for the same defect type.

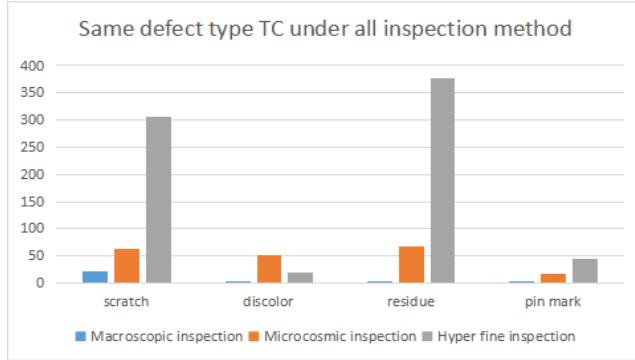


Fig.10 total defect count of the same defect type under all inspection tools

According to the above research, the multi-stage architecture backside Monitoring system is forming.

Detect method	Application
Visual inspection	Pre shipment inspection
Macroscopic inspection	Wafer start and inline Macro scratch monitor
Microcosmic inspection	Routine process monitor
Hyper fine inspection	Research and development

EXPERIMENT

Self-aligned photoresist process has a strict requirement on wafer's uniformity. It also directly affects the quality of the product.

In advanced technology nodes such as 2X nm, semiconductor device manufacturers have become increasingly aware that defects located on the backside can have a significant impact on yield, rework rates, and scrap rate, as illustrated in Fig.11 [3],

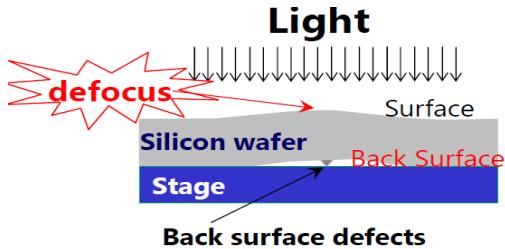


Fig. 11 A wafer backside defect causing defocus issue
Leveling hot spot depend on sharpness but the measure area of defect.

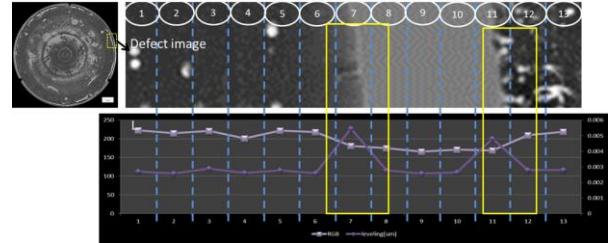


Fig. 12 leveling value &RGB curve cross to backside defect image

Benefit from Self-compensation mechanism, only P7&P11 have worse leveling issue, although P7~11 are all defect area as RGB curve shows.

This paper describes wafer's front side defocus caused by dirty backside. There is obvious special yield loss map which can match with backside image. We design some experiments to reduce this kind of defect.

Traditionally scrubbers with DIW brush have been the tool of choice for cleaning the backside of wafers [4].

In this study, a single wafer clean (SWC) platform was used for evaluation. Tests were carried out on 28nm patterned wafers.

As exhibited in fig.16, backside particle remove ratio nearly 50% with Nano-spray combine brush method.

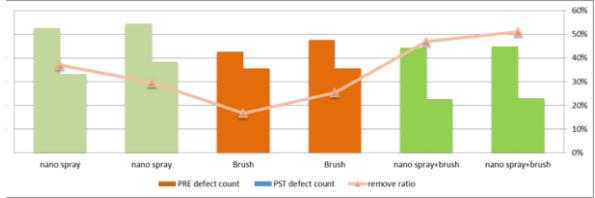


Fig. 13 Remove ratio under: 1) only brush; 2) only Nano-spray; 3) Nano-spray combined brush.

Below is high risk process which need add scrubber.

- 1) Before Litho process: Uniformity is requested during processing as discussed at capture1.3
- 2) Before diffusion: Wafer's backside will grow film due to the process feature. Particle or residue will be covered by grown film.
- 3) After dirty process: according to actual inline condition, generally, scrubber step will be added after this process.

Add Step	Target
Before litho process	Protect from cross contamination
Before DIFF process	Pre-clean to remove the particle
After dirty process	Inline monitor worse tool should be special handle

TRACING ANALYSIS THROUGH IMAGE RECOGNITION

According to the current production experience, most of backside special map have a one-to-one correspondence with equipment's parts on geometric view.

A typical defect map which has the same shape with related parts was shown in Fig14.

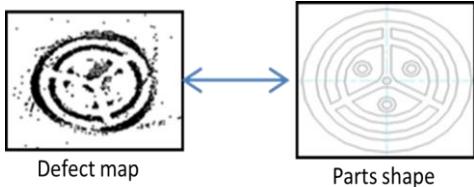


Fig. 14 backside defect map is on the left, parts outline drawing is on the right

A database includes all parts which may contact the backside should be setup and invoked, in the event of an unexpected scratch, residue or stained happened.

Here is a method to get all parts' information. One wafer is used to finish several cycles at target tool. This cycled wafer will be inspected. The scan result has all parts information which presented with a form of special map.

Like the art of printing. Oxide deposition on wafer's backside is a better choice, rather than bare silicon wafer which is too hard to print.

Fig.15 shows a wafer map print all equipment's information, including robot, aligner and chuck which touched through several cycle.

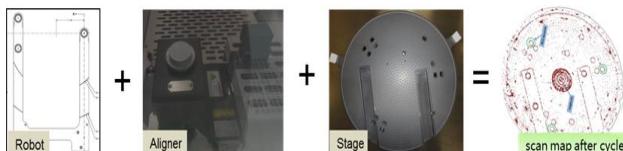


Fig. 15 Robot, aligner and chuck image print at one wafer.

As discussed above, the defect count cannot characterize the backside's severity under certain condition. It's more telling by a backside picture than a defect map in a situation of full of distraction. How to identify and quantify these pictures is expounded in the following content.

The information get from scanning backside includes image and map. Benefit by the development of image processing technology. Backside image can convert to grayscale value. A threshold should be set for filter the noise. Finally,

a purity image as Fig. 16(b) shows with vector value contain tool's parts shape data is collected.

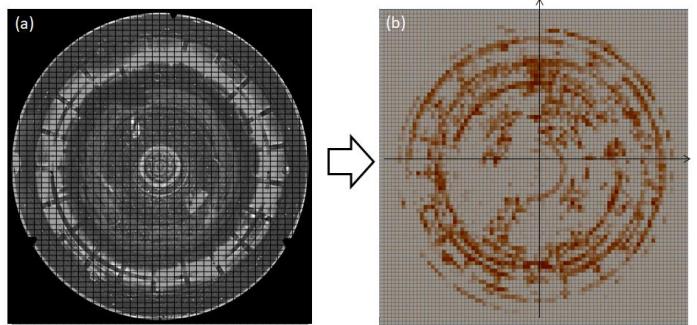


Fig. 16(a) backside image cut into PBS, (b) backside image digitized in a two-dimensional

The parts image from database is also put in a two-dimensional coordinate system. As a result, the monitor image has the same geometric relationship with the parts image.

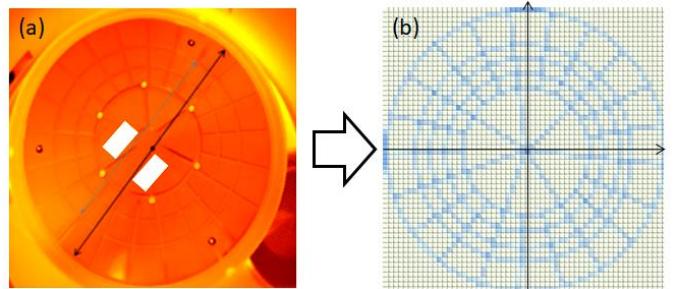


Fig. 17(a) parts image with special figure, (b) parts image digitized in a two-dimensional

Thus, worse backside image scanned by inline backside inspection tools, especially which have special shape can be solved easily by geometric calculate.

CONCLUSION

The challenge of backside inspection is described. The backside defect count index is not applicable under specific conditions. According to the accuracy of backside inspection, applied to wafer start, FEOL, BEOL and shipment stage respectively can bring huge economic benefits in the case of low-cost quotas on backside inspection. Hot spot on the backside is the worst impact during litho process. Improving backside cleanliness is discussed and the solution is given. Add scrubber before litho process, diffusion process and after dirty tool is highly recommended.

Printing the backside is a Convenient and efficient method to collect tool's parts information. Based on the

database, backside image which is digitized and transform by coordinate system can find the similar parts by compare with the database.

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