



CONVOLUTIONAL NEURAL NETWORK (CNN) FOR WAFER EDGE AUTOMATIC DEFECT CLASSIFICATION (ADC)

EG3611A Industrial Attachment Interim Presentation

Name: Tam Zher Min

Company: Systems on Silicon Manufacturing Company (SSMC)

Supervisor: Ms. Pascale Tan

NUS Mentor: Professor Vincent Lee



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01

COMPANY OVERVIEW



COMPANY OVERVIEW

- SSMC is a semiconductor fabrication company
- Joint venture between NXP (Netherlands) and TSMC (Taiwan)
- Recently shipped their 10 millionth wafer in 2020
- Intern under QRA (Quality & Reliability Assurance) Department

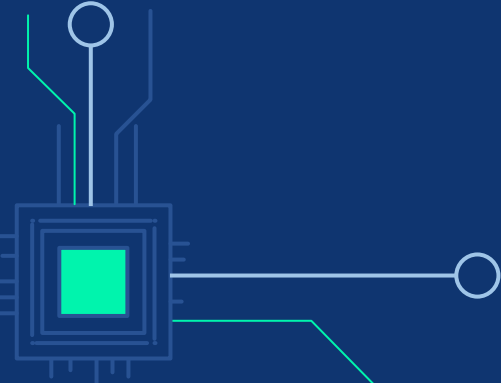




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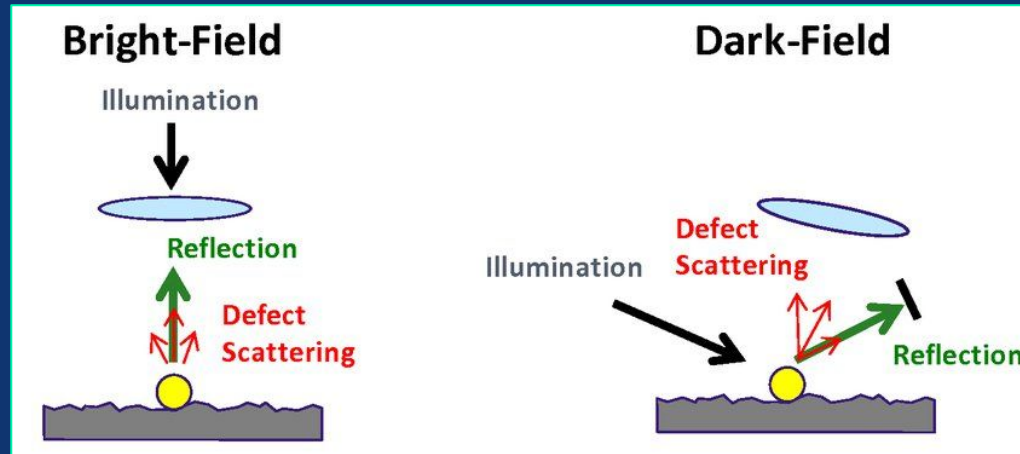


PROJECT REQUIREMENTS



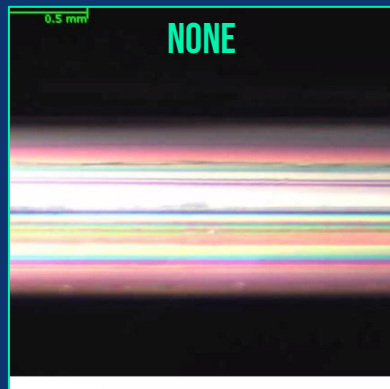
THE PROBLEM

- Silicon wafers encounter defects during wafer fabrication process
- Defects **lower yield** and **impact revenue**
- Specialised machines used to find tiny defects
- **Still difficult** to classify defects **without the help of human inspection**



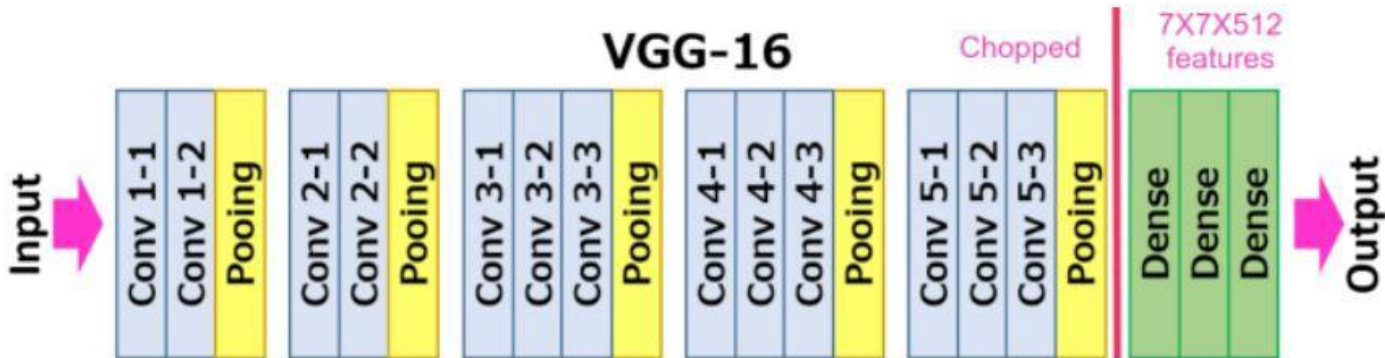
THE TASK

- Defects can occur on the frontside, backside, or edges (focus currently)
- “Defects” flagged by the machines are often false positives
- To gather wafer edge images and train a machine learning (ML) model
- Goal: predict if there is chipping, or not



THE SOLUTION

- CNNs work well with images even with limited data through transfer learning
- Transfer learning is using models trained on millions of images, eg. cats, dogs
- By removing a small part of their model, I can customize it for my problem

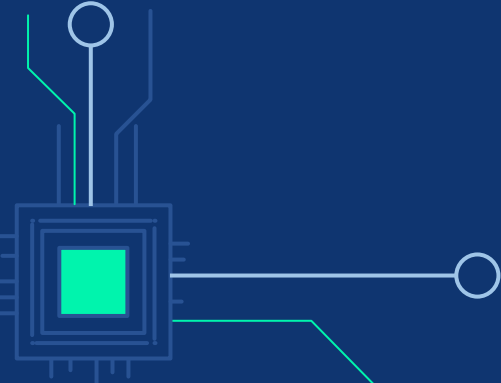




03



PROGRESS & RESULTS



PROGRESS TIMELINE

#1

PRELIMINARY TESTING PHASE

- Using online datasets
- Researching about CNNs and ML training techniques
- Writing custom models

#2

MODELLING WITH REAL DATA

- Saving, loading and sorting of edge scans
- Coding the models and making them work
- Leveraging transfer learning

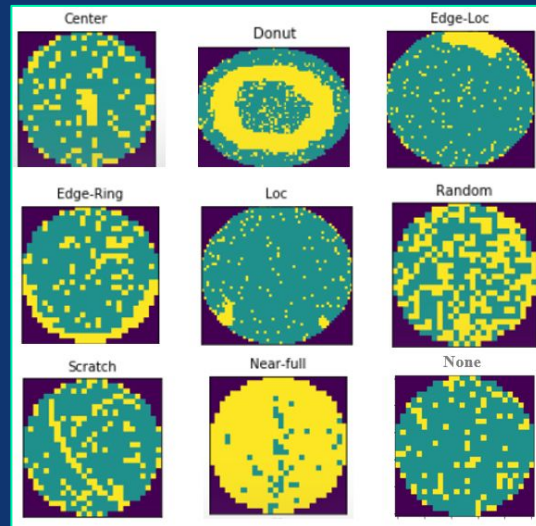
#3

MODEL FINE TUNING

- Testing on new data and recording results
- Implementing different techniques to improve performance

#1 PRELIMINARY TESTING PHASE

- Did not have actual images of the wafer edges yet
- Found wafer defect dataset online, “WM-811K”
- Contains 811,457 wafer maps for wafer frontside
- Poor initial results due to wrong usage of data (~50% acc)
- Performance improved after more research and trial-and-error (~90% acc)



#2 MODELLING WITH REAL DATA

- Obtained 2235 non-chipping images but only 30 chipping images
- This heavy class imbalance poses a big challenge when training models
- Using transfer learning and managing the imbalance mitigates this problem

	TEST_CORRECT	TEST_TOTAL	TEST_ACC
VGG16_30-SEP	4700	4793	98.1%
VGG16_12-OCT	4530	4577	99.0%
VGG16_13-OCT	4571	4577	99.9%

#3 MODEL FINE TUNING

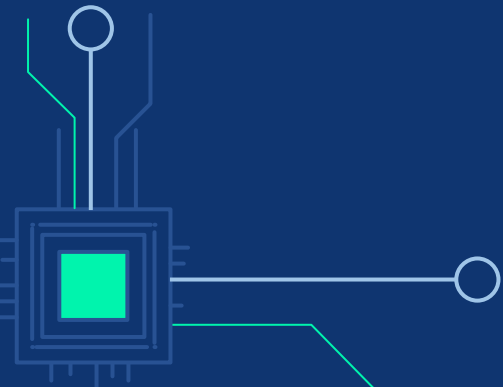
- Experimentation with hyperparameter tweaking and other techniques to improve accuracy
- For example, the **class imbalance problem** has many solutions:
 1. **Undersampling** majority class
 2. **Oversampling** minority class
 3. **Class weights** - Ratio to balance the classes based on quantity
 4. **Data inflation** - Augmenting existing data to inflate dataset
 5. **SMOTE** (Synthetic Minority Oversampling Technique) - “New” data
 6. **Ensemble voting** - Multiple models “vote” for a correct answer
 7. **Focal loss** - Scales loss function to prioritize hard negative examples



04



CHALLENGES & LEARNINGS

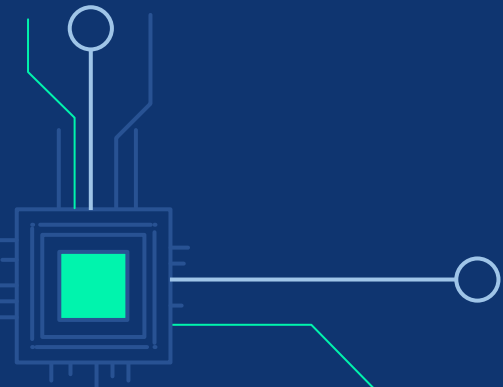


CHALLENGES	LEARNINGS
Data collection and data pipelining	Wafer fabrication process and scripting
Research and implementation	Resourcefulness and programming skills
Debugging and experimenting	Patience and grit
Reporting and documentation	Automating results saving and updating code explanations periodically

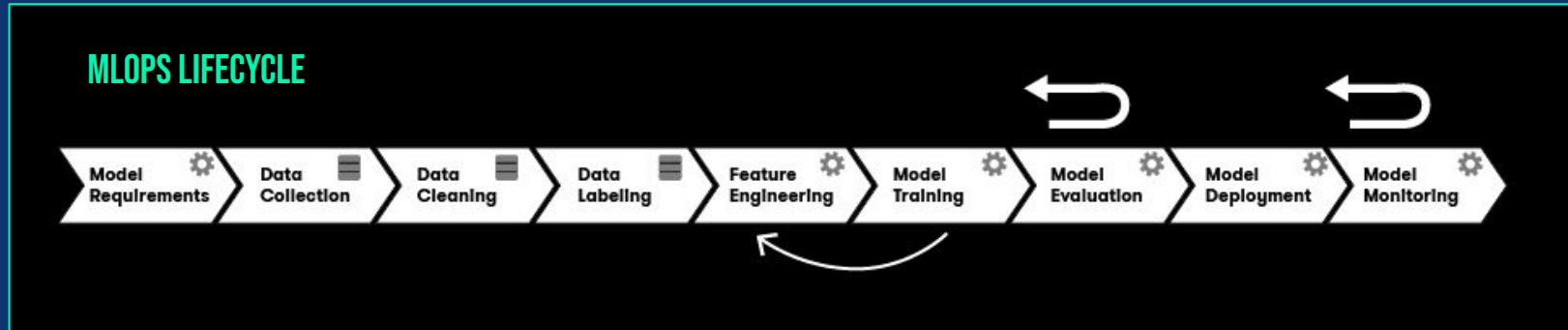


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UPCOMING PLANS



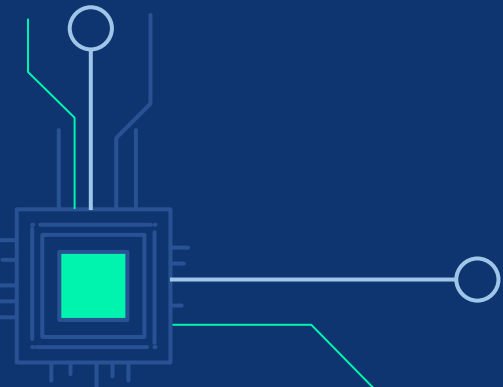
1. More **data collection** for model robustness
2. More **experimentation** for performance improvements
3. Modelling for **wafer backside** defect classification
4. **MLOps** - Deployment and maintenance lifecycle for ML models
5. **Extensive documentation** for solution proposals and handover





06

CONCLUSION



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MAIN TAKEAWAY

DON'T BE AFRAID OF WHAT I DON'T KNOW

A series of light blue lines and dots forming a circuit-like pattern in the bottom left corner of the slide.



THANK YOU!

Q&A

