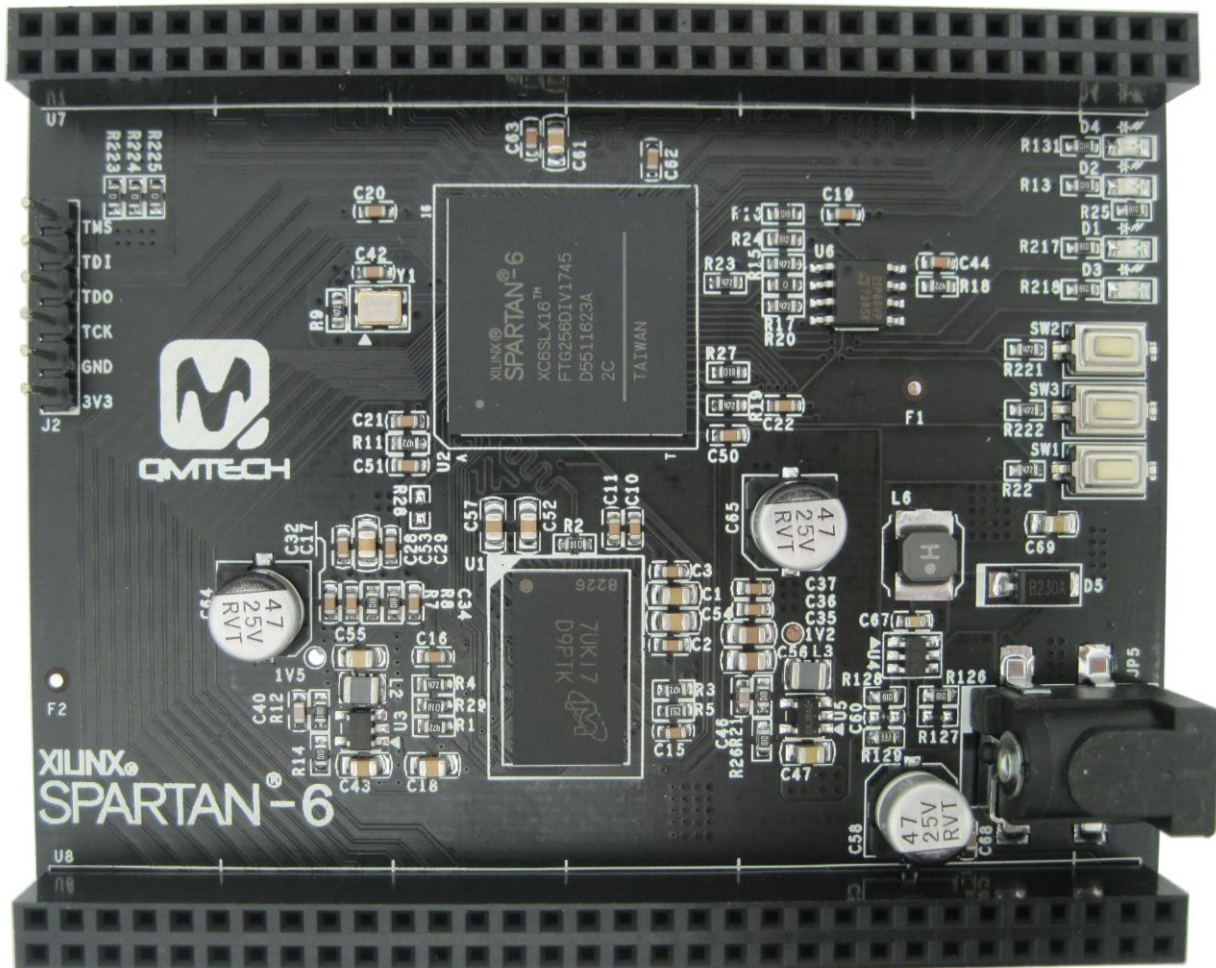


# QM\_XC6SLX16\_DDR3 CORE BOARD

## USER MANUAL



### Preface

The QMTech® XC6SLX16 DDR3 core board uses Xilinx's Spartan®-6 XC6SLX16-2FTG256C device to demonstrate industry leading connectivity features such as high logic-to-pin ratios, small form-factor packaging, MicroBlaze™ soft processor, 800Mb/s DDR3 support, and a diverse number of supported I/O protocols. Built on 45nm technology, the devices are ideally suited for advanced bridging applications found in automotive infotainment, consumer, and industrial automation.



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# 1. Introduction

## 1.1 Document Scope

This demo user manual introduces the QM\_XC6SLX16\_DDR3 core board and describes how to setup the core board running with application software Xilinx ISE 14.7. Users may employ the on board rich logic resource FPGA XC6SLX16-2FTG256C and large DDR3 memory MT41J128M16JT-125 to implement various applications. The core board also has 108 non-multiplexed FPGA I/Os for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

## 1.2 Kit Overview

Below section lists the parameters of the QM\_XC6SLX16\_DDR3 core board:

- On-Board FPGA: XC6SLX16-2FTG256C;
- On-Board FPGA external crystal frequency: 50MHz;
- XC6SLX16-2FTG256C has rich block RAM resource up to 576Kb;
- XC6SLX16-2FTG256C has 14,579 logic cells;
- On-Board M25P80 SPI Flash, 1M bytes for user configuration code;
- On-Board 256MB Micron DDR3, MT41J128M16JT-125;
- On-Board 3.3V power supply for FPGA by using MP2359 wide input range DC/DC;
- XC6SLX16 development board has two 64p, 2.54mm pitch headers for extending user I/Os. All I/Os are precisely designed with length matching;
- XC6SLX16 development board has 3 user switches;
- XC6SLX16 development board has 4 user LEDs;
- XC6SLX16 development board has JTAG interface, by using 6p, 2.54mm pitch header;
- XC6SLX16 development board PCB size is: 6.7cm x 8.4cm;
- Default power source for board is: 1A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;

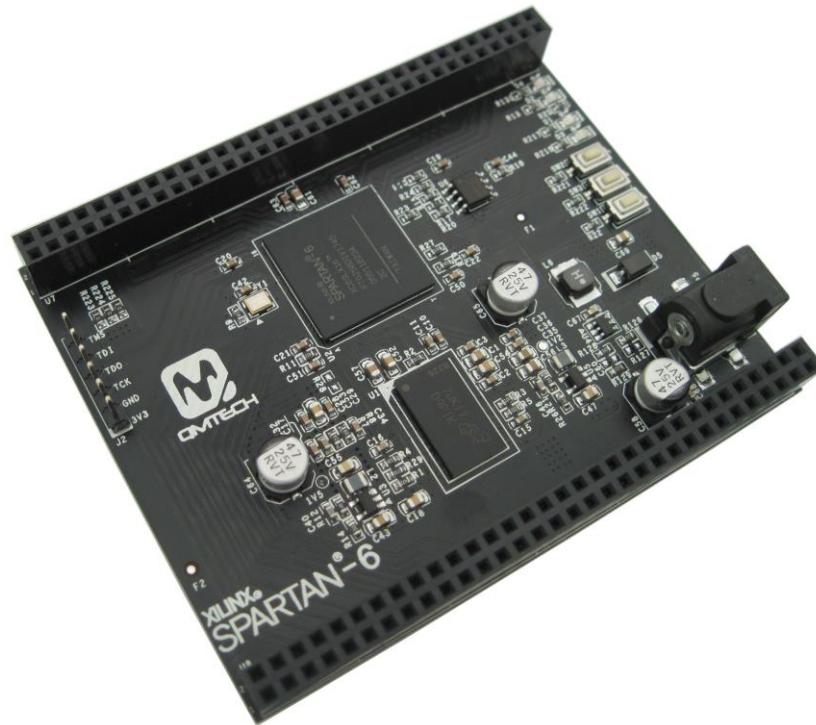


Figure 1-1. QM\_XC6SLX16\_DDR3 Core Board Overview



## 2. Getting Started

The QM\_XC6SLX16\_DDR3 core board includes below item:

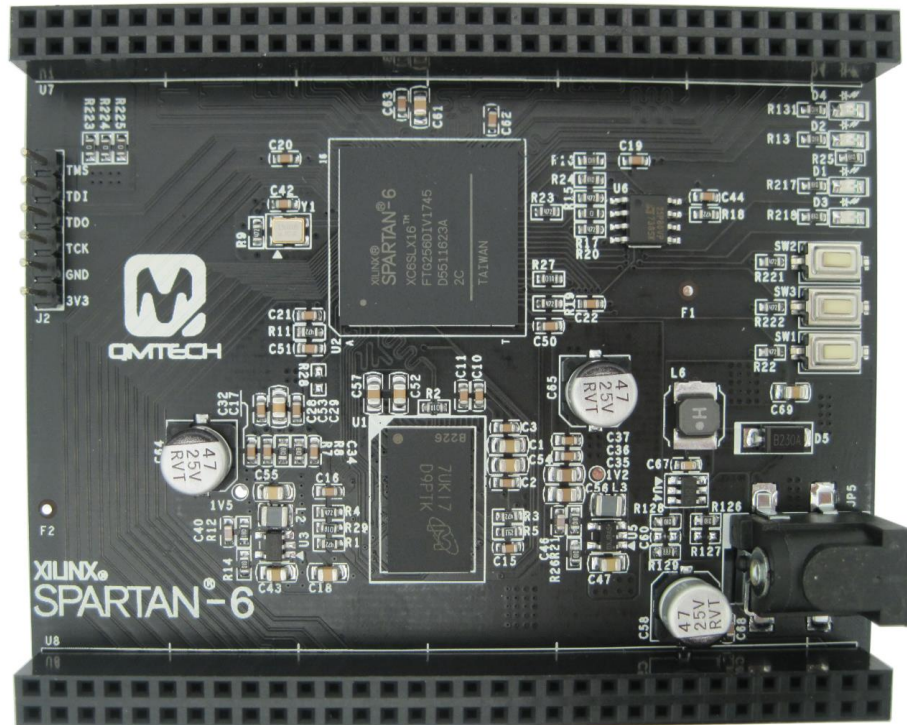


Figure 2-1. QM\_XC6SLX16\_DDR3 Top View

Below image shows the dimension of the QM\_XC6SLX16\_DDR3 core board: 6.7cm x 8.4cm. The unit in below image is millimeter(mm).

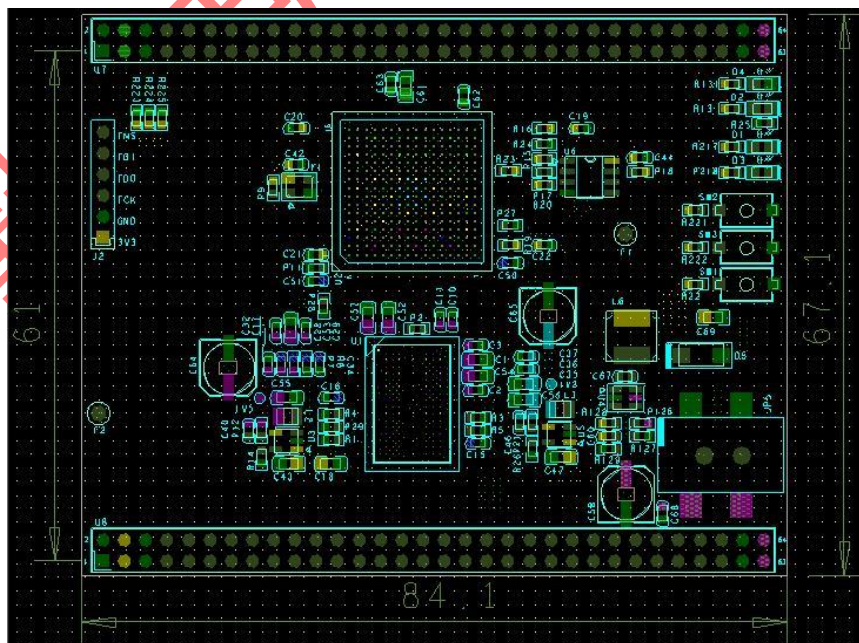


Figure 2-2. QM\_XC6SLX16\_DDR3 Core Board Dimension

## 2.1 Install Development Tools

The QM\_XC6SLX16\_DDR3 core board tool chain consists of Xilinx ISE 14.7, Xilinx USB platform cable, XC6SLX16 core board and 5V DC power supply. Below image shows the Xilinx ISE 14.7 development environment which could be downloaded from [Xilinx office website](#):

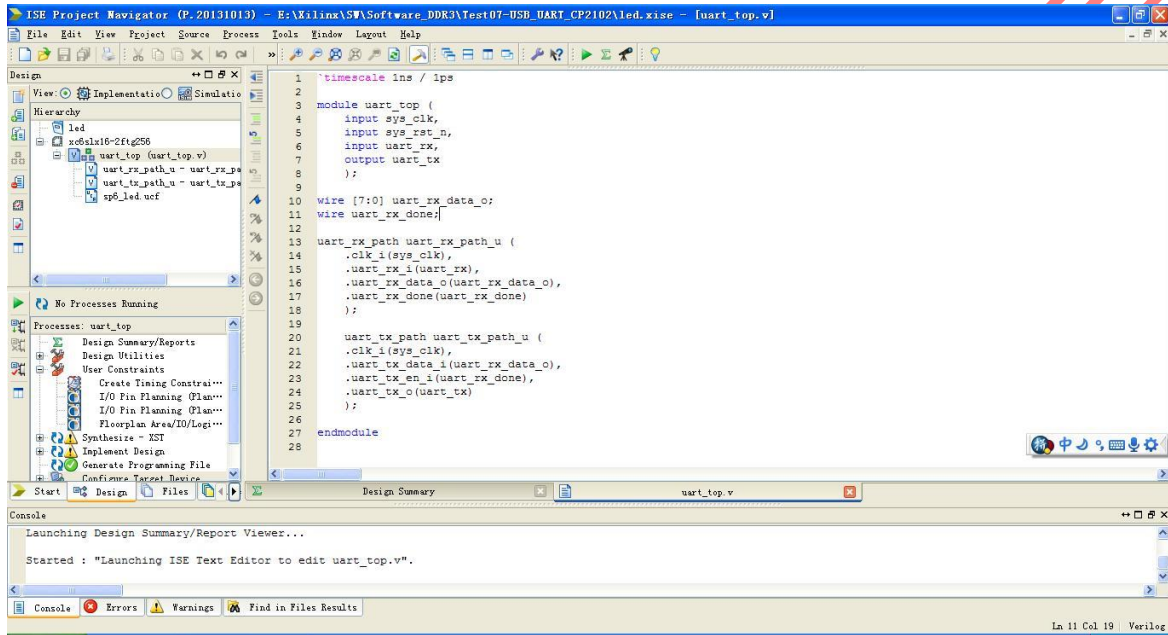


Figure 2-3. ISE 14.7

Below image shows the JTAG connection between Xilinx USB platform cable and XC6SLX16 core board:

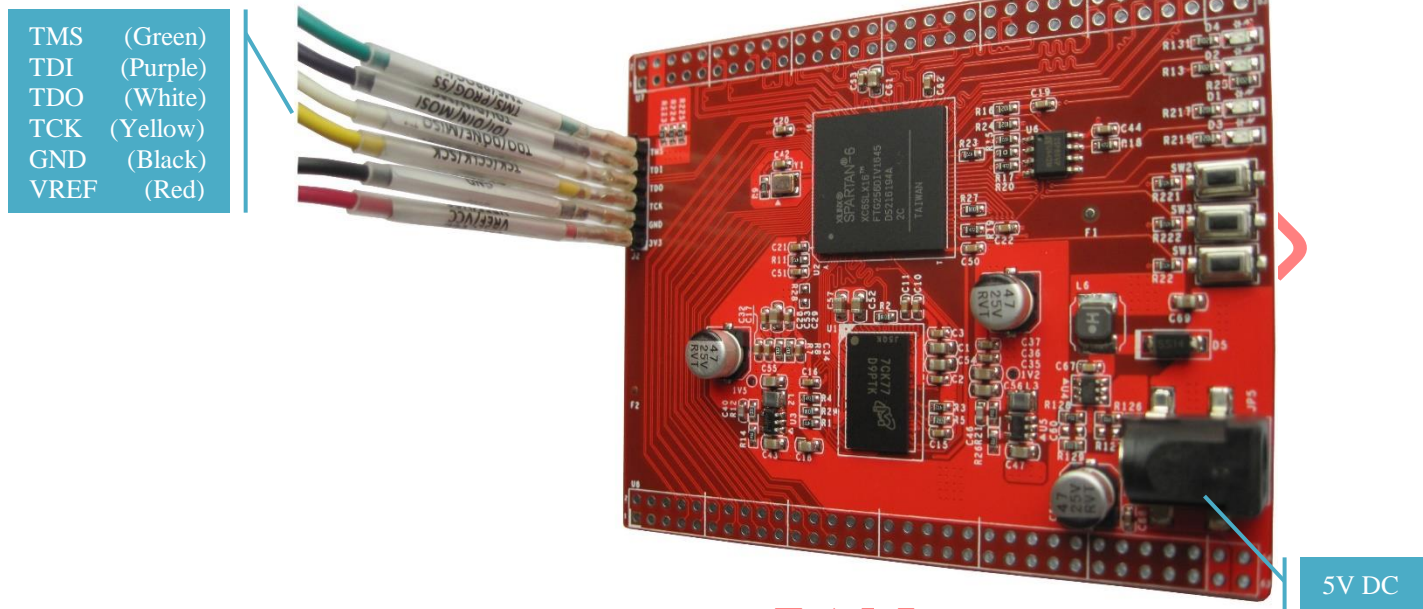


Figure 2-4. JTAG Connection and Power Supply

## 2.2 QM\_XC6SLX16\_DDR3 Hardware Design

### 2.2.1 QM\_XC6SLX16\_DDR3 Power Supply

The core board needs 5V DC input as power supply which could be directly injected from power header or the 64P female header U7/U8. Users may refer to the hardware schematic for the detailed design. The on board LED D4 indicates the 3.3V supply, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V. However, BANK1 IO's power level could be changed according to detailed custom requirement. There're three 0 ohm resisters could be removed: R223/R224/R225, and instead the BANK1's power supply could be injected from 64P female header U7. Detailed design refer to hardware schematic.

Note: FPGA core supply 1.2V is regulated by On-Semi DC/DC chip NCP1529 which could output maximum 1A current.

5V DC



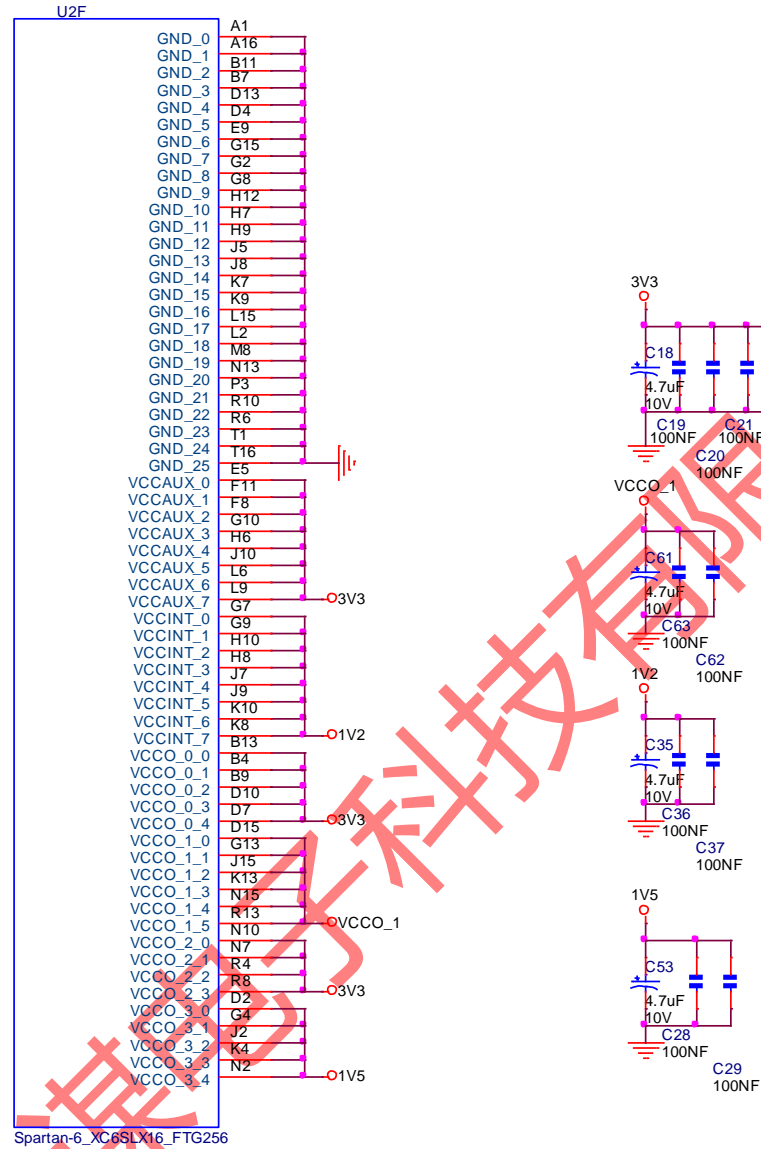
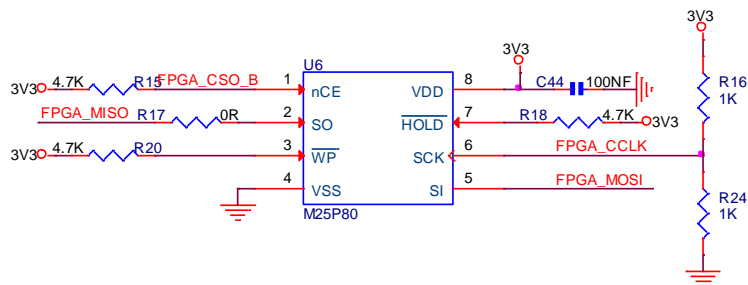


Figure 2-5. Power Supply for the FPGA

### 2.2.2 QM\_XC6SLX16\_DDR3 SPI Boot

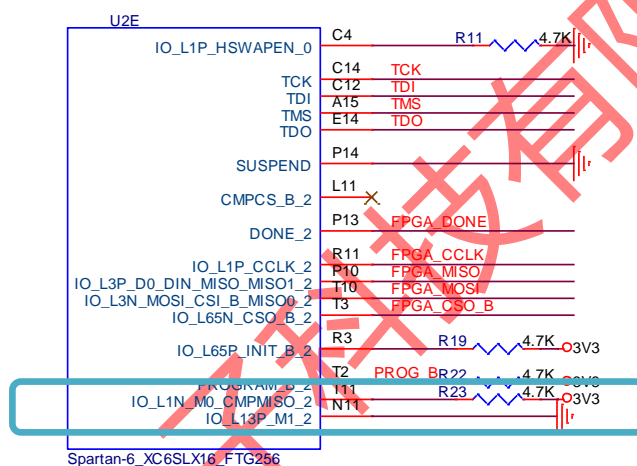
In default, QM\_XC6SLX16 boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using M25P80 manufactured by Micron, with 8Mbit memory storage.





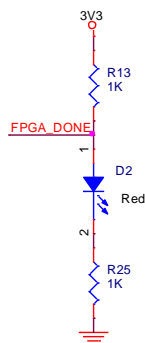
**Figure 2-6. SPI Flash**

The FPGA boot sequence setting M0:M1 is configured as 1:0 which indicates FPGA will boot from SPI Flash after power on.



**Figure 2-7. M0:M1 Hardware Settings**

The LED D2 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D2 could be used as FPGA loading status indicator.



**Figure 2-8. FPGA\_DONE Status Indicator**





### 2.2.3 QM\_XC6SLX16\_DDR3 Memory

QM\_XC6SLX16 has on board 16bit width data bus, 256MB memory size DDR3 MT41J128M16JT-125 provided by Micron. Below image shows the detailed hardware design:

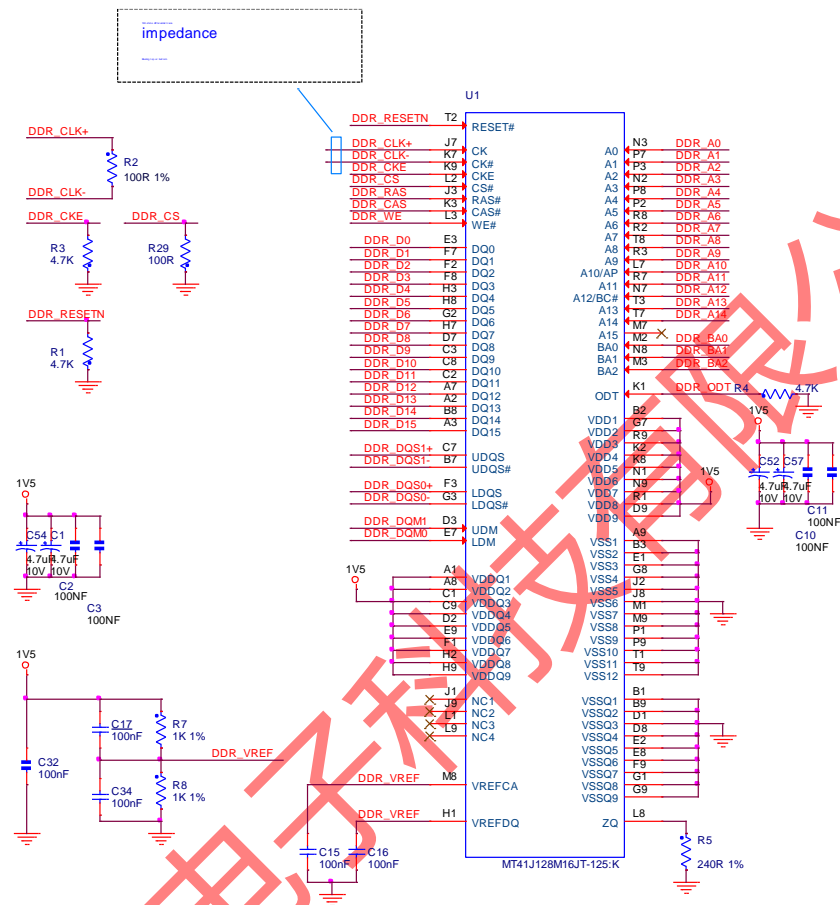


Figure 2-9. DDR3

### 2.2.4 QM\_XC6SLX16\_DDR3 System Clock

FPGA chip XC6SLX16-2FTG256C has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

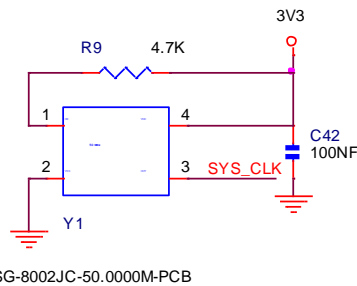


Figure 2-10. 50MHz System Clock



### 2.2.5 QM\_XC6SLX16\_DDR3 Extension IO

The core board has two 64P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

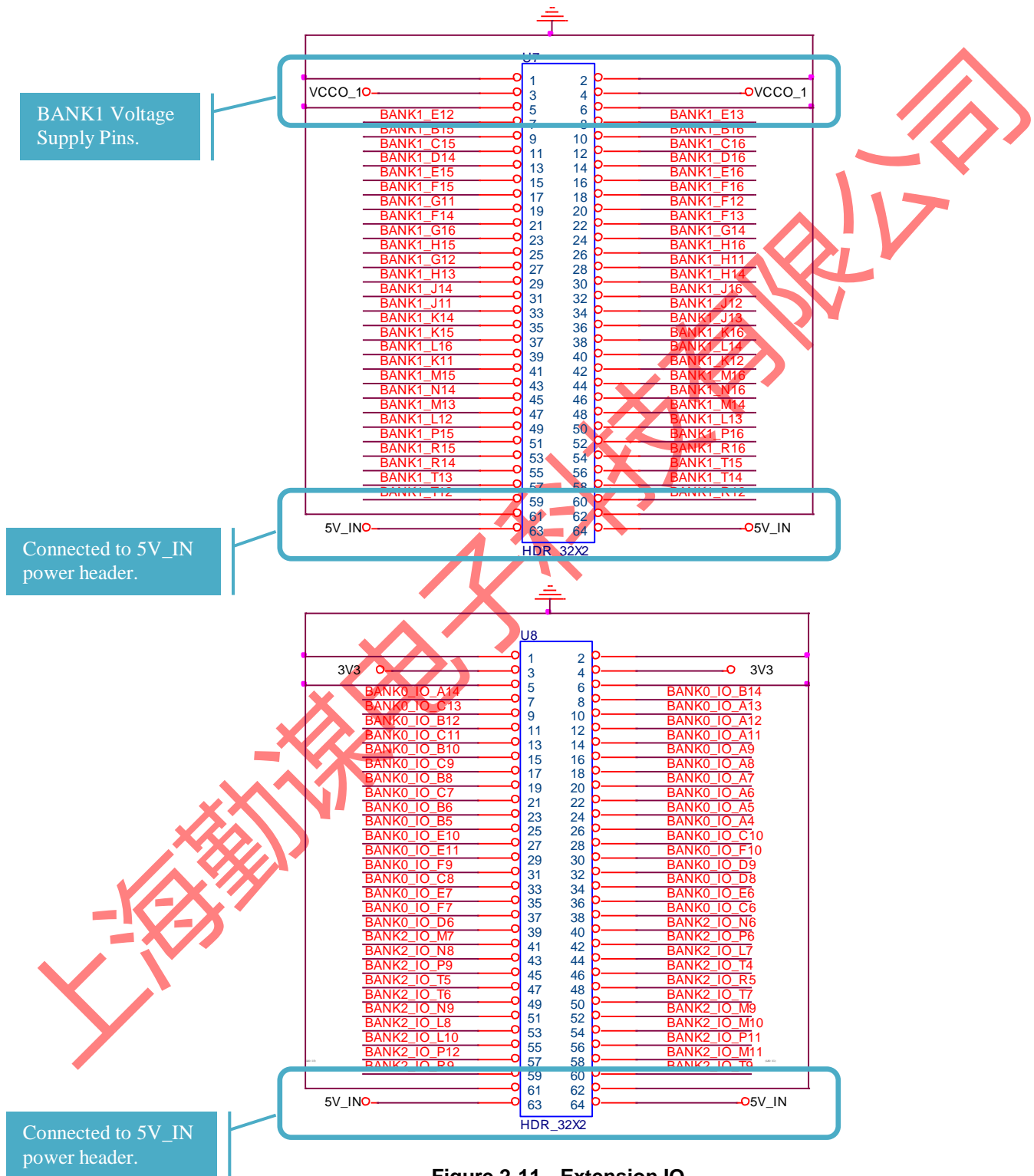


Figure 2-11. Extension IO





## 2.2.4 QM\_XC6SLX16\_DDR3 User Key

Below image shows the PROGRAM\_B key and two user keys:

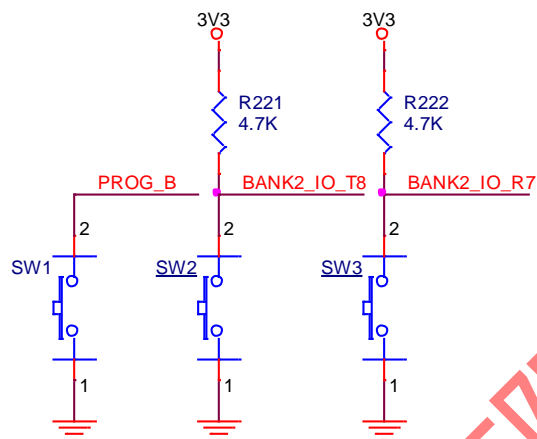


Figure 2-15. Keys





### 3. Reference

- [1] ug380-Configuration.pdf
- [2] ug385-Package.pdf
- [3] ug394-Power Managment.pdf
- [4] M25P80.pdf
- [5] LPC-Link-II\_Rev\_C.pdf
- [6] QM\_XC6SLX16.pdf

上海勤谋电子科技有限公司



#### 4. Revision

Doc. Rev.	Date	Comments
0.1	05/10/2017	Initial Version.
1.0	05/14/2017	V1.0 Formal Release.
2.0	03/31/2018	V2.0 Release. Changed the PCB color.

