

```
RAM: 0x0000 - 0x7FFF
PRP: 0x8000 - 0x8FFF
SER: 0x9000 - 0x9FFF
VID: 0xA000 - 0xAFFF
ROM: 0xB000 - 0xFFFF
```

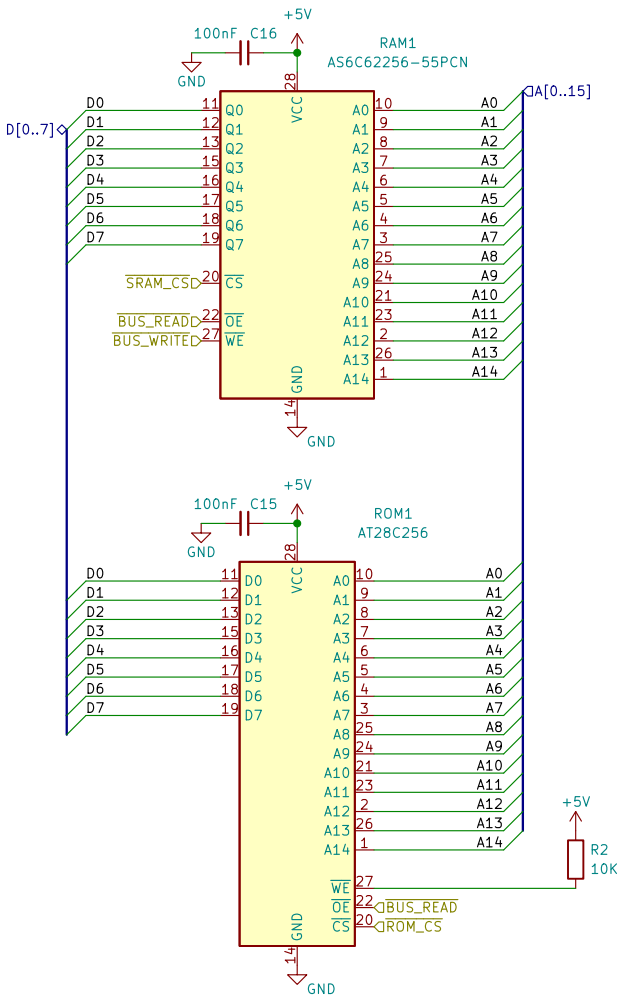
This map will be programmed into the FPGA

Sheet: /
File: 8puter.kicad_sch

Size: A4	Date:
KiCad E.D.A. kicad 6.0.4-1.fc35	

Rev: 1.0
Id: 1/6

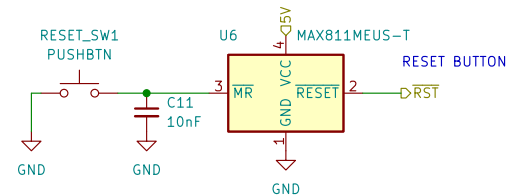
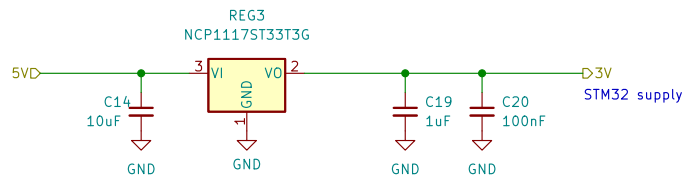
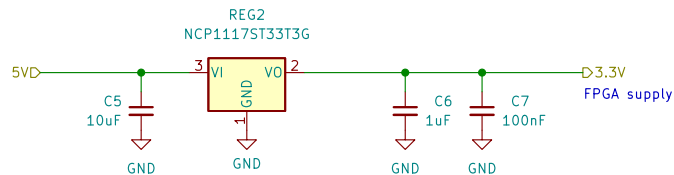
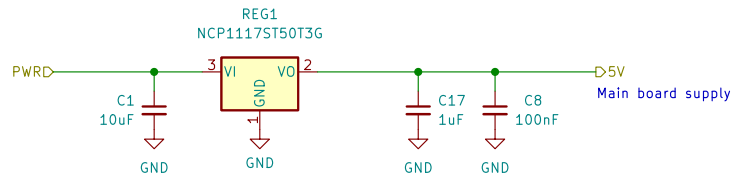
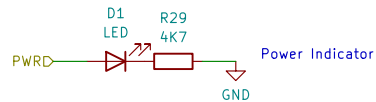
System Memory



RAM: 0x0000 - 0x7FFF
ROM: 0xB000 - 0xFFFF

zrthxn	
Sheet: /Memory Unit/ File: memory.kicad_sch	
Title: 8puter	
Size: A4	Date:
KiCad E.D.A. kicad 6.0.4-1.fc35	Rev: 1.0 Id: 2/6

Power Delivery



zrthxn

Sheet: /Power/
File: power.kicad_sch

Title: 8puter

Size: A4 Date:
KiCad E.D.A. kicad 6.0.4-1.fc35

Rev: 1.0
Id: 3/6

[illegible][illegible]

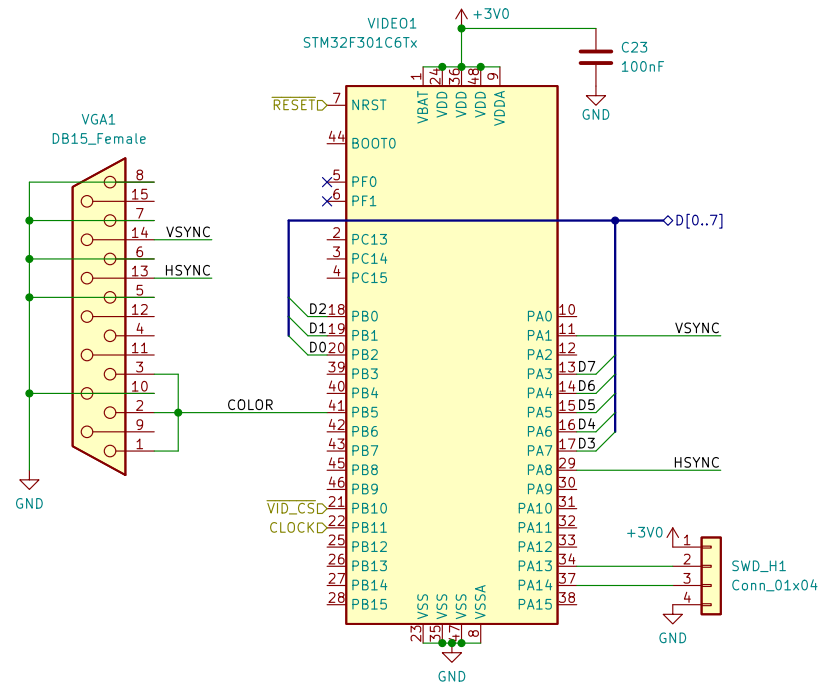
zrthxn Sheet: /Peripheral Handler/ File: peripheral.kicad_sch	
Title: 8puter	
Size: A4	Date:
KiCad E.D.A. kicad 6.0.4-1.fc35	Rev: 1.0 Id: 4/6

Video Controller

Video will be generated using a microcontroller which is fast enough to generate the VGA timing signals.

CPU will send a single byte to the MCU which can be a char code or index of glyph, and the MCU just generates the video signal.

This setup is limited in generating graphics but it avoids having to keep a large framebuffer.



zrthxn

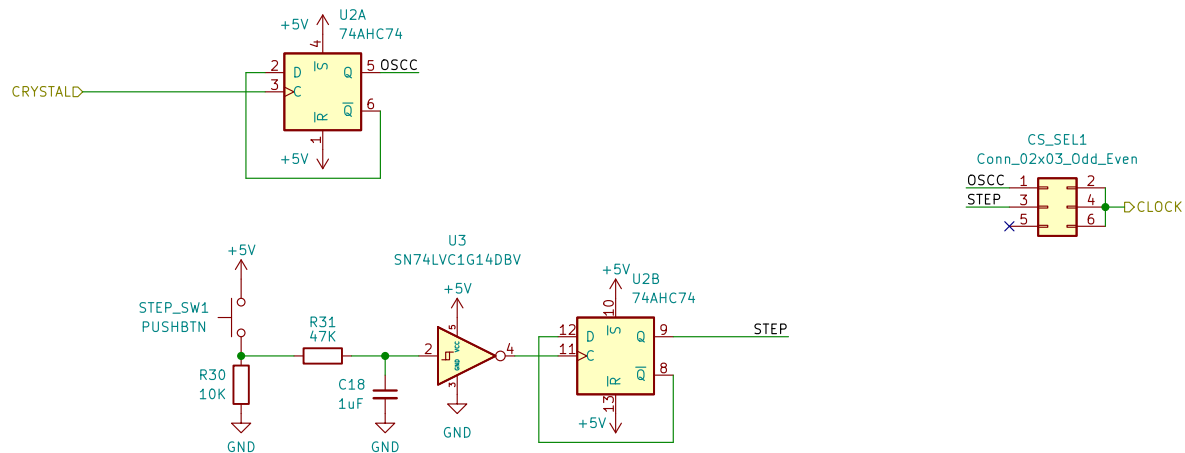
Sheet: /Video/
File: video.kicad_sch

Title: 8puter

Size: A4 Date:
KiCad E.D.A. kicad 6.0.4-1.fc35

Rev: 1.0
Id: 7/6

Clock Source Select



Clicking the button will take us to the next HALF clock cycle.

zrthxn

Sheet: /Clock/
File: clock.kicad_sch

Title: 8puter

Size: A4
KiCad E.D.A. kicad 6.0.4-1.fc35

Date:

Rev: 1.0

Id: 8/6