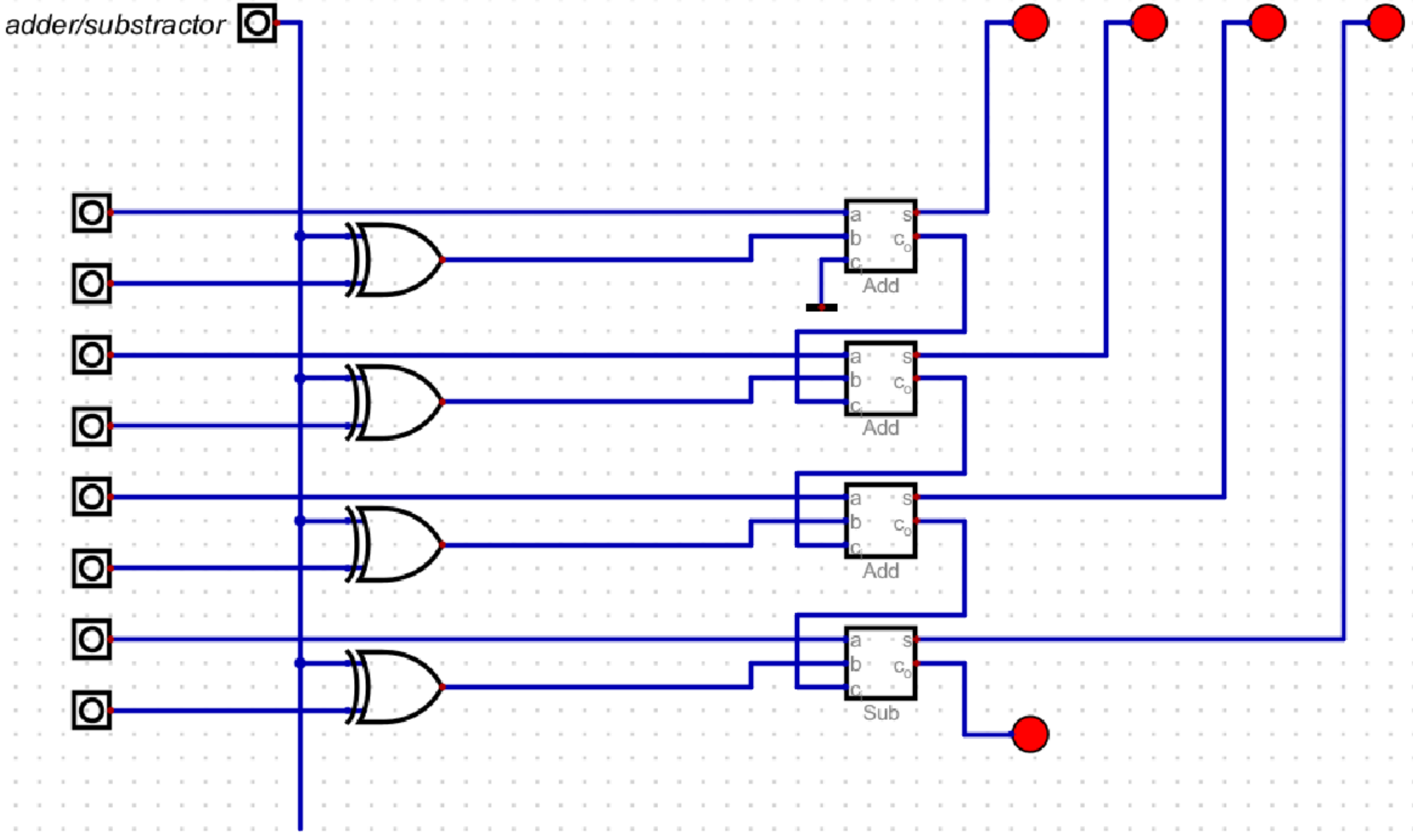
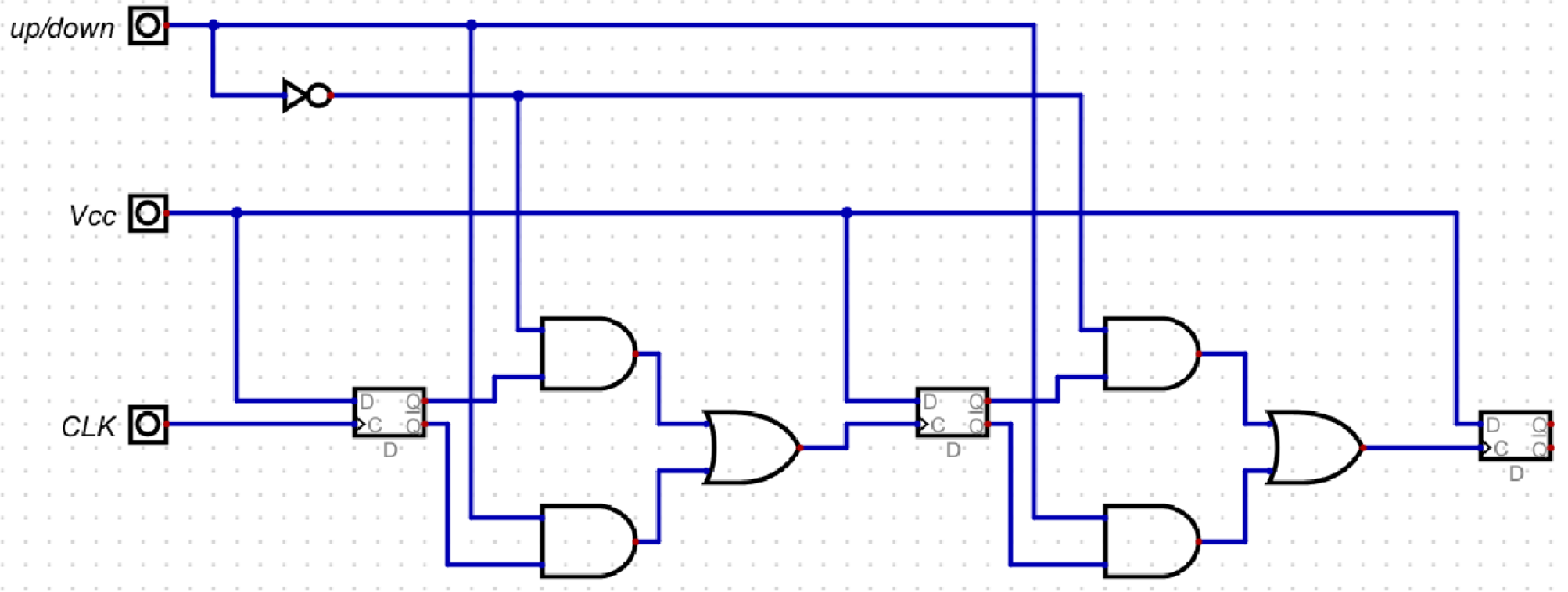

adder/substractor
a
b
c
s
co
Add
Add
Add
Sub


up/down
Vcc
CLK
D
Q
C
Q
D
D
Q
C
Q
D
D
Q
C
Q
D

CS 303 Homework 3

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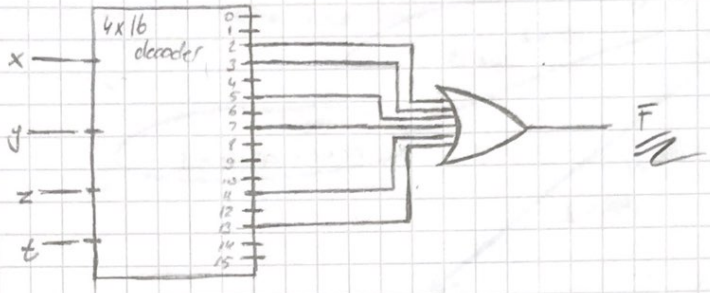
0002325

Q1) $F(x, y, z, t) = \prod(0, 1, 4, 6, 8, 9, 10, 12, 14, 15)$

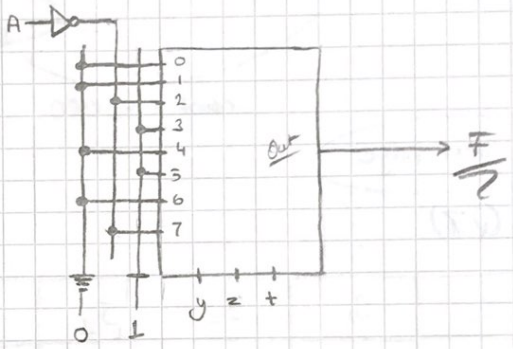
a-) using decoder and or gate

$F(x,y,z,t) = \prod(0,1,4,6,8,9,10,12,14,15) = \sum(2,3,5,7,11,13)$



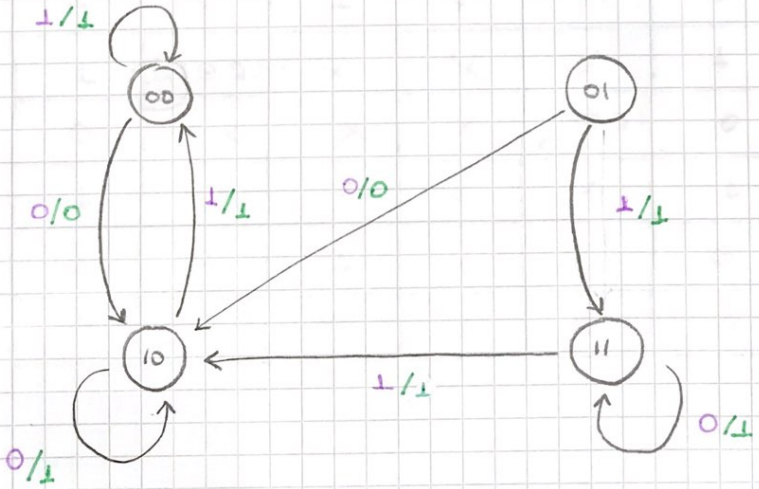
b-)

A'	0	1	2	3	4	5	6	7
A	8	9	10	11	12	13	14	15
	0	0	A'	1	0	1	0	A'
	0	1	2	3	4	5	6	7



Q2)

b) Draw the state diagram of the state table



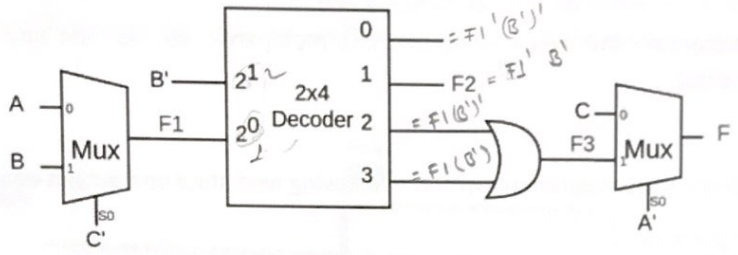
Q3) Design a 4-bit signed/unsigned adder/subtractor circuit. Circuit will have a signed_unsigned input pin to determine the signed/unsigned operation and an adder_subtractor pin to determine adder/subtractor operation. Draw the circuit diagram.

Signed ~~unsigned~~

Answer in previous page

Q4) Consider the following circuit with three inputs (A, B, C) and one output (F).

a. Derive the Boolean expression of the signals F1, F2, F3 and the output function F.



F3 =

b. Complete the following Verilog code part so that it implements the output F.

```
module function_F (A, B, F);
output F;
input A, B, C;
wire F1, F2, F3;
    always @ ( A or B or C )
    begin
        F1 = (~(~C) & A) || ((~C) & B);
        F2 = ~F1 & ~B;
        F3 = (F1 & ~(~B)) || (F1 & ~B);
        F = (~(~A) & C) || (~A & F3);
    end
```

$F_1 = (C')' A + C' B$

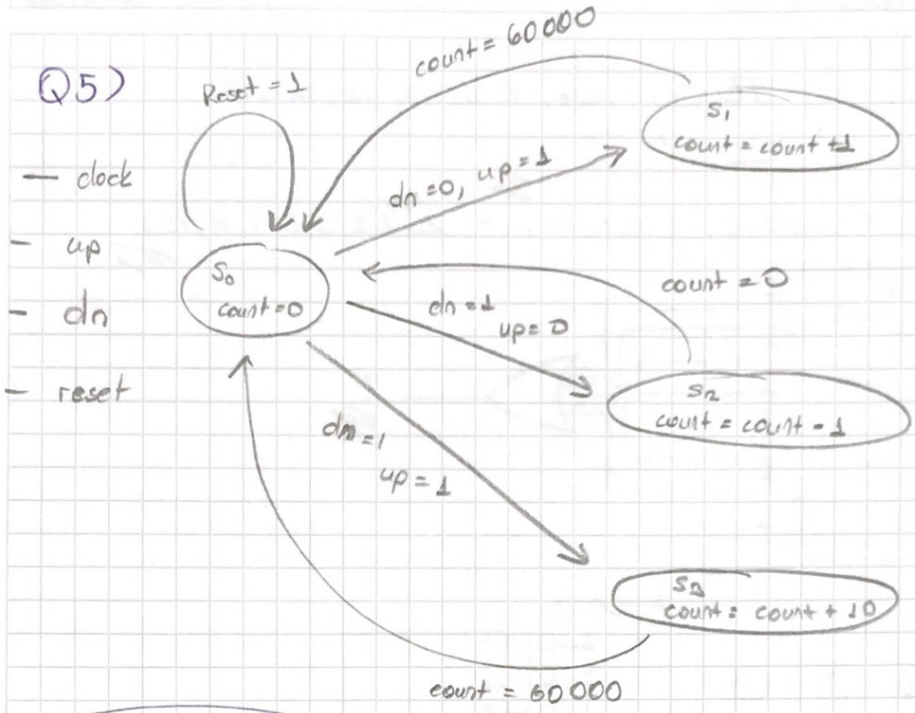
$F_2 = F1' B'$

$F_3 = F1 (B')' + F1 (B')$

$F = (A')' C + A' F2$

Q5)

- clock
- up
- dn
- reset



Q6 in next page

Q7)

S_0	S_1	I_0	I_1	I_2	I_3	F
0	0	$(C \odot A)_1$	X	X	X	1
0	1	X	1	X	X	1
1	0	X	X	1	X	1
1	1	X	X	X	$(C \odot A)_1$	1
0	0	$(C \odot A)_0$	X	X	X	0
0	1	X	1	X	X	1
1	0	X	X	1	X	1
1	1	X	X	X	$(C \odot A)_0$	0