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EE 4513 – Introduction to VLSI Design
Assignment # 5

VLSI Design Using CMOS Ami 0.6 Submicron Technology in Cadence Virtuoso

October 6, 2019

Introduction

This report entails of the cell-based design and simulation of an inverter, 2-AND, 3-NAND, 3-NOR, and a two-level AND-INV network for the purpose of learning VLSI Design in Cadence Virtuoso. The AMI0.6 Submicron technology library from North Carolina State University is used as reference for describing each design with a λ value. Although the largest transistor count explored in this report amounts to a mere 28 MOSFETs—belonging to the label SSI (Small Scale Integration)—the title uses VLSI as a keyword due to the author's class name. Coincidentally, the table below lists attributes pertaining to the design technology.

ATTRIBUTE	VALUE
λ	0.3 micron
Cell Width	15 micron = 50λ
Cell Height	24 micron = 80λ
VDD, GND Rail Width	2.4 micron = 8λ

With this information in mind, the following sections now showcase the design process for each of the logic cells mentioned above.

Inverter

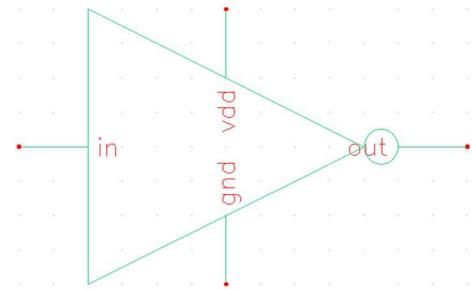


Figure 2: Inverter Symbol

Figure 2 above displays the schematic symbol for the inverter cell as commonly drawn by VLSI designers. Figure 1 on the right displays the inverter design as shown in the Layout window of Cadence Virtuoso. As mentioned in the table above, this cell has a height of 24 micron (80λ) and a width of 15 micron (50λ). It is also important to mention this cell only makes use of the metal 1 layer to bring in pin contacts to the terminals of both PMOS and NMOS FETs. To bring forth a clearer design for the reader, the later sections do not display the grid and measurements as shown in Virtuoso due to the incompatibility of the export feature with extra layers. For the pins of the cell, Figure 3 in the next page displays them clearly along with a brighter image of the inverter. The reader should take into account the markings in Figure 3 to understand the layout as well as the following sections' layouts.

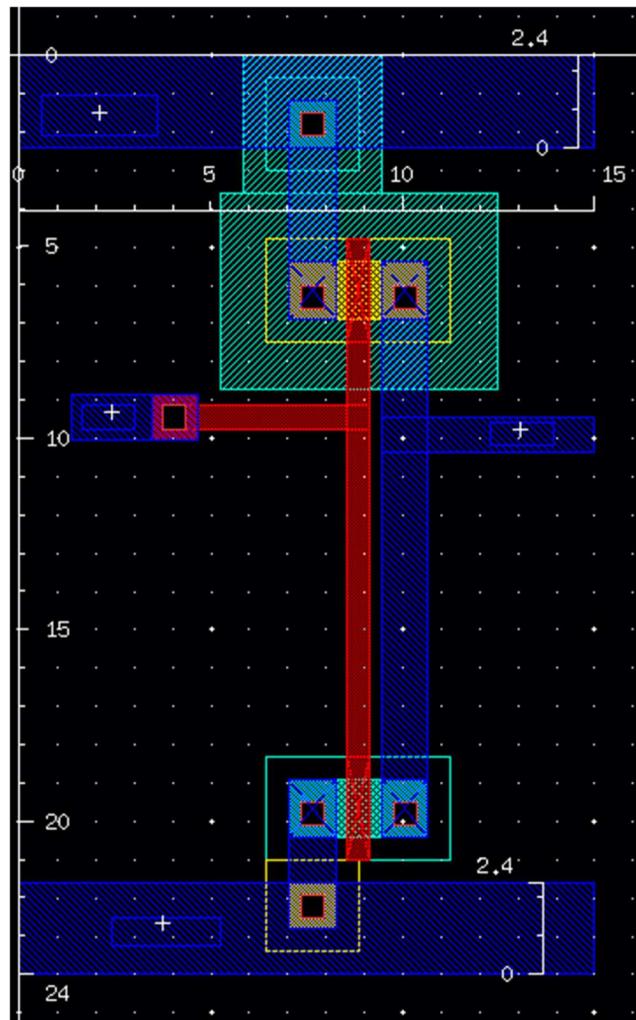


Figure 1: CMOS Inverter Cell

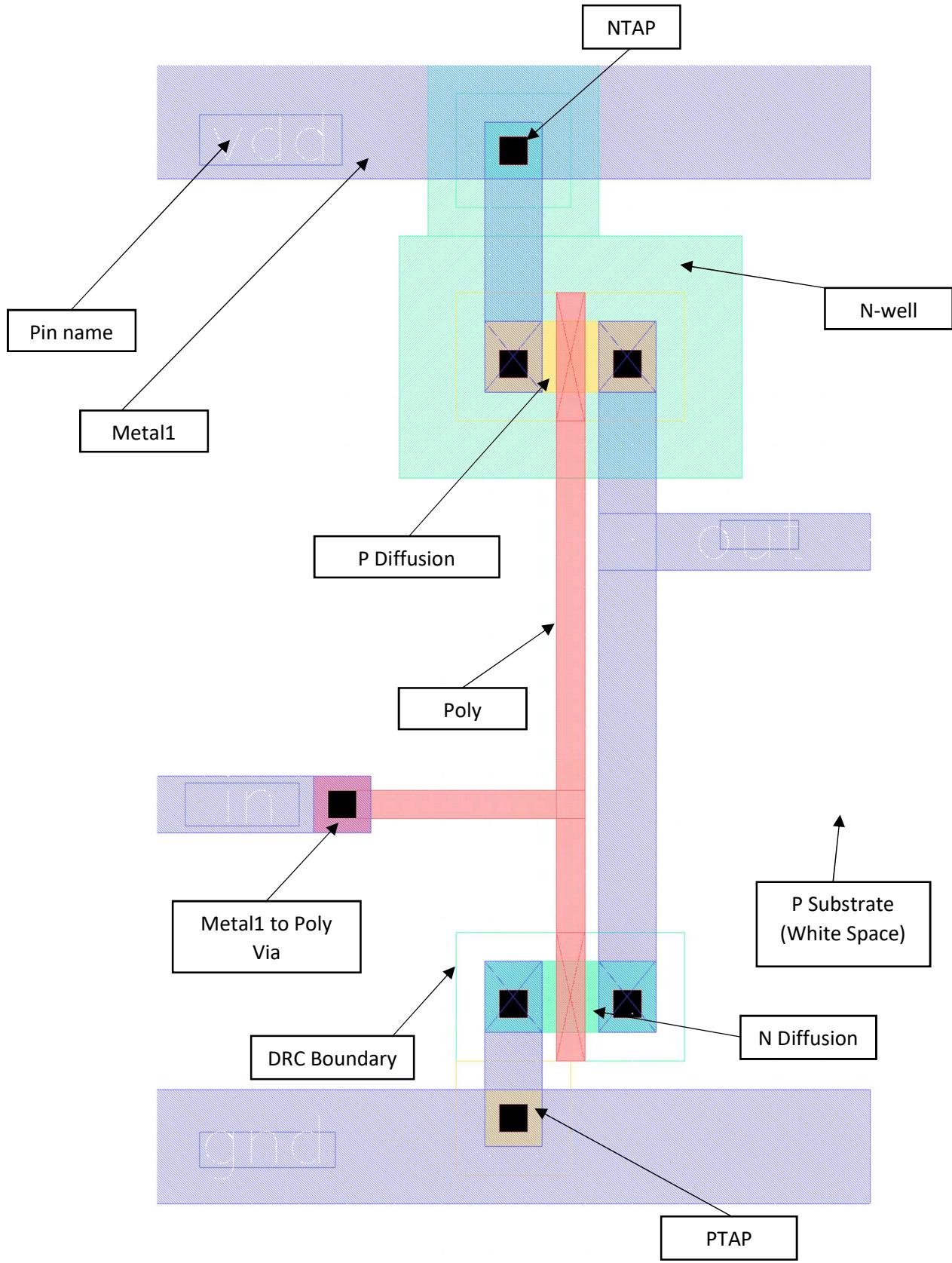


Figure 3: CMOS Inverter with Pins and General Legend

After passing DRC checks, the design is Verified and extracted for the simulation process. Now, the next step is to create a schematic with test signals for testing the desired operation of the Inverter. Figure 4 displays the circuit used to test the inverter using a 5V square wave with a 40ns period at half a duty cycle. This Figure also shows the cell uses 2 MOSFETs. Figure 5 displays the simulation results.

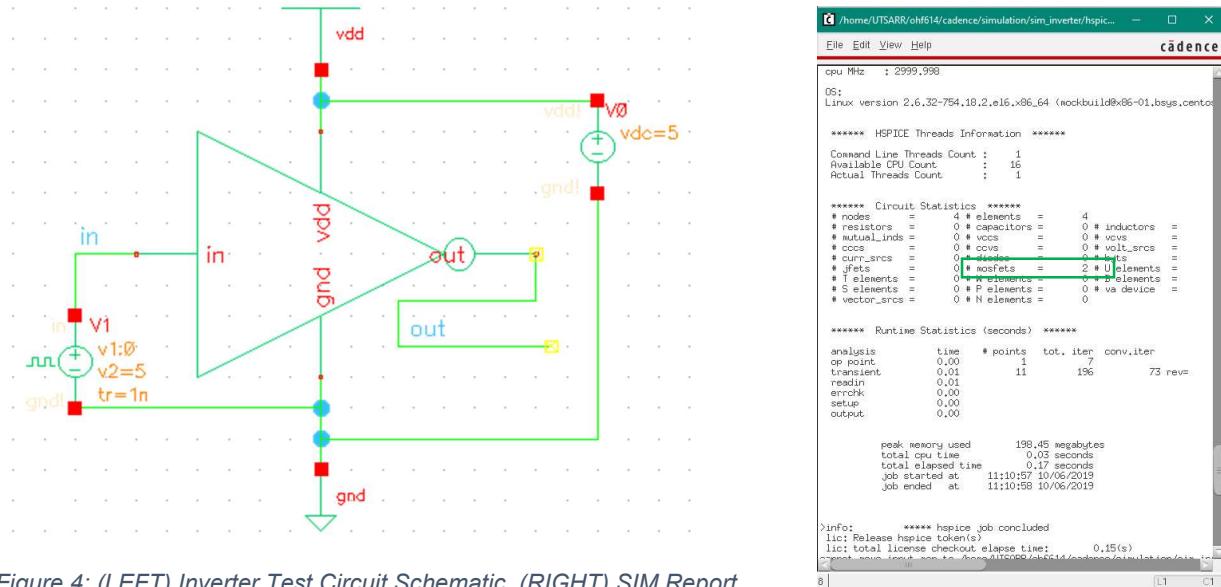


Figure 4: (LEFT) Inverter Test Circuit Schematic, (RIGHT) SIM Report

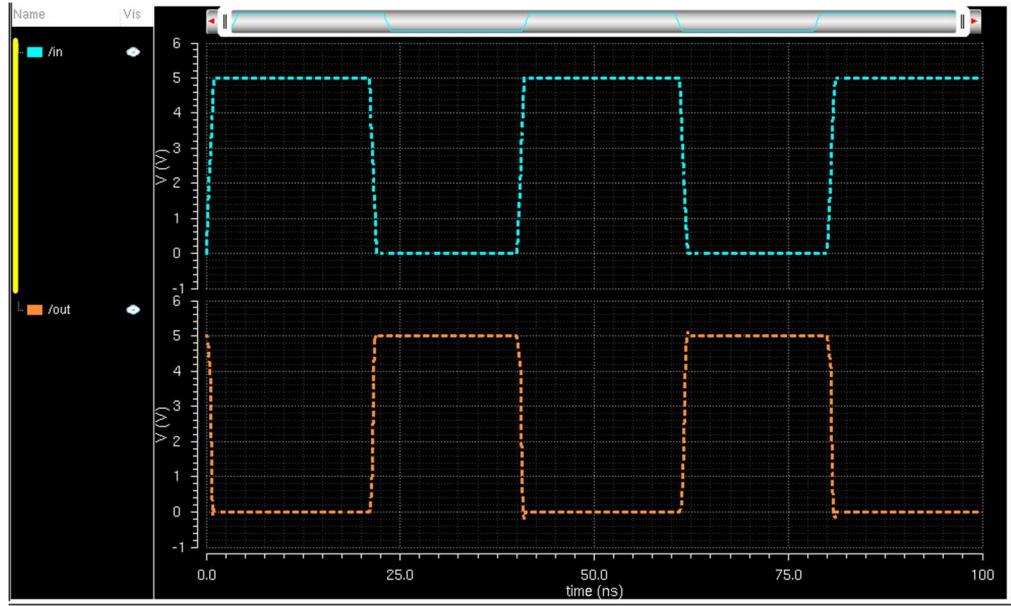


Figure 5: Simulation of Inverter

3-Input NAND

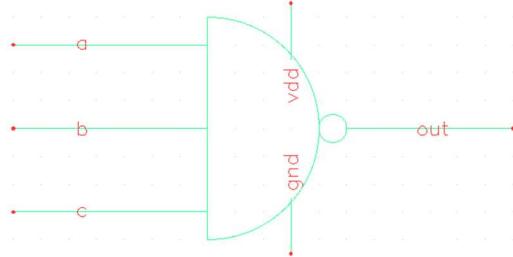


Figure 7: NAND 3 Input Schematic Symbol

The 3-Input NAND cell is explained next. First, the schematic symbol is created in Cadence Virtuoso to map the necessary pins in the layout displayed in Figure 7. Next, the layout is established and built as shown in the right. Figure 6 showcases the pins as defined in the circuit schematic. Here, instead of using 3 fingers and 3 multipliers for the NMOS and PMOS FETs respectively, discrete transistors are used as a learning exercise. Further, the power rails are not the desired 8λ as well. Figure 8 on the next page shows the test circuit built for simulating the operation of the NAND cell.

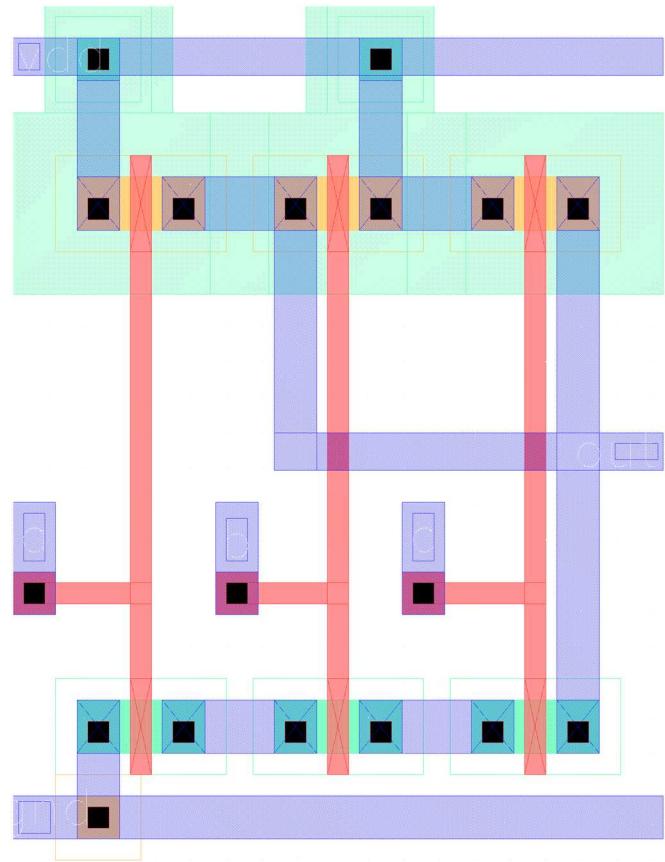


Figure 6: CMOS Layout of NAND 3 Cell

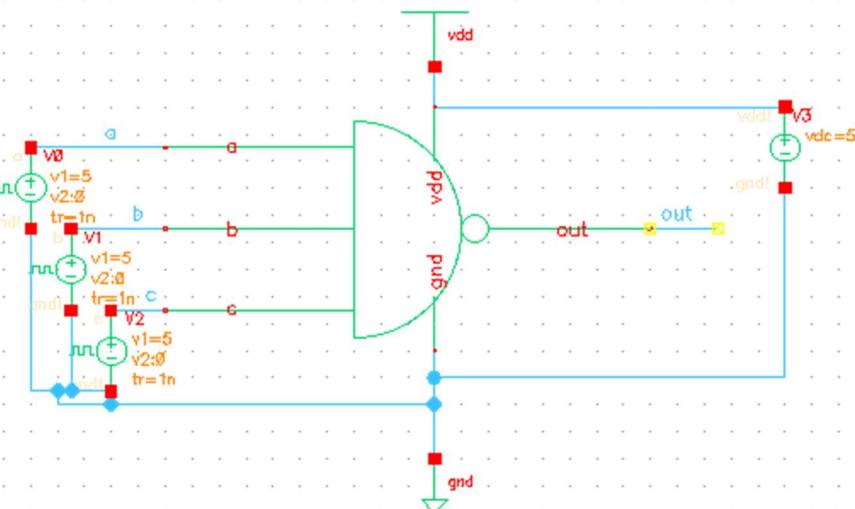


Figure 8: Test Circuit for 3-NAND

The screenshot shows a terminal window titled 'cadence' displaying the results of an HSPICE simulation for a NAND-3 cell. The output includes:

- OS:** Linux version 2.6.32-754.18.2.el6.x86_64 (mockbuild0x06-01.bsys.centos)
- HSPICE Threads Information:**
 - Command Line Threads Count : 1
 - Available CPU Count : 16
 - Actual Threads Count : 1
- Circuit Statistics:**
 - # nodes = 8 # elements = 10
 - # capacitors = 0 # inductors = 0
 - # mutual_inds = 0 # vccs = 0 # vcvs = 0
 - # ccos = 0 # ccvs = 0 # volt_srcs = 0
 - # curv_srcs = 0 # diodes = 0 # bjts = 0
 - # jfets = 0 # mosfets = 0 # U elements = 0
 - # elements = 0 # W elements = 0 # B elements = 0
 - # P elements = 0 # N elements = 0
 - # vector_srcs = 0 # va device = 0
- Runtime Statistics (seconds):**

analysis	time	# points	tot.	iter	conv.
op point	0.00	1	7		
transient	0.00	17	392		137 rev
readin	0.01				
emulk	0.00				
setup	0.00				
output	0.00				
- Memory Usage:**
 - peak memory used 193.48 megarbytes
 - total cpu time 0.01 seconds
 - total elapsed time 6.07 seconds
 - job started at 03:17:11 10/06/2019
 - job ended at 03:17:17 10/06/2019
- Info:**
 - >info: ***** hspice job concluded
 - lic: Release hspice token(s)
 - lic: total license checkout elapsed time: 5.84(s)
 - cannot move input.nic to /home/UTSARR/nhf614/cadence/simulation/nor3.s

Figure 9: ADE Simulation Report for 3-NAND

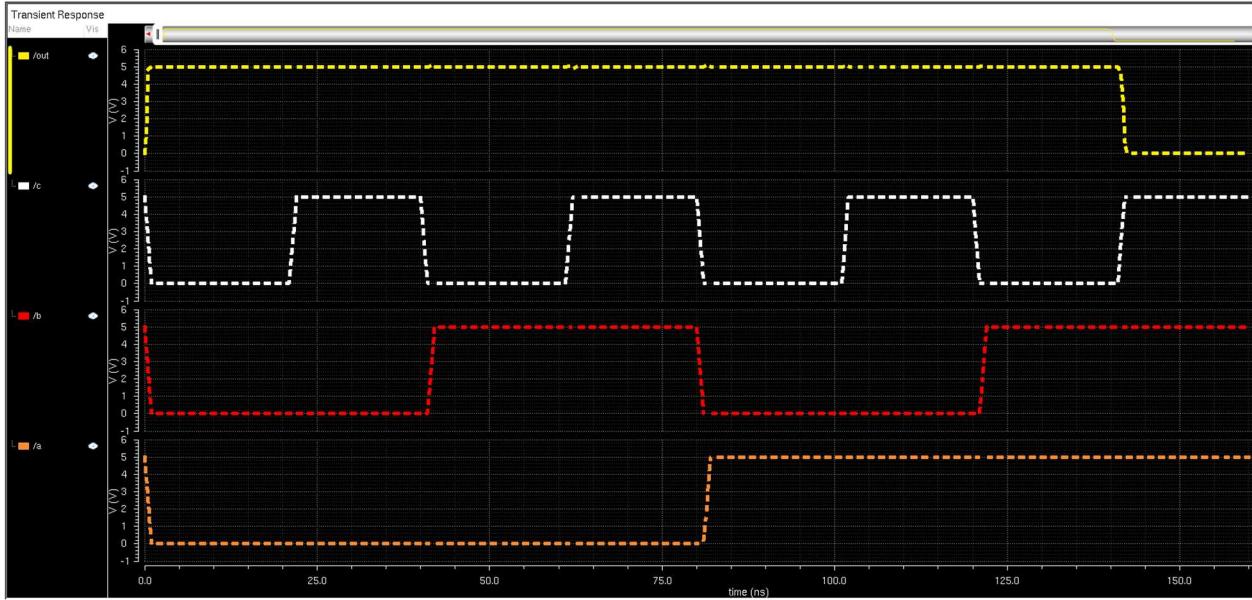


Figure 10: NAND-3 Simulation Results

Figure 9 on the left displays the simulation report for the NAND-3 cell. As expected, only 6 MOSFETs are used as shown in Figure 6—had the fingers and multipliers feature of Virtuoso been used, the result would have been the same. The last step is to simulate the NAND cell, and Figure 10 below verifies the desired operation of the design. To test the $2^3=8$ different input combinations available for a 3-Input NAND, the square waves are defined to have 20, 40, and 80 ns pulses for representing LSB (Least Significant Bit) to MSB (Most Significant Bit) respectively.

3-Input NOR

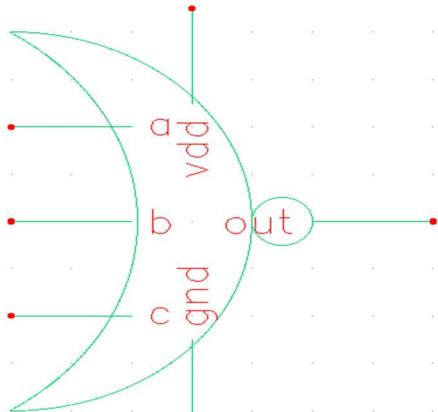


Figure 12: 3-Input NOR

Like the previous cells, the NOR design also follows a similar design process. Figure 12 shows the 3-Input NOR Cell designed in symbol form to setup the pin requirements for the CMOS layout. Next, the PUN (Pull-up-network) and PDN (Pull-down-network) are routed using both metal and poly as shown in Figure 11. The pins are also set— a, b, c as input signals, vdd and gnd as inputoutput signals, and out as output signal.

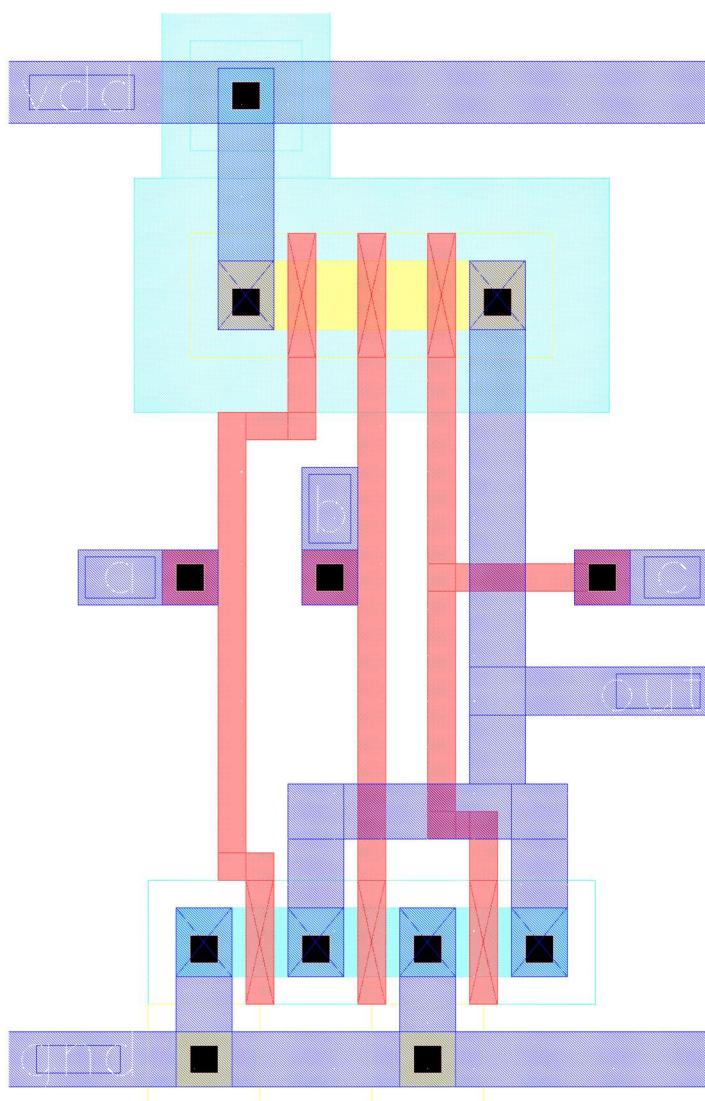


Figure 11: 3-Input NOR CMOS Cell

On the next page, a test circuit is built to simulate the 3-Input NOR gate. The report shows the use of 6 MOS transistors. The simulation waveforms are also displayed to verify the desired operation of the NOR cell.

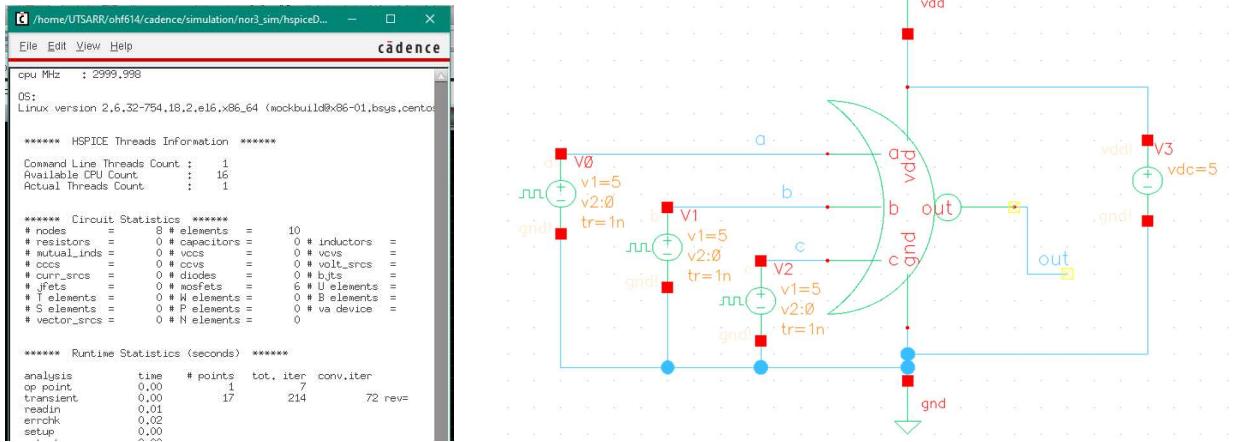


Figure 13: (LEFT) NOR-3 Sim Report, (RIGHT) Test Circuit

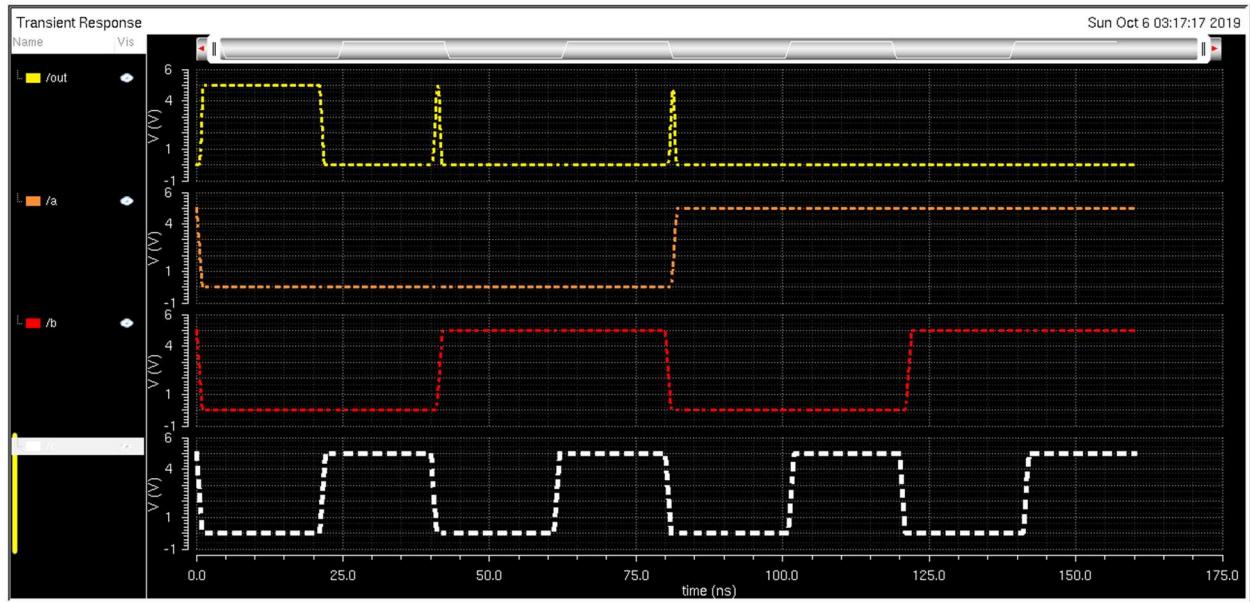


Figure 14: NOR-3 Simulation Results

2-Input AND

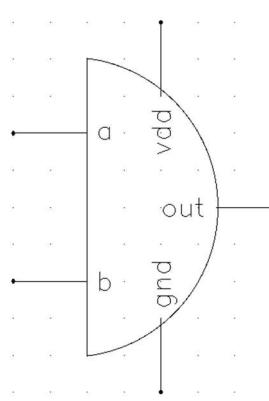


Figure 15: 2-AND Circuit Symbol

As the report progresses, so does too the complexity of each cell. This 2-Input AND is implemented as a 2-Input NAND with an Inverter; this is due to the logical implementation of Boolean Duals in the PUN and PDN's of a CMOS gate. Given the inverter cell layout has been designed and simulated, it is implemented below alongside the 2-Input NAND.

The cell is a good example as to why use uniform dimensions for power/ground rails and overall cell area: larger designs are easier to implement; The output of the 2-Input NAND is fed into the input of the Inverter to complete the design of the 2-Input AND. Overall, 6 MOSFETs are used as shown in Figure 17.

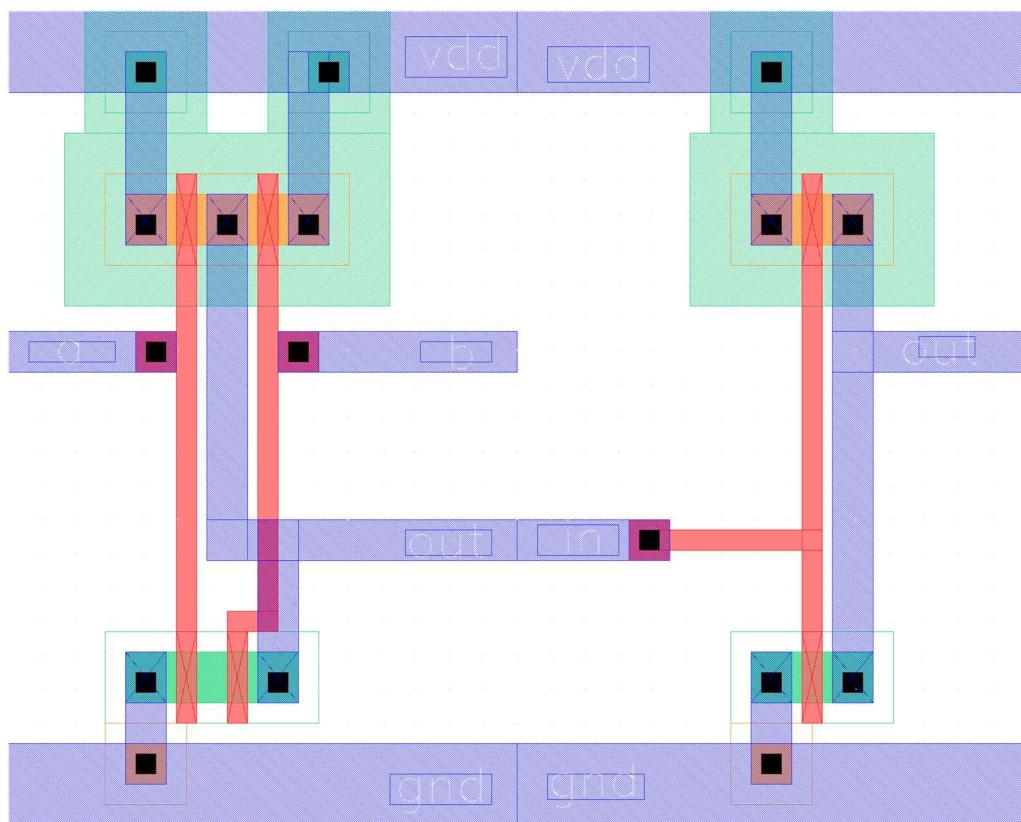


Figure 16: 2-Input AND

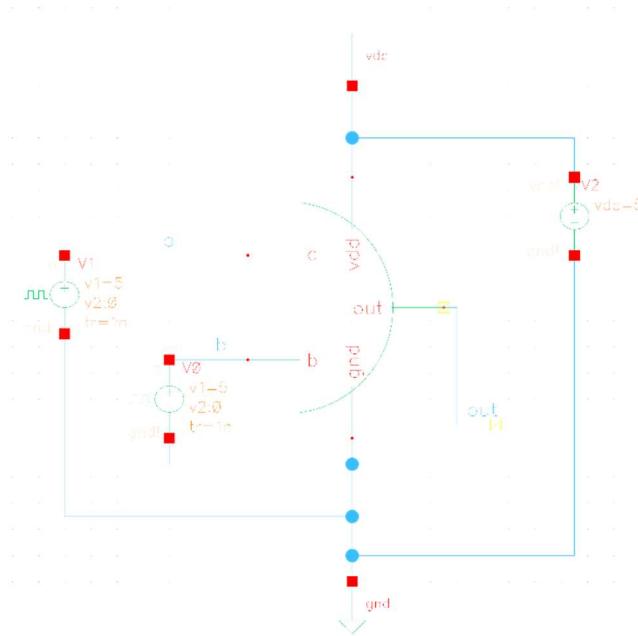


Figure 17: (LEFT) 2-Input AND Test Circuit, (RIGHT) Sim Report

Once again, the last step is to create a test circuit for the design. With two inputs, two square waves with pulse widths of 20ns and 40ns respectively are used to represent the MSB and LSB—given a little endian observation. Figure 17 displays the test circuit for the 2-Input AND and Figure 18 verifies the desired operation of the cell.

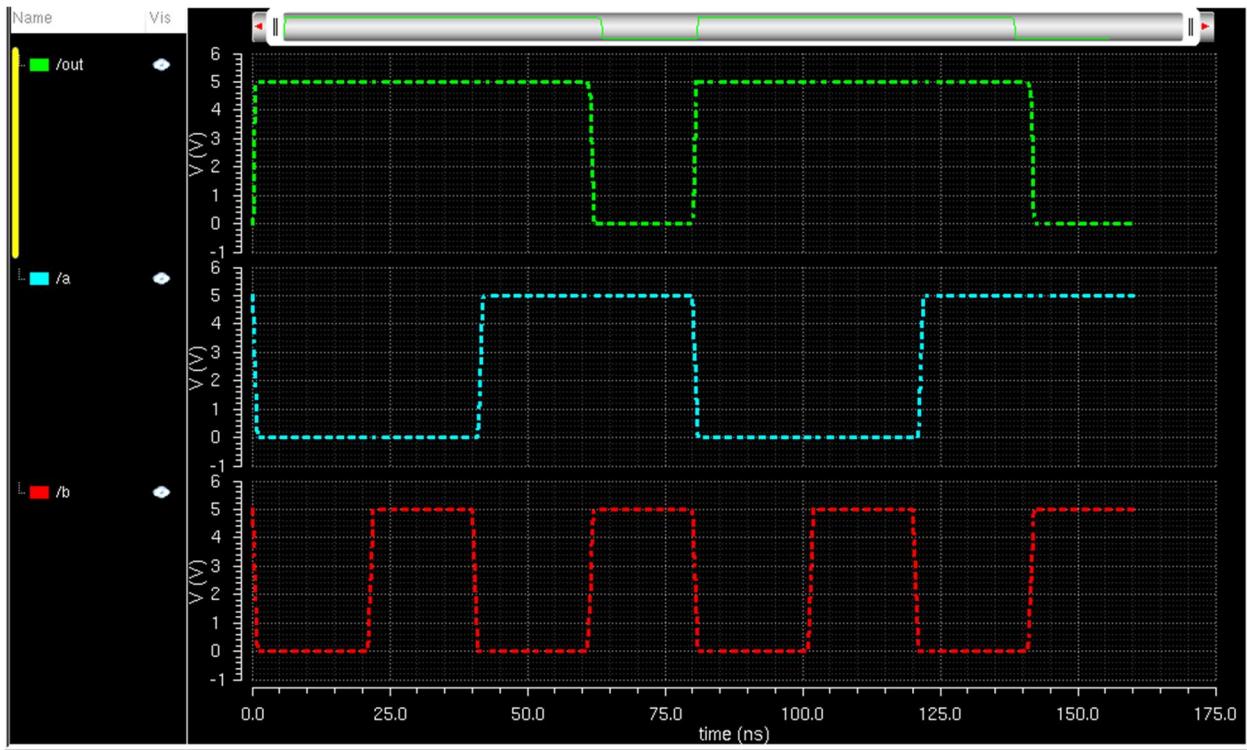


Figure 18: 2-Input AND Circuit Simulation

AND-INV Network Cell Design

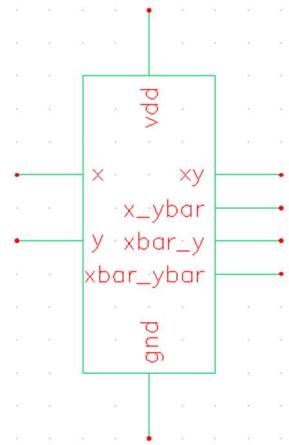


Figure 19: Network Circuit Symbol

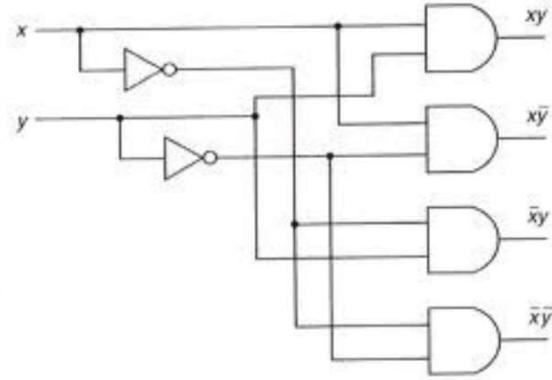


Figure 20: AND-INV Network

For simple implementation, the AND-INV network as shown in Figure 20 is drawn as a “black-box” circuit symbol in Figure 19. Each output of an AND gate is independently modeled, and the symbol can be thought of as a decoder with power/ground rails. For this design, 2 inverter cells and 4 2-AND cells are used, and the overall CMOS layout is presented in Figure 21 in compacted form to make note of the measurements of the layout: 24 micron x 175.2 micron.

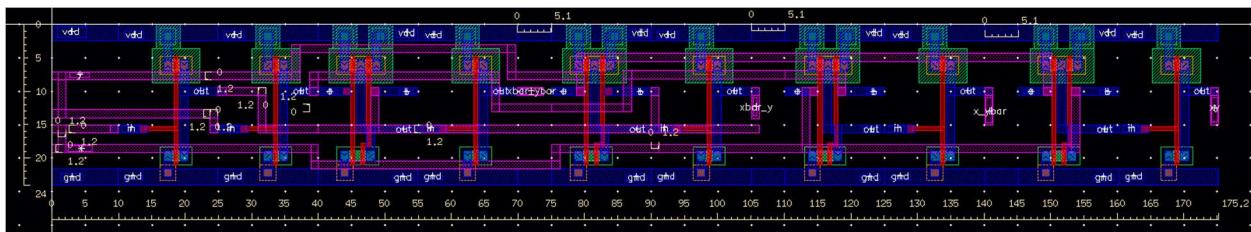


Figure 21: CMOS Layout of AND-INV Network

Now, for a detailed analysis, each cell of the network from left to right is examined briefly for the reader to take note of the design practices of the author. Noteworthy routing choices such as metal1 to metal2 and metal1 to poly are marked on each Figure. These are displayed on the next page, beginning with the Inverter cells in Figure 22. The table below describes the subdivision of the AND-INV cell with reference to the layout shown in Figure 21:

FIGURE #	WIDTH IN MICRON (X AXIS)	CELLS EXAMINED
22	From 0 to ~ 40	Both Inverters
23	40 to ~75	2-AND Cell for ($X'Y'$)
24	75 to ~110	2-AND Cell for ($X'Y$)
25	110 to ~145	2-AND Cell for (XY')
26	145 to 175.2	2-AND Cell for (XY)

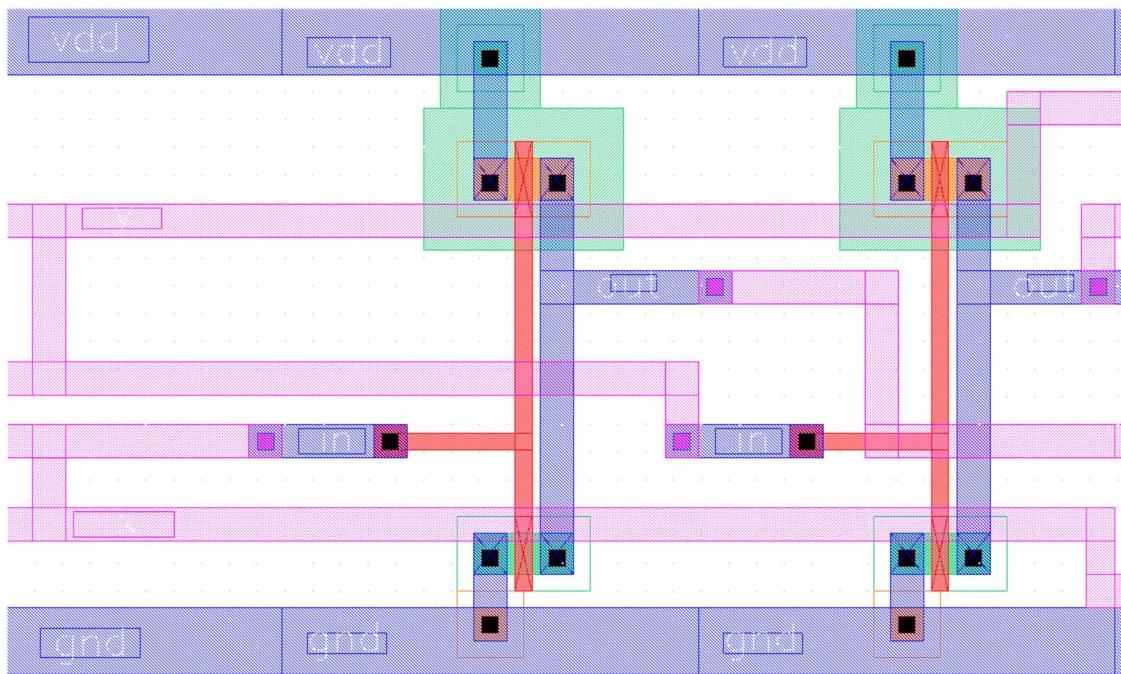


Figure 22: Inverter Cells and Input Pins

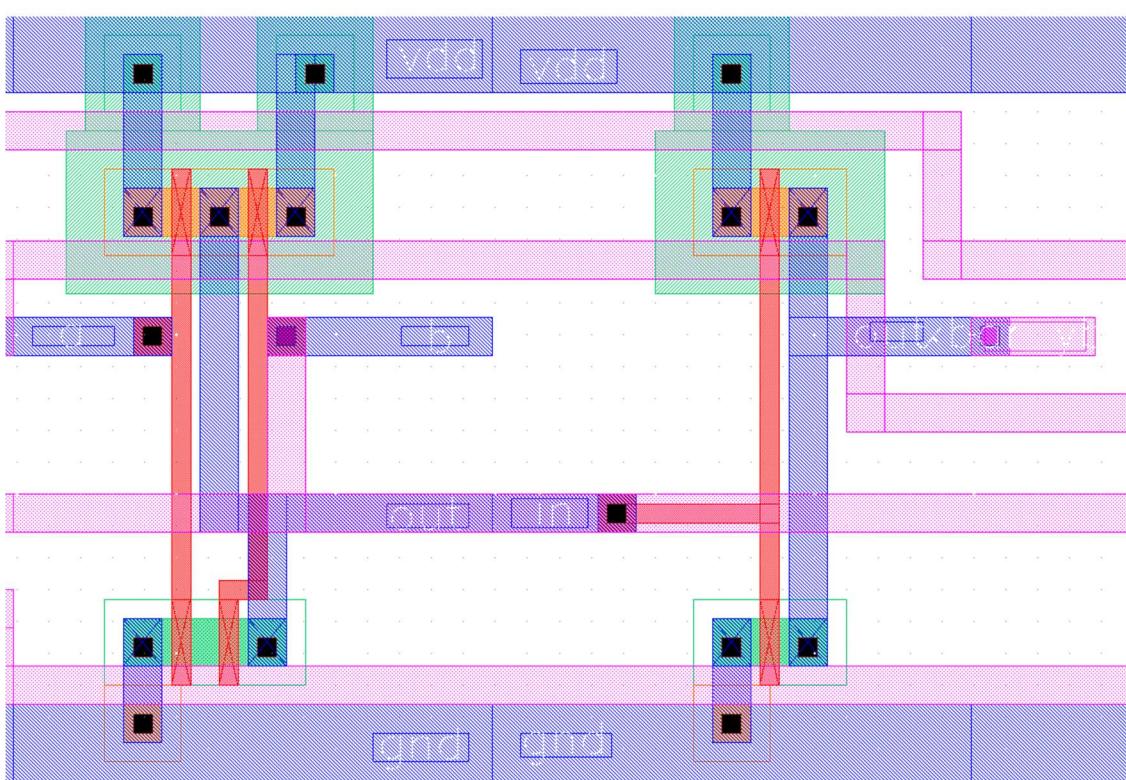


Figure 23: 2-AND Cell output for $X'Y'$

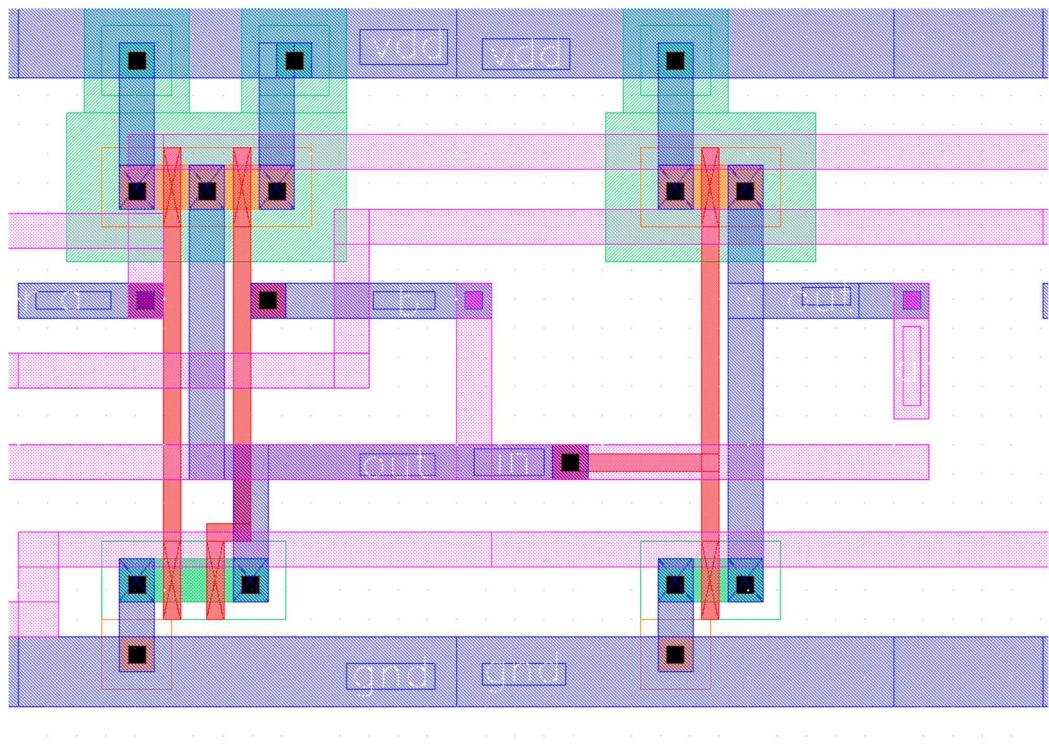


Figure 24: 2-AND Cell for output $X'Y$

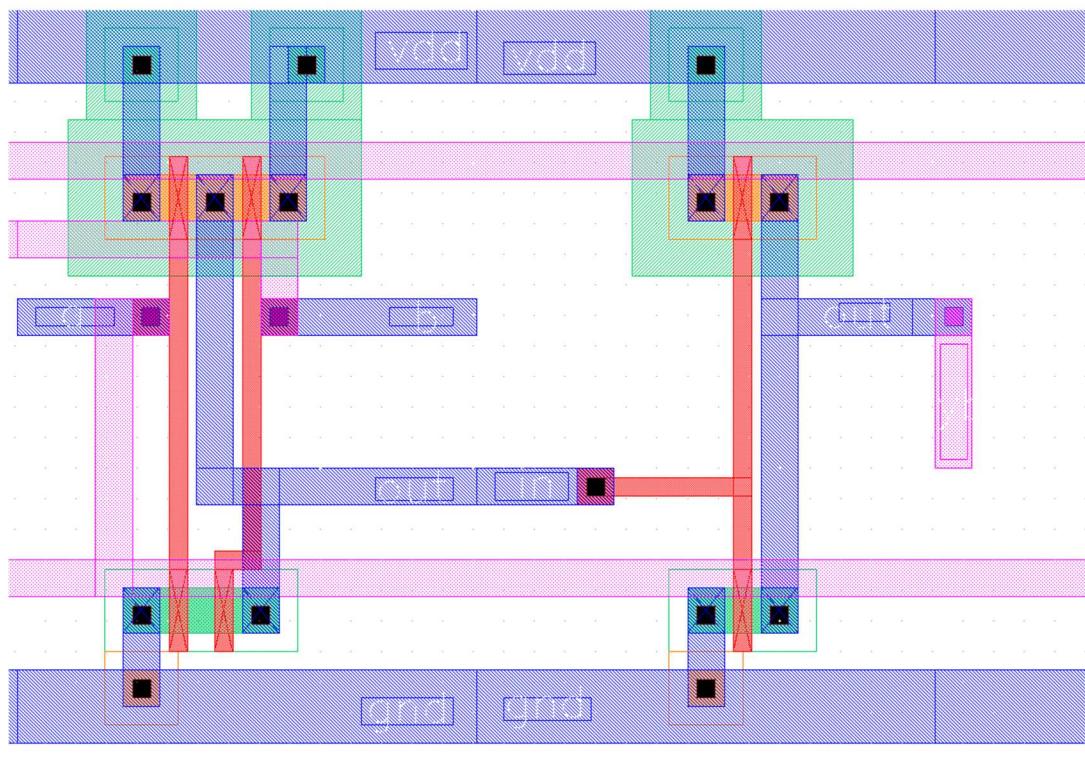


Figure 25: 2-AND Cell for Output XY'

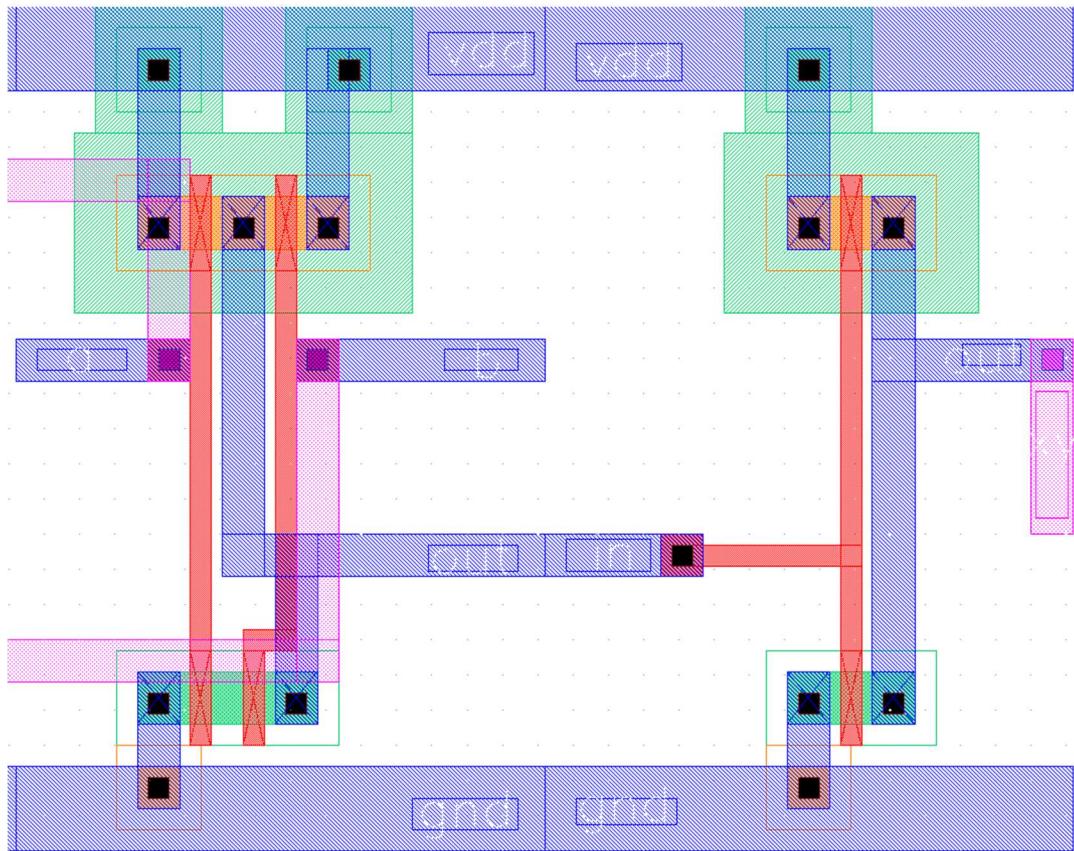


Figure 26: 2-AND Cell for Output XY

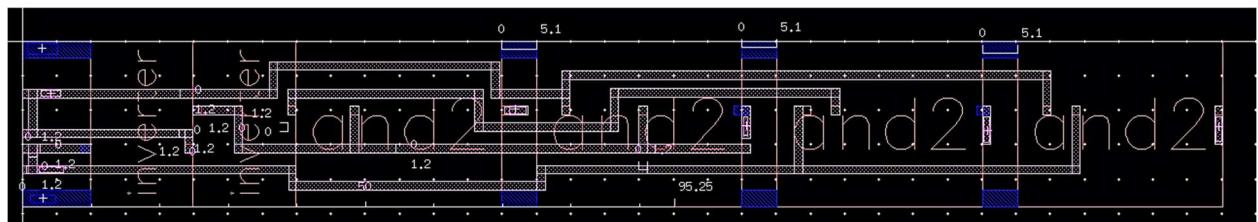


Figure 27: Cell-based abstracted AND-INV Network

After layout, the last step is to simulate the design. The test circuit for testing the “2-4 Decoder” is shown below in Figure 28. As mentioned in the Introduction section, this report entails of SSI—Small Scale Integration—designs, and the sub-100, 28 MOSFET count AND-INV network can attest to this designation. Finally, Figure 29 verifies the desired operation of the network.

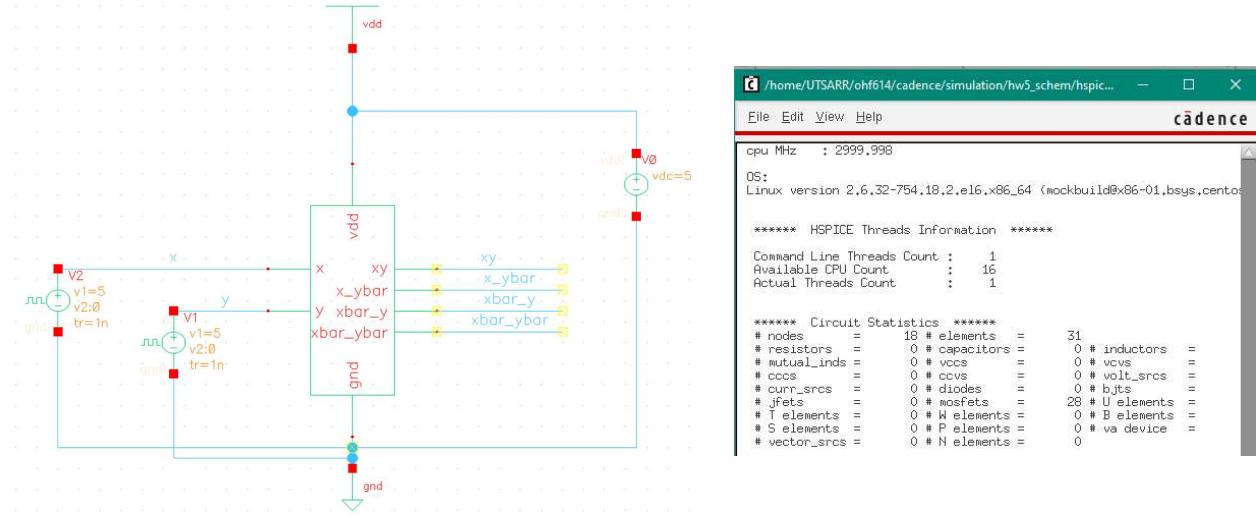


Figure 28: (LEFT) AND-INV Network Test Circuit, (RIGHT) HSPICE Simulation Report

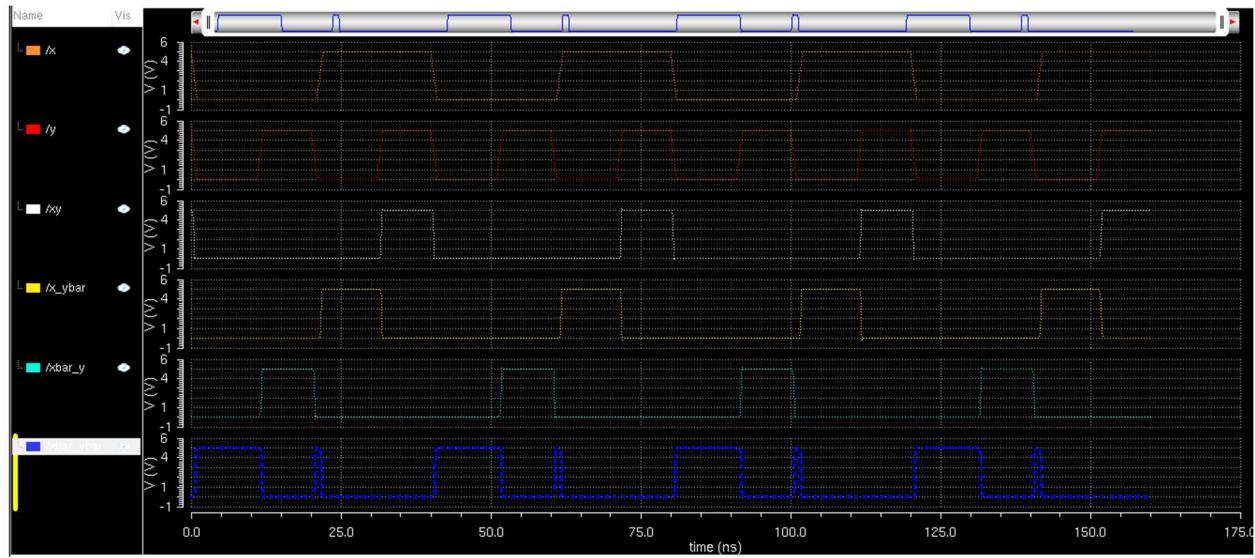


Figure 29: AND-INV Network Simulation Waveforms

Conclusion

As the first assignment using Cadence Virtuoso as part of the EE 4513 class, the designs for every cell proved to be difficult to implement—mainly due to the learning curve in learning the software; there are certain steps to create a design in all levels—symbol, layout, schematic—and with this also added to the overhead of completing the design. Certain technical requirements such as lambda conventions and keyboard controls made it difficult to conceptualize designs. Further, at times I lost all my work due to server issues (the Cadence Virtuoso environment is served over ssh) but this allowed me to reinforce CAD techniques. Above all, I learned to solidify 3 weeks of VLSI lectures in 15 hours of dedicated time to Cadence Virtuoso, and I am excited to complete the next assignment.

Appendix: Cadence Virtuoso Lessons Learned

FIXING WELL SPACING @ 5.40 MICRON

***** Summary of rule violations for cell "nand3_symbol layout" *****

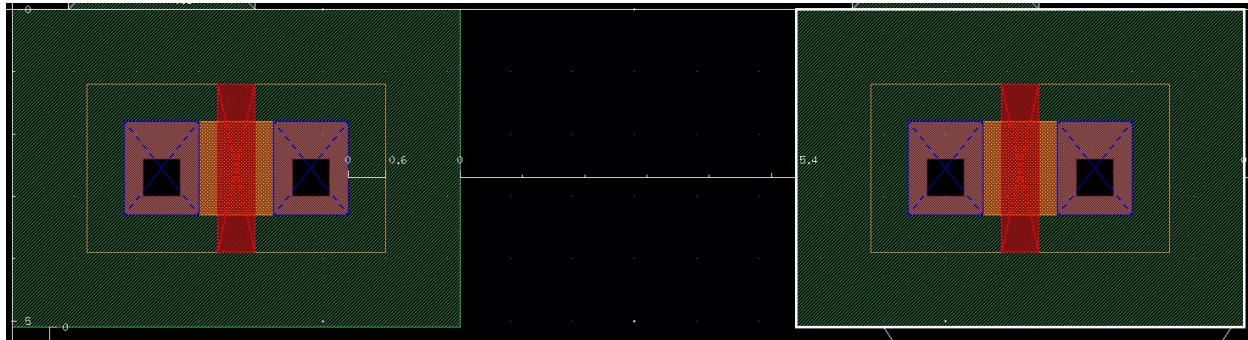
errors Violated Rules

3 (SCMOS_SUBM Rule 1.1) well width: 3.60 um

3 (SCMOS_SUBM Rule 1.2) well spacing, different potential: 5.40 um

6 (SCMOS_SUBM Rule 2.3) source/drain active to well edge: 1.80 um

12 Total errors found



N WELL SPACING = 18 LAMBDA = 5.4 MICRON

FIXING SOURCE DRAIN ACTIVE TO WELL EDGE @ 1.80 MICRON

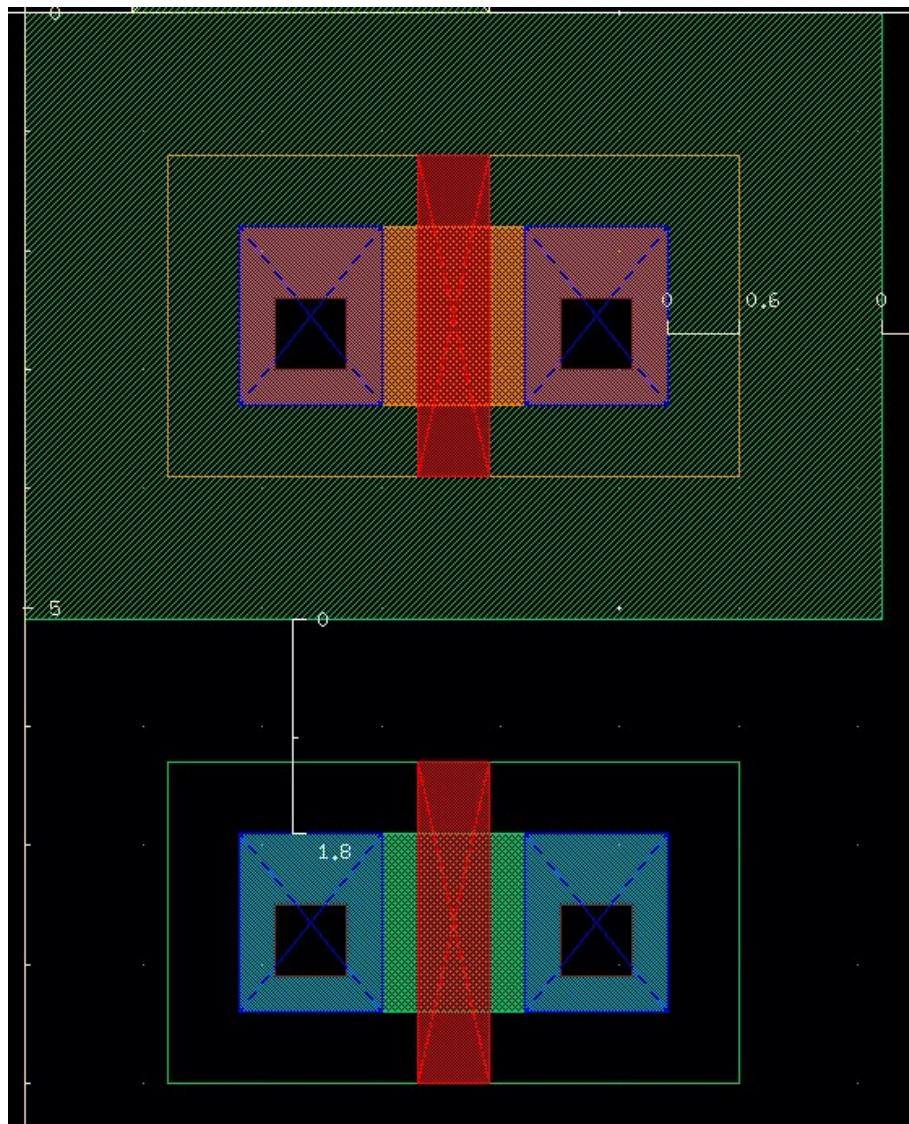
***** Summary of rule violations for cell "nand3_symbol layout" *****

errors Violated Rules

3 (SCMOS_SUBM Rule 1.1) well width: 3.60 um

6 (SCMOS_SUBM Rule 2.3) source/drain active to well edge: 1.80 um

9 Total errors found



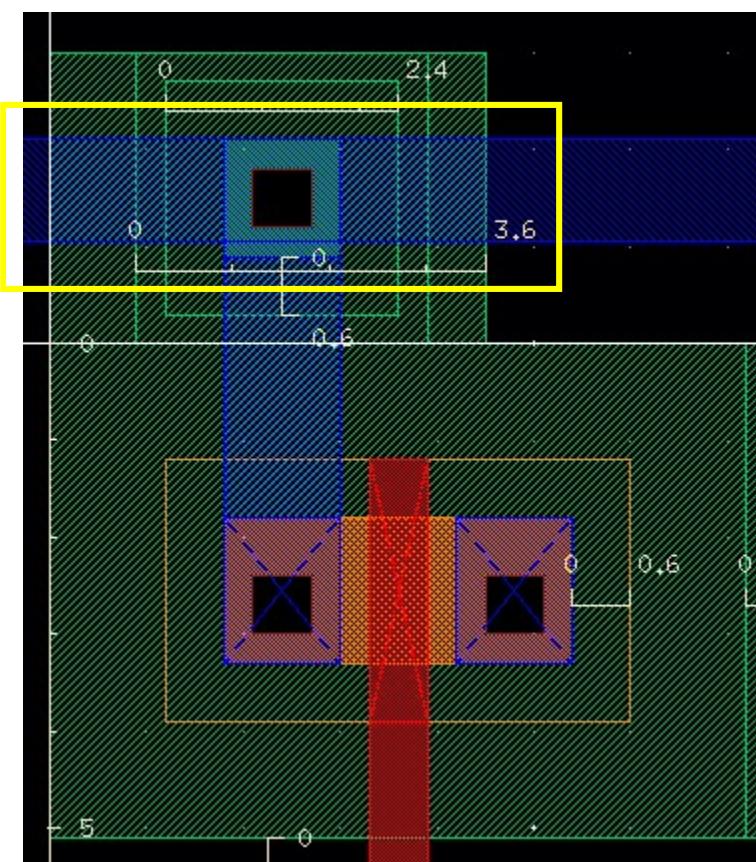
FIXING WELL WIDTH 3.60 MICRON

***** Summary of rule violations for cell "nand3_symbol layout" *****

errors Violated Rules

3 (SCMOS_SUBM Rule 1.1) well width: 3.60 um

3 Total errors found



FIXING ACTIVE CONTACT 0.9 MICRON

***** Summary of rule violations for cell "nand3_symbol layout" *****

errors Violated Rules

2 (SCMOS_SUBM Rule 1.1) well width: 3.60 um

2 (SCMOS_SUBM Rule 6.3) active contact spacing: 0.90 um

4 Total errors found

