Commodore A4091

Rev B Advanced SCSI II Controller Board

This Zorro III board was originally designed and sold by Commodore, which did a single run of the Rev A design before shelving it. Commodore was running out of money at the time and didn't want to risk a second production run. The Rev B design was given to DKB Software for production, marketing, sales, distribution, and support.

Features:

- Boot ROM
- NCR 53C710 SCSI II controller
- 50 pin internal connector
- 50 pin external SCSI2 connector
- 3.5" hard drive mounts on the card
- Active SCSI termination
- Zorro III bus support

Caveats:

- Requires Buster 11
- Does not work with with A3640 Rev 3.0
- No RAM option
- No wide SCSI support

The Commodore A4091 was reverse-engineered by Stefan Reinauer and Chris Hooper.

ReA4091 Rev 4 2023-04-22

Commodore		DATE	Schematic
Design By:	Dave Haynie	1993	A4091
Reverse By:	SR	2021-11-09	Overview
Capture By:	CDH	2021-11-19	365120 REV: B4

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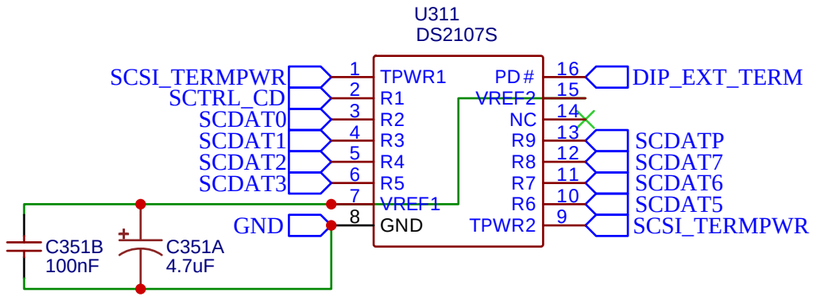
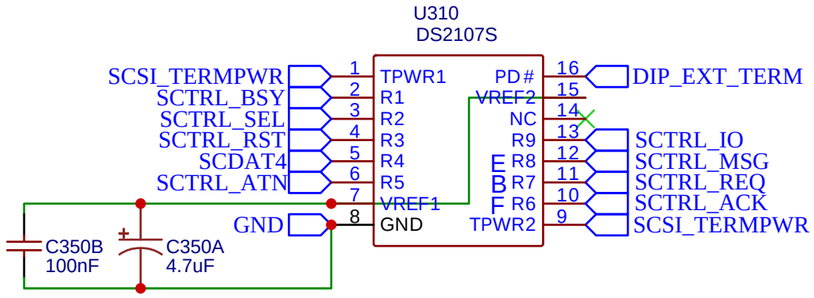
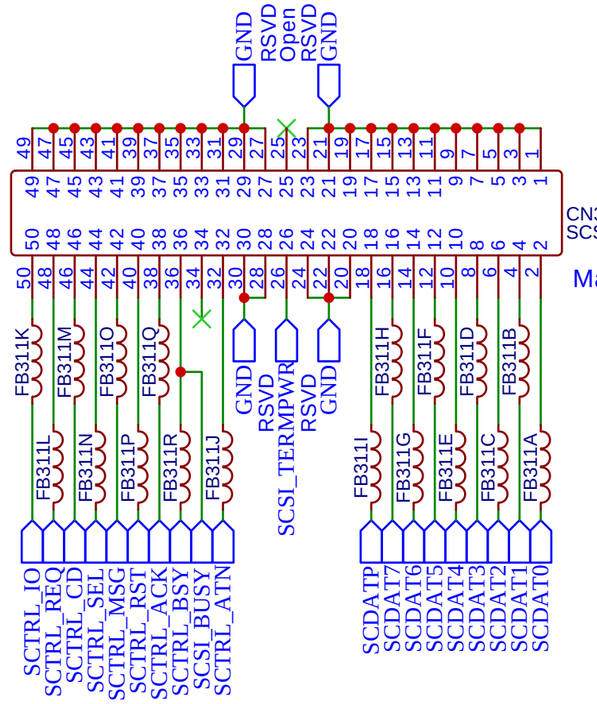
Active Termination

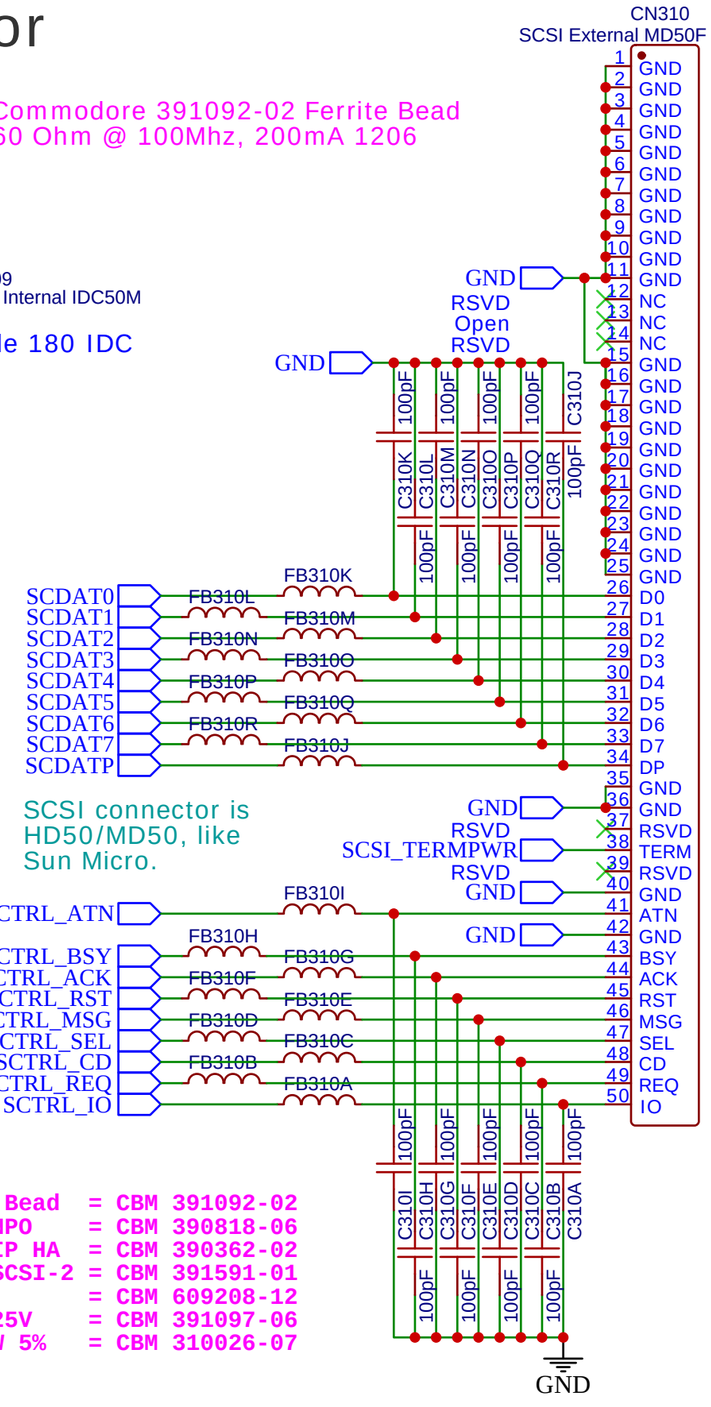




Internal 2x25 Connector

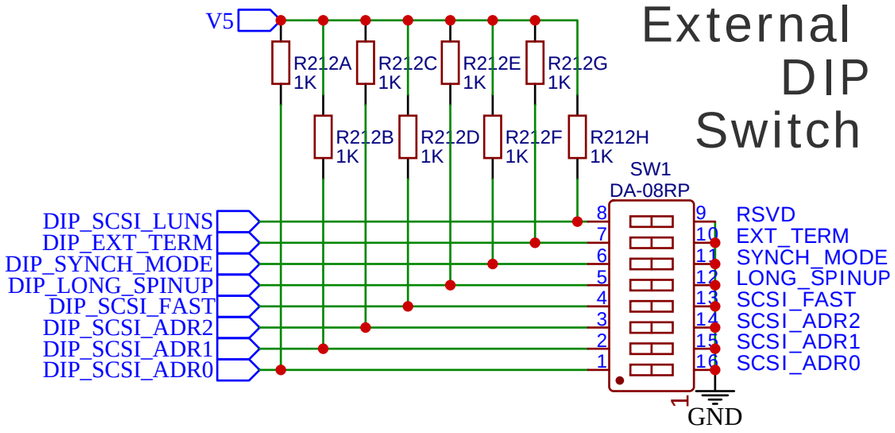


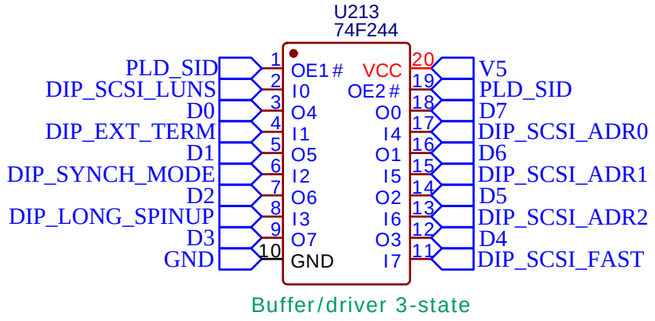
Commodore 391092-02 Ferrite Bead
60 Ohm @ 100Mhz, 200mA 1206



SCSI connector is
HD50/MD50, like
Sun Micro.

External DIP Switch

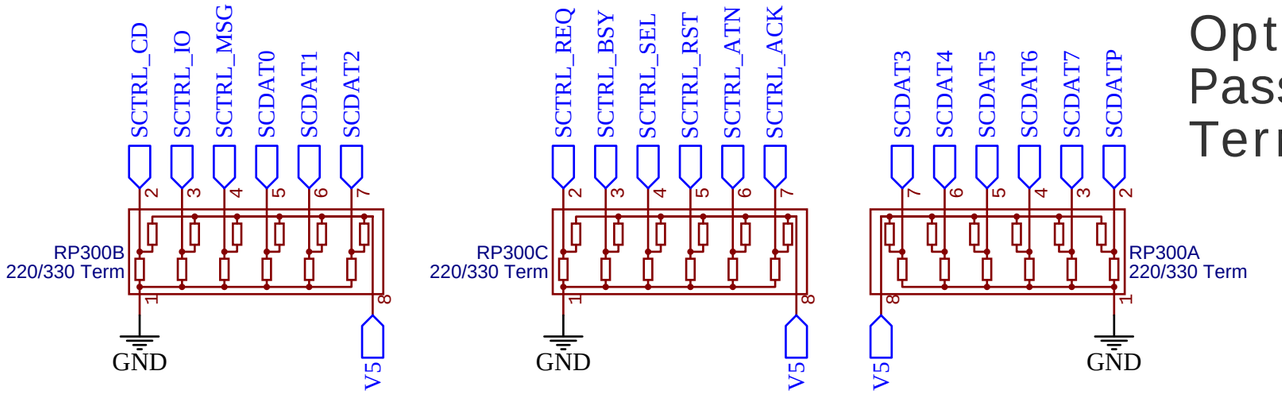




Buffer/driver 3-state

SCSI F.Bead = CBM 391092-02
100pF NPO = CBM 390818-06
SW1 8DIP HA = CBM 390362-02
HD50F SCSI-2 = CBM 391591-01
74F244 = CBM 609208-12
4.7uF 25V = CBM 391097-06
1K 1/8W 5% = CBM 310026-07

Optional Passive Termination



External HD50 Connector

Commodore		DATE	Schematic A4091 SCSI
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B4

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SCSI-2 Controller

32KB/64KB EPROM

U206
27c256

U300
NCR53C710

U301
Abracon 50MHz AC0 D.9403

U302
74F74

CN351
TO-LED

CN308
TO-MB

J100
ESIZE

R398
120

C300I 100nF
C300H 10nF
C300A 100nF
C300B 10nF
C300C 100nF
C300G 100nF
C300E 100nF
C301A 10nF
C302A 100nF
10nF C300D
10nF C300F

R300J 1K
R300I 1K
R300L 1K
R300K 1K
R300P 1K
R300G 1K
R307A 1K
R300A 1K
R307B 1K
R300B 1K
R300E 1K
R300H 1K
R300D 1K
R300C 1K
R300F 1K
R300O 1K
R300N 1K
R300M 1K
R301A 22
R302B 22
R302A 22

FB503
FB506
FB502

74F74 = CBM 391320-01
53C710 = CBM 391593-01

Commodore		DATE	Schematic A4091 NCR53C510
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B4

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PLD Symbols

The GAL/PAL devices on page 5 are programmed with gate configurations which consolidate what would be a large number of discrete components. Original Commodore source program files for the A4091 GAL components can be found on the Internet. The below can be used as a quick reference for symbols used in those programming files.

A0 - SCSI sizing address
A1 - SCSI sizing address _or_ A1/Lock signal
A2 - Address A2
A3 - Address A3
A4 - Address A4
A5 - Address A5
A6 - Address A6
A8 - Address A8 (known as A1 in U202)
A17 - Address A17
A18 - Address A18
A19 - Address A19
A23 - Address A23
!ABOEL - Low order address transfer enable
!ABOEH - High order address transfer enable
!AS - SCSI address strobe
!ASQ - Clocked/qualified version of SCSI AS*

BA2 - SCSI burst address
BA3 - SCSI burst address
!BDTACK - Z3 data acknowledge, buffered
!BERR - Z3 Bus error
BFCS - 1:Buffered cycle strobe
BFCS - 2:A4091 local Z3 cycle strobe
BLOCKBG - after 1st SBG block till end
BMASTER - Buffered/inverted version of MASTER
C7M - Z3 arbiter clock
!CBACK - SCSI burst acknowledge
!CBREQ - SCSI burst request
!CFGIN - Configuration chain input
!CFGOUT - Configuration chain output
CFGLT - Configuration address latch (on 0->1)
!CINH - Z3 cache inhibit
CLK - 1:25MHz NCR 53C710 bus clock
!CLK - 2:25MHz system clock
!CYCZ3 - On-bus Z3 cycle (internal)

!D2Z - Data is transfered to Z3 bus
DBLT - Data is latched
!DCNT - State bit for Z3 stuff (internal)
DMASTER - Master delayed
!DBOE - Data transfer enable
DOE - Z3 Data phase (data output enable)
!DS0 - Z3 low order data strobe
!DS1 - Z3 data strobe
!DS2 - Z3 data strobe
!DS3 - Z3 high order data strobe
!DTACK - Z3 termination cycle
!DTSYNC - Synchronizer for DTACK->STERM (internal)
!DS - SCSI data strobe
!EBG - Expansion bus grant
!EBR - Z3 bus request
!EDTACK - Z3 data acknowledge, on bus
!EFCS - Z3 cycle strobe for DMA

FC0 - CPU read/write function code
FC1 - CPU read/write function code
FC2 - CPU read/write function code
FCS - Z3 full cycle strobe
!INT - We generated an interrupt
!INT2 - Zorro bus interrupt 2
!INTASS - A vector has been assigned
!INTPOLL - An interrupt polling phase is signaled
INTREC - Interrupt register access
!INTSERV - We're servicing this interrupt phase
!INTSPC - Partially qualified interrupt space (decode)
!INTVEC - An interrupt vector phase is signaled

!MASTER - SCSI chip owns the A4091 bus
!MATCH - Address comparator match
!MTACK - Z3 slave burst strobe
!MTCR - Z3 multiple transfer burst cycle strobe
!MYBUS - The A4091 has the bus
!NACK - Data acknowledge
!NOZ3 - 1:Get off the Z3 bus (stop driving)
!NS0 - ROM access counter (internal)
!NS1 - ROM access counter (internal)
!NS2 - ROM access counter (internal)
!NS3 - ROM access counter (internal)

READ - Z3 read strobe (signal/cycle)
!REGED - A4091 is registered as Z3 master
RCHNG - Registration is changing (internal)
!ROM - System ROM access
!RST - System reset
!SBG - SCSI bus grant
!SBR - SCSI bus request
!SCSI - SCSI chip register address (see SREG)
!SHUNT - Z2 configuration shunt (0=Z2 1=Z3)
!SID - SCSI ID jumper access
SIZ0 - SCSI transfer size
SIZ1 - SCSI transfer size
!SINT - SCSI interrupt
!SLACK - NCR 53C710 slave acknowledge
!SLAVE - Z3 slave select for interrupt cycles
!SLAVEOE - Slave output enable
SMASTER - Synched master for fall edge
!SREG - SCSI chip register select (gated by clock)
SSBR - Synched SCSI bus request
!Z2D - Data is transfered from Z3 bus
!SSYNC - SCSI address synchronizer (internal)
!STERM - SCSI termination

Commodore		DATE	Schematic
Design By:	Dave Haynie	1993	A4091
Reverse By:	SR	2021-11-09	PLDs
Capture By:	CDH	2021-11-19	365120 REV: B4

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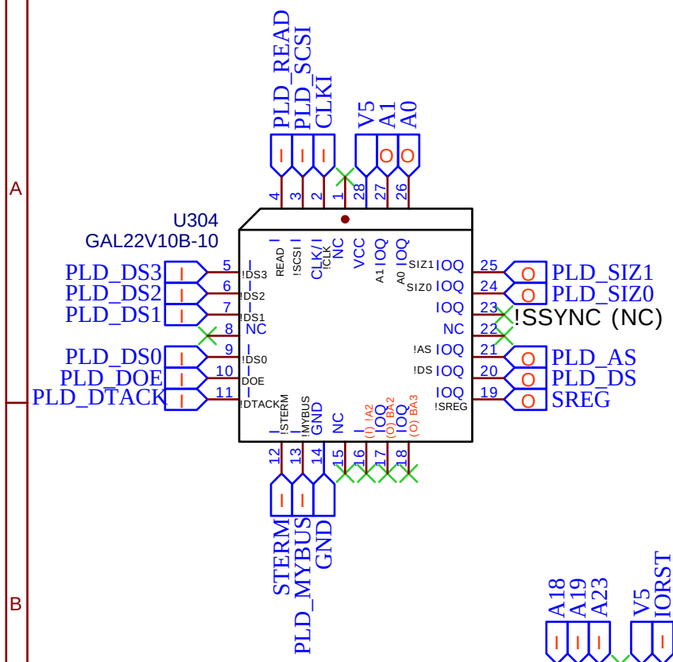
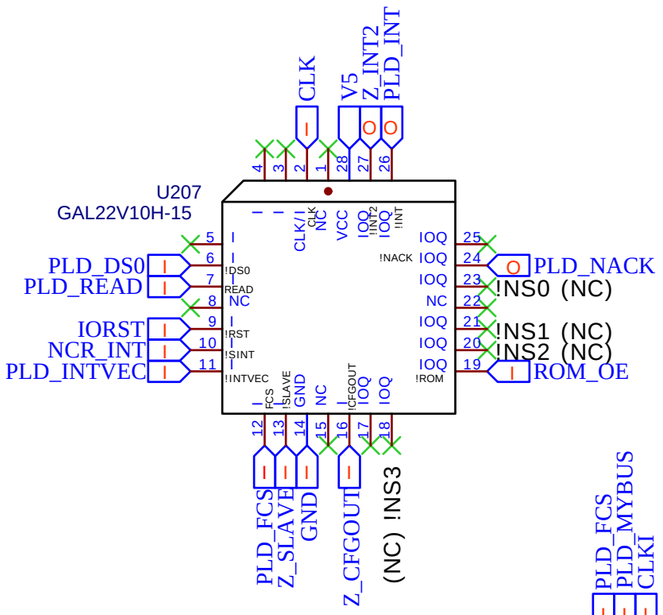
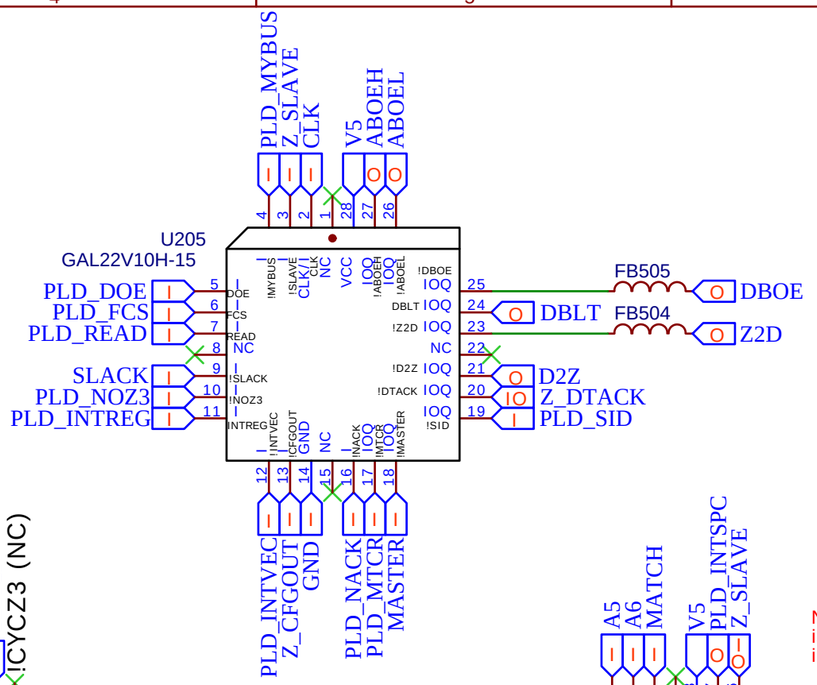
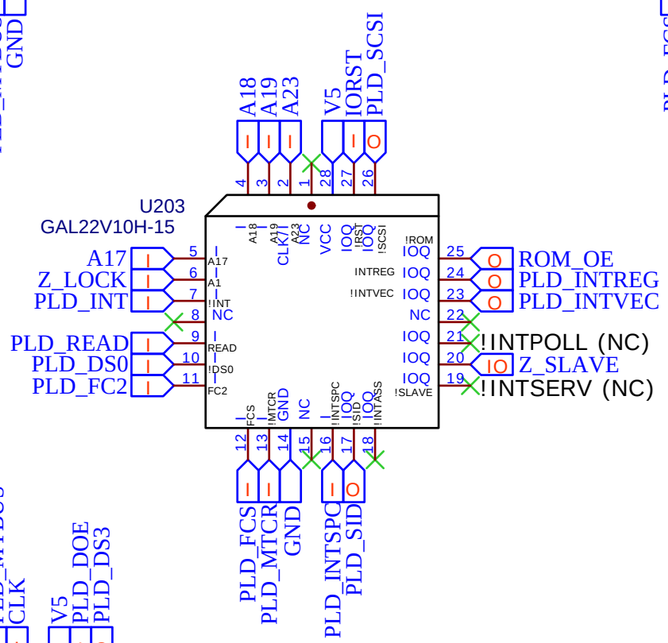
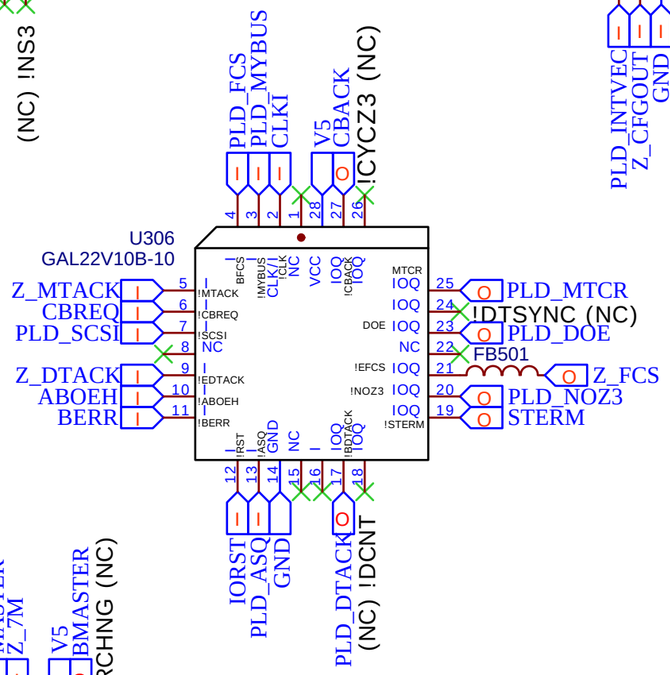
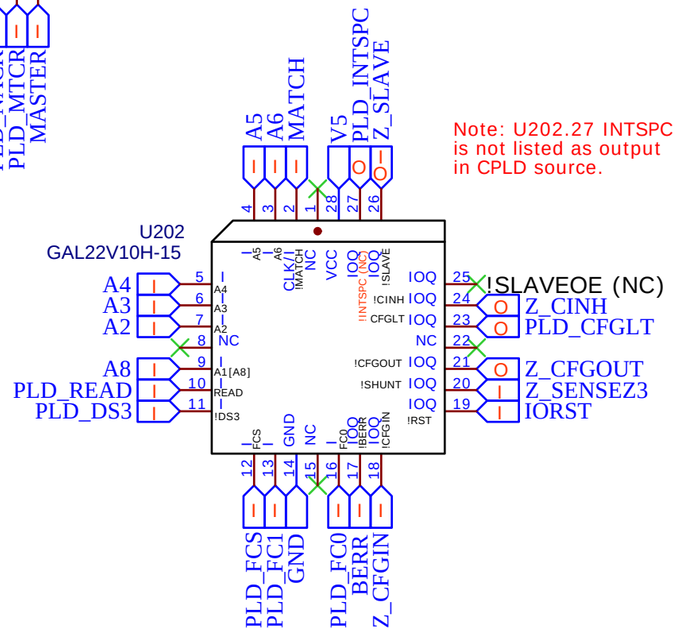




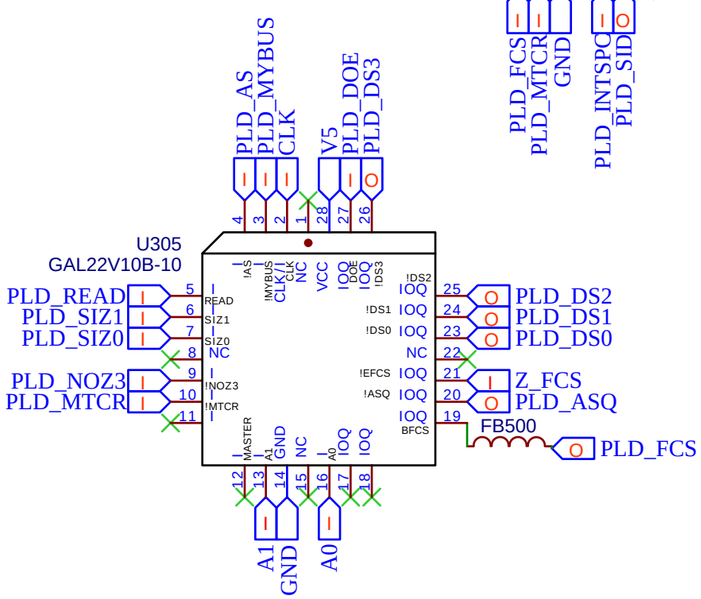


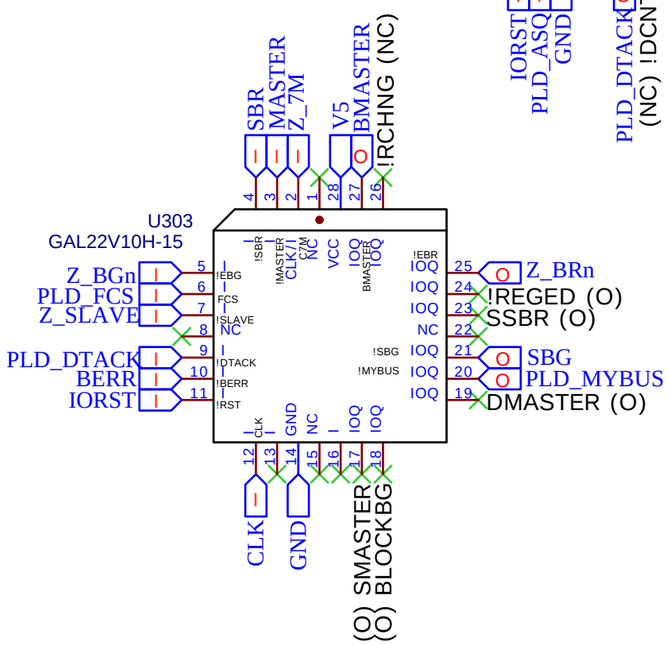






Note: U202.27 INTSPC is not listed as output in CPLD source.





From PLD equations

NC = Used Internally
I = Input
O = Output
IO = Bidirectional

Commodore		DATE	Schematic A4091 PLDs
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B4

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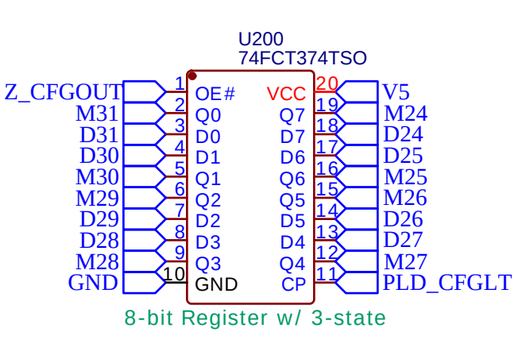
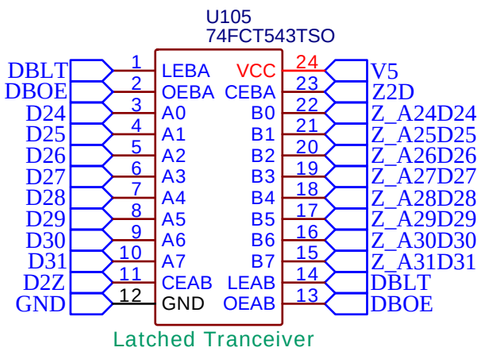
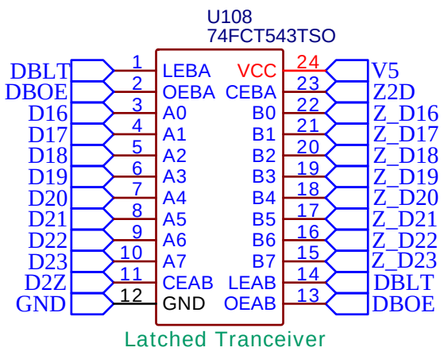
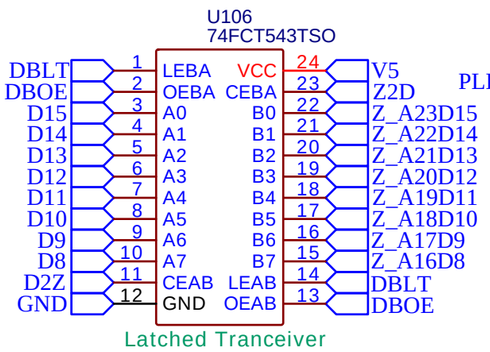
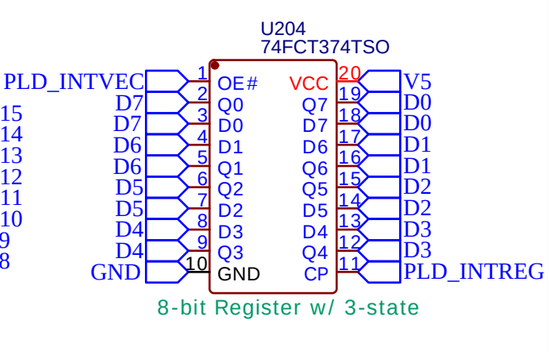
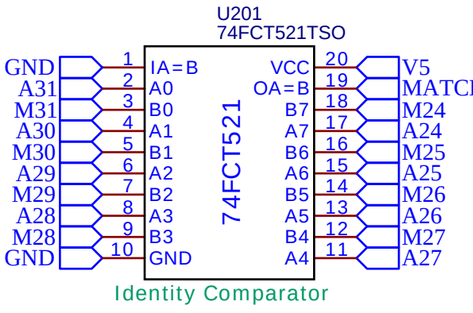


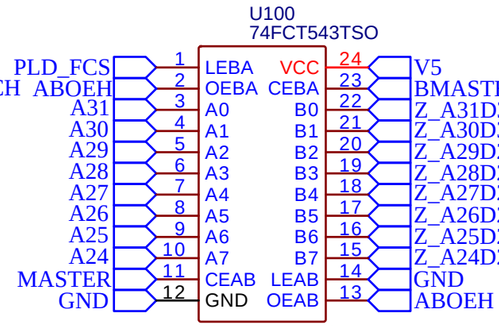


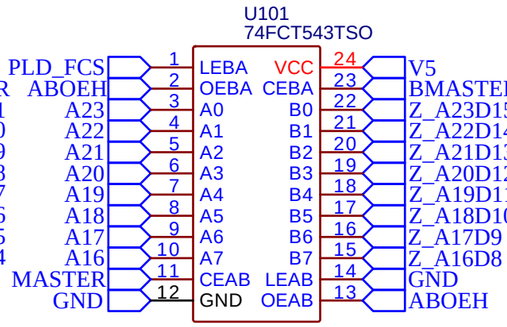


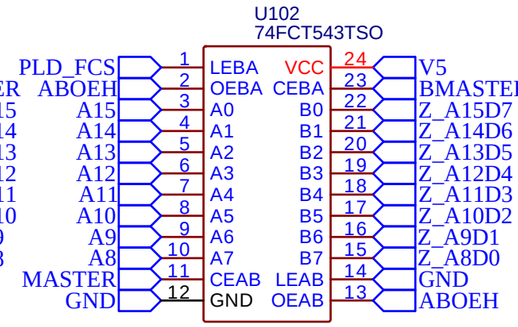


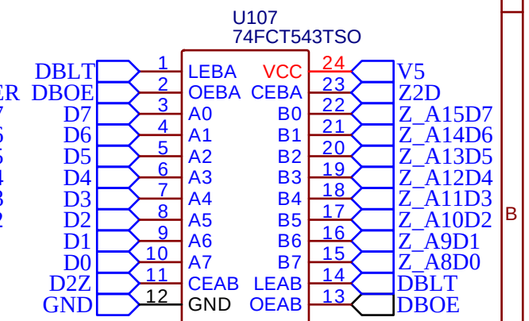


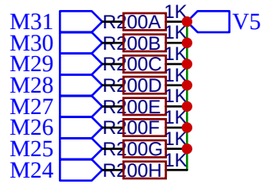


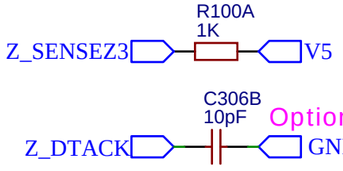




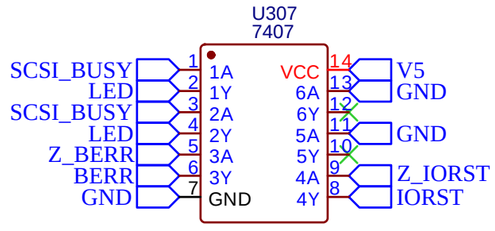


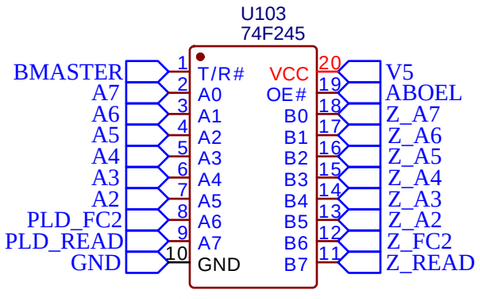


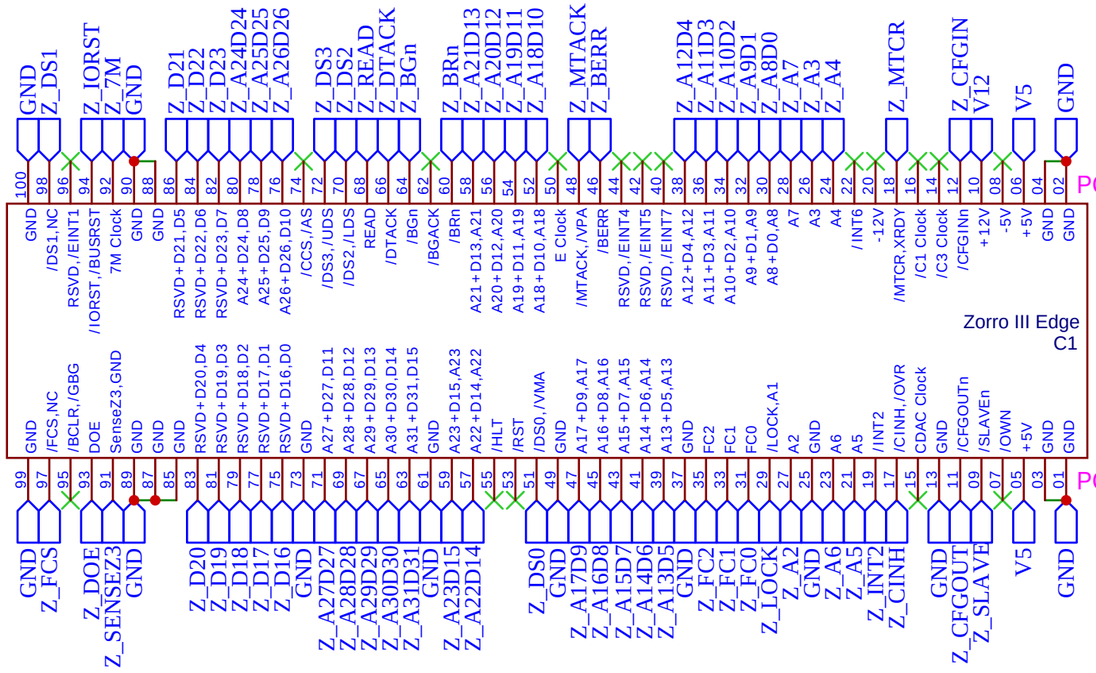


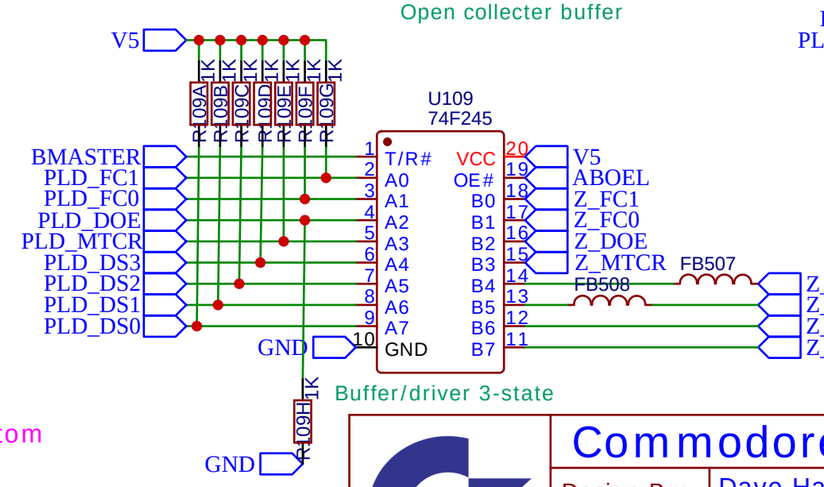


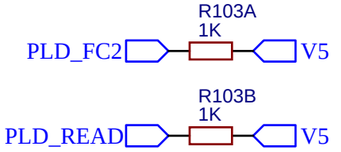
7407 = CBM 391188-01
74F245 = CBM 391375-01
74FCT374 = CBM 390784-02
74FCT543 = CBM 391487-01











Commodore		DATE	Schematic A4091 Zorro
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B4
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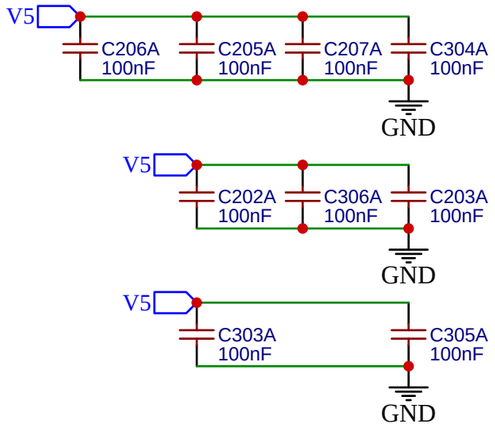
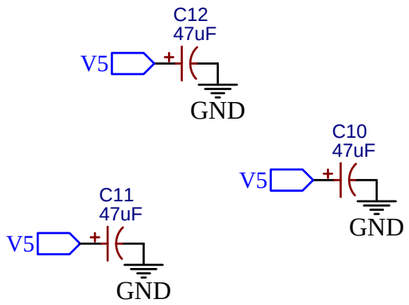
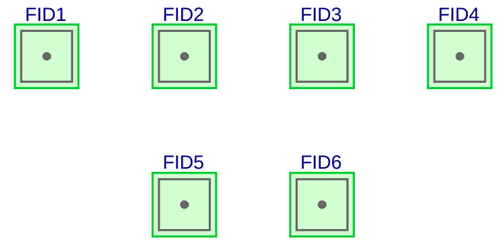
PLD bypass caps



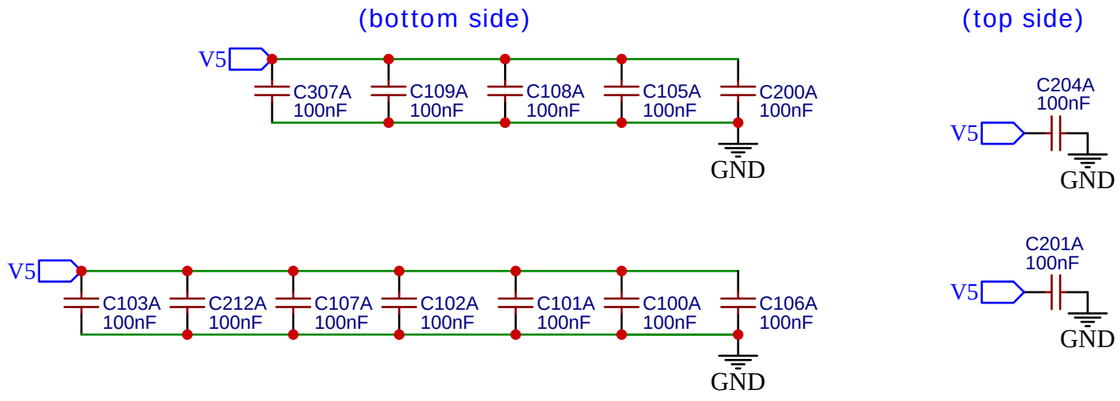
Bulk power



Assembly fiducials



Discrete IC bypass caps



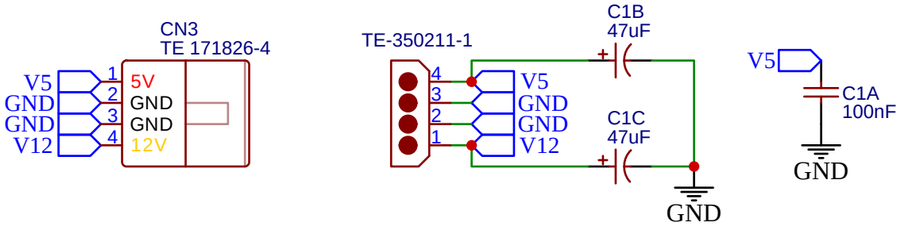
Fan Option

Note: connector has non-standard pin numbering.

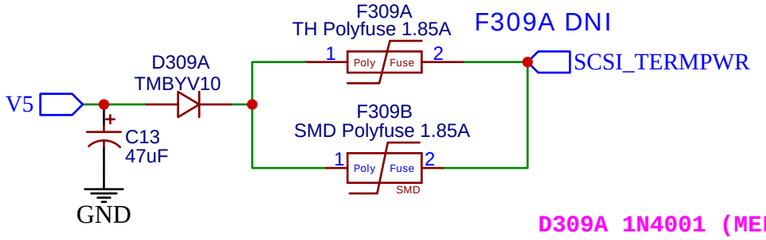
Mechanical holes

Berg Drive Power

MOLEX Drive Power



SCSI termination power



D309A 1N4001 (MELF) = CBM 391327-01

Commodore		DATE	Schematic A4091 Power
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B4
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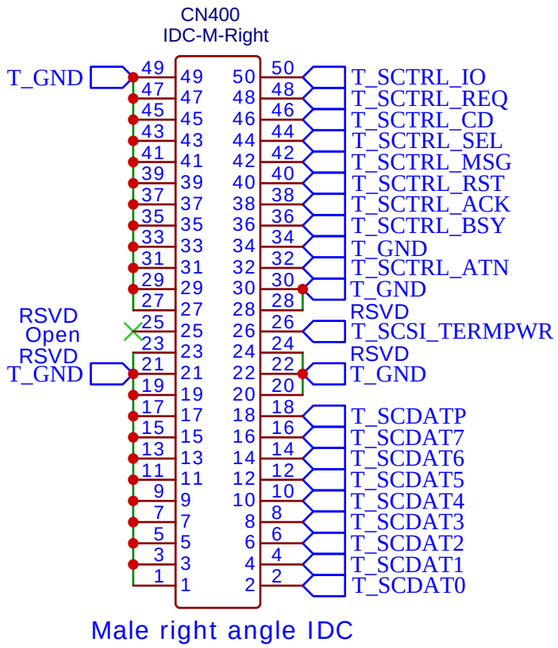
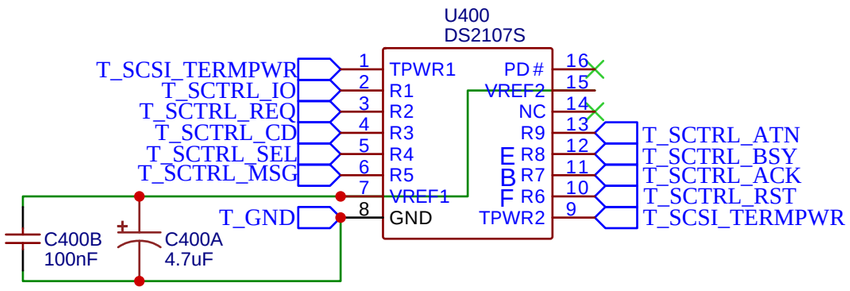
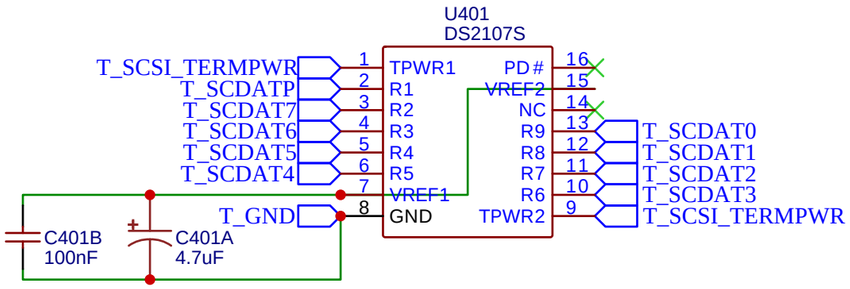
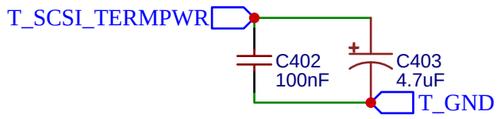
SCSI Active Terminator cut-out board



Male right angle IDC

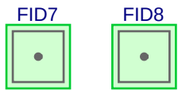






Board Holes

Fiducials



Commodore		DATE	Schematic A4091 SCSI Terminator
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B4

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Sheet: 8 of 8