Commodore A4091

Rev B Advanced SCSI II Controller Board

This Zorro III board was originally designed and sold by Commodore, which did a single run of the Rev A design before shelving it. Commodore was running out of money at the time and didn't want to risk a second production run. The Rev B design was given to DKB Software for production, marketing, sales, distribution, and support.

Features:

- Boot ROM
- NCR 53C710 SCSI II controller
- 50 pin internal connector
- 50 pin external SCSI2 connector
- 3.5" hard drive mounts on the card
- Active SCSI termination
- Zorro III bus support

Caveats:

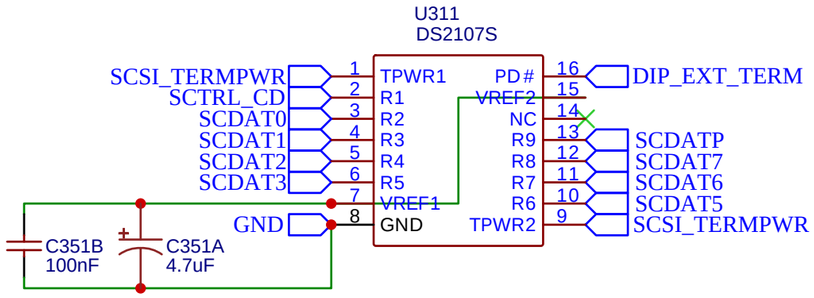
- Requires Buster 11
- Does not work with with A3640 Rev 3.0
- No RAM option
- No wide SCSI support

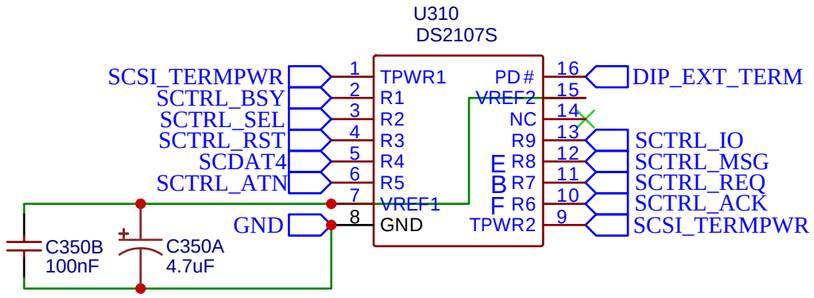
The Commodore A4091 was reverse-engineered by Stefan Reinauer and Chris Hooper.

ReA4091 Rev 3 2022-06-20

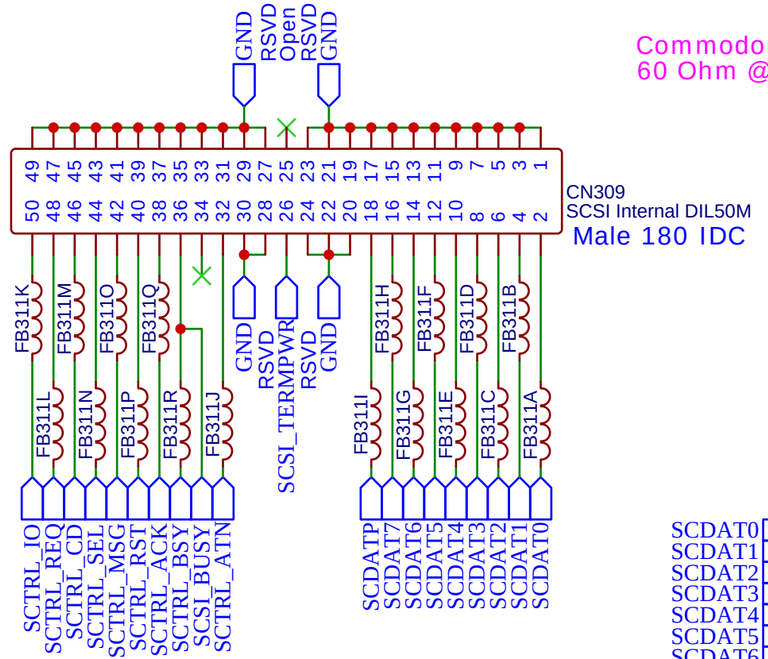
Commodore		DATE	Schematic
Design By:	Dave Haynie	1993	A4091
Reverse By:	SR	2021-11-09	Overview
Capture By:	CDH	2021-11-19	365120 REV: B3

Active Termination

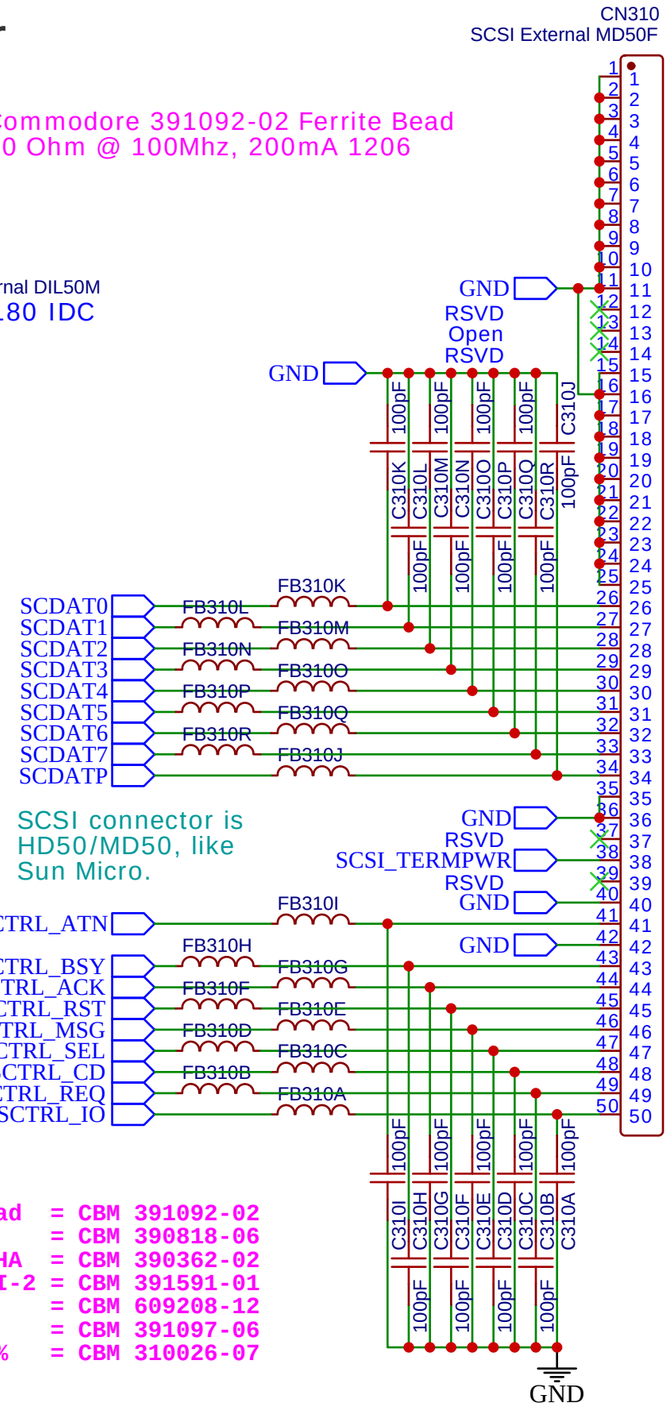




Internal 2x25 Connector

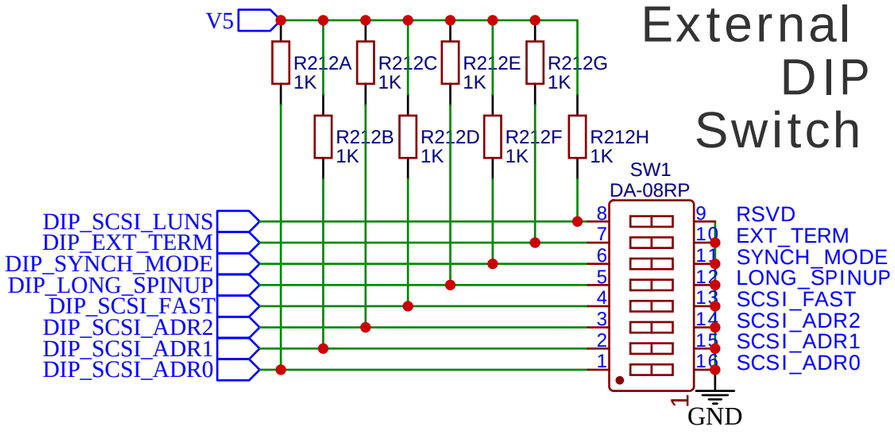


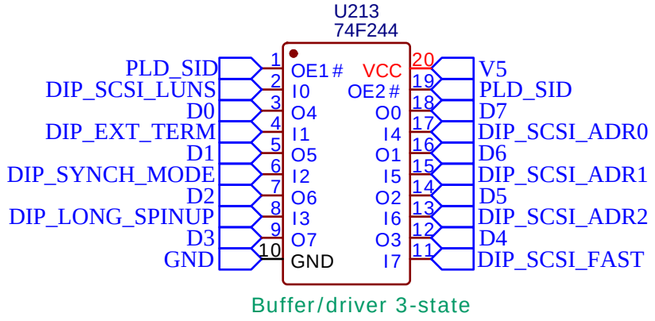
Commodore 391092-02 Ferrite Bead
60 Ohm @ 100Mhz, 200mA 1206



SCSI connector is
HD50/MD50, like
Sun Micro.

External DIP Switch

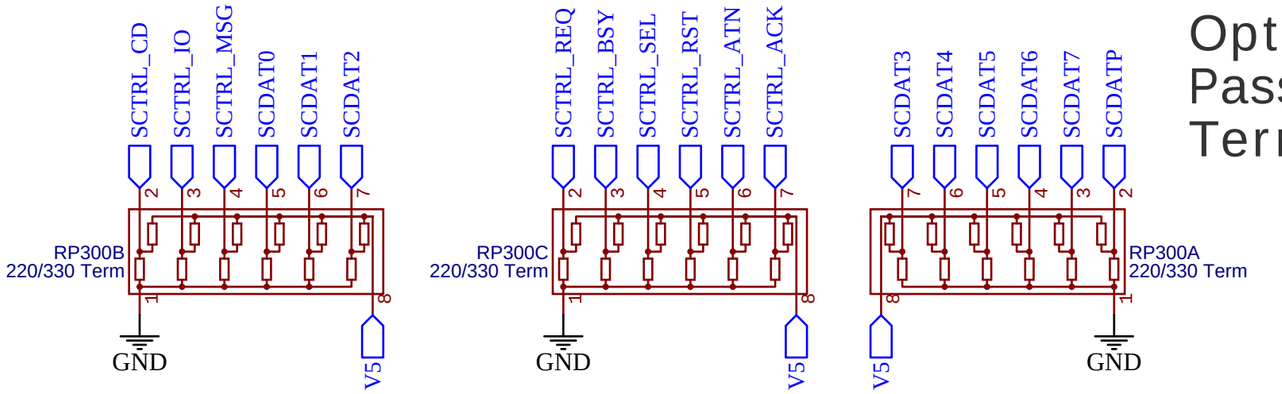




Buffer/driver 3-state

SCSI F.Bead = CBM 391092-02
100pF NPO = CBM 390818-06
SW1 8DIP HA = CBM 390362-02
HD50F SCSI-2 = CBM 391591-01
74F244 = CBM 609208-12
4.7uF 25V = CBM 391097-06
1K 1/8W 5% = CBM 310026-07

Optional Passive Termination



Commodore		DATE	Schematic A4091 SCSI
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B3
			Sheet: 2 of 8

External HD50 Connector

SCSI-2 Controller

32KB/64KB EPROM

U206
27c256

U300

NCR53C710

U301
Abracon 50MHz AC0 D.9403

U302
74F74D

74F74 = CBM 391320-01
53C710 = CBM 391593-01

Commodore		DATE
Design By:	Dave Haynie	1993
Reverse By:	SR	2021-11-09
Capture By:	CDH	2021-11-19

Schematic
A4091
NCR53C510
365120 REV: B3

Sheet: 3 of 8

PLD Symbols

The GAL/PAL devices on page 5 are programmed with gate configurations which consolidate what would be a large number of discrete components. Original Commodore source program files for the A4091 GAL components can be found on the Internet. The below can be used as a quick reference for symbols used in those programming files.

A0 - SCSI sizing address
A1 - SCSI sizing address _or_ A1/Lock signal
A2 - Address A2
A3 - Address A3
A4 - Address A4
A5 - Address A5
A6 - Address A6
A8 - Address A8 (known as A1 in U202)
A17 - Address A17
A18 - Address A18
A19 - Address A19
A23 - Address A23
!ABOEL - Low order address transfer enable
!ABOEH - High order address transfer enable
!AS - SCSI address strobe
!ASQ - Clocked/qualified version of SCSI AS*

BA2 - SCSI burst address
BA3 - SCSI burst address
!BDTACK - Z3 data acknowledge, buffered
!BERR - Z3 Bus error
BFCS - 1:Buffered cycle strobe
BFCS - 2:A4091 local Z3 cycle strobe
BLOCKBG - after 1st SBG block till end
BMASTER - Buffered/inverted version of MASTER
C7M - Z3 arbiter clock
!CBACK - SCSI burst acknowledge
!CBREQ - SCSI burst request
!CFGIN - Configuration chain input
!CFGOUT - Configuration chain output
CFGLT - Configuration address latch (on 0->1)
!CINH - Z3 cache inhibit
CLK - 1:25MHz NCR 53C710 bus clock
!CLK - 2:25MHz system clock
!CYCZ3 - On-bus Z3 cycle (internal)

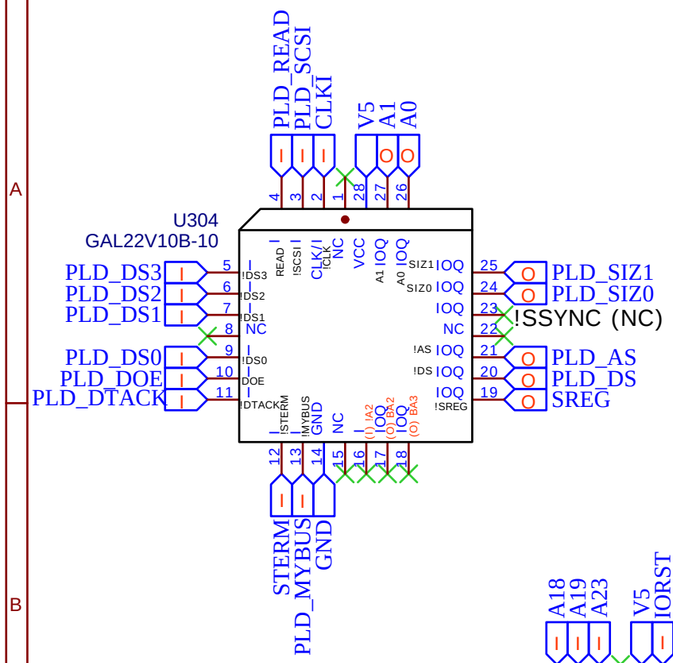
!D2Z - Data is transfered to Z3 bus
DBLT - Data is latched
!DCNT - State bit for Z3 stuff (internal)
DMASTER - Master delayed
!DBOE - Data transfer enable
DOE - Z3 Data phase (data output enable)
!DS0 - Z3 low order data strobe
!DS1 - Z3 data strobe
!DS2 - Z3 data strobe
!DS3 - Z3 high order data strobe
!DTACK - Z3 termination cycle
!DTSYNC - Synchronizer for DTACK->STERM (internal)
!DS - SCSI data strobe
!EBG - Expansion bus grant
!EBR - Z3 bus request
!EDTACK - Z3 data acknowledge, on bus
!EFCS - Z3 cycle strobe for DMA

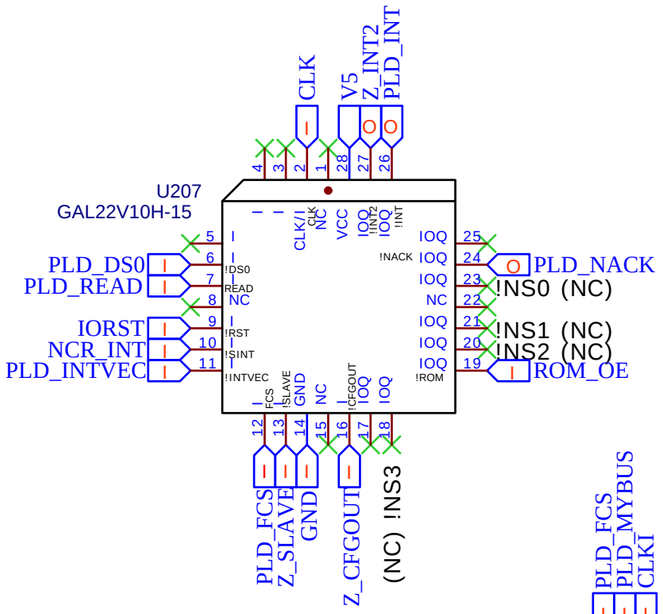
FC0 - CPU read/write function code
FC1 - CPU read/write function code
FC2 - CPU read/write function code
FCS - Z3 full cycle strobe
!INT - We generated an interrupt
!INT2 - Zorro bus interrupt 2
!INTASS - A vector has been assigned
!INTPOLL - An interrupt polling phase is signaled
INTREC - Interrupt register access
!INTSERV - We're servicing this interrupt phase
!INTSPC - Partially qualified interrupt space (decode)
!INTVEC - An interrupt vector phase is signaled

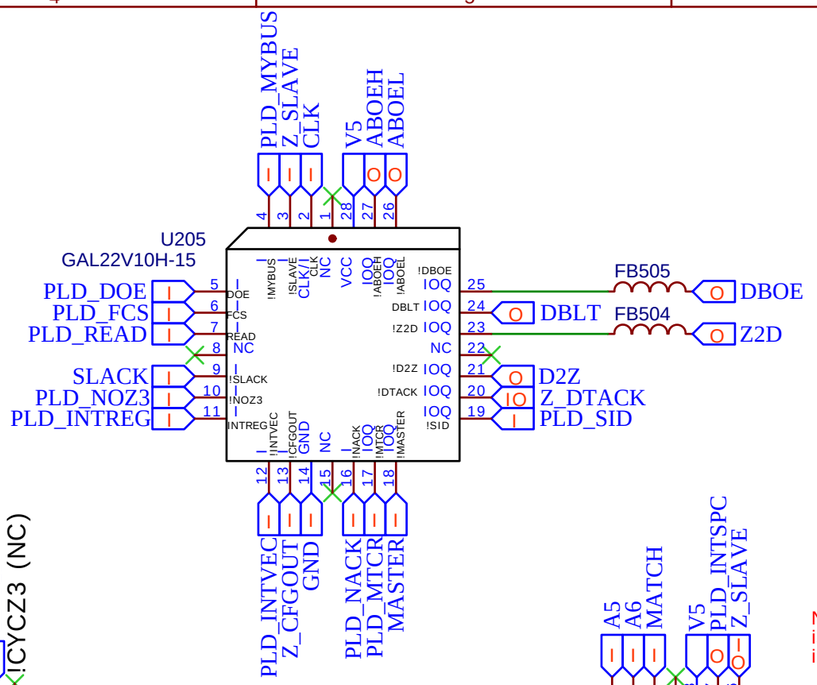
!MASTER - SCSI chip owns the A4091 bus
!MATCH - Address comparator match
!MTACK - Z3 slave burst strobe
!MTCR - Z3 multiple transfer burst cycle strobe
!MYBUS - The A4091 has the bus
!NACK - Data acknowledge
!NOZ3 - 1:Get off the Z3 bus (stop driving)
!NS0 - ROM access counter (internal)
!NS1 - ROM access counter (internal)
!NS2 - ROM access counter (internal)
!NS3 - ROM access counter (internal)

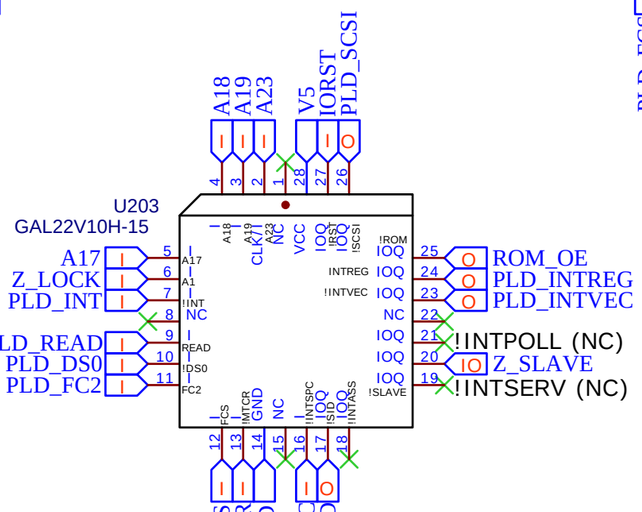
READ - Z3 read strobe (signal/cycle)
!REGED - A4091 is registered as Z3 master
RCHNG - Registration is changing (internal)
!ROM - System ROM access
!RST - System reset
!SBG - SCSI bus grant
!SBR - SCSI bus request
!SCSI - SCSI chip register address (see SREG)
!SHUNT - Z2 configuration shunt (0=Z2 1=Z3)
!SID - SCSI ID jumper access
SIZ0 - SCSI transfer size
SIZ1 - SCSI transfer size
!SINT - SCSI interrupt
!SLACK - NCR 53C710 slave acknowledge
!SLAVE - Z3 slave select for interrupt cycles
!SLAVEOE - Slave output enable
SMASTER - Synched master for fall edge
!SREG - SCSI chip register select (gated by clock)
SSBR - Synched SCSI bus request
!Z2D - Data is transfered from Z3 bus
!SSYNC - SCSI address synchronizer (internal)
!STERM - SCSI termination

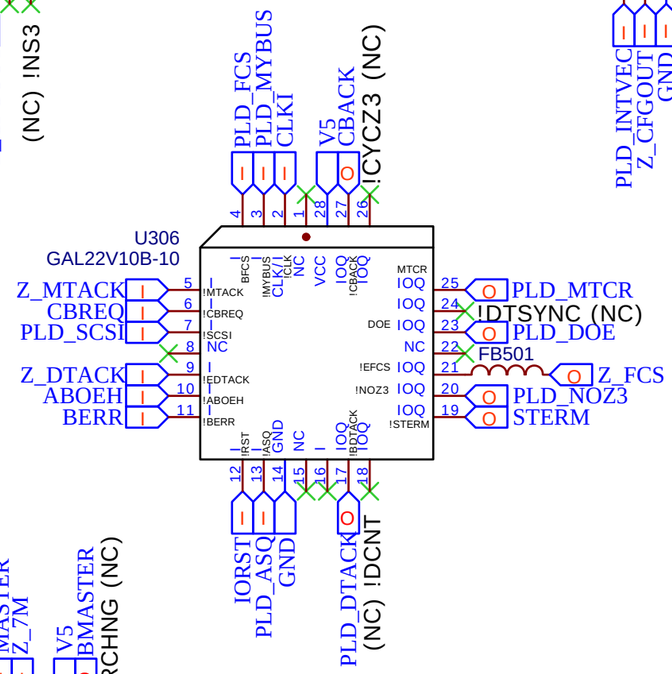
Commodore		DATE	Schematic
Design By:	Dave Haynie	1993	A4091
Reverse By:	SR	2021-11-09	PLDs
Capture By:	CDH	2021-11-19	365120 REV: B3

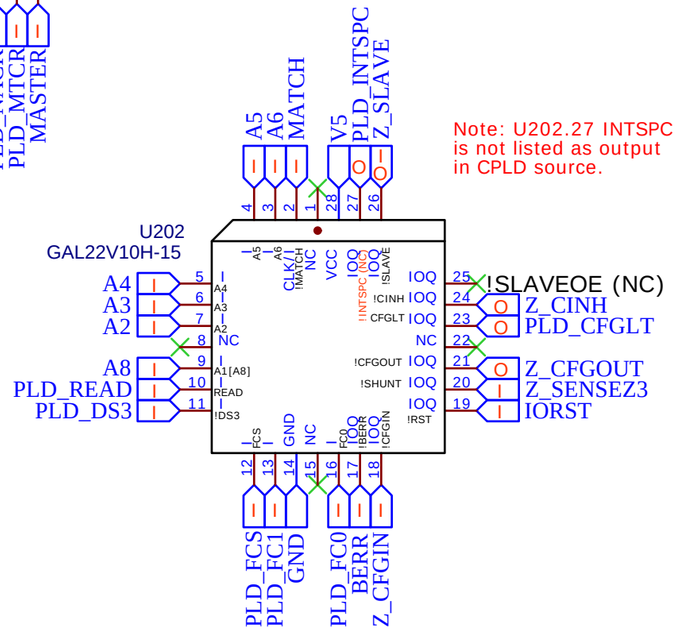




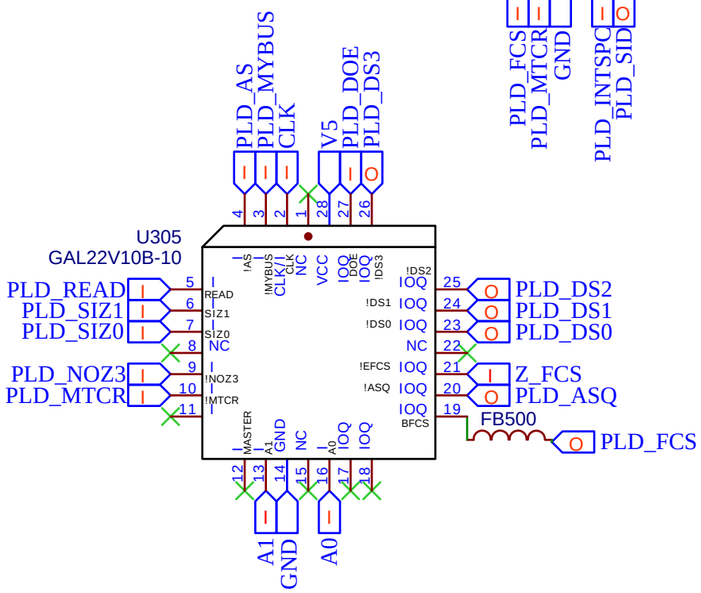


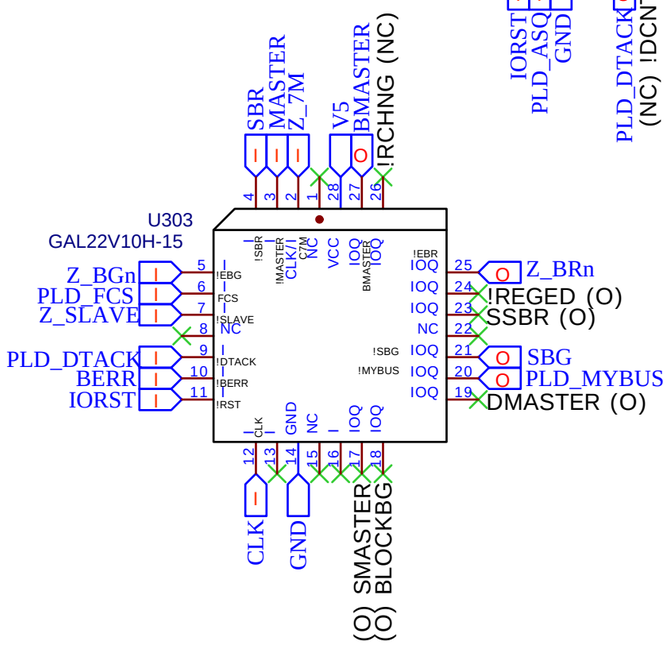






Note: U202.27 INTSPC is not listed as output in CPLD source.





From PLD equations

NC = Used Internally
I = Input
O = Output
IO = Bidirectional

Commodore		DATE	Schematic A4091 PLDs
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B3

U200
74FCT374TSO

Z_CFGOUT	1 OE#	VCC 20	V5
M31	2 Q0	Q7 19	M24
D31	3 D0	D7 18	D24
D30	4 D1	D6 17	D25
M30	5 Q1	Q6 16	M25
M29	6 Q2	Q5 15	M26
D29	7 D2	D5 14	D26
D28	8 D3	D4 13	D27
M28	9 Q3	Q4 12	M27
GND	10 GND	CP 11	PLD_CFGLT

8-bit Register w/ 3-state

U105
74FCT543TSO

DBLT	1 LEBA	VCC 24	V5
DBOE	2 OEBA	CEBA 23	Z2D
D24	3 A0	B0 22	Z_A24D24
D25	4 A1	B1 21	Z_A25D25
D26	5 A2	B2 20	Z_A26D26
D27	6 A3	B3 19	Z_A27D27
D28	7 A4	B4 18	Z_A28D28
D29	8 A5	B5 17	Z_A29D29
D30	9 A6	B6 16	Z_A30D30
D31	10 A7	B7 15	Z_A31D31
D2Z	11 CEAB	LEAB 14	DBLT
GND	12 GND	OEAB 13	DBOE

Latched Tranceiver

U108
74FCT543TSO

DBLT	1 LEBA	VCC 24	V5
DBOE	2 OEBA	CEBA 23	Z2D
D16	3 A0	B0 22	Z_D16
D17	4 A1	B1 21	Z_D17
D18	5 A2	B2 20	Z_D18
D19	6 A3	B3 19	Z_D19
D20	7 A4	B4 18	Z_D20
D21	8 A5	B5 17	Z_D21
D22	9 A6	B6 16	Z_D22
D23	10 A7	B7 15	Z_D23
D2Z	11 CEAB	LEAB 14	DBLT
GND	12 GND	OEAB 13	DBOE

Latched Tranceiver

U106
74FCT543TSO

DBLT	1 LEBA	VCC 24	V5
DBOE	2 OEBA	CEBA 23	Z2D
D15	3 A0	B0 22	Z_A23D15
D14	4 A1	B1 21	Z_A22D14
D13	5 A2	B2 20	Z_A21D13
D12	6 A3	B3 19	Z_A20D12
D11	7 A4	B4 18	Z_A19D11
D10	8 A5	B5 17	Z_A18D10
D9	9 A6	B6 16	Z_A17D9
D8	10 A7	B7 15	Z_A16D8
D2Z	11 CEAB	LEAB 14	DBLT
GND	12 GND	OEAB 13	DBOE

Latched Tranceiver

U204
74FCT374TSO

PLD_INTVEC	1 OE#	VCC 20	V5
D7	2 Q0	Q7 19	D0
D7	3 D0	D7 18	D0
D6	4 D1	D6 17	D1
D6	5 Q1	Q6 16	D1
D5	6 Q2	Q5 15	D2
D5	7 D2	D5 14	D2
D4	8 D3	D4 13	D3
D4	9 Q3	Q4 12	D3
GND	10 GND	CP 11	PLD_INTREG

8-bit Register w/ 3-state

U201
74FCT521TSO

GND	1 IA=B	VCC 20	V5
A31	2 A0	OA=B 19	MATCH
M31	3 B0	B7 18	M24
A30	4 A1	B7 17	A24
M30	5 B1	B6 16	M25
A29	6 A2	A6 15	A25
M29	7 B2	B5 14	M26
A28	8 A3	A5 13	A26
M28	9 B3	B4 12	M27
GND	10 GND	A4 11	A27

74FCT521

Identity Comparator

U100
74FCT543TSO

PLD_FCS	1 LEBA	VCC 24	V5
ABOEH	2 OEBA	CEBA 23	BMASTER
A31	3 A0	B0 22	Z_A31D31
A30	4 A1	B1 21	Z_A30D30
A29	5 A2	B2 20	Z_A29D29
A28	6 A3	B3 19	Z_A28D28
A27	7 A4	B4 18	Z_A27D27
A26	8 A5	B5 17	Z_A26D26
A25	9 A6	B6 16	Z_A25D25
A24	10 A7	B7 15	Z_A24D24
MASTER	11 CEAB	LEAB 14	GND
GND	12 GND	OEAB 13	ABOEH

Latched Tranceiver

U101
74FCT543TSO

PLD_FCS	1 LEBA	VCC 24	V5
ABOEH	2 OEBA	CEBA 23	BMASTER
A23	3 A0	B0 22	Z_A23D15
A22	4 A1	B1 21	Z_A22D14
A21	5 A2	B2 20	Z_A21D13
A20	6 A3	B3 19	Z_A20D12
A19	7 A4	B4 18	Z_A19D11
A18	8 A5	B5 17	Z_A18D10
A17	9 A6	B6 16	Z_A17D9
A16	10 A7	B7 15	Z_A16D8
MASTER	11 CEAB	LEAB 14	GND
GND	12 GND	OEAB 13	ABOEH

Latched Tranceiver

U102
74FCT543TSO

PLD_FCS	1 LEBA	VCC 24	V5
ABOEH	2 OEBA	CEBA 23	BMASTER
A15	3 A0	B0 22	Z_A15D7
A14	4 A1	B1 21	Z_A14D6
A13	5 A2	B2 20	Z_A13D5
A12	6 A3	B3 19	Z_A12D4
A11	7 A4	B4 18	Z_A11D3
A10	8 A5	B5 17	Z_A10D2
A9	9 A6	B6 16	Z_A9D1
A8	10 A7	B7 15	Z_A8D0
MASTER	11 CEAB	LEAB 14	GND
GND	12 GND	OEAB 13	ABOEH

Latched Tranceiver

U107
74FCT543TSO

DBLT	1 LEBA	VCC 24	V5
DBOE	2 OEBA	CEBA 23	Z2D
D7	3 A0	B0 22	Z_A15D7
D6	4 A1	B1 21	Z_A14D6
D5	5 A2	B2 20	Z_A13D5
D4	6 A3	B3 19	Z_A12D4
D3	7 A4	B4 18	Z_A11D3
D2	8 A5	B5 17	Z_A10D2
D1	9 A6	B6 16	Z_A9D1
D0	10 A7	B7 15	Z_A8D0
D2Z	11 CEAB	LEAB 14	DBLT
GND	12 GND	OEAB 13	DBOE

Latched Tranceiver

M31 R200A 1K V5
M30 R200B 1K
M29 R200C 1K
M28 R200D 1K
M27 R200E 1K
M26 R200F 1K
M25 R200G 1K
M24 R200H 1K

R100A
1K
Z_SENSEZ3 V5

7407 = CBM 391188-01
74F245 = CBM 391375-01
74FCT374 = CBM 390784-02
74FCT543 = CBM 391487-01

U307
74F07D

SCSI_BUSY	1 1A	VCC 14	V5
LED	2 1Y	6A 13	GND
SCSI_BUSY	3 2A	6Y 12	
LED	4 2Y	5A 11	GND
Z_BERR	5 3A	5Y 10	
BERR	6 3Y	4A 9	Z_IORST
GND	7 GND	4Y 8	IORST

Open collecter buffer

U103
74F245D

BMASTER	1 T/R#	VCC 20	V5
A7	2 A0	OE# 19	ABOEL
A6	3 A1	B0 18	Z_A7
A5	4 A2	B1 17	Z_A6
A4	5 A3	B2 16	Z_A5
A3	6 A4	B3 15	Z_A4
A2	7 A5	B4 14	Z_A3
PLD_FC2	8 A6	B5 13	Z_A2
PLD_READ	9 A7	B6 12	Z_FC2
GND	10 GND	B7 11	Z_READ

Buffer/driver 3-state

GND Z_DS1 Z_IORST Z_7M GND Z_D21 Z_D22 Z_D23 Z_A24D24 Z_A25D25 Z_A26D26 Z_DS3 Z_DS2 Z_READ Z_DTACK Z_BGn Z_BRn Z_A21D13 Z_A20D12 Z_A19D11 Z_A18D10 Z_MTACK Z_BERR Z_A12D4 Z_A11D3 Z_A10D2 Z_A9D1 Z_A8D0 Z_A7 Z_A3 Z_A4 Z_MTCR Z_CFGIN V12 V5 GND

100 GND 98 /DS1,NC 96 RSVD,/EINT1 94 /IORST,/BUSRST 92 7M Clock 90 GND 88 GND 86 RSVD+D21,D5 84 RSVD+D22,D6 82 RSVD+D23,D7 80 A24+D24,D8 78 A25+D25,D9 76 A26+D26,D10 74 /CCS,/AS 72 /DS3,/UDS 70 /DS2,/LDS 68 READ 66 /DTACK 64 /BGn 62 /BGACK 60 /BRn 58 A21+D13,A21 56 A20+D12,A20 54 A19+D11,A19 52 A18+D10,A18 50 E Clock 48 /MTACK,/VPA 46 /BERR 44 RSVD,/EINT4 42 RSVD,/EINT5 40 RSVD,/EINT7 38 A12+D4,A12 36 A11+D3,A11 34 A10+D2,A10 32 A9+D1,A9 30 A8+D0,A8 28 A7 26 A3 24 A4 22 /INT6 20 -12V 18 /MTCR,XRDY 16 /C1 Clock 14 /C3 Clock 12 /CFGINn 10 +12V 08 -5V 06 +5V 04 GND 02 GND

PCB Top

Zorro III Edge
C1

PCB Bottom

99 GND 97 /FCS,NC 95 /BCLR,/GBG 93 DOE 91 SenseZ3,GND 89 GND 87 GND 85 GND 83 RSVD+D20,D4 81 RSVD+D19,D3 79 RSVD+D18,D2 77 RSVD+D17,D1 75 RSVD+D16,D0 73 GND 71 A27+D27,D11 69 A28+D28,D12 67 A29+D29,D13 65 A30+D30,D14 63 A31+D31,D15 61 GND 59 A23+D15,A23 57 A22+D14,A22 55 /HLT 53 /RST 51 /DS0,/VMA 49 GND 47 A17+D9,A17 45 A16+D8,A16 43 A15+D7,A15 41 A14+D6,A14 39 A13+D5,A13 37 GND 35 FC2 33 FC1 31 FC0 29 /LOCK,A1 27 A2 25 GND 23 A6 21 A5 19 /INT2 17 /CINH,/OVR 15 CDAC Clock 13 GND 11 /CFGOUTn 09 /SLAVEn 07 /OWN 05 +5V 03 GND 01 GND

GND Z_FCS Z_DOE Z_SENSEZ3 GND Z_D20 Z_D19 Z_D18 Z_D17 Z_D16 GND Z_A27D27 Z_A28D28 Z_A29D29 Z_A30D30 Z_A31D31 GND Z_A23D15 Z_A22D14 Z_DS0 GND Z_A17D9 Z_A16D8 Z_A15D7 Z_A14D6 Z_A13D5 GND Z_FC2 Z_FC1 Z_FC0 Z_LOCK Z_A2 GND Z_A6 Z_A5 Z_INT2 Z_CINH GND Z_CFGOUT Z_SLAVE V5 GND

V5
R109A 1K
R109B 1K
R109C 1K
R109D 1K
R109E 1K
R109F 1K
R109G 1K

U109
74F245D

BMASTER	1 T/R#	VCC 20	V5
PLD_FC1	2 A0	OE# 19	ABOEL
PLD_FC0	3 A1	B0 18	Z_FC1
PLD_DOE	4 A2	B1 17	Z_FC0
PLD_MTCR	5 A3	B2 16	Z_DOE
PLD_DS3	6 A4	B3 15	Z_MTCR
PLD_DS2	7 A5	B4 14	
PLD_DS1	8 A6	B5 13	
PLD_DS0	9 A7	B6 12	
GND	10 GND	B7 11	

FB507
FB508
Z_DS3 Z_DS2 Z_DS1 Z_DS0

Buffer/driver 3-state

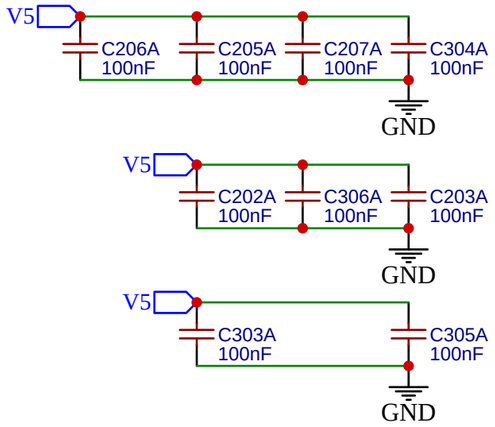
R109H 1K
GND

R103A
1K
PLD_FC2 V5

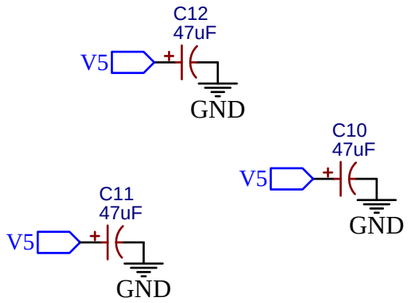
R103B
1K
PLD_READ V5

Commodore		DATE	Schematic A4091 Zorro
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B3
© 1993 Commodore Business Machines			Sheet: 6 of 8

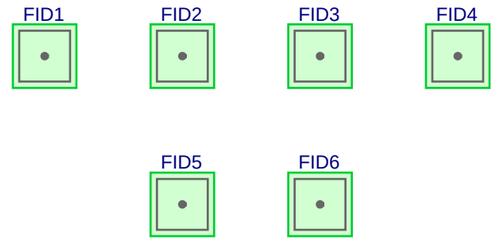
PLD bypass caps



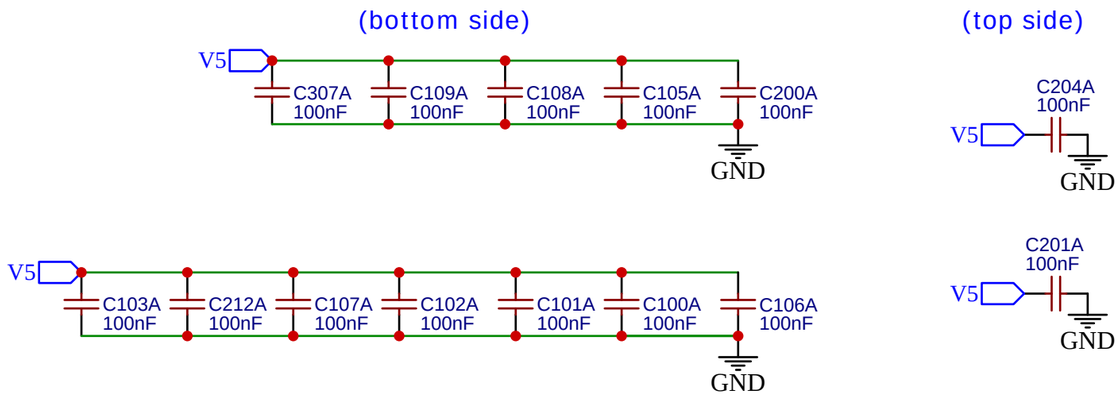
Bulk power



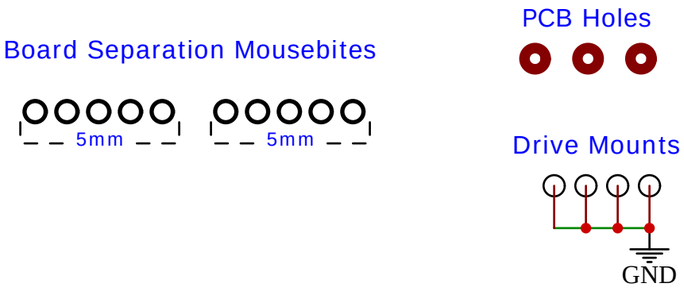
Assembly fiducials



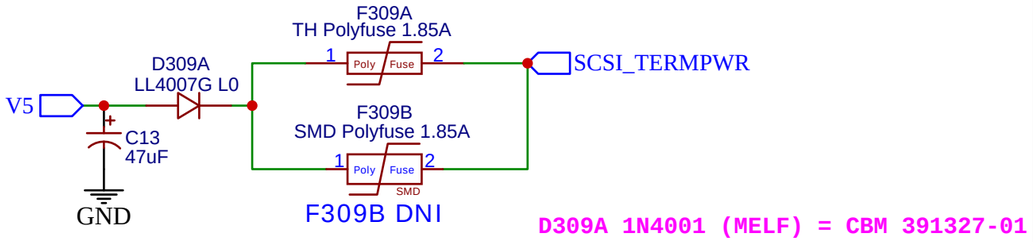
Discrete IC bypass caps



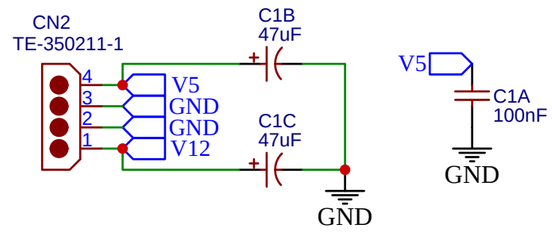
Mechanical holes



SCSI termination power



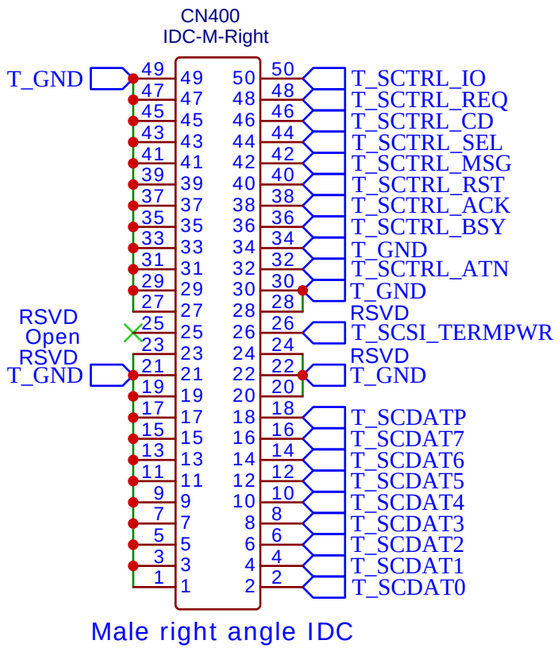
MOLEX Drive Power



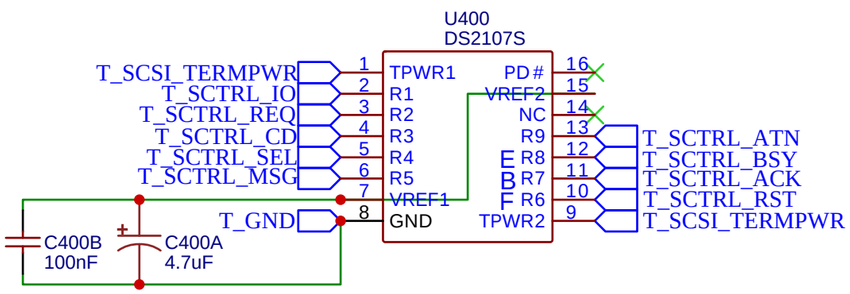
Commodore		DATE	Schematic A4091 Power
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B3

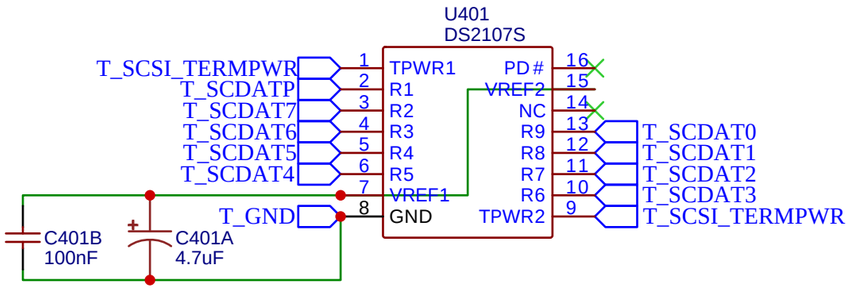
Sheet: 7 of 8

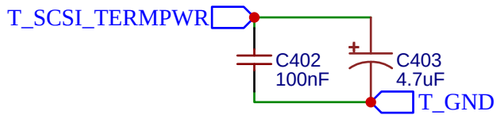
SCSI Active Terminator cut-out board



Male right angle IDC

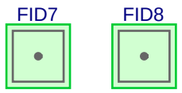






Board Holes

Fiducials



Commodore		DATE	Schematic
Design By:	Dave Haynie	1993	A4091
Reverse By:	SR	2021-11-09	SCSI Terminator
Capture By:	CDH	2021-11-19	365120 REV: B3

Sheet: 8 of 8