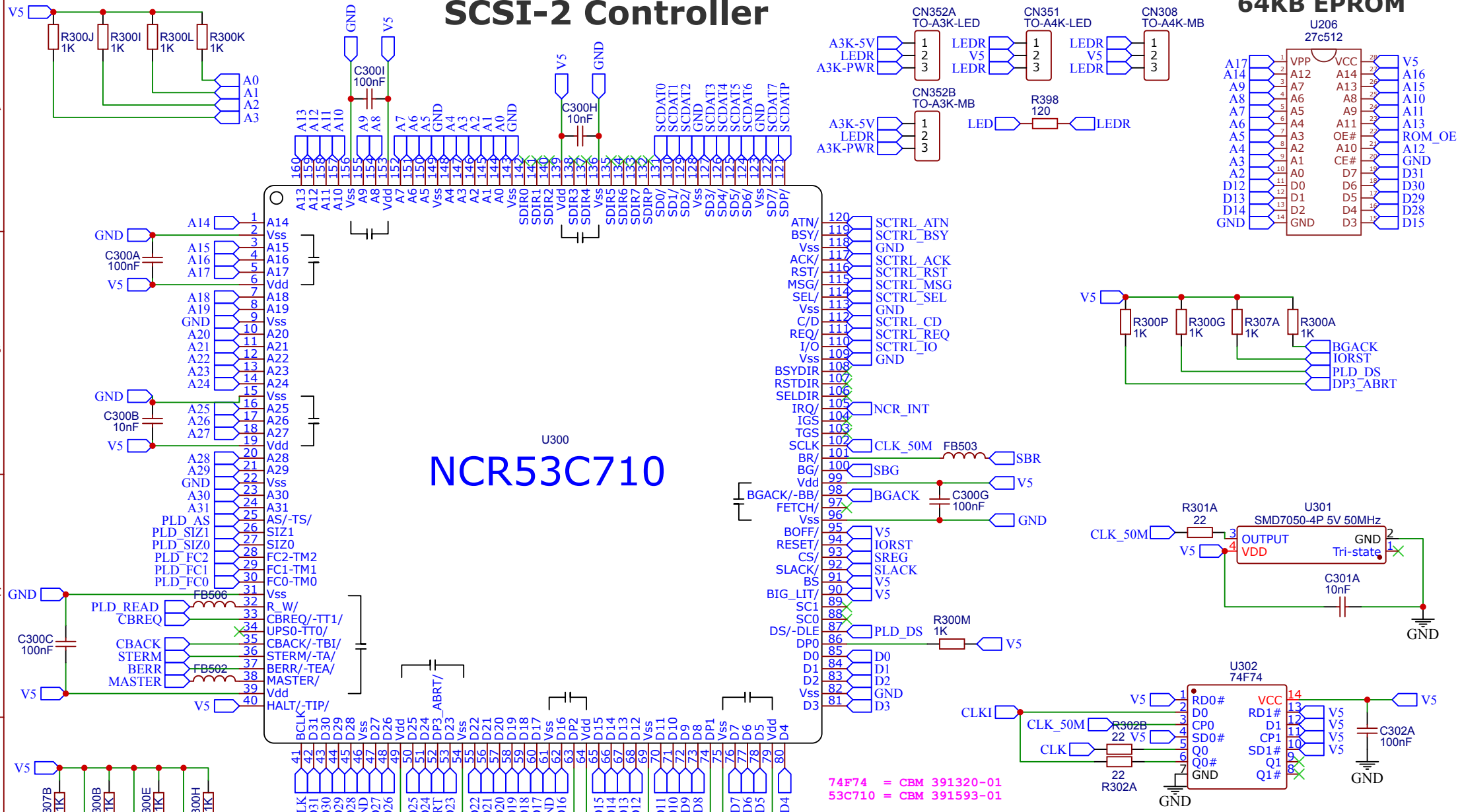
SCSI-2 Controller



Commodore	DATE	Schematic	
Design By:	Dave Haynie	1993	A4091
Reverse By:	SR	2021-11-09	NCR53C510
Capture By:	CDH	2021-11-19	365120 REV: B4
			Sheet: 3 of 8

PLD Symbols

The GAL/PAL devices on page 5 are programmed with gate configurations which consolidate what would be a large number of discrete components. Original Commodore source program files for the A4091 GAL components can be found on the Internet. The below can be used as a quick reference for symbols used in those programming files.

A0 - SCSI sizing address
A1 - SCSI sizing address _or_ A1/Lock signal
A2 - Address A2
A3 - Address A3
A4 - Address A4
A5 - Address A5
A6 - Address A6
A8 - Address A8 (known as A1 in U202)
A17 - Address A17
A18 - Address A18
A19 - Address A19
A23 - Address A23
!ABOEL - Low order address transfer enable
!ABOEH - High order address transfer enable
!AS - SCSI address strobe
!ASQ - Clocked/qualified version of SCSI AS*

BA2 - SCSI burst address
BA3 - SCSI burst address
!BDTACK - Z3 data acknowledge, buffered
!BERR - Z3 Bus error
BFCS - 1:Buffered cycle strobe
BFCS - 2:A4091 local Z3 cycle strobe
BLOCKBG - after 1st SBG block till end
BMASTER - Buffered/inverted version of MASTER
C7M - Z3 arbiter clock
!CBACK - SCSI burst acknowledge
!CBREQ - SCSI burst request
!CFGIN - Configuration chain input
!CFGOUT - Configuration chain output
CFGLT - Configuration address latch (on 0->1)
!CINH - Z3 cache inhibit
CLK - 1:25MHz NCR 53C710 bus clock
!CLK - 2:25MHz system clock
!CYCZ3 - On-bus Z3 cycle (internal)

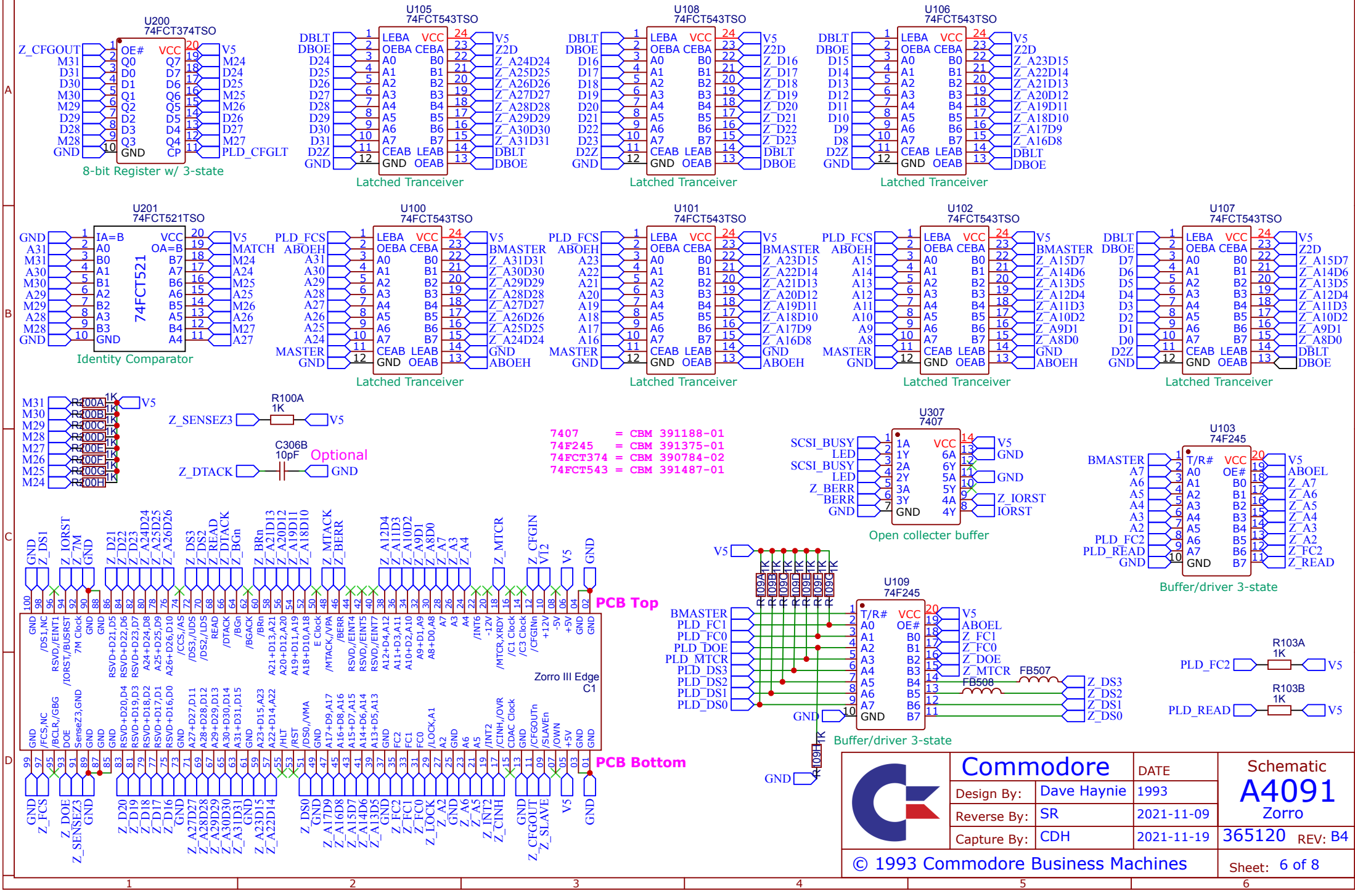
!D2Z - Data is transfered to Z3 bus
DBLT - Data is latched
!DCNT - State bit for Z3 stuff (internal)
DMASTER - Master delayed
!DBOE - Data transfer enable
DOE - Z3 Data phase (data output enable)
!DS0 - Z3 low order data strobe
!DS1 - Z3 data strobe
!DS2 - Z3 data strobe
!DS3 - Z3 high order data strobe
!DTACK - Z3 termination cycle
!DTSYNC - Synchronizer for DTACK->STERM (internal)
!DS - SCSI data strobe
!EBG - Expansion bus grant
!EBR - Z3 bus request
!EDTACK - Z3 data acknowledge, on bus
!EFCS - Z3 cycle strobe for DMA

FC0 - CPU read/write function code
FC1 - CPU read/write function code
FC2 - CPU read/write function code
FCS - Z3 full cycle strobe
!INT - We generated an interrupt
!INT2 - Zorro bus interrupt 2
!INTASS - A vector has been assigned
!INTPOLL - An interrupt polling phase is signaled
INTREC - Interrupt register access
!INTSERV - We're servicing this interrupt phase
!INTSPC - Partially qualified interrupt space (decode)
!INTVEC - An interrupt vector phase is signaled

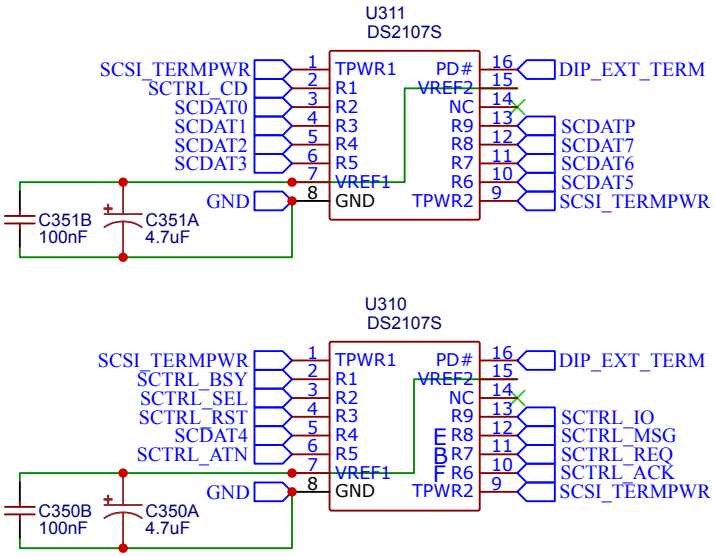
!MASTER - SCSI chip owns the A4091 bus
!MATCH - Address comparator match
!MTACK - Z3 slave burst strobe
!MTCR - Z3 multiple transfer burst cycle strobe
!MYBUS - The A4091 has the bus
!NACK - Data acknowledge
!NOZ3 - 1:Get off the Z3 bus (stop driving)
!NS0 - ROM access counter (internal)
!NS1 - ROM access counter (internal)
!NS2 - ROM access counter (internal)
!NS3 - ROM access counter (internal)

READ - Z3 read strobe (signal/cycle)
!REGED - A4091 is registered as Z3 master
RCHNG - Registration is changing (internal)
!ROM - System ROM access
!RST - System reset
!SBG - SCSI bus grant
!SBR - SCSI bus request
!SCSI - SCSI chip register address (see SREG)
!SHUNT - Z2 configuration shunt (0=Z2 1=Z3)
!SID - SCSI ID jumper access
SIZ0 - SCSI transfer size
SIZ1 - SCSI transfer size
!SINT - SCSI interrupt
!SLACK - NCR 53C710 slave acknowledge
!SLAVE - Z3 slave select for interrupt cycles
!SLAVEOE - Slave output enable
SMASTER - Synched master for fall edge
!SREG - SCSI chip register select (gated by clock)
SSBR - Synched SCSI bus request
!Z2D - Data is transfered from Z3 bus
!SSYNC - SCSI address synchronizer (internal)
!STERM - SCSI termination

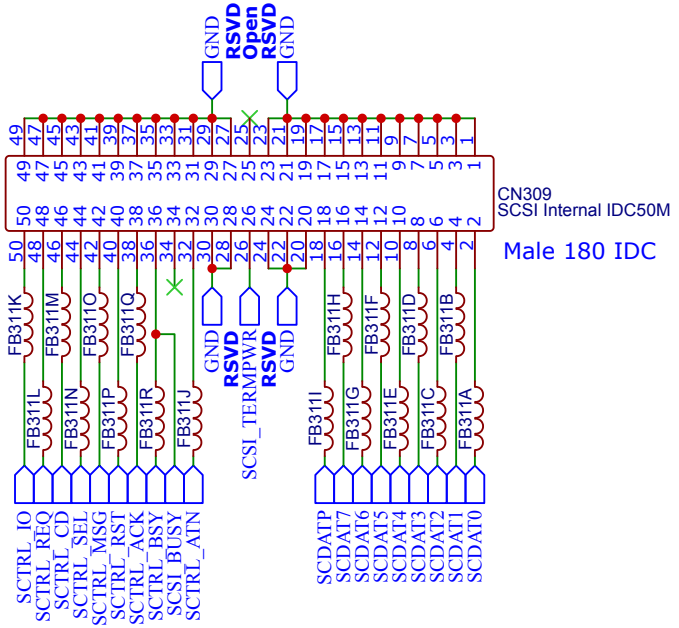
Commodore		DATE	Schematic
Design By:	Dave Haynie	1993	A4091
Reverse By:	SR	2021-11-09	PLDs
Capture By:	CDH	2021-11-19	365120 REV: B4


U200
74FCT374TSO
8-bit Register w/ 3-state
U105
74FCT543TSO
Latched Tranceiver
U108
74FCT543TSO
Latched Tranceiver
U106
74FCT543TSO
Latched Tranceiver
U201
74FCT521TSO
Identity Comparator
U100
74FCT543TSO
Latched Tranceiver
U101
74FCT543TSO
Latched Tranceiver
U102
74FCT543TSO
Latched Tranceiver
U107
74FCT543TSO
Latched Tranceiver
R100A
1K
C306B
10pF
Optional
7407 = CBM 391188-01
74F245 = CBM 391375-01
74FCT374 = CBM 390784-02
74FCT543 = CBM 391487-01
U307
7407
Open collecter buffer
U103
74F245
Buffer/driver 3-state
U109
74F245
Buffer/driver 3-state
R103A
1K
R103B
1K
PCB Top
PCB Bottom
Zorro III Edge
C1
Commodore
DATE
Design By: Dave Haynie 1993
Reverse By: SR 2021-11-09
Capture By: CDH 2021-11-19
Schematic
A4091
Zorro
365120 REV: B4
© 1993 Commodore Business Machines
Sheet: 6 of 8

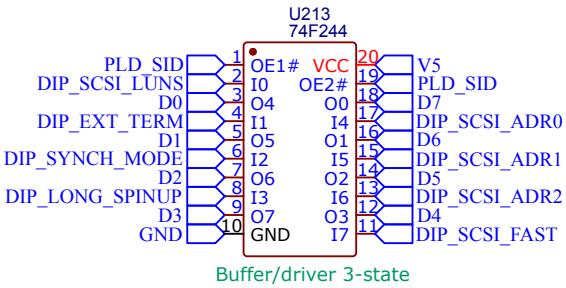
Active Termination



Internal 2x25 Connector

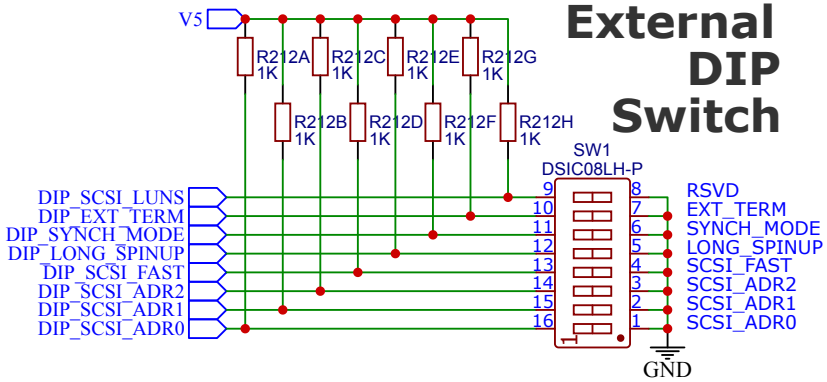


Commodore 391092-02 Ferrite Bead
60 Ohm @ 100Mhz, 200mA 1206



Buffer/driver 3-state

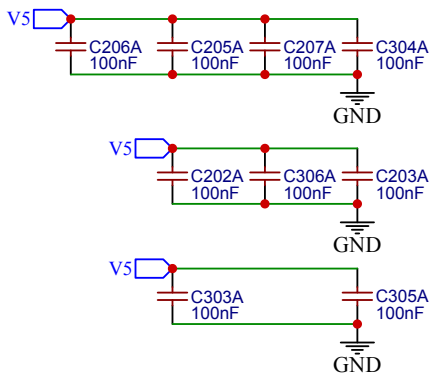
External DIP Switch



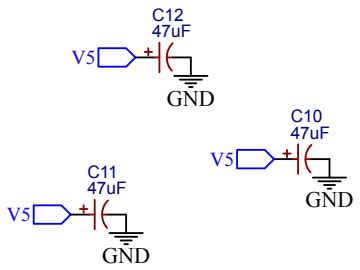
SCSI F.Bead	= CBM 391092-02
100pF NPO	= CBM 390818-06
SW1 8DIP HA	= CBM 390362-02
74F244	= CBM 609208-12
4.7uF 25V	= CBM 391097-06
1K 1/8W 5%	= CBM 310026-07

Commodore		DATE	Schematic
Design By:	Dave Haynie	1993	A4091 SCSI
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B4

PLD bypass caps

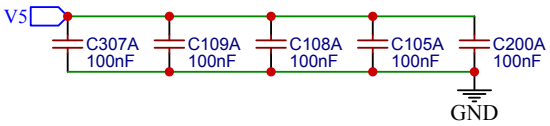


Bulk power

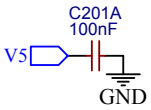


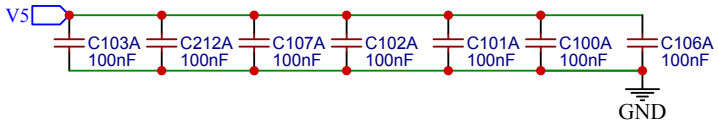
Discrete IC bypass caps

(bottom side)



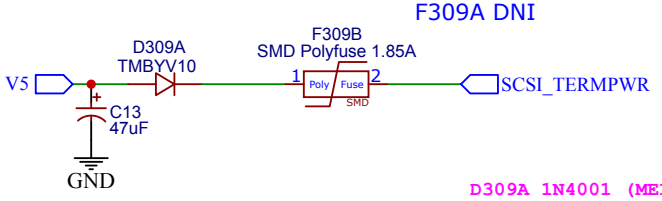
(top side)





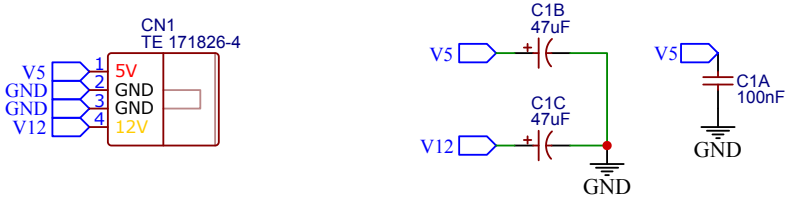
SCSI termination power

F309A DNI



D309A 1N4001 (MELF) = CBM 391327-01

Berg Drive Power



Commodore		DATE	Schematic A4091 Power
Design By:	Dave Haynie	1993	
Reverse By:	SR	2021-11-09	
Capture By:	CDH	2021-11-19	365120 REV: B4

Sheet: 7 of 8

Commodore A4091

Rev B Advanced SCSI II Controller Board

This Zorro III board was originally designed and sold by Commodore, which did a single run of the Rev A design before shelving it. Commodore was running out of money at the time and didn't want to risk a second production run. The Rev B design was given to DKB Software for production, marketing, sales, distribution, and support.

Features:

- Boot ROM
- NCR 53C710 SCSI II controller
- 50 pin internal connector
- 50 pin external SCSI2 connector
- 3.5" hard drive mounts on the card
- Active SCSI termination
- Zorro III bus support

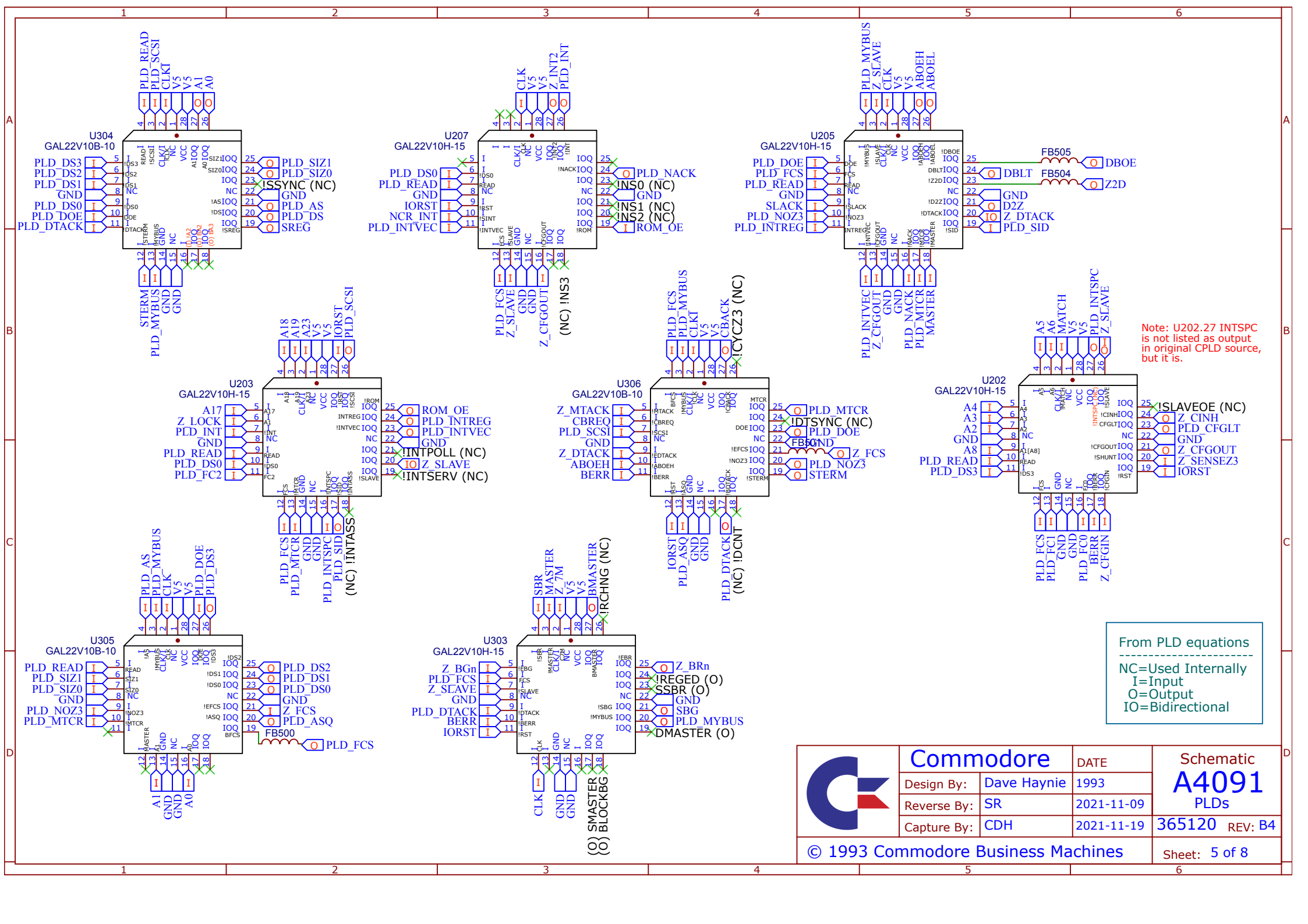
Caveats:

- Requires Buster 11
- Does not work with with A3640 Rev 3.0
- No RAM option
- No wide SCSI support

The Commodore A4091 was reverse-engineered by Stefan Reinauer and Chris Hooper.

ReA4091 Rev 4 2023-05-15

Commodore		DATE	Schematic
Design By:	Dave Haynie	1993	A4091
Reverse By:	SR	2021-11-09	Overview
Capture By:	CDH	2021-11-19	365120 REV: B4


U304
GAL22V10B-10
PLD_READ
PLD_SCSI
CLK1
V5
V5
A1
A0
PLD_DS3
PLD_DS2
PLD_DS1
GND
PLD_DS0
PLD_DOE
PLD_DTACK
!SSYNC (NC)
PLD_SIZ1
PLD_SIZ0
GND
PLD_AS
PLD_DS
SREG
STERM
PLD_MYBUS
GND
GND
U207
GAL22V10H-15
CLK
V5
V5
Z_INT2
PLD_INT
PLD_DS0
PLD_READ
GND
IORST
NCR_INT
PLD_INTVEC
PLD_NACK
!INS0 (NC)
GND
!INS1 (NC)
!INS2 (NC)
ROM_OE
PLD_FCS
Z_SLAVE
GND
GND
Z_CFGOUT
(NC) !INS3
U205
GAL22V10H-15
PLD_MYBUS
Z_SLAVE
CLK
V5
V5
ABOEH
ABOEL
PLD_DOE
PLD_FCS
PLD_READ
GND
SLACK
PLD_NOZ3
PLD_INTREG
FB505
DBOE
DBLT
FB504
Z2D
GND
D2Z
Z_DTACK
PLD_SID
PLD_INTVEC
Z_CFGOUT
GND
GND
PLD_NACK
PLD_MTCR
MASTER
U203
GAL22V10B-15
A18
A19
A23
V5
V5
IORST
PLD_SCSI
A17
Z_LOCK
PLD_INT
GND
PLD_READ
PLD_DS0
PLD_FC2
ROM_OE
PLD_INTREG
PLD_INTVEC
GND
!INTPOLL (NC)
Z_SLAVE
!INTSERV (NC)
PLD_FCS
PLD_MTCR
GND
GND
PLD_INTSPC
PLD_SID
(NC) !INTASS
U306
GAL22V10B-10
PLD_FCS
PLD_MYBUS
CLK1
V5
V5
CBACK
!CYCZ3 (NC)
Z_MTACK
CBREQ
PLD_SCSI
GND
Z_DTACK
ABOEH
BERR
PLD_MTCR
!DTSYNC (NC)
PLD_DOE
FB501
GND
Z_FCS
PLD_NOZ3
STERM
IORST
PLD_ASQ
GND
GND
PLD_DTACK
(NC) !DCNT
U202
GAL22V10H-15
A5
A6
MATCH
V5
V5
PLD_INTSPC
Z_SLAVE
A4
A3
A2
GND
A8
PLD_READ
PLD_DS3
!SLAVEOE (NC)
Z_CINH
PLD_CFGLT
GND
Z_CFGOUT
Z_SENSEZ3
IORST
PLD_FCS
PLD_FC1
GND
GND
PLD_FC0
BERR
Z_CFGIN
Note: U202.27 INTSPC is not listed as output in original CPLD source, but it is.
U305
GAL22V10B-10
PLD_AS
PLD_MYBUS
CLK
V5
V5
PLD_DOE
PLD_DS3
PLD_READ
PLD_SIZ1
PLD_SIZ0
GND
PLD_NOZ3
PLD_MTCR
PLD_DS2
PLD_DS1
PLD_DS0
GND
Z_FCS
PLD_ASQ
FB500
PLD_FCS
A1
GND
GND
A0
U303
GAL22V10H-15
SBR
MASTER
Z_7M
V5
V5
BMASTER
!RCHNG (NC)
Z_BGn
PLD_FCS
Z_SLAVE
GND
PLD_DTACK
BERR
IORST
Z_BRn
!REGED (O)
!SSBR (O)
GND
SBG
PLD_MYBUS
DMASTER (O)
CLK
GND
GND
(O) SMASTER
(O) BLOCKBG
From PLD equations
NC=Used Internally
I=Input
O=Output
IO=Bidirectional
Commodore
DATE
Design By:
Dave Haynie
1993
Reverse By:
SR
2021-11-09
Capture By:
CDH
2021-11-19
Schematic
A4091
PLDs
365120
REV: B4
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Sheet: 5 of 8