

Commodore A4091

Rev B Advanced SCSI II Controller Board

This Zorro III board was originally designed and sold by Commodore, which did a single run of the Rev A design before shelving it. Commodore was running out of money at the time and didn't want to risk a second production run. The Rev B design was given to DKB Software for production, marketing, sales, distribution, and support.

Features:


- Boot ROM
- NCR 53C710 SCSI II controller
- 50 pin internal connector
- 50 pin external SCSI2 connector
- 3.5" hard drive mounts on the card
- Active SCSI termination
- Zorro III bus support

Caveats:

- Requires Buster 11
- Does not work with with A3640 Rev 3.0
- No RAM option
- No wide SCSI support

The Commodore A4091 was reverse-engineered by Stefan Reinauer and Chris Hooper.

ReA4091 Rev 4 2023-05-15

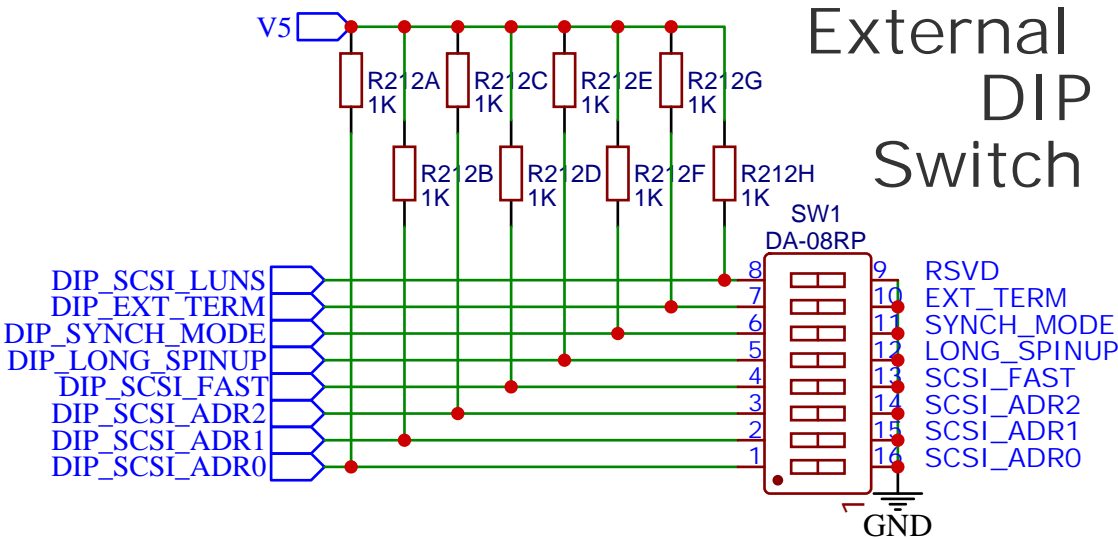
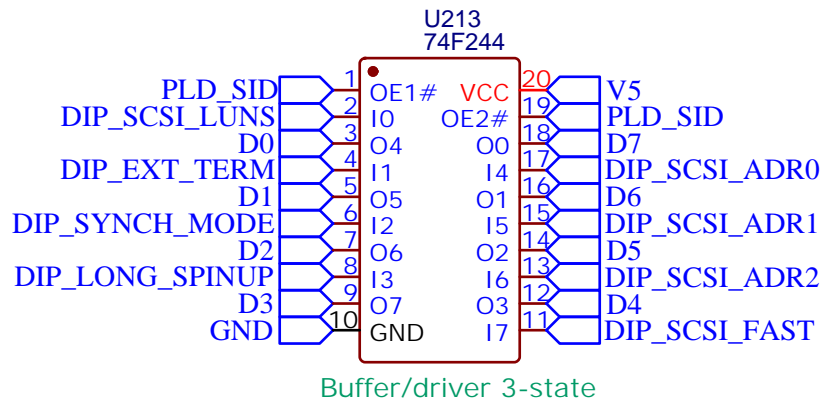
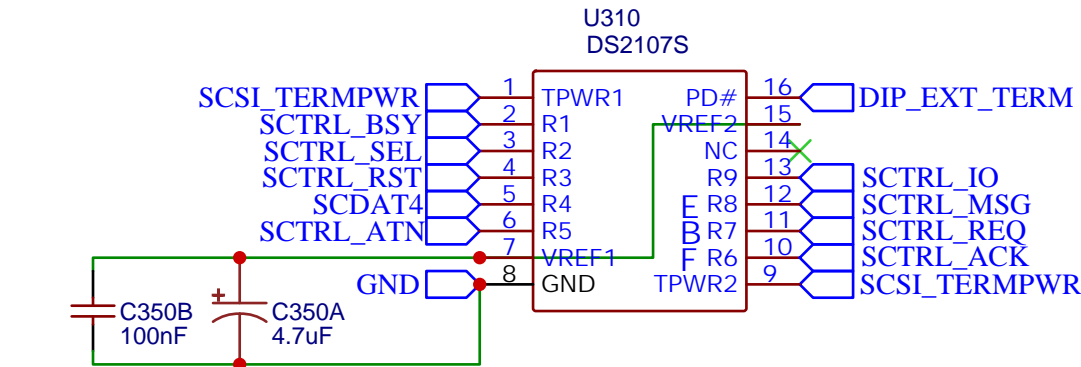
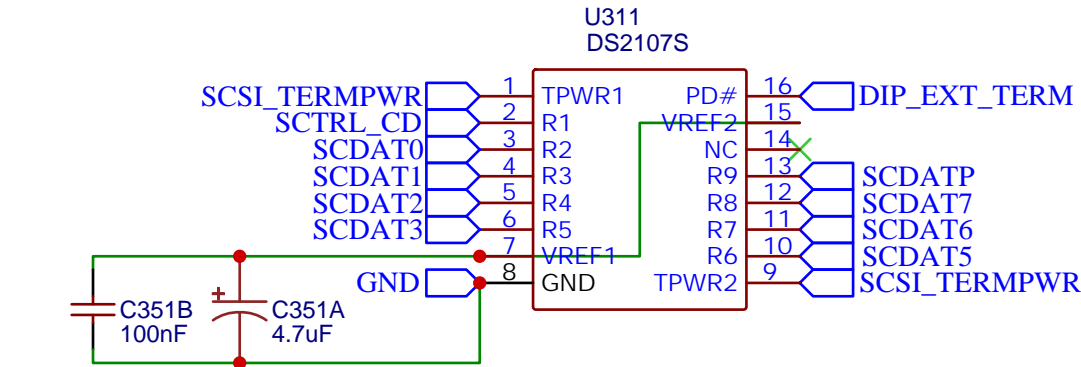
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|---|-------------|-------------|------------|---|
|  | Commodore | | DATE | Schematic A4091 Overview 365120 REV: B4 |
| | Design By: | Dave Haynie | 1993 | |
| | Reverse By: | SR | 2021-11-09 | |
| | Capture By: | CDH | 2021-11-19 | |
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Active Termination

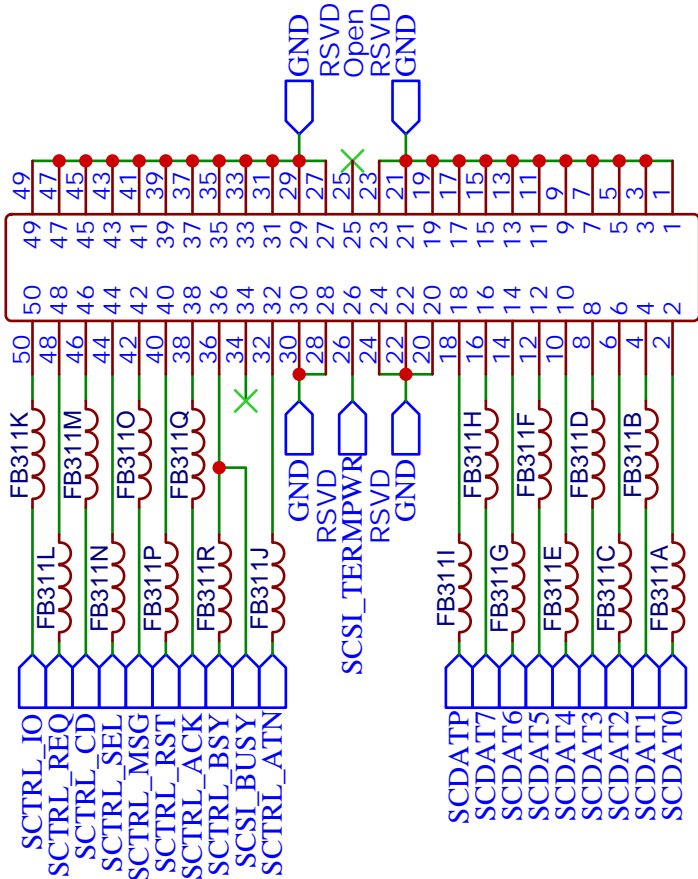
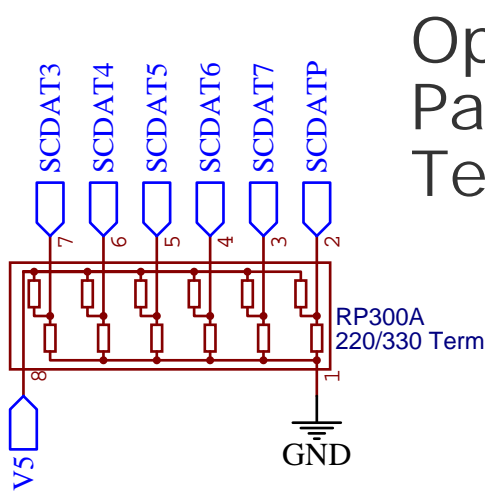
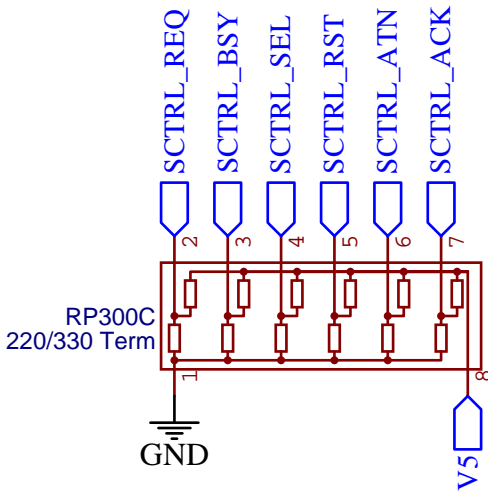
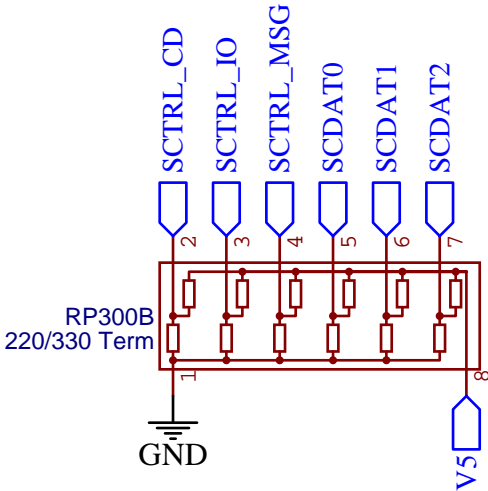
Internal 2x25 Connector

Commodore 391092-02 Ferrite Bead
60 Ohm @ 100Mhz, 200mA 1206

External HD50 Connector

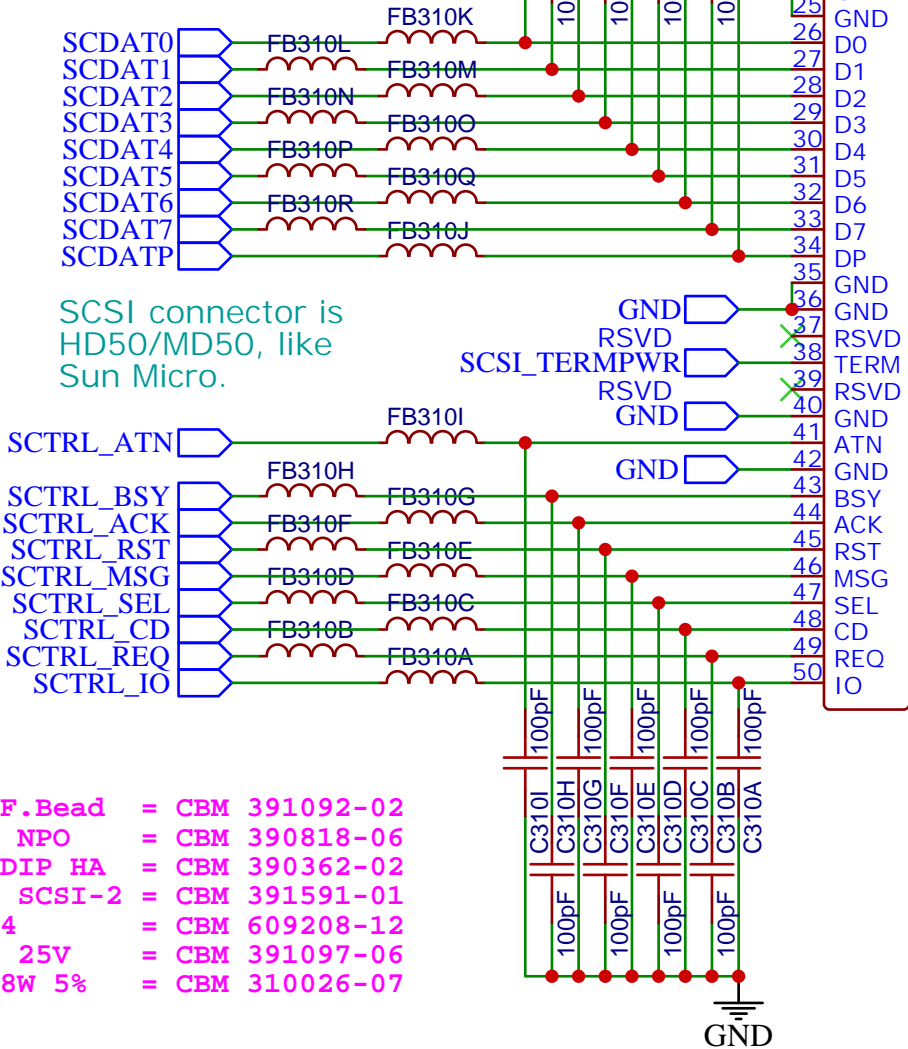


Optional Passive Termination




CN309 SCSI Internal IDC50M
Male 180 IDC

SCSI connector is HD50/MD50, like Sun Micro.



- SCSI F.Bead = CBM 391092-02
- 100pF NPO = CBM 390818-06
- SW1 8DIP HA = CBM 390362-02
- HD50F SCSI-2 = CBM 391591-01
- 74F244 = CBM 609208-12
- 4.7uF 25V = CBM 391097-06
- 1K 1/8W 5% = CBM 310026-07




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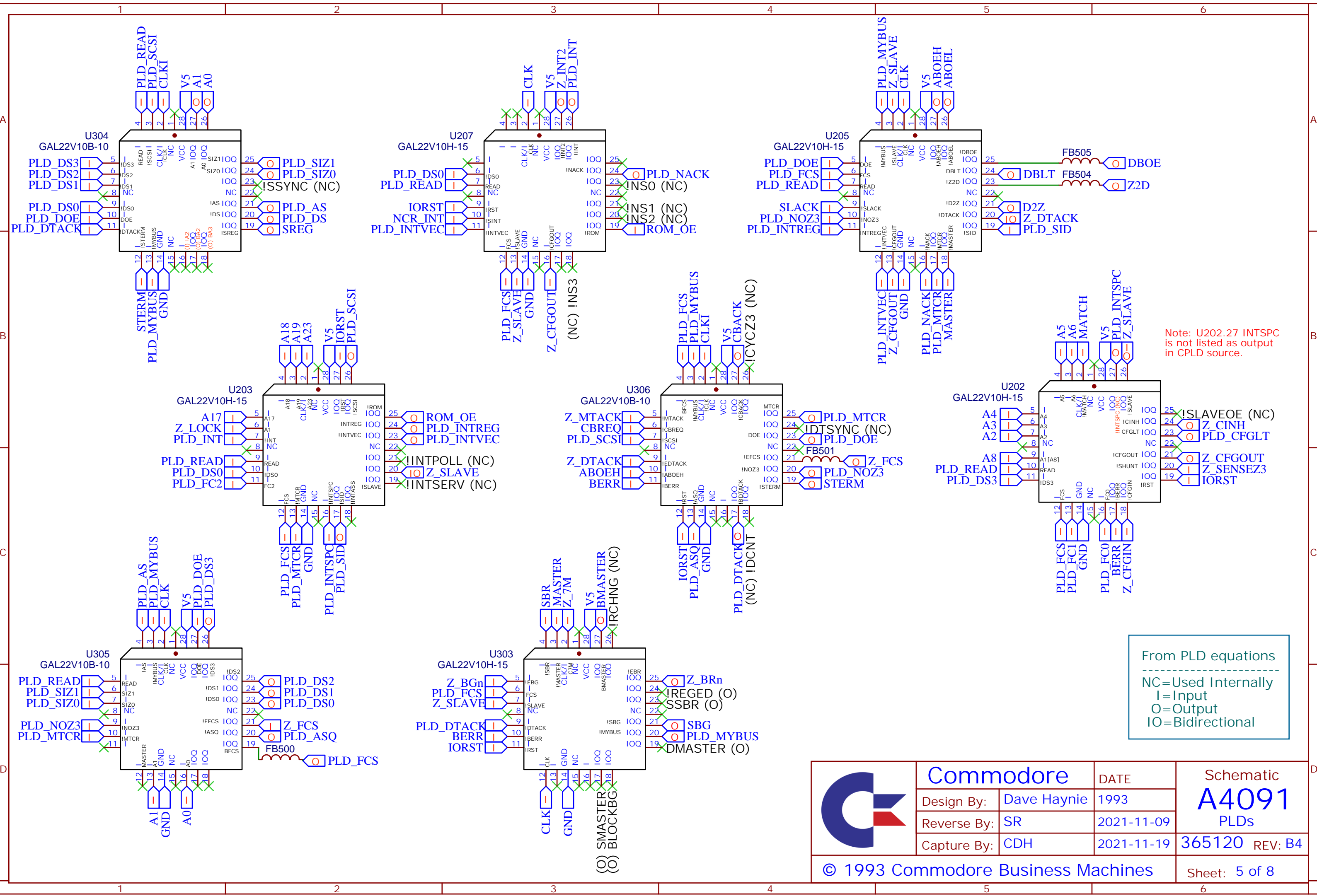
PLD Symbols

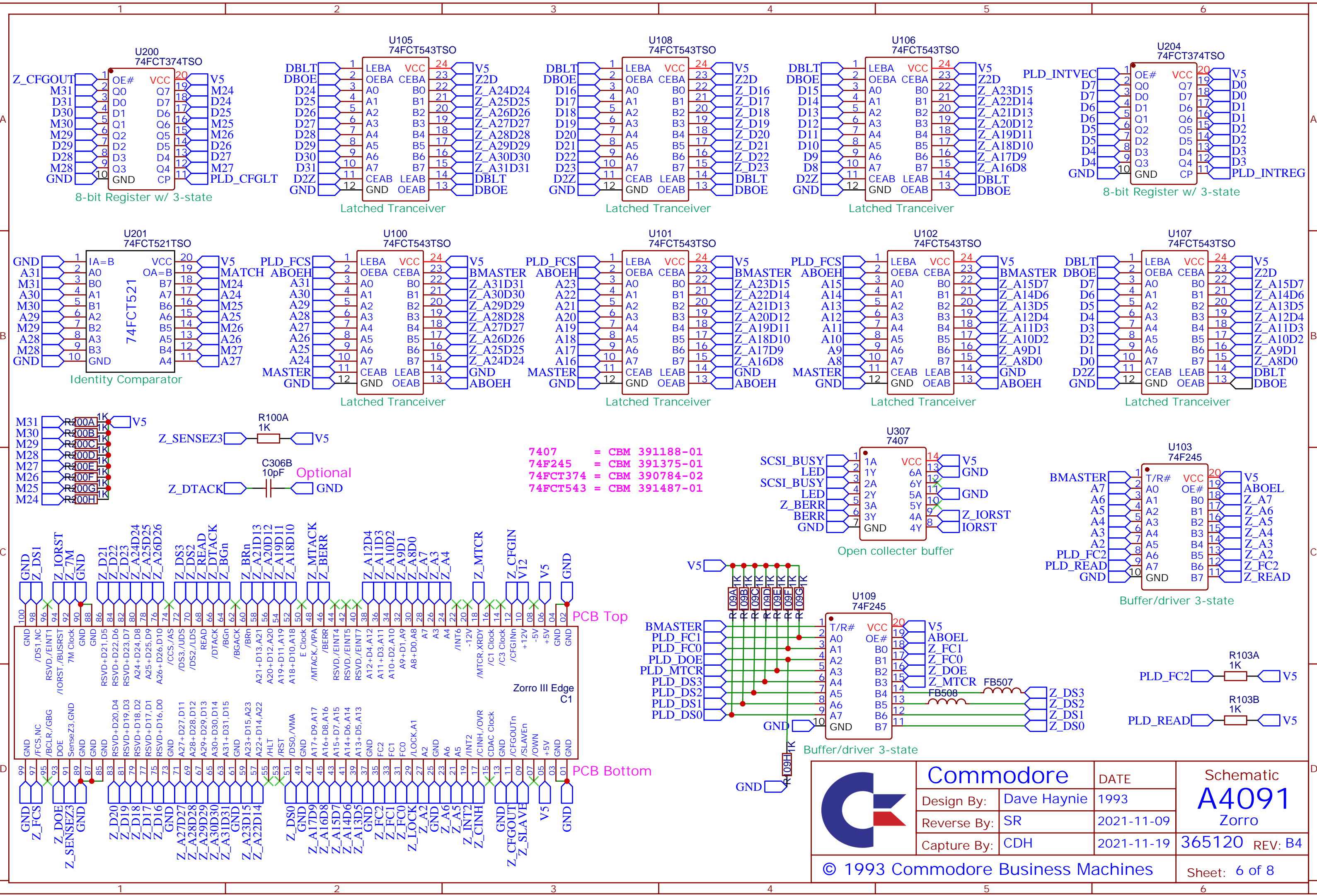
The GAL/PAL devices on page 5 are programmed with gate configurations which consolidate what would be a large number of discrete components. Original Commodore source program files for the A4091 GAL components can be found on the Internet. The below can be used as a quick reference for symbols used in those programming files.

| | | |
|---|--|--|
| A0 - SCSI sizing address | !D2Z - Data is transfered to Z3 bus | !MASTER - SCSI chip owns the A4091 bus |
| A1 - SCSI sizing address _or_ A1/Lock signal | DBLT - Data is latched | !MATCH - Address comparator match |
| A2 - Address A2 | !DCNT - State bit for Z3 stuff (internal) | !MTACK - Z3 slave burst strobe |
| A3 - Address A3 | DMASTER - Master delayed | !MTCR - Z3 multiple transfer burst cycle strobe |
| A4 - Address A4 | !DBOE - Data transfer enable | !MYBUS - The A4091 has the bus |
| A5 - Address A5 | DOE - Z3 Data phase (data output enable) | !NACK - Data acknowledge |
| A6 - Address A6 | !DS0 - Z3 low order data strobe | !NOZ3 - 1: Get off the Z3 bus (stop driving) |
| A8 - Address A8 (known as A1 in U202) | !DS1 - Z3 data strobe | !NS0 - ROM access counter (internal) |
| A17 - Address A17 | !DS2 - Z3 data strobe | !NS1 - ROM access counter (internal) |
| A18 - Address A18 | !DS3 - Z3 high order data strobe | !NS2 - ROM access counter (internal) |
| A19 - Address A19 | !DTACK - Z3 termination cycle | !NS3 - ROM access counter (internal) |
| A23 - Address A23 | !DTSYNC - Synchronizer for DTACK->STERM (internal) | |
| !ABOEL - Low order address transfer enable | !DS - SCSI data strobe | |
| !ABOEH - High order address transfer enable | !EBG - Expansion bus grant | |
| !AS - SCSI address strobe | !EBR - Z3 bus request | |
| !ASQ - Clocked/qualified version of SCSI AS* | !EDTACK - Z3 data acknowledge, on bus | |
| | !EFCS - Z3 cycle strobe for DMA | |
| | | READ - Z3 read strobe (signal/cycle) |
| | | !REGED - A4091 is registered as Z3 master |
| | | RCHNG - Registration is changing (internal) |
| | | !ROM - System ROM access |
| | | !RST - System reset |
| | | !SBG - SCSI bus grant |
| | | !SBR - SCSI bus request |
| | | !SCSI - SCSI chip register address (see SREG) |
| | | !SHUNT - Z2 configuration shunt (0=Z2 1=Z3) |
| | | !SID - SCSI ID jumper access |
| | | SIZ0 - SCSI transfer size |
| | | SIZ1 - SCSI transfer size |
| | | !SINT - SCSI interrupt |
| | | !SLACK - NCR 53C710 slave acknowledge |
| | | !SLAVE - Z3 slave select for interrupt cycles |
| | | !SLAVEOE - Slave output enable |
| | | SMMASTER - Synched master for fall edge |
| | | !SREG - SCSI chip register select (gated by clock) |
| | | SSBR - Synched SCSI bus request |
| | | !Z2D - Data is transfered from Z3 bus |
| | | !SSYNC - SCSI address synchronizer (internal) |
| | | !STERM - SCSI termination |
| BA2 - SCSI burst address | FC0 - CPU read/write function code | |
| BA3 - SCSI burst address | FC1 - CPU read/write function code | |
| !BDTACK - Z3 data acknowledge, buffered | FC2 - CPU read/write function code | |
| !BERR - Z3 Bus error | FCS - Z3 full cycle strobe | |
| BFCS - 1: Buffered cycle strobe | !INT - We generated an interrupt | |
| BFCS - 2: A4091 local Z3 cycle strobe | !INT2 - Zorro bus interrupt 2 | |
| BLOCKBG - after 1st SBG block till end | !INTASS - A vector has been assigned | |
| BMASTER - Buffered/inverted version of MASTER | !INTPOLL - An interrupt polling phase is signaled | |
| C7M - Z3 arbiter clock | INTREC - Interrupt register access | |
| !CBACK - SCSI burst acknowledge | !INTSERV - We're servicing this interrupt phase | |
| !CBREQ - SCSI burst request | !INTSPC - Partially qualified interrupt space (decode) | |
| !CFGIN - Configuration chain input | !INTVEC - An interrupt vector phase is signaled | |
| !CFGOUT - Configuration chain output | | |
| CFGLT - Configuration address latch (on 0->1) | | |
| !CINH - Z3 cache inhibit | | |
| CLK - 1: 25MHz NCR 53C710 bus clock | | |
| !CLK - 2: 25MHz system clock | | |
| !CYCZ3 - On-bus Z3 cycle (internal) | | |



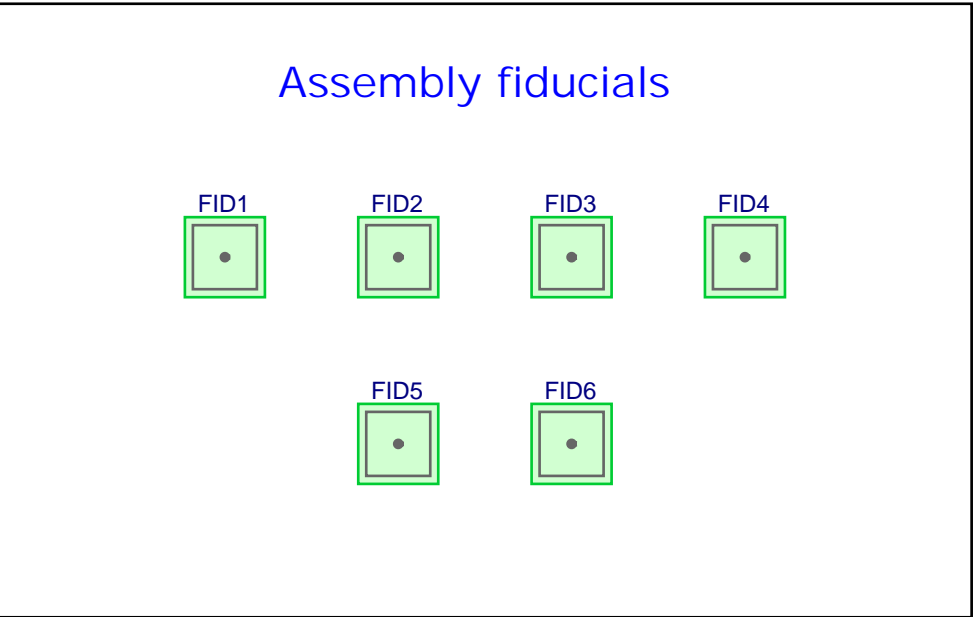
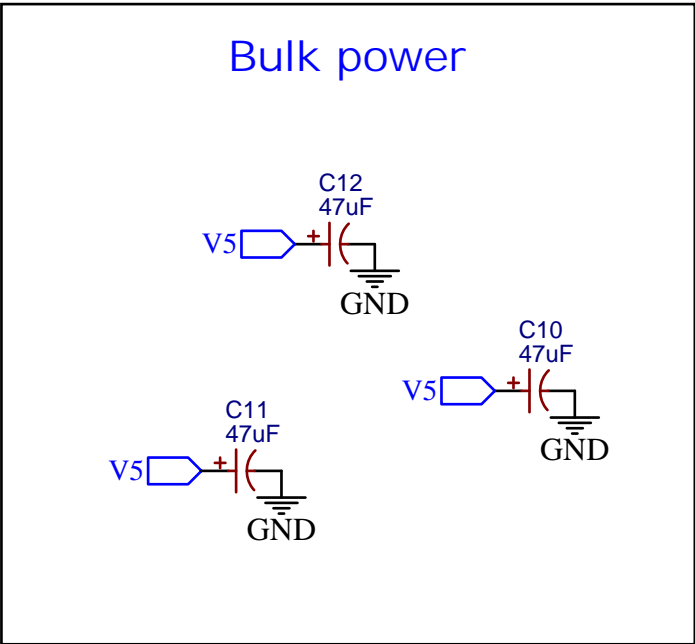
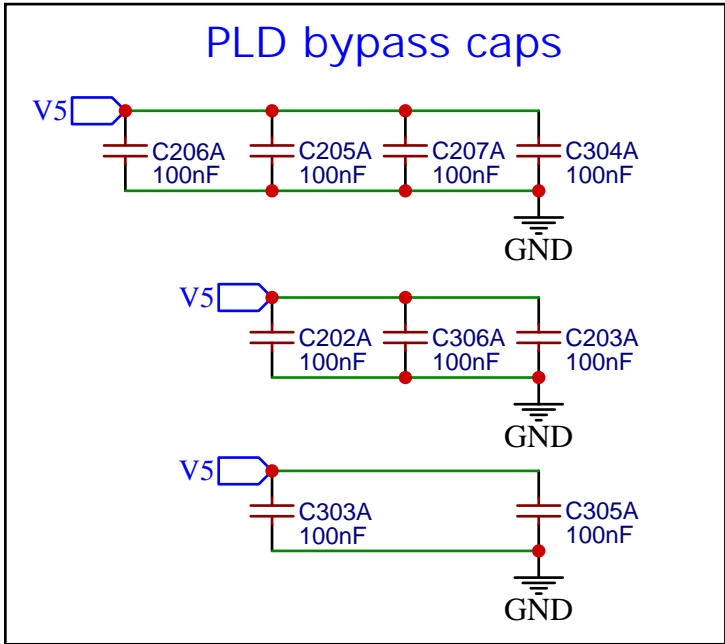
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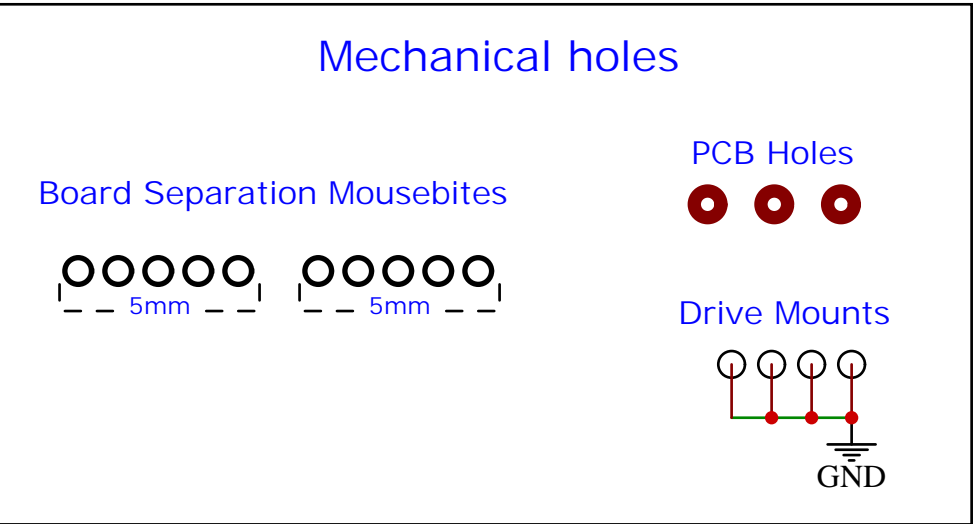
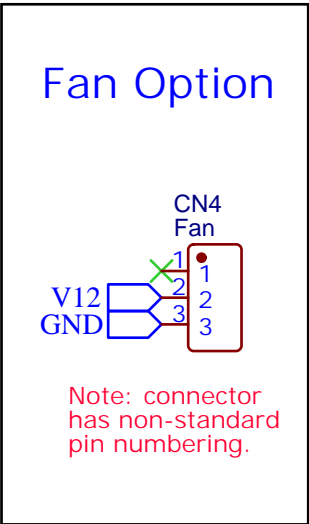
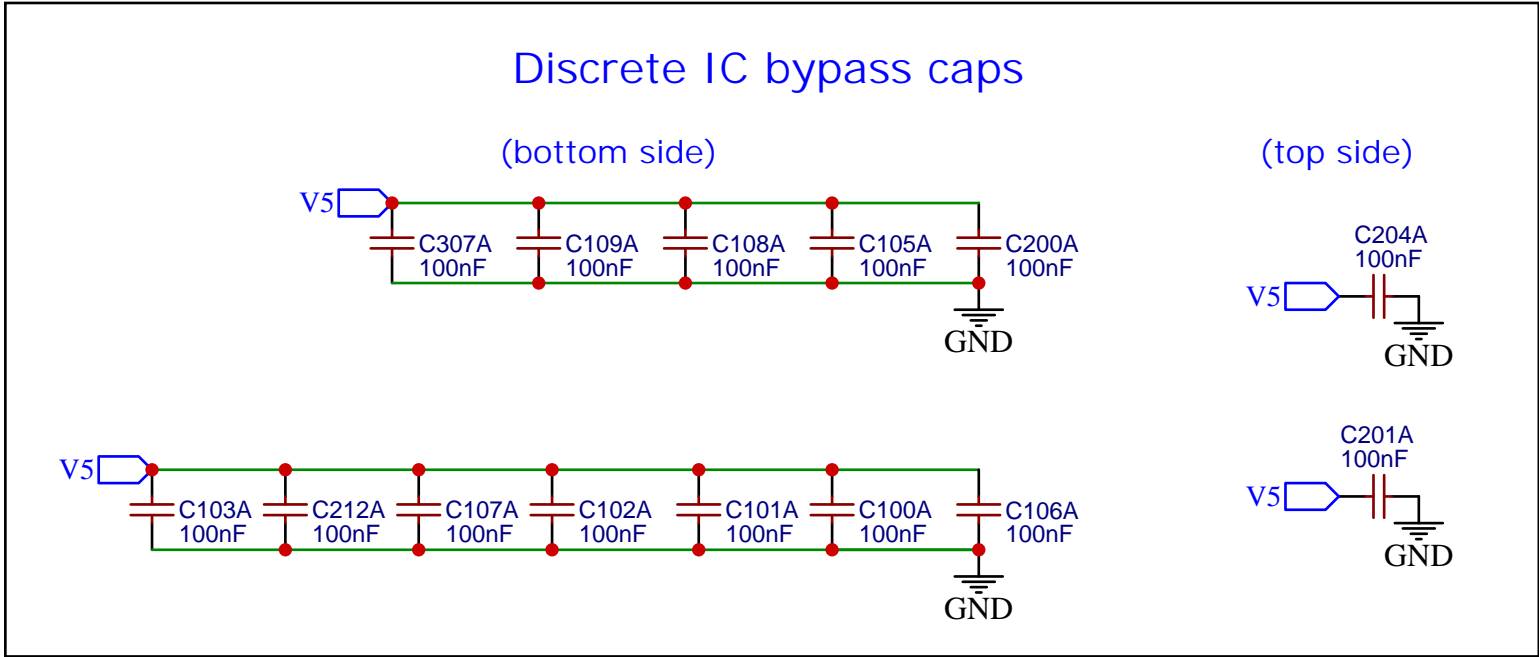
A

A



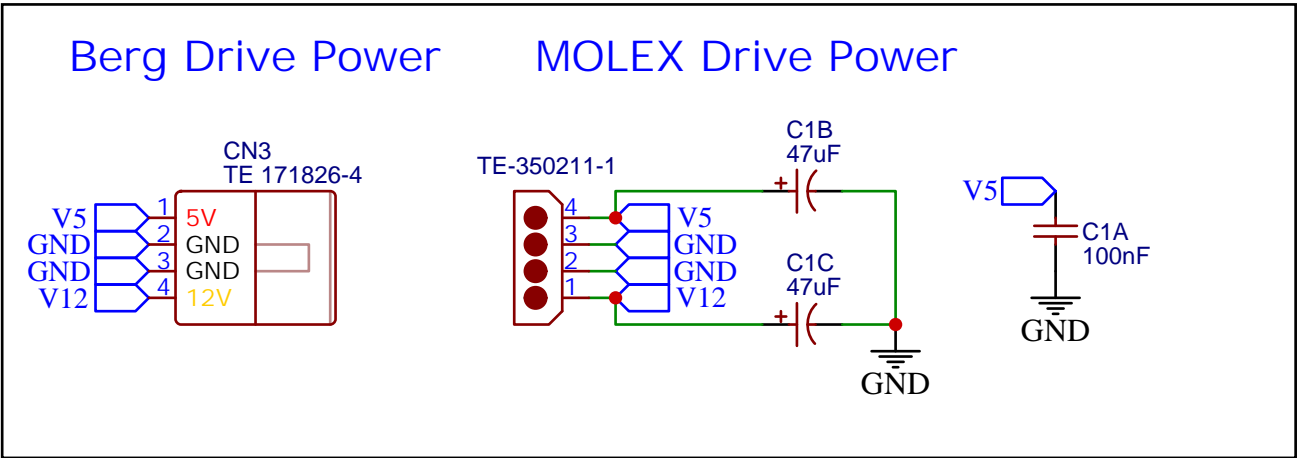
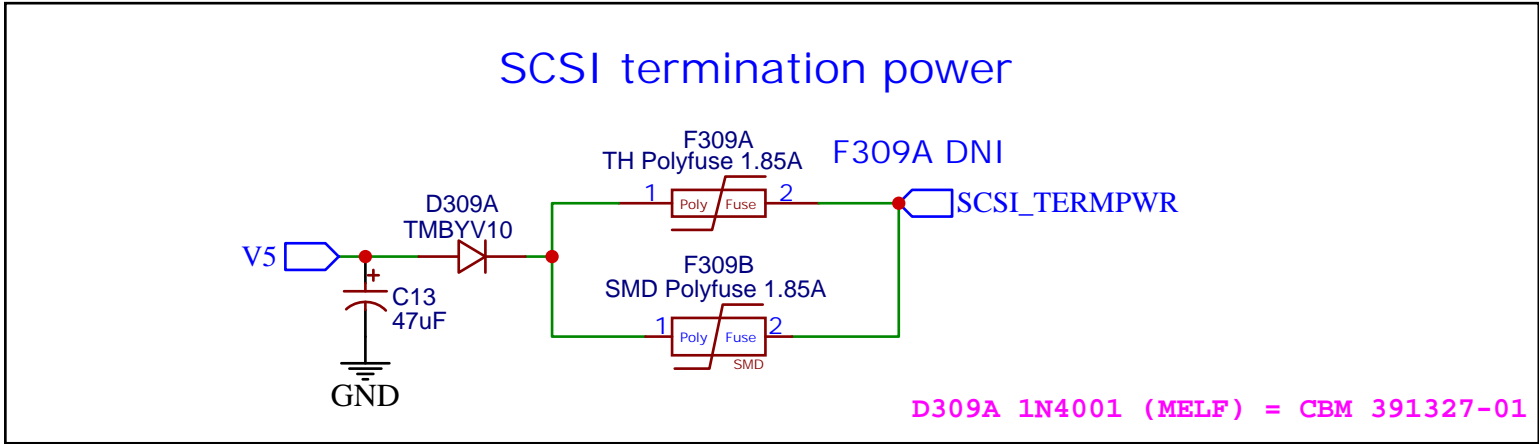
B

B



C

C

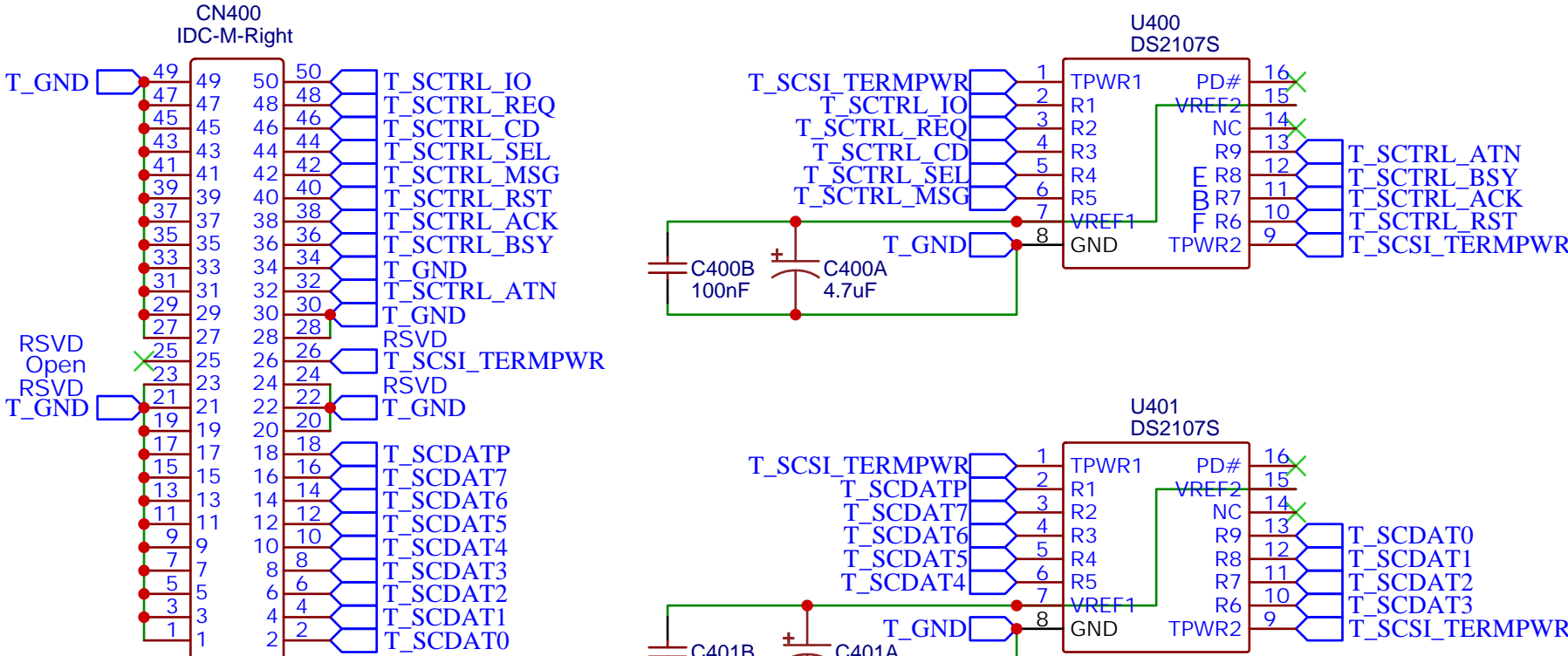


D

D

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SCSI Active Terminator cut-out board



Male right angle IDC

Board Holes



Fiducials

