Commodore A4091
Rev B Advanced SCSI II Controller Board

This Zorro III board was originally designed and sold by Commodore, which did a single run of the Rev A design before shelving it. Commodore was running out of money at the time and didn't want to risk a second production run. The Rev B design was given to DKB Software for production, marketing, sales, distribution, and support.

Features:

- Boot ROM
- NCR 53C710 SCSI II controller
- 50 pin internal connector
- 50 pin external SCSI2 connector
- 3.5" hard drive mounts on the card
- Active SCSI termination
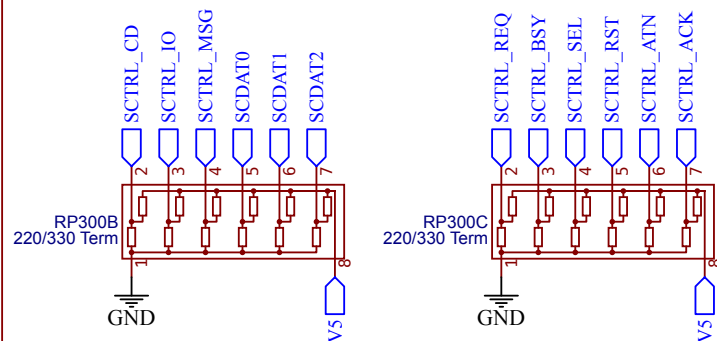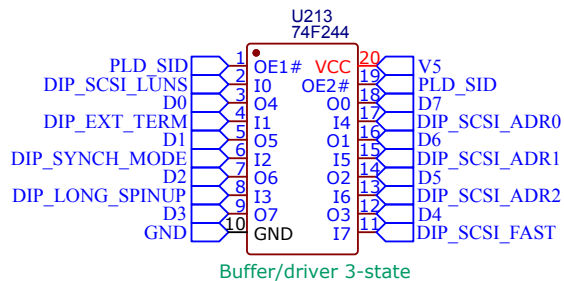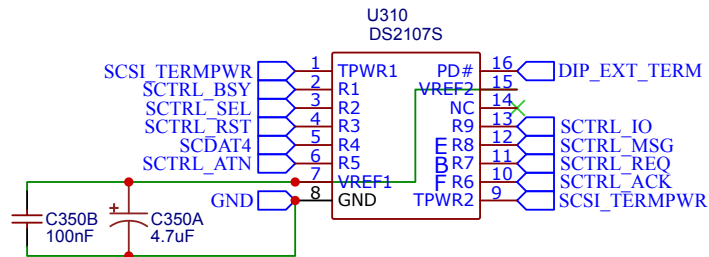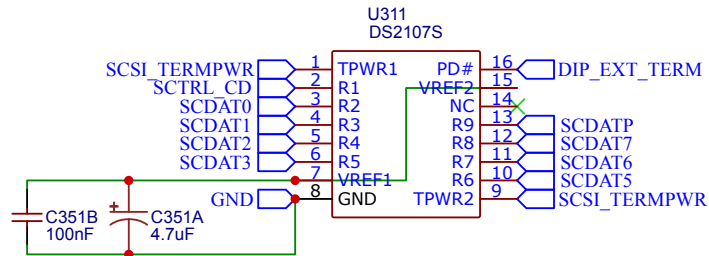- Zorro III bus support

Caveats:

- Requires Buster 11
- Does not work with with A3640 Rev 3.0
- No RAM option
- No wide SCSI support

The Commodore A4091 was reverse-engineered by Stefan Reinauer and Chris Hooper.
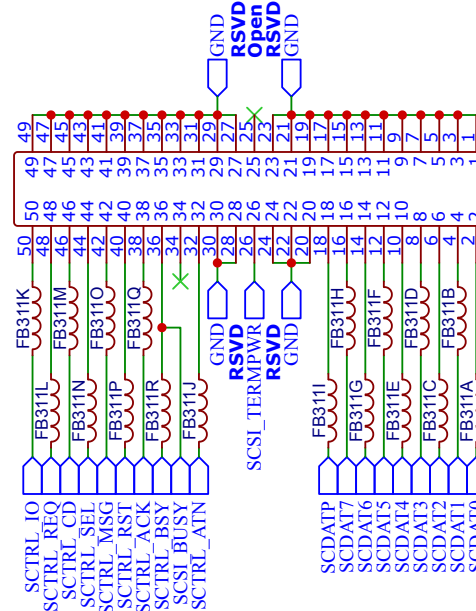
ReA4091 Rev 4   2023-05-15

Active Termination

Internal 2x25 Connector

U311
DS2107S

SCSI_TERMPWR — 1 TPWR1 PD# 16 — DIP_EXT_TERM
SCTRL_CD — 2 R1 VREF2 15
SCDAT0 — 3 R2 NC 14
SCDAT1 — 4 R3 R9 13 — SCDATP
SCDAT2 — 5 R4 R8 12 — SCDAT7
SCDAT3 — 6 R5 R7 11 — SCDAT6
— 7 VREF1 R6 10 — SCDAT5
GND — 8 GND TPWR2 9 — SCSI_TERMPWR

C351B 100nF   C351A 4.7uF

U310
DS2107S

SCSI_TERMPWR — 1 TPWR1 PD# 16 — DIP_EXT_TERM
SCTRL_BSY — 2 R1 VREF2 15
SCTRL_SEL — 3 R2 NC 14
SCTRL_RST — 4 R3 R9 13 — SCTRL_IO
SCDAT4 — 5 R4 R8 12 — SCTRL_MSG
SCTRL_ATN — 6 R5 R7 11 — SCTRL_REQ
— 7 VREF1 R6 10 — SCTRL_ACK
GND — 8 GND TPWR2 9 — SCSI_TERMPWR

C350B 100nF   C350A 4.7uF

CN310
SCSI External MD50F

Commodore 391092-02 Ferrite Bead
60 Ohm @ 100Mhz, 200mA 1206

GND RSVD Open RSVD GND

CN309
SCSI Internal IDC50M

Male 180 IDC

Male 180 IDC

GND RSVD SCSI_TERMPWR RSVD GND

FB311K FB311M FB311O FB311Q FB311H FB311F FB311D FB311B
FB311L FB311N FB311P FB311R FB311J FB311I FB311G FB311E FB311C FB311A

SCTRL_IO SCTRL_REQ SCTRL_CD SCTRL_SEL SCTRL_MSG SCTRL_ACK SCTRL_BSY SCSI_BUSY SCTRL_ATN
SCDATP SCDAT7 SCDAT6 SCDAT5 SCDAT4 SCDAT3 SCDAT2 SCDAT1 SCDAT0

SCSI connector is HD50/MD50, like Sun Micro.

GND RSVD SCSI_TERMPWR RSVD GND

C310K C310L C310M C310N C310O C310P C310Q C310R C310J 100pF

SCDAT0 — FB310L FB310K — D0
SCDAT1 — FB310M — D1
SCDAT2 — FB310N — D2
SCDAT3 — FB310O — D3
SCDAT4 — FB310P — D4
SCDAT5 — FB310Q — D5
SCDAT6 — FB310R — D6
SCDAT7 — FB310J — D7
SCDATP — DP

SCTRL_ATN — FB310I — ATN
SCTRL_BSY — FB310H FB310G — BSY
SCTRL_ACK — FB310F — ACK
SCTRL_RST — FB310E — RST
SCTRL_MSG — FB310D — MSG
SCTRL_SEL — FB310C — SEL
SCTRL_CD — FB310B — CD
SCTRL_REQ — FB310A — REQ
SCTRL_IO — IO

C310I C310H C310G C310E C310D C310C C310B C310A 100pF

External HD50 Connector

External HD50 Connector

1 GND
2 GND
3 GND
4 GND
5 GND
6 GND
7 GND
8 GND
9 GND
10 GND
11 GND
12 NC
13 NC
14 NC
15 NC
16 GND
17 GND
18 GND
19 GND
20 GND
21 GND
22 GND
23 GND
24 GND
25 GND
26 D0
27 D1
28 D2
29 D3
30 D4
31 D5
32 D6
33 D7
34 DP
35 GND
36 GND
37 RSVD
38 TERM
39 RSVD
40 GND
41 ATN
42 GND
43 BSY
44 ACK
45 RST
46 MSG
47 SEL
48 CD
49 REQ
50 IO

External DIP Switch

V5

R212A 1K R212C 1K R212E 1K R212G 1K
R212B 1K R212D 1K R212F 1K R212H 1K

SW1
DA-08RP

DIP_SCSI_LUNS — 8 ... 9 — RSVD
DIP_EXT_TERM — 7 ... 10 — EXT_TERM
DIP_SYNCH_MODE — 6 ... 11 — SYNCH_MODE
DIP_LONG_SPINUP — 5 ... 12 — LONG_SPINUP
DIP_SCSI_FAST — 4 ... 13 — SCSI_FAST
DIP_SCSI_ADR2 — 3 ... 14 — SCSI_ADR2
DIP_SCSI_ADR1 — 2 ... 15 — SCSI_ADR1
DIP_SCSI_ADR0 — 1 ... 16 — SCSI_ADR0

GND

U213
74F244

PLD_SID — 1 OE1# VCC 20 — V5
DIP_SCSI_LUNS — 2 I0 OE2# 19 — PLD_SID
— 3 O4 O0 18 — D7
DIP_EXT_TERM — 4 I1 I4 17 — DIP_SCSI_ADR0
— 5 O5 O1 16 — D6
DIP_SYNCH_MODE — 6 I2 I5 15 — DIP_SCSI_ADR1
— 7 O6 O2 14 — D5
DIP_LONG_SPINUP — 8 I3 I6 13 — DIP_SCSI_ADR2
— 9 O7 O3 12 — D4
GND — 10 GND I7 11 — DIP_SCSI_FAST

Buffer/driver 3-state

Optional Passive Termination

SCSI F.Bead = CBM 391092-02
100pF NPO = CBM 390818-06
SW1 8DIP HA = CBM 390362-02
HD50F SCSI-2 = CBM 391591-01
74F244 = CBM 609208-12
4.7uF 25V = CBM 391097-06
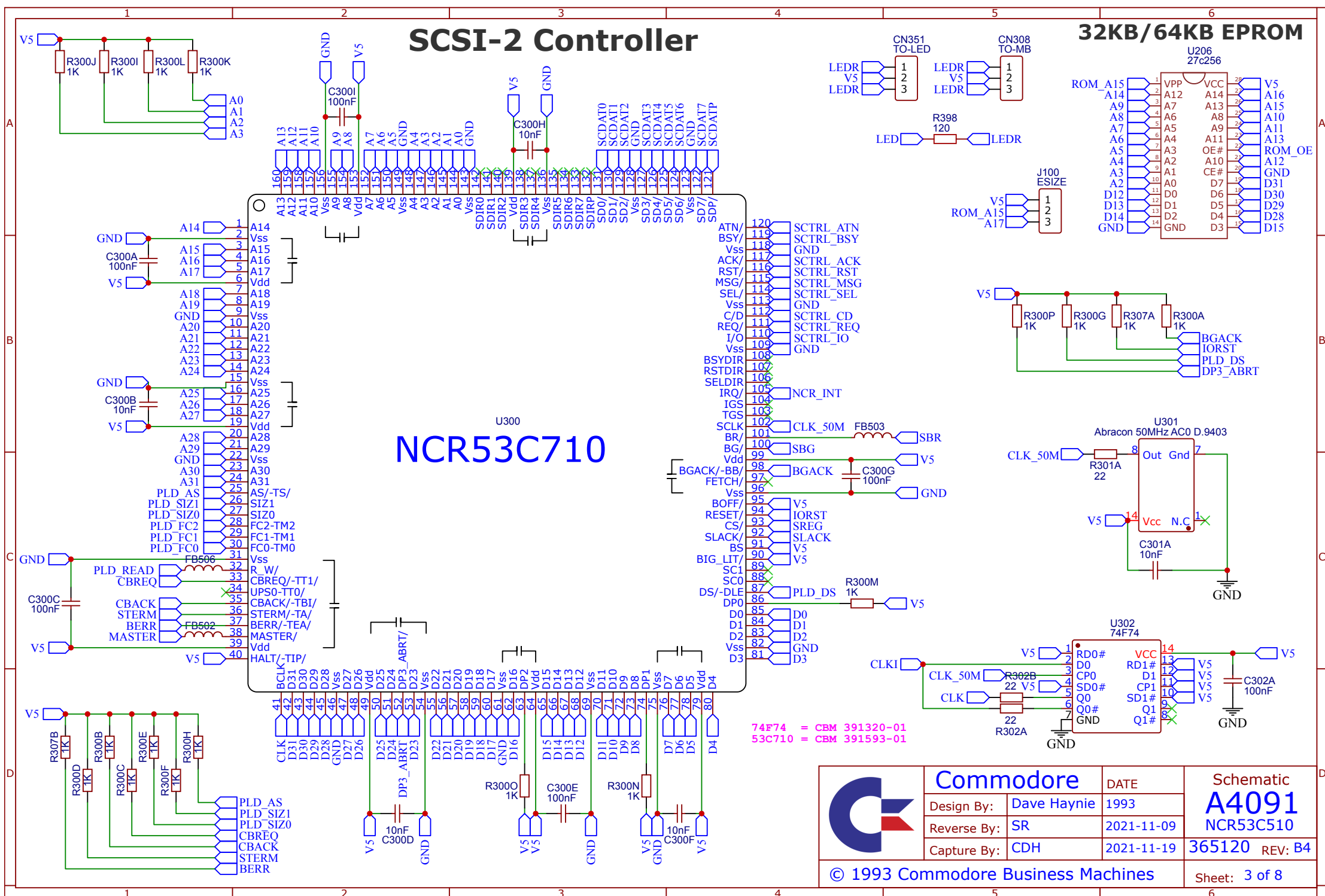**1K 1/8W 5% = CBM 310026-07**

RP300B
220/330 Term

SCTRL_CD SCTRL_IO SCTRL_MSG SCDAT0 SCDAT1 SCDAT2

RP300C
220/330 Term

SCTRL_REQ SCTRL_BSY SCTRL_SEL SCTRL_RST SCTRL_ATN SCTRL_ACK

RP300A
220/330 Term

SCDAT3 SCDAT4 SCDAT5 SCDAT6 SCDAT7 SCDATP

GND   V5   GND   V5   GND

U300
NCR53C710

U206
27c256

CN351
TO-LED

CN308
TO-MB

J100
ESIZE

U301
Abracon 50MHz AC0 D.9403

U302
74F74

74F74 = CBM 391320-01
53C710 = CBM 391593-01

Commodore	DATE	Schematic
Design By: Dave Haynie	1993	A4091
Reverse By: SR	2021-11-09	NCR53C510
Capture By: CDH	2021-11-19	365120 REV: B4
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PLD Symbols

The GAL/PAL devices on page 5 are programmed with gate configurations which consolidate what would be a large number of discrete components. Original Commodore source program files for the A4091 GAL components can be found on the Internet. The below can be used as a quick reference for symbols used in those programming files.

A0 - SCSI sizing address
A1 - SCSI sizing address _or_ A1/Lock signal
A2 - Address A2
A3 - Address A3
A4 - Address A4
A5 - Address A5
A6 - Address A6
A8 - Address A8 (known as A1 in U202)
A17 - Address A17
A18 - Address A18
A19 - Address A19
A23 - Address A23
!ABOEL - Low order address transfer enable
!ABOEH - High order address transfer enable
!AS - SCSI address strobe
!ASQ - Clocked/qualified version of SCSI AS*

BA2 - SCSI burst address
BA3 - SCSI burst address
!BDTACK - Z3 data acknowledge, buffered
!BERR - Z3 Bus error
BFCS - 1:Buffered cycle strobe
BFCS - 2:A4091 local Z3 cycle strobe
BLOCKBG - after 1st SBG block till end
BMASTER - Buffered/inverted version of MASTER
C7M - Z3 arbiter clock
!CBACK - SCSI burst acknowledge
!CBREQ - SCSI burst request
!CFGIN - Configuration chain input
!CFGOUT - Configuration chain output
CFGLT - Configuration address latch (on 0->1)
!CINH - Z3 cache inhibit
CLK - 1:25MHz NCR 53C710 bus clock
!CLK - 2:25MHz system clock
!CYCZ3 - On-bus Z3 cycle (internal)

!D2Z - Data is transfered to Z3 bus
DBLT - Data is latched
!DCNT - State bit for Z3 stuff (internal)
DMASTER - Master delayed
!DBOE - Data transfer enable
DOE - Z3 Data phase (data output enable)
!DS0 - Z3 low order data strobe
!DS1 - Z3 data strobe
!DS2 - Z3 data strobe
!DS3 - Z3 high order data strobe
!DTACK - Z3 termination cycle
!DTSYNC - Synchronizer for DTACK->STERM (internal)
!DS - SCSI data strobe
!EBG - Expansion bus grant
!EBR - Z3 bus request
!EDTACK - Z3 data acknowledge, on bus
!EFCS - Z3 cycle strobe for DMA

FC0 - CPU read/write function code
FC1 - CPU read/write function code
FC2 - CPU read/write function code
FCS - Z3 full cycle strobe
!INT - We generated an interrupt
!INT2 - Zorro bus interrupt 2
!INTASS - A vector has been assigned
!INTPOLL - An interrupt polling phase is signaled
INTREC - Interrupt register access
!INTSERV - We're servicing this interrupt phase
!INTSPC - Partially qualified interrupt space (decode)
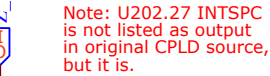!INTVEC - An interrupt vector phase is signaled

!MASTER - SCSI chip owns the A4091 bus
!MATCH - Address comparator match
!MTACK - Z3 slave burst strobe
!MTCR - Z3 multiple transfer burst cycle strobe
!MYBUS - The A4091 has the bus
!NACK - Data acknowledge
!NOZ3 - 1:Get off the Z3 bus (stop driving)
!NS0 - ROM access counter (internal)
!NS1 - ROM access counter (internal)
!NS2 - ROM access counter (internal)
!NS3 - ROM access counter (internal)

READ - Z3 read strobe (signal/cycle)
!REGED - A4091 is registered as Z3 master
RCHNG - Registration is changing (internal)
!ROM - System ROM access
!RST - System reset
!SBG - SCSI bus grant
!SBR - SCSI bus request
!SCSI - SCSI chip register address (see SREG)
!SHUNT - Z2 configuration shunt (0=Z2 1=Z3)
!SID - SCSI ID jumper access
SIZ0 - SCSI transfer size
SIZ1 - SCSI transfer size
!SINT - SCSI interrupt
!SLACK - NCR 53C710 slave acknowledge
!SLAVE - Z3 slave select for interrupt cycles
!SLAVEOE - Slave output enable
SMASTER - Synched master for fall edge
!SREG - SCSI chip register select (gated by clock)
SSBR - Synched SCSI bus request
!Z2D - Data is transfered from Z3 bus
!SSYNC - SCSI address synchronizer (internal)
!STERM - SCSI termination

	Commodore	DATE		Schematic
Design By:	Dave Haynie	1993		A4091
Reverse By:	SR	2021-11-09		PLDs
Capture By:	CDH	2021-11-19	365120 REV: B4	

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U304 — GAL22V10B-10

Top: PLD_READ, PLD_SCSI, CLKT, V5, A1, A0

PLD_DS3, PLD_DS2, PLD_DS1, NC, PLD_DS0, PLD_DOE, PLD_DTACK

!SSYNC (NC)
25 O PLD_SIZ1
24 O PLD_SIZ0
22 O !SSYNC (NC)
21 O PLD_AS
20 O PLD_DS
19 O SREG

Bottom: STERM, PLD_MYBUS, GND

U207 — GAL22V10H-15

Top: CLK, V5, Z_INT2, PLD_INT

PLD_DS0, PLD_READ, IORST, NCR_INT, PLD_INTVEC

25 !NACK
24 O PLD_NACK
23 INS0 (NC)
21 INS1 (NC)
20 INS2 (NC)
19 ROM_OE

Bottom: PLD_FCS, Z_SLAVE, GND, Z_CFGOUT   (NC) !INS3

U205 — GAL22V10H-15

Top: PLD_MYBUS, Z_SLAVE, CLK, V5, ABOEH, ABOEL

PLD_DOE, PLD_FCS, PLD_READ, NC, SLACK, PLD_NOZ3, PLD_INTREG

25 O DBOE FB505
24 O DBLT
23 Z2D FB504
22 NC
21 O D2Z
20 IO Z_DTACK
19 PLD_SID

Bottom: PLD_INTVEC, Z_CFGOUT, GND, PLD_NACK, PLD_MTCR, MASTER

Note: U202.27 INTSPC is not listed as output in original CPLD source, but it is.

U203 — GAL22V10H-15

Top: A18, A19, A23, V5, IORST, PLD_SCSI

A17, Z_LOCK, PLD_INT, NC, PLD_READ, PLD_DS0, PLD_FC2

25 O ROM_OE
24 O PLD_INTREG
23 O PLD_INTVEC
22 NC
21 !INTPOLL (NC)
20 IO Z_SLAVE
19 !INTSERV (NC)

Bottom: PLD_FCS, PLD_MTCR, GND, PLD_INTSPC, PLD_SID   (NC) !INTASS

U306 — GAL22V10B-10

Top: PLD_FCS, PLD_MYBUS, CLKT, V5, CBACK

Z_MTACK, CBREQ, PLD_SCSI, NC, Z_DTACK, ABOEH, BERR

25 O PLD_MTCR
24 !DTSYNC (NC)
22 O PLD_DOE
21 FB501
20 O Z_FCS
19 O STERM

Bottom: IORST, PLD_ASQ, GND, PLD_DTACK   (NC) !DCNT

!CYCZ3 (NC)

U202 — GAL22V10H-15

Top: A5, A6, MATCH, V5, PLD_INTSPC, Z_SLAVE

A4, A3, A2, NC, A8, PLD_READ, PLD_DS3

25 !SLAVEOE (NC)
23 Z_CINH
23 O PLD_CFGLT
21 !CFGOUT (NC)
20 IO Z_CFGOUT
19 Z_SENSEZ3

Bottom: PLD_FCS, PLD_FC1, GND, PLD_FC0, BERR, Z_CFGIN   IORST

U305 — GAL22V10B-10

Top: PLD_AS, PLD_MYBUS, CLK, V5, PLD_DOE, PLD_DS3

PLD_READ, PLD_SIZ1, PLD_SIZ0, NC, PLD_NOZ3, PLD_MTCR

25 O PLD_DS2
23 O PLD_DS1
22 O PLD_DS0
22 NC
20 Z_FCS
19 O PLD_ASQ   FB500
     O PLD_FCS

Bottom: A1, GND, A0

U303 — GAL22V10H-15

Top: SBR, MASTER, Z_7M, V5, BMASTER

Z_BGn, PLD_FCS, Z_SLAVE, NC, PLD_DTACK, BERR, IORST

25 Z_BRn
24 !REGED (O)
     SSBR (O)
22 NC
21 O SBG
19 PLD_MYBUS

!RCHNG (NC)

Bottom: CLK, GND   (O) SMASTER (O) BLOCKBG

From PLD equations

NC=Used Internally
I=Input
O=Output
IO=Bidirectional

U200
74FCT374TSO
8-bit Register w/ 3-state

U105
74FCT543TSO
Latched Tranceiver

U108
74FCT543TSO
Latched Tranceiver

U106
74FCT543TSO
Latched Tranceiver

U204
74FCT374TSO
8-bit Register w/ 3-state

U201
74FCT521TSO
74FCT521
Identity Comparator

U100
74FCT543TSO
Latched Tranceiver

U101
74FCT543TSO
Latched Tranceiver

U102
74FCT543TSO
Latched Tranceiver

U107
74FCT543TSO
Latched Tranceiver

U307
7407
Open collecter buffer

U103
74F245
Buffer/driver 3-state

U109
74F245
Buffer/driver 3-state

7407   = CBM 391188-01
74F245   = CBM 391375-01
74FCT374 = CBM 390784-02
74FCT543 = CBM 391487-01

R100A 1K
C306B 10pF Optional
Z_SENSEZ3
Z_DTACK

R103A 1K
PLD_FC2 V5
R103B 1K
PLD_READ V5

Zorro III Edge
C1

PCB Top
PCB Bottom

PLD bypass caps

V5

C206A 100nF — C205A 100nF — C207A 100nF — C304A 100nF
GND

V5

C202A 100nF — C306A 100nF — C203A 100nF
GND

V5

C303A 100nF — C305A 100nF
GND

Bulk power

V5 — C12 47uF — GND

V5 — C10 47uF — GND

V5 — C11 47uF — GND

Assembly fiducials

FID1 FID2 FID3 FID4

FID5 FID6

Discrete IC bypass caps

(bottom side)

V5

C307A 100nF — C109A 100nF — C108A 100nF — C105A 100nF — C200A 100nF
GND

V5

C103A 100nF — C212A 100nF — C107A 100nF — C102A 100nF — C101A 100nF — C100A 100nF — C106A 100nF
GND

(top side)

V5 — C204A 100nF — GND

V5 — C201A 100nF — GND

Fan Option

CN4
Fan

V12
GND

1
2
3

Note: connector
has non-standard
pin numbering.

Mechanical holes

Board Separation Mousebites

ooooo   ooooo
5mm   5mm

PCB Holes

Drive Mounts

GND

Berg Drive Power

CN3
TE 171826-4

V5   1   5V
GND   2   GND
GND   3   GND
V12   4   12V

MOLEX Drive Power

TE-350211-1

4   V5   C1B 47uF
3   GND
2   GND   C1C 47uF
1   V12

GND

V5 — C1A 100nF — GND

SCSI termination power

V5 — D309A TMBYV10 —

F309A
TH Polyfuse 1.85A
1 Poly Fuse 2

F309A DNI

F309B
SMD Polyfuse 1.85A
1 Poly Fuse 2
SMD

SCSI_TERMPWR

C13 47uF
GND

D309A 1N4001 (MELF) = CBM 391327-01

Commodore

	DATE	
Design By: Dave Haynie	1993	
Reverse By: SR	2021-11-09	
Capture By: CDH	2021-11-19	
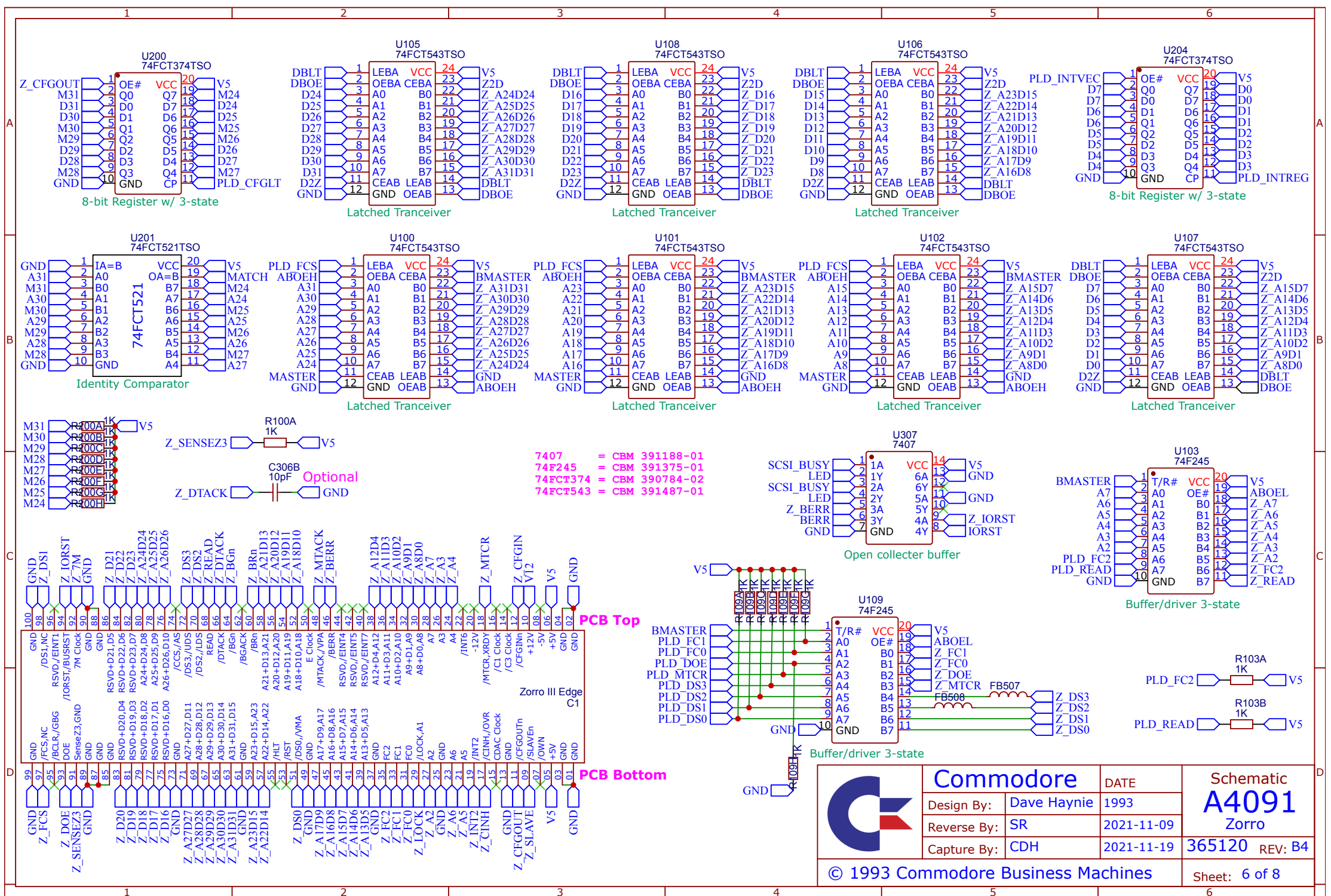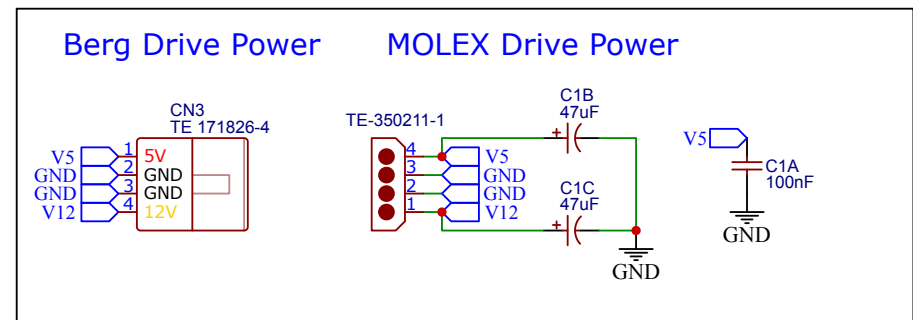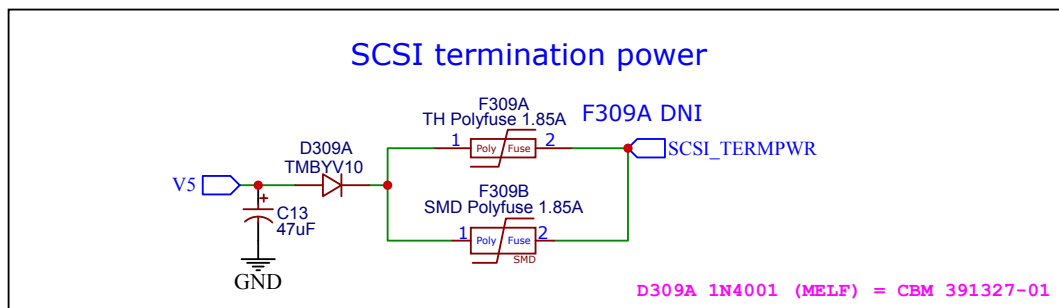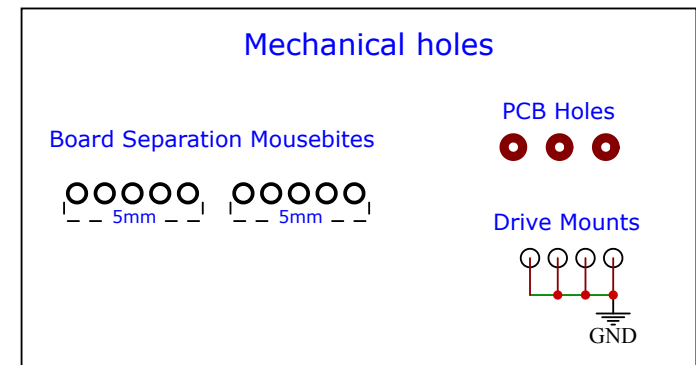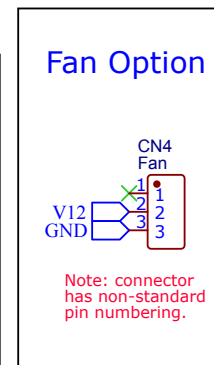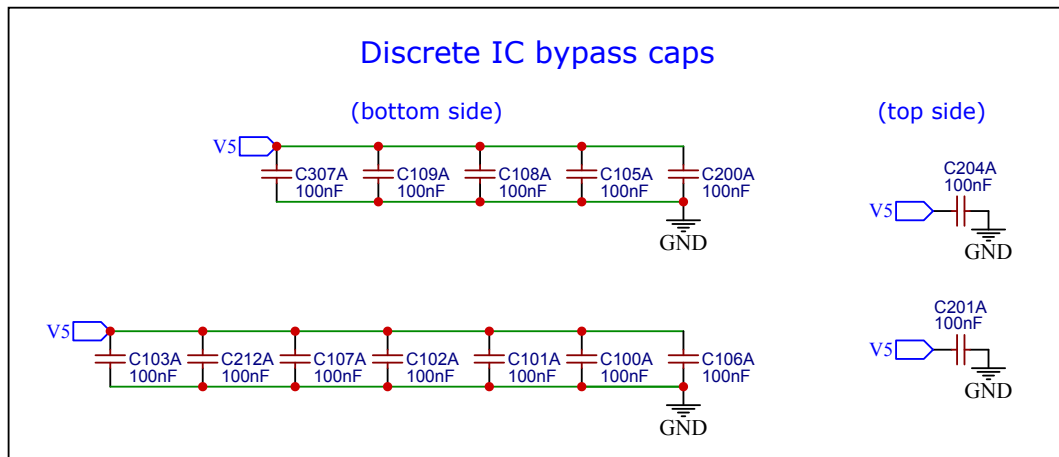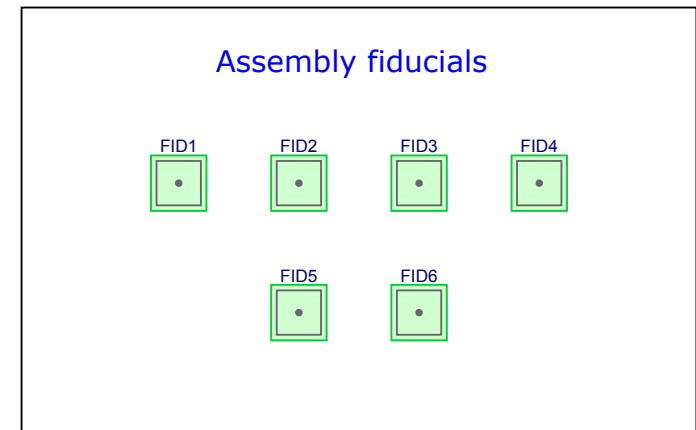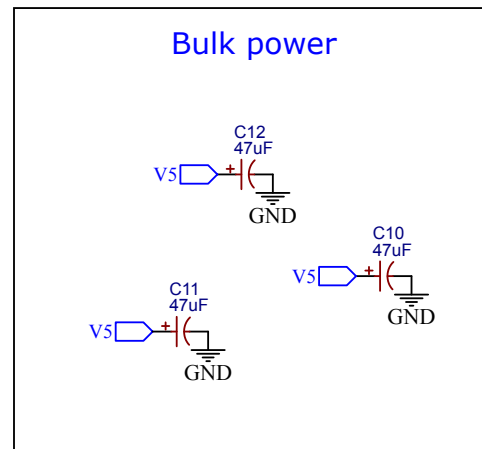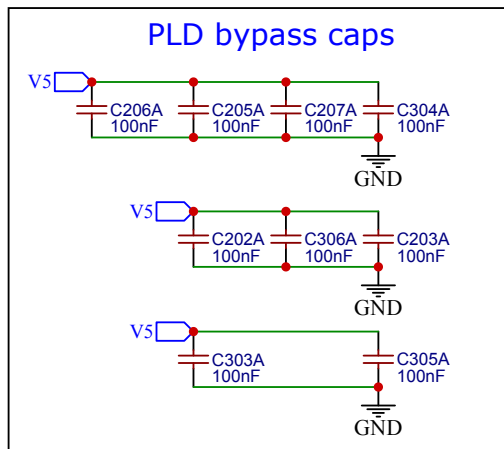
Schematic
A4091
Power
365120 REV: B4

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Sheet: 7 of 8

SCSI Active Terminator cut-out board

CN400
IDC-M-Right

T_GND — 49 | 50 — T_SCTRL_IO
47 | 48 — T_SCTRL_REQ
45 | 46 — T_SCTRL_CD
43 | 44 — T_SCTRL_SEL
41 | 42 — T_SCTRL_MSG
39 | 40 — T_SCTRL_RST
37 | 38 — T_SCTRL_ACK
35 | 36 — T_SCTRL_BSY
33 | 34 — T_GND
31 | 32 — T_SCTRL_ATN
29 | 30 — T_GND
27 | 28 — RSVD
RSVD Open — 25 | 26 — T_SCSI_TERMPWR
RSVD — 23 | 24 — **RSVD**
T_GND — 21 | 22 — T_GND
19 | 20
17 | 18 — T_SCDATP
15 | 16 — T_SCDAT7
13 | 14 — T_SCDAT6
11 | 12 — T_SCDAT5
9 | 10 — T_SCDAT4
7 | 8 — T_SCDAT3
5 | 6 — T_SCDAT2
3 | 4 — T_SCDAT1
1 | 2 — T_SCDAT0

Male right angle IDC

U400
DS2107S

T_SCSI_TERMPWR — 1 — TPWR1 | PD# — 16
T_SCTRL_IO — 2 — R1 | VREF2 — 15
T_SCTRL_REQ — 3 — R2 | NC — 14
T_SCTRL_CD — 4 — R3 | R9 — 13 — T_SCTRL_ATN
T_SCTRL_SEL — 5 — R4 | E R8 — 12 — T_SCTRL_BSY
T_SCTRL_MSG — 6 — R5 | B R7 — 11 — T_SCTRL_ACK
7 — VREF1 | F R6 — 10 — T_SCTRL_RST
T_GND — 8 — GND | TPWR2 — 9 — T_SCSI_TERMPWR

C400B 100nF
C400A 4.7uF
T_GND

U401
DS2107S

T_SCSI_TERMPWR — 1 — TPWR1 | PD# — 16
T_SCDATP — 2 — R1 | VREF2 — 15
T_SCDAT7 — 3 — R2 | NC — 14
T_SCDAT6 — 4 — R3 | R9 — 13 — T_SCDAT0
T_SCDAT5 — 5 — R4 | R8 — 12 — T_SCDAT1
T_SCDAT4 — 6 — R5 | R7 — 11 — T_SCDAT2
7 — VREF1 | R6 — 10 — T_SCDAT3
T_GND — 8 — GND | TPWR2 — 9 — T_SCSI_TERMPWR

C401B 100nF
C401A 4.7uF
T_GND

T_SCSI_TERMPWR
C402 100nF
C403 4.7uF
T_GND

Board Holes

Fiducials

FID7 | FID8