

/ Ansys DDR Eye Analyzer

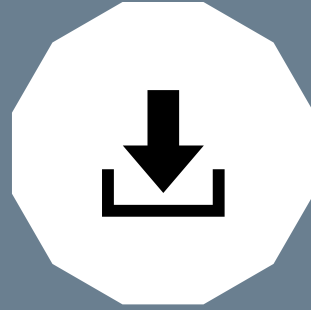


About ADEA

New DDR Solution for
Easy! Simple! and Customizable!

[See more details about ADEA!](#)

01

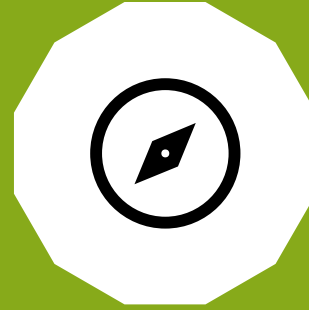


GitHub

All ADEA source codes are
published on the GitHub.

[Download and Enjoy ADEA!](#)

02



How to Use

User guide is included in ADEA .

Go to `./Resources/help`
[Check the guide video!](#)

03



Questions

Any questions & problems,
Send an e-mail to developer

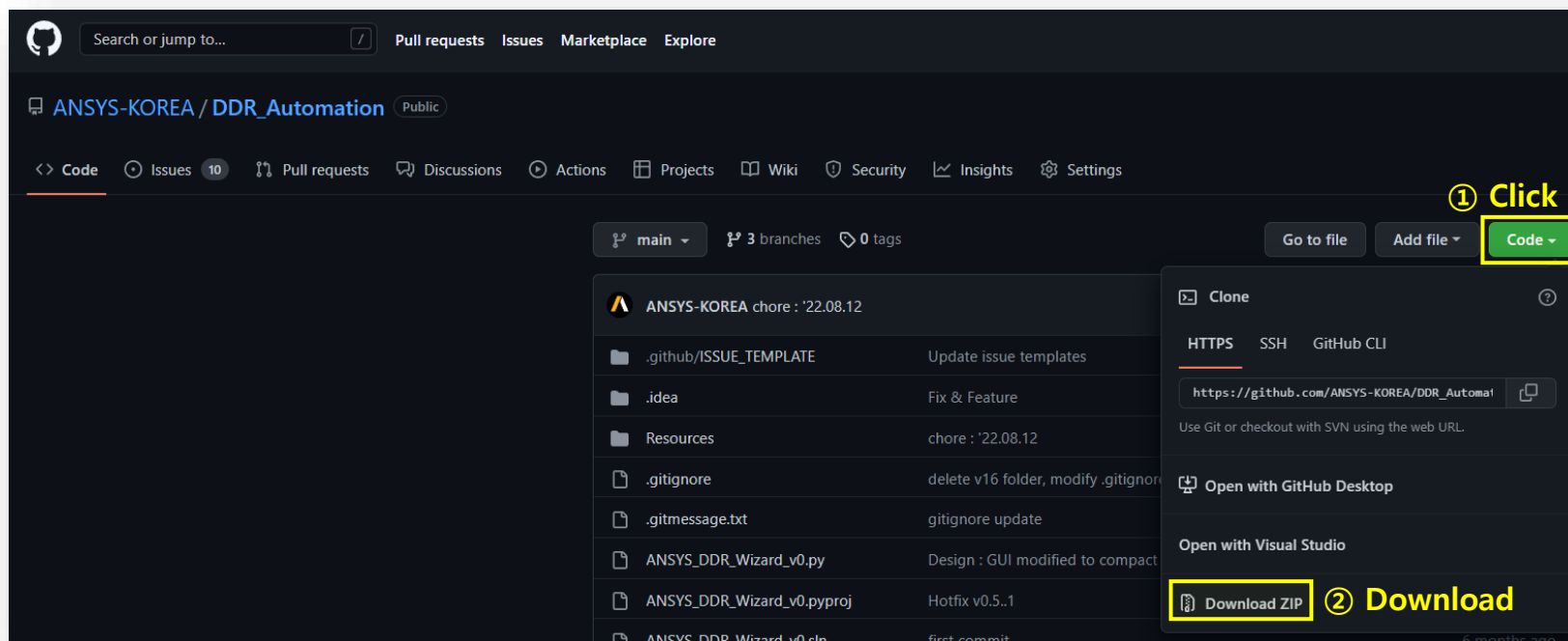
04

Getting Start with ADEA

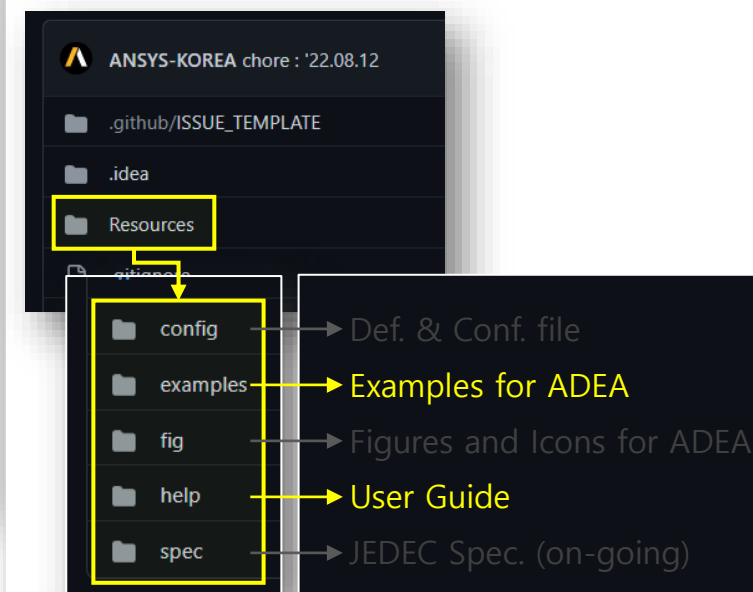


❑ ADEA의 소스 코드, 예제, 그리고 User Guide를 GitHub에서 다운로드 받으실 수 있습니다.

- [Ansys-Korea GitHub Homepage](#)에서 ADEA를 Download 합니다.



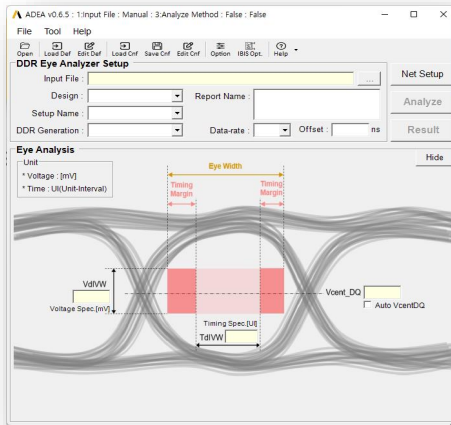
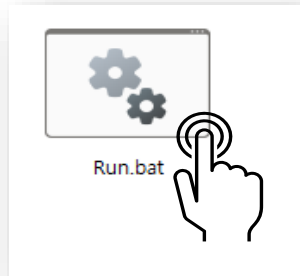
Download한 File의 **Resources folder**에서,
ADEA의 **예제**와 **User Guide**를 확인하세요



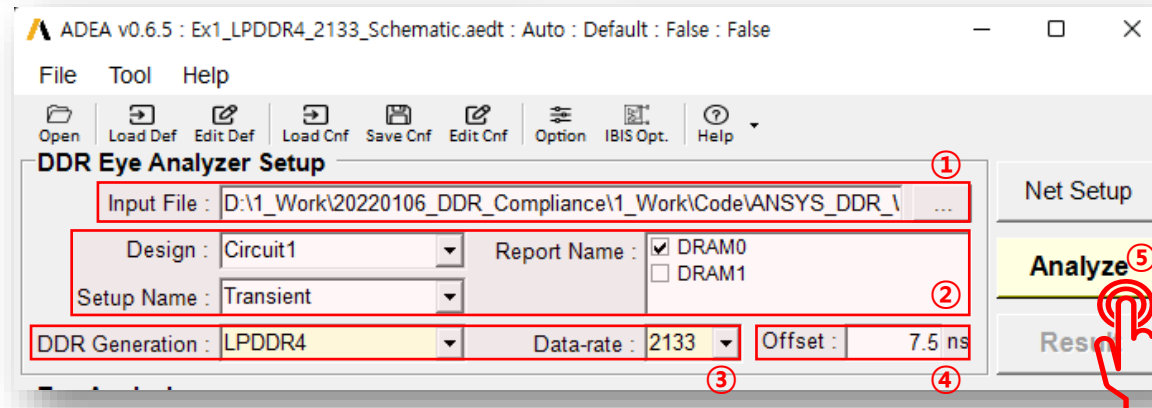
User Guide – Ansys DDR Eye Analyzer : Eye Analyze



1. Launch ADEA



2. ADEA Setup



- ① 입력 파일(*.aedt) 선택
- ② Design, Setup Name, Report Name 선택
- ③ DDR Type 및 Data-rate 선택
- ④ Eye 해석 Offset 입력
- ⑤ Click 'Analyze'

4. Result

Net Name	Width [ps]	Margin [ps]	Analyze Group	Group
✓ V(U2A5_M_DQ_0__AL2)	411	308	None	DQ
✓ V(U2A5_M_DQ_1__AK2)	361	257	None	DQ
✓ V(U2A5_M_DQ_2__AL2)	352	249	None	DQ
✓ V(U2A5_M_DQ_3__AH2)	360	257	None	DQ
✓ V(U2A5_M_DQ_4__AG2)	351	247	None	DQ
✓ V(U2A5_M_DQ_5__AJ2)	331	227	None	DQ
✓ V(U2A5_M_DQ_6__AH2)	351	248	None	DQ
✓ V(U2A5_M_DQ_7__AK2)	350	247	None	DQ

Plot EYE with Mask Image Width : 200 [pixel]

Report Format : Default Export Close

- ⑥ 결과창 자동 Pop-up
- ⑦ Timing 분석 결과 확인
- ⑧ 필요시 Report 출력

User Guide – Ansys DDR Eye Analyzer : IBIS Opt.

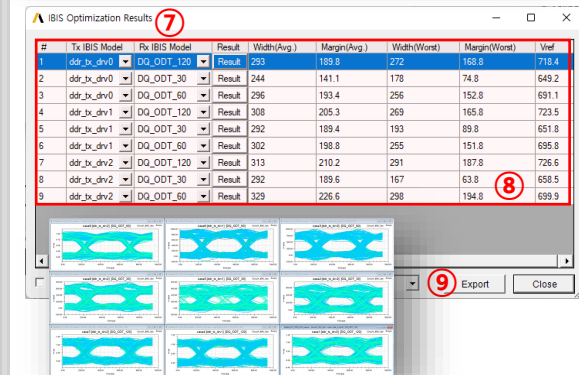
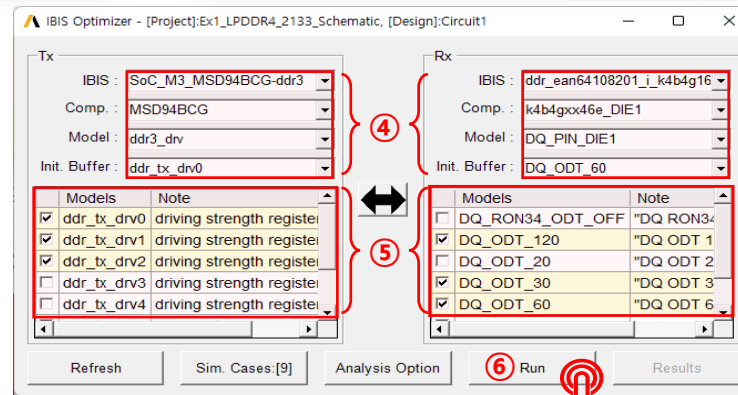
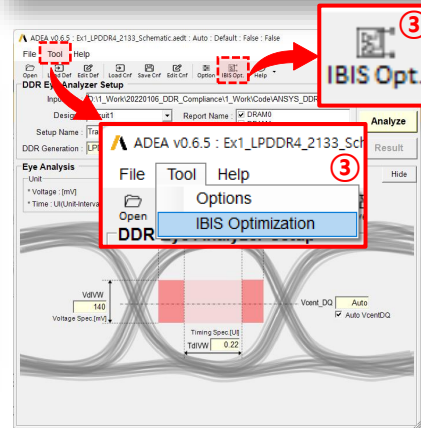
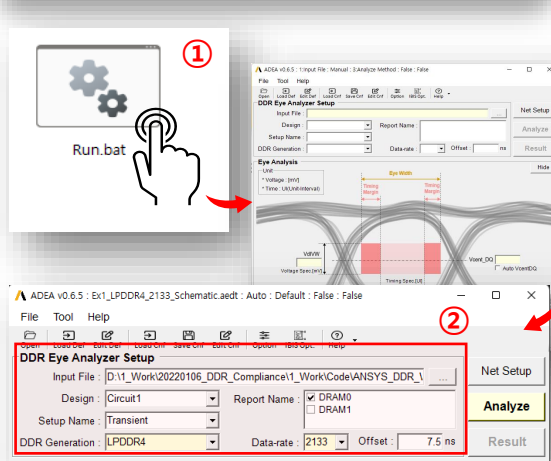


1. IBIS Opt. Setup

2. Sim. Case Setup

3. Analyze

4. Result



Eye Analyze와 동일하게,

- ① Launch AEDA
- ② AEDA Setup

③ Click '**IBIS Opt.**' Icon

or **Tool → IBIS Opt.**

④ Check Tx & Rx IBIS Info.

✓ **IBIS file, Comp., Model, Initial Buffer**

⑤ Select **IBIS Models for Tx/Rx**

⑥ Click 'Run'

⑦ 결과창 자동 Pop-up

⑧ Case별 분석 결과 확인

⑨ 필요시 Report 출력(TBD)

Eye Analyze

1. Launch ADEA

2. ADEA Setup

3. Analyze

4. Result

- 제공받은 File 중, Run.bat file을 이용하여 ADEA를 실행합니다.

Tool Strip Menu & Icons

Analyzer Setup 입력

DDR Type과 Speed에 따른 Spec.

Run.bat

Target Net 설정

해석 시작

해석 결과

GUI Size Control Button

ADEA가 실행되지 않을 경우

The screenshot shows the ADEA v0.6.5 software interface. The main window has a menu bar (File, Tool, Help) and a toolbar with icons for Open, Load Def, Edit Def, Load Cnf, Save Cnf, Edit Cnf, Option, IBIS Opt., and Help. Below the toolbar is the 'DDR Eye Analyzer Setup' section, which includes fields for Input File, Design, Report Name, Setup Name, DDR Generation, Data-rate, and Offset. To the right of this section are buttons for Net Setup, Analyze, and Result. Below the setup section is the 'Eye Analysis' section, which displays a signal eye diagram. The diagram shows multiple signal traces with a central red shaded area representing the eye. Various timing and voltage specifications are labeled on the diagram, including Eye Width, Timing Margin, VdIVW, Voltage Spec. [mV], Vcent_DQ, Timing Spec. [UI], and TdIVW. To the left of the diagram are fields for Unit, Voltage, and Time. A smaller inset window on the right shows the 'Run.bat' file being executed, with a 'Show' button. Annotations with arrows point to specific UI elements: 'Tool Strip Menu & Icons' points to the top menu bar; 'Analyzer Setup 입력' points to the input fields in the 'DDR Eye Analyzer Setup' section; 'DDR Type과 Speed에 따른 Spec.' points to the 'Unit' section in the 'Eye Analysis' section; 'Run.bat' points to a file icon; 'Target Net 설정' points to the 'Net Setup' button; '해석 시작' points to the 'Analyze' button; '해석 결과' points to the 'Result' button; 'GUI Size Control Button' points to the 'Hide' button; and 'ADEA가 실행되지 않을 경우' points to the 'Show' button in the inset window.



Eye Analyze

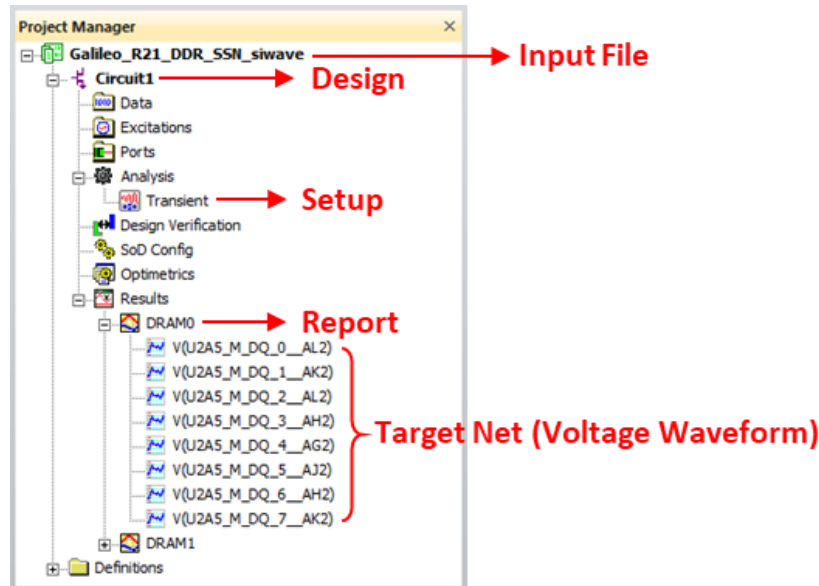
1. Launch ADEA

2. ADEA Setup

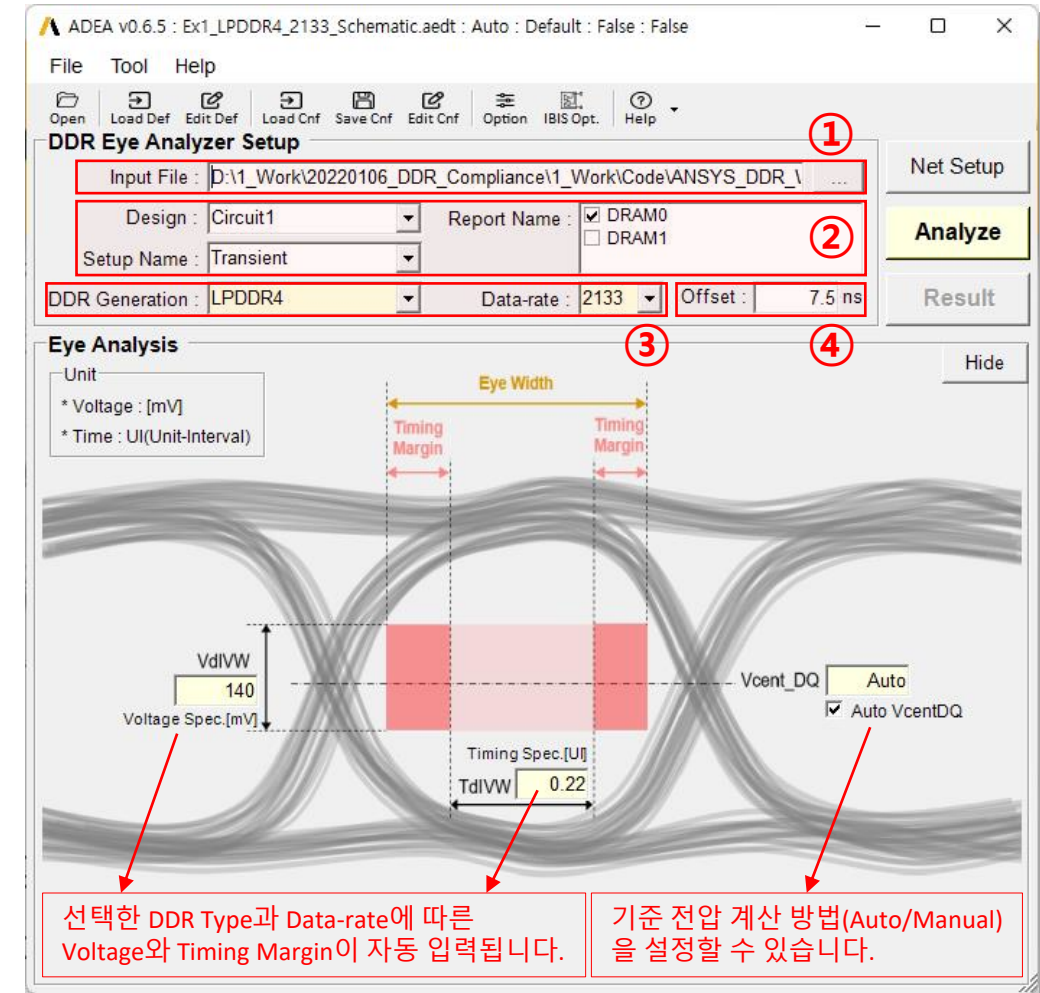
3. Analyze

4. Result

- ①  버튼 또는  Icon을 클릭 → Input File 선택.
- ② 해석을 원하는 Design, Setup, Report를 선택.



- ③ DDR Type과 Data-rate를 선택.
- ④ Offset을 입력.



Eye Analyze

1. Launch ADEA

2. ADEA Setup

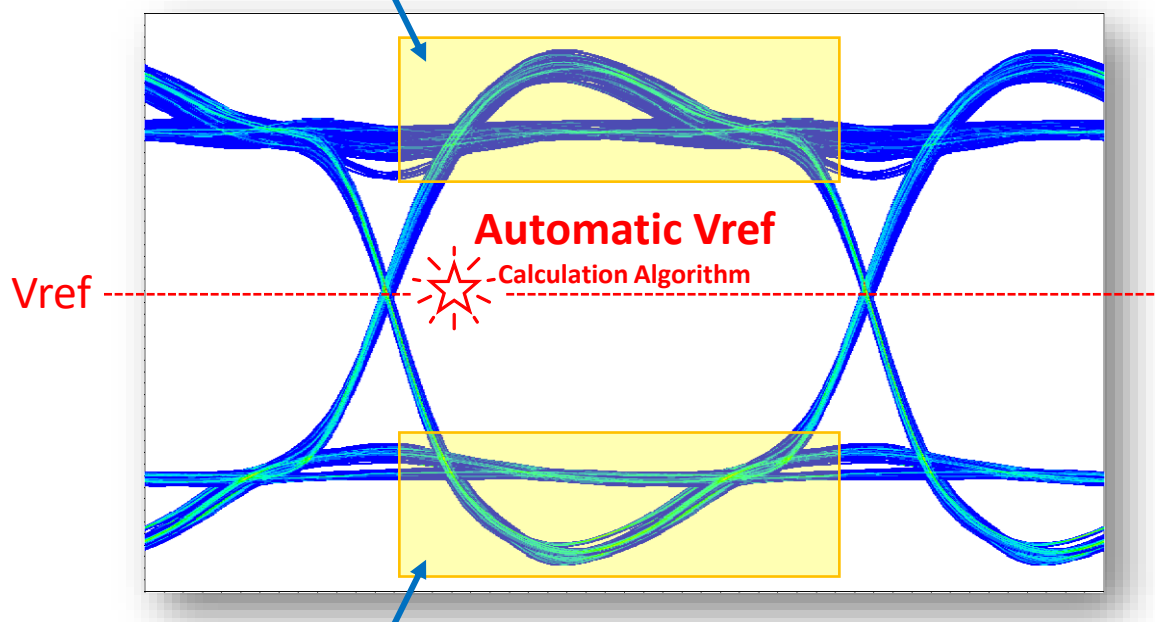
3. Analyze

4. Result

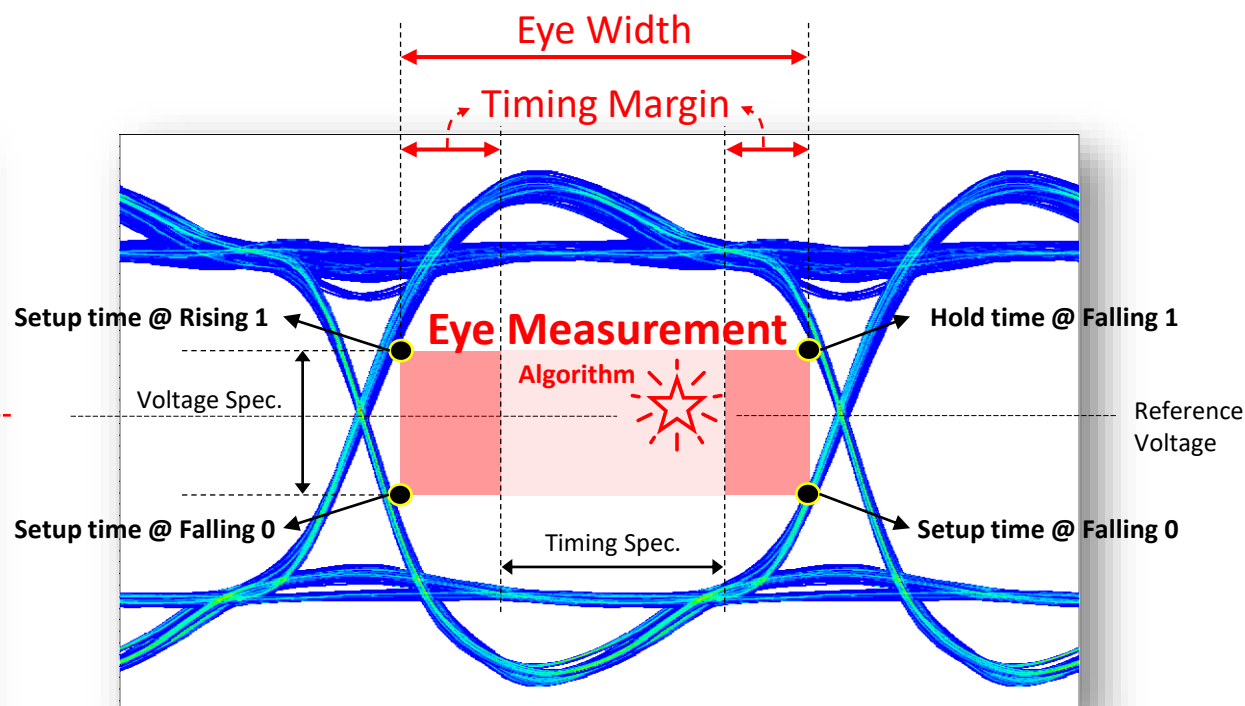
- Analyze 버튼을 클릭하여 해석을 진행합니다.

- ✓ 기준 전압 Level 자동 계산 Algorithm과 Eye 계측 Algorithm을 내장하고 있습니다.
- ✓ 사용자가 원하는 특정 방법의 기준 전압 Level 계산 방법과 Eye 계측 방법을 추가할 수 있습니다.

Statistical Logic 1 Level



Statistical Logic 0 Level



Eye Analyze

1. Launch ADEA

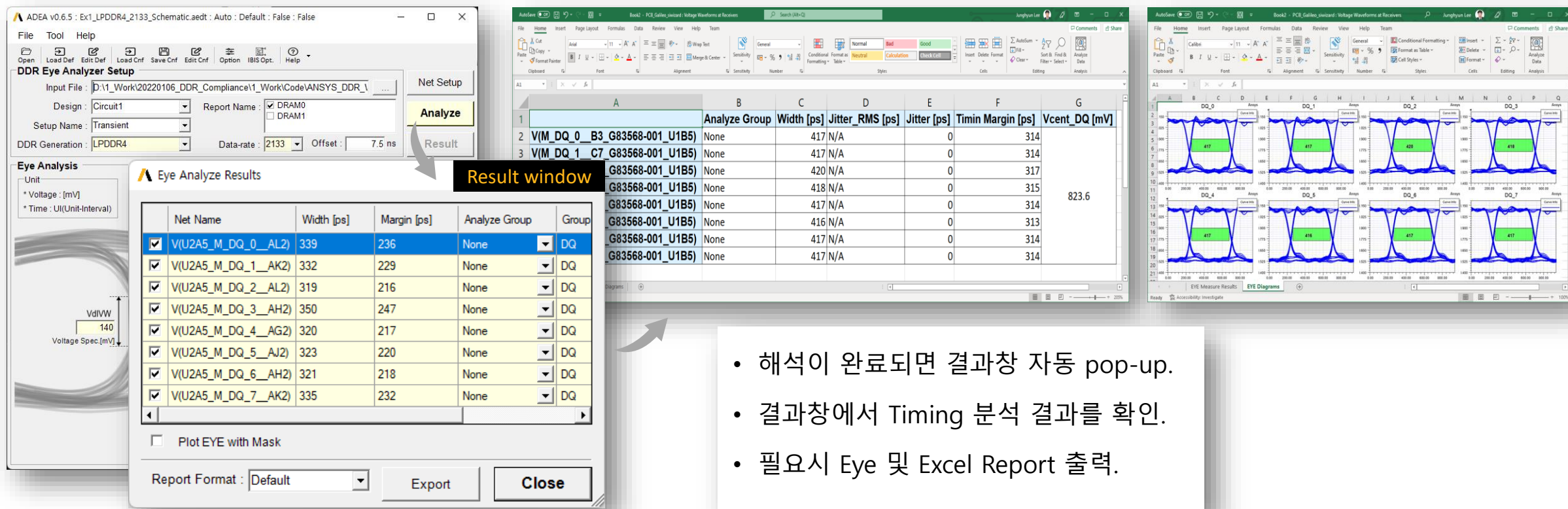
2. ADEA Setup

3. Analyze

4. Result

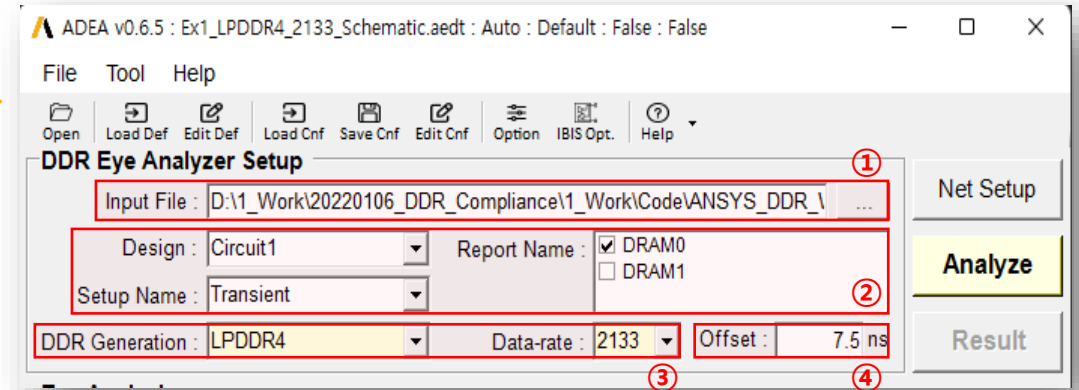
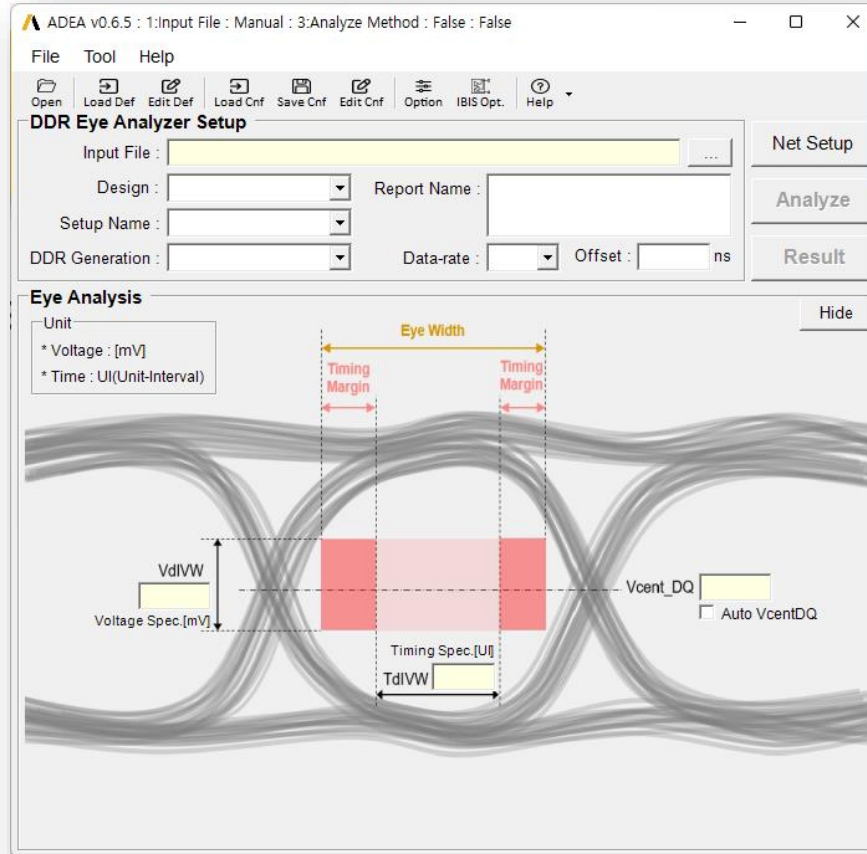
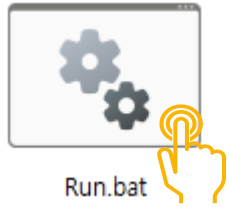
결과창에서 해석 결과를 확인합니다.

- ✓ 내장된 형식의 Excel Report 출력이 가능합니다.
- ✓ HTML Report 출력도 가능하며(TBD), 사용자가 원하는 형식으로 쉽게 Customize가 가능합니다.



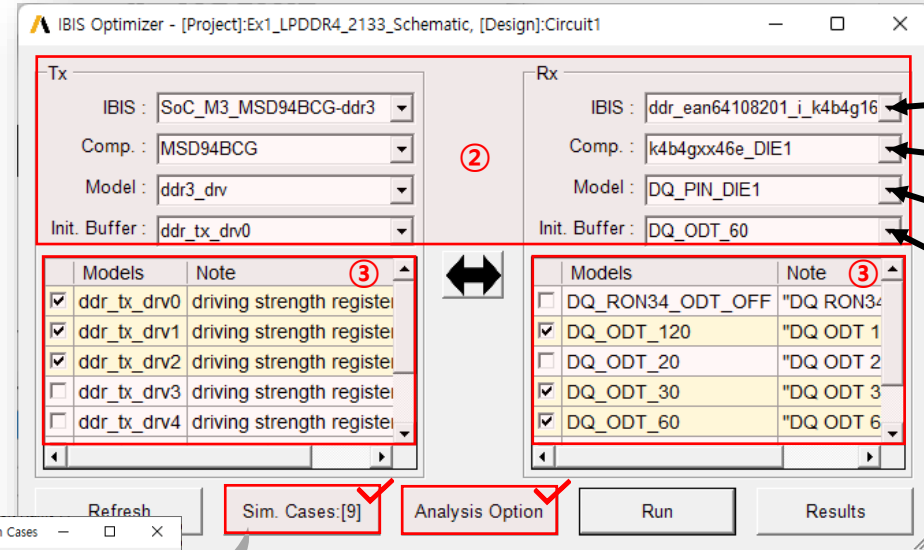
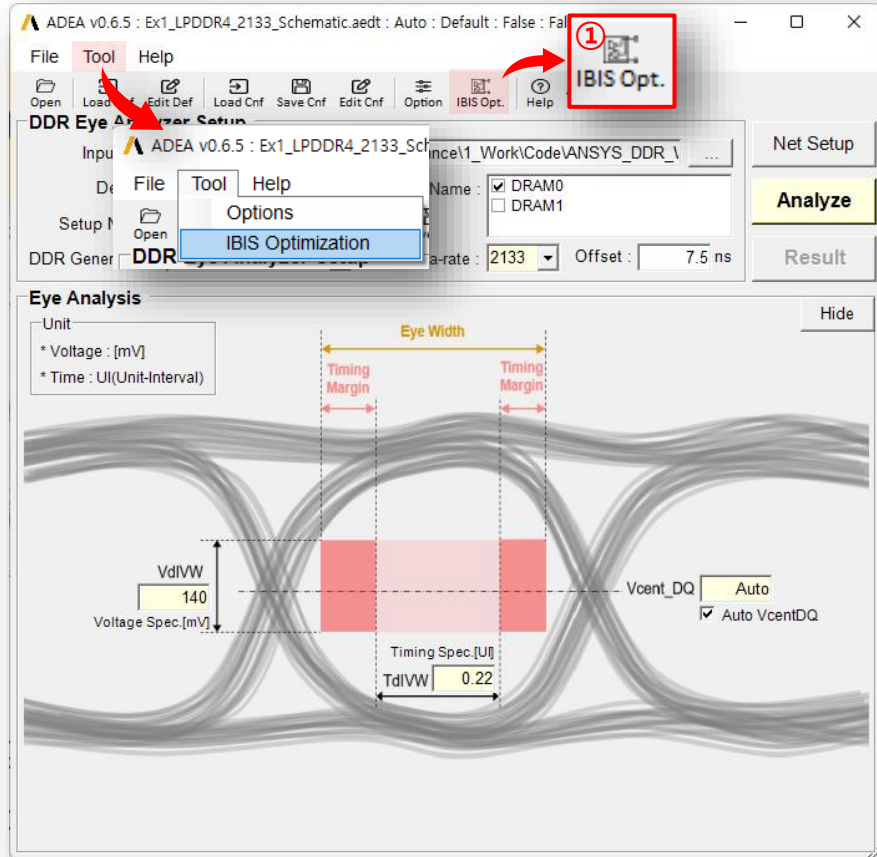
- 해석이 완료되면 결과창 자동 pop-up.
- 결과창에서 Timing 분석 결과를 확인.
- 필요시 Eye 및 Excel Report 출력.

- ADEA를 실행하고, Eye Analyze 과정과 동일하게 ADEA setup을 마칩니다.

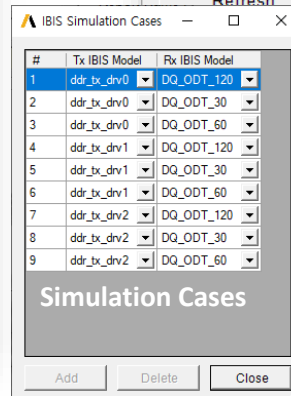


- ① 입력 파일(*.aedt) 선택.
- ② Design, Setup Name, Report 선택.
- ③ DDR Type 및 속도 선택.
- ④ Eye 해석 Offset 입력.

- IBIS Optimizer를 실행하고 IBIS 및 Simulation case를 선택합니다.



- IBIS File (*.ibs)
- IBIS Component
- IBIS Model
- Initial Buffer model for input schematic



- Tx/Rx IBIS model 조합 확인

- IBIS Optimizer 실행
 - IBIS file, component, model, initial buffer model 확인 및 선택.
 - 해석하고자 하는 Tx와 Rx buffer model 선택.
- ✓ Simulation case 확인.
 - ✓ Analysis option 확인.

IBIS Opt.

1. IBIS Opt. Setup

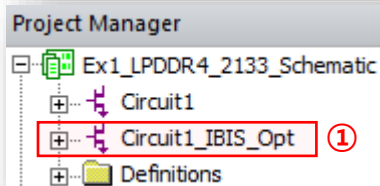
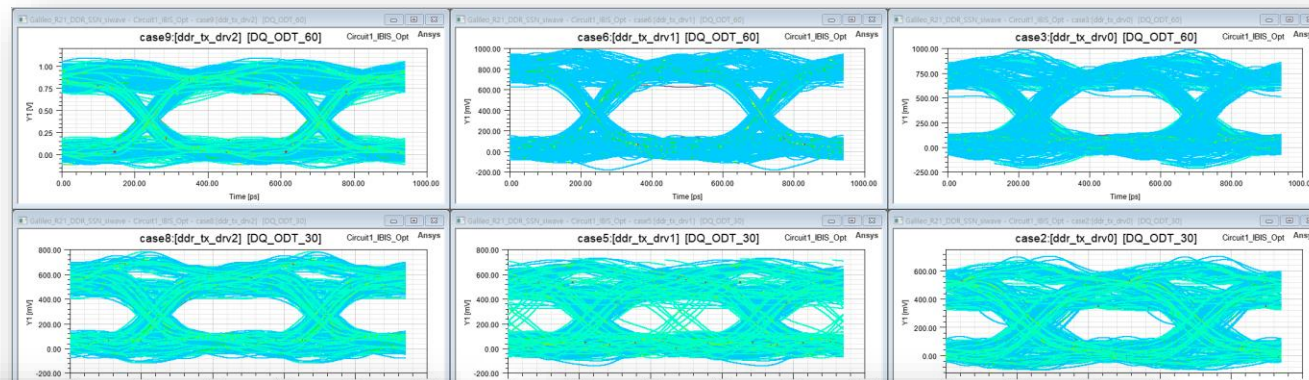
2. Sim. Case Setup

3. Analyze

4. Result

- Run 버튼을 클릭하여 해석을 진행하고 결과를 확인합니다.

- ① IBIS opt.을 위한 Schematic이 자동 생성.
- ② 해석이 완료되면 결과창 자동 pop-up.
- ✓ Simulation case별 상세 결과 확인
- ✓ 필요시 Eye 및 Excel Report 출력(TBD).



IBIS Optimization Results

#	Tx IBIS Model	Rx IBIS Model	Result	Width(Avg.)	Margin(Avg.)	Width(Worst)	Margin(Worst)	Vref
1	ddr_tx_drv0	DQ_ODT_120	Result	293	189.8	272	168.8	718.4
2	ddr_tx_drv0	DQ_ODT_30	Result	244	141.1	178	74.8	649.2
3	ddr_tx_drv0	DQ_ODT_60	Result	296	193.4	256	152.8	691.1
4	ddr_tx_drv1	DQ_ODT_120	Result	308	205.3	269	165.8	723.5
5	ddr_tx_drv1	DQ_ODT_30	Result	292	189.4	193	89.8	651.8
6	ddr_tx_drv1	DQ_ODT_60	Result	302	198.8	255	151.8	695.8
7	ddr_tx_drv2	DQ_ODT_120	Result	313	210.2	291	187.8	726.6
8	ddr_tx_drv2	DQ_ODT_30	Result	292	189.6	167	63.8	658.5
9	ddr_tx_drv2	DQ_ODT_60	Result	329	226.6	298	194.8	699.9

☐ Plot EYE Report Format: [Dropdown] Export Close

Eye Analyze Results - IBIS case1

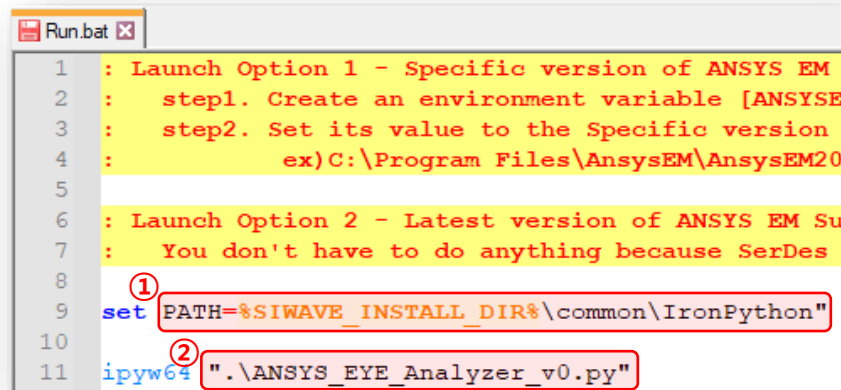
Net Name	Width [ps]	Margin [ps]	Analyze Group	Group
<input checked="" type="checkbox"/> V(U2A5_M_DQ_0__AL2)	294	190.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1__AK2)	277	173.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2__AL2)	300	196.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3__AH2)	308	204.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4__AG2)	295	191.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5__AJ2)	286	182.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_6__AH2)	272	168.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_7__AK2)	312	208.82	None	DQ

☐ Plot EYE with Mask Sim. Case 별 상세 해석 결과
Report Format: [Default] Export Close

Appendix A.1 – Launching ADEA

❑ Run.bat file을 이용하여 Ansys DDR Eye Analyzer를 실행합니다.

- Run.bat file로 Ansys DDR Eye Analyzer가 실행되지 않을 경우 아래 내용을 순차적으로 적용합니다.



```
1 : Launch Option 1 - Specific version of ANSYS EM
2 :   step1. Create an environment variable [ANSYS_EYE_Analyzer_v0.py]
3 :   step2. Set its value to the Specific version
4 :   ex) C:\Program Files\AnsysEM\AnsysEM20
5
6 : Launch Option 2 - Latest version of ANSYS EM Su
7 :   You don't have to do anything because SerDes
8
9 set PATH=%SIWAVE_INSTALL_DIR%\common\IronPython"
10
11 ipyw64 ".\ANSYS_EYE_Analyzer_v0.py"
```

❖ [Ansys Electronics Desktop Version 설정 방법](#)

① 항목의 경로를 AEDT가 설치된 절대 경로로 수정합니다.

ex) 수정 전 : `set PATH=%SIWAVE_INSTALL_DIR%\common\IronPython"`

수정 후 : `set PATH="C:\Program Files\AnsysEM\AnsysEM21.2\Win64\common\IronPython"`

② 항목을 “ANSYS_EYE_Analyzer_v0.py” file의 절대 경로로 수정합니다.

✓ 상대 경로 이용 시, Run.bat file과 ANSYS_EYE_Analyzer_v0.py file은 같은 경로에 존재해야 합니다.

Appendix A.2 – AEDT Version Selection

❑ Version Selection for Ansys Electronics Desktop(AEDT)

- 기본적으로 시스템 변수(ANSYSEM_ROOTxxx)를 검색하여 가장 최신 version의 AEDT를 자동 선택합니다.

시스템 변수(S)

변수	값
ANSYSEM_ROOT180	C:\#AnsysEM\#AnsysEM18.0\#Win64
ANSYSEM_ROOT202	C:\#AnsysEM\#AnsysEM20.2\#Win64
ANSYSEM_ROOT212	C:\#AnsysEM\#AnsysEM21.2\#Win64
ANSYSEM_ROOT221	C:\#AnsysEM\#v221\#Win64

→ AEDT 2022 R1 선택

- 특정 Version의 AEDT 사용을 원할 경우,

- ① [ANSYSEM_INSTALL_DIR] 시스템 변수를 생성합니다.
- ② 원하는 version의 AEDT 설치 경로를 위 시스템 변수의 값으로 설정합니다.

새 시스템 변수

변수 이름(N): ANSYSEM_INSTALL_DIR ①

변수 값(V): C:\#AnsysEM\#AnsysEM21.2\#Win64 ②

디렉터리 찾아보기(D)... 파일 찾아보기(F)... 확인 취소

시스템 변수(S)

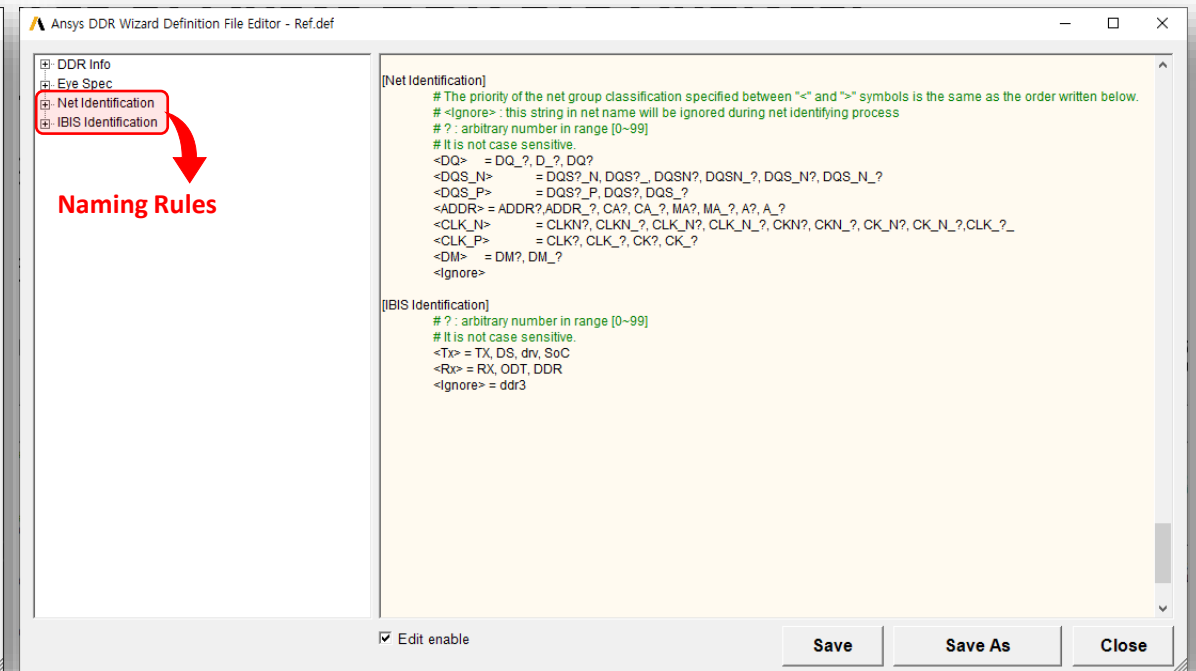
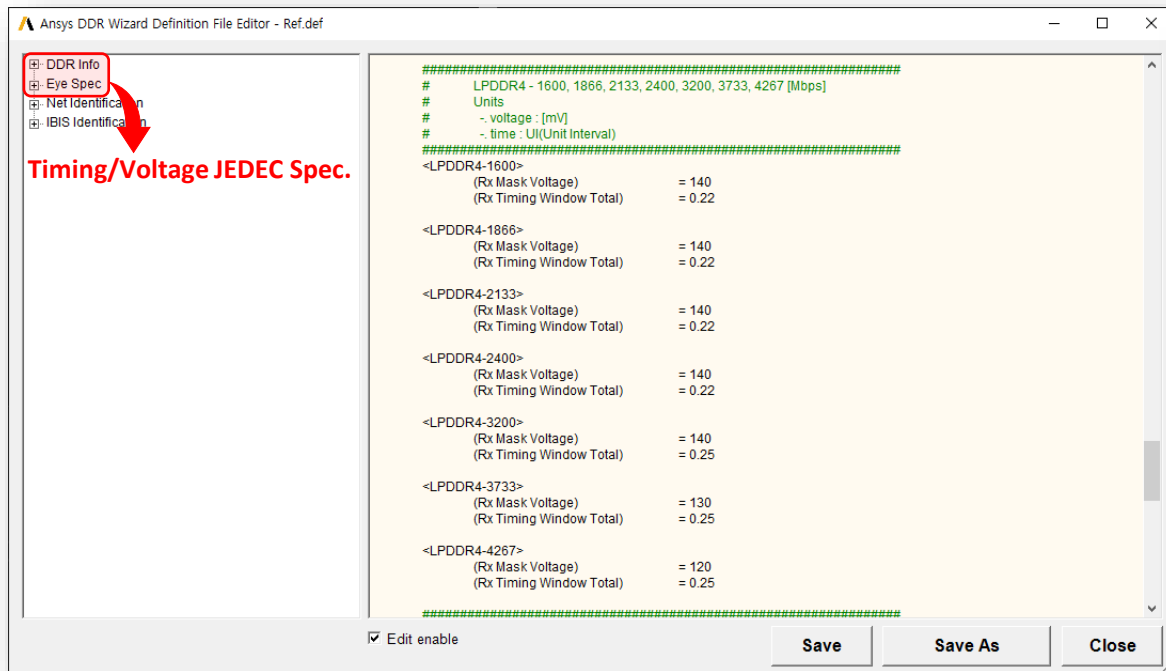
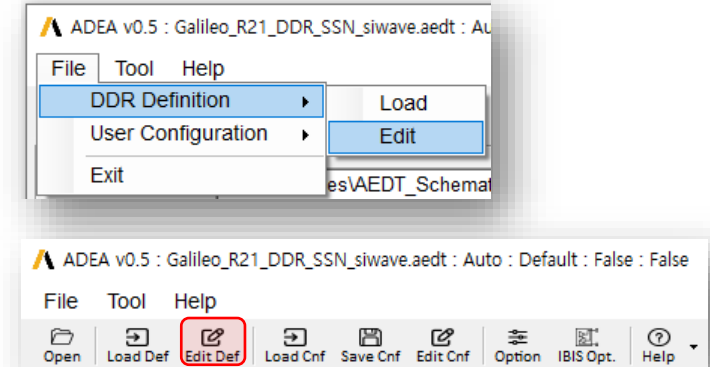
변수	값
ANSYSEM_INSTALL_DIR	C:\#AnsysEM\#AnsysEM21.2\#Win64
ANSYSEM_ROOT180	C:\#AnsysEM\#AnsysEM18.0\#Win64
ANSYSEM_ROOT202	C:\#AnsysEM\#AnsysEM20.2\#Win64
ANSYSEM_ROOT212	C:\#AnsysEM\#AnsysEM21.2\#Win64
ANSYSEM_ROOT221	C:\#AnsysEM\#v221\#Win64

→ AEDT 2021 R2 선택

Appendix B.1 – Pre-Configurations

❑ Definition File (*.def)

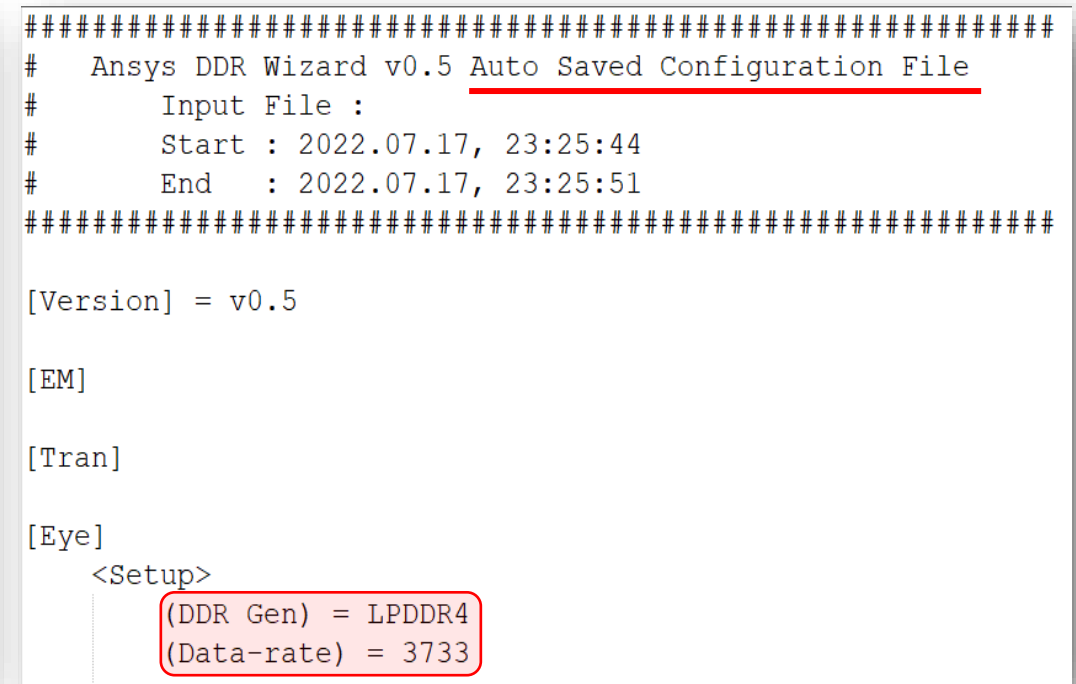
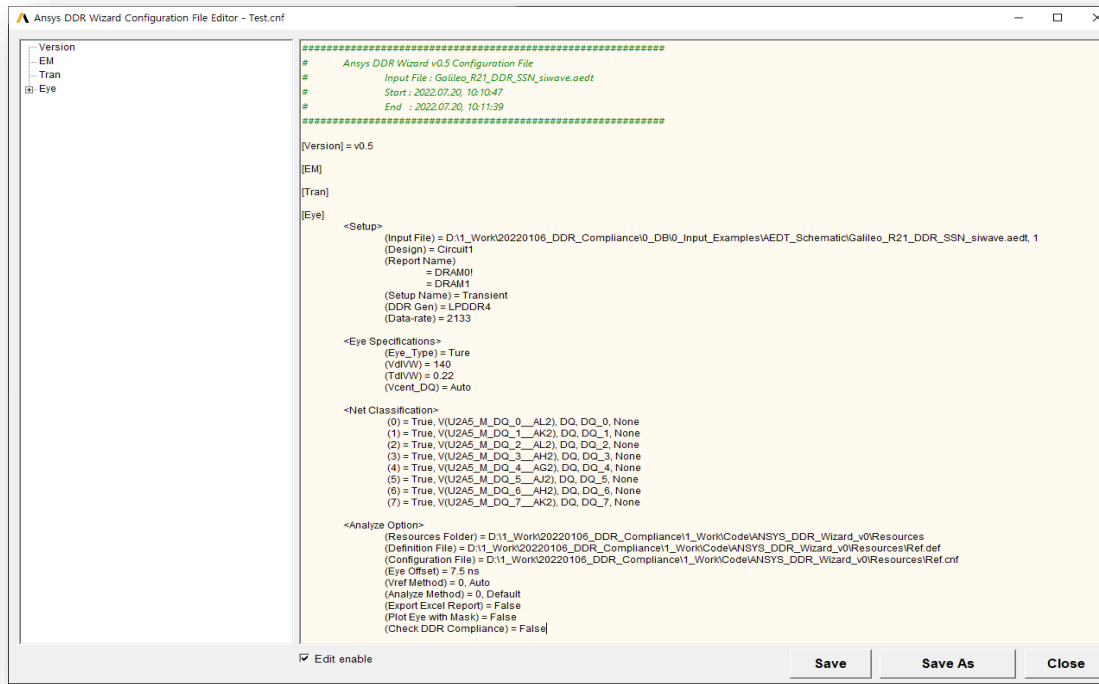
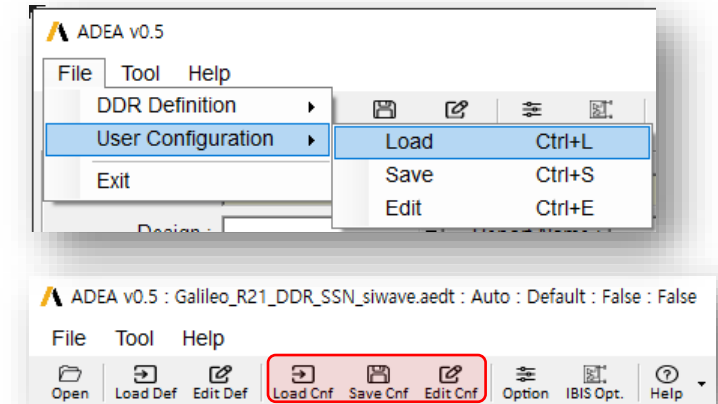
- (LP)DDR2/3/4/5의 Timing/Voltage JEDEC Spec.이 정의 되어 있습니다.
- 사용자가 원하는 Spec.을 추가 혹은 수정이 가능합니다.
- Target Net 분류 및 IBIS 모델 선택을 위한 Naming Rule이 정의 되어 있으며, 추가 혹은 수정이 가능합니다.



Appendix B.2 – Pre-Configurations

❑ Configuration File (*.cnf)

- ADEA 사용을 위한 모든 입력을 Cnf File에 저장 할 수 있습니다.
- 저장된 Cnf File을 로드하여 모든 입력을 자동으로 채울 수 있습니다.
- DDR Type 및 Data-rate 항목은 사용자의 편의를 위하여 자동 저장/로드 됩니다.



Appendix B.3 – Automatic Net Classification

Automatic Net Classification

- Ansys DDR Eye Analyzer는 해석 대상 Net을 하기의 7개 Group으로 자동 분류합니다.

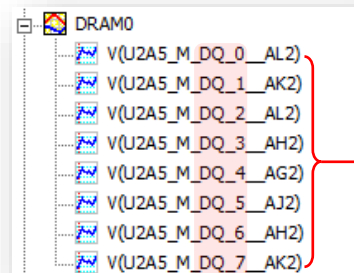
① DQ ② DQS_N ③ DQS_P ④ ADDR ⑤ CLK_N ⑥ CLK_P ⑦ DM

- Definition File에 정의되어 있는 Net Identification Rule에 따라 자동으로 분류됩니다.

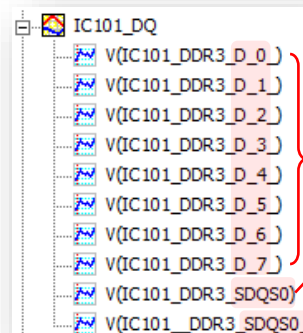
[Net Identification]

```
# The priority of the net group classification specified between "<" and ">" symbols is the same as the order written below.
# <Ignore> : this string in net name will be ignored during net identifying process
# ? : arbitrary number in range [0~99]
# It is not case sensitive.
<DQ>    = DQ_?, D_?, DQ?
<DQS_N> = DQS?_N, DQS?_, DQSN?, DQSN_?, DQS_N?, DQS_N_?
<DQS_P> = DQS?_P, DQS?, DQS_?
<ADDR>  = ADDR?, ADDR_?, CA?, CA_?, MA?, MA_?, A?, A_?
<CLK_N> = CLKN?, CLKN_?, CLK_N?, CLK_N_?, CKN?, CKN_?, CK_N?, CK_N_?, CLK_?
<CLK_P> = CLK?, CLK_?, CK?, CK_?
<DM>    = DM?, DM_?
<Ignore>
```

- Rule은 사용자의 환경에 따라 수정 또는 추가 가능합니다.



<DQ> = DQ_?, D_?, DQ?
DQ Group으로 자동 분류됨.




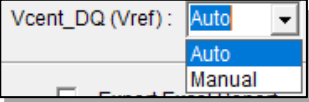
<DQ> = DQ_?, D_?, DQ?
DQ Group으로 자동 분류됨.

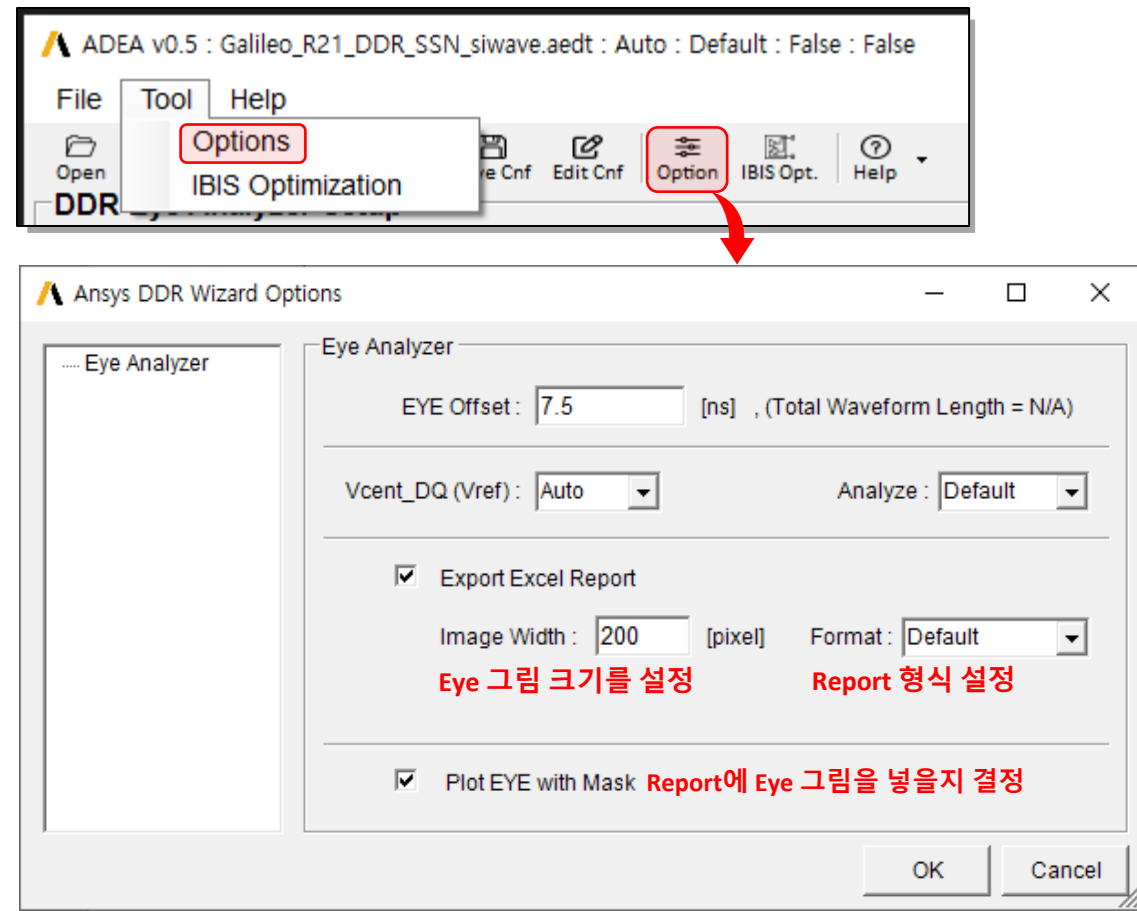
<DQS_P> = DQS?_P, DQS?, DQS_?
DQS_P Group으로 자동 분류됨.

<DQS_N> = DQS?_N, DQS?, DQSN?, DQSN_?,
DQS_N Group으로 자동 분류됨.

Appendix C.1 – Analysis Option Setup

❑ Ansys DDR Eye Analyzer – Option setup

- Tool → Option 메뉴 또는  Icon을 클릭합니다.
Option
- Option창에서 Eye 해석을 위한 설정을 입력합니다.
 - ✓ Eye Offset : Voltage waveform의 offset을 입력.
 - ✓ Vcent_DQ(Vref) : 기준 전압 계산법 선택 → 
 - ✓ Analyze : Eye 계측 방법 선택
 - ✓ Export Excel : Excel report 생성 여부 선택.
해석 완료 후 결과 창에서 report 생성 가능.
- 기준 전압 계산법, Eye 계측 방법, 그리고 report 형식은 요청에 의해 Customize될 수 있습니다.



Default option 설정값으로 해석 진행 시, Option Setup 과정은 생략될 수 있습니다.

Appendix C.2 – Target Net Setup

Target Net Setup

- 자동 분류된 Group 중 DQ Group은 자동으로 Check 됩니다.
- Net을 Check 또는 Uncheck하여 수동으로 Target Net 설정이 가능합니다.
- Rule을 수정하여 적용하거나 Dropdown 메뉴로 Group 수정이 가능합니다.
- Analyze Group을 이용하여 Net의 묶음 해석이 가능합니다.

Analyze Group : → DQ 번호로 자동 Grouping

✓ Analyze Group이 설정되지 않은 경우 개별 Net으로 해석합니다.

Net Name	Group	Matched String	Analyze Group
<input checked="" type="checkbox"/> V(U2A5_M_DQ_0__AL2)	DQ	DQ_0	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1__AK2)	DQ	DQ_1	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2__AL2)	DQ	DQ_2	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3__AH2)	DQ	DQ_3	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4__AG2)	DQ	DQ_4	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5__AJ2)	DQ	DQ_5	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_6__AH2)	DQ	DQ_6	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_7__AK2)	DQ	DQ_7	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_8__AT2)	DQ	DQ_8	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_9__AP2)	DQ	DQ_9	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_10__A...	DQ	DQ_10	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_11__A...	DQ	DQ_11	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_12__A...	DQ	DQ_12	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_13__A...	DQ	DQ_13	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_14__A...	DQ	DQ_14	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_15__A...	DQ	DQ_15	None

→ Bit별 개별 해석

Net Name	Group	Matched String	Analyze Group
<input checked="" type="checkbox"/> V(U2A5_M_DQ_0__AL2)	DQ	DQ_0	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1__AK2)	DQ	DQ_1	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2__AL2)	DQ	DQ_2	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3__AH2)	DQ	DQ_3	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4__AG2)	DQ	DQ_4	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5__AJ2)	DQ	DQ_5	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_6__AH2)	DQ	DQ_6	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_7__AK2)	DQ	DQ_7	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_8__AT2)	DQ	DQ_8	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_9__AP2)	DQ	DQ_9	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_10__A...	DQ	DQ_10	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_11__A...	DQ	DQ_11	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_12__A...	DQ	DQ_12	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_13__A...	DQ	DQ_13	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_14__A...	DQ	DQ_14	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_15__A...	DQ	DQ_15	Byte1

→ Byte별 묶음 해석

<input checked="" type="checkbox"/> V(U2A5_M_DQ_0__AL2)	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1__AK2)	DM
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2__AL2)	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3__AH2)	DQS_P
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4__AG2)	DQS_N
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5__AJ2)	CLK_P
	CLK_N
	ADDR
	OTHER

Net Group 선택 Dropdown Menu

Target Net Setup - latest.cnf

Net Name	Group	Matched String	Analyze Group
<input checked="" type="checkbox"/> Test_A1	ADDR	A1	None
<input type="checkbox"/> Test_A11	ADDR	A11	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_0__B2)	DQ	DQ_0	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_1__C2)	DQ	DQ_1	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_2__C2)	DQ	DQ_2	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_3__C2)	DQ	DQ_3	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_4__E2)	DQ	DQ_4	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_5__E2)	DQ	DQ_5	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_6__D2)	DQ	DQ_6	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_7__E2)	DQ	DQ_7	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_8__B2)	DQ	DQ_8	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_9__C2)	DQ	DQ_9	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_10__C2)	DQ	DQ_10	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_11__C2)	DQ	DQ_11	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_12__E2)	DQ	DQ_12	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_13__E2)	DQ	DQ_13	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_14__D2)	DQ	DQ_14	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_15__E2)	DQ	DQ_15	None
<input type="checkbox"/> V(U1A1_M_DQS_1__C2)	DQS_P	DQS_1	None
<input type="checkbox"/> V(U1A1_M_DQS_N_1__...	DQS_N	DQS_N_1	None

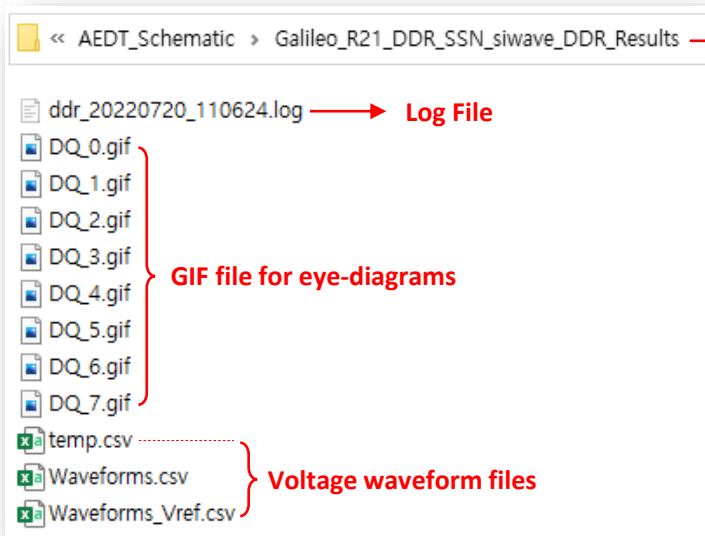
Analyze Group :

Rule 수정 및 적용 버튼

Appendix D – Eye Measurement Results

□ Eye Measurement Results

- 해석 종료 후 Result Window가 자동으로 Pop-up 됩니다.
- Bit별 또는 Byte별 Eye Width와 Timing Margin을 확인할 수 있습니다.
- 결과 확인 후 , Result Window에서 Report 출력이 가능합니다.
- Log file, Eye-diagram GIF file등의 결과 파일이 생성됩니다.



→ {Input file name}_DDR_Results 폴더 자동 생성

	Net Name	Width [ps]	Margin [ps]	Analyze Group	Group
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_0__AL2)	375	272	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_1__AK2)	368	265	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_2__AL2)	360	257	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_3__AH2)	381	278	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_4__AG2)	336	233	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_5__AJ2)	359	256	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_6__AH2)	373	270	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_7__AK2)	355	251	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_8__AT2)	386	283	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_9__AP2)	386	283	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_10__A...	375	272	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_11__A...	374	271	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_12__A...	379	276	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_13__A...	368	265	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_14__A...	399	296	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_15__A...	367	264	None	DQ

☒ Plot EYE with Mask Image Width : 200 [pixel]

Report Format : Default Export Close

Appendix E – IBIS File and Model Selection

IBIS File and Model Selection

- Definition File에 정의되어 있는 IBIS Identification Rule에 따라 Tx/Rx의 IBIS File과 Model이 자동 분류됩니다.

[IBIS Identification]

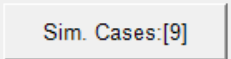
? : arbitrary number in range [0~99]
It is not case sensitive.
<Tx> = TX, DS, drv, SoC
<Rx> = RX, ODT, DDR
<Ignore> = ddr3

U23:ddr_tx_drv0_msd94bcg-ddr3 Properties: Galileo_R21_DDR_SSN_siwave

Parameter Values	Component	Symbol	Property Displays
<input checked="" type="radio"/> Value <input type="radio"/> Statistics			
Name	Value		
file	SoC_M3_MSD94BCG-ddr3.ibs		
model	ddr_tx_drv0		

U16:DQ_ODT_60_DDR_EAN64108201_i_k4b4g1646e_bcxx_june23 Prop

Parameter Values	Component	Symbol	Property Displays
<input checked="" type="radio"/> Value <input type="radio"/> Statistics			
Name	Value		
file	DDR_EAN64108201_i_k4b4g1646e_bcxx_june23.ibs		
model	DQ_ODT_60		

- Rule 수정 및 추가가 가능합니다.
- IBIS File, Comp., Model를 수동 선택할 수 있습니다.
- 해석하고자 하는 Tx와 Rx의 Model을 선택합니다.
-  버튼으로 Sim. Case를 확인할 수 있습니다.

IBIS Optimizer - [Project]:Galileo_R21_DDR_SSN_siwave, [Design]:Circuit1

Tx

IBIS : SoC_M3_MSD94BCG-ddr3 View

Comp. : MSD94BCG

Model : ddr3_drv

Models	Note
<input checked="" type="checkbox"/> ddr_tx_drv0	driving strength register
<input checked="" type="checkbox"/> ddr_tx_drv1	driving strength register
<input checked="" type="checkbox"/> ddr_tx_drv2	driving strength register
<input type="checkbox"/> ddr_tx_drv3	driving strength register
<input type="checkbox"/> ddr_tx_drv4	driving strength register

Rx

IBIS : DDR_EAN64108201_i_k4 View

Comp. : k4b4gxx46e_DIE1

Model : DQ_PIN_DIE1

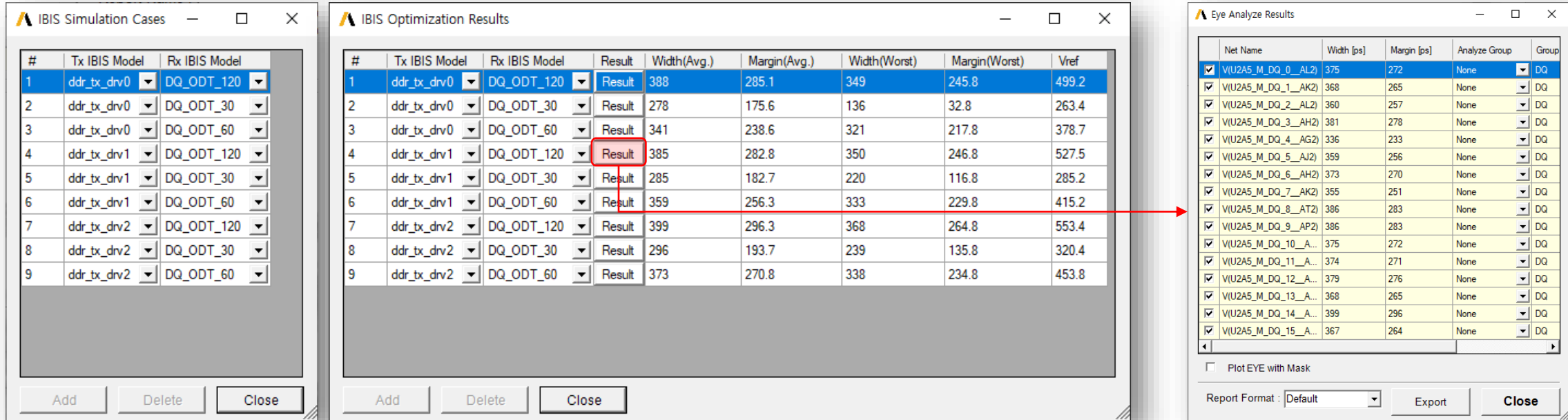
Models	Note
<input type="checkbox"/> DQ_RON34_ODT_OFF	"DQ RON34
<input type="checkbox"/> DQ_ODT_120	"DQ ODT 1
<input checked="" type="checkbox"/> DQ_ODT_20	"DQ ODT 2
<input checked="" type="checkbox"/> DQ_ODT_30	"DQ ODT 3
<input checked="" type="checkbox"/> DQ_ODT_60	"DQ ODT 6

Sim. Cases:[9] Analysis Option Run Results

Appendix F – IBIS Optimization Results

IBIS Optimization Results

- 선택한 Tx와 Rx Model의 모든 조합에 따른 Eye 분석 결과를 확인할 수 있습니다.



#	Tx IBIS Model	Rx IBIS Model
1	ddr_tx_drv0	DQ_ODT_120
2	ddr_tx_drv0	DQ_ODT_30
3	ddr_tx_drv0	DQ_ODT_60
4	ddr_tx_drv1	DQ_ODT_120
5	ddr_tx_drv1	DQ_ODT_30
6	ddr_tx_drv1	DQ_ODT_60
7	ddr_tx_drv2	DQ_ODT_120
8	ddr_tx_drv2	DQ_ODT_30
9	ddr_tx_drv2	DQ_ODT_60

#	Tx IBIS Model	Rx IBIS Model	Result	Width(Avg.)	Margin(Avg.)	Width(Worst)	Margin(Worst)	Vref
1	ddr_tx_drv0	DQ_ODT_120	Result	388	285.1	349	245.8	499.2
2	ddr_tx_drv0	DQ_ODT_30	Result	278	175.6	136	32.8	263.4
3	ddr_tx_drv0	DQ_ODT_60	Result	341	238.6	321	217.8	378.7
4	ddr_tx_drv1	DQ_ODT_120	Result	385	282.8	350	246.8	527.5
5	ddr_tx_drv1	DQ_ODT_30	Result	285	182.7	220	116.8	285.2
6	ddr_tx_drv1	DQ_ODT_60	Result	359	256.3	333	229.8	415.2
7	ddr_tx_drv2	DQ_ODT_120	Result	399	296.3	368	264.8	553.4
8	ddr_tx_drv2	DQ_ODT_30	Result	296	193.7	239	135.8	320.4
9	ddr_tx_drv2	DQ_ODT_60	Result	373	270.8	338	234.8	453.8

Net Name	Width [ps]	Margin [ps]	Analyze Group	Group
V(U2A5_M_DQ_0__AL2)	375	272	None	DQ
V(U2A5_M_DQ_1__AK2)	368	265	None	DQ
V(U2A5_M_DQ_2__AL2)	360	257	None	DQ
V(U2A5_M_DQ_3__AH2)	381	278	None	DQ
V(U2A5_M_DQ_4__AG2)	336	233	None	DQ
V(U2A5_M_DQ_5__AJ2)	359	256	None	DQ
V(U2A5_M_DQ_6__AH2)	373	270	None	DQ
V(U2A5_M_DQ_7__AK2)	355	251	None	DQ
V(U2A5_M_DQ_8__AT2)	386	283	None	DQ
V(U2A5_M_DQ_9__AP2)	386	283	None	DQ
V(U2A5_M_DQ_10__A...	375	272	None	DQ
V(U2A5_M_DQ_11__A...	374	271	None	DQ
V(U2A5_M_DQ_12__A...	379	276	None	DQ
V(U2A5_M_DQ_13__A...	368	265	None	DQ
V(U2A5_M_DQ_14__A...	399	296	None	DQ
V(U2A5_M_DQ_15__A...	367	264	None	DQ

- 각 Case별 Eye Width와 Timing Margin은 Target Net의 평균값과 Worst값으로 나타납니다.
- Result 버튼을 Click하여 각 Case별 상세 해석 결과를 확인할 수 있습니다.