

# / Ansys DDR Eye Analyzer

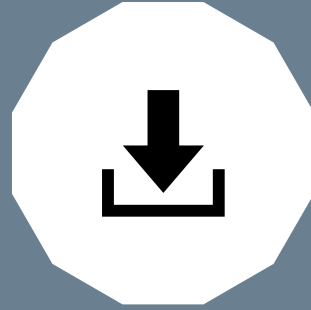


## About ADEA

New DDR Solution for  
Easy! Simple! and Customizable!

[See more details about ADEA!](#)

01

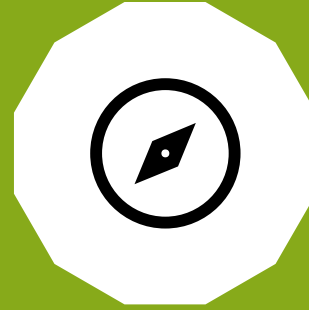


## GitHub

All ADEA source codes are  
published on the GitHub.

[Download and Enjoy ADEA!](#)

02



## How to Use

User guide is included in ADEA .

Go to `./Resources/help`

[Check the guide video!](#)

03



## Questions

Any questions & problems,  
Send an e-mail to developer

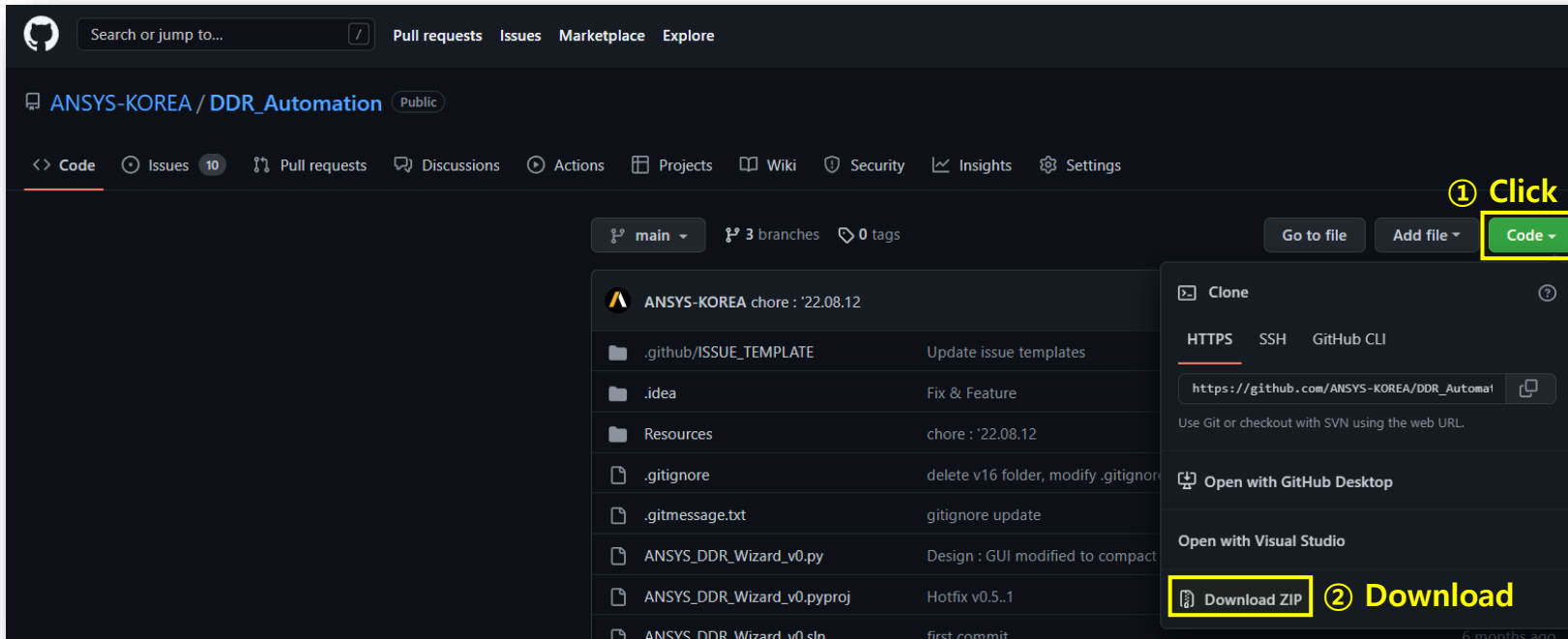
04

# / Getting Start with ADEA

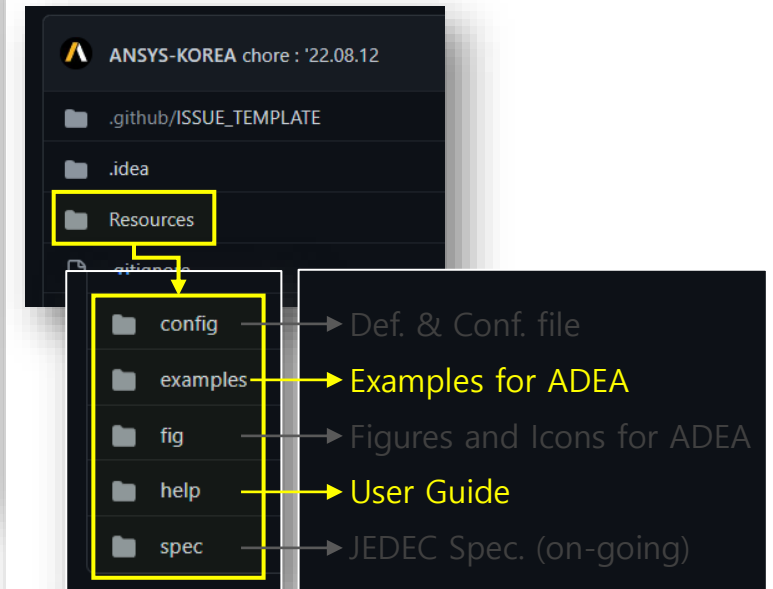


❏ Source code, example, and user guides of ADEA are available for download from GitHub.

- Download ADEA from the [Ansys-Korea GitHub Homepage](https://github.com/ANSYS-KOREA/DDR_Automation).



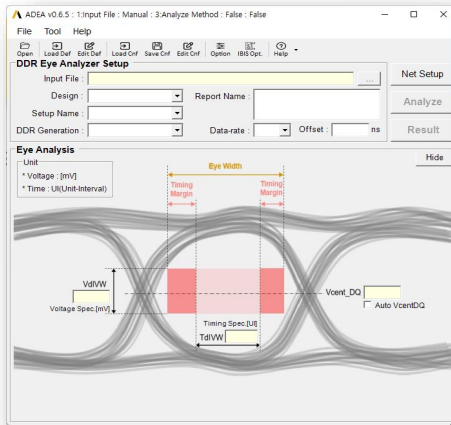
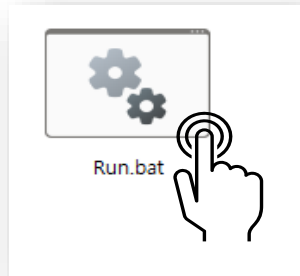
Check the **Examples** and **User Guide**  
in the **Resources** folder 😊



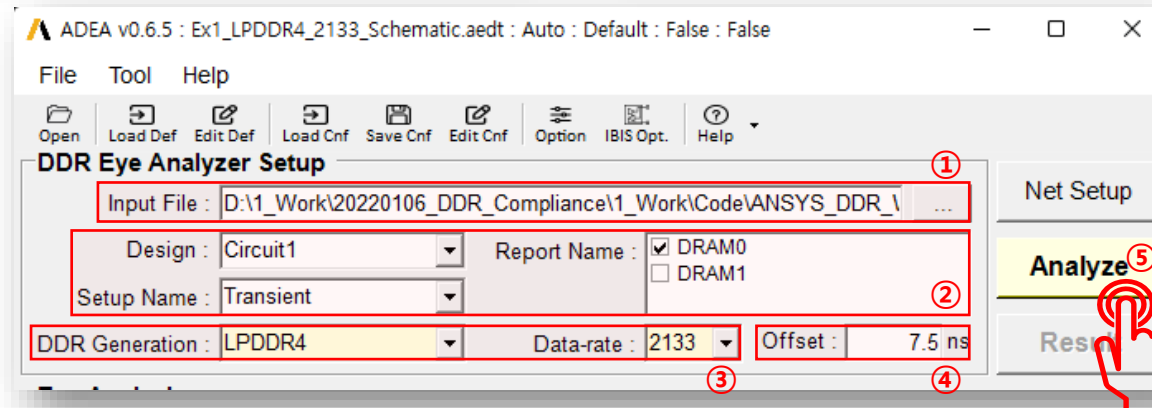
# User Guide – Ansys DDR Eye Analyzer : Eye Analyze



## 1. Launch ADEA



## 2. ADEA Setup



① Load **Input File** (\*.aedt).

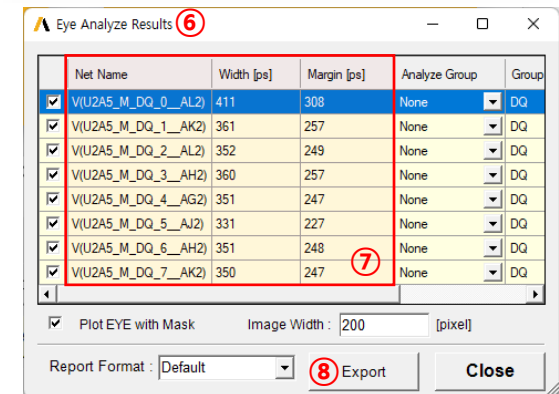
② Select **Design**, **Setup**, and **Report**.

③ Select **DDR Type** and **Data-rate**.

④ Enter **Offset** for eye analyze.

⑤ Click '**Analyze**'

## 4. Result



⑥ Result Window Pops up.

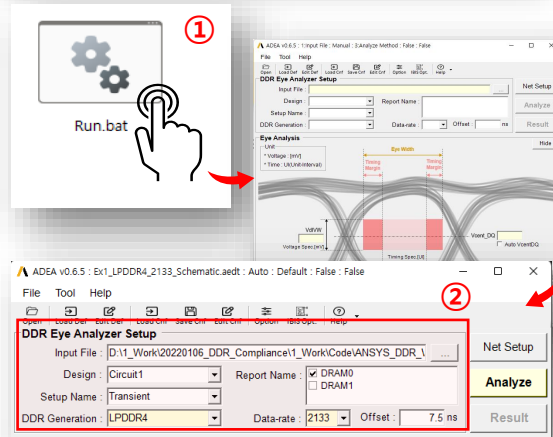
⑦ Check Analysis Results

⑧ Export Report (Optional)

# User Guide – Ansys DDR Eye Analyzer : IBIS Opt.



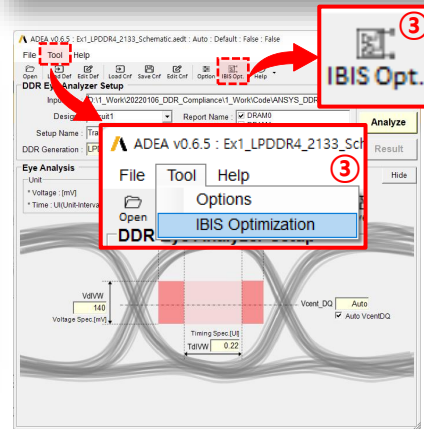
## 1. IBIS Opt. Setup



Same way as Eye Analyze

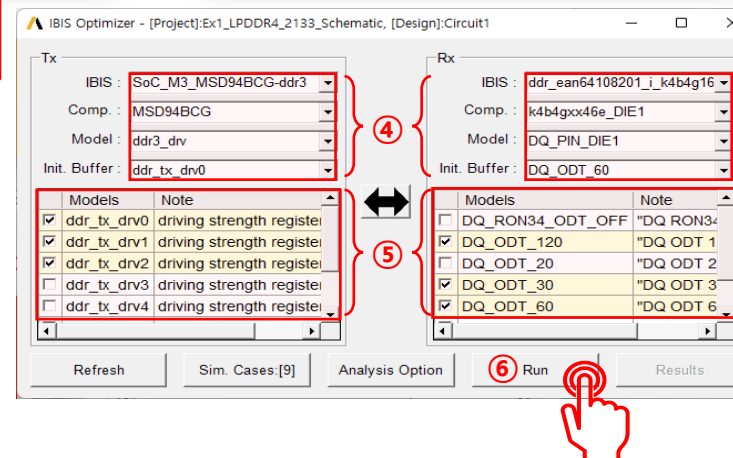
- ① Launch AEDA
- ② ADEA Setup

## 2. Sim. Case Setup



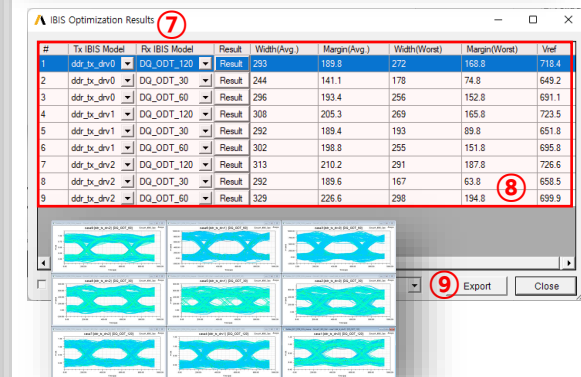
- ③ Click 'IBIS Opt.' Icon  
or Tool → IBIS Opt.
- ④ Check Tx & Rx IBIS Info.  
✓ IBIS file, Comp., Model, Initial Buffer
- ⑤ Select IBIS Models for Tx/Rx.

## 3. Analyze



- ⑥ Click 'Run'

## 4. Result



- ⑦ Result Window Pops Up.
- ⑧ Check Analysis Results.
- ⑨ Export Report (TBD)

# Eye Analyze

## 1. Launch ADEA

## 2. ADEA Setup

## 3. Analyze

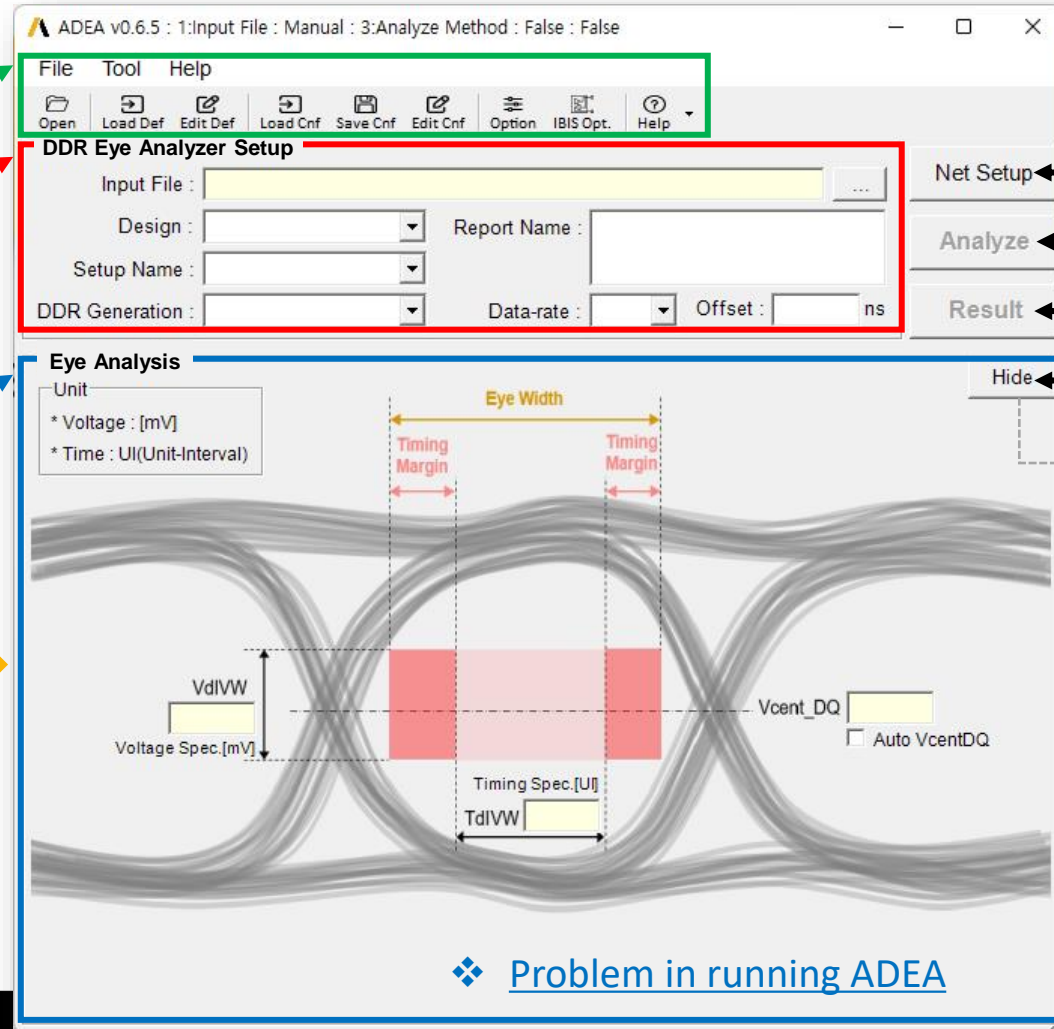
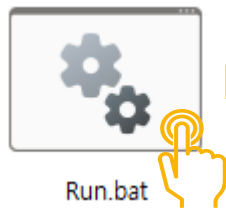
## 4. Result

- Launch ADEA using Run.bat file among the files provided.

Tool Strip Menu & Icons

Analyzer Setup

Specifications by DDR Type & Speed

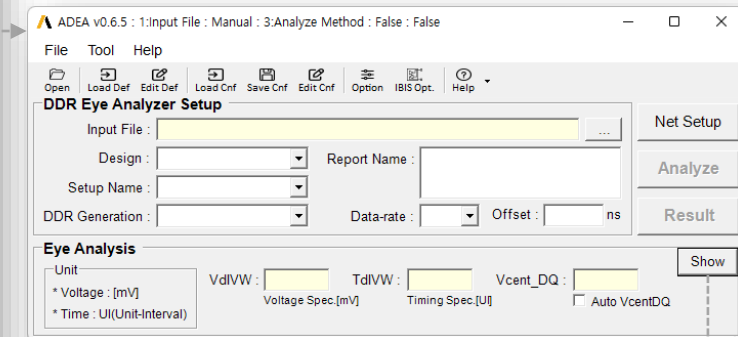


Target Net Setup

Analyze

View Analyze Result

GUI Size Control Button





# Eye Analyze

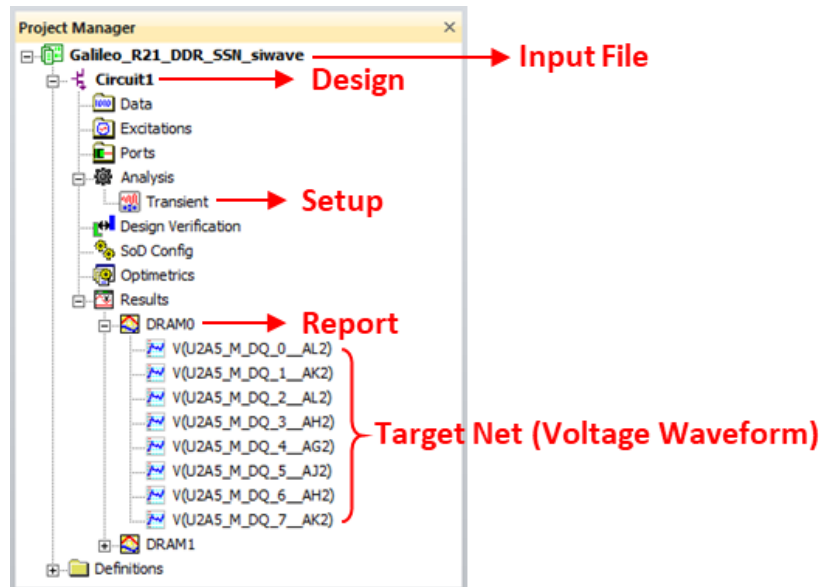
1. Launch ADEA

2. ADEA Setup

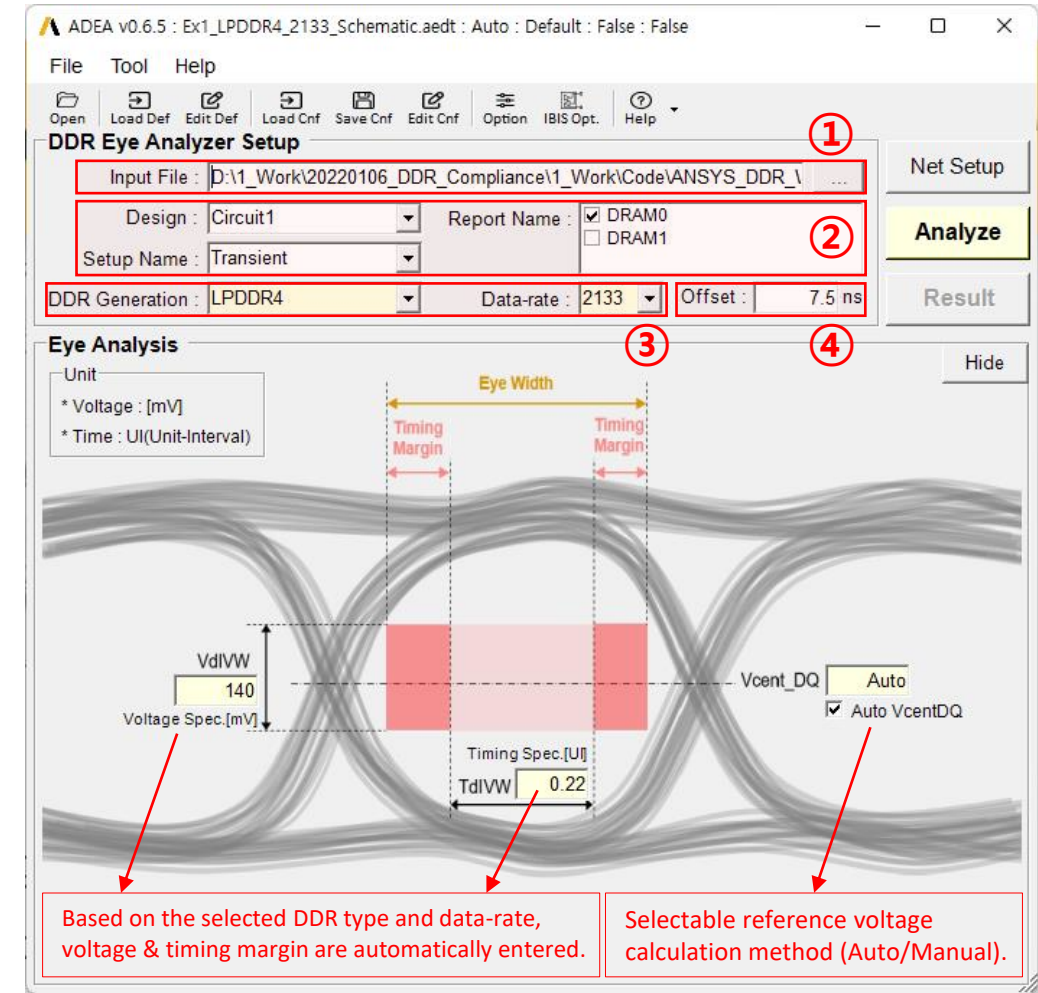
3. Analyze

4. Result

- ① Click  button or  Icon → Select Input File.
- ② Select Design, Setup, and Report to analyze.



- ③ Select DDR Type and Data-rate.
- ④ Enter Offset.





# Eye Analyze

1. Launch ADEA

2. ADEA Setup

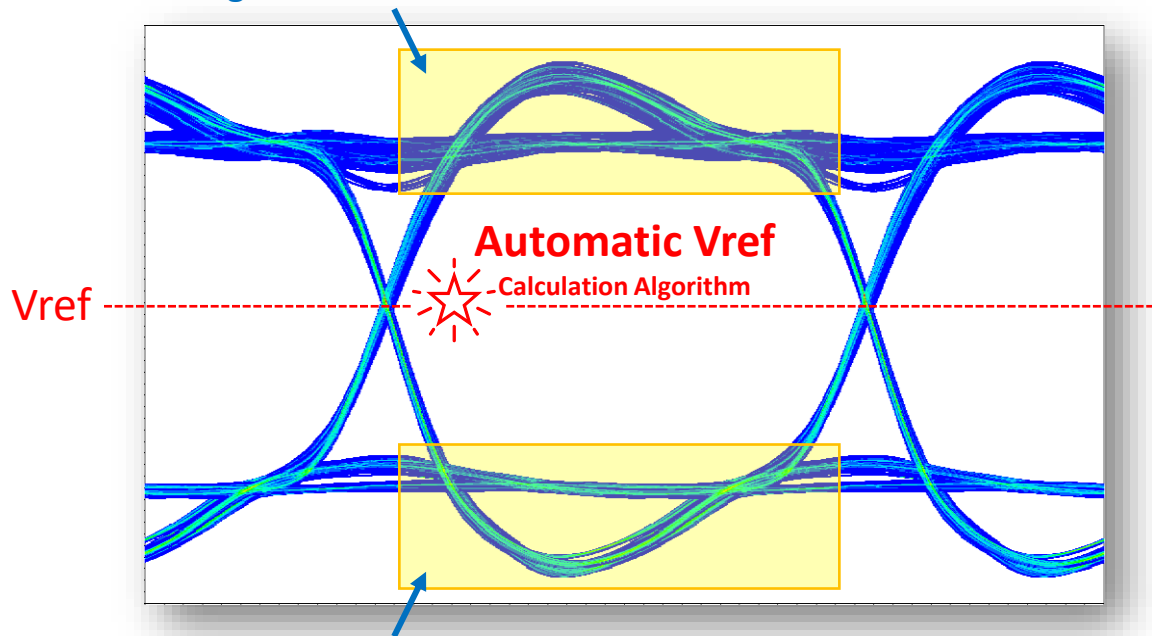
3. Analyze

4. Result

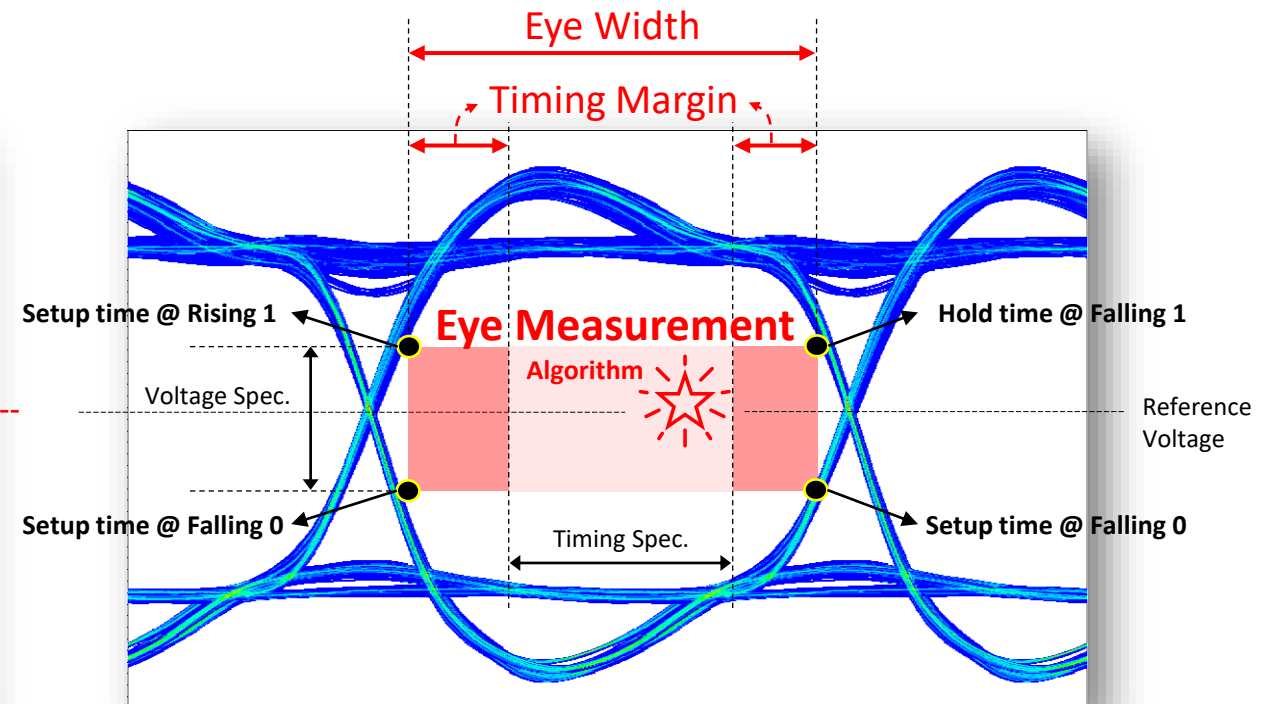
- Click the Analyze button to proceed with the analysis

- ✓ Reference voltage level calculation and eye measurement algorithms are built in.
- ✓ Customized reference voltage level calculation and/or eye measurement method can be added.

Statistical Logic 1 Level



Statistical Logic 0 Level



# Eye Analyze

1. Launch ADEA

2. ADEA Setup

3. Analyze

4. Result

- View the analysis result in the Result Window

- ✓ Possible to export built-in Excel report.
- ✓ HTML report is also available (TBD), and customization is possible easily in the format desired by the user.

The screenshot displays the ADEA v0.6.5 software interface. The 'DDR Eye Analyzer Setup' window is open, showing the 'Input File' as 'D:\1\_Work\20220106\_DDR\_Compliance\1\_Work\Code\ANSYS\_DDR\_1...'. The 'Design' is set to 'Circuit1', and the 'Report Name' is 'DRAM0'. The 'Setup Name' is 'Transient', and the 'DDR Generation' is 'LPDDR4'. The 'Data-rate' is '2133' and the 'Offset' is '7.5 ns'. The 'Eye Analysis' window is also open, showing the 'Unit' as 'Voltage: [mV]' and 'Time: UI(Unit/Interval)'. The 'Eye Analyze Results' window is open, displaying a table of analysis results. The 'Result window' is also open, showing a table of analysis results. The 'Eye Diagrams' window is open, showing multiple eye diagrams for different signals.

**Eye Analyze Results**

Net Name	Width [ps]	Margin [ps]	Analyze Group	Group
<input checked="" type="checkbox"/> V(U2A5_M_DQ_0_AL2)	339	236	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1_AK2)	332	229	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2_AL2)	319	216	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3_AH2)	350	247	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4_AG2)	320	217	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5_AJ2)	323	220	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_6_AH2)	321	218	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_7_AK2)	335	232	None	DQ

☐ Plot EYE with Mask

Report Format: Default

Export Close

**Result window**

	Analyze Group	Width [ps]	Jitter_RMS [ps]	Jitter [ps]	Timin Margin [ps]	Vcent_DQ [mV]
1 V(M_DQ_0_B3_G83568-001_U1B5)	None	417	N/A	0	314	823.6
3 V(M_DQ_1_C7_G83568-001_U1B5)	None	417	N/A	0	314	
G83568-001_U1B5)	None	420	N/A	0	317	
G83568-001_U1B5)	None	418	N/A	0	315	
G83568-001_U1B5)	None	417	N/A	0	314	
G83568-001_U1B5)	None	416	N/A	0	313	
G83568-001_U1B5)	None	417	N/A	0	314	
G83568-001_U1B5)	None	417	N/A	0	314	

**Eye Diagrams**

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21

DQ\_0 DQ\_1 DQ\_2 DQ\_3 DQ\_4 DQ\_5 DQ\_6 DQ\_7

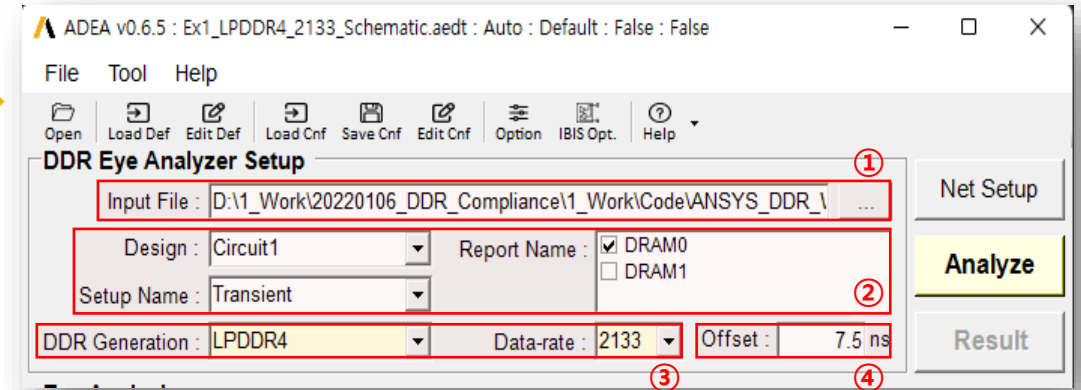
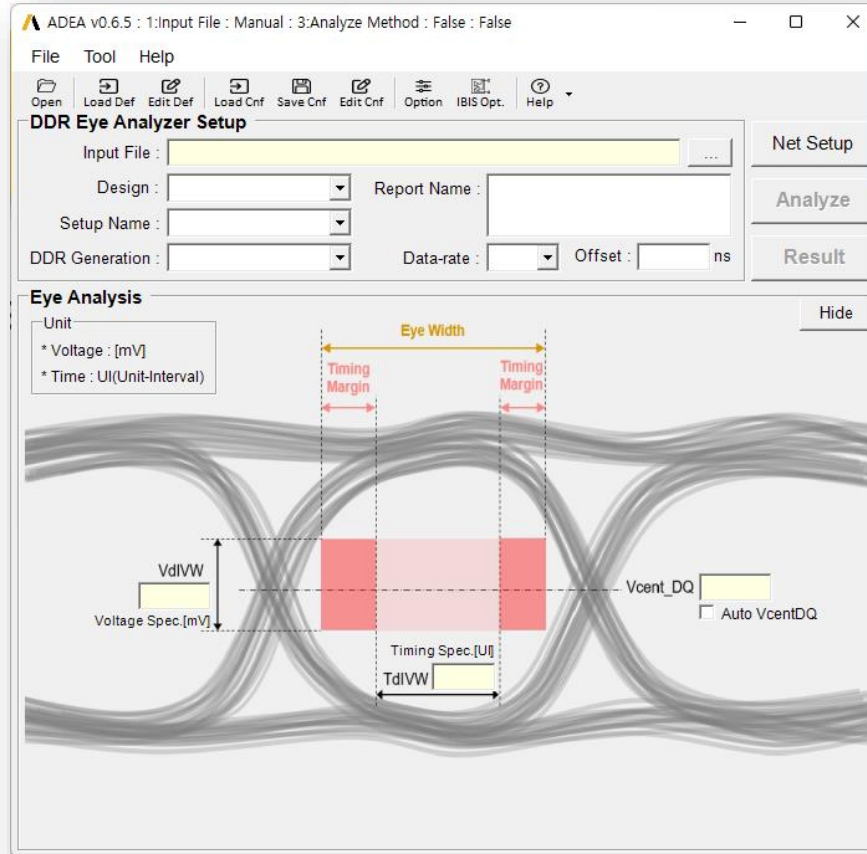
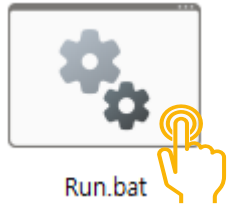
EYE Measure Results EYE Diagrams

Ready Accessibility Investigate

- Automatically pop-up the result window when the analysis is complete.
- Check the result of the timing analysis in the result window.
- Export eye and Excel report as required.

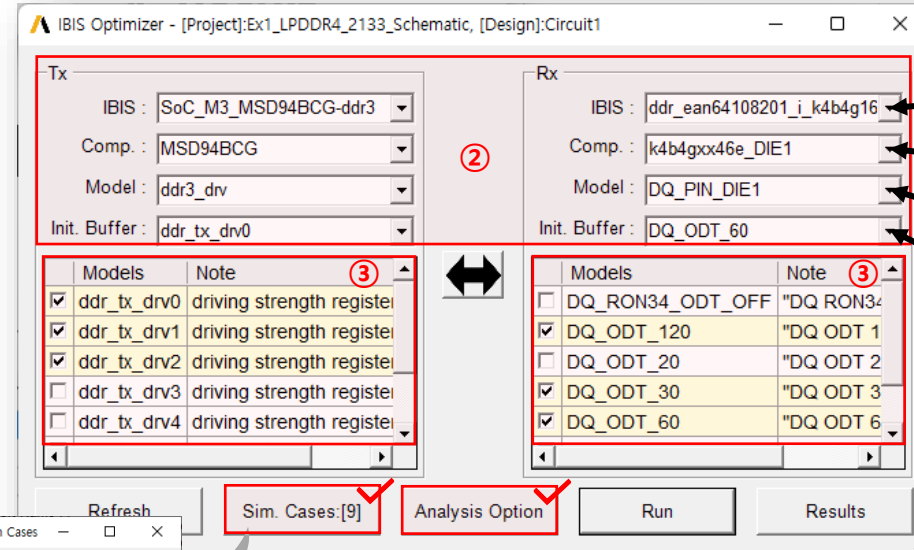
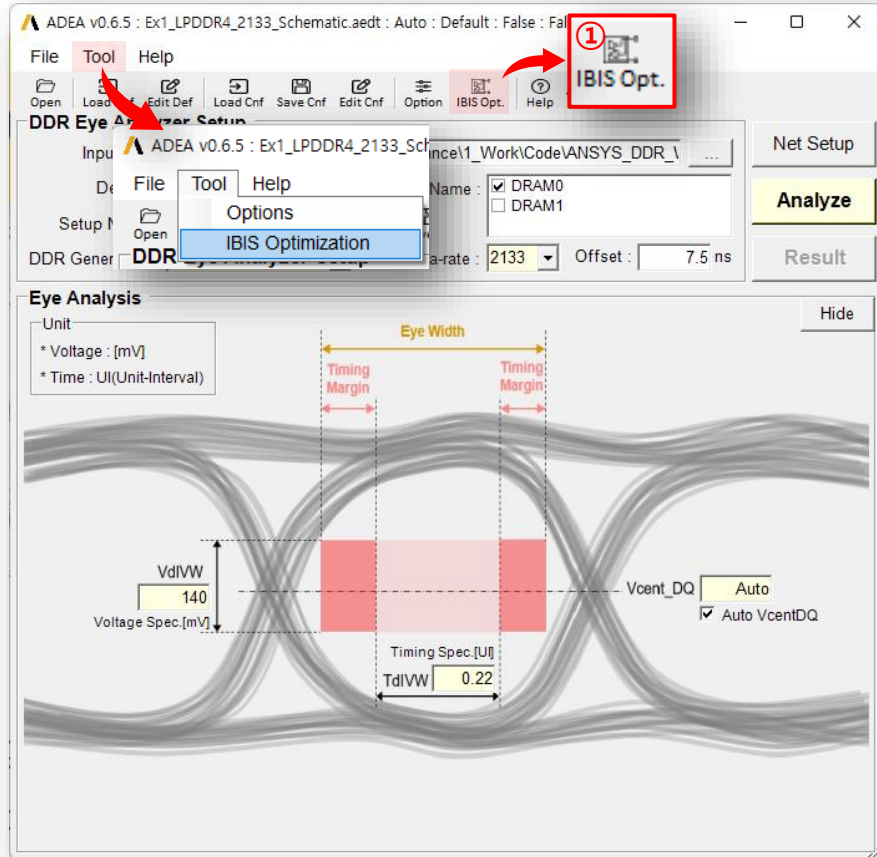


- Run ADEA and complete the ADEA setup in the same way as the Eye Analyze



- ① Select Input File (\*.aedt).
- ② Select Design, Setup Name, and Report.
- ③ Select DDR Type and Data-rate.
- ④ Enter Eye Offset.

- Run IBIS Optimizer and select IBIS and simulation case.



- IBIS File (\*.ibs)
- IBIS Component
- IBIS Model
- Initial Buffer model for input schematic

IBIS Simulation Cases

#	Tx IBIS Model	Rx IBIS Model
1	ddr_tx_drv0	DQ_ODT_120
2	ddr_tx_drv0	DQ_ODT_30
3	ddr_tx_drv0	DQ_ODT_60
4	ddr_tx_drv1	DQ_ODT_120
5	ddr_tx_drv1	DQ_ODT_30
6	ddr_tx_drv1	DQ_ODT_60
7	ddr_tx_drv2	DQ_ODT_120
8	ddr_tx_drv2	DQ_ODT_30
9	ddr_tx_drv2	DQ_ODT_60

Simulation Cases

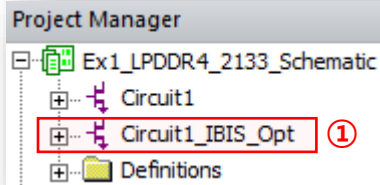
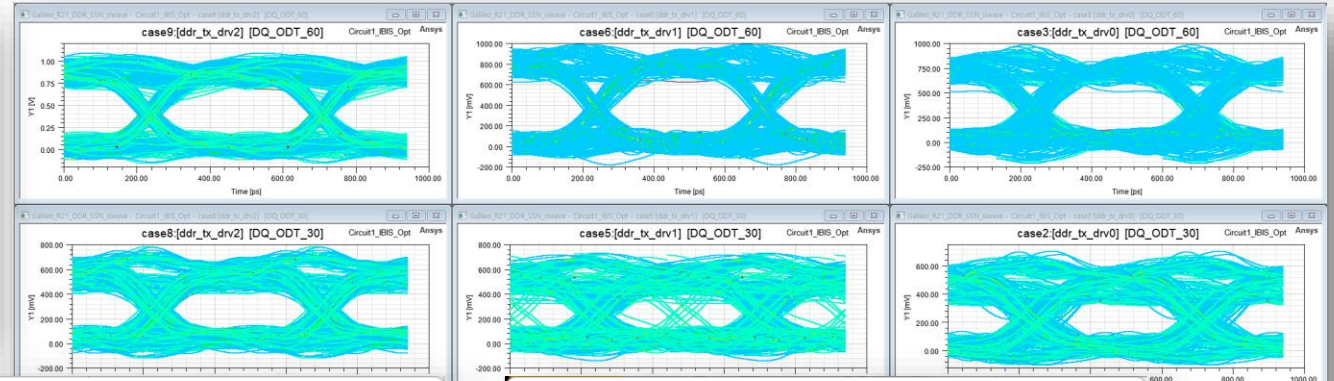
Add Delete Close

- Run IBIS Optimizer.
- Select and/or check
  - IBIS file, component, model, and initial buffer model.
- Select the Tx/Rx buffer models to be analyzed.
  - Check the Simulation cases.
  - Check Analysis option.

- Check the combination of Tx/Rx IBIS models

- Click the Run button to proceed with the analysis and check the results.

- Schematic for IBIS opt. is automatically created.
  - Automatically pop-up the result window.
- ✓ Check the detailed result for each simulation case.
  - ✓ Export eye and Excel report as required (TBD).



IBIS Optimization Results

#	Tx IBIS Model	Rx IBIS Model	Result	Width(Avg.)	Margin(Avg.)	Width(Worst)	Margin(Worst)	Vref
1	ddr_tx_drv0	DQ_ODT_120	Result	293	189.8	272	168.8	718.4
2	ddr_tx_drv0	DQ_ODT_30	Result	244	141.1	178	74.8	649.2
3	ddr_tx_drv0	DQ_ODT_60	Result	296	193.4	256	152.8	691.1
4	ddr_tx_drv1	DQ_ODT_120	Result	308	205.3	269	165.8	723.5
5	ddr_tx_drv1	DQ_ODT_30	Result	292	189.4	193	89.8	651.8
6	ddr_tx_drv1	DQ_ODT_60	Result	302	198.8	255	151.8	695.8
7	ddr_tx_drv2	DQ_ODT_120	Result	313	210.2	291	187.8	726.6
8	ddr_tx_drv2	DQ_ODT_30	Result	292	189.6	167	63.8	658.5
9	ddr_tx_drv2	DQ_ODT_60	Result	329	226.6	298	194.8	699.9

☐ Plot EYE
 Report Format: 
Export Close

Eye Analyze Results - IBIS case1

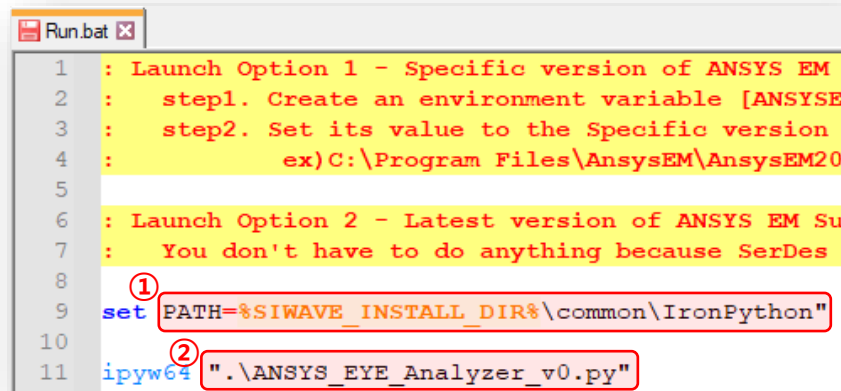
Net Name	Width [ps]	Margin [ps]	Analyze Group	Group
<input checked="" type="checkbox"/> V(U2A5_M_DQ_0__AL2)	294	190.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1__AK2)	277	173.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2__AL2)	300	196.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3__AH2)	308	204.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4__AG2)	295	191.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5__AJ2)	286	182.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_6__AH2)	272	168.82	None	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_7__AK2)	312	208.82	None	DQ

☐ Plot EYE with Mask
 Detailed Result for a Sim. Case
 Report Format: Default
Export Close

# Appendix A.1 – Launching ADEA

## ❑ Launch Ansys DDR Eye Analyzer using Run.bat file.

- If ADEA does not run using the Run.bat file, apply the following sequentially.



The screenshot shows a Windows batch file named 'Run.bat'. It contains two main sections for launching ANSYS EM. The first section, 'Launch Option 1', sets environment variables for a specific version of ANSYS EM (2021.2) and sets the PATH to the IronPython directory. The second section, 'Launch Option 2', is for the latest version. Two annotations are present: a red circle with the number 1 pointing to the PATH variable assignment in the first section, and a red circle with the number 2 pointing to the relative path for the Python script in the second section.

```
1 : Launch Option 1 - Specific version of ANSYS EM
2 :   step1. Create an environment variable [ANSYS_EYE_ANALYZER]
3 :   step2. Set its value to the Specific version
4 :   ex) C:\Program Files\AnsysEM\AnsysEM2021.2
5
6 : Launch Option 2 - Latest version of ANSYS EM Suite
7 :   You don't have to do anything because SerDes
8
9 ① set PATH=%SIWAVE_INSTALL_DIR%\common\IronPython"
10
11 ② ipyw64 ".\ANSYS_EYE_Analyzer_v0.py"
```

❖ [Setup the Version for Ansys Electronics Desktop](#)

A. Modify the path of ① to the absolute path where AEDT is installed.

ex) Before : `set PATH=%SIWAVE_INSTALL_DIR%\common\IronPython"`

After : `set PATH="C:\Program Files\AnsysEM\AnsysEM21.2\Win64\common\IronPython"`

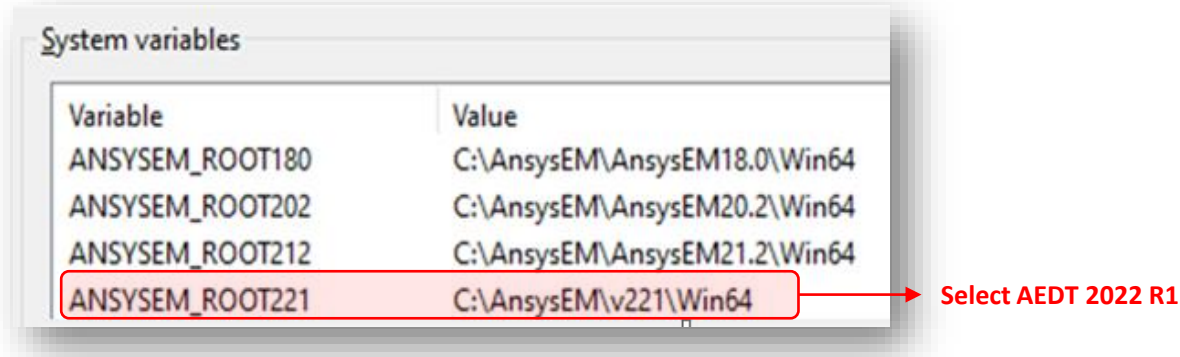
B. Modify ② to the absolute path of the file “ANSYS\_EYE\_Analyzer\_v0.py”.

- ✓ When using relative paths, the Run.bat file and “ANSYS\_EYE\_Analyzer\_v0.py” file must be in the same path.

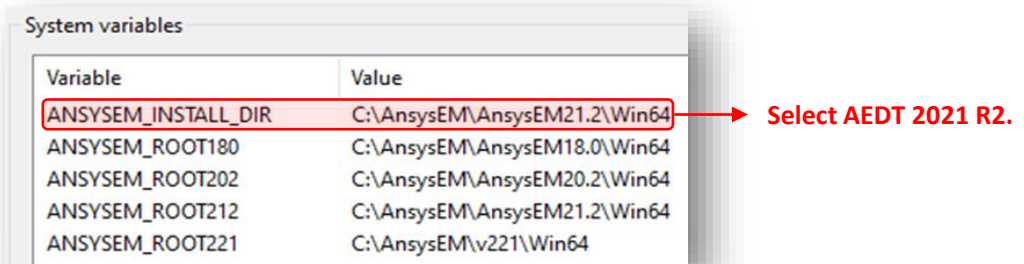
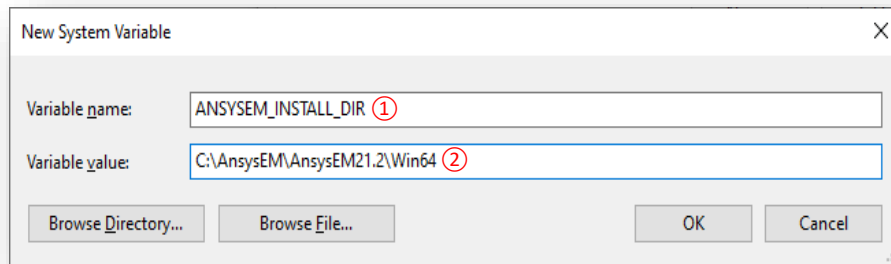
## Appendix A.2 – AEDT Version Selection

### ❑ Version Selection for Ansys Electronics Desktop(AEDT)

- By default, search for the system variable (ANSYSEM\_ROOTxxx) to automatically select the most recent AEDT version.



- If you want to use AEDT for a specific version,
  - ① Create the [ANSYSEM\_INSTALL\_DIR] system variable.
  - ② Set the AEDT installation path for the desired version to the value of the above system variable.

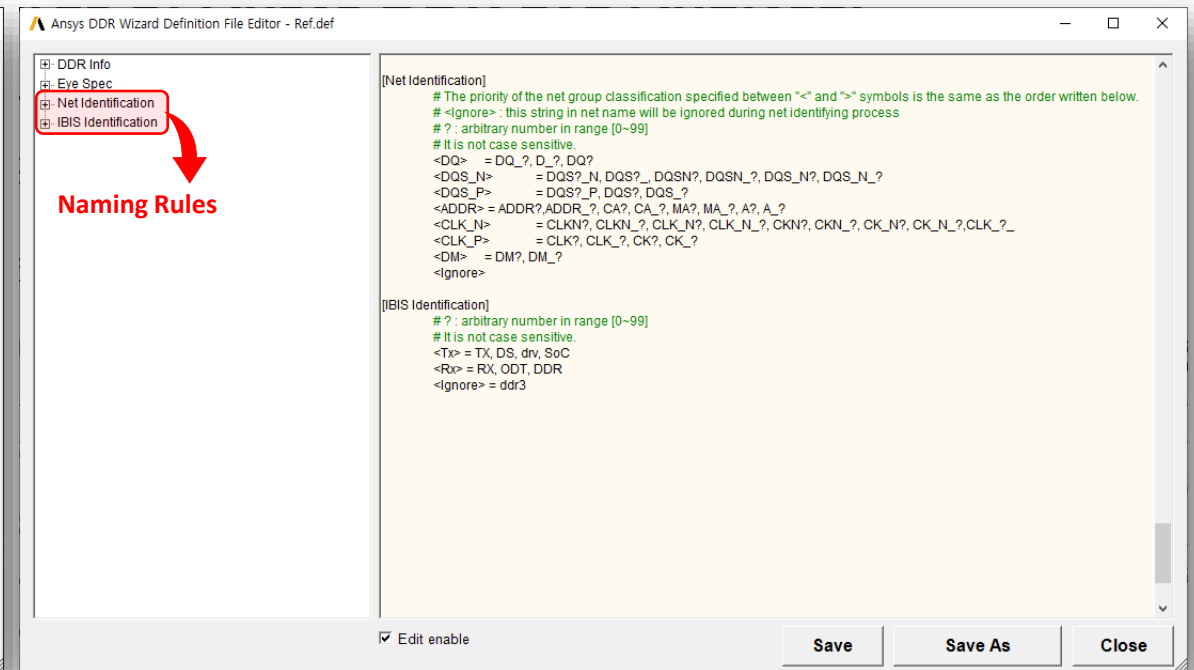
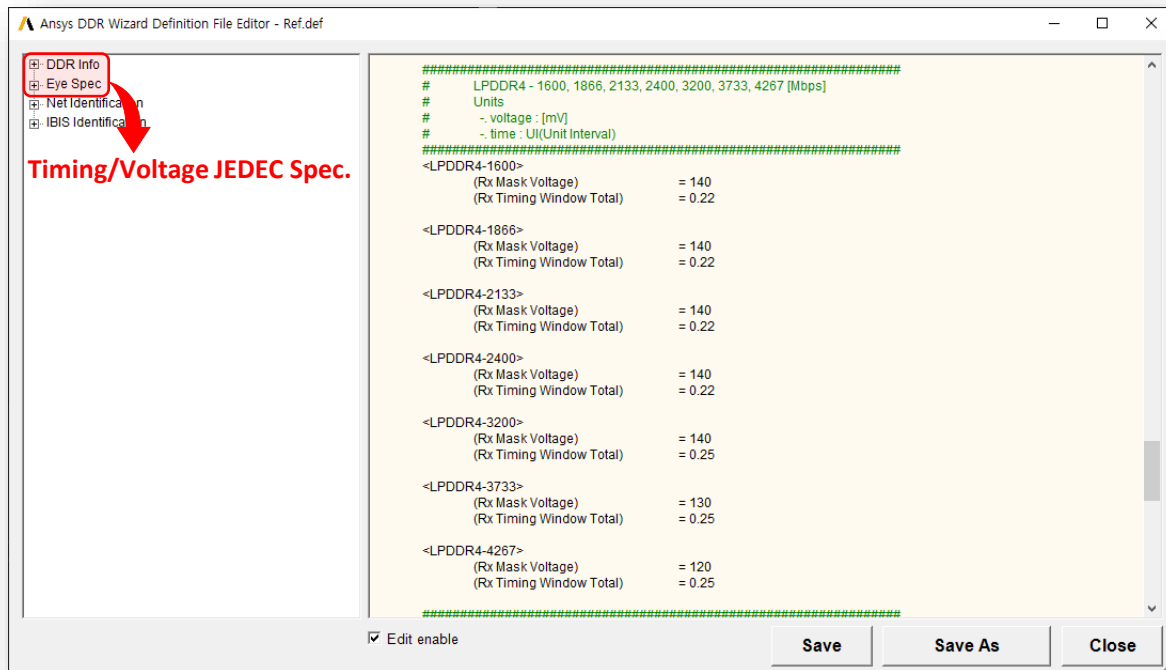
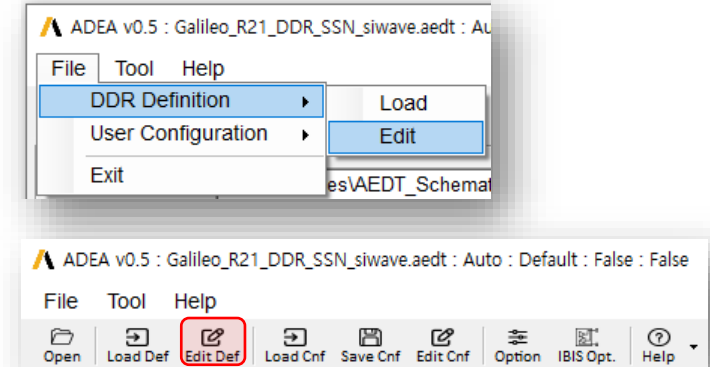




# Appendix B.1 – Pre-Configurations

## ❑ Definition File (\*.def)

- Timing/Voltage JEDEC specifications of (LP)DDR2/3/4/5 are defined.
- User can modify and/or add customized specifications.
- Naming rules for target net and IBIS model classification are defined. The rules can be modified and/or added.

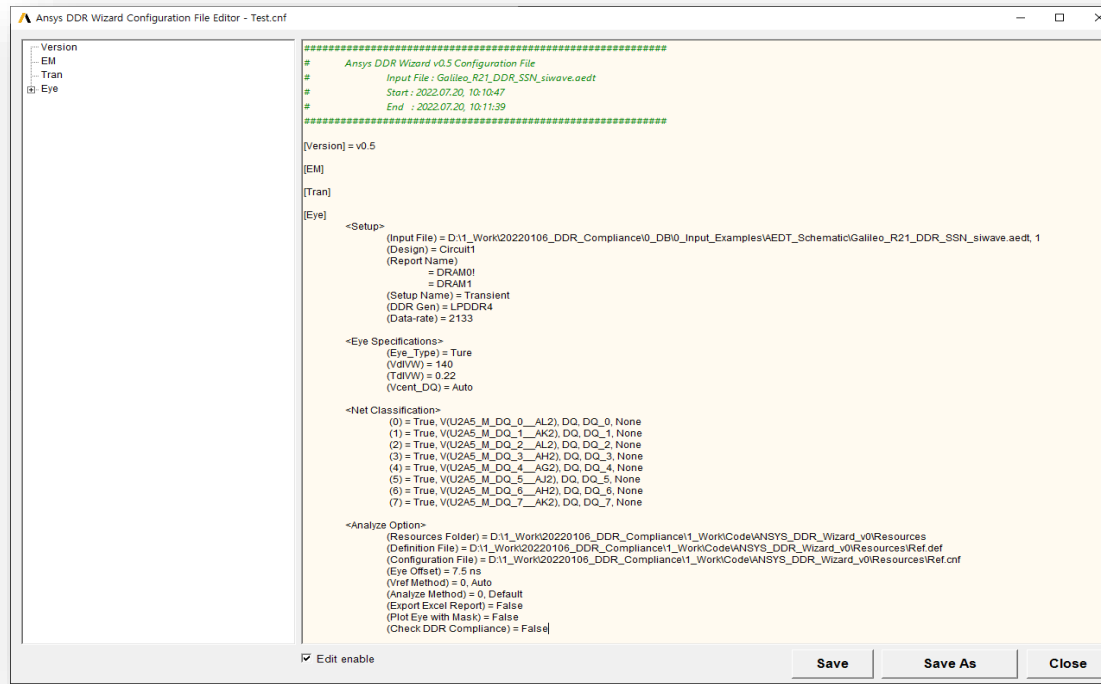
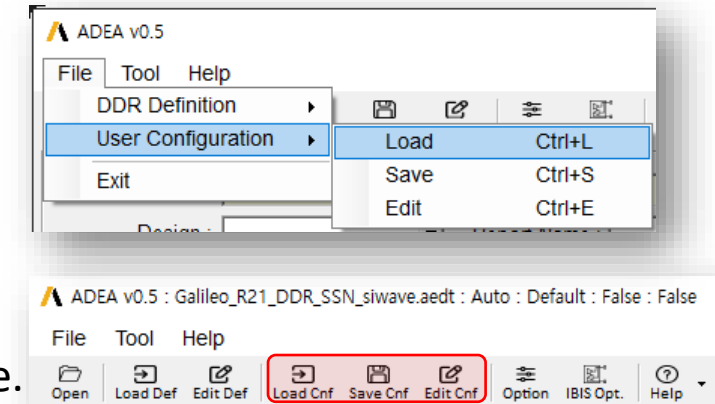




## Appendix B.2 – Pre-Configurations

### ❑ Configuration File (\*.cnf)

- All inputs for ADEA can be saved in the configuration file.
- All inputs for ADEA can be automatically filled by importing the configuration file.
- DDR Type and Data-rate are automatically saved and loaded for convenience.



```
#####  
#   Ansys DDR Wizard v0.5 Auto Saved Configuration File  
#   Input File :  
#   Start : 2022.07.17, 23:25:44  
#   End   : 2022.07.17, 23:25:51  
#####  
  
[Version] = v0.5  
  
[EM]  
  
[Tran]  
  
[Eye]  
  <Setup>  
    (DDR Gen) = LPDDR4  
    (Data-rate) = 3733
```

# Appendix B.3 – Automatic Net Classification

## Automatic Net Classification

- ADEA automatically classify the net to be analyzed into the following groups:

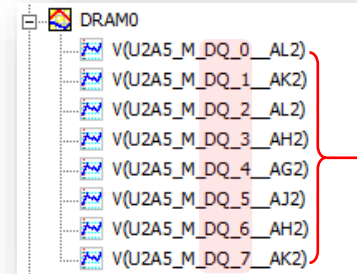
① DQ ② DQS\_N ③ DQS\_P ④ ADDR ⑤ CLK\_N ⑥ CLK\_P ⑦ DM

- It is automatically classified according to the 'Net Identification' rule defined in the definition file.

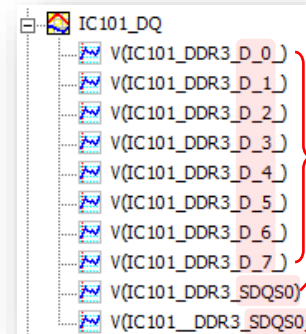
### [Net Identification]

```
# The priority of the net group classification specified between "<" and ">" symbols is the same as the order written below.
# <Ignore> : this string in net name will be ignored during net identifying process
# ? : arbitrary number in range [0~99]
# It is not case sensitive.
<DQ>    = DQ_?, D_?, DQ?
<DQS_N> = DQS?_N, DQS?_, DQSN?, DQSN_?, DQS_N?, DQS_N_?
<DQS_P> = DQS?_P, DQS?, DQS_?
<ADDR>  = ADDR?, ADDR_?, CA?, CA_?, MA?, MA_?, A?, A_?
<CLK_N> = CLKN?, CLKN_?, CLK_N?, CLK_N_?, CKN?, CKN_?, CK_N?, CK_N_?, CLK_?
<CLK_P> = CLK?, CLK_?, CK?, CK_?
<DM>    = DM?, DM_?
<Ignore>
```

- The 'Net Identification' rule can be modified and/or added.



<DQ> = DQ\_?, D\_?, DQ?  
Classify DQ Group.




<DQ> = DQ\_?, D\_?, DQ?  
Classify DQ Group.

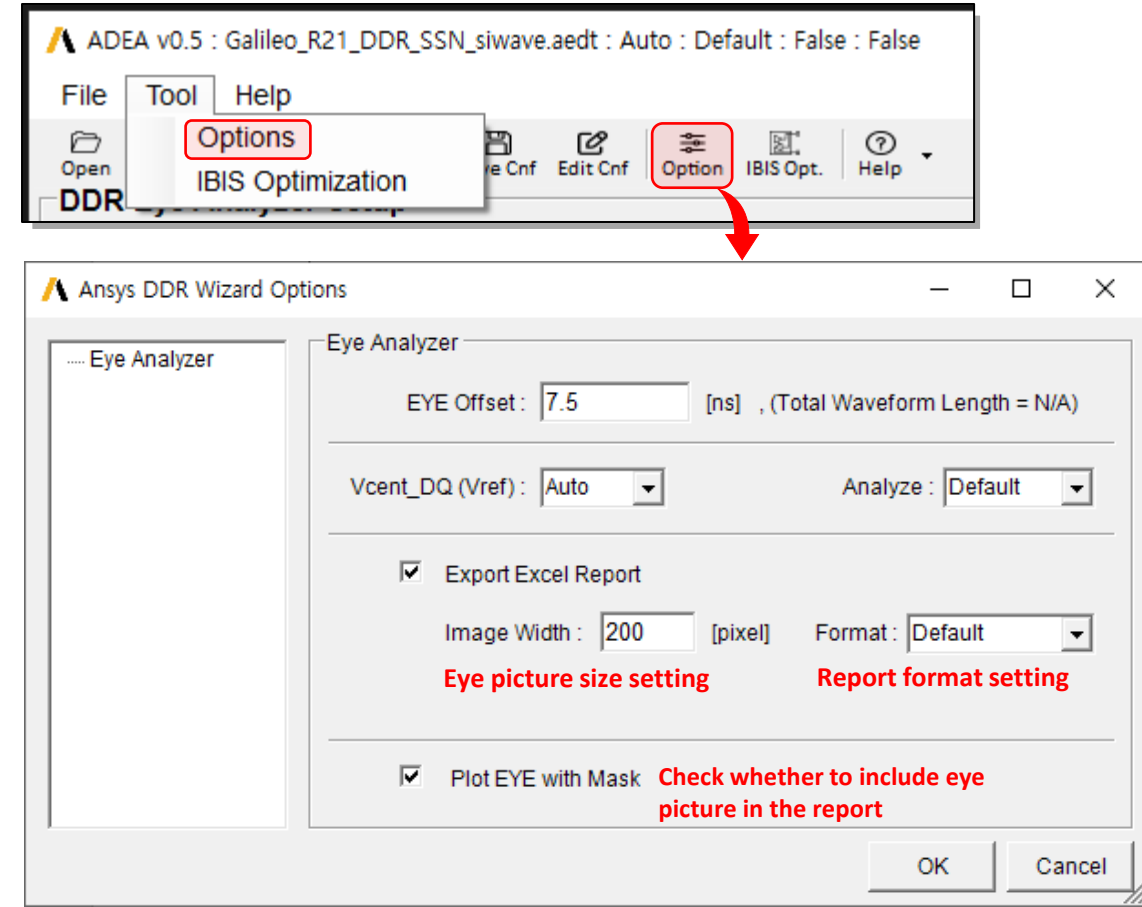
<DQS\_P> = DQS?\_P, DQS?, DQS\_?  
Classify DQS\_P Group.

<DQS\_N> = DQS?\_N, DQS?, DQSN?, DQSN\_?,  
Classify DQS\_N Group.

# Appendix C.1 – Analysis Option Setup

## ❑ Ansys DDR Eye Analyzer – Option setup

- Click Tool → Option Menu or  Icon.
- In the Option Window, enter the settings for eye analysis.
  - ✓ Eye Offset : Enter the offset for voltage waveform.
  - ✓ Vcent\_DQ(Vref) : Select voltage reference calculation method.
  - ✓ Analyze : Select eye measurement algorithm
  - ✓ Export Excel : Check whether to export the Excel report or not.
- The reference voltage calculation method, eye measurement method, and report format can be customized by request.



**Option Setup process can be skipped when analyze with default option setup.**

# Appendix C.2 – Target Net Setup

## Target Net Setup

- DQ groups among auto-classified groups are automatically checked as target net.
- Target nets can also be set and/or un-set by checking or unchecking the net.
- Net groups can also be manually set using the dropdown button.
- Using the Analyze Group, nets can be analyzed as a group.

Analyze Group :    → Automatic grouping according to the DQ number

- ✓ If the Analyze Group is not set up, analyze it as an individual net.

Net Name	Group	Matched String	Analyze Group
<input checked="" type="checkbox"/> V(U2A5_M_DQ_0__AL2)	DQ	DQ_0	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1__AK2)	DQ	DQ_1	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2__AL2)	DQ	DQ_2	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3__AH2)	DQ	DQ_3	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4__AG2)	DQ	DQ_4	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5__AJ2)	DQ	DQ_5	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_6__AH2)	DQ	DQ_6	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_7__AK2)	DQ	DQ_7	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_8__AT2)	DQ	DQ_8	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_9__AP2)	DQ	DQ_9	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_10__A...	DQ	DQ_10	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_11__A...	DQ	DQ_11	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_12__A...	DQ	DQ_12	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_13__A...	DQ	DQ_13	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_14__A...	DQ	DQ_14	None
<input checked="" type="checkbox"/> V(U2A5_M_DQ_15__A...	DQ	DQ_15	None

→ Analysis for each Bit line.

Net Name	Group	Matched String	Analyze Group
<input checked="" type="checkbox"/> V(U2A5_M_DQ_0__AL2)	DQ	DQ_0	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1__AK2)	DQ	DQ_1	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2__AL2)	DQ	DQ_2	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3__AH2)	DQ	DQ_3	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4__AG2)	DQ	DQ_4	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5__AJ2)	DQ	DQ_5	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_6__AH2)	DQ	DQ_6	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_7__AK2)	DQ	DQ_7	Byte0
<input checked="" type="checkbox"/> V(U2A5_M_DQ_8__AT2)	DQ	DQ_8	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_9__AP2)	DQ	DQ_9	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_10__A...	DQ	DQ_10	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_11__A...	DQ	DQ_11	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_12__A...	DQ	DQ_12	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_13__A...	DQ	DQ_13	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_14__A...	DQ	DQ_14	Byte1
<input checked="" type="checkbox"/> V(U2A5_M_DQ_15__A...	DQ	DQ_15	Byte1

→ Grouping analysis for Byte lane

<input checked="" type="checkbox"/> V(U2A5_M_DQ_0__AL2)	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_1__AK2)	DM
<input checked="" type="checkbox"/> V(U2A5_M_DQ_2__AL2)	DQ
<input checked="" type="checkbox"/> V(U2A5_M_DQ_3__AH2)	DQS_P
<input checked="" type="checkbox"/> V(U2A5_M_DQ_4__AG2)	DQS_N
<input checked="" type="checkbox"/> V(U2A5_M_DQ_5__AJ2)	CLK_P
<input checked="" type="checkbox"/> V(U2A5_M_DQ_6__AH2)	CLK_N
<input checked="" type="checkbox"/> V(U2A5_M_DQ_7__AK2)	ADDR
<input checked="" type="checkbox"/> V(U2A5_M_DQ_8__AT2)	OTHER

Dropdown Menu for net group selection

Target Net Setup - latest.cnf

Net Name	Group	Matched String	Analyze Group
<input checked="" type="checkbox"/> Test_A1	ADDR	A1	None
<input type="checkbox"/> Test_A11	ADDR	A11	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_0__B2)	DQ	DQ_0	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_1__C2)	DQ	DQ_1	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_2__C2)	DQ	DQ_2	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_3__C2)	DQ	DQ_3	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_4__E2)	DQ	DQ_4	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_5__E2)	DQ	DQ_5	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_6__D2)	DQ	DQ_6	None
<input checked="" type="checkbox"/> V(U1B5_M_DQ_7__E2)	DQ	DQ_7	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_8__B2)	DQ	DQ_8	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_9__C2)	DQ	DQ_9	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_10__C2)	DQ	DQ_10	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_11__C2)	DQ	DQ_11	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_12__E2)	DQ	DQ_12	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_13__E2)	DQ	DQ_13	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_14__D2)	DQ	DQ_14	None
<input checked="" type="checkbox"/> V(U1A1_M_DQ_15__E2)	DQ	DQ_15	None
<input type="checkbox"/> V(U1A1_M_DQS_1__C2)	DQS_P	DQS_1	None
<input type="checkbox"/> V(U1A1_M_DQS_N_1__...	DQS_N	DQS_N_1	None

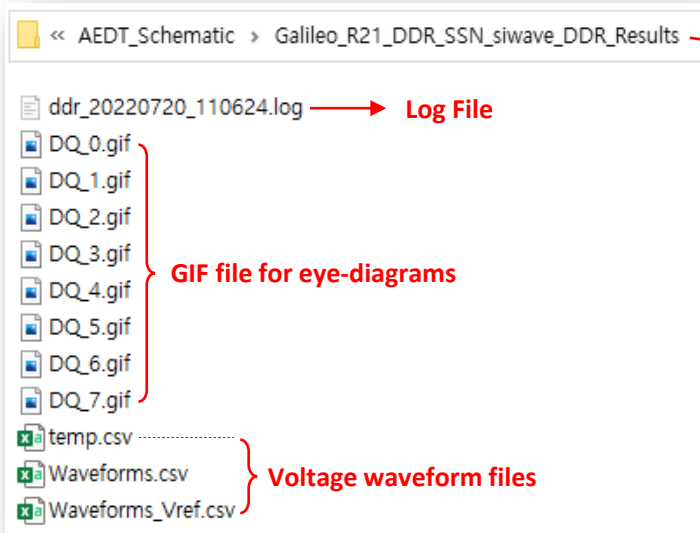
Analyze Group :

Modify and apply rule

# Appendix D – Eye Measurement Results

## □ Eye Measurement Results

- The Result Window is automatically pop-up, after the analysis complete.
- User can check the eye width and timing margin by bit or byte.
- After checking the results, user can export the report.
- Result files such as \*.log file and eye diagram GIF file are generated.



Automatically create folder  
"{Input file name}\_DDR\_Results"

	Net Name	Width [ps]	Margin [ps]	Analyze Group	Group
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_0__AL2)	375	272	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_1__AK2)	368	265	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_2__AL2)	360	257	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_3__AH2)	381	278	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_4__AG2)	336	233	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_5__AJ2)	359	256	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_6__AH2)	373	270	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_7__AK2)	355	251	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_8__AT2)	386	283	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_9__AP2)	386	283	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_10__A...	375	272	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_11__A...	374	271	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_12__A...	379	276	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_13__A...	368	265	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_14__A...	399	296	None	DQ
<input checked="" type="checkbox"/>	V(U2A5_M_DQ_15__A...	367	264	None	DQ

☒ Plot EYE with Mask    Image Width : 200 [pixel]

Report Format : Default    **Export**    **Close**

# Appendix E – IBIS File and Model Selection

## IBIS File and Model Selection

- The IBIS file and model in Tx/Rx are automatically classified according to the IBIS identification rule in Def. file.

### [IBIS Identification]

# ? : arbitrary number in range [0~99]  
# It is not case sensitive.  
<Tx> = TX, DS, drv, SoC  
<Rx> = RX, ODT, DDR  
<Ignore> = ddr3

U23:ddr\_tx\_drv0\_msd94bcg-ddr3 Properties: Galileo\_R21\_DDR\_SSN\_siwave

Parameter Values	Component	Symbol	Property Displays
<input checked="" type="radio"/> Value <input type="radio"/> Statistics			
Name	Value		
file	SoC_M3_MSD94BCG-ddr3.ibs		
model	ddr_tx_drv0		

U16:DQ\_ODT\_60\_DDR\_EAN64108201\_i\_k4b4g1646e\_bcxx\_june23 Prop

Parameter Values	Component	Symbol	Property Displays
<input checked="" type="radio"/> Value <input type="radio"/> Statistics			
Name	Value		
file	DDR_EAN64108201_i_k4b4g1646e_bcxx_june23.ibs		
model	DQ_ODT_60		

- IBIS identification rule can be modified and added.
- IBIS File, Comp., and Model can be selected manually.
- Select the Tx and Rx models to analyze.
- Simulation cases can be checked by Sim. Cases:[9] button.

IBIS Optimizer - [Project]:Galileo\_R21\_DDR\_SSN\_siwave, [Design]:Circuit1

**Tx**

IBIS : SoC\_M3\_MSD94BCG-ddr3 View

Comp. : MSD94BCG

Model : ddr3\_drv

Models	Note
<input checked="" type="checkbox"/> ddr_tx_drv0	driving strength register
<input checked="" type="checkbox"/> ddr_tx_drv1	driving strength register
<input checked="" type="checkbox"/> ddr_tx_drv2	driving strength register
<input type="checkbox"/> ddr_tx_drv3	driving strength register
<input type="checkbox"/> ddr_tx_drv4	driving strength register

Sim. Cases:[9] Analysis Option

**Rx**

IBIS : DDR\_EAN64108201\_i\_k4 View

Comp. : k4b4gxx46e\_DIE1

Model : DQ\_PIN\_DIE1

Models	Note
<input type="checkbox"/> DQ_RON34_ODT_OFF	"DQ RON34
<input type="checkbox"/> DQ_ODT_120	"DQ ODT 1
<input checked="" type="checkbox"/> DQ_ODT_20	"DQ ODT 2
<input checked="" type="checkbox"/> DQ_ODT_30	"DQ ODT 3
<input checked="" type="checkbox"/> DQ_ODT_60	"DQ ODT 6

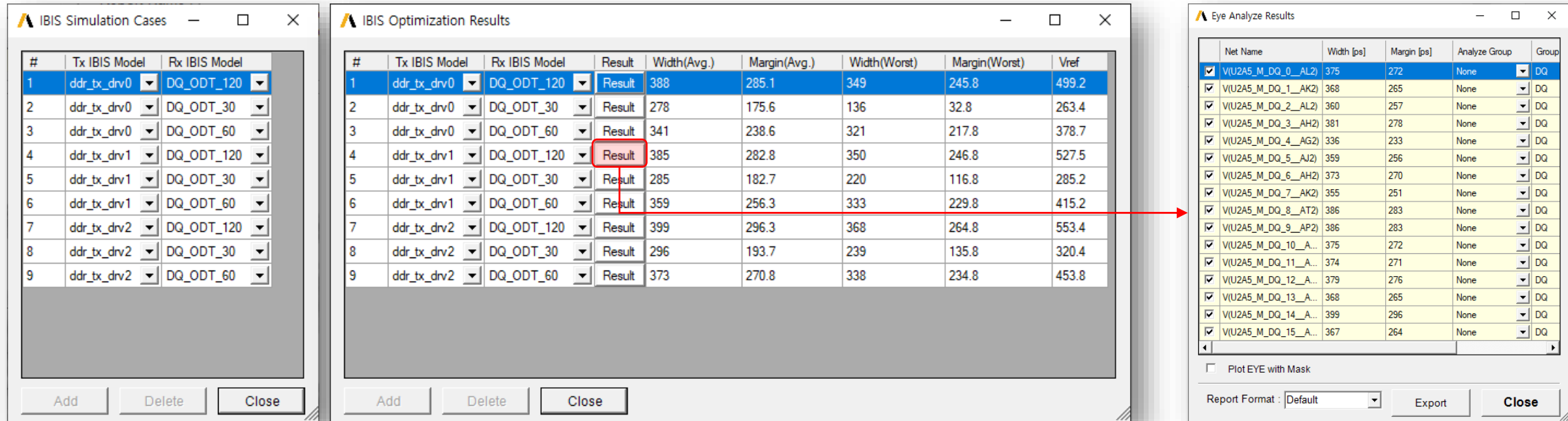
Run Results



# Appendix F – IBIS Optimization Results

## IBIS Optimization Results

- The eye analyze results for the simulation cases are automatically pop up.



The 'IBIS Simulation Cases' window displays a list of simulation cases with columns for case number, Tx IBIS Model, and Rx IBIS Model. The 'IBIS Optimization Results' window shows a table of results for these cases, including Width(Avg.), Margin(Avg.), Width(Worst), Margin(Worst), and Vref. The 'Eye Analyze Results' window shows a detailed table of eye analysis results for the selected case, including Net Name, Width [ps], Margin [ps], Analyze Group, and Group.

#	Tx IBIS Model	Rx IBIS Model	Result	Width(Avg.)	Margin(Avg.)	Width(Worst)	Margin(Worst)	Vref
1	ddr_tx_drv0	DQ_ODT_120	Result	388	285.1	349	245.8	499.2
2	ddr_tx_drv0	DQ_ODT_30	Result	278	175.6	136	32.8	263.4
3	ddr_tx_drv0	DQ_ODT_60	Result	341	238.6	321	217.8	378.7
4	ddr_tx_drv1	DQ_ODT_120	Result	385	282.8	350	246.8	527.5
5	ddr_tx_drv1	DQ_ODT_30	Result	285	182.7	220	116.8	285.2
6	ddr_tx_drv1	DQ_ODT_60	Result	359	256.3	333	229.8	415.2
7	ddr_tx_drv2	DQ_ODT_120	Result	399	296.3	368	264.8	553.4
8	ddr_tx_drv2	DQ_ODT_30	Result	296	193.7	239	135.8	320.4
9	ddr_tx_drv2	DQ_ODT_60	Result	373	270.8	338	234.8	453.8

Net Name	Width [ps]	Margin [ps]	Analyze Group	Group
V(U2A5_M_DQ_0__AL2)	375	272	None	DQ
V(U2A5_M_DQ_1__AK2)	368	265	None	DQ
V(U2A5_M_DQ_2__AL2)	360	257	None	DQ
V(U2A5_M_DQ_3__AH2)	381	278	None	DQ
V(U2A5_M_DQ_4__AG2)	336	233	None	DQ
V(U2A5_M_DQ_5__AJ2)	359	256	None	DQ
V(U2A5_M_DQ_6__AH2)	373	270	None	DQ
V(U2A5_M_DQ_7__AK2)	355	251	None	DQ
V(U2A5_M_DQ_8__AT2)	386	283	None	DQ
V(U2A5_M_DQ_9__AP2)	386	283	None	DQ
V(U2A5_M_DQ_10__A...	375	272	None	DQ
V(U2A5_M_DQ_11__A...	374	271	None	DQ
V(U2A5_M_DQ_12__A...	379	276	None	DQ
V(U2A5_M_DQ_13__A...	368	265	None	DQ
V(U2A5_M_DQ_14__A...	399	296	None	DQ
V(U2A5_M_DQ_15__A...	367	264	None	DQ

- Eye width and timing margin for each case are represented by the average and worst values of the target net.
- Click the **Result** button to see the detailed analysis results for each case.