RESEARCH PROJECT-2

Project Title	Engineering of High Performance Signal Processing Elements for Real-time Infrastructure
Abstract	This proposal states an FPGA prototype based digital signal co-processor architecture, which can perform variable precision fixed and floating point elementary signal processing operations such as addition, subtraction, shift, logical operation, multiplication, multiply-accumulation, and CORDIC. Here, the proposed multiplier-cum-accumulator (MAC) is to perform multiplication or MAC without any change in the hardware, where the previous MAC result is fed as one of the partial products to carry save stages of the multiplier. In this proposed co-processor architecture, CORDIC is added as one of the functional units, where the number of iterations can be variable and the special functions can be computed by defining the values in the instruction field. This co-processor will be used to perform the Video Compression with Ethernet/10GBaseR interconnect between the FPGA and PC.
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Name of the Co-PI(s) with affiliation	NIL
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