

Troubleshooting Guide

MICROLOK® II System Maintenance

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NOTE

Wiring diagrams in this manual depict typical high-level installation applications and are provided to demonstrate hardware design theory and typical system operation. Always refer to the project Book of Plans (BOP) of a particular location for actual circuit wiring.

NOTE

Except as noted, information in this guide supersedes that of the SM-6800 series manuals.

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1 SYSTEM TROUBLESHOOTING

The system log and system event log can be very useful when troubleshooting MICROLOK® II unit malfunctions. Information placed in these logs falls into three general categories, as described below (Refer to Section 13.3 and 14.2.2).

1.1 Critical Errors

Result from fault conditions that cause the unit to fail and restart or shutdown.

- Failure of any internal test causes logging of a critical error and either restart or shutdown of the unit.
- Failure of a test that verifies proper operation of hardware is generally due to a component failure, and is correctable by replacing the component indicated in the critical error message.
- Failure of a test that verifies the correct operation of executive hardware may be correctable in the short-term only by reconfiguring the MICROLOK II installation or modifying the application program to avoid the situation that caused the critical error. Critical errors like these for which no user corrective action is suggested, requires that the ASTS USA RAIL team be consulted for assistance.

1.2 Warnings

Result from fault conditions that may cause the unit to operate improperly, but do not cause a restart or shutdown of the unit.

- Warnings usually result from the malfunction of equipment external to the MICROLOK II unit, or from minor, recoverable internal malfunctions. Warnings should be taken seriously, especially if they occur repeatedly and if they are not readily explainable. Warnings should not routinely appear.

1.3 Events

Result from the occurrence of good or bad conditions that might be of interest to anyone troubleshooting or monitoring the performance of the MICROLOK II unit.

- The system error log contains only a record of critical errors resulting from the last fifty failures that caused a controlled unit restart or a unit shutdown. The system event log includes everything in the system error log, along with informational warnings and events generated during normal system operation.
- Typically, event messages are information and require no corrective action. They simply contain information that may be of interest to anyone that

troubleshoots or maintains the MICROLOK II unit. They are logged on the occurrence of significant but routine events that occur during operation of the unit.



2 Central Processor Unit (CPU)

CPU – N17061301

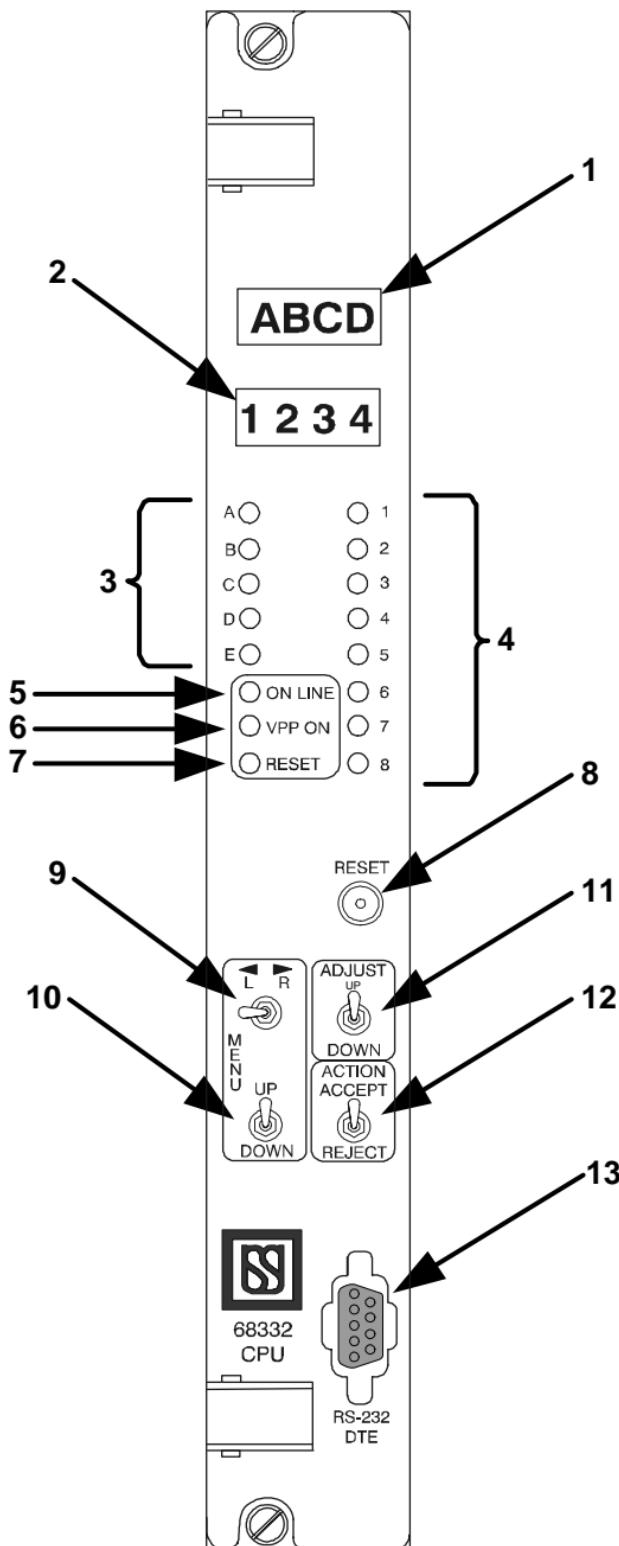


Figure 2-1.CPU Front Panel Detail

Note: Switches 9 through 12 shown toggled to depict direction of operation. Switches are spring return-to-center at rest.

Table 2-1.CPU Indicators/Controls

REF FIGURE 2-1	LABEL	DEVICE	PURPOSE
1, 2	(none)	Two, four-character alphanumeric displays Top display is Red Bottom display is Green	On-site configuration programming menus and options. Normal operating display is: <ul style="list-style-type: none"> • The upper four-character display will continuously scroll the phrase "US&S MICROLOK II." • The lower four-character display will continuously scroll the application name.
3	A, B, C, D, E	LEDs (Yellow)	<i>Select serial port with CPU front panel switches (9, 10, 11, & 12) via the on-line serial test menu (See Section 13.5).</i> A – Selected serial link is transmitting data. B – Selected serial link has received a valid message. C – Selected serial link has recognized the address in a received message. D – Selected serial link is receiving a DCD signal. E – Selected serial link has detected a receiver error.
4	1, 2, 3, 4, 5, 6, 7, 8	LEDs (Red)	User-defined in application software.
5	ON LINE	LED (Green)	Lit indicates normal system operation (successful diagnostics). If out: reset system.

REF FIGURE 2-1	LABEL	DEVICE	PURPOSE
6	VPP ON (Voltage Input Flash Programming)	LED (Yellow)	When lit, indicates FLASH +5V or +12V programming voltage enabled (via CPU PCB jumper). Lit only during programming on CPUs without PCMCIA card installed. Lit continually on CPUs with PCMCIA card installed.
7	RESET	LED (Red)	When lit, indicates that the system is in reset mode. Normal operation = Off
8	RESET	Momentary pushbutton	When pressed, resets the CPU. Also used to place the CPU in the reset mode.
9	MENU L/R	Three-position (spring return-to-center) toggle switch	Used to search main program menu items shown on displays.
10	MENU UP/DOWN	Three-position (spring return-to-center) toggle switch	Used to select main program menu items shown on displays.
11	ADJUST UP/DOWN	Three-position (spring return-to-center) toggle switch	Used to cycle through configuration values shown on displays.
12	ACTION ACCEPT/REJECT	Three-position (spring return-to-center) toggle switch	Executes or cancels menu items shown on displays.
13	RS-232 DTE Diagnostic Link Connector	DB9, RS-232 connector (DTE)	Used for connection to PC laptop computer for system monitoring/diagnosis

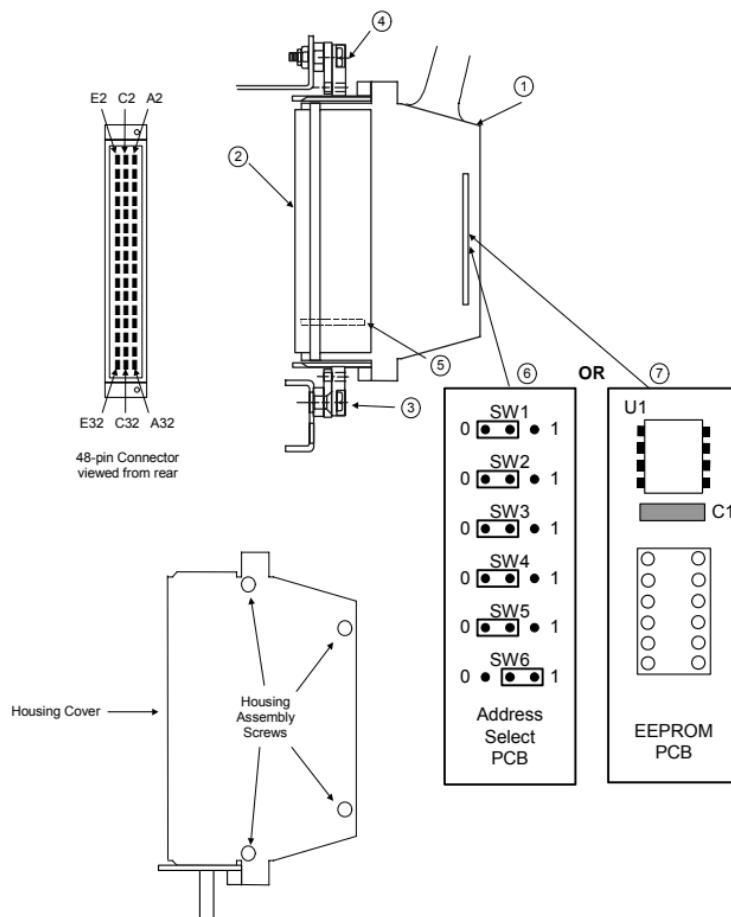


Figure 2-2.PCB Top Wiring Connector Address PCB

2.1 PCB Top Connector Wiring Interface

Refer to Figure 2-2 for PCB top connector pin configuration and Figure 2-4 for PCB pin-out information.

2.2 CPU Jumpers

When replacing a MICROLOK II CPU PCB with another CPU PCB, ensure that the jumpers are positioned as indicated in the Book of Plans for that particular location.

The application for the location will need to be uploaded to the new CPU. The Flash jumpers on the CPU must be positioned correctly before uploading the program (See Table 2-2).

Section 2

Central Processor Unit (CPU)

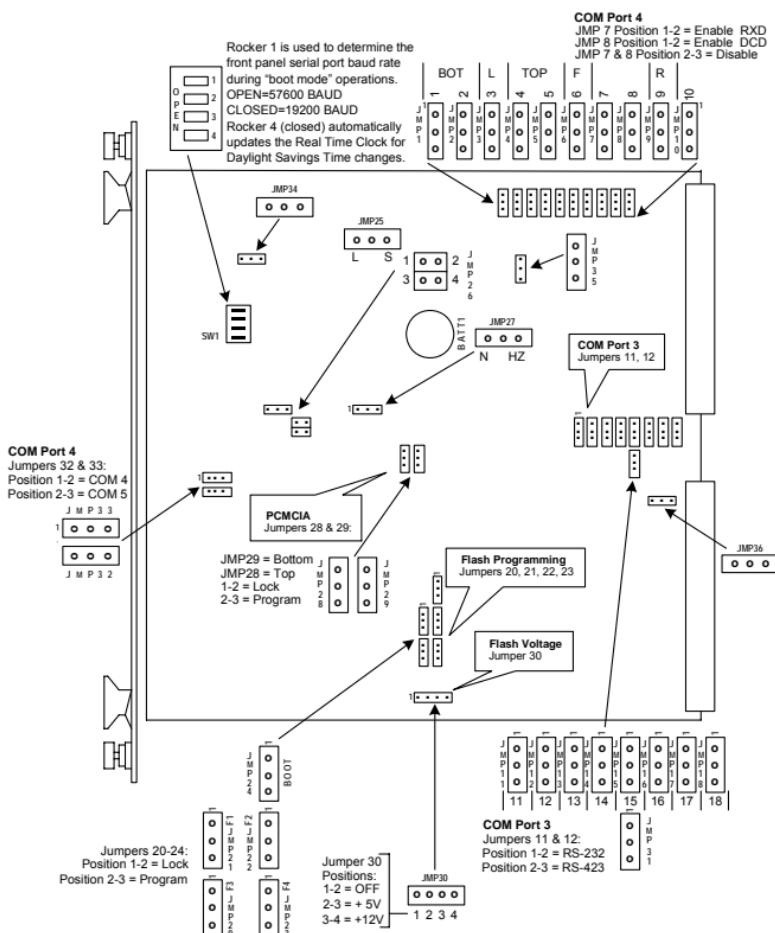


Figure 2-3.CPU PCB Jumper and Jumper Positions

(Example Only)

Table 2-2.CPU Jumpers

REFER TO FIGURE 2-3	DESCRIPTION	POSITION	NOTE
JMP1	Bottom Personal Computer Memory Card International Assoc.(PCMCIA) 2 Wait States	Position 2-3	
JMP2		Not installed	
JMP3	On-Board Random Access Memory (RAM) 1 Wait State	Position 2-3	1
JMP4	Top PCMCIA 2 Wait States	Position 2-3	
JMP5		Not installed	
JMP6	FLASH 1 Wait State	Position 2-3	1
JMP7	Enable COMM4 Receive Data (RXD)	Position 1-2	
JMP8	Enable COMM4 Data Carrier Detect (DCD)	Position 1-2	
JMP9	Disable Backplane CPU Reset	Position 1-2	
JMP10	COMM1 TX.CLK is an Output (Transmit Clock)	Position 2-3	
JMP11	COMM3 Voltage Drive Levels	RS-232 RS-423	Position 1-2 Position 2-3
JMP12	COMM3 Voltage Drive Levels	RS-232 RS-423	Position 1-2 Position 2-3
JMP13	COMM3 TX.CLK is an Output	Position 2-3	
JMP14	COMM3 TX.CLK is an Output	Position 1-2	
JMP15	COMM4 RX.CLK=9.83Mhz (Receive Clock)	Position 1-2	
JMP16	COMM3 RX.CLK=9.83Mhz	Position 1-2	
JMP17	COMM2 RX.CLK=9.83Mhz	Position 1-2	
JMP18	COMM1 RX.CLK=9.83Mhz	Position 1-2	
JMP19	Not Available	N/A	
JMP20	FLASH 3 Programming Language (Application space)	Locked Program	Position 1-2 Position 2-3
JMP21	FLASH 1 Programming Language (Executive space)	Locked Program	Position 1-2 Position 2-3

Section 2

Central Processor Unit (CPU)

REFER TO FIGURE 2-3	DESCRIPTION	POSITION	NOTE
JMP22	FLASH 2 Programming Language (Executive space) Locked Program	Position 1-2 Position 2-3	2
JMP23	FLASH 4 Programming Language (Application space) Locked Program	Position 1-2 Position 2-3	2
JMP24	FLASH 1 Boot Block (Boot space) Locked Program	Position 1-2 Position 2-3	2
JMP25	Speaker Volume Soft Loud Off	Position 2-3 Position 1-2 Not Installed	
JMP26	IRQ7 Off	Position 2-4	
JMP27	68332 Normal	Position 1-2	1
JMP28	Top PCMCIA Programming Voltage Locked Program	Position 1-2 Position 2-3	2
JMP29	Bottom PCMCIA Programming Voltage Locked Program	Position 1-2 Position 2-3	2
JMP30	FLASH Programming Voltage <i>Use only 5V for MICROLOK II CPUs</i> Off 5V 12V	Position 1-2 Position 2-3 Position 3-4	2
JMP31	Conditional Power Supply (CPS) Drive Normal	Position 1-2	1
JMP32	J1 Com Port Transmit (Tx) Select May be used to redirect the front diagnostics serial port to J1 connector. *Com 4 Com 5	Position 1-2 Position 2-3	3

REFER TO FIGURE 2-3	DESCRIPTION	POSITION	NOTE
JMP33	J1 Com Port Receive (Rx) Select May be used to redirect the front diagnostics serial port to J1 rear connector.	*Com 4 Com 5	Position 1-2 Position 2-3 3
JMP34	External +5VBAT Zener Diode Select (regulates to 3.3 volts) Use only when fixed power supply (Not Lithium Battery) feeds +5VBAT line and where additional current drain is not an issue.	*Disable Enable	Position 1-2 Position 2-3 3
JMP35	Real Time Clock (RTC) Coin Battery Enable	*Disable Enable	Position 1-2 Position 2-3 3
JMP36	Backplane SYS.CLK Always disable SYS.CLK from Backplane when not required.	*Enable Disable	Position 1-2 Position 2-3 3

The Position Column indicates default jumper settings. Dependent upon PCB serial number, jumpers may be soldered. Bold text without note indicates the recommended setting for user configurable jumpers. Always refer to the location's Book of Plans for specific settings.

Notes:

If header posts are not installed in these locations, no jumper is required.

Settings shown in boldface are the jumper positions that lock the FLASH devices and prevent their contents from being modified. Refer to SM-6800B FLASH Programming and PCMCIA instructions for further information.

*Denotes settings to ensure compatibility as N1700130x replacement.

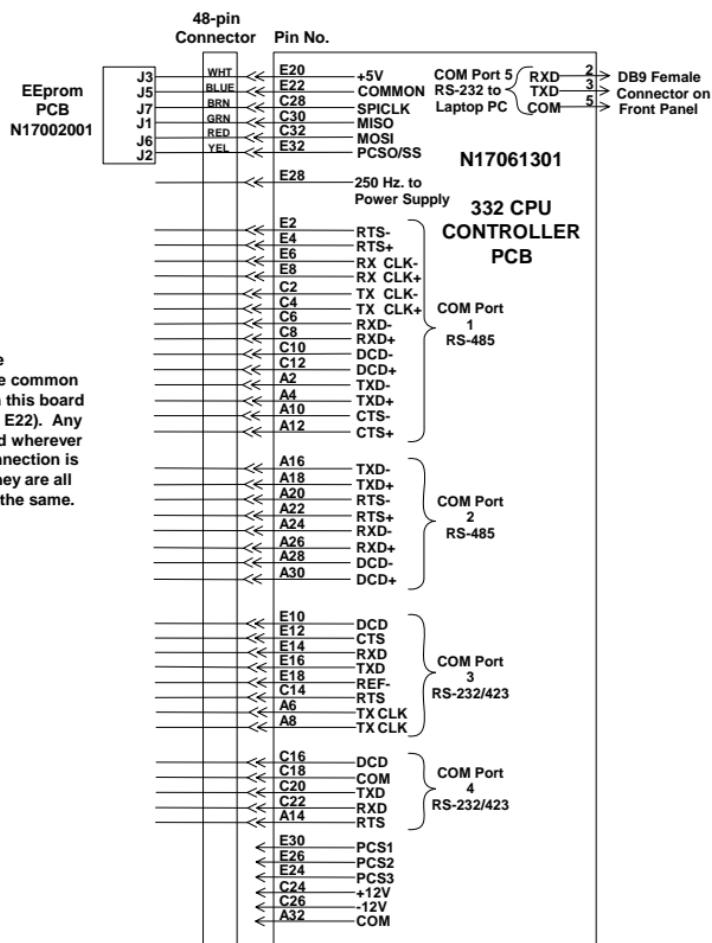


Figure 2-4.CPU PCB Top Connector Pin-Outs



3 POWER SUPPLY/CPS

Power Supply/Conditional Power Supply (CPS) – N16660301

or

N16661203

CPS only PCB – N451910-7501

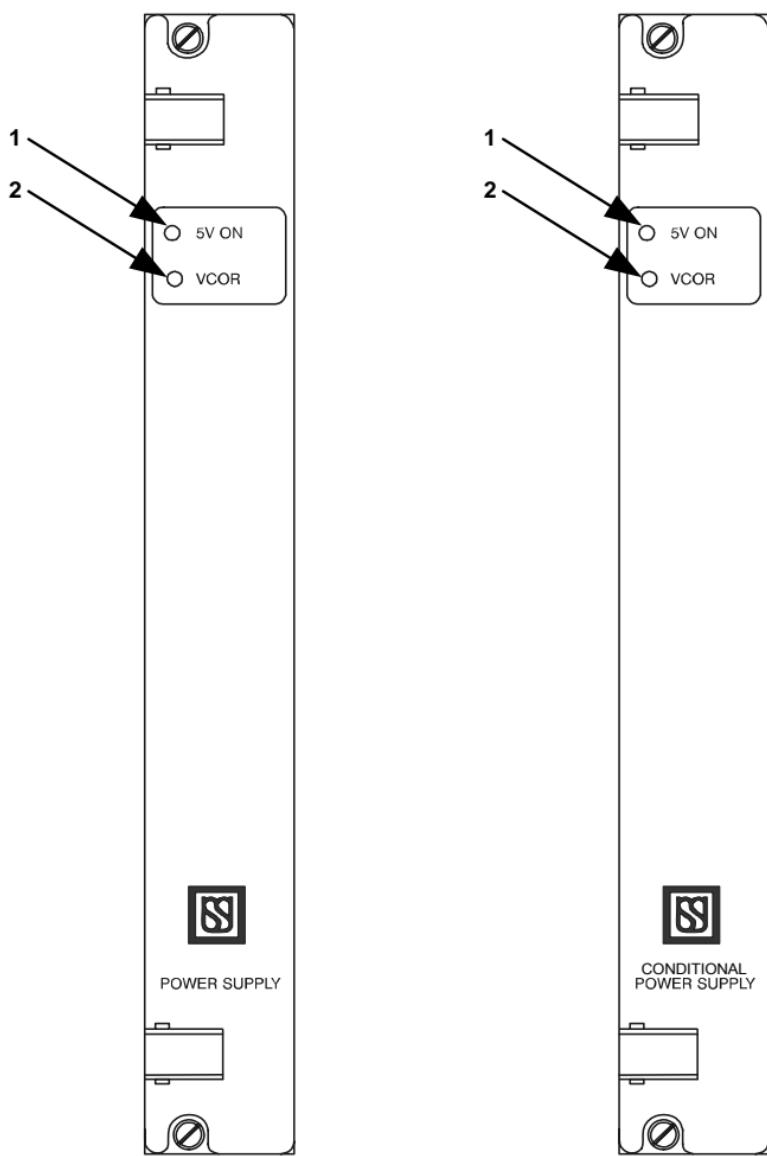


Figure 3-1.Power Supply/CPS Front Panel Detail

Table 3-1.Power Supply/CPS Indicators

REF FIGURE 3-1	LABEL	DEVICE	PURPOSE
1	5V ON	Green LED	When lit, indicates 5V operating power "On" to other cardfile PCBs.
2	VCOR	Green LED	When lit, indicates conditional power "On" to Vital Cut-Off relay (VCOR) relay (CPU diagnostics normal). If not lit refer to Section 12.2.

Table 3-2.Power Supply/CPS PCBs Specifications

ASTS USA PART	INPUT POWER	+ 5V OUTPUT	+ 12V OUTPUT	- 12V OUTPUT	ISOLATED OUTPUT	CPS OUTPUT
N16660301	9.8VDC to 16.2VDC (Auto off at 9.8, 11.5 min for turn-on)	3 amps	1 amp	1 amp	11.5VDC @ 20ma 510 Ω load 14VDC unloaded	- 13V ref to N12 VCOR 400 Ω relay
N16661203	9.8VDC to 32VDC (Auto off at 9.8 and 32, 11.5 min for turn-on)	5 amps	1 amp	2 amps	11.5VDC @ 20ma 510 Ω load 14VDC unloaded	- 9.5V ref to N12 VCOR 400 Ω relay
N451910-7501	+5V +12V	-	-	-	-	- 9.5V ref to N12 VCOR 400 Ω relay

CAUTION

While the N1661203 PCB detects overvoltage (above 32VDC) and removes PCB operating voltage to the cardfile; it does **not** disconnect system battery from the Power Supply PCB input. A continuing condition of system battery in excess of 32VDC will damage the Power Supply PCB.

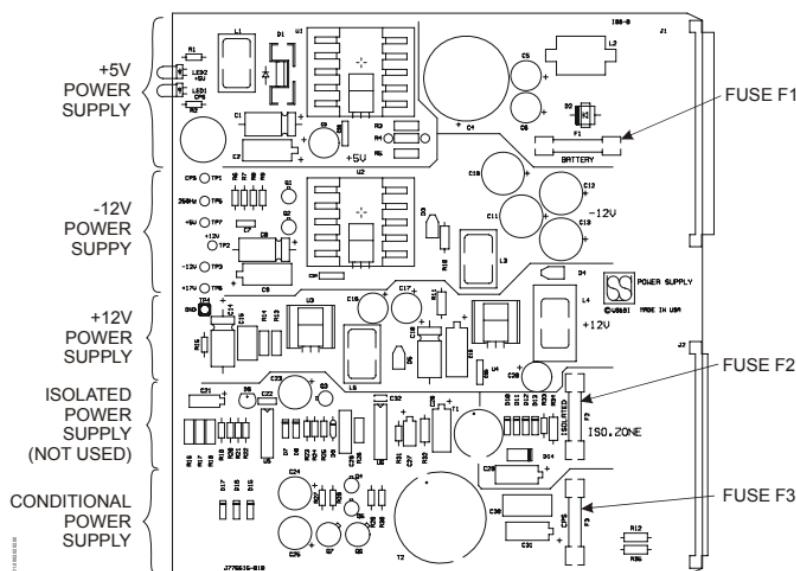


Figure 3-2.N16660301 PCB Layout

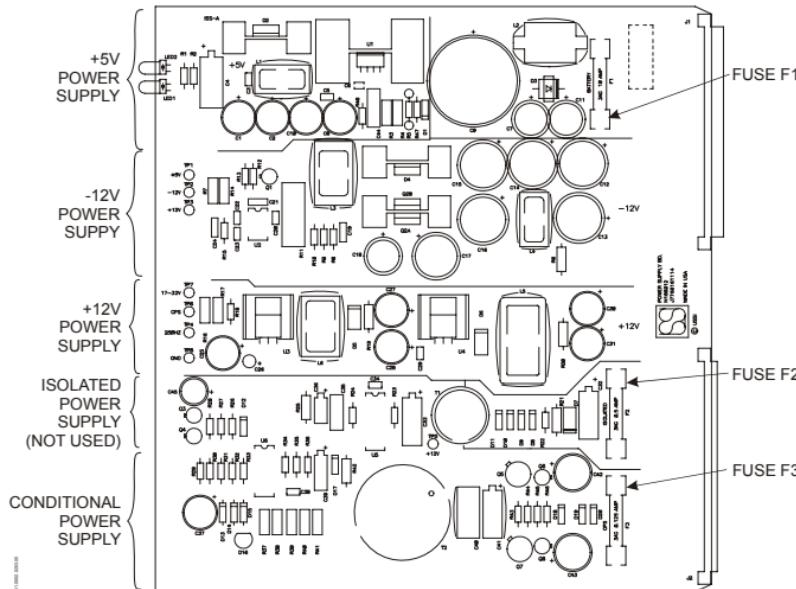


Figure 3-3.N16661203 PCB Layout

Table 3-3 lists the designation, part number, and rating of fuses used on the power supply PCBs. Refer to Figure 3-2 and Figure 3-3 for fuse location.

Table 3-3.Fuses on the Power Supply PCB

REF. FIGURE 3-2 AND FIGURE 3-3	CIRCUIT APPLICATION	ASTS USA PART NUMBER	DESCRIPTION
F1	System Battery	J710083*	7.5 amp, 32 volt
		J7100380027**	10 amp, 250 volt
F2	Isolated Output	J071190	1/2 amp, 250 volt
F3	Conditional Power Supply Circuit	J071075	1/8 amp, 250 volt

* Used on the N16660301 Power Supply PCB.

** Used on the N16661203 Power Supply PCB.

WARNING

When replacing a power supply PCB, make certain of the PCB type. An old model PCB (N16660301) can be replaced by a new model PCB (N16661203), but not a new with an old (due to current rating).

A power supply PCB cannot be replaced with a CPS only PCB.

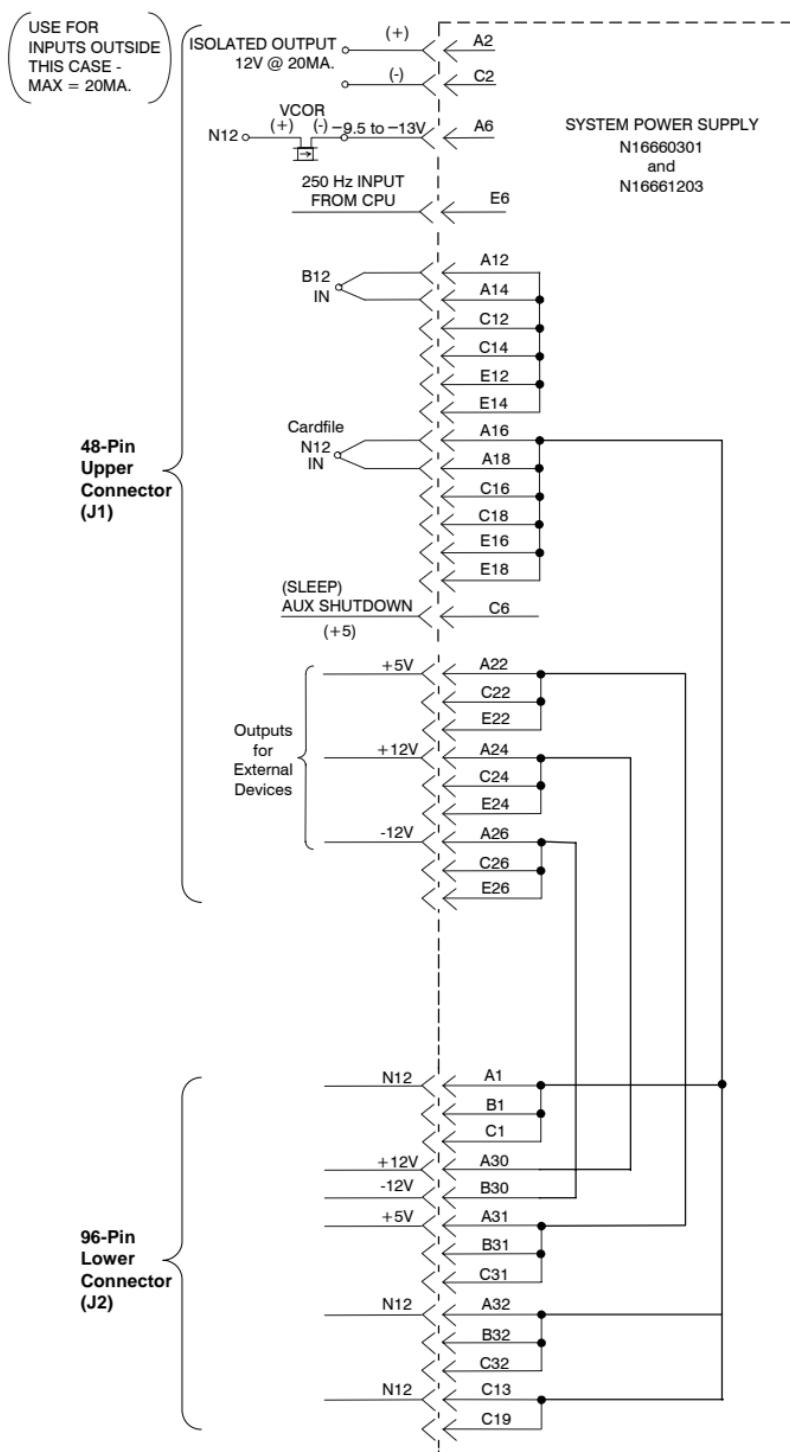


Figure 3-4.Power Supply PCB Pin-Out

NOTE

The purpose of a CPS only PCB is to drive a VCOR. It has no PCB lower connector and therefore no connection to the cardfile motherboard.

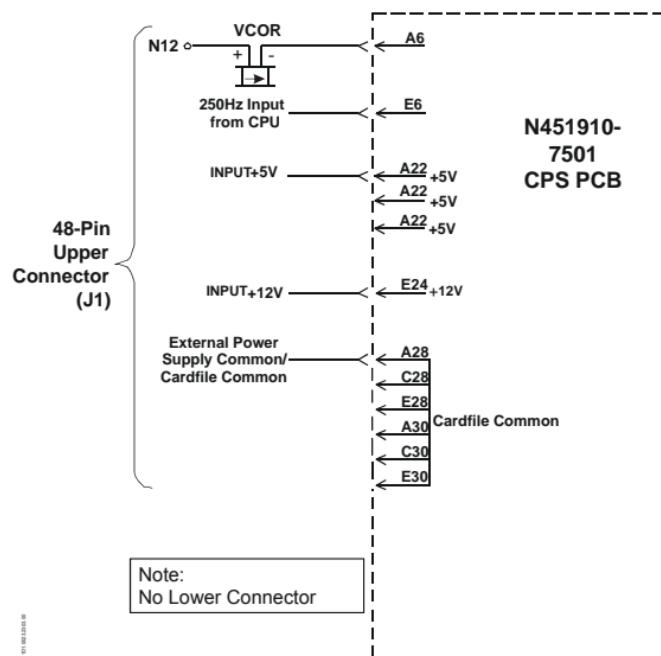


Figure 3-5.CPS Only PCB Pin-Out

NOTE

The VCOR voltage (nominal -9VDC), generated by the CPS, is negative with respect to N12.

Table 3-4.Fuse on the Conditional Power Supply PCB

DESIGNATION REF. FIGURE 3-6	CIRCUIT APPLICATION	ASTS USA PART NUMBER	DESCRIPTION
F1	System Battery	J071075	1/8 amp, 250 volt

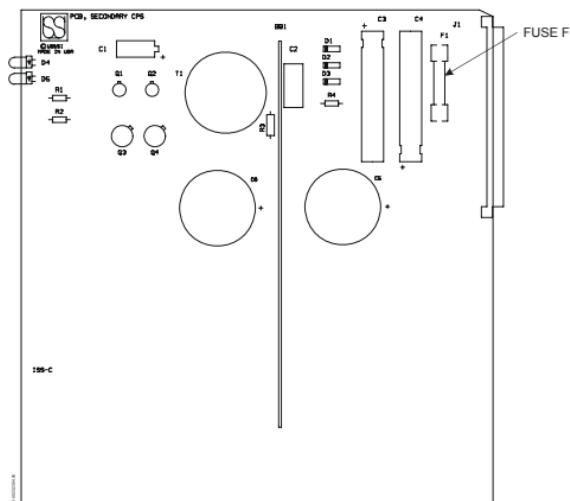


Figure 3-6.CPS PCB Fuse Location

3.1 VCOR

The Vital Cut-Off Relay (VCOR) is used by the MICROLOK II system to control power to all vital outputs (See Figure 3-7). System battery B12 passes through the VCOR contacts when the relay is energized (picked). This relay is energized by the conditional output from the CPS PCB in the system cardfile. The MICROLOK II CPU PCB controls this fail-safe function. A ASTS USA PN-150B vital biased relay serves as the VCOR. This relay incorporates a 400 ohm coil and low voltage silver-to-silver contacts.

Table 3-5.VCOR Contacts and Ratings

TYPE PART NUMBER	CONTACTS	CONTACT RATING	COIL RESIST. (OHMS)	PICKUP AMPS	PICKUP DC VOLTS	SYSTEM VOLTAGE
ASTS USA PN- 150HD N322505- 701	4FB	15 amps	400	0.0132	5.3	10
	2FB	4 amps				
ASTS USA PN- 150B N322500- 701 or N322500- 801 (no front test)	6FB	4 amps	400	0.0132	5.3	10

NOTE

To increase the output current capacity of the relay contacts the following relays can be used as repeaters of the VCOR:

- PN-150B (400 or 800 ohm coil)
- PN-150HD (400 or 800 ohm coil)
- PN-250B (250 ohm coil – 12 volt system)

CAUTION

At no time should the operation of an installed VCOR relay be checked by applying +12VDC to the 1C terminal of the coil. This will result in damage to the cardfile power supply.

To check relay operation, first remove it from the installation.

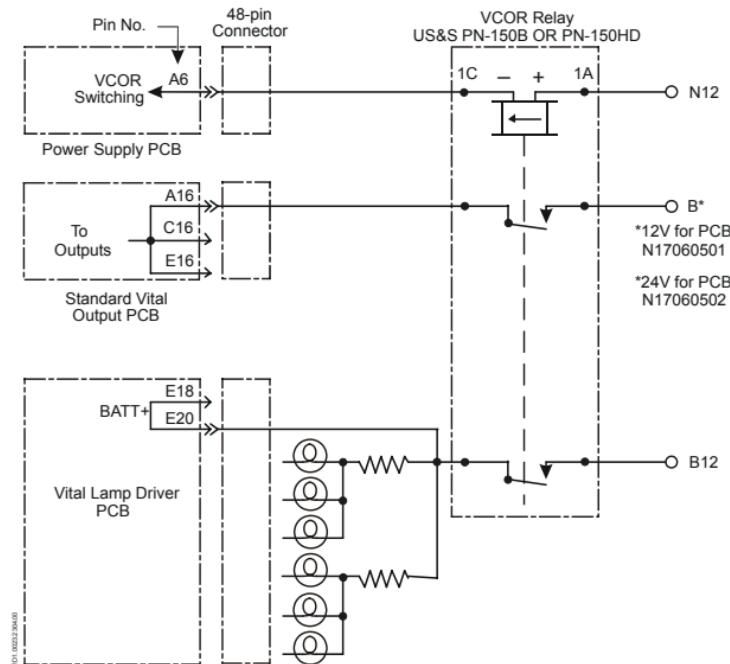


Figure 3-7.Typical VCOR Wiring with Power Supply PCB

(shown with incandescent signals – Example Only)

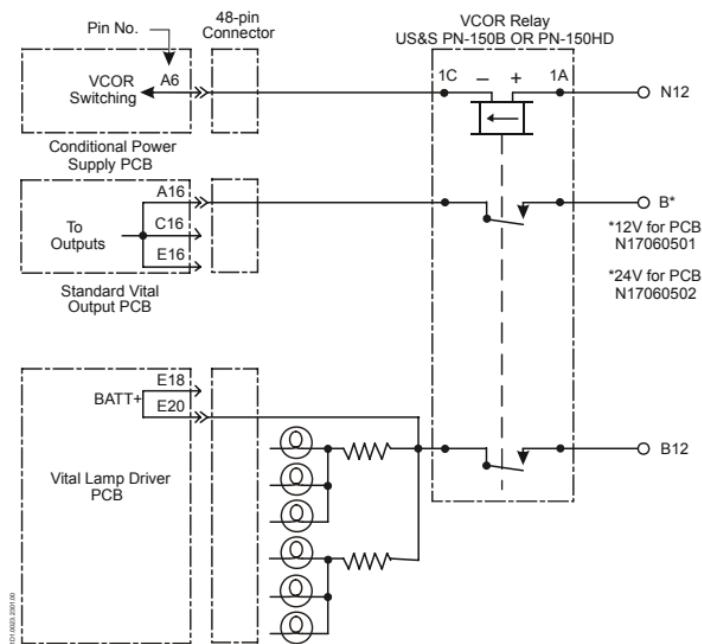


Figure 3-8.Typical VCOR Wiring with CPS PCB

(Example Only)



4 VITAL PCBS

4.1 Input (IN16) – Output (OUT16)

IN16 – Vital Isolated Inputs – N17061001
OUT16 – Vital Outputs – N17060501

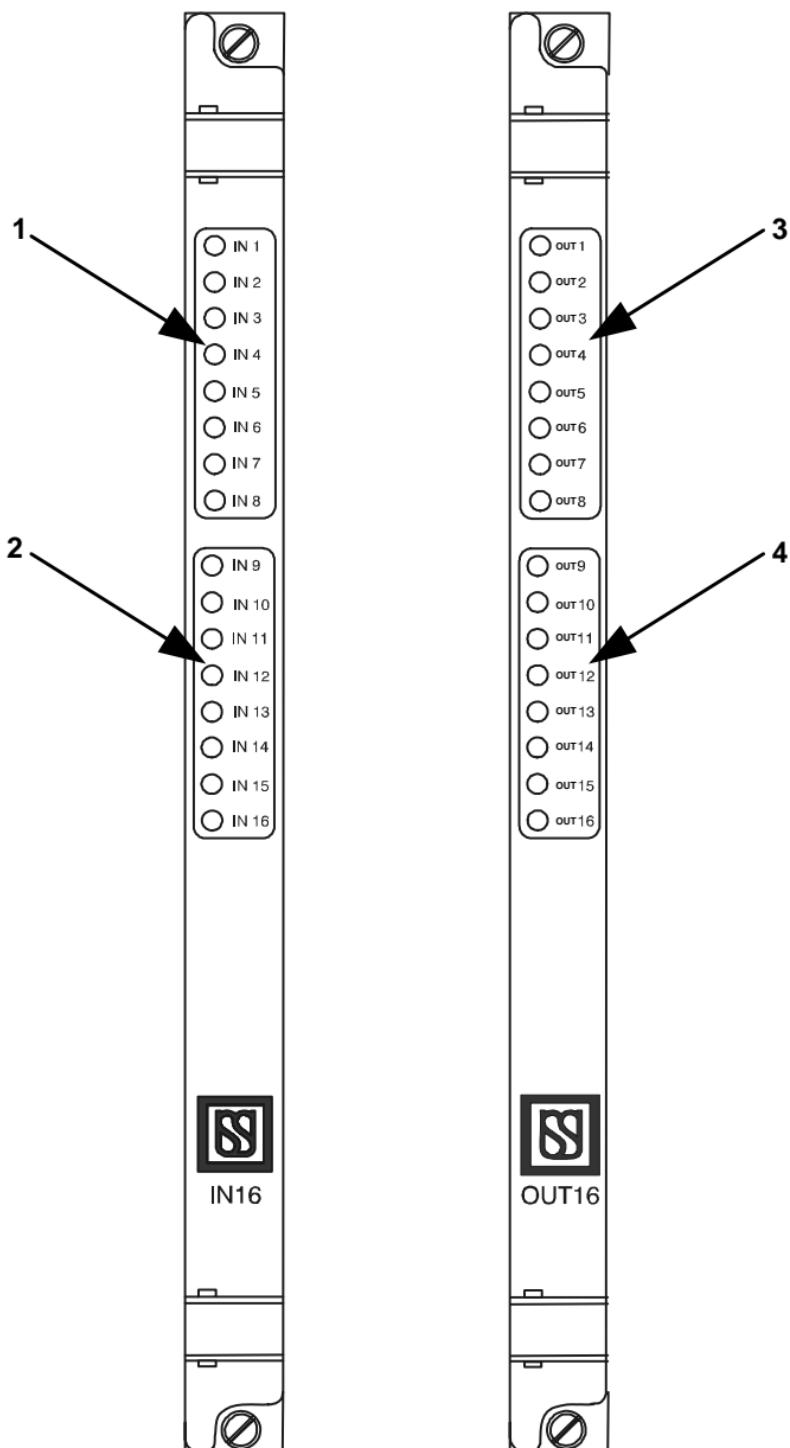
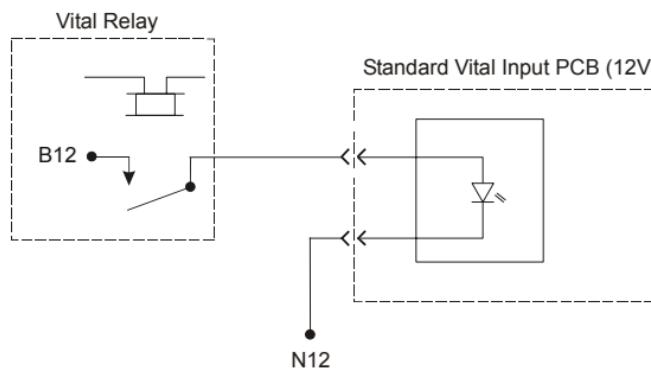


Figure 4-1.Vital IN16 and OUT16 Front Panel Detail

Table 4-1.IN16 Indicators

REF FIGURE 4-1	LABEL	DEVICE	PURPOSE
1	IN1 - IN8	Green LEDs	Monitor state of vital inputs 1 through 8. When lit, indicates respective input is turned on.
2	IN9 - IN16	Green LEDs	Monitor state of vital inputs 9 through 16. When lit, indicates respective input is turned on.


Figure 4-2.Typical Vital IN16 Input
(Example Only)
Table 4-2.OUT16 Indicators

REF FIGURE 4-1	LABEL	DEVICE	PURPOSE
3	OUT1 - OUT8	Yellow LEDs	Monitor state of vital outputs 1 through 8. When lit, indicates respective output is turned on.
4	OUT9 - OUT16	Yellow LEDs	Monitor state of vital outputs 9 through 16. When lit, indicates respective output is turned on.

4.2 Input PCB Top Connector Wiring Interface

Refer to Figure 4-3 for PCB pin-out information and Figure 2-2 for PCB top connector pin configuration.

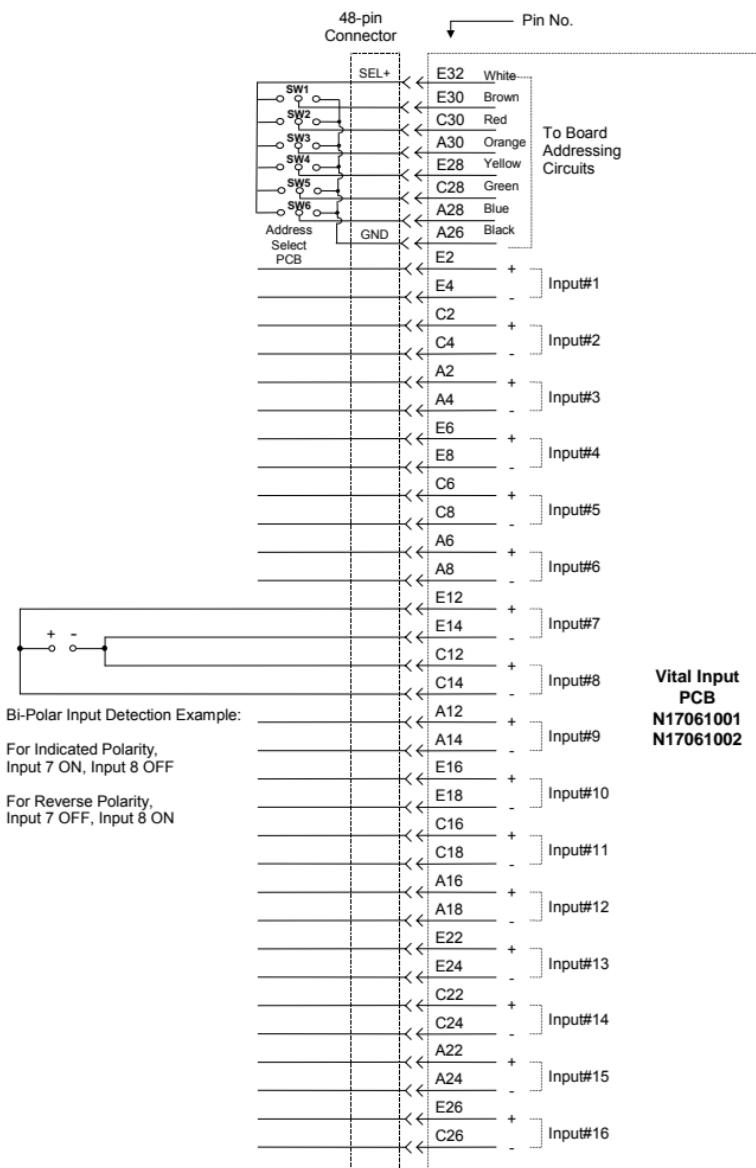


Figure 4-3.Vital Input IN16 PCB - Basic Interface Wiring
(Example Only)

4.3 Output PCB Top Connector Wiring Interface

Refer to Figure 4-5 for PCB pin-out information and Figure 2-2 for PCB top connector pin configuration.

NOTE

Pairs of LEDs will flash briefly in sequence (top to bottom) during operation as the PCB performs the output tests.

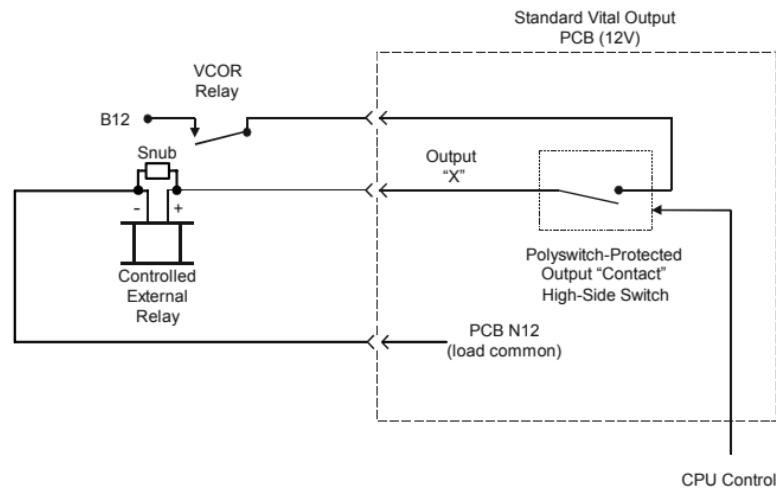
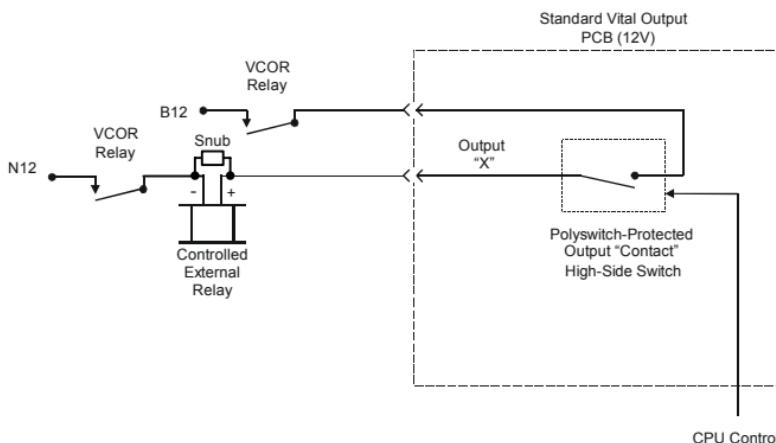


Figure 4-4.Typical Vital OUT16 Output

(Single Outputs Shown – Typical N12 Connections – Example Only)

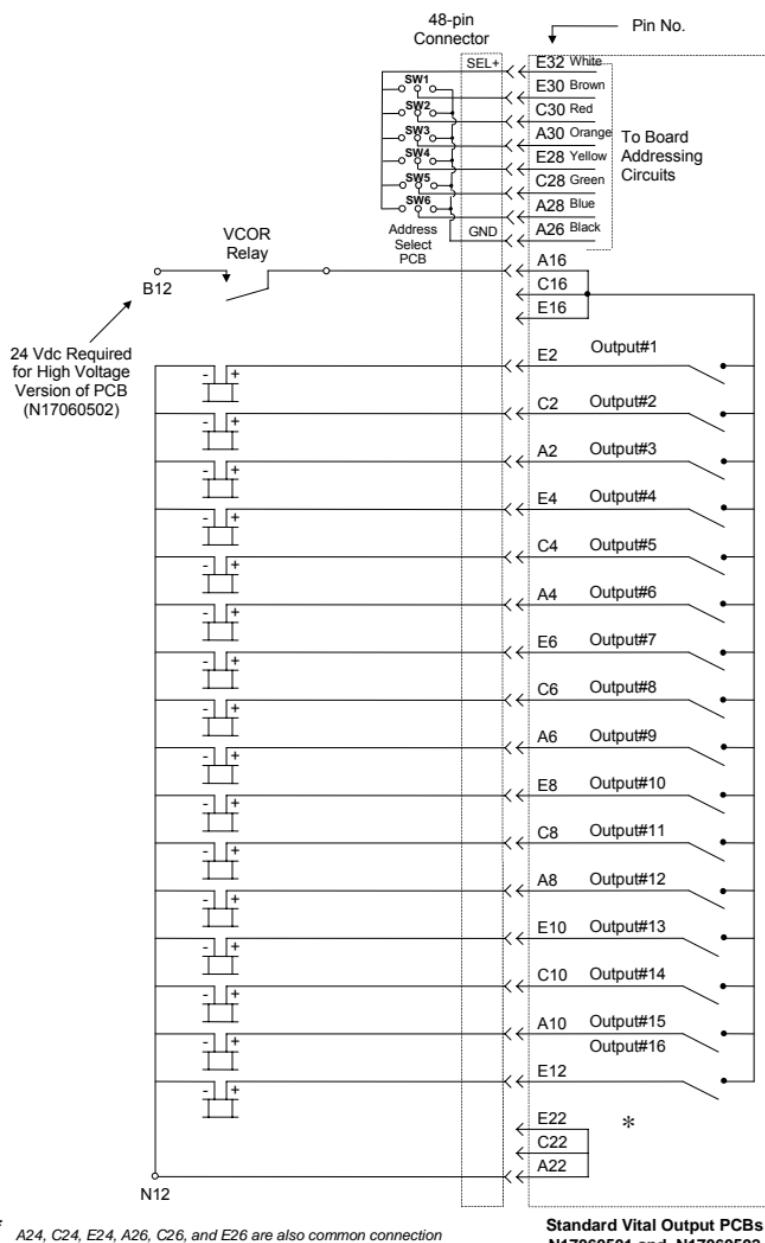


Figure 4-5.Vital Output OUT16 PCB - Basic Interface Wiring
(Example Only)

4.4 Vital Output Isolation

4.4.1 High Power Output Isolator

The MICROLOK II isolation module (See Figure 4-6) provides the equivalent of double-break circuit protection when the system is controlling vital relays or interfacing line circuits in a separate equipment house or case. This device can also be used to create a vital bipolar output from two single break standard outputs.

Three versions of the isolation module are provided:

- N17001101 12V output
- N17001102 50V output
- N17001103 24V output

Outputs are short-circuit protected and are designed to withstand a single short to B12 or N12 without damage. The outputs can also withstand 2000V rms to battery and earth ground. Output current is limited to 0.4A.

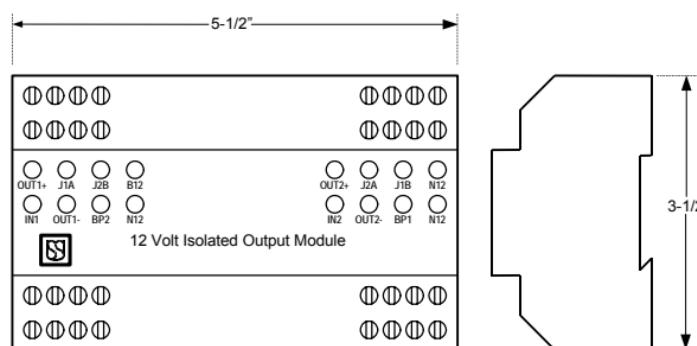


Figure 4-6.Vital Output Isolator Module

Table 4-3.Isolation Module Voltage Ratings

PART NUMBER	SYS BATT	ISOLATOR BATT	OUTPUT VOLTAGE
1101	12VDC	9.8 - 16.2VDC	10 - 18VDC
1102	12VDC	14 - 18VDC	40 - 55VDC
1103	12VDC	18 - 35VDC	18.2 - 36.8VDC

NOTE

Module 1102 assumes a 500 Ω or greater load.

Module 1103 assumes a 1000 Ω or greater load.

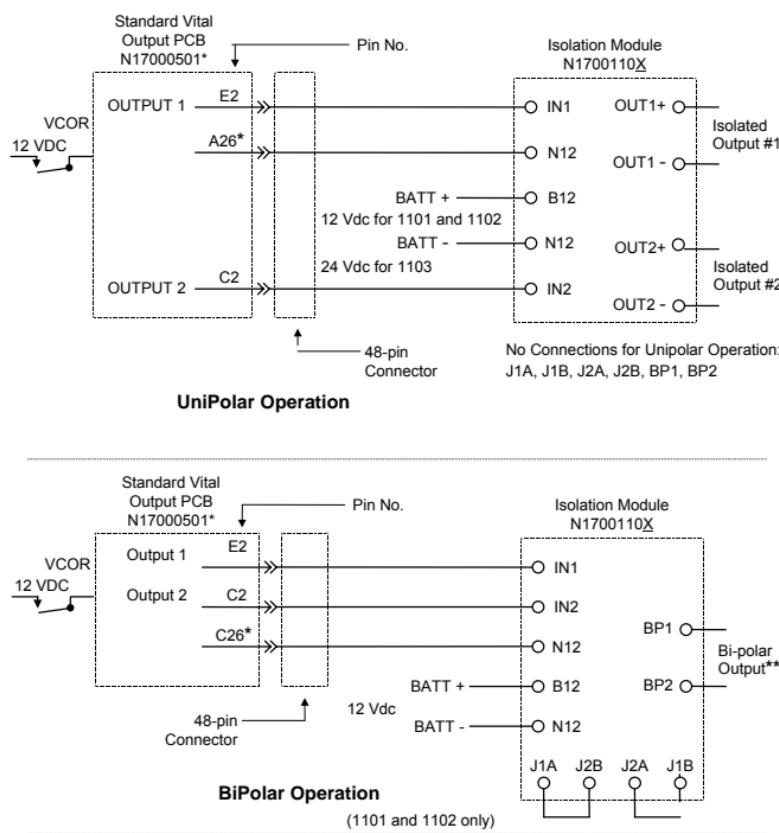


Figure 4-7.Typical Vital Output Isolator Wiring Interface

Isolation module terminals **B12** and **N12** designate battery positive and battery negative, respectively. For two independent outputs, with terminal **IN1** activated by a nominal +12 voltage relative to N12, output 1 is activated with the indicated polarity (**OUT1+** or **OUT1-**). Output 2 is similarly activated.

NOTE

For bipolar operation, both inputs should never be activated simultaneously.

4.4.2 Low Power Output Isolator

In low power applications the module shown in Figure 4-8 or the bipolar version shown in Figure 4-9 can be used.

INPUT VOLTAGE: 9.8 – 16.2 VDC

OUTPUT VOLTAGE:

N34800201 – 12V version: 10.0 – 17.5 VDC (400-ohm load)

N34800202 – 18V version: 14.0 – 24.0 VDC (1300-ohm load)

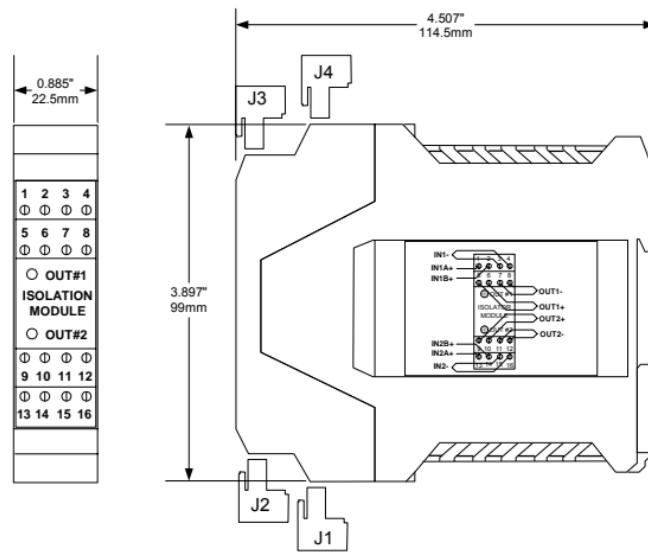


Figure 4-8.Low Power Vital Output Isolator

Yellow LEDs are visible through the front panel and are labeled "OUT #1" and "OUT #2." They are driven directly from the output stage of the isolator and they indicate that there is some voltage present at the output.

INPUT VOLTAGE: 9.8 – 16.2 VDC

OUTPUT VOLTAGE:

N34800301 – 12V version: 9.75 – 16.9 VDC (200-ohm load)

N34800302 – 18V version: 14.0 – 23.9 VDC (650-ohm load)

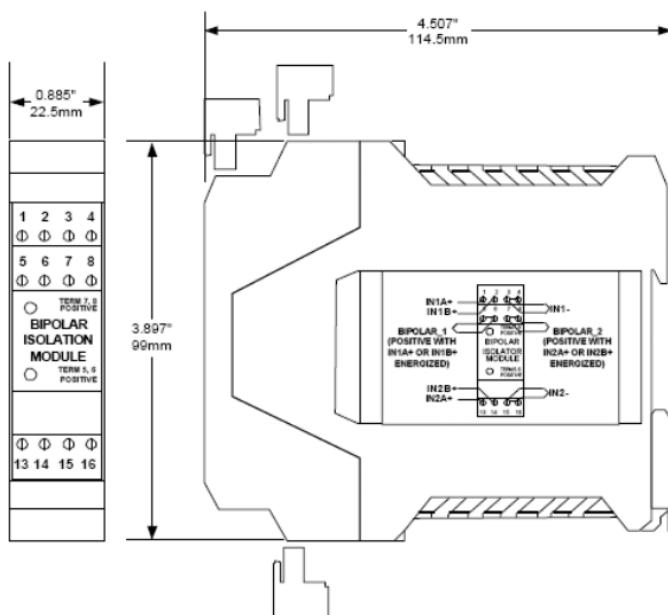


Figure 4-9.Low Power Bipolar Vital Output Isolator

Yellow LEDs are visible in the front panel and are labeled "OUT #1" and "OUT #2." They are driven directly from the output stage of the isolator and they indicate the polarity of the output.



4.5 Vital Isolated Output (OUT8.ISO)

OUT8.ISO – 8 Vital Isolated Outputs – N17065801 (12V)
N17065802 (24V)

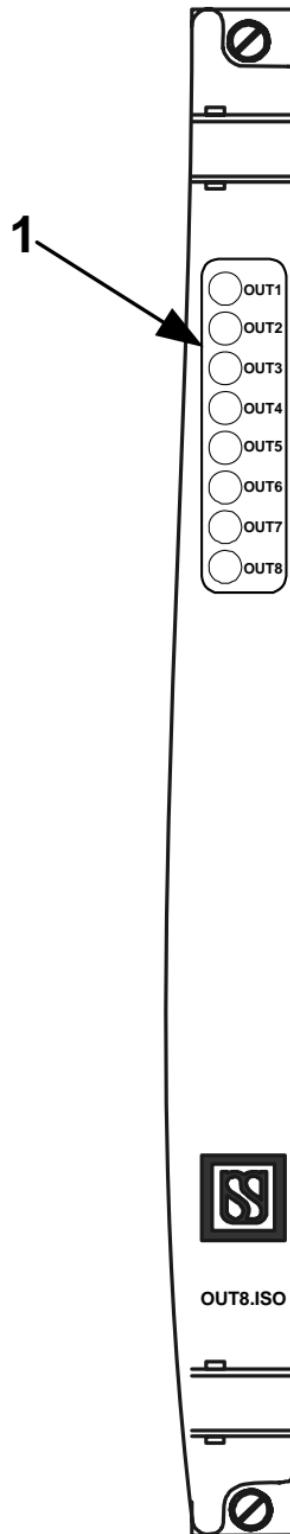


Figure 4-10. Out8.ISO PCB Front Panel

Controls eight normal and four bipolar vital isolated outputs (switch machine, relay coil, or bipolar drive for example).

The vital isolated output PCB provides eight vital isolated outputs for double break control of relays and bipolar relays. Each output provides a + and a – connection that is isolated from the house battery and other outputs.

The outputs are jumper selectable (JP1 – JP8) to drive normal vital relays or outputs can be combined to drive bipolar relays. Always verify that jumpers JP1 – JP8 are in the correct position before installation and applying power.

Output voltage is dependent on two factors, battery voltage and load resistance.

Table 4-4.OUT8.ISO Indicators

REF FIGURE 4-10	LABEL	DEVICE	PURPOSE
1	OUT1 - OUT8	Yellow LEDs	Monitor state of vital outputs 1 through 8. When lit, indicates respective output is turned on.

Table 4-5.OUT8.ISO Output Specifications

VITAL OUT8.ISO PRINTED CIRCUIT BOARDS				
OUTPUT SPECIFICATIONS				
ASTS USA PART NO.	VOLTAG E V _{BATT} RANGE	LOAD RESISTANCE RANGE	MAX. OFF VOLTAGE	MIN. ON VOLTAGE
N1706 5801	12V	50 Ω - ∞	0.75V	≈11.50V
N1706 5801	12V	400 Ω - ∞	0.75V	≈12.50V
N1706 5802	24V	100 Ω - ∞	1.5V	≈23V
N1706 5802	24V	800 Ω - ∞	1.5V	≈24V

NOTE

Pairs of LEDs will flash briefly in sequence (top to bottom) during operation as the board performs the output tests.

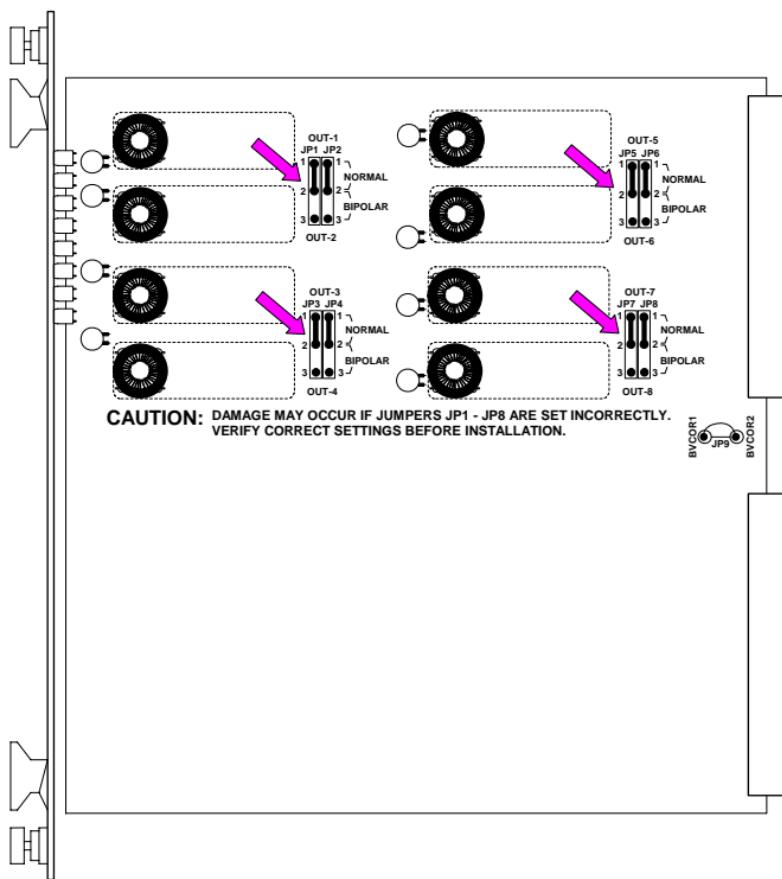


Figure 4-11.OUT8.ISO PCB Jumper Location

(For NORMAL or BIOPOLAR output selection)

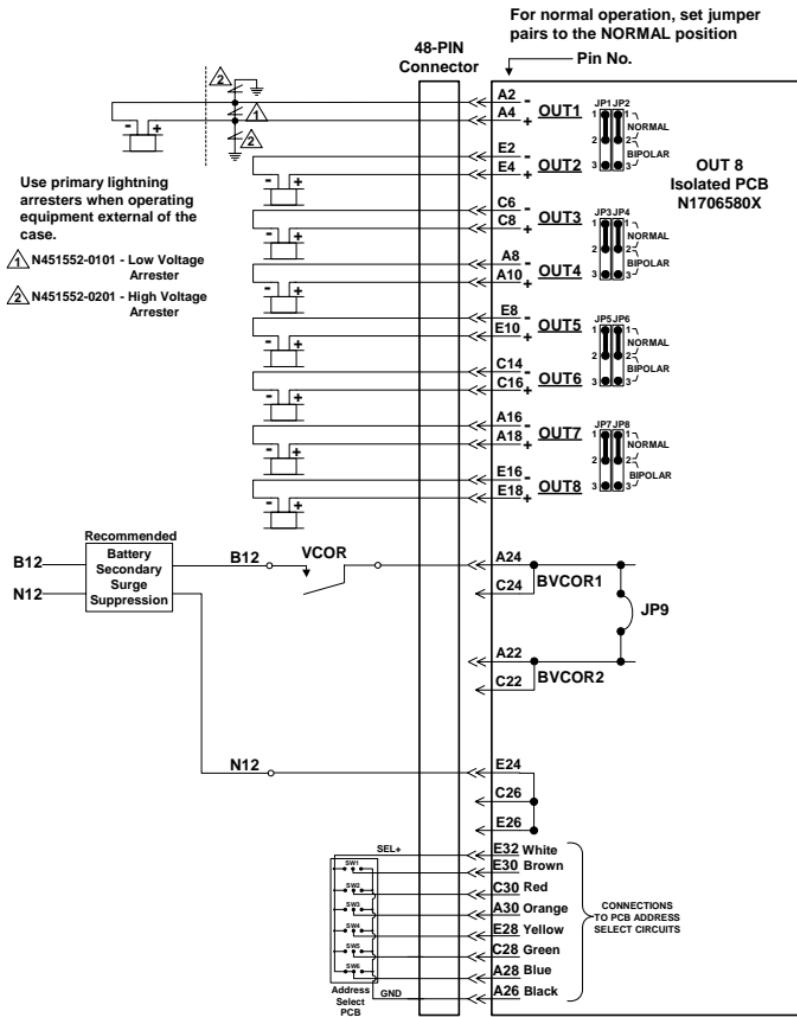


Figure 4-12.Basic Interface Wiring for NORMAL Operation

(BVCOR1 and BVCOR2 using the Same Battery)

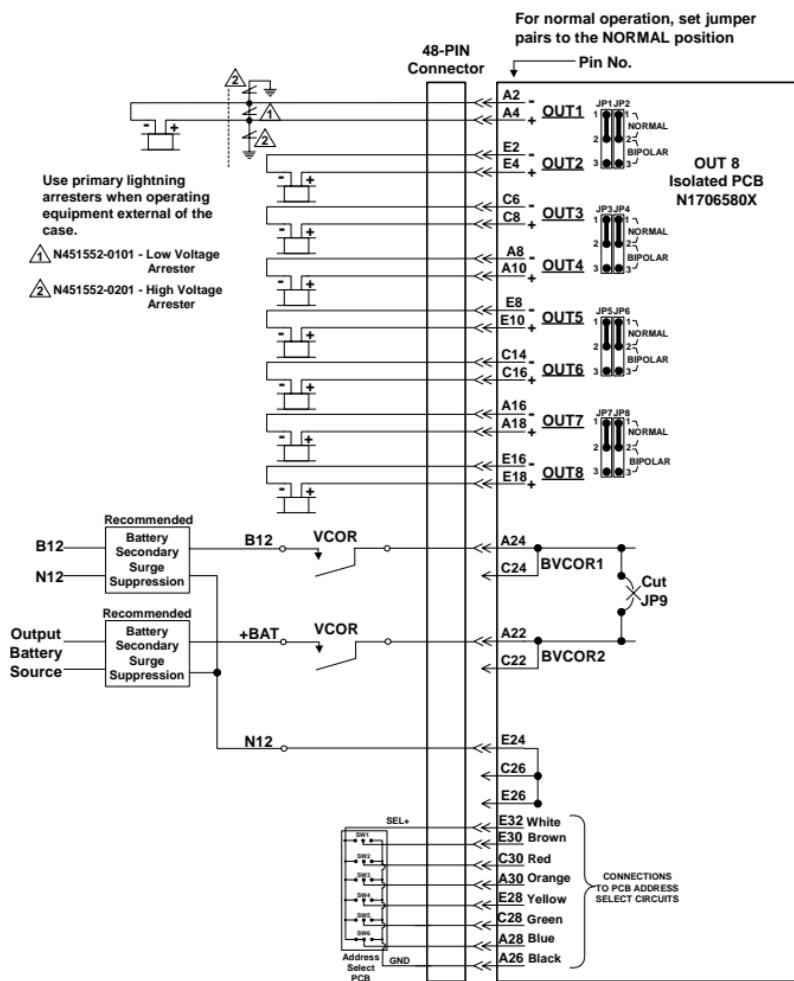


Figure 4-13.Basic Interface Wiring for NORMAL Operation

(BVCOR1 and BVCOR2 using Separate Batteries)

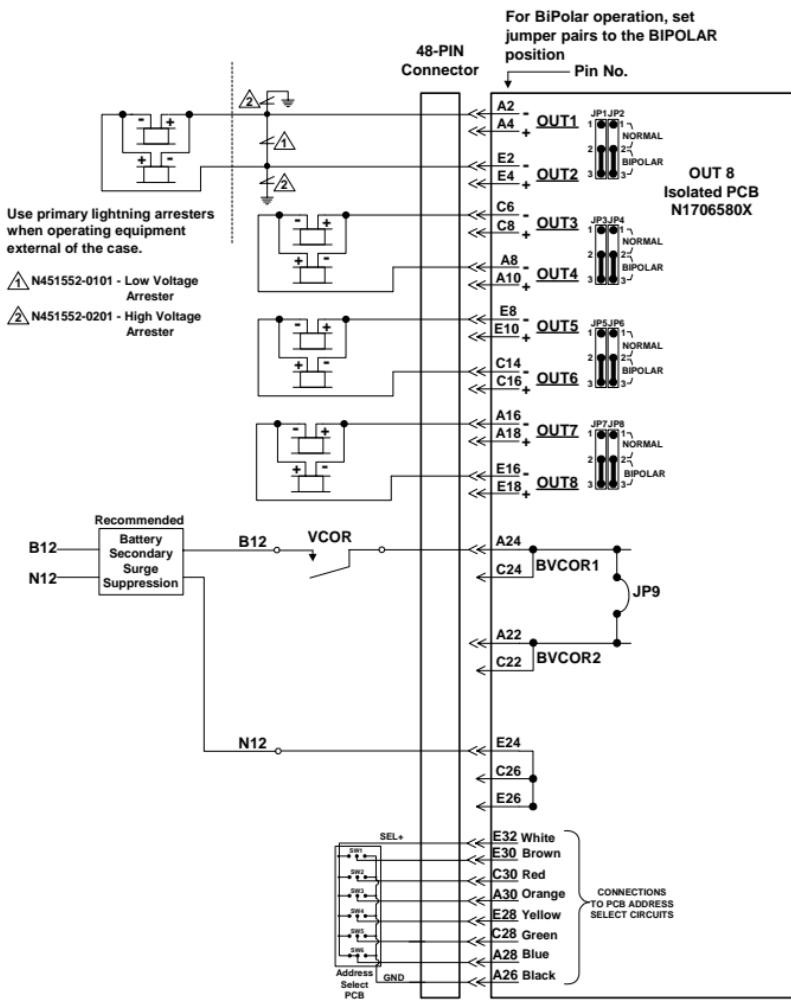


Figure 4-14.Basic Interface Wiring for BIPOLEAR Operation
(BVCOR1 and BVCOR2 using the Same Battery)

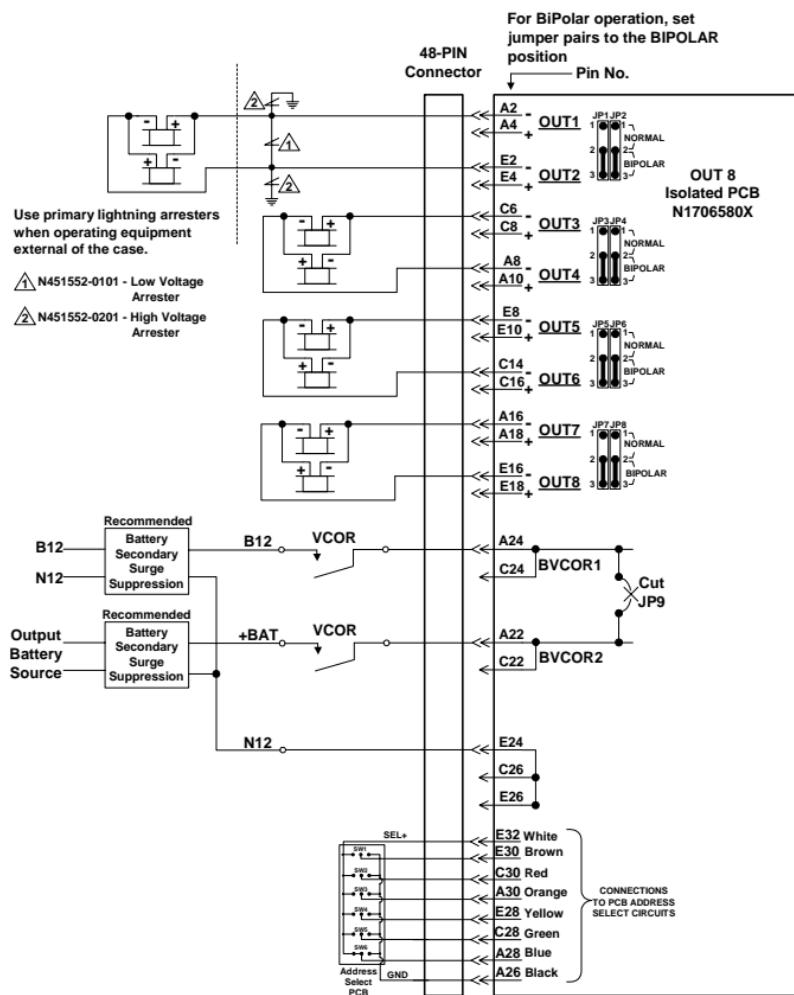


Figure 4-15.Basic Interface Wiring for BIPOLEAR Operation

(BVCOR1 and BVCOR2 using Separate Batteries)



4.6 Mixed Vital I/O (IN8.OUT8)

IN8.OUT8 – 8 Vital Isolated Inputs, 8 Vital Outputs – 17061601

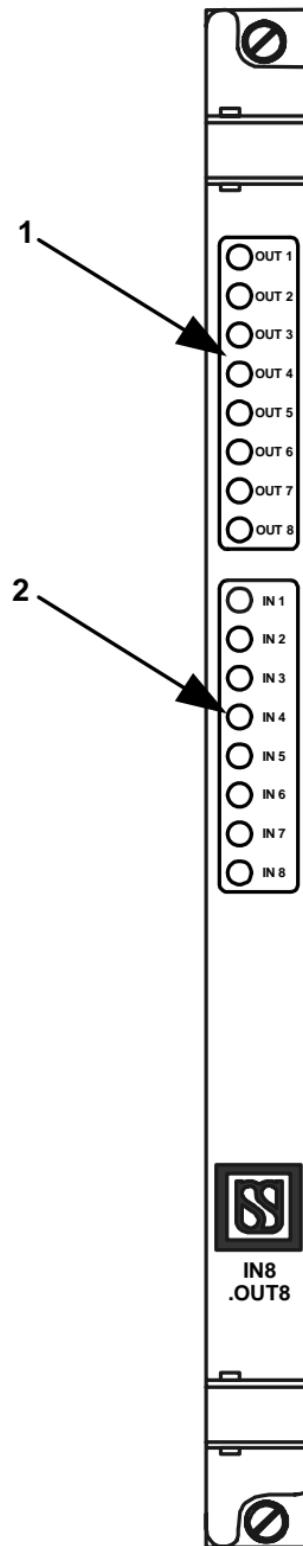


Figure 4-16.Vital IN8.OUT8 Front Panel Detail

The vital mixed IN8.OUT8 I/O board provides up to eight isolated inputs and eight non-isolated outputs. This PCB type is used in applications that do not require more than eight vital input or outputs.

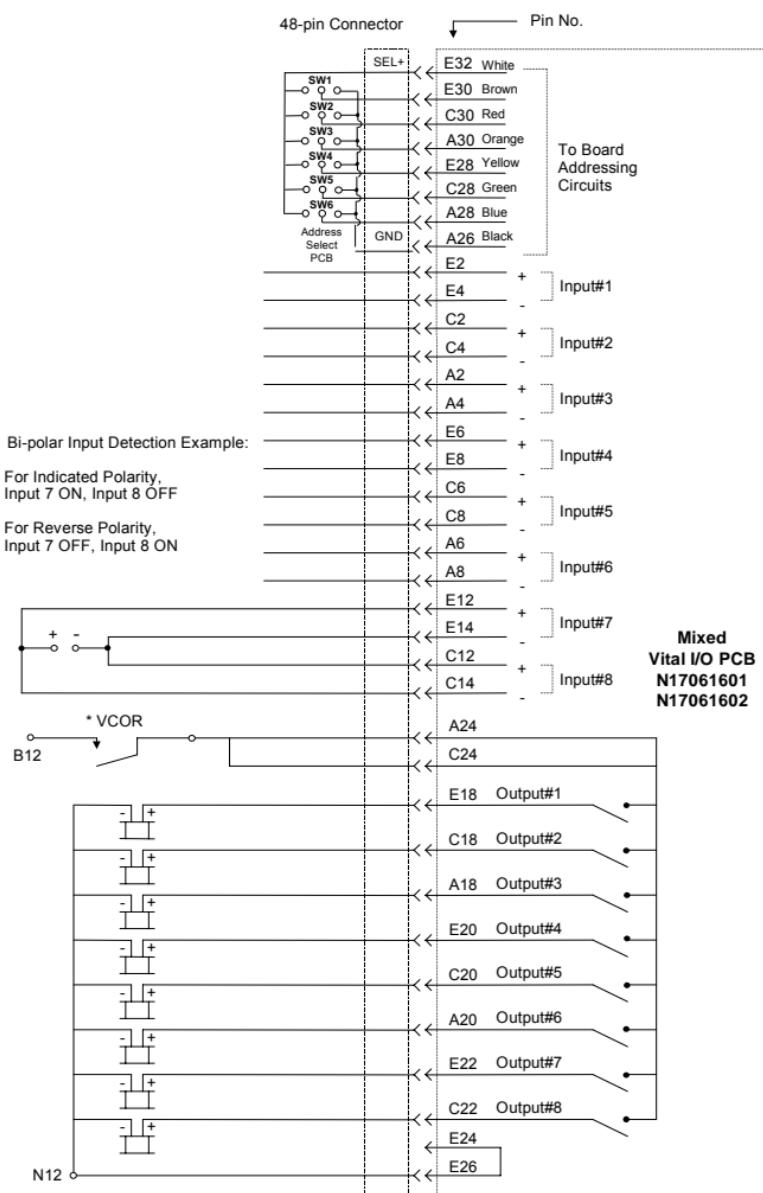
Table 4-6.IN8.OUT8 Indicators

REF FIGURE 4-16	LABEL	DEVICE	PURPOSE
1	OUT1 - OUT8	Yellow LEDs	Monitor state of vital outputs 1 through 8. When lit, indicates respective output is turned on.
2	IN1 - IN8	Green LEDs	Monitor state of vital inputs 1 through 8. When lit, indicates respective input is turned on.

4.6.1 PCB Top Connector Wiring Interface

Refer to Figure 4-17 for PCB pin-out information and Figure 2-2 for PCB top connector pin configuration.

Inputs can be wired in a bipolar configuration. Note that in Figure 4-17 example that input 7 is on and input 8 is off for the polarity indicated. For the reverse polarity, input 7 is off and input 8 is on.



* Note: Even if only inputs are used on this PCB, B12 must be connected to A24 and/or C24. This may or may not be through the VCOR.

Figure 4-17.Mixed Vital I/O PCB - Basic Interface Wiring
(Example Only)



4.7 Vital Lamp Driver (LAMP16)

LAMP16 – Vital Output – N17060101

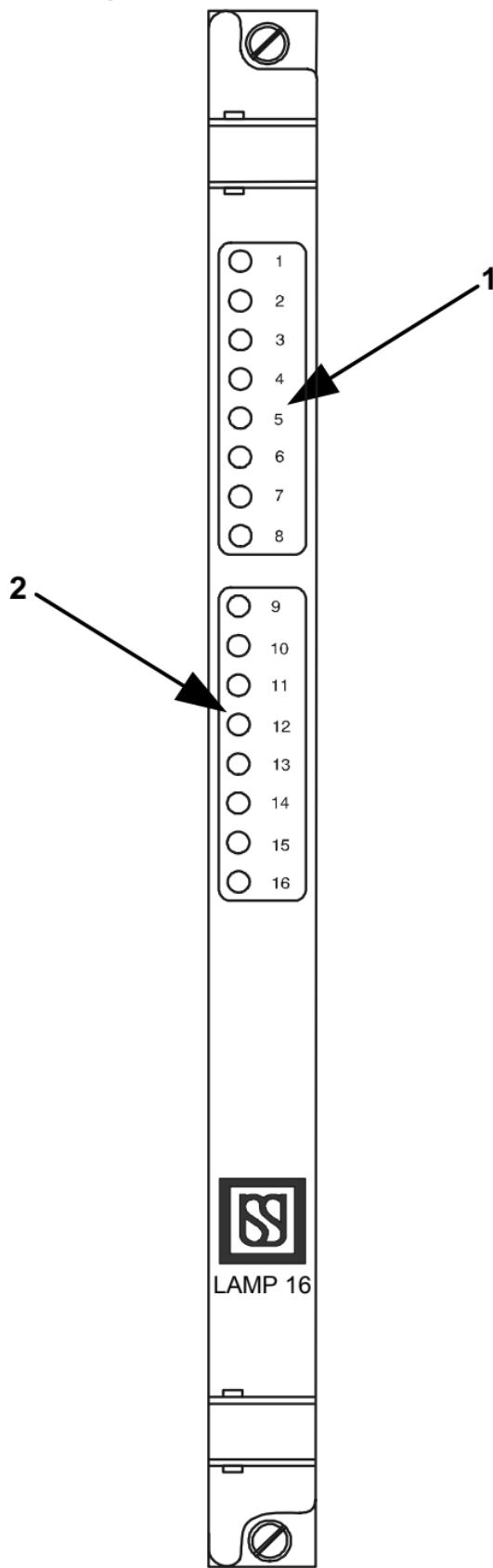


Figure 4-18.Vital LAMP16 Front Panel Detail

Table 4-7.LAMP16 Indicators

REF FIGURE 4-18	LABEL	DEVICE	PURPOSE
1	1 - 8	LEDs (Yellow)	Monitors vital lamp driver outputs 1 through 8. When lit, indicates respective lamp output is on.
2	9 - 16	LEDs (Yellow)	Monitors vital lamp driver outputs 9 through 16. When lit, indicates respective lamp output is on.

4.7.1 Lamp Out Condition

When a lamp load is determined to be in a "LAMP-OUT" condition the LED corresponding to that lamp will flash. The flash pattern is three short pulses followed by a one-second off interval. It is expected that this pattern is unique from any normal lamp flashing patterns.

4.7.2 PCB Top Connector Wiring Interface

Refer to Figure 4-19 for PCB pin-out information and Figure 2-2 for PCB top connector pin configuration.

Table 4-8.LAMP16 PCB Specifications

ASTS USA PART NO.	SIGNAL LAMP VOLTAGE RANGE	MAX. ACTIVATED LOAD	SIGNAL LAMP WATTAGE RANGE	MAX. NO. OF 18W LAMPS	MAX. NO. OF 25W LAMPS	MAX. NO. OF 36W LAMPS
N17060101	10V – 12V	300W	16W – 36W	16	12	8

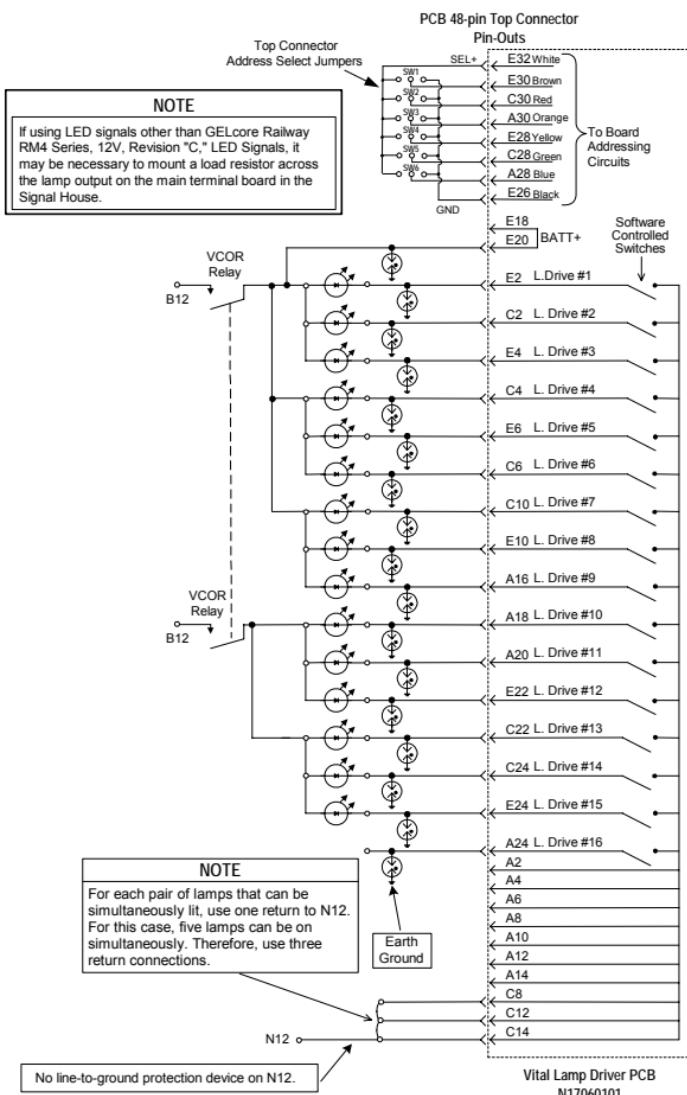


Figure 4-19.LAMP16 - LED Basic Interface Wiring

(Example Only)

NOTE

When driving LED signals always consult the specific location's Book of Plans for actual wiring information.

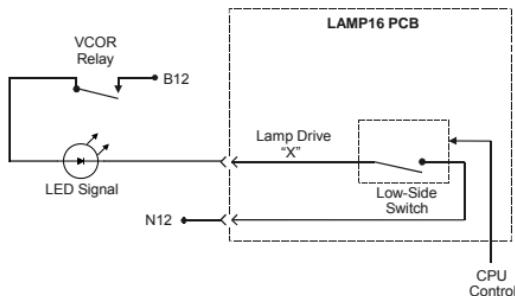


Figure 4-20.Vital LAMP Driver Output Block Diagram

(LED Signal Shown - Example Only)

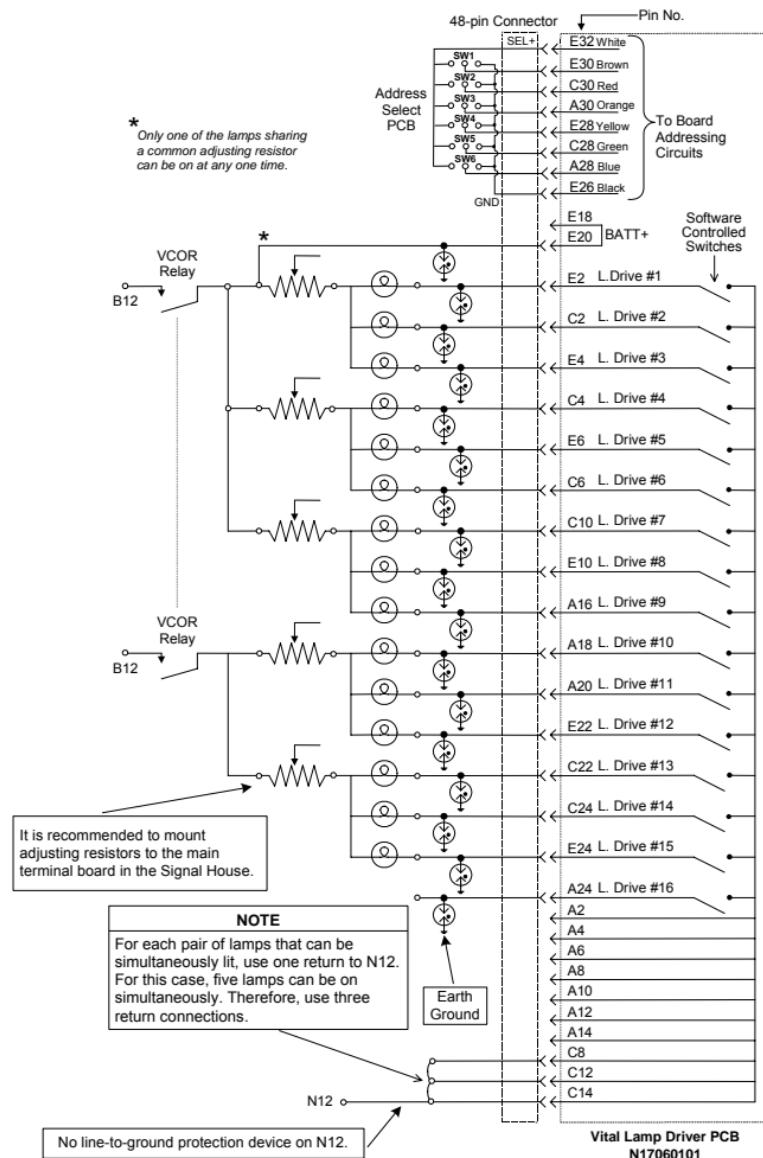


Figure 4-21.LAMP16 - Lamp Basic Interface Wiring
(Example Only)

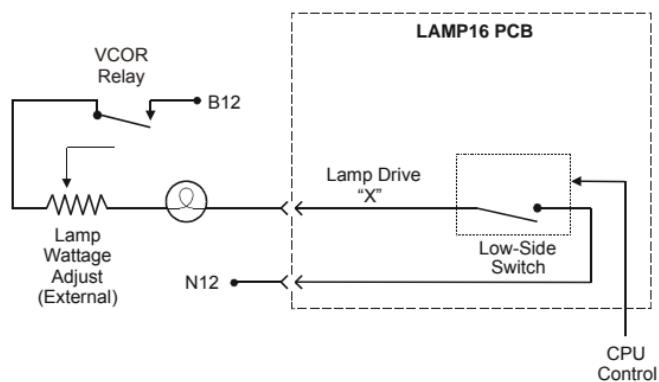


Figure 4-22.Vital LAMP Driver PCB Block Diagram
(Incandescent Lamp Shown – Example Only)

4.7.3 LAMP16 Configuration

The following key points must be considered when driving GELcore RM4 LED signals with the MICROLOK II LAMP16 board.

1. The MICROLOK II Executive Program from Rev. 8.0 includes the ability to drive only GELcore Railway RM4 Series, AREMA compliant, LED Signals (Refer to Table 4-9).
2. No other revision of the GELcore RM4 Signal, nor any other brand or model of LED signal is supported at this time.
3. The signals must be powered from a nominal 12VDC source. Typically, this will be the system's battery. Battery supply voltage and wire gauge must be selected to insure that a voltage greater than 7.5 volts is maintained at the terminals of the signals.

NOTE

A reliable method to accomplish this is by supplying two wires (a separate positive battery lead) to each signal head. If this is not possible then the total voltage drops on the signal leads must be calculated.

4. LED signals must be located no farther than 1500 feet from the LAMP16 board (3000 loop feet of wire).
5. Slide-wire resistors are not required and must not be used with GELcore LED signals.
6. MODE 1 operation will be the most reliable mode of operation.
7. In MODE 0, GELcore signals may operate better when designated as 13, 16, or 18-watt loads dependent upon battery voltage and the lead run from the LAMP16 board to the signal. For this reason, it is suggested that the application programmer designate ALL GELcore LED signals as ADJUSTABLE. This will allow the most appropriate wattage range to be selected at the track site. This is not a concern in MODE 1, as all loads (except 36-watt) are tested to the same current limits.
8. The GELcore Signals are designed to produce an open input state when a low light output condition is detected. The MICROLOK II, LAMP16 board will detect this LAMP-OUT state in both the ON and OFF state (i.e., both hot and cold filament checks are conducted).

NOTE

If the voltage drops below the 7.5 volt limit the MICROLOK II will detect the error and set a critical system error. The error will display as, "Good Lamp Flipped, Multiple Lamps Responded."

It is recommended that the application logic be designed to set the signal to the off state whenever a LAMP-OUT bit is set.

9. GELcore LED Signals may be flashed at rates up to 70 times per minute.
10. The MODE 0, 13-watt load setting may be used to drive an incandescent lamp if required. In MODE 0 a 13-watt load must draw at least 1.2 amp and no more than 1.9 amps when ON.
11. The "13 watt" load is verified and diagnosed in exactly the same manner as the "16, 18, 24 and 25 watt" loads.

Table 4-9.GELcore LED Signal Part Numbers

COLOR	GELCORE PART NUMBER
Red	RM4-RCFB-25B-92G RM4-RCFB-75B-92G
Yellow	RM4-YCFB-43B-92G RM4-YCFB-85B-92G
Green	RM4-GCFB-25B-92G RM4-GCFB-75B-92G
Luna (White)	RM4-WCFB-25B-92G RM4-WCFB-75B-92G

Note: GELcore is discontinuing the "Rev D" designation in favor of these "92" part numbers.

IMPORTANT

The GELcore RM4 signals will blow open an internal fuse if the battery supply voltage or current drawn by the load decreases to ~ 1 Amp. If this is due to a low battery condition, any on signal is in danger of being made inoperative. Therefore, it is important that the application program monitors the lampout bit. The lampout bit will be set when a low current to the signal is detected. This will occur at 1.2 Amps. At this current level the fuse should not blow. If the application program will then turn off the signal, the signal can be saved. Turning off a signal that has a failure and low current will do no harm since the fuse should properly blow.

4.8 Vital LED Driver PCB (LED12)

LED 12 – Vital Output – N17066101

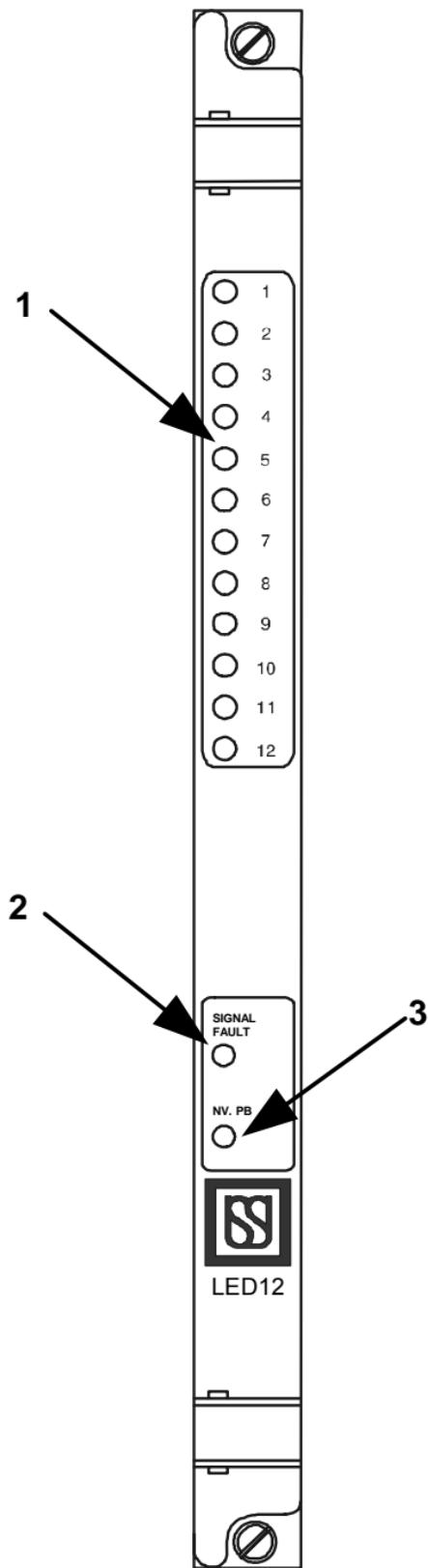


Figure 4-23.LED 12 PCB Front Panel Detail

The ASTS USA LED12 Signal Driver PCB (N17066101) provides twelve vital outputs for control of ASTS USA Color Light LED Signals. Outputs are controlled by "high-side" software-controlled switches, which connect and disconnect the output of the ASTS USA Constant Current Regulators for the LED signals. The LED12 PCB performs diagnostic and light-out detection functions without the use of external "check pulses."

Table 4-10.Vital LED12 PCB Indicators

REF FIGURE 4-23	LABEL	DEVICE	PURPOSE
1	LED1 - LED12	LEDs (Yellow)	Monitor state of vital outputs 1 through 12. When lit, indicates respective output is turned on.
2	Signal Fault	LED (Red)	Lit when diagnostics on any of the LED12 outputs detects a faulty signal.
3	NV.PB	Momentary Push Button	When pressed for three seconds, this non-vital pushbutton sets the state of the board's system bit to clear the fault state of all signals connected to the PCB.

NOTE

The LED12 PCB is designed to vitally drive only ASTS USA Color Light LED Signals. It is not compatible with driving incandescent signals or other LED signals (such as GELcore products).

The front panel non-vital LEDs are software driven to indicate the controlled state of the PCB outputs. A lamp out condition is indicated by an uneven flashing pattern of the output LED indicator (several quick On pulses followed by a longer Off period).

The PCB interfaces to the MICROLOK II cardfile via the PCB lower connector and the motherboard data bus. The PCB utilizes six address jumpers on the top rear connector for CPU addressing. Operating voltages for the interface portion of the PCB are provided by the motherboard.

Power for the PCB output circuitry is provided by an isolated on-board power supply. This supply also produces the reverse polarity voltage used for the Off State output test. Power to the supply is from the system VCOR contacts.

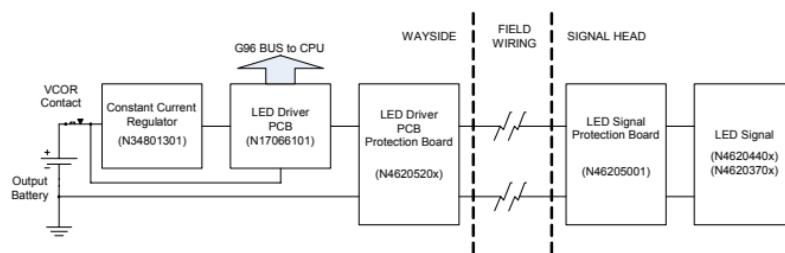


Figure 4-24. System Block Diagram (One Output Shown)

Refer to Figure 4-24 for a block diagram of one LED12 PCB output.

The ASTS USA LED Driver PCB Protection PCB (N46205201) is an entrance panel mounted PCB, that when used in combination with ASTS USA lightning arrestors, provides a high level of surge protection for the LED12 PCB from surges induced on the signal's field wiring connections. The PCB is designed to mount on standard AAR terminal spacing (See Figure 4-25).

The N46205201 version allows house wiring to be terminated on the left hand side of the entrance panel while the field wiring is terminated on the right hand side of the PCB. The N46205202 version of the LED driver protection PCB is reversed and allows for house wiring to be terminated on the right hand side of the PCB while field wiring is terminated on the left hand side of the PCB. Both versions of the PCB use the same components and allow the components to be viewed for inspection while preserving the necessary polarity markings and electrical connectivity for the resistors and Metal Oxide Varistor (MOV) devices relative to the house and field wiring.



**Figure 4-25. LED Driver PCB Protection PCB
(N46205201)**

The ASTS USA Constant Current Regulator Module (N34801301 - See Figure 4-26) provides a constant 350mA regulated current output for driving ASTS USA Color Light LED Signals. The output of the regulator includes both open and short circuit protection. A regulator (mounted on a DIN rail external to the system cardfile) is required for every energized ASTS USA LED Color Light Signal in a system; however a regulator can be shared between signals that will never be on at the same time. Power to the constant current regulator is supplied via a VCOR contact.

NOTE

It is recommended that if the regulators are installed side by side, a $\frac{1}{2}$ " space should be left between them to prevent heat build-up.



Figure 4-26.ASTS USA Constant Current Regulator Module N34801301

Characteristics of the ASTS USA Color Light Signal, which differ from typical existing signal applications are as follows:

- Due to the constant current drive, the electrical readings taken at the LED signal load will be different from typical signals. Where the load voltage of an ON-state incandescent signal is typically battery (i.e., 12V or lower due to line drop), the load voltage of a ON-state ASTS USA LED signal is typically around 35V.
- An ASTS USA Color Light LED Signal cannot be checked for operation (lit) by applying battery directly to its terminals. An ASTS USA Constant Regulator or equivalent current source is required to light the signal. Also, an ohmmeter across the terminals of the signal will not provide an indication of the signal's integrity.
- The ASTS USA Color Light LED Signal has five terminals (three which require a field connection, two have no external connection), which are clearly marked. Care needs to be taken to insure that the connections are made to the proper terminals.
- The ASTS USA Color Light LED Signal field terminals have a polarity that must be observed, where incandescent signals typically do not. A signal hooked up with reversed polarity will not operate and could eventually damage the signal.
- When used in combination with the ASTS USA LED12 Vital Output Board, an OFF-state ASTS USA Color Light LED Signal will have a load voltage of approximately -2.5V. This voltage is present due to

the OFF-state diagnostics that are being performed by the control system and is normal.

- The diagnostic and light-out detection functions of the ASTS USA LED12 Vital Output Board do not make use of external "check pulses". For both ON- and OFF-state ASTS USA Color Light LED Signals, a "check pulse" will never be seen at the load.
- Slide-wire resistors are not required for use with a ASTS USA Color Light LED Signals and should never be installed. Also, an ASTS USA Color Light LED signal cannot be dimmed by switching in a series resistance, as what can typically be done with an incandescent signal.
- The ASTS USA LED12 board will detect shorts between signals that cause an incorrect signal state. If the return leads (-) of any two or more signals are shorted together the system will not indicate an error, since this is a legal wiring option. If the controlled lead (+) of two or more signals are shorted together the system will not indicate an error if all of the signals are in the same state, all on or all off. If a wiring short causes an off-state signal to turn on then a critical error will occur and the MICROLOK II system will reset.

4.8.1 Lightning Protection

Each signal output includes a bi-directional TransZorb to protect the PCB against damage due to high voltage and current levels induced by lightning strikes or other sources. The TransZorb is the third level in the lightning protection scheme for this design. The primary (lightning arrestors) and secondary (N46205201) levels are separate modules that are located external to the Signal Driver PCB.

4.8.2 ASTS USA LED Troubleshooting

4.8.2.1 Typical System Measurements

This section provides a list of voltage and/or current measurement of a good system and of a faulty system. It will refer to measurements taken using a meter and using the MICROLOK II Development System.

4.8.2.2 Constant Current Source

Table 4-11 summarizes the expected measurements that can be taken from a functional ASTS USA Constant Current Regulator Module operating off of a 9.8 to 16.2V source. Any readings outside of the stated ranges are a possible indication of a faulty module.

Table 4-11.Valid ASTS USA Constant Current Regulator Readings

CONDITION	EXPECTED READING
Voltage at output with no load connected (pin4 reference to pin1)	$V = \sim 52V$
Voltage at output with resistive load connected (pin4 reference to pin1)	$V = 0.35 * R \pm 10\%$, where $R \leq 140\text{ohms}$
Voltage at output with a known good ASTS USA Color Light LED Signal connected (pin4 reference to pin1)	$29V \leq V \leq 50V$
Current output with valid load (pin4)	$I = 350mA \pm 10\%$

Table 4-12.Valid ASTS USA LED12 Vital Output Readings

CONDITION	EXPECTED READING
Output ON	$29V \leq V \leq 48V$ $I = 350mA \pm 10\%$
Output OFF	$V < 0V$ $-150mA \leq I < 0A$

4.8.2.3 LED Driver Protection Board

The expected voltage readings taken across the LED Driver Protection PCB signal terminals will be the same or slightly less (due to resistance in the wiring) than the readings taken at the LED12 Vital Output Board outputs, shown above in Table 4-12. Any readings outside of the stated ranges are a possible indication of a faulty system module.

4.8.2.4 ASTS USA LED Color Light

The expected voltage readings taken across the ASTS USA Color Light LED Signal field wiring terminals will be the same or slightly less (due to resistance in the wiring) than the readings taken at the LED12 Vital Output Board outputs, shown in Table 4-12. Any readings outside of the stated ranges are a possible indication of a faulty system module.

4.8.2.5 Replacing LED Protection Board

Inspect the components for signs of stress or damage. If present, replace the PCB with a spare and return the faulty PCB to ASTS USA for repair (or discard?). Figure 4-27 illustrates the proper orientation of the protection PCB on the back of the ASTS USA Color Light LED Signal.



**Figure 4-27.LED Signal Protection PCB
(N46205001)**

4.8.2.6 LED Fault Detection (Light-Out)

The ASTS USA LED Color Light System follows the AREMA Guidelines for LED signals. The system repeatedly monitors the status signals connected to the LED12 board. On-state signals are monitored for opens and short circuits between each signal's leads. Off-state signals are monitored for continuity of the leads to the signal ad short circuits between each signal's leads. Faulty on-or-off-state signals are detected in five seconds. Flashing signals can take up to ten seconds to detect since the system is separately monitoring the on-and-off states.

Once a signal has been determined to be faulty the MICROLOK II System will log a warning and the LED12 front panel LED corresponding to the faulty signal will begin flashing. This flashing pattern is several quick on pulses followed by a longer off period. This will help distinguish a faulty signal from a normally flashing signal. When diagnostics on any of the 12 LED12 outputs detects a faulty signal the red LED at the bottom of the front panel will also turn on. This LED will quickly draw the maintainer's attention to boards with faulty signals.

NOTE

An LED12 board SIGNAL.GOOD bit is set (1 State) when the attached signal is detected as good. A LAMP16 board's LIGHT.OUT bit is set (1 State) when the attached signal is detected to be faulty.

Light out protection actually has two FAULT modes:

- Mode 1 is associated with an open LED. Since the signal is a series device (all LEDs in series) any open LED will cause a fault that will flash the LED indicator on the front of the board. A warning will also be logged in the event log. Application software will automatically give a more restrictive (downgraded) signal. The fault is latched until the NV/PB on the front panel is pushed. The fault is

detected whether the LED signal is either "Off" or "On."

- Mode 2 is associated with a short. If the LED fails short then the voltage level will drop. An allowable level is set at >29VDC. The LED indicator on the front panel of the PCB will flash. One LED may not cause the voltage to drop below the fault threshold. A warning will be logged in the event log if the voltage level falls below allowable limit.

Regulator failure or any PCB associated failure will cause a critical error.

Replacing a faulty signal will be automatically detected and the fault condition cleared in five seconds except in the condition of a faulty "On" signal.

Following AREMA guidelines a signal that is detected as faulty in the on-state will continue to be considered faulty in the off-state. This will prevent an application from inadvertently flashing a signal when it downgrades a faulty on signal. To clear fault condition of a signal detected as faulty while in the on-state, the output either has to be turned on or the application logic must set and then clear the .Retest.LEDs board application bit. This is typically done by mapping the "Non-Vital" pushbutton on the front of the LED12 board to the retest bit.

Adding the following line to the LOGIC section of an application program will do this mapping:

```
ASSIGN LED12boardname.NV.PB to  
LED12boardname.Retest.LEDs;
```

The NV.PB signal is held set for ten seconds after the front panel pushbutton is pressed for three seconds. The application logic must become stable within the ten second window of time for the output to be delivered to the .Retest.LEDs bit.

With this line in the application the maintainer must press the "Non-Vital" front panel pushbutton for three seconds. Once recognized as being actuated the MICROLOK II will set the status of all signals connected to that LED12 to be "good" and begin retesting. Five seconds later all signals will be updated to their current status, good or faulty. When the "Non-Vital" front panel pushbutton is pressed an event will be logged. If the button is stuck depressed for greater than one minute a warning will be issued. The MICROLOK II must detect the button to have been released before it will respond to a second pushing. This prevents a stuck "Non-Vital" pushbutton from continuously clearing the signal's status.

After a faulty signal has been replaced and recognized by the MICROLOK II, an event will be logged and the .SIGNAL.GOOD bit for the signal will be set (1). If all signals connected to a LED12 board are good the front panel red LED will be off.

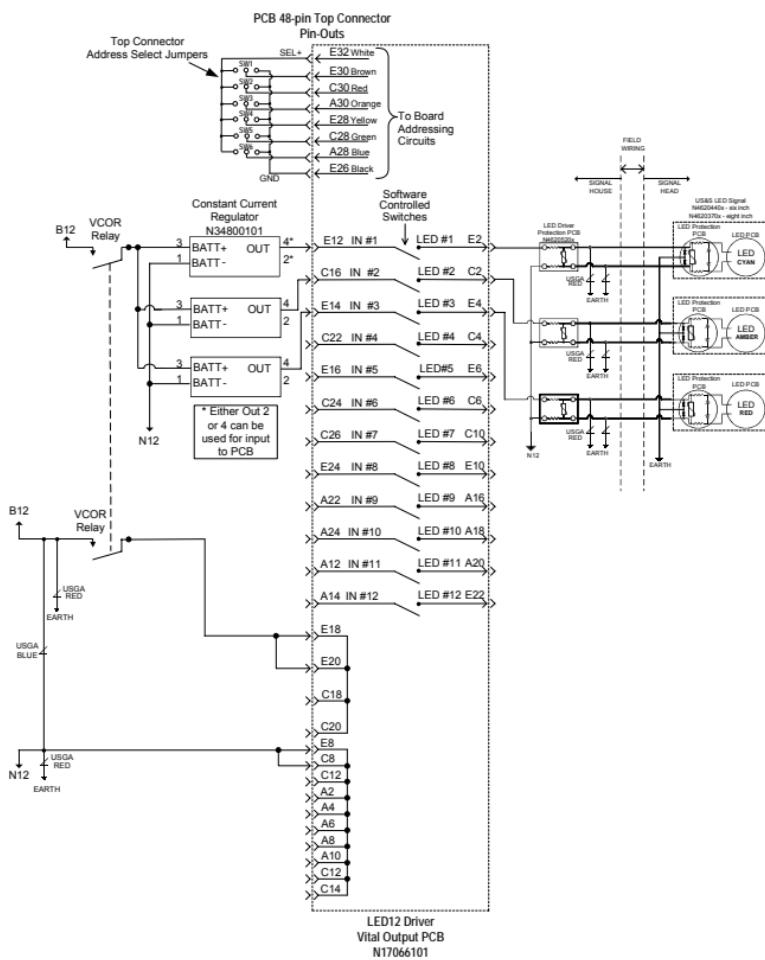


Figure 4-28.Vital LED12 Driver PCB Typical Interface Wiring

4.8.3 Troubleshooting Notes

4.8.3.1 Field Testing Open Signal Detection

When field testing a system for the detection of open signals special attention should be made to how the open wiring condition is created. If the maintainer attempts to open a circuit by removing a ring terminal from a tall AAR stud, many makes and breaks will usually occur. This can cause the MICROLOK II system to log "Shift Test" Events and possibly a "Shift Test" Critical Error. This occurs because the signal's output is unstable during the LED12 Board circuit diagnostics. The maintainer can choose to ignore the logged events or break the circuit in a quicker manner.

4.8.3.2 Field Wiring

ASTS USA recommends the following wiring specific requirements/notes for the ASTS USA LED Color Light Signaling System:

- For all applications, the use of the lightning/surge protection components of the LED Color Light signaling system is required.
- ASTS USA recommends the use of twisted pair wiring (two to three turns per foot) to minimize possible noise. This should be done wherever possible on all I/O wiring.
- ASTS USA recommends the physical separation of clean and dirty wiring. Ideally, all outputs are gathered in a bundle, inputs are gathered in a bundle, and power wiring is gathered in a bundle. Each of these bundles is physically separated from each other and all bundles are physically separated from other house wiring. It is particularly important to maintain this physical separation from high-current, "dirty" wiring.
- The ASTS USA Common Mode Filter (N451552-1001) is recommended for use on the battery lines to the MICROLOK and all battery-powered LED signaling system components (including battery broken-by-relay contacts). This filter needs to be located as close as possible to the equipment to maximize its effectiveness. Note that on MICROLOK II systems that include LAMP16 PCBs in addition to LED12 PCBs, power to the LAMP16 PCB and incandescent aspects must NOT be filtered. Using the filter in this instance can cause check-pulse problems.
- Users must not connect additional loads, such as local indicators, across the signal leads of the LED Color Light Signal.
- Multiple signals cannot be wired in series or parallel. (i.e., color position lights must be separately wired to individual constant current sources.)
- The outputs of multiple constant current sources should not be connected in parallel or series.
- Fuses are not needed/recommended on the signal outputs; the ASTS USA constant current regulator output includes short-circuit protection, and no damage will occur to the system if an output is inadvertently shorted to ground. Fuses can be installed on the system battery connections to the system as required.
- All field wiring should be configured to minimize crosstalk between wires. Cables and wires should be kept as short as possible to minimize induced line noise. Case/house wiring layouts should also be arranged to minimize noise. Battery leads should be as short as possible and must be isolated as much as possible from noisy wiring.

4.8.4 OS Track Circuit PCB

OS Track Circuit – N451810-6701

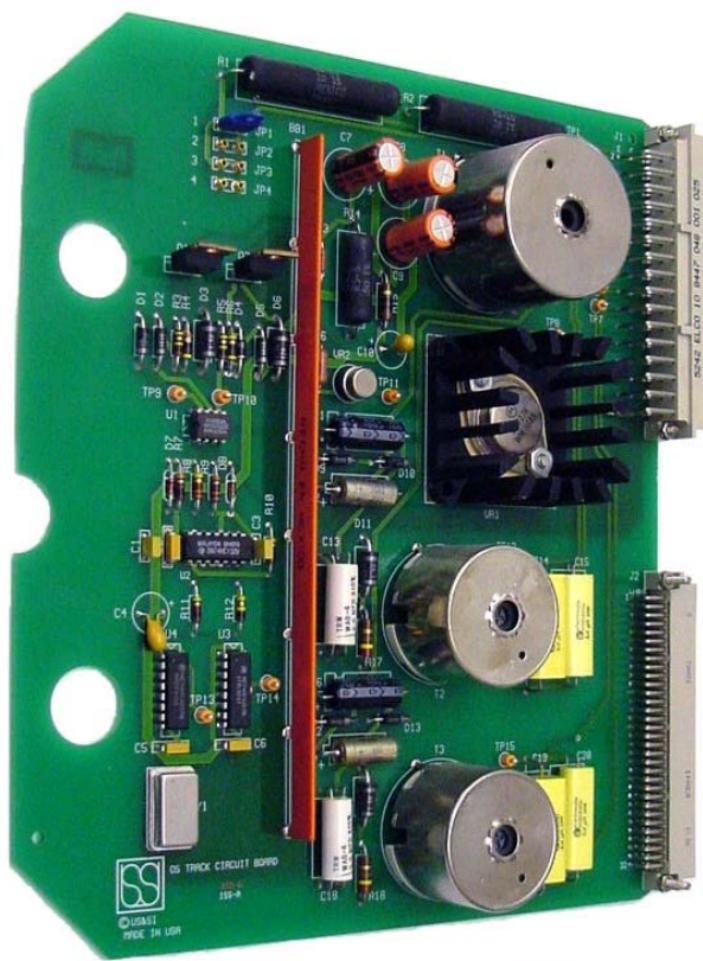


Figure 4-29.OS Track Circuit PCB Detail

The On Switch (OS) track circuit PCB interfaces the MICROLOK II system to the OS track circuit in interlocking applications requiring one OS transmitter and two OS receivers (end-of-siding).

An OS track circuit is used to indicate the track occupancy status of both the crossover track and the short section of mainline track near the switch. The detection of the presence of a train in either of these areas is used to prohibit activation of the switch machine. Also in MICROTRAX cab applications, train detection in the OS area may be used to transfer the location of the cab amplifier feed point.

The PCB has no front panel so only the PCB edge is seen from the front of the cardfile if it is not covered by a blank panel. The PCB has no connection to the cardfile data bus. The lower connector is provided only for physical support of the PCB.

Specifications for this PCB are listed in Table 4-13.

Table 4-13.OS Track Circuit PCB Specifications

TRANSMITTER/ RECEIVER FREQUENCY	RECEIVER OUTPUT VOLTAGE	TRACK CIRCUIT LENGTH	TRACK LEAD RESISTANCE
400Hz	12VDC to 20VDC 15VDC (nominal)	1000 ft. @ 5Ω/1000 ft. Ballast	0.5Ω (max).

It is not necessary to connect both receivers if it is not required by the application. In many cases the transmitter is connected at the heel block and the two receivers provide independent train detection on the interlocking through and turnout tracks.

NOTE

Transmitter output power is insufficient to drive a relay.

Figure 4-30 shows the basic wiring of the OS track circuit PCB. Outputs OUT1 and OUT2 must be wired to one of the inputs on the vital input PCB to provide the train detection input to the CPU PCB. OUT1 and OUT2 should each be wired to a "+" input on the vital input PCB, with N12 connected to each negative input.

Separate B12/N12 and +5V connections are also required to power the OS track circuit PCB transmitters and PCB circuitry. Also, note the installation of primary surge protection on the wiring.

CAUTION

Lightning arresters (shown in Figure 4-30) must be used in all MICROLOK II OS track installations, otherwise the system could be damaged from lightning surges or operate improperly as the result of transient signals.

Refer to Section 4.8.4.1 for procedures to adjust the OS track circuit PCB power output for various track circuit lengths.

CAUTION

The OS track circuit provides a transmitter and two receivers at an "end of siding" type location; this puts either a transmitter or receiver at each end of the OS circuit. All OS track circuits operate at the same frequency. If multiple OS circuits are used at a double-crossover type location, a defective joint potentially could cause a falsely energized track output.

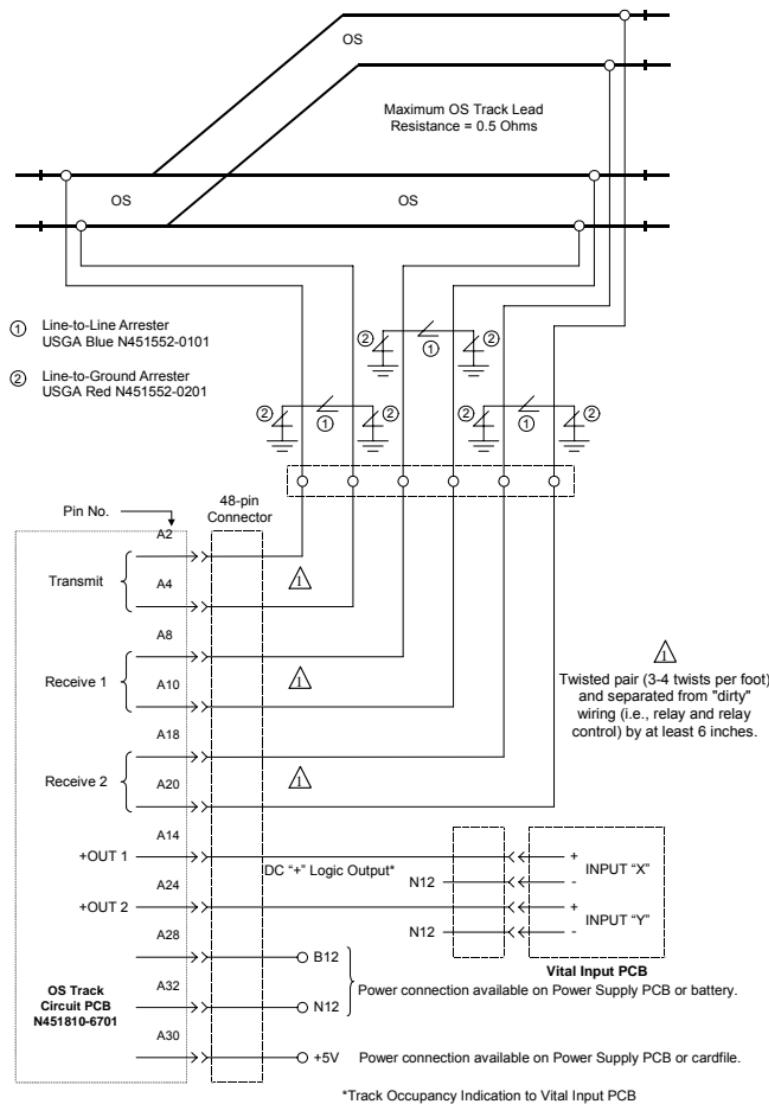


Figure 4-30.OS Track Circuit PCB - Basic Interface Wiring

4.8.4.1 OS Track Circuit Voltage Adjustment

Four jumper locations are provided on the OS track circuit PCB that are used to set the OS track shunting voltage (See Figure 4-31). JP1 represents the lowest power setting and JP4 the highest. The jumper is factory installed in the JP1 position.

To make this adjustment:

1. Connect a voltmeter across each of the outputs of the OS track circuit PCB at the inputs to the vital input PCB (See Figure 4-30). Consult the system installation drawings for test point locations.
2. Note the reading on each voltmeter. Each meter should indicate at least 12.0VDC at the vital input. If this is the case, the test is complete. Proceed to Step 5. If either voltmeter indicates less than 12.0VDC, proceed as follows:
 - a. Remove battery power from the MICROLOK II cardfile.
 - b. Loosen the retaining screws that secure the OS track circuit board into the cardfile. Remove the board from the cardfile.
 - c. Move the voltage adjustment jumper from position JP1 to JP2.
 - d. Hold the PCB vertically in front of the cardfile.
 - e. Insert the PCB upper and lower edges into the plastic card guides inside the cardfile.

CAUTION

When installing any MICROLOK II circuit PCB into the cardfile, do not attempt to force the PCB into the slot. Damage to the circuit PCB and motherboard 96-Pin connector may result. If resistance is encountered when installing a PCB, gently rock the PCB to engage the male and female connectors. If the PCB still cannot be fully inserted into the card slot, remove the PCB from the cardfile and attempt to determine the source of the resistance.

- f. Gently push the PCB into the cardfile until the PCB and cardfile connectors are fully engaged.
- g. Restore battery power to the cardfile and allow the CPU PCB to reboot.

3. Recheck the OS track circuit voltage inputs per Step 2. If either voltage is still below 12.0VDC, repeat Steps 2.a through 2.g to move the voltage adjustment jumper to position JP3.
4. If either voltage is still below 12.0VDC with the jumper in position JP3, repeat Steps 2.a through 2.g to move the voltage adjustment jumper to position JP4.
5. Verify the jumper setting by placing a 0.06 ohm shunt across each leg of the OS circuit, one leg at a time. Each shunt must result in at least one of the two input voltages dropping below 3.0VDC. If this test fails, try lowering the jumper setting one position. Then re-check the input voltages and repeat the shunt test.

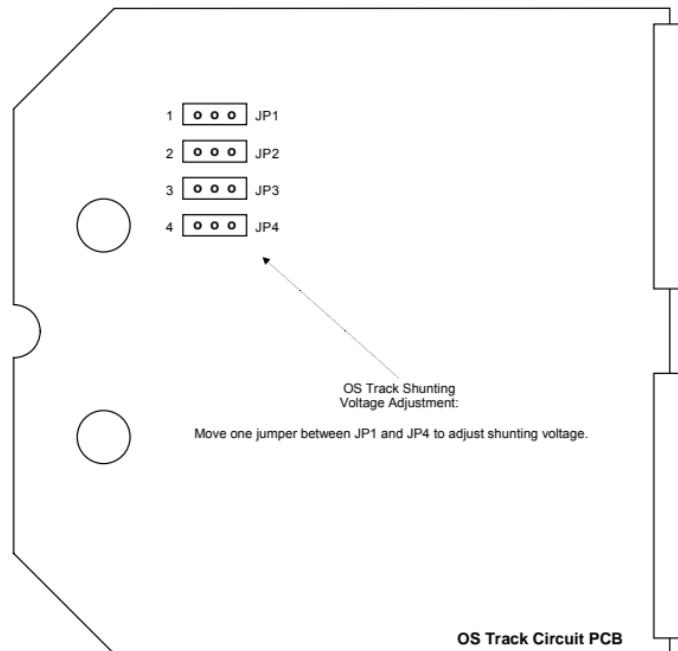


Figure 4-31.OS Track Circuit PCB Shunting Voltage Adjustment (Jumper)

4.9 Coded Track Communications

4.9.1 Track PCB

TRACK BOARD – N4519100701

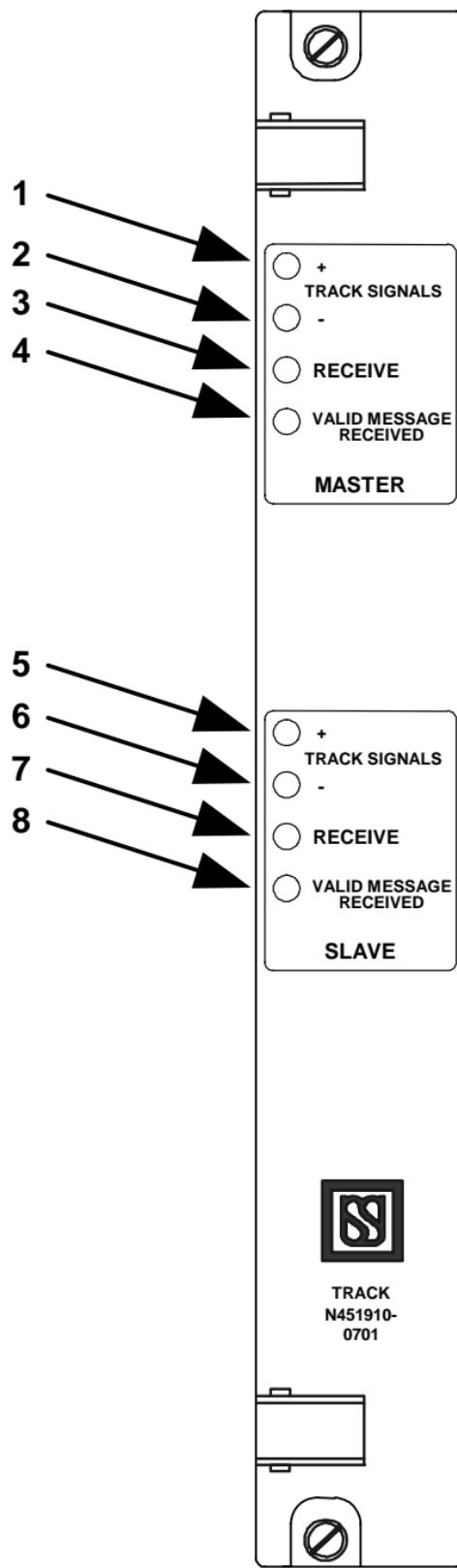


Figure 4-32. Track PCB Front Panel Detail

Table 4-14. Track PCB Indicators

REF FIGURE 4-32	LABEL	DEVICE	PURPOSE
1	TRACK SIGNALS + (MASTER)	Red LED	When flashing, indicates Master track circuit "+" code pulse (alternating with - LED). When dark, no Master track circuit activity.
2	TRACK SIGNALS - (MASTER)	Red LED	When flashing, indicates Master track circuit "-" code pulse (alternating with + LED). When dark, no Master track circuit activity.
3	RECEIVE (MASTER)	Red LED	When lit, indicates code received from Slave end of track circuit. When dark, indicates code transmission to Slave end of track circuit.
4	VALID MESSAGE RECEIVED (MASTER)	Red LED	When lit, indicates valid message received from Slave end of track circuit. When dark, indicates Master end track circuit message not accepted (track circuit shunted or in remove-shunt mode).
5	TRACK SIGNALS + (SLAVE)	Red LED	When flashing, indicates Slave track circuit "+" code pulse (alternating with - LED). When dark, no Slave track circuit activity.
6	TRACK SIGNALS - (SLAVE)	Red LED	When flashing, indicates Slave track circuit "-" code pulse (alternating with + LED). When dark, no Slave track circuit activity.
7	RECEIVE (SLAVE)	Red LED	When lit, indicates code received from Master end of track circuit. When dark, indicates code transmission to Master end of track circuit.
8	VALID MESSAGE RECEIVED (SLAVE)	Red LED	When lit, indicates valid message received from Master end of track circuit. When dark, indicates Slave end track circuit message not accepted (track circuit shunted or in remove-shunt mode).

The coded track circuit is based on an organized polling "handshake" type superiority protocol and the overall system track coding format must be designed for this feature. The Track PCB is capable of operating one "master" and one "slave" portion of two separate track circuits. Track connections are designated "Master" and "Slave" and "+" and "-". Either side of the insulated rail joints can be designated Master or Slave; however, after one end of a track circuit is designated Master or Slave, the other end must be given the opposite designation. When establishing rail polarities, two rules must be observed:

1. Polarity must be staggered or alternated across a set of insulated joints. For example, if the north rail is positive on the left side of the joints, the north rail must be negative on the right side of the joints.
2. The rail must have the same polarity at both ends of the same circuit.

Because the coding format is low frequency AC, track circuit lengths in the range of 22,000 feet @ 3 ohms ballast/1000 feet are attained.

The track code signal is connected to the rails through a Track Interface Panel consisting of a transformer and a low impedance inductor. There are four different types of single-track interface panels that provide inductance levels ranging from 10 to 40 mH. The 10 mH panel offers about 10 ohms impedance at 150Hz and proportionately more impedance at higher frequencies. This makes the MicroTrax system compatible with highway crossing motion and predictor equipment without need of external blocking units. The 15 mH Track Interface Panel is designed for maximum compatibility with 86Hz crossing predictors and should be used where there is 60Hz noise interference.

A received valid code indicates the track circuit is unoccupied.

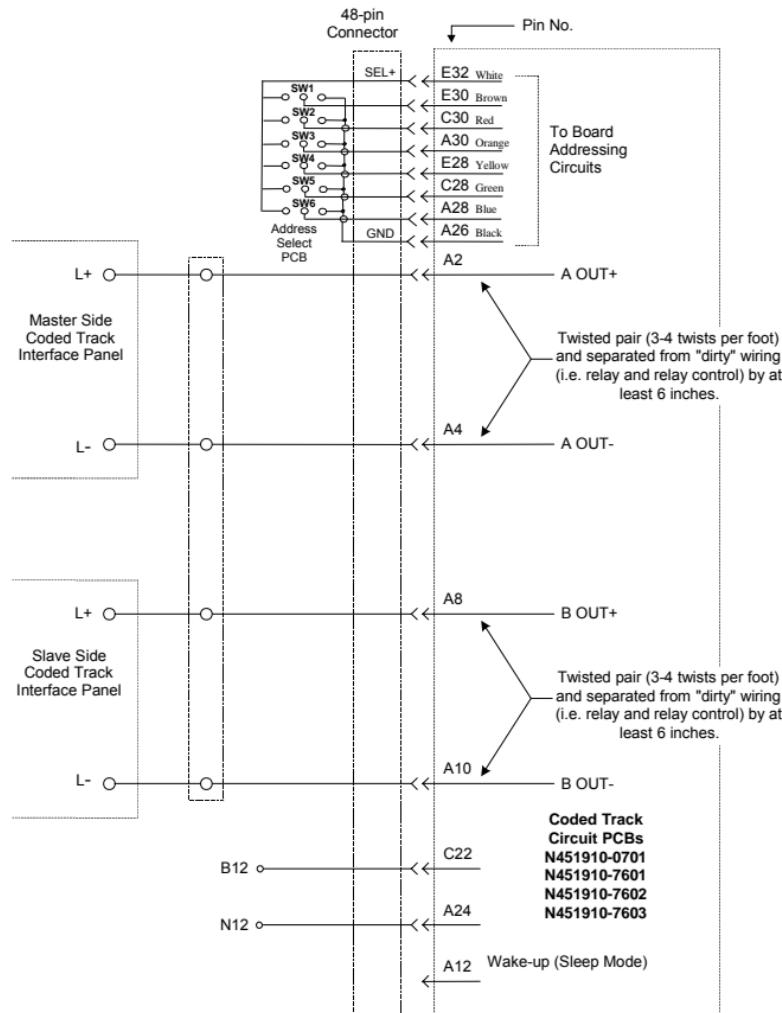


Figure 4-33. Track PCB - Board Pin-Outs

4.9.2 Quick Shunt Module

The optional Quick Shunt Module, N451052-4601 (See Figure 4-34), is used in applications where an improved shunt detection time is required. The quick shunt module reduces the detection time to approximately 100 milliseconds and contains circuitry for independent train detection on both sides of the insulated joint. Two 8-way screw-lock connectors are provided for external wiring. Internal circuits are contained in a type sheet metal housing designed for shelf or wall mounting. The unit contains no user displays or controls.

Two independent receivers on this device are connected to the coded track interface panels as shown in Figure 4-35. With this configuration, true shunt mode operation is attained without the need for separate track termination leads. The detection zone is limited to approximately 75 feet. For greater lengths, the transmitted and receiver track terminations must be separated.

Typically the action of the module is to initiate the cab signal transmission as the train enters the circuit without waiting for the MicroTrax circuit to declare occupancy.

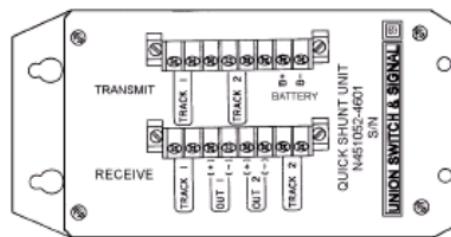


Figure 4-34.Quick Shunt Module

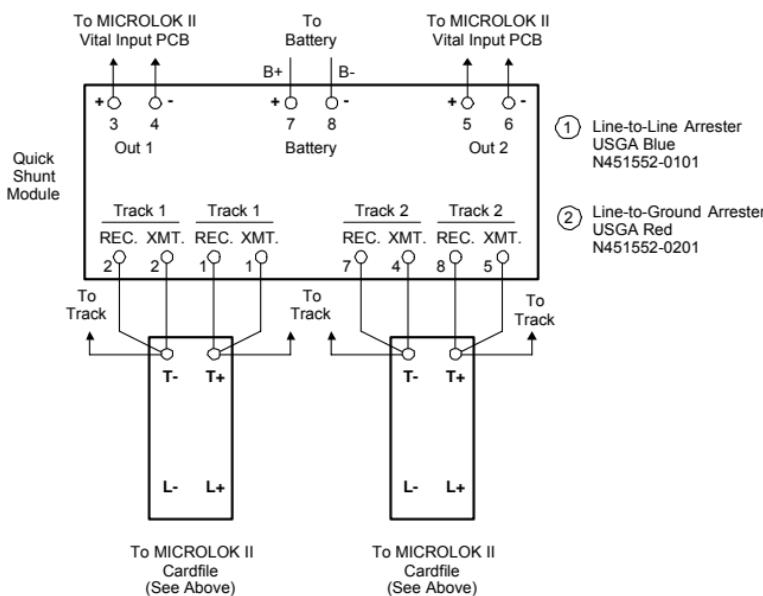


Figure 4-35.Quick Shunt Module – Basic Wiring Interface



4.9.3 Coder Output PCB

CODER OUTPUT – N4519105801

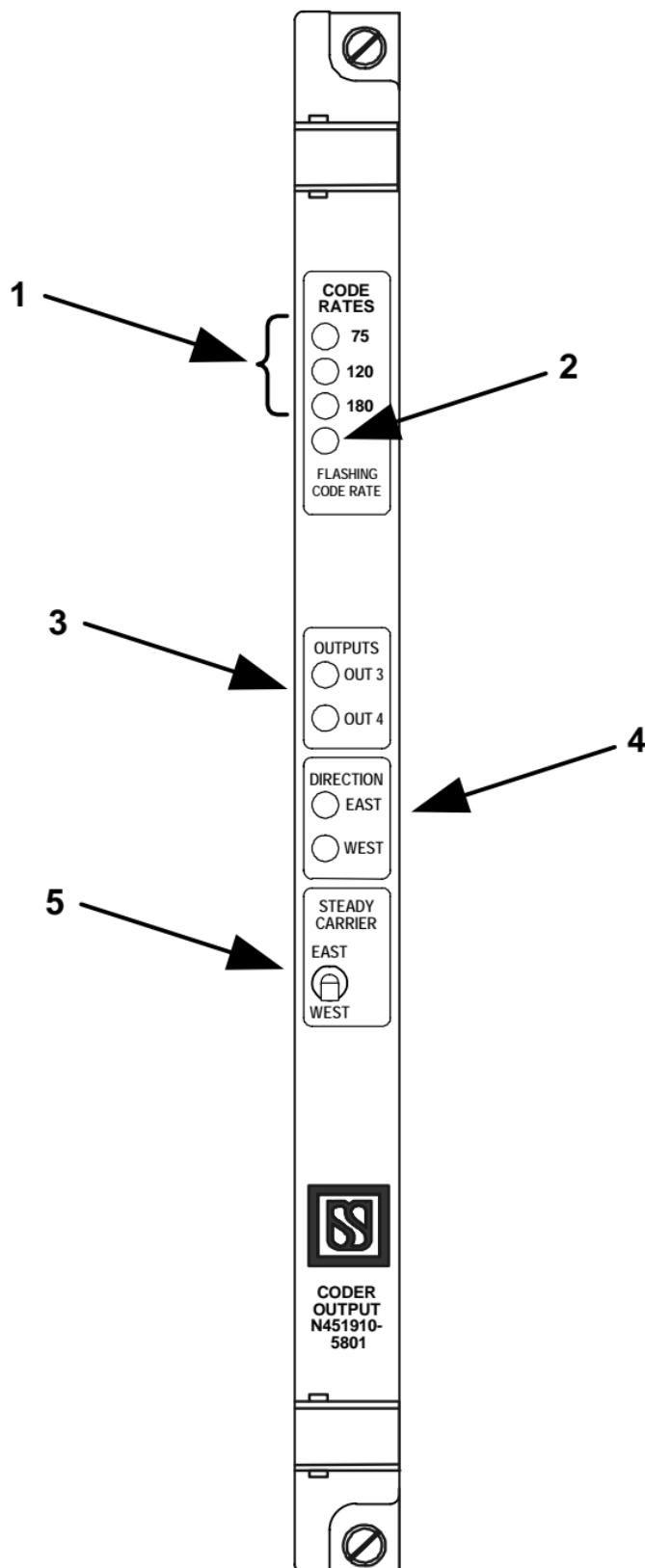


Figure 4-36. Code Output PCB Front Panel Detail

Table 4-15. Code Output PCB Indicators

REF FIGURE 4-36	LABEL	DEVICE	PURPOSE
1	CODE RATES 75, 120, 180	Green LEDs	When lit, indicates cab signal code rate in effect (CPM).
2	FLASHING CODE RATE	Green LED	When flashing, shows code rate pulse.
3	OUTPUTS OUT3, OUT4	Green LEDs	Not used in MICROLOK II systems.
4	DIRECTION EAST, WEST	Green LEDs	When lit, indicates track circuit direction selected by the CPU PCB.
5	STEADY CARRIER EAST, NORM, WEST	3-position toggle switch	<p>NORM position: Board configured for normal cab signal operation.</p> <p>EAST position: Steady energy applied to east track circuit during rail current adjustment procedure.</p> <p>WEST position: Steady energy applied to west track circuit during rail current adjustment procedure.</p>

The Coder Output and Cab Amplifier PCBs are used to generate cab signal carrier frequencies and code rates, and output these signals to the rails through cab signal interface panels. Each MICROLOK II cab signal application requires one coder output board and one or two cab amplifier boards installed in combinations listed in Table 4-16.

Table 4-16.Cab Coder/Cab Amplifier PCB Specifications

AMPLIFIER PCB	CODER PCB(S)	APPLICATION
N451910-6401	N451910-5801	For 60 or 100Hz carrier, 75/120/180 code rates
N451910-6901	N451910-5801, N451910-7001	For 40 or 50Hz carrier, 50/75/120/180 code rates

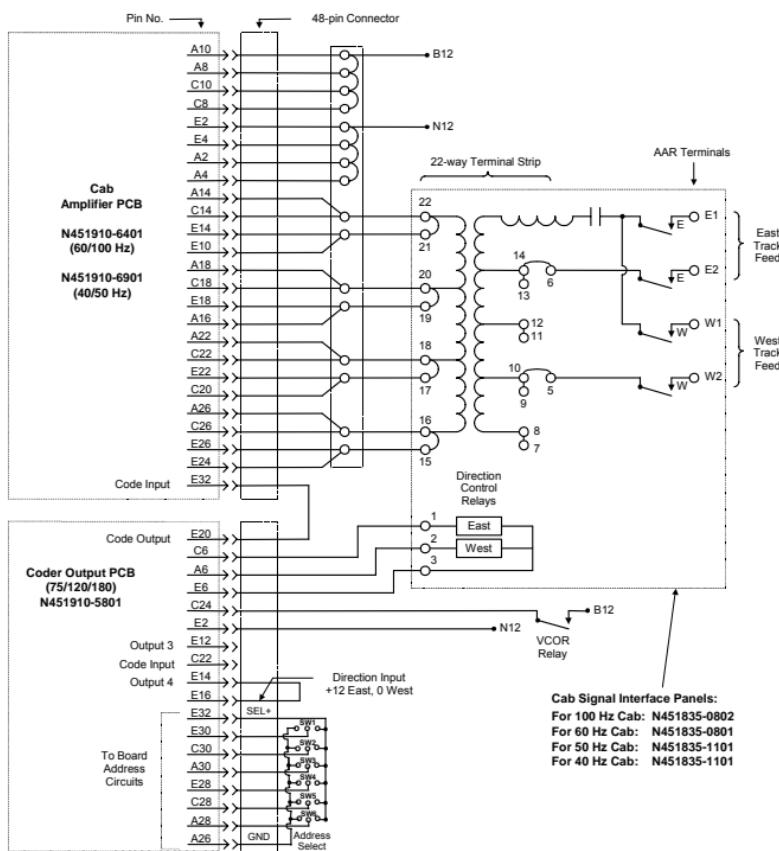


Figure 4-37.Code Output and Cab Amplifier PCB Basic Interface Wiring

The -5801 coder output PCB (75/120/180 CPM) is controlled by the MICROLOK II CPU PCB and requires an Address Select PCB with six two-position jumpers in the connector housing to set its cardfile bus address.

Code rates produced by the -5801 PCB are delivered to the cab amplifier PCB through the upper wiring connectors, not the cardfile bus. The Cab Amplifier PCB also operates separately from the CPU PCB (no cardfile bus communications). The Cab Amplifier PCB output is wired to the cab signal interface panel for final connection to the rails.

Cab amplifier output connections to cab panel transformer primary are doubled to carry the extra current load. The East and West direction relays on the panel are energized through three additional wire connections. A jumper is required between pin-outs E14 and E16 on the Coder Output PCB (See Figure 4-37). This jumper provides the east/west direction input from output #4 on the Coder Output PCB.

4.9.4 Cab Amplifier PCB

CAB AMPLIFIER – N4519106401

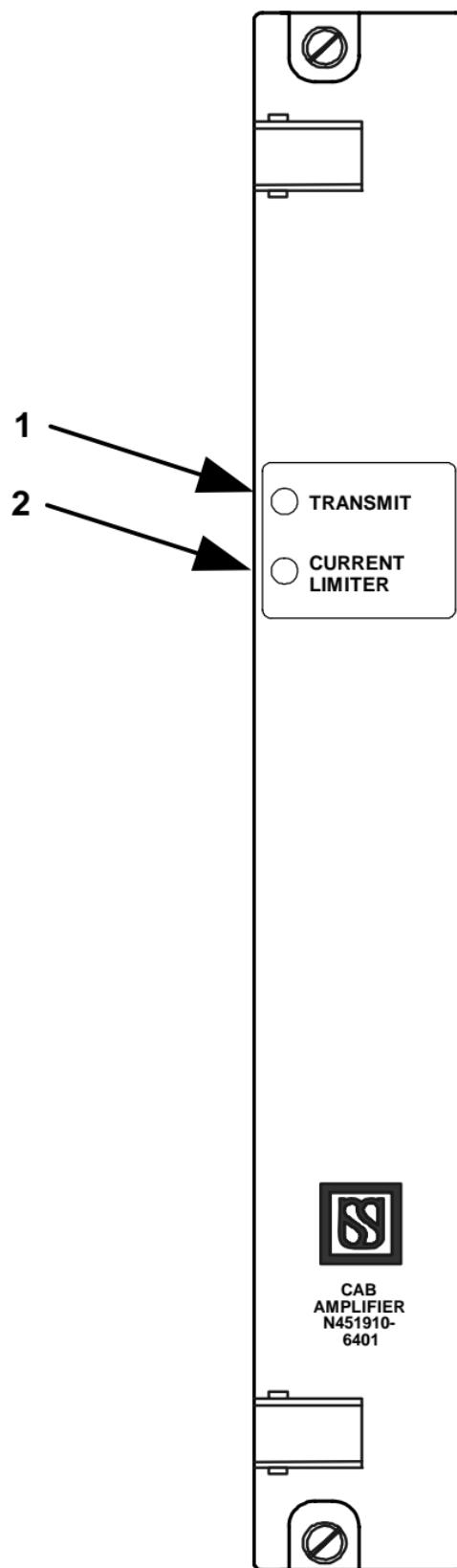


Figure 4-38.60/100HZ Cab Amplifier PCB Front Panel Detail

Table 4-17.60/100Hz Cab Amplifier PCB Indicators

REF FIGURE 4-38	LABEL	DEVICE	PURPOSE
1	TRANSMIT	Green LED	When lit (flashing or steady), indicates transmission of coded cab signal to the associated cab signal interface panel.
2	CURRENT LIMITER	Red LED	Monitors on-board current-limiting circuit. When lit (flashing or steady), indicates active circuit.

5 NON-VITAL PCBS

NV.IN32 – Non-Vital 32 Isolated Inputs – N17063701
NV.OUT32 – Non-Vital 32 Isolated Outputs – N17062701

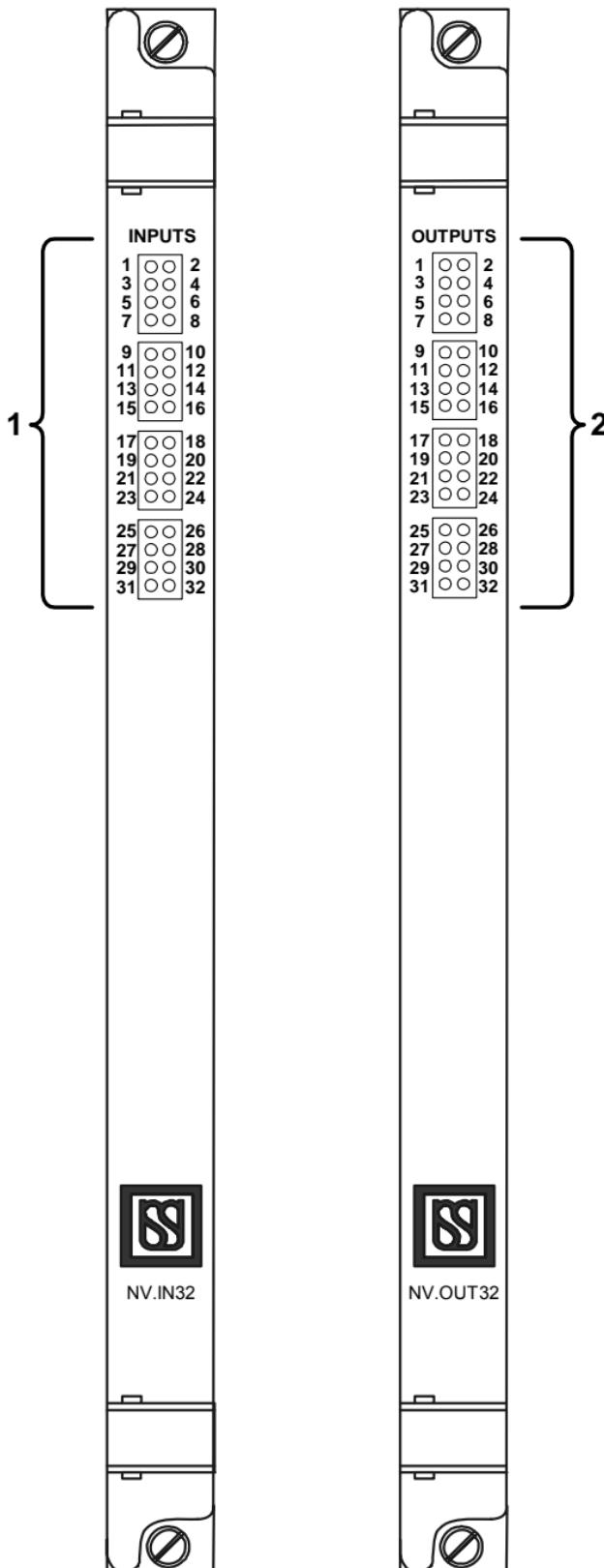


Figure 5-1.NV.IN32 and NV.OUT32 Front Panel Detail

5.1 Input and Output PCBs (NV.IN32, NV.OUT32)

Table 5-1.NV.IN32/NV.OUT32 Indicators

REF FIGURE 5-1	LABEL	DEVICE	PURPOSE
1	INPUTS 1-32	Green LEDs	Monitors states of non-vital inputs 1-32. When LED is lit, respective input is on.
2	OUTPUTS (SWITCHED TO N12) 1-32	Yellow LEDs	Monitors states of non-vital outputs 1-32. When LED is lit, respective output is on.

5.1.1 PCB Top Connector Wiring Interface

Refer to Figure 5-3 and Figure 5-5 for PCB pin-out information and Figure 2-2 for PCB top connector pin configuration.

Representative block diagrams of an input and output are given in Figure 5-2 and Figure 5-4.

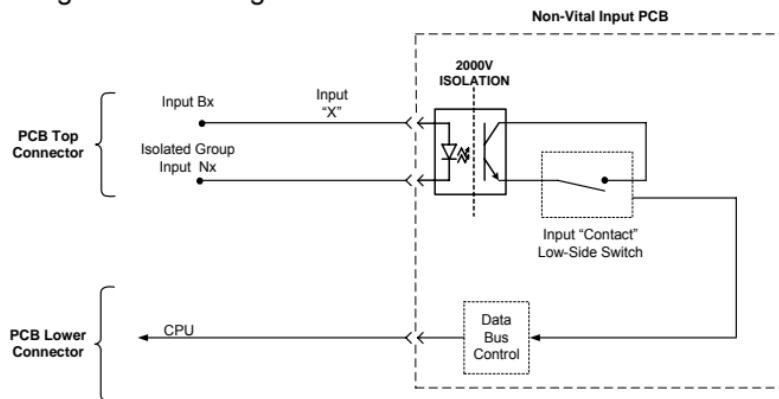


Figure 5-2.NV.IN32 Block Diagram

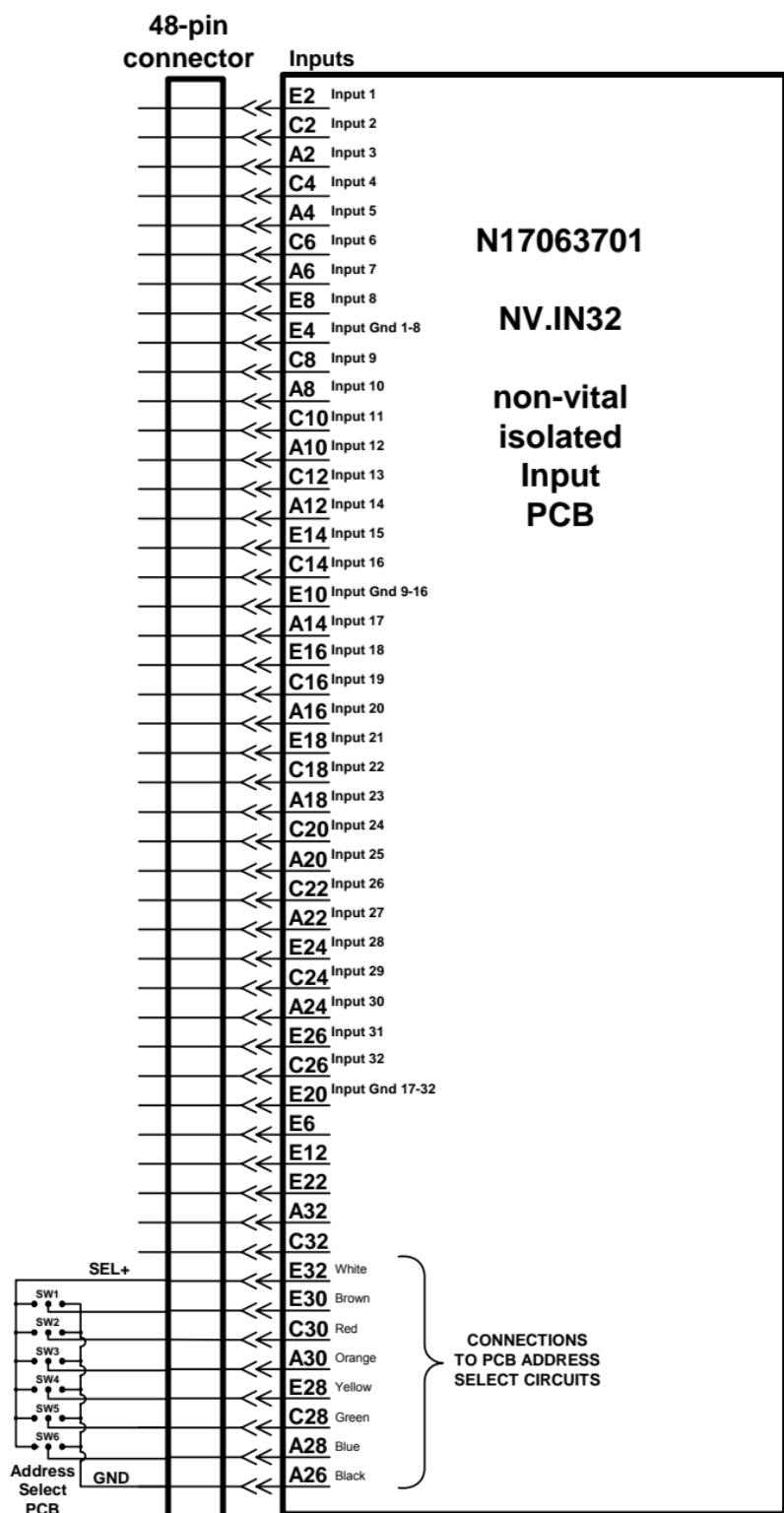


Figure 5-3. Non-Vital IN.32 PCB - Board Pin-Outs

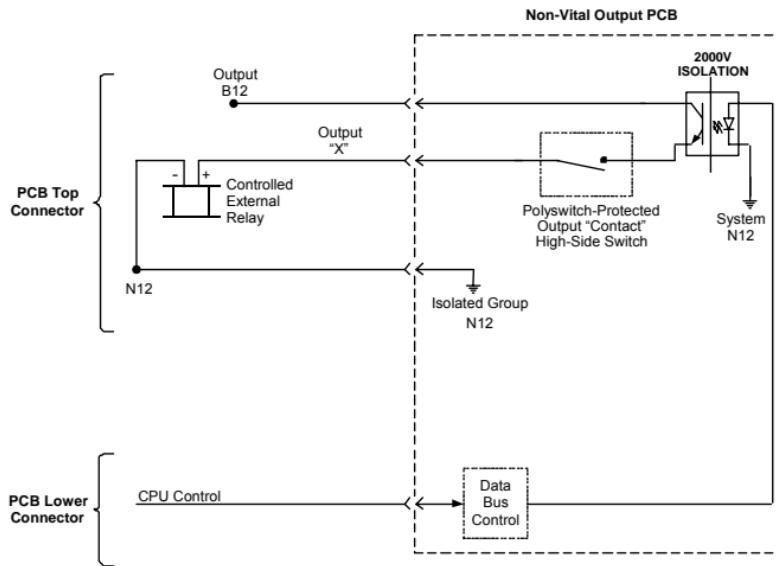


Figure 5-4.NV.OUT32 Block Diagram

(Example Only)

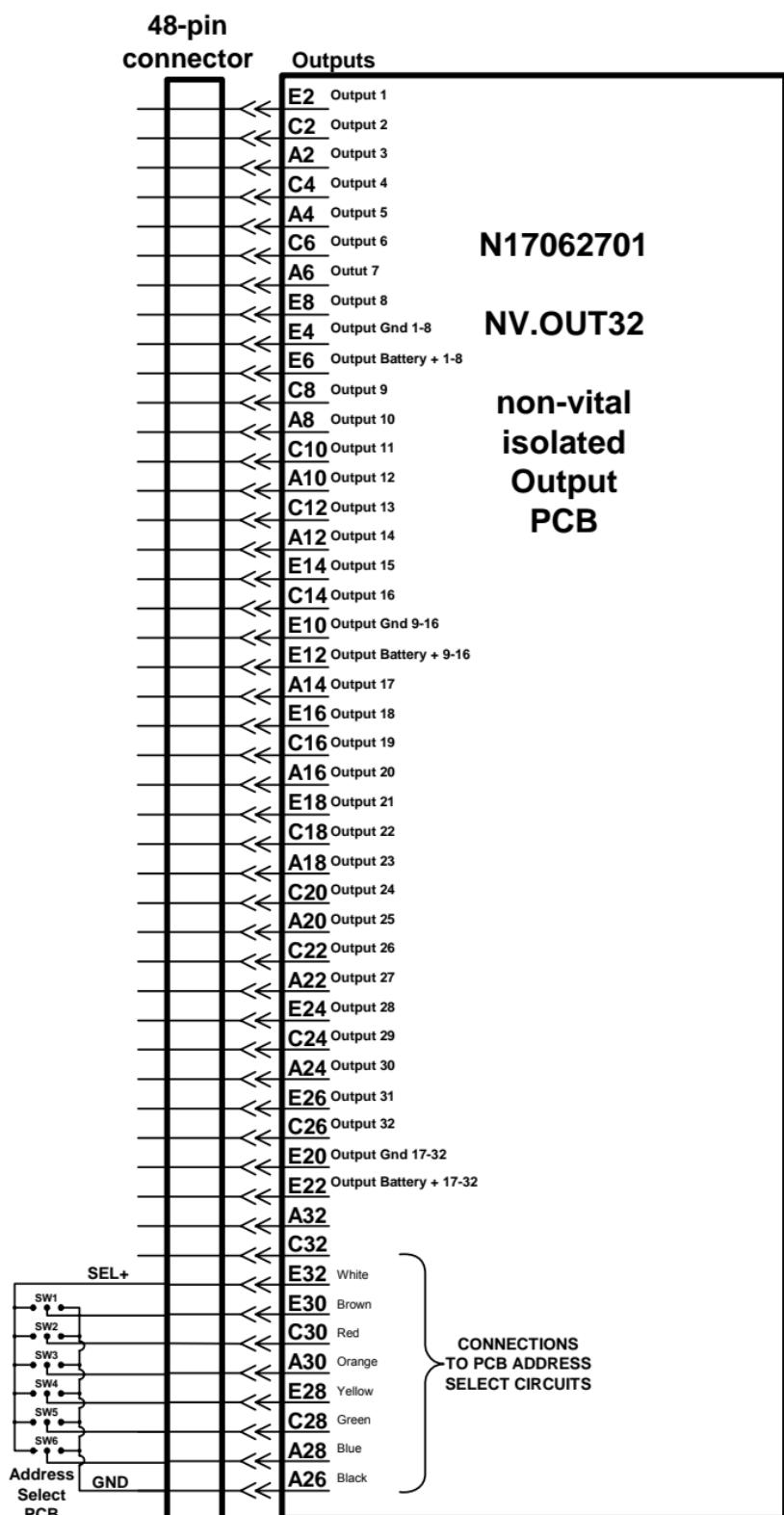


Figure 5-5. Non-Vital OUT.32 PCB - Board Pin-Outs



5.2 Non-Vital Input/Output PCB (NV.IN32.OUT32)

Non-Vital 32 Inputs/32 Outputs – N17061501

Non-Vital 16 Inputs/8 Outputs – N17000601 (for cardfile LCP)

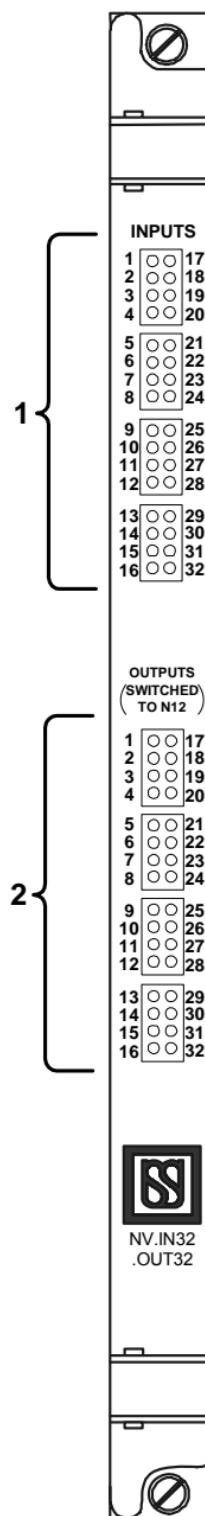


Figure 5-6.NV.IN32.OUT32 PCB Front Panel Detail

Table 5-2. Non-Vital 32 I/O PCB Indicators

REF FIGURE 5-6	LABEL	DEVICE	PURPOSE
1	INPUTS 1-32	LEDs (Green)	Monitors states of non-vital inputs 1-32. When LED is lit, respective input is on.
2	OUTPUTS (SWITCHED TO N12) 1-32	LEDs (Yellow)	Monitors states of non-vital outputs 1-32. When LED is lit, respective input is on.

Table 5-3. Non-Vital 32 I/O PCB Specifications

ASTS USA PART NO.	INPUT AND OUTPUT VOLTAGE RANGE	EXTERNALLY AVAILABLE INPUTS	EXTERNALLY AVAILABLE OUTPUTS	CURRENT RATING ON OUTPUTS
N17006101	6.0 to 30.0VDC	16	8	Outputs 25-30: 0.5A fuse Outputs 31, 32: 5.0A fuse*
N17061501	6.0 to 30.0VDC	32	32	Outputs 1-30: 0.25A (polyswitch-protected) Outputs 31, 32: 5.0A fuse*

*Suitable for lighting lamp up to 25W.

The non-vital I/O PCBs use latch ICs to buffer inputs and Field Effect Transistors (FETs) to drive outputs. The input/output LEDs are under software control and thus indicate the internal logic state of the inputs/outputs, as opposed to being under the direct hardware control of the input/output voltage.

The N17061501 PCB contains 32 Input circuits and 32 Output circuits. All of these circuits are non-vital and are non-isolated (i.e., they are common to system ground). Each output circuit contains a "low-side" FET transistor switch, which is turned On or Off by the I/O Bus. This switch grounds the circuit's load; the other side of which is connected to system battery voltage.

Outputs (1 through 30) employ 0.5Amp PolySwitches (self-resetting semiconductor devices), to protect the output circuitry, allowing the PCB to drive a variety of loads.

Two outputs (31 and 32) on both PCB types are protected by 5A fuses. These output circuits are reserved for control of a relatively high current device.

Note that this PCB does not make use of the vital power source created via the system Conditional Power Supply (CPS) and the system Vital Cut-Off Relay (VCOR). Therefore, the PCB's operation is unaffected by the state of the VCOR.

The LCP version of this PCB (N17000601) is designed for use with the optional MICROLOK II cardfile Local Control Panel (LCP) – N16901301. This version of the PCB is fitted with a 48-pin connector on the front and back. The front connector engages the LCP. The remaining PCB I/O (16 Inputs and 8 Outputs), are available on the top rear connector.

The PCBs may be used in both nominal 12V battery and nominal 24V battery systems.

CAUTION

Output power ground (e.g., N12) tie points (Pins A17 through C29) – at least one of these pins must be connected to output power ground to prevent possible damage to the PCB.

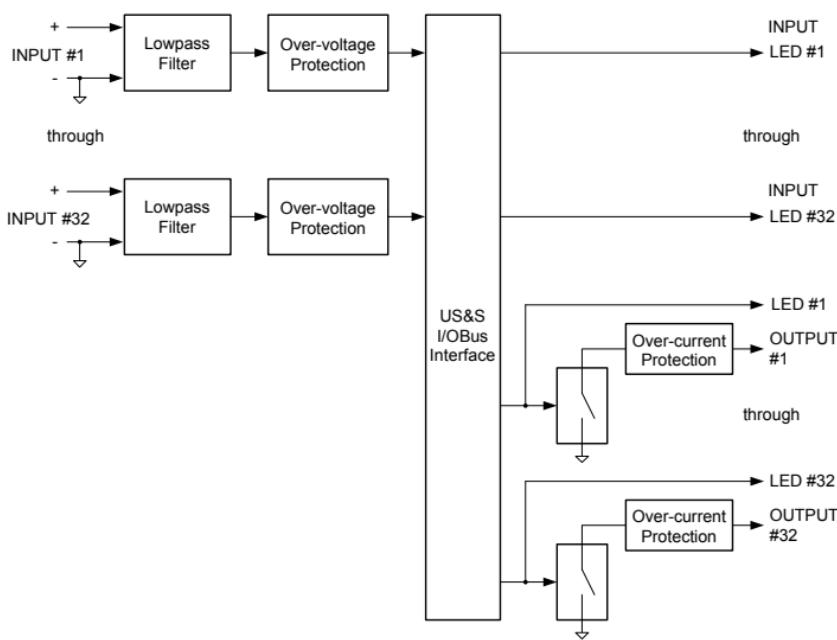


Figure 5-7.NV.IN32.OUT32 PCB - Block Diagram



6 SYSTEM TROUBLESHOOTING

6.1 Power Troubleshooting

Table 6-1.Instrument House Power Distribution System Troubleshooting Guide

SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Loss of AC Power	Circuit breaker or safety switch open.	<p>Note: This fault indication could be due to any of three source failures: commercial power, emergency power, or the POR.</p> <p>Check breaker at signal circuit breaker panel. Check commercial power line breakers. Check emergency power safety switch. Close as required.</p>
	Component failure or loss of commercial power external to ASTS USA system.	Troubleshoot commercial and emergency power inputs to relay house or room. Check wiring, transfer panel, and isolation transformer.
	POR failure.	Check POR for proper function. Replace as required.
	Wiring failure in AC power circuit.	Check circuits associated with AC power distribution (power input, POR, ground). Repair as required.
	Non-vital MICROLOK II failure.	Troubleshoot non-vital MICROLOK II. (Refer to MICROLOK II Service Manuals).
DC Power Interruption	Breaker on signal circuit breaker panel open.	<p>Note: This fault indication could be from any of the 12V rectifiers.</p> <p>Check applicable circuit breakers on signal breaker panel. Close as required.</p>
	Rectifier breaker open.	Check that input and output circuit breakers of the 12V rectifiers are closed. Close as required.
	Rectifier failure.	Test rectifiers for proper power output. Replace failed rectifier.
	Wiring failure in DC power distribution circuit.	Check DC power distribution circuits. Repair as required.
	Non-vital MICROLOK II failure.	Troubleshoot non-vital MICROLOK II. (Refer to MICROLOK II Service Manuals).

SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Loss of power at MICROLOK II	Wiring/breaker failure in battery charger supply circuits.	Check for wiring failure or blown fuse in power distribution circuits supplying applicable battery charger. Repair as required.
	Wiring failure in charger output DC power supply distribution circuit (downstream of chargers).	Check applicable DC power distribution circuits from chargers to system battery supplies to MICROLOK II for wiring failure. Repair as required.
Loss of power at groups of components (signals, switches etc.)	Wiring failure or blown fuse downstream from applicable rectifier or charger.	Check for wiring failure or blown fuse in power distribution circuits downstream from applicable rectifier/charger. Repair as required.
Loss of AC power input at both battery chargers (system power provided by batteries)	Main circuit breaker open.	Close main breaker at circuit breaker panel.
	Loss of power input to CIH breaker panel.	First, check for commercial and emergency power input at external distribution point (applicable house/room breaker panel). Re-establish power as required. If power is present at external distribution point, check for failures in wiring and components between the distribution point and the CIH breaker panel. Repair wiring or replace components as required.
Loss of AC power input at one battery charger (power input OK at other charger)	Battery charger breaker at circuit breaker panel open.	Close battery charger breaker at circuit breaker panel.
	Wiring failure between breaker panel and battery charger.	Check wiring between breaker panel and battery charger. Repair as required.

SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Battery charger does not output power	Battery charger breaker at circuit breaker panel open.	Close battery charger breaker at circuit breaker panel.
	Battery charger input or output circuit breaker open.	Close battery charger circuit breaker.
	Battery charger failure.	Test battery charger for proper power output. Replace as required.
	Wiring failure between breaker panel and battery charger.	Check wiring between breaker panel and battery charger. Repair as required.
Battery voltage output low or nonexistent	Wiring failure between battery cells or between battery and bus.	Check wiring between battery cells. Check wiring between battery and bus. Check connections at battery cell terminals. Repair as required.
	Battery charger improperly adjusted and not charging battery correctly.	Check that variable settings (no. of cells, battery type, float voltage) on battery charger are set properly. Adjust as required. (Refer to battery charger manual.)
	Battery cell failure.	Test individual battery cell voltages. Replace cell as required.
	Battery charger failure.	Test battery charger for proper power output. Replace as required.
DC bus voltage low or high	Battery charger improperly adjusted.	Check that variable settings (no. of cells and float voltage) on battery charger are set properly. Adjust as required. (Refer to battery charger service manual.)

SYMPTOM	POSSIBLE CAUSE	CORRECTIVE ACTION
Power-off indicated by MICROLOK II	Power-off relay (POR) de-energized due to AC power loss.	Refer to the failure symptom listed above, "loss of AC power input at both battery chargers." Possible causes and corrective actions are the same. Re-establish AC power accordingly.
	Wiring failure between circuit breaker panel and POR.	Check wiring between breaker panel and POR. Repair as required.
	POR failure.	Check POR for proper function. Replace POR as required.
	Non-vital MICROLOK II failure.	Troubleshoot non-vital MICROLOK II. (Refer to MICROLOK II Service Manuals).

7 CARDFILE CABLING/WIRING

7.1 Noise Protection

7.1.1 General Wiring Practices

MICROLOK II installations that are wired in the field should be configured to minimize cross talk between wires. "Dirty" wiring (connections to external equipment) should be separated as much as possible from wires carrying electronic data signals. Cables and wires in general should be kept as short as possible to minimize induced line noise. (The input and output wires should be twisted in pairs). Case/house wiring layouts should also be arranged to minimize noise. Switch heater wire runs, track leads, switch machine power wiring and any other "noisy" wiring should be separated as much as possible from MICROLOK II wiring, both in the case or house and in outside cable runs. Battery leads should be as short as possible and must be isolated as much as possible from noisy wiring.

Output battery busses should be isolated from other battery busses to minimize interference.

VCOR relays switching LAMP board output battery should always be installed in the same equipment rack as the cardfile containing the LAMP16 PCB.

7.1.2 Relay Coil Snub

Relay snubs are intended to dissipate large electromagnetic surges from the coil inductance and to prevent these surges from interfering with normal operation of the MICROLOK II system. It is recommended that all relays being driven by MICROLOK II be snubbed to prevent unwanted monitor errors. This is particularly true where the coil load to the MICROLOK II relay driver is being broken by a series contact.

Relay snubs can also be installed on other relays that are not directly controlled by MICROLOK II outputs, but may be contributing to possible noise due to their close proximity to the MICROLOK II wiring.

ASTS USA recommends the use of TransZorbs (J7927360030, [5KP16A] 16 volt) for relay snubbing. They will have minimal effect on relay timing.

Resistors are also suitable relay snubs. When using a resistor loading of the MICROLOK II output an effect on timing (relay drop away) must be considered.

Diodes can also be used as snubs but:

1. They will definitely increase relay drop time.
2. They may cause contact burning in some circuits.

WARNING

Do not use diodes or any devices that could function as a diode in AC or DC electrified territory; otherwise, voltage induced by the device could cause a relay to remain falsely energized.

7.1.3 Twisted Wire

ASTS USA recommends the use of twisted pair wiring (2 to 3 turns per foot) for all relay loads to minimize possible noise. This should be done wherever possible on all I/O wiring.

7.1.4 Wire Separation

ASTS USA recommends the physical separation of clean and dirty wiring.

- a. All output wires should be gathered into a bundle.
- b. Input wires should be gathered into a bundle.
- c. Power wiring should be gathered into a bundle.
- d. Each of these bundles should be physically separated from each other and all bundles physically separated from other house wiring.
- e. It is particularly important to maintain this physical separation from high-current "dirty" wiring.

7.2 MICROLOK II Cardfile Cabling

The configuration of the external wiring to each MICROLOK II printed circuit board depends entirely on the PCB type and the selected application.

- ASTS USA recommends the use of twisted pair wiring (2 to 3 turns per foot) for all relay loads to minimize possible noise. This should be done wherever possible on all I/O wiring.
- Cables and wires in general should be kept as short as possible to minimize induced line noise.
- Battery leads should be as short as possible to minimize voltage drop. They also must be isolated as much as possible from noisy wiring.

When wiring a vital input PCB through a relay contact circuit contained in the same house as the MICROLOK II cardfile, the signal battery may be used as the energy source to activate the inputs. Terminals designated (-) may be connected to battery N12 and B12 switched over relay contacts.

7.2.1 Cardfile Grounding

All MICROLOK II circuitry is isolated from the MICROLOK II cardfile chassis. This allows the cardfile to be connected to earth ground for shielding purposes if desired.

7.2.2 Lightning Protection

In geographic areas where the incidence of lightning is moderate to high, the following external lightning protection is recommended:

- The physical location of the protection devices should be at the Main Terminal Board.
- External wiring should be protected with an equalizer lightning arrester from line-to-line (ASTS USA Part Number N451552-0101) and with high voltage arresters from line-to-ground (ASTS USA Part Number N451552-0201) on each wire pair.
- The recommended protection device is a Gas Discharge Tube Surge Arrester, Littelfuse CG2-145L (ASTS USA Part Number J7927360131).
- This is a two-wire device with no polarity concerns. One of these devices is to be wired between each pair of equalizer lines leaving the Signal House and earth ground.

When the gas arresters are installed, one side of every arrester will be grounded. The arresters should be grouped so that they all share a solid grounding bus. This bus must be connected to the earth ground using the shortest, most direct path possible (no wire bends if possible). It is recommended that two #6 American Wire Gauge (AWG) conductors be used to make the connection from the grounding bus to earth ground.

7.2.3 Non-Isolated Vital Output PCB

In the case of a non-isolated vital output PCB in a cardfile powered by a Power Supply PCB observe the typical wiring convention shown in Figure 7-1.

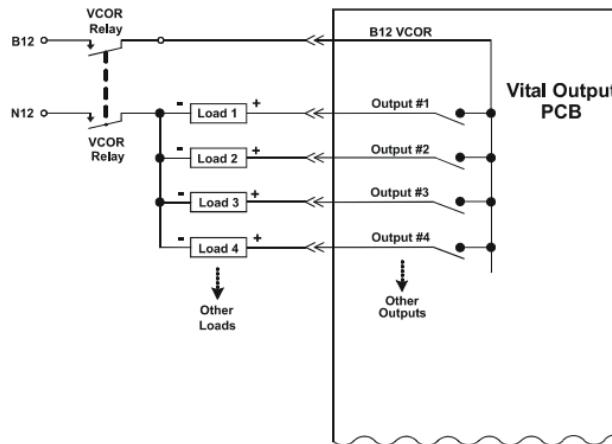


Figure 7-1.Single MICROLOK II Unit Driving More than 16 Loads



8 SERIAL COMMUNICATION

Selection of the CPU serial ports is handled entirely in the MICROLOK II application software; Comm1 and Comm2 are configured as RS-485 format, Comm3 is RS-232/423 format (jumper selectable on CPU PCB – See Figure 2-3), and Comm4 is RS-232 format.

During configuration all of the communication ports in a MICROLOK II unit must be vitally enabled and disabled in software so that the unit's communication ports are enabled.

Pin-outs for the CPU top connector are listed in Table 8-1.

Table 8-1. Serial Connections to CPU Top Connector

SIGNAL	PORT 1 RS-485	PORT 2 RS-485	PORT 3 RS-423	PORT 4 RS-232
TXD-	A2	A16	E16	C20
TXD+	A4	A18		
RXD-	C6	A24	E14	C22
RXD+	C8	A26		
RTS-	E2	A20	C14	A14
RTS+	E4	A22		
CTS-	A10		E12	
CTS+	A12			
DCD-	C10	A28	E10	C16
DCD+	C12	A30		
TXC-	C2		A6	
TXC+	C4			
RXC-	E6		A8	
RXC+	E8			
RXREF			E18	
COM (0V)	A32	A32	C18	E22
+12V	C24	C24	C24	C24
-12V	C26	C26	C26	C26

8.1 Serial Link Relay

Serial Link Relay PCB – N17002301

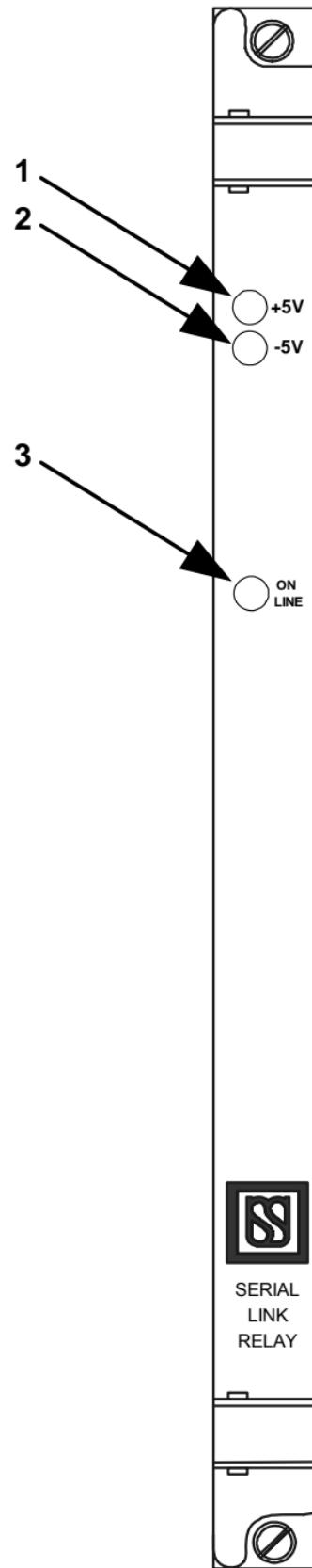


Figure 8-1. Serial Link Relay Front Panel Detail

Table 8-2. Serial Link Relay PCB Indicators

REF FIGURE 8-1	LABEL	DEVICE	PURPOSE
1	+5V	Red LED	Monitors the state of the +5 volt system power. When lit it indicates the +5 volts is present.
2	-5V	Yellow LED	Monitors the state of the -5 volt power on this PCB. When lit it indicates the -5 volts is present.
3	On Line	Green LED	Indicates which Serial Link Board and which cardfile is on-line. For units with a VCOR, when lit it indicates the unit is on-line and sending serial information. For units without a VCOR, it indicates system power.

A special cardfile is required for this PCB since it plugs into its own motherboard (Serial Link Motherboard) located at the left-front side of the cardfile. The Motherboard/Backplane for the cardfile using the Serial Link Relay PCB has only seventeen available PCB slots vs. the standard twenty-slot MICROLOK II cardfile.

A cable from the CPU top connector to the Serial Link Motherboard connects the CPU serial outputs to four serial ports on the Serial Link Relay PCB that can be manually configured to suit the serial system communication line project needs.

The PCB provides a non-vital means of connecting and disconnecting a MICROLOK II unit's serial links to the system communication lines. Serial lines from the CPU pass through the Serial Link Relay Board's relay contacts. Typically these relay coils are energized by voltage passing through the VCOR contacts. This allows the Transmit Data (TxD) and Request-to-Send (RTS) lines to be disconnected from the external wiring when the VCOR is dropped.

The PCB also provides two level shifters to convert RS-232 lines to RS-485 thus allowing four RS-485 serial links.

External communication ports are wired to "D" connectors on the Serial Link Motherboard. A set of four Dual In-line Package (DIP) switches with associated termination resistors are located on the Serial Link Motherboard for termination/biasing of the RS-485 communication ports.

8.1.1 Serial Link Relay PCB Jumpers

When replacing this PCB refer to the location Book of Plans for correct positioning of jumpers 1 through 4. These jumpers select the serial protocol of Comm3 and Comm4.

NOTE

The protocol set by these jumpers must match the corresponding outputs of the Com links on the CPU.

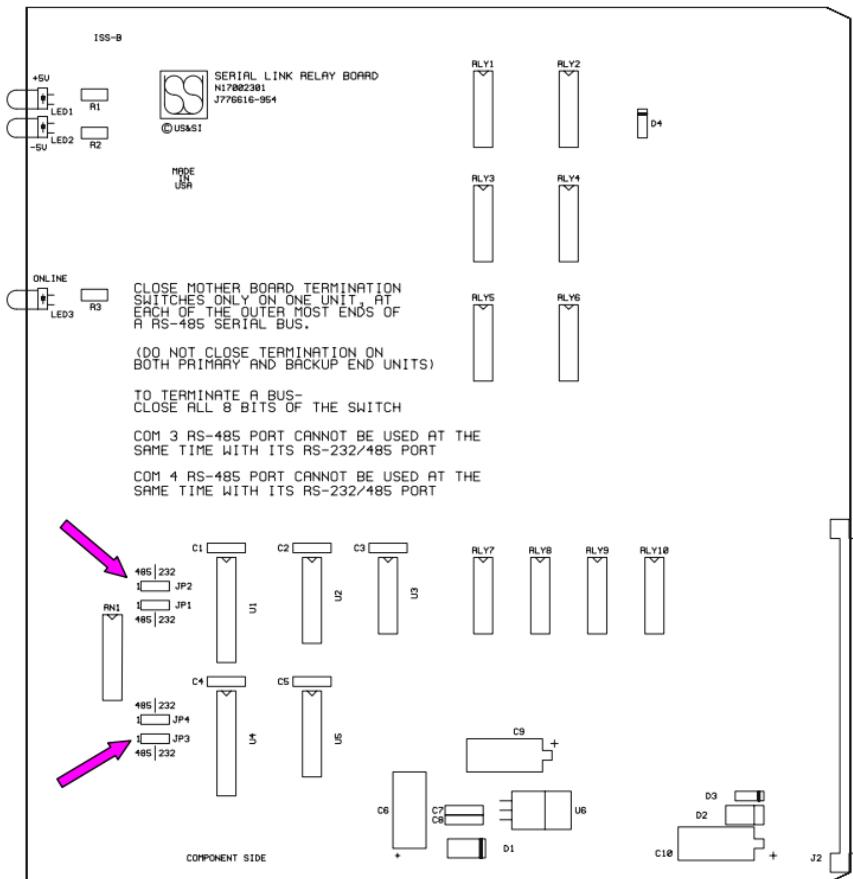


Figure 8-2. Serial Link Relay PCB Detail

8.1.2 Serial Link Motherboard Configuration

Cardfile/w Backplane and Serial Link Motherboard PCBs – N16903101

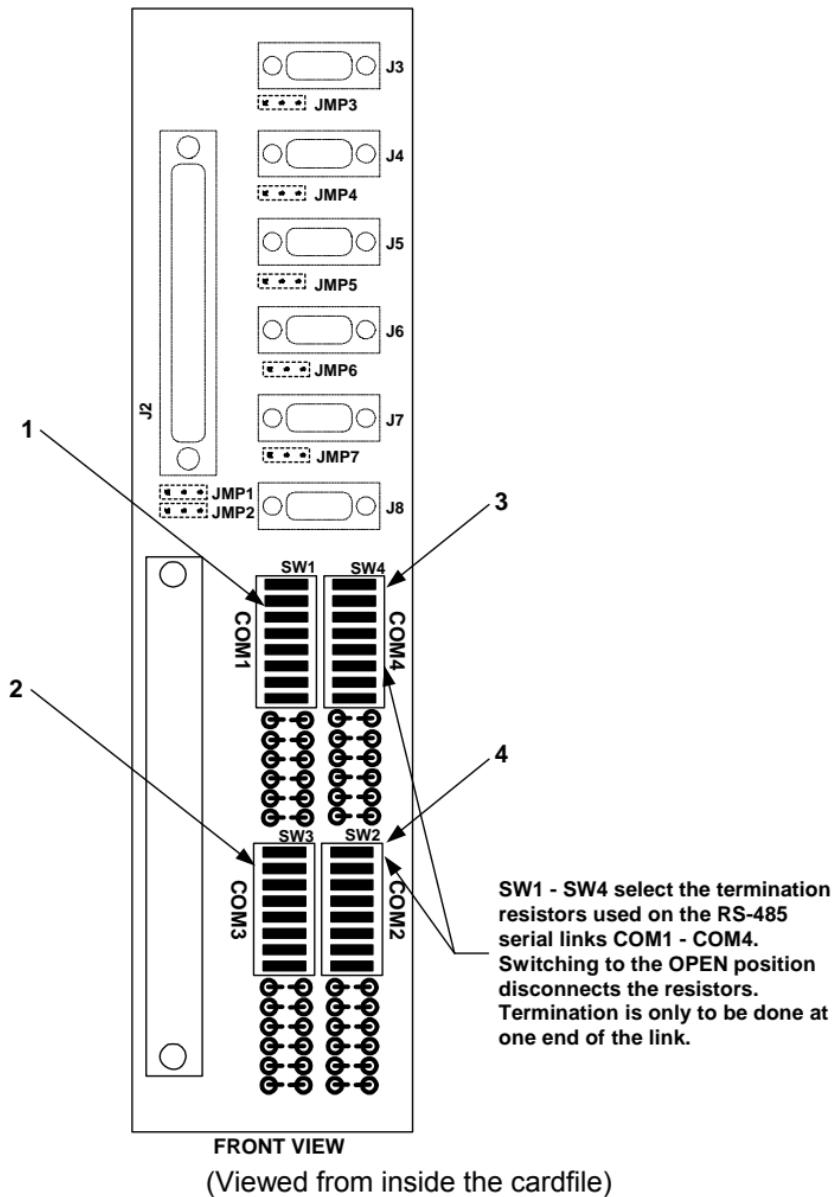


Figure 8-3. Serial Link Motherboard Front View

(Dual In-Line Package [DIP] Switches for the RS-485 Termination Resistors)

Table 8-3. Serial Link Motherboard Termination Configuration

REF FIGURE 8-3	LABEL	DEVICE	PURPOSE
1	SW1	Eight-position Dip Switch	COMM1 serial link termination.
2	SW3	Eight-position Dip Switch	COMM3 serial link termination.
3	SW4	Eight-position Dip Switch	COMM4 serial link termination.
4	SW2	Eight-position Dip Switch	COMM2 serial link termination.

Table 8-4. Serial Link Motherboard Jumper Configuration

REF FIGURE 8-4	LABEL	DEVICE	PURPOSE
1	JMP3	Two-position Jumper	Position 1-2 uses local ground, 2-3 uses remote common for COMM1, RS-485.
2	JMP4	Two-position Jumper	Position 1-2 uses local ground, 2-3 uses remote common for COMM2, RS-485.
3	JMP5	Two-position Jumper	Position 1-2 uses local ground, 2-3 uses remote common for COMM3, RS-485.
4	JMP6	Two-position Jumper	Position 1-2 uses local ground, 2-3 uses remote common for COMM4, RS-485.

REF FIGURE 8-4	LABEL	DEVICE	PURPOSE
5	JMP7	Two-position Jumper	Position 1-2 uses local ground, 2-3 uses remote common for COMM4, RS-232.
6	JMP1 and JMP2	Two-position Jumpers	<p>Setting JMP1 to position 1-2 COMM3 RS-232/423 uses local ground as reference.</p> <p>Setting JMP2 to position 1-2 grounds the cable common for COMM3 RS-232/423.</p> <p>Setting both JMP1 and JMP2 to 2-3 uses remote ground as COMM3 RS-232/423 reference.</p>

NOTE

Concerning GND selection jumpers: J7 uses JMP1 and JMP2, and J8 uses JMP7.

ASTS USA recommends jumper position 1-2 (local GND) for all serial outputs.

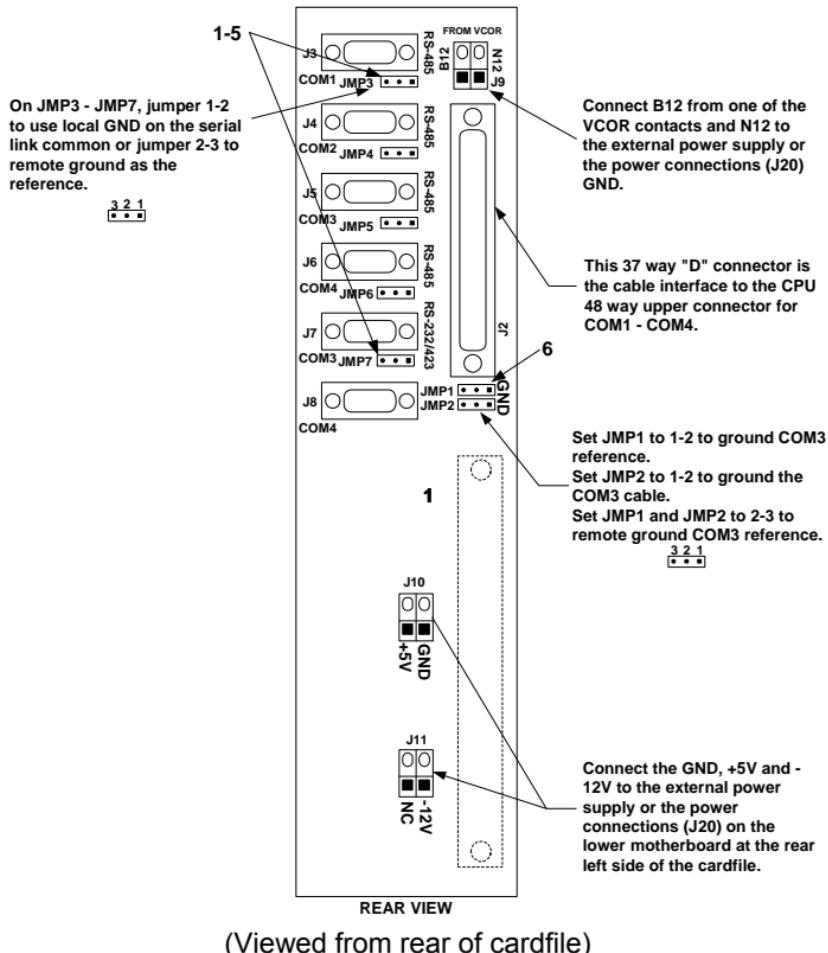


Figure 8-4. Serial Link Motherboard Configuration Jumpers



8.2 Serial To Ethernet Converter

Part Number – N16920401

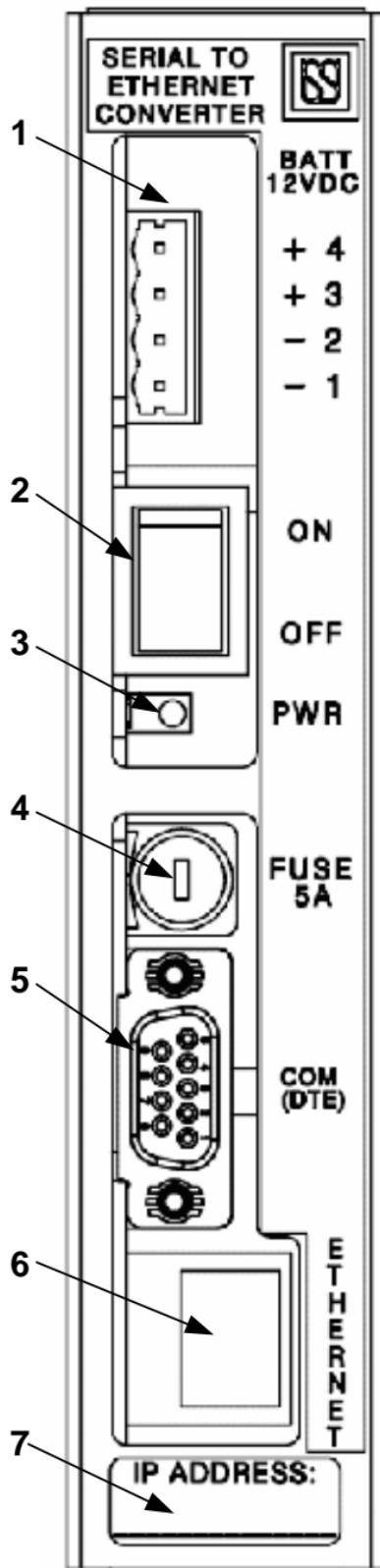


Figure 8-5. Serial To Ethernet Converter - Front Panel Detail

The Serial to Ethernet Converter (SEC) is a DIN-rail mounted (typically on the rear of the MICROLOK II cardfile) self-contained unit that interfaces a MICROLOK II CPU RS-232 serial com port to a wire Ethernet.

It provides Ethernet network connectivity to MICROLOK II units. The SEC converts the MICROLOK II Peer messages from the MICROLOK II serial ports to Ethernet data which is then available to other devices across an Ethernet network. The SEC thus enables the routing of MICROLOK II Peer messages using the TCP and UDP network protocols. Conversely, the SEC converts Ethernet signals to serial data for use by a MICROLOK II unit.

MICROLOK II serial data placed on the network is also available for central office applications enabling MICROLOK II units to communicate with central office applications that support the Peer protocol. The SEC can route Peer messages to any destination that implements the Peer protocol.

Opto-coupled data in and out lines isolate the network from the MICROLOK II cardfile.

Table 8-5. Serial to Ethernet Converter Interface/Indicators

FIGURE 8-5 REF	LABEL	DEVICE	PURPOSE
1	BATT 12VDC	Power Connection	Connection to system battery (12VDC).
2	ON/OFF	Power Switch	Two-position power rocker switch.
3	PWR	Power Indicator	Red LED power indicator.
4	FUSE	5 amp fuse	Input power line fuse.
5	COM (DTE)	DB-9 Connector	Serial connector to MICROLOK II CPU.
6	ETHERNET	RJ45 Connector	Ethernet connector to wire Ethernet (Digi).
7	IP ADDRESS	Label	Label for recording the unit's IP address.

The SEC functionally consists of the following:

- A serial protocol communication channel which translates between MICROLOK II RS-232 signals and Ethernet to allow MICROLOK II units to communicate with outside networks using Peer protocol.
- Power source circuitry which conditions a nominal 12-volt battery source to provide isolated power.
- An internal web server/interface that provides screens for configuring the SEC unit.

8.3 Code System Interface Board (CSIB)

CSIB – N17061401

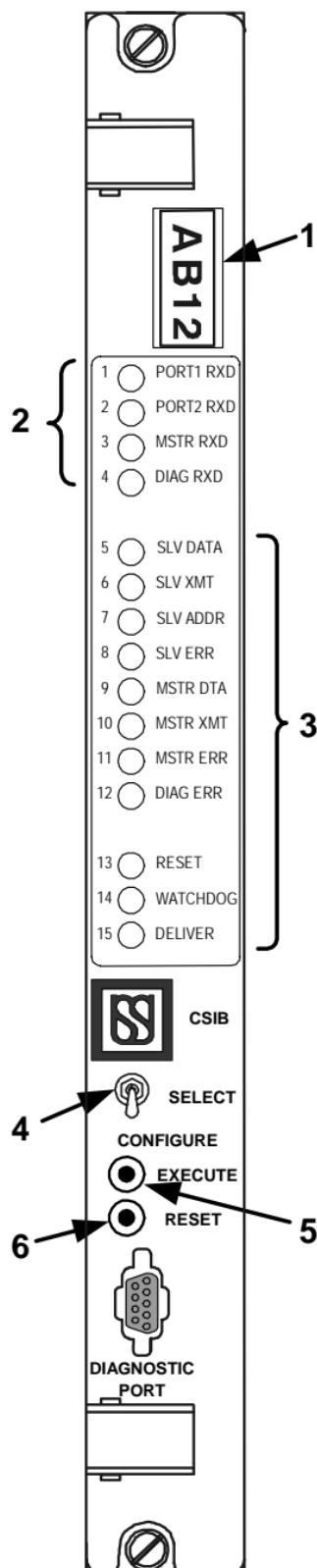


Figure 8-6.Code System Interface PCB - Front Panel Detail

Table 8-6.CSIB INDICATORS/CONTROLS

REF FIGURE 8-6	LABEL	DEVICE	PURPOSE
1	(none)	four-character alpha-numeric LED display	Displays on-unit configuration menu and options.
2	1 PORT 1 RXD	red LED	Flashes when serial port 1 is receiving data. Otherwise, this LED is off.
	2 PORT 2 RXD	red LED	Flashes when serial port 2 is receiving data. Otherwise, this LED is off.
	3 MSTR RXD	red LED	Flashes when the Master port is receiving data from the Slave unit. Otherwise, this LED is off.
	4 DIAG RXD	red LED	Flashes when the diagnostic port is receiving data from the connected laptop computer. Otherwise, this LED is off.
3	5 SLV DATA	red LED	50 millisecond flash when the Slave port receives good data. Otherwise, this LED is off.
	6 SLV XMT	red LED	Flashes on when the Slave port transmits good data. Otherwise, this LED is off.
	7 SLV ADDR	red LED	50 millisecond flash when the Master unit correctly addresses the Slave port. Otherwise, this LED is off.
	8 SLV ERR	red LED	This LED is on steady when the Slave port receives bad data from the Master unit. This LED goes out when the Slave port receives good data.
	9 MSTR DTA	red LED	50 millisecond flash when the Master port receives good data. Otherwise, this LED is off.
	10 MSTR XMT	red LED	Flashes on when the Master port transmits good data. Otherwise, this LED is off.
	11 MSTR ERR	red LED	This LED is on steady when the Master port receives bad data from the Slave unit. This LED goes out when the Master port receives good data.
	12 DIAG ERR	red LED	This LED is on steady when the diagnostic port receives bad data from the laptop computer. This LED goes out when the diagnostic port receives good data.

REF FIGURE 8-6	LABEL	DEVICE	PURPOSE
	13 RESET	red LED	When lit, indicates that the CPU is in the reset mode.
	14 WATCHDOG	red LED	Flashes at a 2Hz rate when the PCB is functioning properly.
	15 DELIVER	red LED	Flashes when delivering outputs to GENISYS or Microlok-Plus output PCBs.
4	SELECT	2-pos. toggle switch (return-to-center type - shown toggled)	Used to select on-unit configuration items from menu as shown on four-character alphanumeric display.
5	EXECUTE	Momentary pushbutton.	Used to enter configuration item selected with SELECT toggle switch.
6	RESET	Momentary pushbutton.	Used to reset the code system interface PCB.

The code system interface PCB interfaces the MICROLOK II system to various types of non-vital code lines. Basic functions include conversion of the particular code line protocol to a format compatible with the MICROLOK II system (GENISYS Master) and operation as a non-vital logic controller. This PCB is electrically identical to the enhanced controller PCB used in the ASTS USA GENISYS-2000 systems, and uses executive and application software that is identical to that used on the enhanced controller PCB. The GENISYS-2000 hardware is modified to make the PCB mechanically compatible with the MICROLOK II cardfile.

The basic interfacing rules for the code system interface PCB are as follows:

1. This PCB must be used when interfacing the MICROLOK II system to all types of non-vital code systems except GENISYS. Either the code system interface PCB or the MICROLOK II CPU PCB can be used for the GENISYS interface.
2. When interfacing the MICROLOK II system to a DC code line, an external GENISYS unit must be included to provide the electrical interface to the code line. The MICROLOK II system does not include an equivalent to the GENISYS code line interface PCB.
3. MICROLOK II serial link isolator units should be included in the interface to the code line to protect circuits on both ends of the interface from potentially damaging voltage transients. These units are different from the GENISYS surge suppression/serial interface panels. The latter cannot be used as a substitute. Serial link isolator unit specifications are listed in Table 8-7.

Table 8-7. Serial Link Isolator Specifications

UNIT TYPE	ASTS USA PART NO.	UNIT SPECIFICATIONS
Type A serial link isolator unit	N17002201	<p>Interfaces the code system PCB (cardfile) to a Glenaire modem or MCP in ARES and serial line carrier code systems.</p> <p>Input Power: 9.5 to 16.2VDC</p> <p>Modem Power Outputs: +12VDC and -12VDC</p>
Type B serial link isolator unit	(Contact ASTS USA)	<p>Interfaces the code system interface PCB to ATCS systems.</p> <p>Signal compatibility: Balanced RS-485 and unbalanced RS-423 ports</p>

Figure 8-7 shows the standard interface wiring pin-outs for the code system interface PCB.

The CSIB PCB is a 1 ¼ width PCB and as such is best placed at the extreme right-hand side of the MICROLOK II cardfile, once the small filler strip is removed.

48-pin Connector	Pin No.	
	C2	Slave Receive Data “-” (S1RXD-)
	C4	Slave Receive Data “+” (S1RXD+)
	C6	Slave Receive Clock “-” (S1RXC-)
	C8	Slave Receive Clock “+” (S1RXC+)
	C10	Slave Transmit Clock “-” (S1TXC-)
	A10	Slave Transmit Clock “+” (S1TXC+)
	C14	Slave 2 Receive Clock (S2RXC)
	C16	Slave Data Carrier Detect (S2DCD)
	C18	Slave Receive Data “-” (S2RXD-)
To Serial or ATCS-compliant Code System via Serial Link Isolator Unit	A2	Slave Clear To Send “-” (S1CTS-)
	A4	Slave Clear To Send “+” (S1CTS+)
	A6	Slave Data Carrier Detect “-” (S1DCD-)
	A8	Slave Data Carrier Detect “+” (S1DCD+)
	E2	Slave Transmit Data (S1TXD)
	E4	Slave Transmit Clock (S1TXC) (Output)
	E6	Slave Request To Send (S1RTS)
	E8	Slave Data Terminal Ready (S1DTR)
	E10	0 Volts
	E12	Slave 2 Common (0 Volts)
	E14	Slave Transmit Data (S2TXD) (In / Out)
	E16	Slave Transmit Clock (S2TXC)
	E18	Slave Request To Send (S2RTS)
	E20	Slave Data Terminal Ready (S2DTR)
	E22	+ 5 Volts
	E32	0 Volts
	C12	0 Volts
	C20	+ 12 Volts
	C22	+ 5 Volts
	C28	- 12 Volts
	C32	0 Volts
	A20	+ 12 Volts
	A22	Master Receive Data (MRXD)
	A24	Master Data Carrier Detect (MDCD)
	A28	- 12 Volts
	A30	0 Volts
	A32	Master Common - 0 Volts
	A12	Slave Common - 0 Volts (S1COM)
	A14	Master Transmit Data (MTXD)
	A16	Master Request To Send (MRTS)
	A18	Master Data Terminal Ready (MDTR)
To DC Code Lines (US&S 500 Series or GRS K Series)	E24	Parallel Output 1 (POUT1)
Refer to SM-6700B for Application Data	C24	Parallel Output 2 (POUT2)
	C26	Parallel Output 3 (POUT3)
	A26	Parallel Output 4 (POUT4)
	E26	Parallel Input 1 (PIN1)
	E28	Parallel Input 2 (PIN2)
	E30	Parallel Input 3 (PIN3)
	C30	Parallel Input 4 (PIN4)

Code System Interface PCB N17061401

**Figure 8-7.Code System Interface PCB - Basic Interface
Wiring**

8.4 Serial Link Isolation

Isolation between serial signal commons is necessary when serially connecting MICROLOK II units that are powered by different batteries.

NOTE

Care must be exercised to insure that devices that ARE serially connected directly to a MICROLOK II unit DO NOT have serial connections to devices that might ground serial common.

Application engineers should note that the serial commons for all MICROLOK II serial ports are connected directly to negative vital battery AND to each other. This means that anything connected to any serial port signal common is also connected to negative vital battery. Furthermore, anything connected to the serial common of any equipment that is directly connected to any MICROLOK II serial port is connected to negative vital battery through MICROLOK II. This imposes serious restrictions on the characteristics of the devices that can be DIRECTLY CONNECTED to the MICROLOK II serial ports. It should be noted, for example, that most commercial data modems connect their serial common to earth ground in some way, either directly or through a low resistance. It should also be noted that most data radios connect their serial common directly to their antenna ground. Both of these conditions create a problem since they introduce a connection between negative vital battery and earth ground.

As these battery power supplies are considered vital and are required to float with respect to ground, significant potential differences can develop between the battery negatives. These potential differences can end up being equalized by the connection between serial commons.

This situation poses a threat both to communication circuit reliability and the electrical integrity of the connected MICROLOK II units. In addition, interconnection of battery commons by any means is not a recommended practice.

This situation is remedied by introducing a serial line isolator in the serial line between the MICROLOK II units (See Figure 8-9). This unit provides a high level of isolation between the signal commons of MICROLOK II and serial devices such as modems and data radios.

The RS-232 link from the MICROLOK II CPU Com Port passes through an ASTS USA serial isolator before going to the modem. This ensures there will be no grounding problems between interconnected MICROLOK II units.

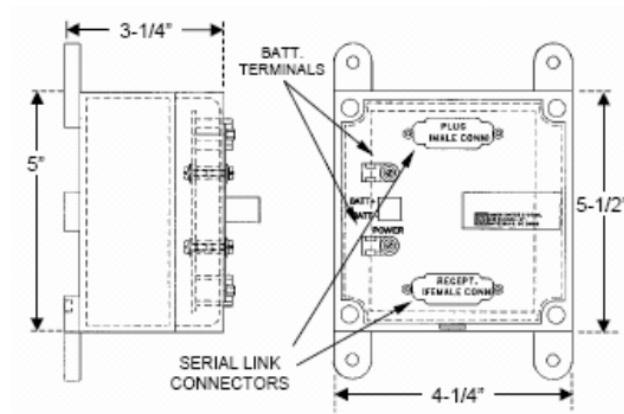


Figure 8-8.Serial Link Isolator

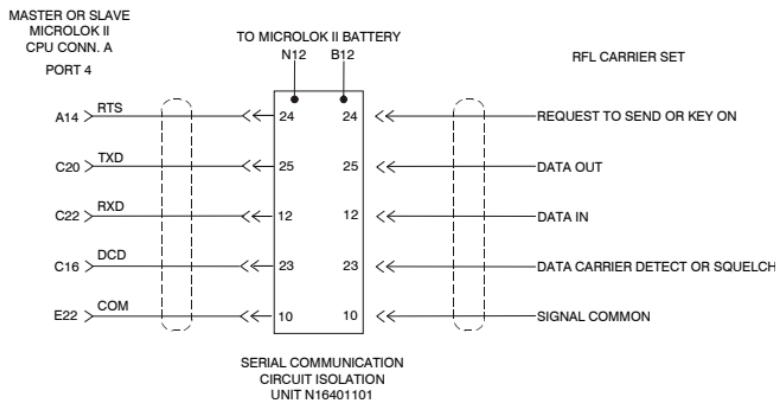


Figure 8-9.Typical RS-232 Port 4 with Serial Isolator
(MICROLOK or GENISYS® Protocol)

8.5 Serial Communications Adapter Panel

This panel converts the EIA-level signals at both ends of the link to a 20mA current loop level. This protects the serial channels from voltage transients. A single, standoff-mounted printed circuit board on the panel contains the EIA/current loop conversion circuitry. User devices include a power on/off switch, a fuse assembly, power status lamps, and communications status lamps for the current loop half of the interface (See Figure 8-11 and Figure 8-12).

8.5.1 Interface Wiring

Figure 8-10 shows a typical 20 milliamp current loop interface between master and slave MICROLOK II systems using the serial communications adapter panel. Transmit Data, Request-to-Send, Data Carrier Detect, and Receive Data are each placed in a twisted pair with a separate ground wire. This is done to improve noise immunity from external sources and eliminate possible cross talk between lines.

The current loop cable assembly is cut to length per the application and fitted with connectors. Cable specifications are listed in Table 8-8.

Table 8-8. Current Loop Interface Cable Specifications

MAXIMUM CABLE LENGTH	MAXIMUM TOTAL CABLE PATH LENGTH	NOMINAL CABLE WIRE GAUGE/TYPE	MINIMUM CABLE WIRE GAUGE/TYPE	WIRE CAPACITANCE	WIRE RESISTANCE
5,000 ft.	10,000 ft.	#19 AWG twisted pair	#24 AWG twisted pair	0.09 mF/1000 ft.	30 ohms/mile

The 20-milliamp current loop cable should be run below ground where it runs outside of the equipment house or case to minimize possible lightning damage. The shield wire at the end of the cable should be grounded using one of the 25-pin "D" connector attachment screws on the interface panel. Also, a rack ground wire should be run from the panel's **EARTH GROUND** dual fasten terminal to the equipment rack prime ground bus. Keep this wire as short as possible and minimize the number of bends. Make certain that both ends of the serial link have both shield and rack ground connections as shown in Figure 8-10. The current loop cable should also be provided strain relief by securing it to the rack frame with wire tie straps.

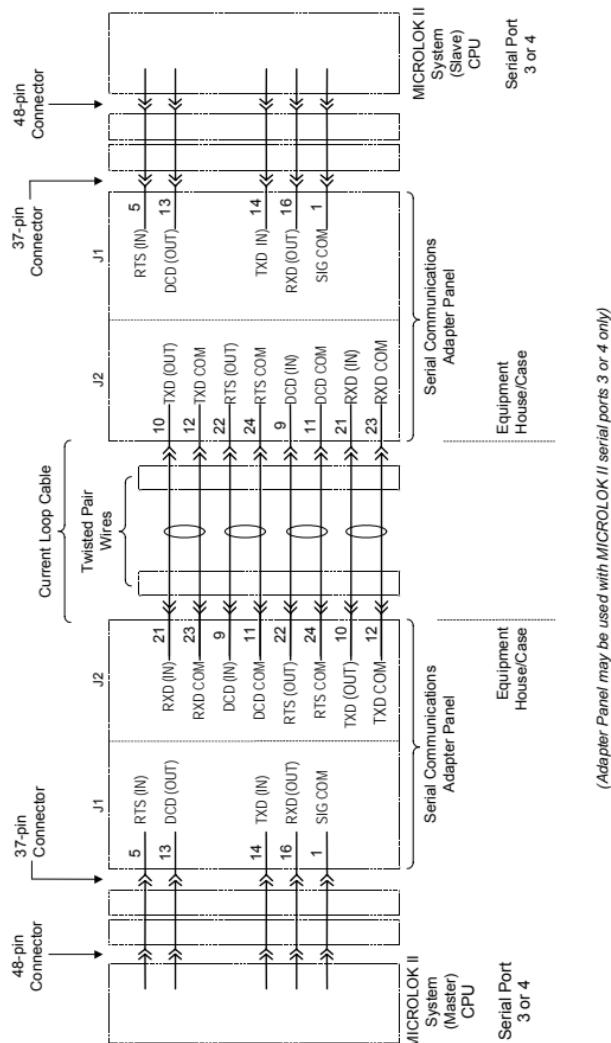


Figure 8-10.Typical Adapter Application - Master and Slave MICROLOK II Systems

8.5.1.1 Input Connector

This is a 37D-type connector (J1), which is used for field wiring. There are pins for four RS-232 signals – TXD, RXD, DCD, and RTS plus pins for signal common.

TXD – J1 - 14, 33
 RTS – J1 - 5, 24
 RXD – J1 - 16, 35
 DCD – J1 - 11, 13, 30, 32

8.5.1.2 Current Loop Connector

This is a 25D-type connector (J2), which is used for field wiring. It is the Current Loop connections between the two panels. There are also pins for four RS-232 signals – TXD, RXD, DCD and RTS plus pins for signal common.

TXD – J2 - 8, 10 and 12, 13
 RTS – J2 - 20, 22 and 24, 25
 RXD – J2 - 19, 23 and 17, 21
 DCD – J2 - 7, 11 and 5, 9



Figure 8-11. Serial Communications Adapter Front Panel Detail

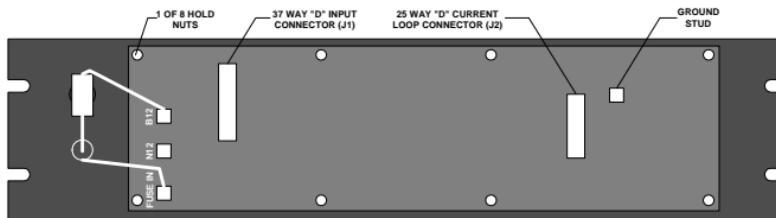


Figure 8-12. Serial Communications Adapter Rear Panel Detail

9 COMMUNICATION PROTOCOL

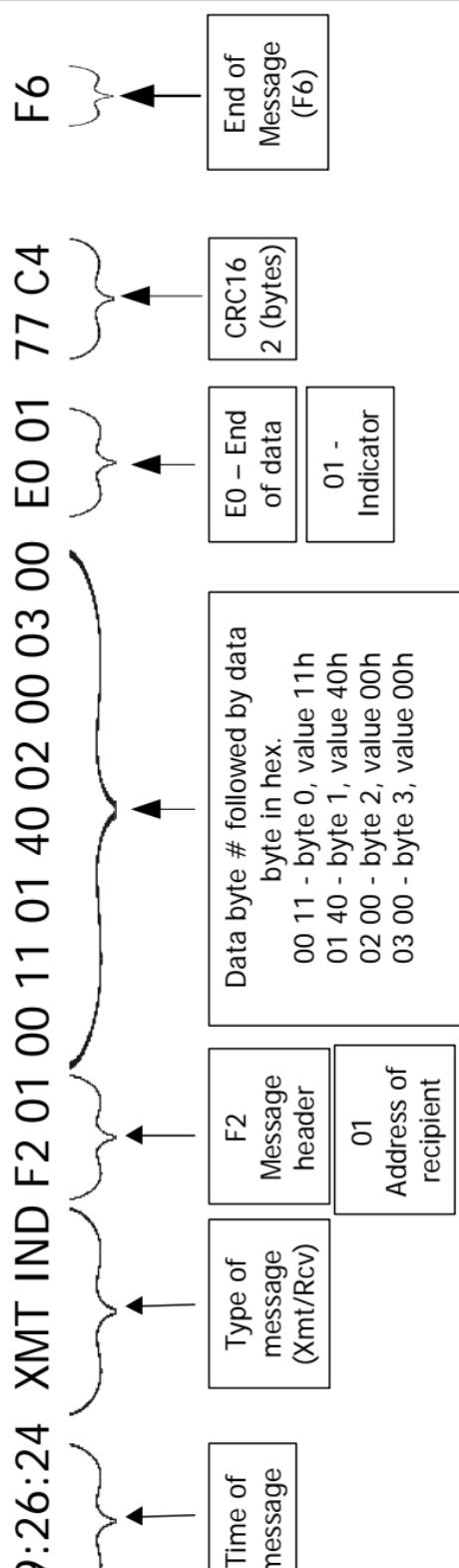


Figure 9-1.GENISYS Protocol

See Figure 9-1, Figure 9-2, and Figure 9-3 for a breakdown of the respective serial protocol messages.

9.1 GENISYS Protocol

The GENISYS protocol is a binary, byte oriented, serial polling protocol in which all messages are framed by unique header/control and terminator bytes. It is normally transmitted and received by asynchronous serial communication controllers configured to process eight bit characters with one start bit and one stop bit.

The GENISYS message is composed of a header/control character, a station address, data bytes (optional), two checksum bytes, and a terminator byte.

NOTE

In the following paragraphs character (byte) values preceded by "\$" are hexadecimal values.

There are thirteen possible header/control characters (bytes) in the GENISYS protocol (\$F1 - \$FE). Character \$F0 is reserved for use as an "escape" character, \$F6 is reserved for uses as a message terminator, and \$FF is not used. Headers \$F1 - \$F3 are assigned to slave to master message while header \$F9 - \$FE are assigned to master to slave messages.

NOTE

GENISYS protocol reads the binary right-to-left, with the least significant bit in the right position.

Refer to Figure 9-1. The first data byte "00" has a hex value of "11" and second data byte "01" has a value of "40". Converting this hex # to binary reveals the individual bit values.

Therefore "11" is equal to:

0001 0001 Flipping this in order to orient this to the bit list in the serial section of the software it can be seen that the 1st and the 5th bit are high = 10001000. This is directly related to the bit list in the application program.

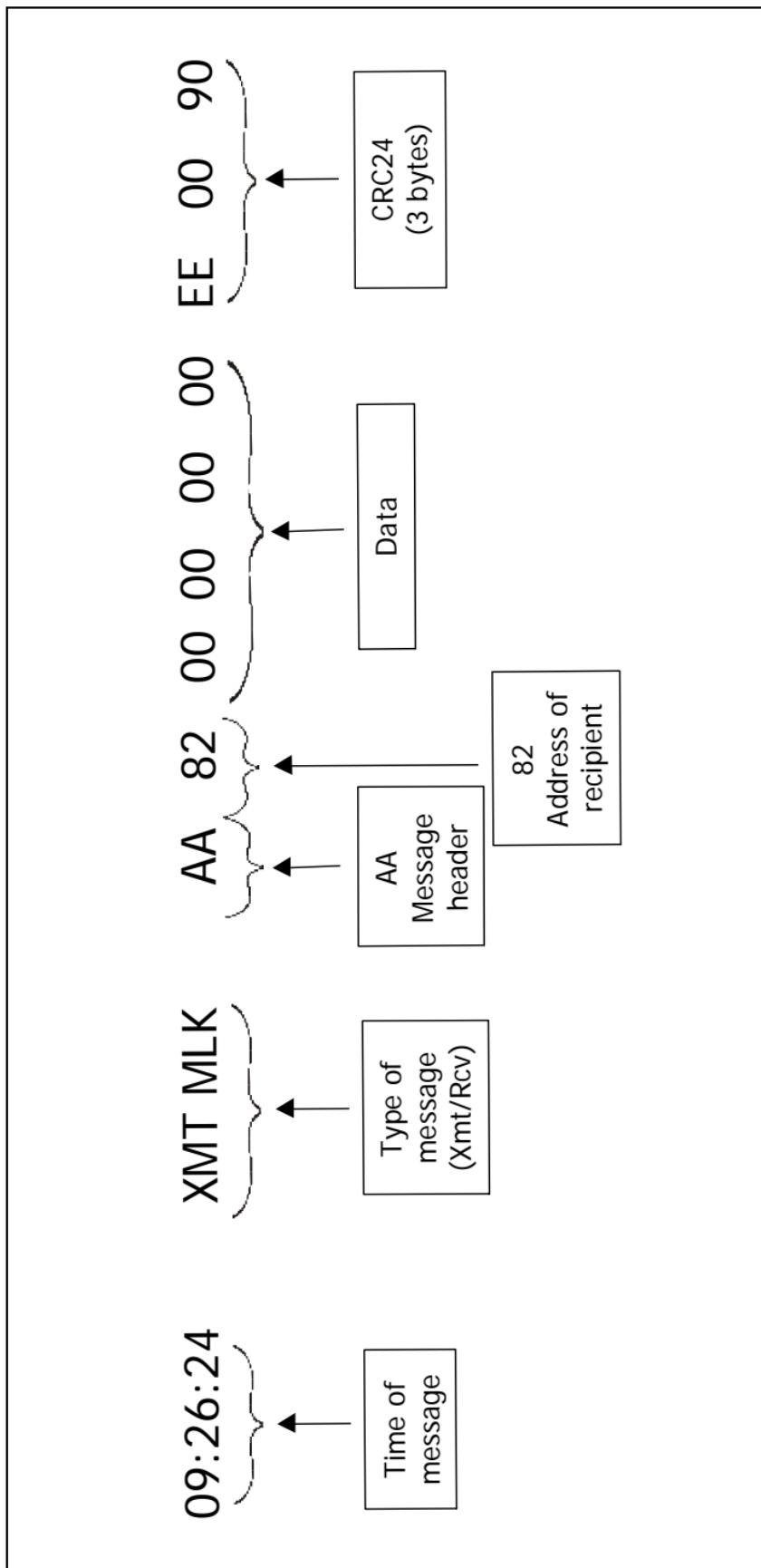


Figure 9-2. MICROLOK Protocol

NOTE: Data is read left to right, same as the F/A sheet. (88 = 10001000)

9.2 MICROLOK Protocol

The MICROLOK protocol is significantly different than that of the GENISYS.

Refer to Figure 9-2. The header byte is the same transmit or receive "AA." The "01" is the slave address and the "81" is from the Master end. The "8" is attached to the "1," if the master recognizes the last data message. If it does not it will transmit "01," the same as the slave.

The data bytes are not identified by their byte #, only the data is shown.

NOTE

MICROLOK protocol reads the binary right-to-left, with the least significant bit in the left position.

The data is read opposite that of the GENISYS protocol. If the first data byte is "88," converting this hex # to binary allows the individual bit values to be read as follows:

"88" is equal to:

1000 1000 This shows that the 1st and the 5th bit are high = 10001000

There are three "CRC" bytes as opposed to two in the GENISYS protocol.

There is no end of message byte.

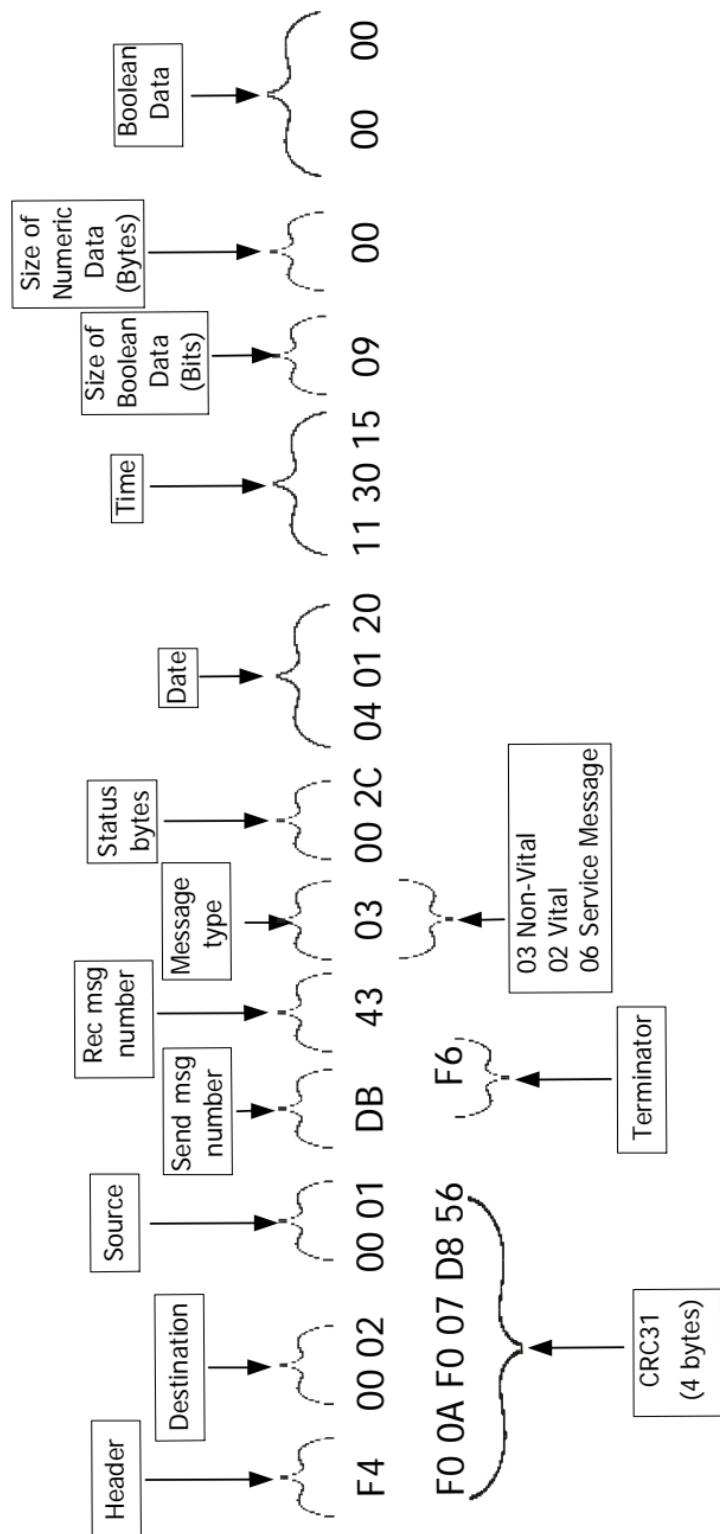


Figure 9-3.Peer-to-Peer Protocol

NOTE: Date and time fields are optional. The default is OFF. Also, F0 0A compresses to FA and F0 07 to F7 for the CRC.

9.3 PEER Protocol

The Peer protocol is significantly different than that of the GENISYS or MICROLOK. This protocol is available in ASTS USA MICROLOK II Executive, beginning with Revision 7.0.

Refer to Figure 9-3. The header byte is always an "F4" followed by a packet header. The packet header contains the information from/to and date/time a counter for the send and receive messages and message status. The next two bytes ID the number of Boolean bits and numeric data bits. Data follows with a four-byte CRC packet. The end byte always terminates the message with "F6." As with MICROLOK the data byte number is not included with the data.

When the data is converted from hex to binary it is read the same as GENISYS.

NOTE

Peer protocol reads the binary right-to-left, with the least significant bit in the right position.

Therefore "11" is equal too:

0001 0001 Flipping this in order to orient this to the bit list in the serial section of the software it can be seen that the 1st and the 5th bit are high = 10001000.

NOTE

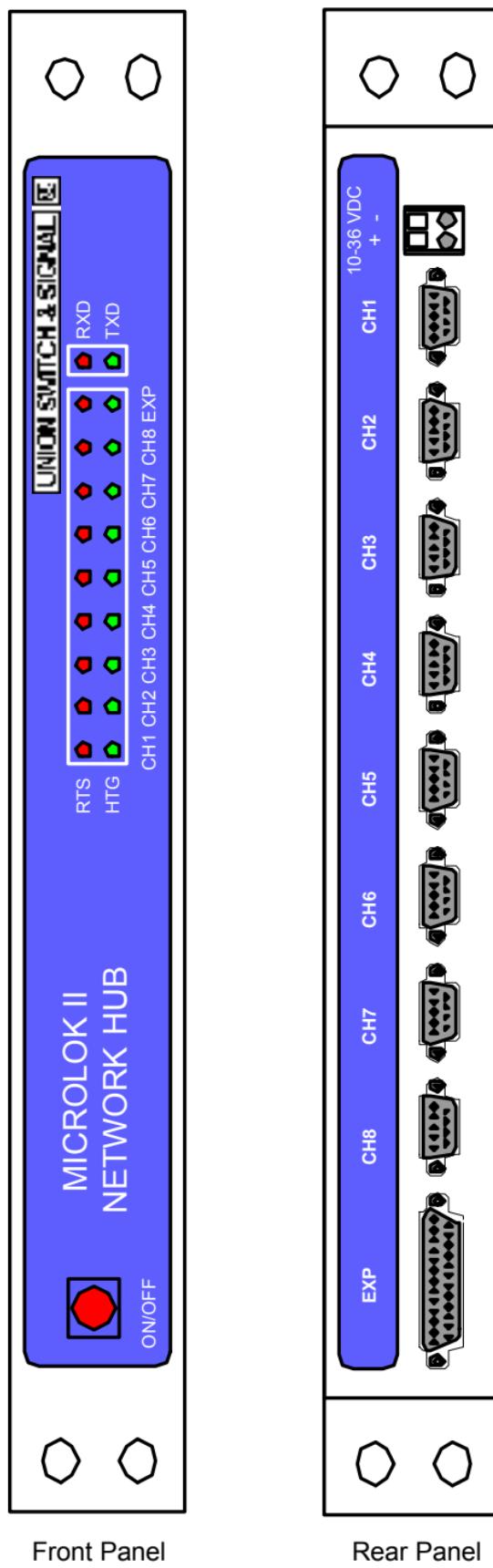
There is a cable wiring change, from that used in MICROLOK protocol, to use PEER protocol.

Table 9-1.MII.PEER Configuration Parameters

(All times are in milliseconds.)

CONFIG ITEM	DE-FAULT VALUE	RESOLUTION	MIN VALUE	MAX VALUE	RE-QUIRED
Link Enable Bit	None	1	0	1	Yes
Point.Point	1	1	0	1	No
Baud	19200	Tabled – 300,600,1200,2400,4800,9600, 19200,38400			No
Stopbits	1	1	1	2	No
Parity	None	None, Even, Odd, Mark, Space			No
Key.On.Delay	0	1	0	280	No
Key.Off.Delay	12	1	0	280	No
Grant.Delay	1000	1	10	10,000	No

10 MICROLOK II NETWORK HUB



Front Panel

Rear Panel

Figure 10-1.Network Hub

The Network Hub (ASTS USA Part Number - N16906701) allows up to eight co-located MICROLOK II units to connect to it and communicate through it. Each of the eight supported channels is configurable to be compatible with each of the serial communications standards available on MICROLOK II CPU PCBs, either RS-232, RS-423, or RS-485. The Hub services a single request from one of the possible eight MICROLOK II units connected to it and broadcasts it to the other channels simultaneously.

The Hub also includes a single expansion port that will allow two Hubs to be interconnected to allow up to 16 co-located MICROLOK II units to communicate using the MICROLOK II Network protocol. When an expansion Hub is connected, the first Hub will service a request from one of the eight possible MICROLOK II units connected to it or the expansion Hub. The first Hub will then broadcast the message to each of the remaining channels connected to it and to all channels connected to the expansion Hub, when the expansion Hub grants it access.

The expansion port is a custom port that accommodates the necessary handshake signals between two connected Hubs.

Each channel on the Hub is comprised of drivers and receivers based on the RS-423 standard.

Table 10-1.Signal/Pin Assignments for DB-9 Connectors

PIN NO.	SIGNAL
1	Hub Transmit Grant (HTG) (Output)
2	Receive Data (RXD) (Output)
3	Transmit Data- (TXD-) (Input)
4	Transmit Data+ (TXD+) (Input)
5	Signal Common
6	Request to Send+ (RTS+) (Input)
7	Request to Send- (RTS-) (Input)
8	Signal Common
9	Signal Common

Table 10-2. MICROLOK II to Hub Connections

MICROLOK II (HARTING) CPU CONNECTOR					HUB (DB-9)	
PORT 1 PIN	PORT 2 PIN	PORT 3 PIN	PORT 4 PIN	SIGNAL	PIN NO.	SIGNAL
A2	A16	E16	C20	TXD- (Output)	3	TXD- (Input)
A4	A18	NC	NC	TXD+ (Output)	4	TXD+ (Input)
C6	A24	E14	C22	RXD- (Output)	2	RXD (Output)
C8	A26	NC	NC	RXD+	8	Signal Common
E2	A20	C14	A14	RTS- (Output)	7	RTS- (Input)
E4	A22	NC	NC	RTS+ (Output)	6	RTS+ (Input)
C10	A28	E10	C16	DCD- (Input)	1	HTG (Output)
C12	A30	NC	NC	RTS+ (Output))	9	Signal Common
NC	NC	E18	NC	RXREF	9	Signal Common
C18	C18	E22	E22	Signal Common	5	Signal Common

**Table 10-3.Signal/Pin Assignments for Expansion Port
(DB-25 Connector)**

PIN NO.	SIGNAL	TO	PIN NO.	SIGNAL
1	Signal Common		1	Signal Common
2	Transmit Data (Output)		3	Receive Data (Input)
3	Receive Data (Input)		2	Transmit Data (Output)
4	Service Request (Output)		8	Service Request (Input)
5	Reserved		5	Reserved
6	Service Grant (Output)		20	Expansion Present (Input)
7	Signal Common		7	Signal Common
8	Service Request (Input)		4	Service Request (Output)
9	NC		9	NC
10	NC		10	NC
11	NC		11	NC
12	NC		12	NC
13	NC		13	NC
14	NC		14	NC
15	NC		15	NC
16	NC		16	NC
17	NC		17	NC
18	Expansion Present (Output)		21	Expansion Present (Input)
19	NC		19	NC
20	Service Grant (Input)		6	Service Grant (Output)
21	Expansion Present (Input)		18	Expansion Present (Output)
22	Reserved		22	Reserved
23	NC		23	NC
24	Signal Common		24	Signal Common
25	Signal Common		25	Signal Common

10.1 Cable Recommendations

Cables from a MICROLOK II unit, a MICROLOK II network Hub, or a MICROLOK II NIA should not be run outside of the house. If the cables do need to be run outside of the house, a modem should be used.

MICROLOK II Serial Ports 1 and 2 are RS-485 ports. Each RS-485 port signal is transported by a twisted pair of wires labeled as "XXX-" and "XXX+" (TXD- and TXD+, for example). In addition, the signal COMMONs for all ports on an RS-485 communication link must be connected together to equalize the potential between signal commons for the connected units. Note that signal COMMON cannot be connected to a frame or earth ground as it is directly connected through the MICROLOK II power supply to negative vital battery. RS-485 ports should be

interconnected using ONLY twisted pair cable with an over-all shield. For best performance, the interconnecting cables should not contain extra, unused pairs. Any unused pairs should be connected together at both ends of the cable and connected to signal COMMON for best noise immunity. If connected, the shield should be connected to a frame ground at one end of the cable only.

MICROLOK II units require that a 120-ohm, ½-watt, external load resistor be placed across the TXD and RTS transmitters and across the RXD and DCD receivers when using the RS-485 ports. However, when the MICROLOK II RS-485 port is connected to a MICROLOK II Network Hub no external resistors are required on the Hub end, and on the MICROLOK II end they are only required for the TXD and RTS outputs. Note that the DIP switches inside the Hub switch in the proper termination for that end of the link.

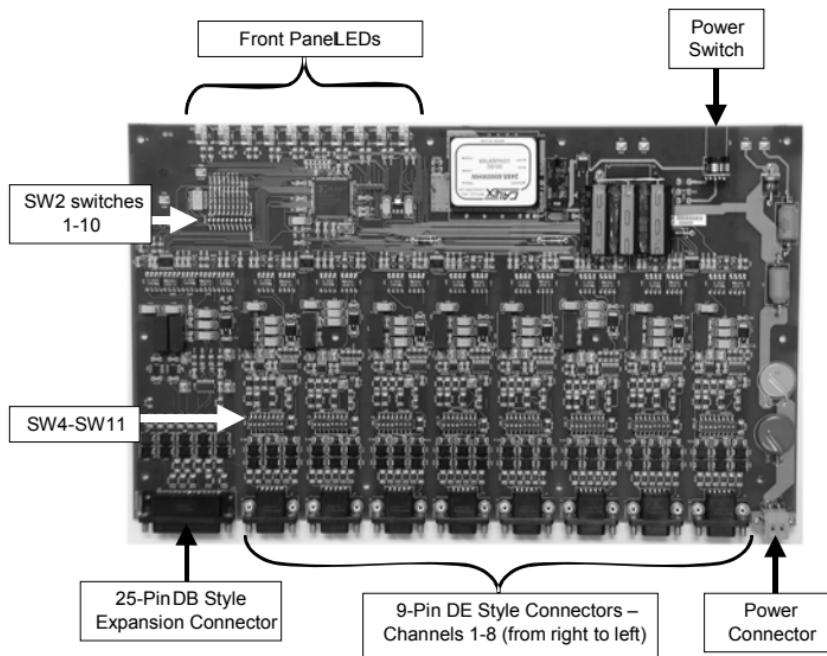


Figure 10-2.Hub PCB Layout

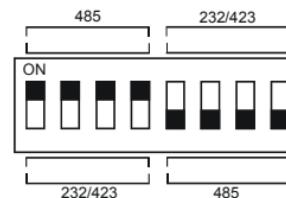


Figure 10-3.Hub SW4 – SW11

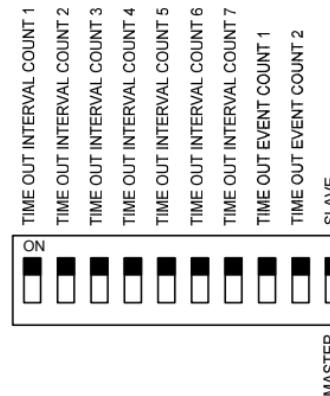


Figure 10-4.Hub SW2

The Hub delay switch SW2 (switches 1 through 7 – time out interval count) sets the length of transmission time in 25-millisecond intervals for a port with RTS asserted (high). Switches 8 and 9 (time out event count) set the number of times the system will allow the transmission to time out before declaring the port invalid. This is done to prevent a failed unit with RTS stuck high from dominating the network. Once a port is declared invalid the Hub will not provide a Grant signal until the port RTS goes low.

Switch 10 (Master/Slave) is used when multiple Hubs are interconnected. A one-Hub system has the switch set in the Master position. Another Hub connected to the same system has its switch set to Slave.

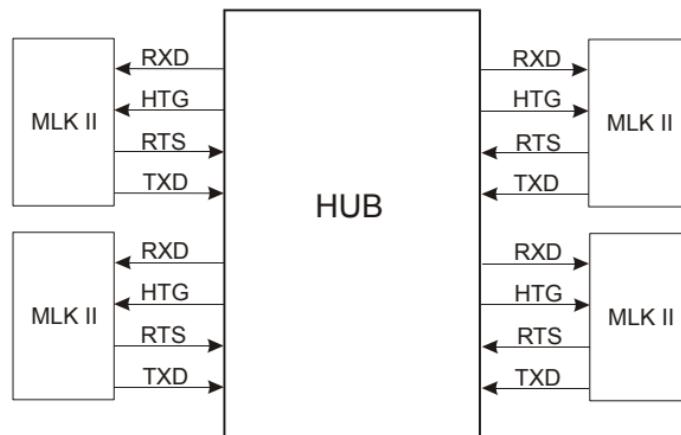


Figure 10-5.Local Hub Network

(No Connection to External Network - Typical Interface)

11 NETWORK INTERFACE ADAPTER

The NIA forms the link between an external network and the Hub, or between an external network and a separate MICROLOK II unit. It accepts a message and transports it on a TCP/IP based network. The NIA does non-vital protocol conversion to format messages as required, inserting the entire MICROLOK II Network Protocol message into the data field of the TCP/IP message. The NIA handles all issues, both hardware and software, relating to the network interface. It does not modify the content of the MICROLOK II message in any way. The messages are passed intact from end to end allowing for both vital and non-vital data processing within the MICROLOK II units.

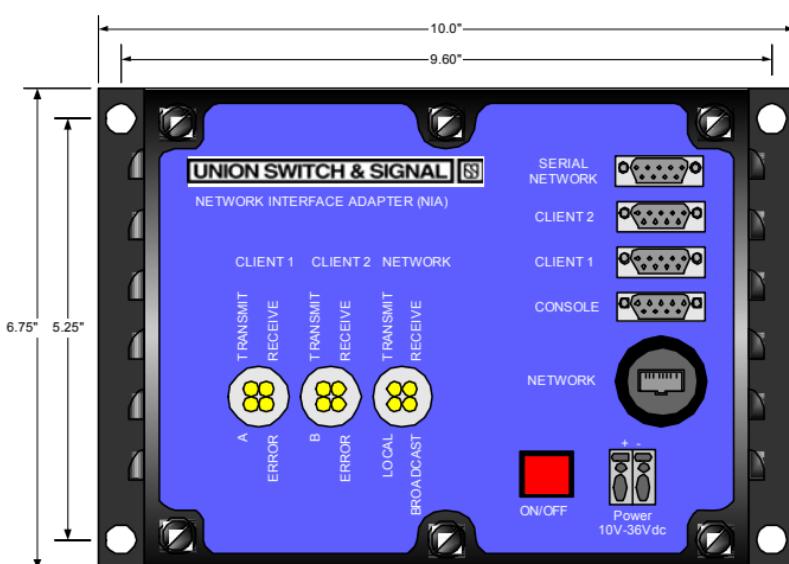


Figure 11-1.NIA Front Panel

11.1 Serial Cable Connections

The NIA is connected to the Hub or a MICROLOK II unit using a 9-pin DB style connector with a plastic shell. The DB-9 connector is connected to the CLIENT 1 port.

11.2 Communicating with the NIA

The initial default IP address of the NIA is 192.168.1.10. During configuration a new default address is set and recorded in flash memory, which then becomes the new default address.

Table 11-1.NIA LED Indicators

LED REFER TO FIGURE 11-1	OPERATION
CLIENT1 TRANSMIT	This LED indicates that a message is ready to send and a Request to Send (RTS) signal has been sent. It is on when the RTS signal is set, and goes off when the RTS signal is cleared.
CLIENT1 RECEIVE	This LED indicates that a message is being received. It is on while the message is being received, and turns off when the message has been received, or a byte has not been received within one second.
CLIENT1 A	This LED is on when the NIA's grant timer has expired before the NIA has finished transmitting its message to the Hub, and the Hub Transmit Grant (HTG) signal is set. This LED is cleared when the RTS signal is cleared.
CLIENT1 ERROR	This LED is on whenever an error is detected reading a message and clears when the message has been received, or a byte has not been received within one second.
CLIENT2 TRANSMIT	This LED indicates that a message is ready to send and a Request to Send (RTS) signal has been sent. It is on when the RTS signal is set, and goes off when the RTS signal is cleared.
CLIENT2 RECEIVE	This LED indicates that a message is being received. It is on, only while a message is being received. It is off when no messages are being received or a byte has not been received within one second.
CLIENT2 B	This LED is on when the NIA's grant timer has expired before the NIA has finished transmitting its message to the Hub, and the Hub Transmit Grant (HTG) signal is set. This LED is cleared when the RTS signal is cleared.
CLIENT2 ERROR	This LED is on whenever an error is detected reading a message, and clears when the message has been received or a byte has not been received within one second.
NETWORK TRANSMIT	This LED is on only when the last message was transmitted over the network. It is off when the last message was transmitted to a MICROLOK II unit attached to the same Hub, or a byte has not been read from the serial port within one second.
NETWORK RECEIVE	This LED is on when a message is received from the network, and is being passed along to the serial connection. This LED is cleared when the serial connection's RTS signal is cleared.
NETWORK BROADCAST	This LED is on only when the last message was broadcast over the network. It is off when the last message was not broadcast over the network or a byte hasn't been read within one second.
NETWORK LOCAL	This LED is on only when the last message was not sent over the network because the destination was on the same serial port as the source. This LED is off when the last message was sent over the network or a byte has not been read within one second.

Table 11-2.NIA to Hub Connections

NIA (DB-9)		HUB (DB-9)	
PIN NO.	SIGNAL	PIN NO.	SIGNAL
2	RXD (Input)	2	RXD (Output)
3	TXD (Output)	3	TXD (Input)
5	Signal Common	5	Signal Common
7	RTS (Output)	7	RTS (Input)
8	CTS (Input)	1	HTG (Output)

Table 11-3.NIA to MICROLOK II Connections

NIA (DB-9)		MICROLOK II (HARTING)		
PIN NO.	SIGNAL	PORT 3 PIN NO.	PORT 4 PIN NO.	SIGNAL
2	RXD (Input)	E16	C20	TXD (Output)
3	TXD (Output)	E14	C22	RXD (Input)
5	Signal Common	E22	E22	Signal Common
Jumper Pin 7, RTS (Output) to Pin 8, CTS (Input)		For Port 3, jumper Pin C14, RTS (Output) to Pin E10, DCD (Input) and jumper Pin E18, RXREF to E22, Signal Common For Port 4, jumper Pin A14, RTS (Output) to Pin C16, DCD (Input)		

Table 9-1 identifies the ranges, resolution, and default value for the link related parameters.

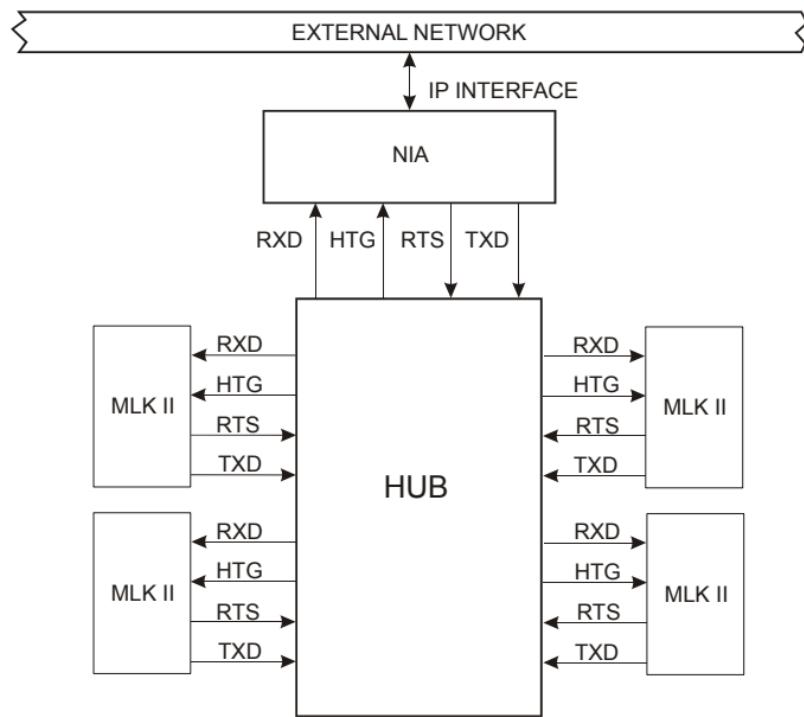


Figure 11-2.Local Hub Network

(Connection to External Network through NIA)

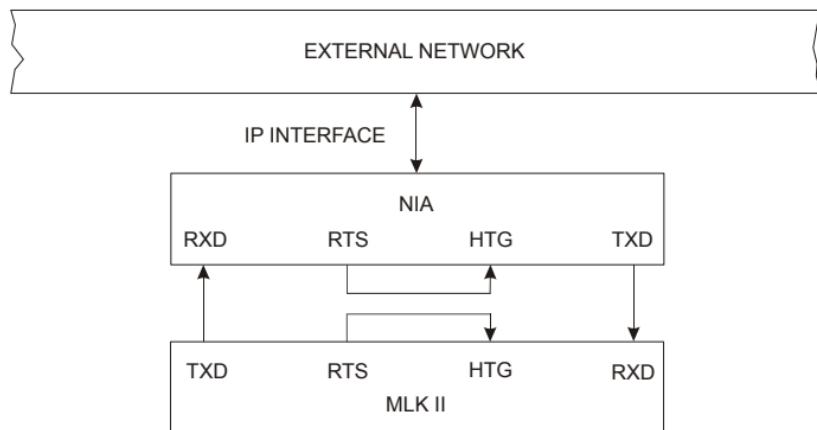


Figure 11-3.Connection to External Network

(Single MICROLOK II)

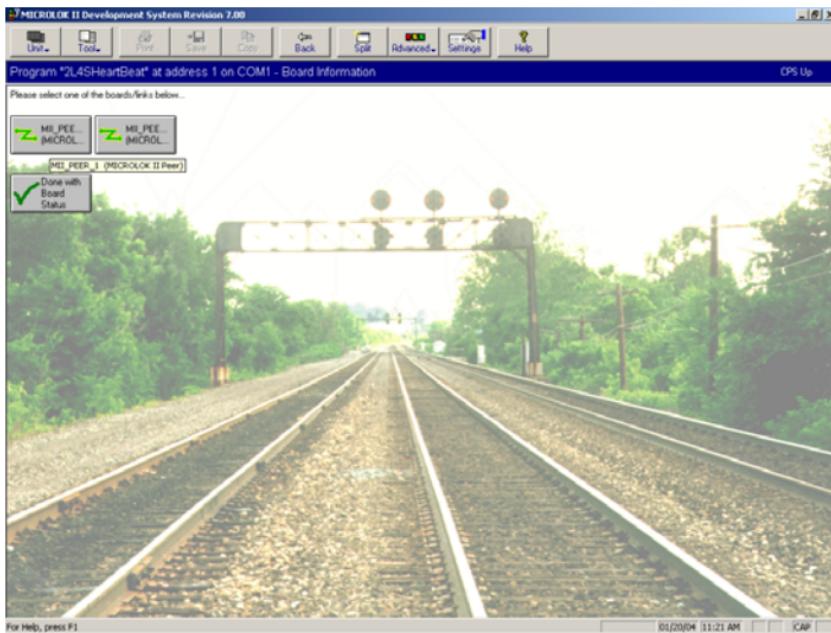


Figure 11-4. Board Information Screen

This view displays statistical information for both boards and protocol links.

Figure 11-4 shows two MICROLOK II Network Protocol links. The first link is called MII_PEER_1, and the second link is called MII_PEER_2. These are user defined link names in the application program. As shown in the figure, a tooltip is shown when the cursor hovers above a button. To enter the Link Information view for a particular link, simply click on the appropriate button.

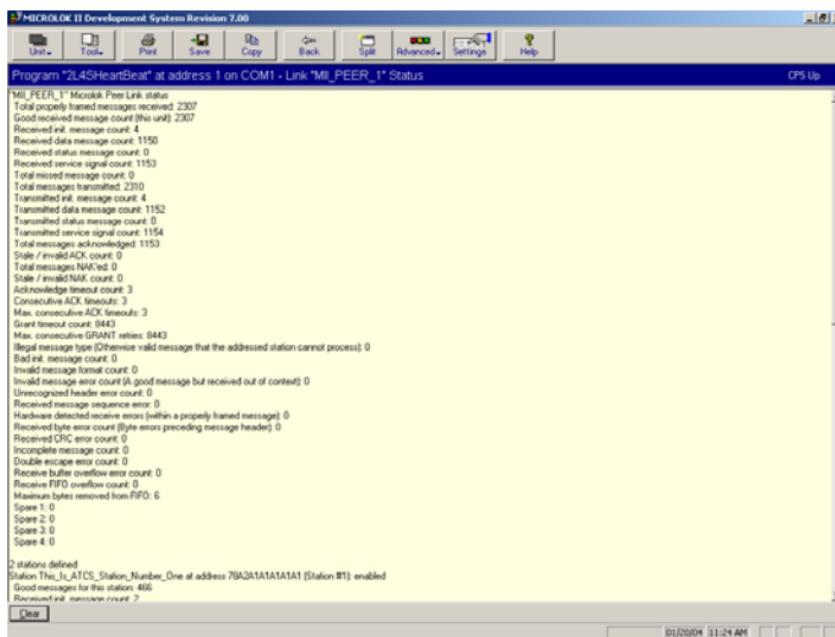


Figure 11-5.Protocol Link Statistics

The first section in Figure 11-5 displays the statistics for the main protocol link.

The next sections display the station statistics. In this particular screen, there are two stations defined. Scrolling down the screen will bring the station statistical information into view.

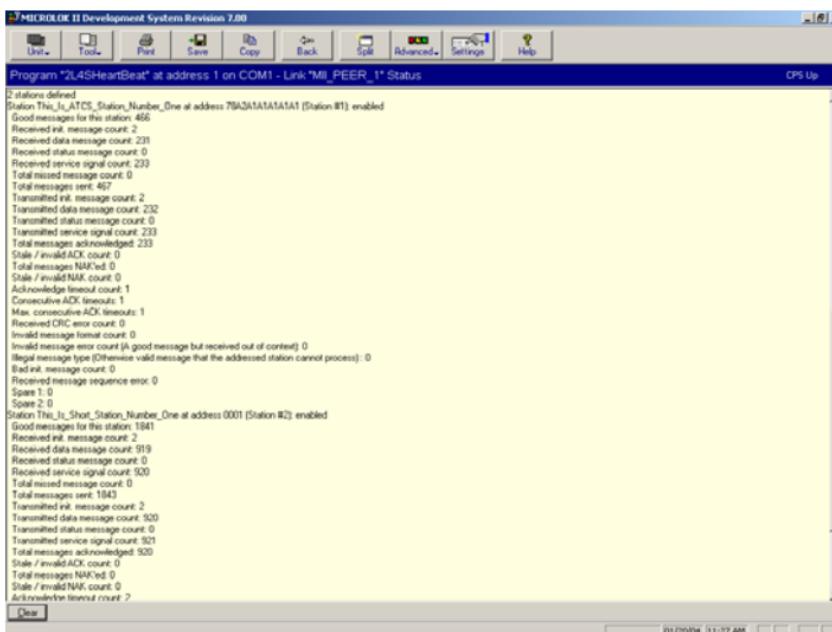


Figure 11-6.Station Statistics

Figure 11-6 displays the station statistics, which include the number of stations on the protocol link, each station name, station address, whether the station is enabled or not, and the station's statistics.

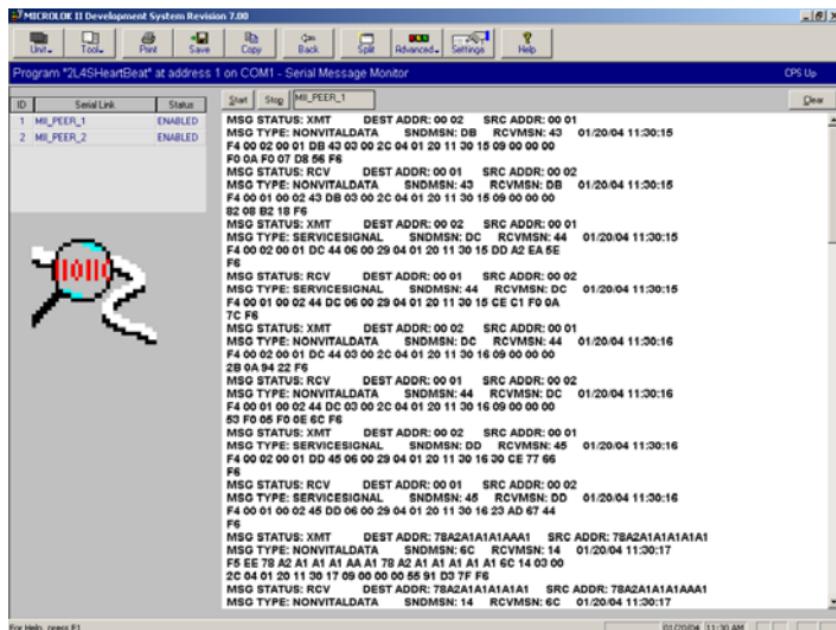


Figure 11-7. Serial Link Monitor

Figure 11-7 shows the Serial Link Monitor view for the MICROLOK II Network Protocol.

The Serial Link Monitor View displays a MICROLOK II PEER record with a descriptive information section and then the actual serial bytes.

The possibilities for the MSG STATUS (Message Status) information are:

- XMT (Transmit)
 - RCV (Receive)
 - MONITOR DATA LOST
 - BAD SEQUENCE ERROR
 - HARDWARE ERROR
 - FORMAT ERROR
 - CRC ERROR
 - MAINTENANCE TOOL ERROR

The possibilities for MSG TYPE (Message Type) are

- UNKNOWN (Unknown due to error) – byte value 0x00
 - INIT (Initialization) – 0x01
 - VITALDATA – 0x02
 - NONVITALDATA – 0x03
 - STATUS (Station Status) – 0x04
 - SERVICESIGNAL – 0x06

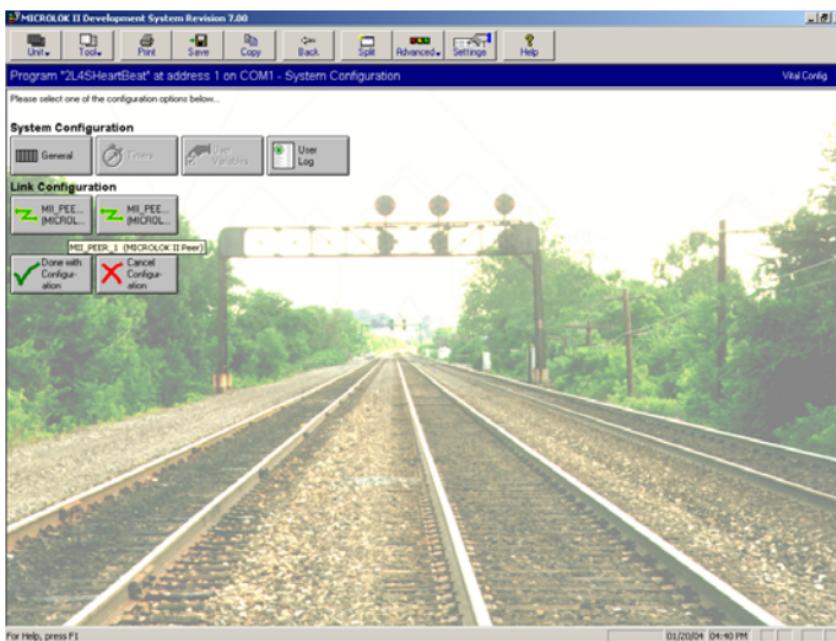


Figure 11-8.System Configuration Main Screen

Figure 11-8 displays the configuration parameters for a MICROLOK II Peer link named "MII_PEER_1." The first section displays the main link parameters and the second section displays a list of all the stations defined for the link. In this case, there are two stations defined.

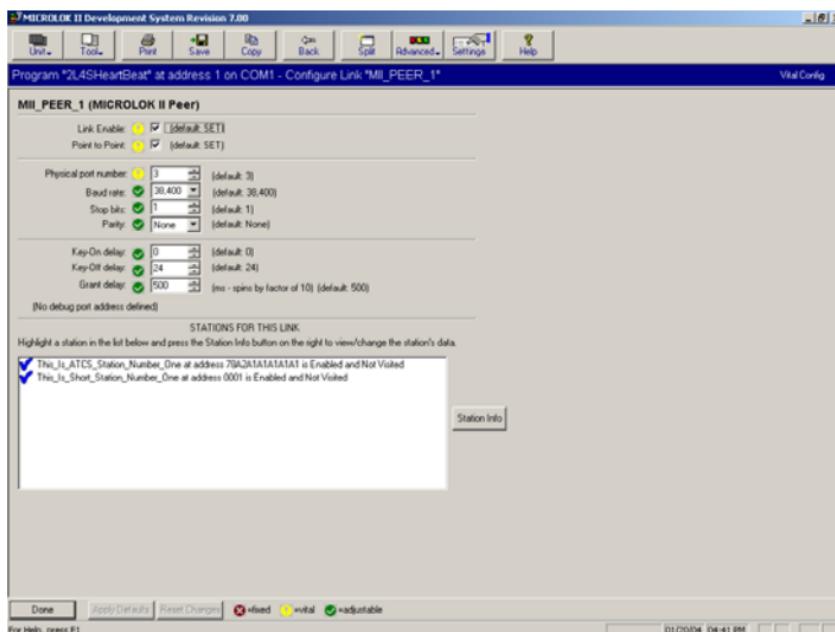


Figure 11-9.Network 1 Screen

The white box below the link parameters contains the station information for this link. Each row represents information for a station. The station's name is displayed first, the station's address, whether the station is enabled or not, and then the station's status. Note that the station address can be shown in either short or long format, depending if the address is of type PEER or ATCS.

A station's status can be one of four conditions: Not Visited, Visited, Data Changed, or Disabled. The station status "Not Visited" means the configuration screen for a station has never been looked at by the user and is represented by a blue checkmark icon on the left side of the row.

There are two ways to enter the configuration screen for a particular station. The first way is to double-click a station's line of text. The second way is to select a station and then click on the "Station Info" button on the right side of the window. Only one station can be viewed at a time.

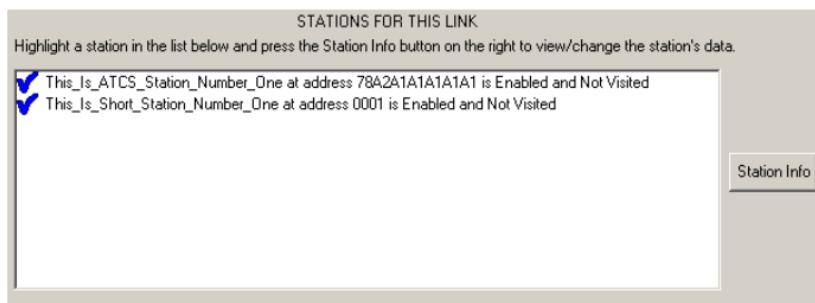


Figure 11-10.Link Station Information Window

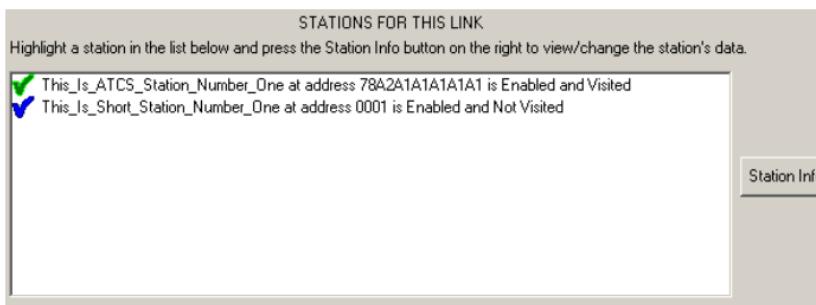


Figure 11-11.First Station Visited Indication Window

Figure 11-11 shows the two stations after the first station's configuration screen was visited. The status "Visited" means that the user viewed the contents of the station's configuration parameters but did not change anything. It refers to a read-only mode by the user. The status "Visited" is shown in the text defining the station. The second station remains unchanged since the user has not visited that station's configuration parameters yet. Its line of text indicates "Not Visited."

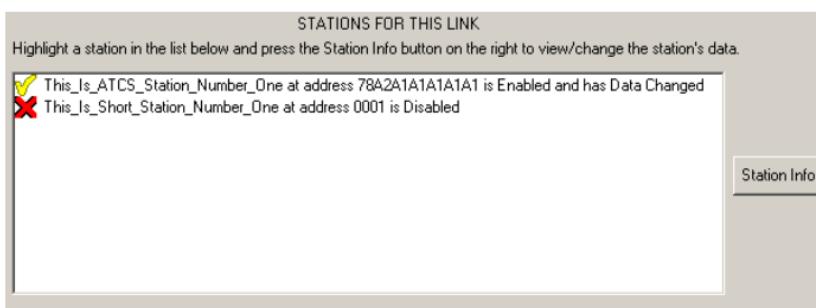


Figure 11-12.Link Station Status Window

Figure 11-12 shows the two stations after both station's configuration screens were visited. The first station's status "Data Changed" means that the user viewed the contents of the station's configuration parameters and made one or more changes.

The second station's status "Disabled" means that the user viewed the contents of the station's configuration parameters and unchecked the Station Enable parameter. The user may or may not have changed other station configuration parameters, but did change the Station Enable parameter to disabled. The status "Disabled" is represented by an X icon to the left side of the line of text (the station will also be disabled if it is unchecked).

When the user opens the main link configuration screen for the first time, all stations will be shown as defined in the application program. An application program allows a station to be defined as ENABLED or DISABLED. Thus, a station's status will either be Enabled and Not Visited or Disabled (X icon).

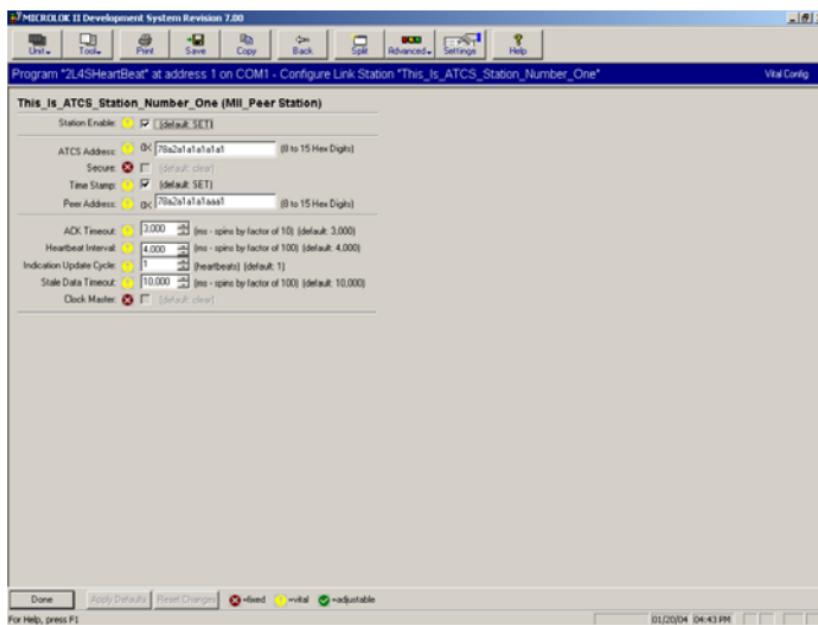


Figure 11-13. Station Configuration Parameters

Figure 11-13 displays the configuration parameters for one station on a MICROLOK II Peer link. This station is named "This_Is_ATCS_Station_Number_One." The parameters for this station are listed on the screen.



12 RESET MENU (RES|MENU)

The primary purpose of the *reset mode* is to reset the VCOR relay and the MICROLOK II system software following the occurrence of a CPS trip.

This mode also provides access to the event and error logs and some hardware configuration functions. The reset mode must be manually selected using the CPU PCB front panel controls.

When the "Reset" button is pressed, the reset LED on the CPU PCB front panel is illuminated. When the "Reset" button is released, it is no longer illuminated.

References to menu options are indicated as XXXX|XXXX representing the information displayed on the upper and lower CPU four-character alphanumeric displays. The upper case characters indicate what is actually displayed e.g., VIEW|SysLOG.

NOTE

The CPU PCB processor reads the front panel switches once every second. Therefore, it is important to be deliberate when operating the switches. Hold the switch in position until the display updates.

To enter the reset mode:

Press and release the "Reset" pushbutton on the CPU PCB front panel.

Quickly operate any one of the four front panel toggle switches. Hold the switch in the toggled position.

Release the toggle switch that was operated in Step 2 after the CPU PCB four-character displays shows **RES|MENU**. The first term (**RES**) is shown on the upper four-character display and the second term (**MENU**) is shown on the lower display.

NOTE

If a parameter adjustment is rejected, the menu returns to the next higher option box in the menu.

Section 12

Reset Menu (RES|MENU)

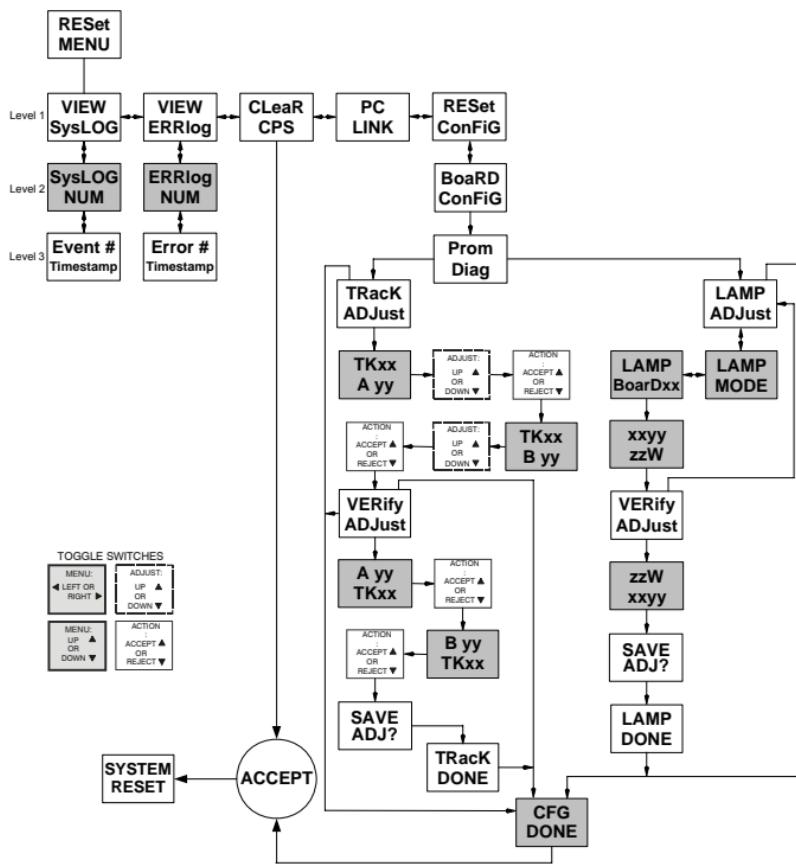


Figure 12-1. MICROLOK II CPU Reset Menu

(with configurable PCBs)

12.1 System Event and Error Logs

Whenever the MICROLOK II unit is operating in normal mode, PC LINK mode, or shutdown mode, information can be recovered from the system error log and the system event log using the MICROLOK II Development System. When troubleshooting a unit that has failed or is malfunctioning, it is important to first check the critical error history contained in the system error log. The system error log contains information on the most recent failure as well as historical information on past failures.

The system error log cannot be cleared by the user, and it retains information as long as the CPU PCB has not been powered-down for more than several hours. It is important to check entries in the system error log for patterns; i.e., the same failure or group of failures occurring repeatedly.

If no recent critical errors are found in the system error log, the system event log should be downloaded to the MICROLOK II Development System and reviewed. The system event log contains information on less-severe conditions that can cause various unit malfunctions.

Logged warnings and events included recoverable errors associated with physical I/O PCBs, and information concerning

performance of the serial links. Most warnings and event messages are self-explanatory.

VIEW|SLOG and VIEW|ERR details are covered in Section 13.3.

In Reset Mode navigate through the menu as shown in Figure 12-1 by using the four CPU toggle switches.

12.2 Clear CPS (CLR|CPS)

Power to the vital outputs is switched from battery through the CPS-controlled VCOR. If the unit has detected errors, the VCOR indicator on the power supply PCB (See Figure 3-1) will be "Off" and the unit will attempt to function with the VCOR down (all voltage to vital outputs disabled). The CLeaR|CPS option in the Reset Menu shown in Figure 12-1 attempts to recover from this CPS Down Mode.

The CLeaR|CPS option is accessed from the VIEW|SysLOG option, toggle the Menu L/R switch to the "Right" position.

With **CLR|CPS** shown on the CPU PCB displays, toggle the Accept/Reject switch to the "Accept" position. This action resets the CPU software and the VCOR relay, and returns the CPU to the on-line mode (assuming that the original cause of the CPS trip is no longer present).

12.3 PC Link (PC|LINK)

Connection via the front diagnostic link connection to a Personal Computer (PC) laptop or Remote Diagnostic Terminal (RDT) running the MICROLOK II Development System. After the PC|LINK mode is activated, the display will show "CNFG" on the upper display and the maintenance port data-rate on the lower display. If, for example, the data-rate is 19200 Bits Per Second (BPS), "1920" appear on the lower display.

12.4 Reset Configure (RES|CFG)

This menu allows the manual configuration of selected track circuit and signal lamp parameters via the BoaRD ConFiGure Menu (BRD|CFG).

NOTE

Only configuration items listed as "adjustable" in the application can be modified via any menu.

NOTE

The MICROLOK II unit will be non-operational while adjustments are made.

12.4.1 Track Board Configure

If no Track Boards are installed in the cardfile, toggle the Menu L/R switch to the "Right" from the TRK|ADJ menu option.

If there is at least one enabled TRACK board installed in the MICROLOK II cardfile, the CPU board displays will show **TRK|BRDS** when the option is selected.

The TRacK BoaRDS option enables you to view the track status and track margin for a selected coded track circuit board. Use the following procedure to select a track circuit board and view the available data:

1. With **TRK|BRDS** showing on the CPU PCB displays, toggle the Menu Up/Down switch to the down position.
2. The CPU PCB displays will show **TRK|BD#**, indicating the selection of one of the installed track boards. The menu is configured for one to four track boards.
3. To change the track board selection, toggle the Menu L/R switch as necessary until the desired track board number is indicated in the lower display.
4. Toggle the Menu Up/Down switch to the down position to display the track status for the selected board. Track status is shown on the CPU PCB displays in the following formats:

XYwZ|STAT or

XYwZ|STAT

... where lower case "x" and "w" represent track codes being received, upper case "X" and "W" are track codes being transmitted, and "Y" and "Z" are track modes. Possible entries for the track modes characters are:

N = normal

R = remove shunt

S = shunt

5. Toggle the Menu L/R switch to either position to display additional data (track margin) for the selected board. The upper four-character display shows (from left to right) the track length in thousands of feet, the track mode (**N**, **R**, or **S**), and the track side (**A** [master] or **B** [slave]). The lower four-character display shows the track margin as a percentage of signal. If the selected track board has two functional track circuits enabled, the displays will automatically toggle between the A track information and the B track information. To return to the TRacK BoaRD# option, toggle the Menu Up/Down switch to the up position twice.

12.4.2 Lamp Board Adjust Menu (LAMP|ADJ)

Lamp wattage is usually specified in the application Programmable Read Only Memory (PROM). If changes are necessary confirm the configuration as loaded from the application are correct and valid.

From the LAMP|MODE option toggle the Accept/Reject switch to the "Accept" position. This sets the lamp sensitivity mode override bit for a period of ten minutes. The displays will read LAMP|BDxx, with xx indicating the default lamp driver board number.

If there is more than one Lamp PCB toggle the Menu L/R switch until the desired board is displayed in the lower display.

Toggle the Accept/Reject switch to "Accept" and the display will read xxyy|zzW.

- "xx" is the lamp board.
- "yy" is the lamp number.
- "zz" is the present wattage setting.

Toggle the Adjust Up/Down switch to set the desired wattage (12, 16, 18, 24, 25, or 36).

The next enabled lamp will display.

Repeat the process until all lamps have been set.

From the VER|ADJ (Verify|Adjust) toggle the Accept/Reject switch to "Accept" and the lamp information will be displayed as zzW|xxyy (data fields opposite of before to verify correct display operation). Toggle the Accept/Reject switch to "Accept." SAVE|ADJ? will display.

To save changes, toggle the Accept/Reject switch to "Accept" and the CPU will write the change to the Electrically Erasable Programmable Read Only Memory (EEPROM). If the write is successful the display will read LAMP|DONE. If unsuccessful it will read ADJ|FAIL.

Toggling any switch on the CPU will abort the set operation and return the user to the LAMP ADJust point.



13 ON-LINE MENU DIAGNOSTICS

The On-Line menu provides access to six separate Level 1 menus (See Figure 15-1). Each of these menus provides a specific set of administrative and diagnostic functions:

- SYSTEM CONFIGURATION menu - view the state of pre-assigned auxiliary bits (See SM-6800C) and adjust system clock parameters.
- DISPLAY SYSTEM menu - display the version number of the installed executive software, display the current system operating load, and view the state of system data bits.
- DISPLAY LOGS menu - display the contents of the system event log and the system error log.
- DISPLAY I/O (Inputs/Outputs) menu - display the status of installed and enabled MICROLOK II printed circuit boards.
- SERIAL TEST - allows testing of the serial ports by use of selected communications test.
- SERIAL PORTS menu - individually determine the status of the four serial links associated with the MICROLOK II's cardfile.

The two four-character displays at the top of the CPU PCB front panel show the current position in the menu structure by displaying or scrolling alphanumeric phrases.

NOTE

Text shown in each menu block (See Figure 15-1) in upper-case letters appears on the MICROLOK II CPU PCB four-character displays e.g., SYStem CoNFiG is displayed as SYS in the upper display and CFIG in the lower display and will be referred to in the following text as SYS|CFIG.

The shaded option boxes are the only menu options that require either an adjustment (up or down) or an action intervention (accept or reject).

13.1 System Configuration Menu (SYS|CNFG)

13.1.1 Auxiliary Bits (AUX|BITS)

View or modify any of the 32 input bit parameters assigned in the application.

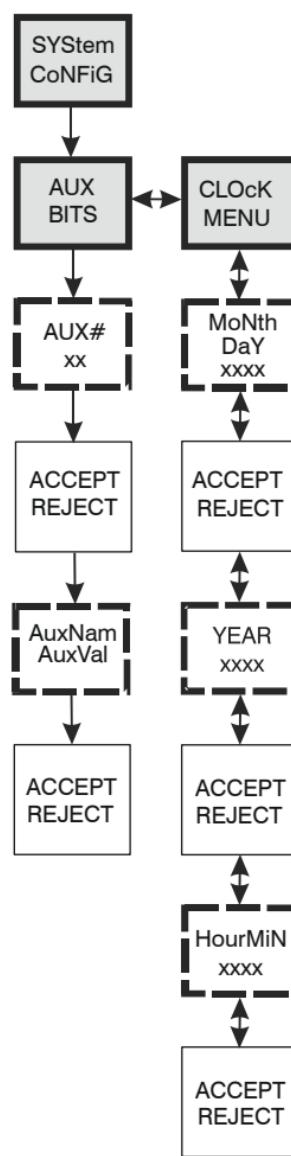


Figure 13-1. MICROLOK II System Configuration Menu

13.1.2 Clock Menu (CLOK|MENU)

View or modify the current settings of the MICROLOK II CPU Real Time Clock (RTC).

13.2 Display System Menu (DISP|SYS)

13.2.1 Display Executive (DISP|EXEC)

The upper alphanumeric display will scroll "Copyright 2xxx, Union Switch and Signal Inc. All Rights Reserved."

The lower display will scroll the phrase Exec Ver • yy.yy (where yy.yy indicates the software version number).

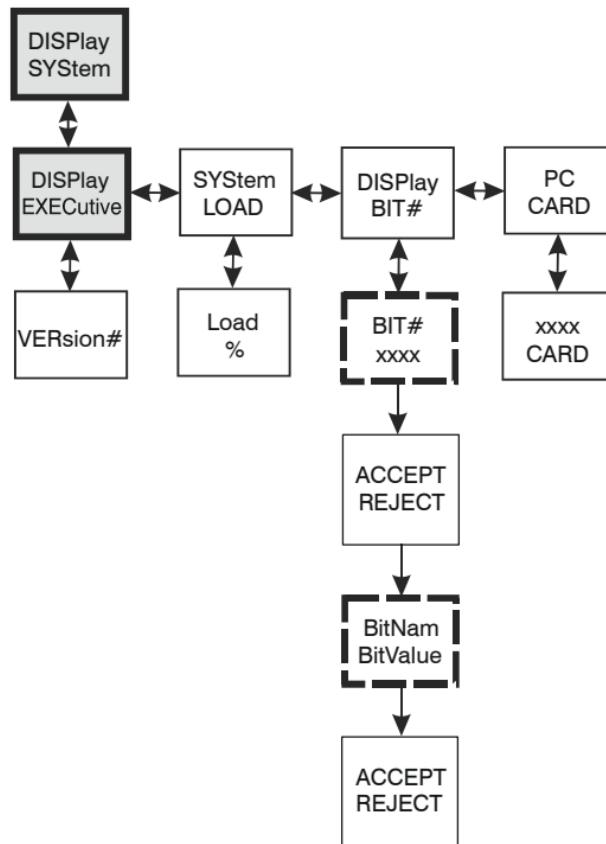


Figure 13-2. MICROLOK II CPU Display System Menu

13.2.2 System Load (SYS|LOAD)

This function displays an approximation (in percent) of the present loading of the MICROLOK II system resources. A loading of 100 percent indicates that the system resources are fully loaded.

13.2.3 Display Bits (DISP|BITS)

Displays any system or application bit and its current Boolean or numeric value.

With **BIT|0001** displayed (1 flashing):

- Use the Adjust toggle until the correct value appears.
- Use the L/R toggle to move left to the next digit.
- Set this value and continue until the desired bit number is displayed.
- Toggle the Accept/Reject switch to Accept.
- The upper alphanumeric display will show the system or application bit name associated with the bit number entered.

13.2.4 PC Card (PC|CARD)

This option displays the location of the PC (PCMCIA) Card on the CPU PCB. The upper display will indicate "NO," "TOP," or "BOT."

The Personal Computer Memory Card International Assoc. (PCMCIA) memory card module can be used to provide additional logging capability for the User Data Log.

Any Static Random Access Memory (SRAM) card may be used in the system. Current restrictions of the hardware limit the size of the PC Card to a maximum of 6Mb. A 4Mb FLASH Card (J703105-0107) is available from ASTS USA.

NOTE

The User Data Log can be downloaded to a PC via the MICROLOK II Development System. If the PC Card is in the write-protect mode (to maintain the data on the card), data can only be retrieved if the application on the CPU PCB matches the one stored on the PC Card.

The User Data Log cannot be cleared if the PC Card is write-protected.

13.3 Display Logs (DISP|LOGS)

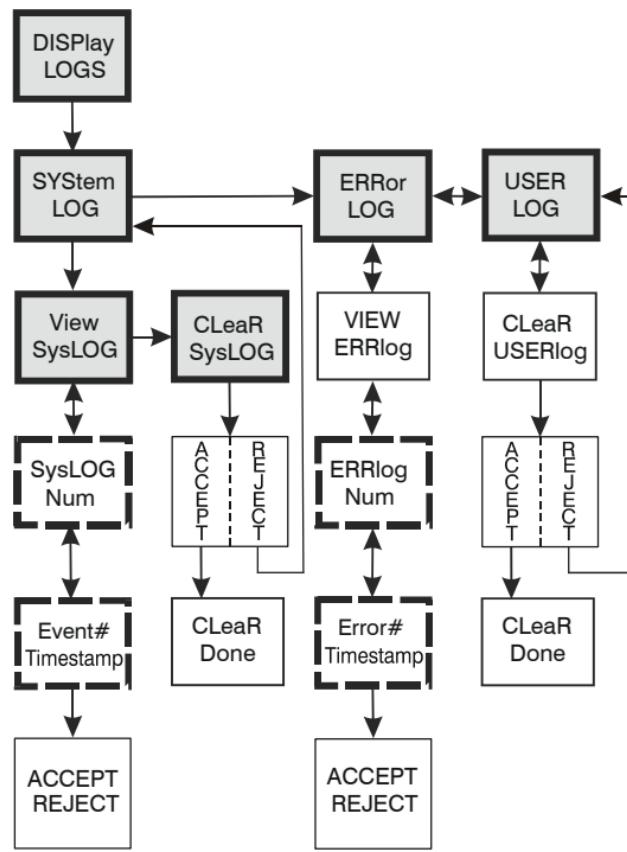


Figure 13-3. MICROLOK II CPU Display Logs Menu

Three logs can be viewed by using the toggle switches on the CPU:

- The system Event Log records up to 5000 of the most recent critical errors, warnings, and events.
- The system Error Log records up to 50 of the most recent critical system errors.
- The User Log records only those events that the user specifies in the application.

13.3.1 System Event Log (SLOG|NUM)

The Event Log (system log) contains a chronological listing of all significant system events and errors.

The upper display shows the event number and the lower display shows its relative position in the queue. The first event in the queue is the most recent.

Toggle Up/Down to move within the queue.

View the time stamp for the displayed event by toggling the Accept/Reject switch to "Accept." The upper display will show the event number and the lower display will scroll the time stamp.

Toggle the Accept/Reject switch to "Reject" to return to VIEW|SLOG.

13.3.1.1 Clear Event Log (CLR|SLOG)

Navigate to the entry and toggle Accept/Reject switch to "Accept" to reset the Event Log. The display will read CLR|DONE for two seconds and return to the Level 1 DISP|LOGS option in the menu.

13.3.2 Error Log (ERR|LOG)

The Error Log information is displayed in the same manner as the Event Log.

If there are no error logs the display will read "NONE."

13.3.3 User Log (USER|LOG)

This log is defined in the application to enable the user at each site to specify a custom set of variables and events that are to be logged in the user log.

The Accept/Reject switch allows the log to be cleared by toggling the switch to "Accept."

The log can only be viewed via a PC or RDT running the MICROLOK II Development System.

13.4 Display I/O (DISP|IO)

These menus display the status of MICROLOK II PCBs.

NOTE

Only the I/O PCBs that are defined in the application will appear in the I/O menu structure.

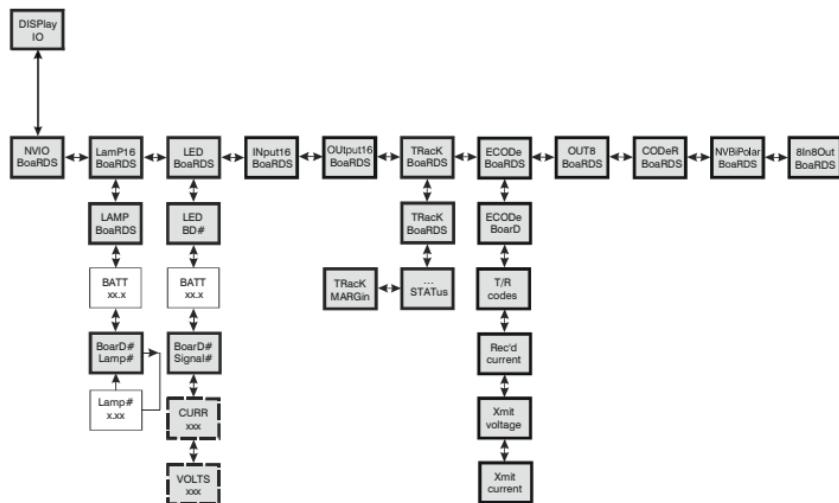


Figure 13-4. MICROLOK II CPU Display I/O Menu

13.4.1 Non-Vital I/O Boards (NVIO|BRDS)

Non-Vital I/O PCBs will display if one is installed in the cardfile.

The only board configuration available (via the MICROLOK II Development System) is Enable/Disable of the PCB.

13.4.2 Vital Input and Output PCBs

13.4.2.1 IN16 PCB (IN16|BRDS)

Vital Input PCBs will display if they are installed in the cardfile.

The only board configuration available (via the MICROLOK II Development System) is Enable/Disable of the PCB.

13.4.2.2 LAMP16 Output PCB (LP16|BRDS)

Allows the user to view output battery voltage and signal lamp currents associated with the PCB selected.

- From the LAMP|BD#, toggle the Menu L/R switch to display the desired PCB.
- Toggle the Menu Up/Down switch down to display the output battery voltage for the PCB (BATT|xx.x)
- Toggle the Menu Up/Down switch down to display the PCB and Lamp (BD#|L#).
- Change the lamp selection with the Menu L/R switch.
- Toggle the Menu Up/Down switch down to view the Direct Current (DC) current being drawn by the lamp (L#|x.xx).

13.4.2.3 TRACK PCB (TRK|BRDS)

The TRack BoaRDS option enables you to view the track status and track margin for a selected coded track circuit board. Use the following procedure to select a track circuit board and view the available data:

1. With **TRK|BRDS** showing on the CPU PCB displays, toggle the Menu Up/Down switch to the down position.
2. The CPU PCB displays will show **TRK|BD#**, indicating the selection of one of the installed track boards. The menu is configured for one to four track boards.
3. To change the track board selection, toggle the Menu L/R switch as necessary until the desired track board number is indicated in the lower display.
4. Toggle the Menu Up/Down switch to the down position to display the track status for the selected board.
Track status is shown on the CPU PCB displays in the following formats:

XYwZ|STAT or
XYWZ|STAT

... where lower case **x** and **w** represent track codes being received, upper case **X** and **W** are track codes being transmitted, and **Y** and **Z** are track modes. Possible entries for the track modes characters are:

N = normal

R = remove shunt

S = shunt

Toggle the Menu L/R switch to either position to display additional data (track margin) for the selected board. The upper four-character display shows (from left to right) the track length in thousands of feet, the track mode (**N**, **R**, or **S**), and the track side (**A** [master] or **B** [slave]). The lower four-character display shows the track margin as a percentage of the received signal. If the selected track board has two functional track circuits enabled, the displays will automatically toggle between the A track information and the B track information. To return to the TRacK BoaRD# option, toggle the Menu Up/Down switch to the up position.

13.4.2.4 LED12 Output PCB (LED|BRDS)

Allows the user to view voltage and current for individual signals for the PCB selected (See Figure 13-5).

- From the **LED|BD#**, toggle the Menu L/R switch to display the desired PCB.
- Toggle the Menu Up/Down switch down to display the output battery voltage for the PCB (**BATT|xx.x**).
- Toggle the Menu Up/Down switch down to display the PCB and LED (**BD#|S#**).
- Change the LED selection with the Menu L/R switch.

- Toggle the Menu Up/Down switch down to view the Direct Current (DC) current being supplied to the signal (CURR|x.xx).
- Toggle the Menu Up/Down switch down to view the LED Voltage (DC) being supplied to the signal (VOLTS|x.xx).

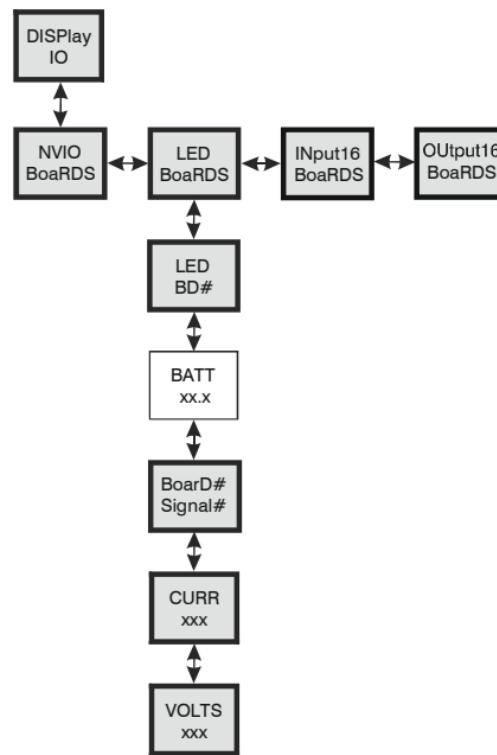


Figure 13-5. MICROLOK II CPU Display LED12 Menu

The only LED12 board configuration available (via the MICROLOK II Development System) is Enable/Disable of the PCB.

13.4.2.5 OUT16 Output PCB (O16|BRDS)

Vital Output PCBs will display if they are installed in the cardfile. No control or indication functions are available.

The only board configuration available (via the MICROLOK II Development System) is Enable/Disable of the PCB.

13.4.2.6 OUT8 ISO Output PCB (OUT8|BRDS)

If there is at least one enabled OUT8.ISO board installed in the MICROLOK II cardfile, the CPU PCB displays will show **OUT8|BRDS** when the option is selected. This option provides no control or indication functions. MENU UP, MENU LEFT, and MENU RIGHT are the only available toggle switch operations for this menu function.

13.5 Serial Port Test Menu

This menu (See Figure 13-6) enables generation of test-signals to be used for testing attached serial communication circuits.

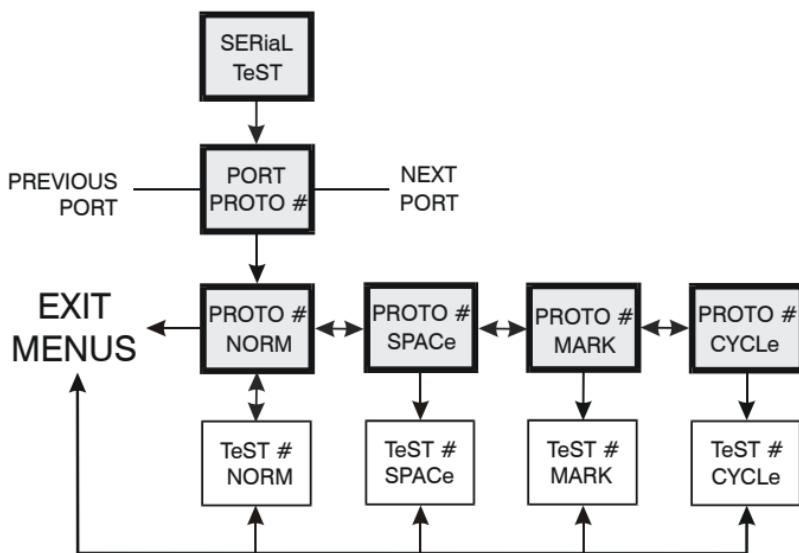


Figure 13-6. MICROLOK II CPU Serial Test Menu

From DISP|IO toggle the Menu L/R switch to the "Right" to the SERL|TEST option.

Toggle the Menu Up/Down switch to the "Down" position.

If no serial ports are defined and active, the display will not change and it will not be possible to enter the serial port test menus; otherwise, the upper CPU display will show the phrase PORT in the upper display. The lower display will show the port protocol as follows:

- From the left the first character can be M (MICROLOK), G (GENISYS), or P (PEER - beginning with Revision 7.0).
- The second character will be M for Master, S for Slave, or R for PEER (beginning with Revision 7.0).
- The third character is blank.
- The last character to the right is the physical port number (1 through 4).

To select the serial port to be tested, repeatedly toggle the Menu L/R switch until the desired physical serial port number is shown in the lower CPU four-character display.

Toggle the Menu Up/Down switch to the "Down" position. The upper CPU PCB display will show the port protocol and the physical port number. The lower display will show the Port Test mode. The display will read NORM (no test in progress).

To change the test mode for the selected port, toggle the Menu L/R switch to select the desired test mode. Options are:

- NORM - Normal operation or no port test mode selected
- MARK - Port sends a continuous mark
- SPAC - Port sends a continuous space
- CYCL - Port sends a 50 percent duty cycle at the configured data rate

When the desired test mode has been selected, the test mode can be initiated by toggling the Menu Up/Down switch to the "Down" position. The CPU display will then show TST# on the upper display and the test mode (NORM, SPAC, MARK, or CYCL) on the lower display.

The selected test mode will remain in effect until a new mode is selected.

A new test mode may be selected by toggling the Menu L/R switch until the new desired test mode appears on the lower display. The new test mode can be activated by toggling the Menu Up/Down switch to the "Down" position.

To exit Serial Port Test mode, select Normal Mode (NORM) by toggling the Menu L/R switch until NORM appears on the CPU display. Exit the serial port text menus by toggling the Menu Up/Down switch to the "Down" position twice.

NOTE

It is not possible to exit the Serial Port Test Menus until the serial port under test has returned to Normal Mode.

13.6 Serial Ports

For a communication link to operate efficiently, the total receiver error count should be no more than 10% of the total count of good messages processed.

NOTE

The default PCB/board numbers that will appear on the four-character displays in the following text are based on the application defined board position.

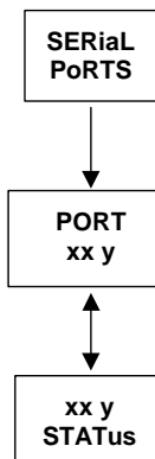


Figure 13-7. MICROLOK II CPU Serial Ports Menu

Use the following procedure to select a serial port and view the status of the port:

1. Toggle the Menu Up/Down switch to the "Down" position. The upper CPU display will show the phrase **PORT**. If no serial ports are defined, the lower display will show 0. Otherwise, the format for the four characters in the lower display is as follows:
 - a. From the left the first character can be M (MICROLOK), G (GENISYS), or P (PEER - Rev. 8.0 exec only).
 - b. The second character will be M for Master, S for Slave, or R for PEER (Rev. 8.0 exec only).
 - c. The third character is blank.
 - d. The right-most character is the port number (1 through 4).
2. To change the serial port being displayed, repeatedly toggle the Menu L/R switch to either position until the desired serial port number is shown in the lower four-character display.
3. Toggle the Menu Up/Down switch to the "Down" position. The upper CPU PCB display will show the port type and the port number. The lower display will show the phrase **STAT**.
4. To determine the status of the selected serial port, look at the five LEDs directly below the CPU PCB four-character displays. These LEDs are labeled as "A" through "E." Each

LED provides a specific type of information about the selected serial port:

- The "A" LED flashes when the serial port is transmitting data to the device at the opposite end of the connection.
- The "B" LED flashes when the serial port is receiving data from the device at the opposite end of the connection.
- The "C" LED indicates that a good address has been received from the device at the opposite end of the connection. This LED is normally on.
- The "D" LED indicates Data Carrier Detect (DCD) detected. This LED is normally flashing.
- The "E" LED indicates that a serial receive error has been detected. This LED is normally off.

To return to the SERiaL|PoRTS option, toggle the Menu Up/Down switch to the "Up" position two times.



14 MICROLOK II DEVELOPMENT SYSTEM

To access the Development System with a laptop PC use a DB-9 to DB-9 null modem cable to connect the COMM1 serial port of the laptop computer to the diagnostics serial port connector on the front of the MICROLOK II CPU PCB.

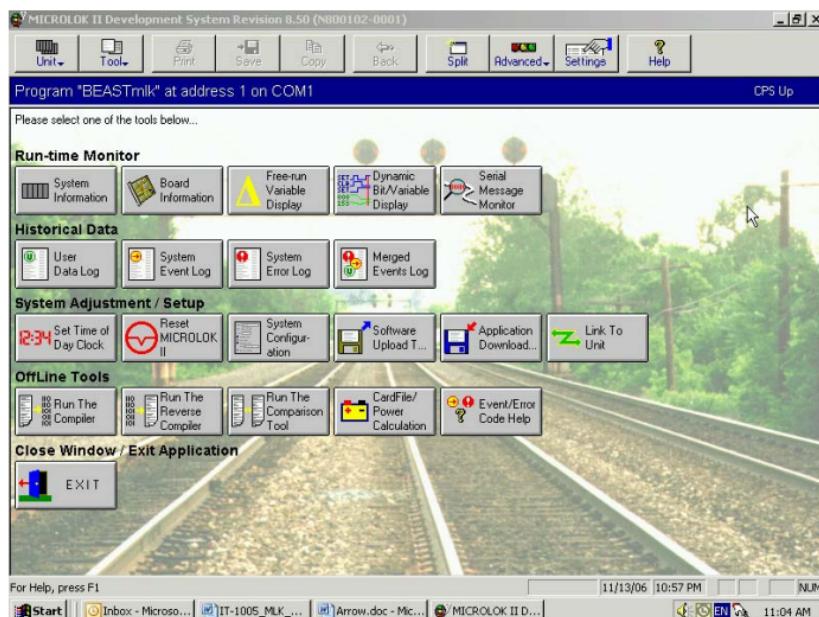
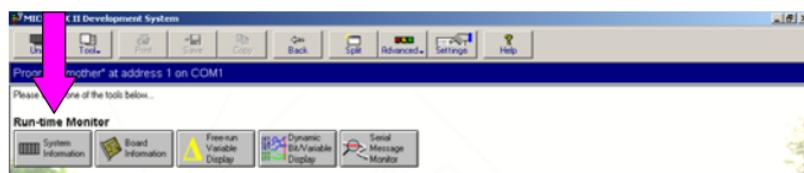


Figure 14-1. Development System Main Menu

NOTE

Screen shots are typical of versions 5.24 through 8.5.

14.1 Run-Time Monitor Buttons



14.1.1 System Information

Displays data about an operating MICROLOK II and its application.

- Executive version, executive Cyclic Redundancy Check ([checksum] CRC), application CRC and compiler version.
- System adjustment table consisting of the event number, the time the event occurred and the event description and any other useful information.

There are twelve possible events for this view. If events are skipped (for example Event 1 then Event 3) that just means an event for Event Class 2 has not occurred.

NOTE

The "Clear" button (lower left) does actually clear the display screen and send a clear message to the MICROLOK II unit. The data may be the same as before the clear because the data is polled every 500 milliseconds, for example, and the data has not changed.

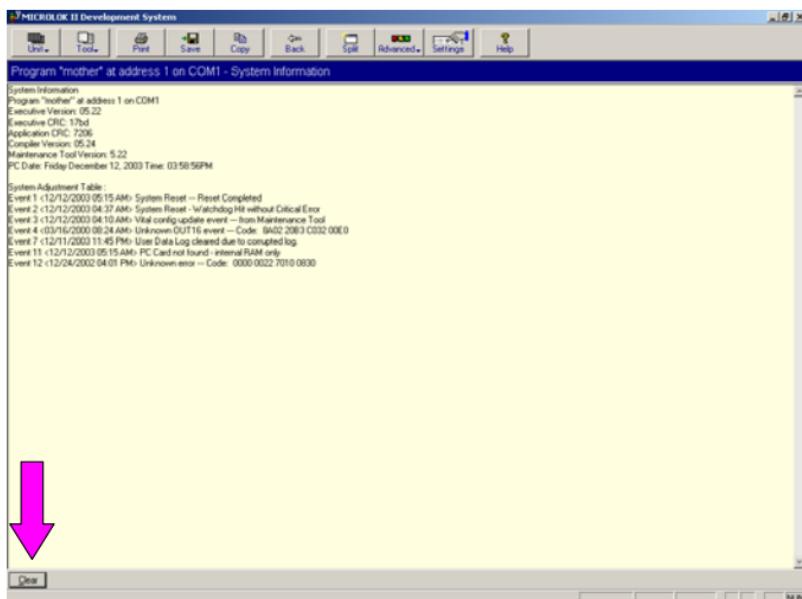


Figure 14-2. System Information Display

14.1.2 Board Information Display



Displays status information about track boards, lamp boards, and also any links included in the configuration.

A button is displayed for each enabled board or link. If all links and boards are disabled no buttons will appear.

Boards and links are enabled during the configuration process.

NOTE

Only an "Exit" button may appear when accessing this view because the boards and links have not been enabled in System Configuration.

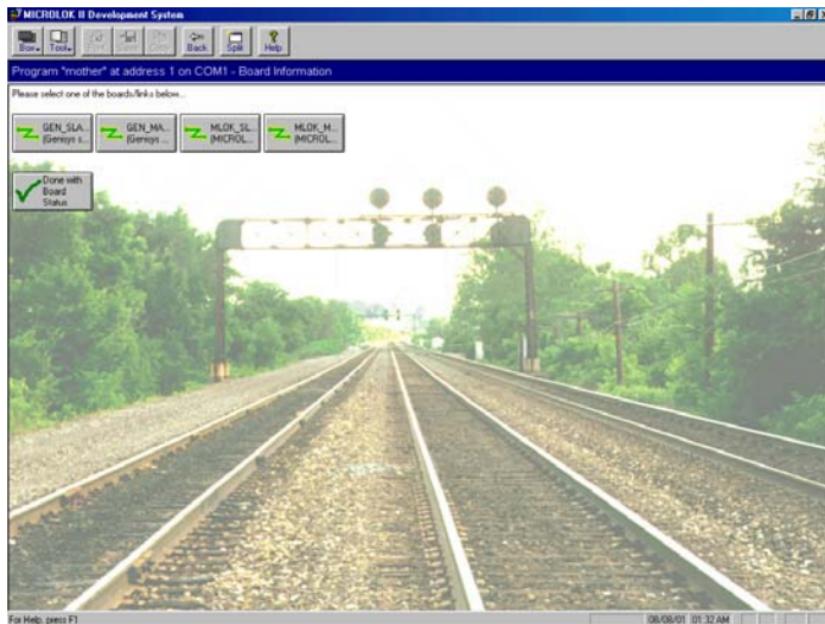


Figure 14-3. Board Information Display

14.1.3 Free Run Display



Lists the current values for user selected variables and bits as well as a real-time list of changes. The free run listing can be saved to a log file or current buffer file.

- User selects from the display list of bits and variables on the left side of the screen.
- Variable selected with either the left mouse button or using the Shift key and the up and down arrow keys.
- Blue rectangle represents a selected symbol.
- Monitored symbols are listed above the "end of active symbols" text.
- Symbols below this text are not monitored.
- Double clicking a symbol sends it to be monitored or unmonitored.
- Recent unmonitored symbols appear at the top of the current unmonitored list.
- The variable list can be sorted by ID or Name.

Current values for selected variables and bits are shown on the text display on the right side of the screen. The scrolling text represents real-time changes. The user has the choice to save the text listing to a continuous log file or a current buffer file. If

the user chooses to save to a log file, the text will be appended to this file if it already exists.

Refer to Figure 14-4.

- "All" button – selects all the symbols on the left side to be monitored.
- "None" button – deselects any symbols in the monitored list (above the "end of active symbols" text).
- White text box – enter the name of a symbol the user is searching for in the box.
- "Advanced" button – performs a more detailed string search and presents the user with two radio buttons. The first radio button allows the user to find all the symbols which begin with certain letters. For example, the string "LED" will return all symbols which begin with the letters "LED" such as LED1, LED2, and LED3. The second radio button allows the user to find all symbols which contain certain letters.



- "Freeze" button – will stop the real time scrolling text and allow the user to scroll up and down the text.

Options are to save the current buffer to a file, create and append a continuous log file, or cancel out.

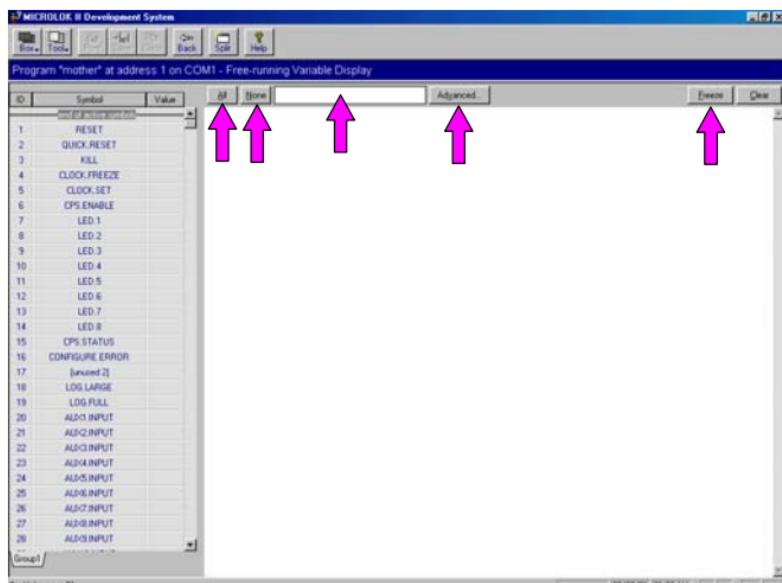


Figure 14-4.Free Run Display

14.1.4 Dynamic Bit Variable Display



Displays a strip-chart view of bit and variable changes in real time.

- User selects from the display list of bits and variables on the left side of the screen.
- Variable selected with either the left mouse button or using the Shift key and the up and down arrow keys.
- Blue rectangle represents a selected symbol.
- Monitored symbols are listed above the "end of active symbols" text.
- Symbols below this text are not monitored.
- The variable list can be sorted by ID or Name.

The current values for selected variables and bits are shown on the graph display on the right side of the screen. The scrolling graph represents real-time changes. The user has the choice to save the corresponding text listing to a continuous log file or a current buffer file. If the user chooses to save to a log file, the text will be appended to this file if it already exists.

Double clicking a symbol sends it to be monitored or unmonitored. Recent unmonitored symbols appear at the top of the current unmonitored list.

- "All" button – selects all the symbols on the left side to be monitored.
- "None" button – deselects any symbols in the monitored list (above the "end of active symbols" text).
- The white text box – is used to enter the name of a symbol the user is looking for. As the user types in the name of the symbol, the program will try to find the symbol associated with the text.
- "Advanced" button – will perform a more detailed string search and presents the user with two radio buttons. The first radio button allows the user to find all the symbols which begin with certain letters. For example, the string "LED" will return all symbols which begin with the letters "LED" such as LED1, LED2, and LED3. The second radio button allows the user to find all symbols which contain certain letters.
- "Freeze" button will stop the real time scrolling graph and allow the user to scroll to the left and right.
- "Clear" button will clear the scrolling graph.

For example, the string "INPUT" will return all symbols which contain the letters "INPUT" such as Gen_Master.1.Inputs.Received, INPUT1 and AUX1.Input. The user chooses the matching symbol and it will be found and selected on the list to the left.

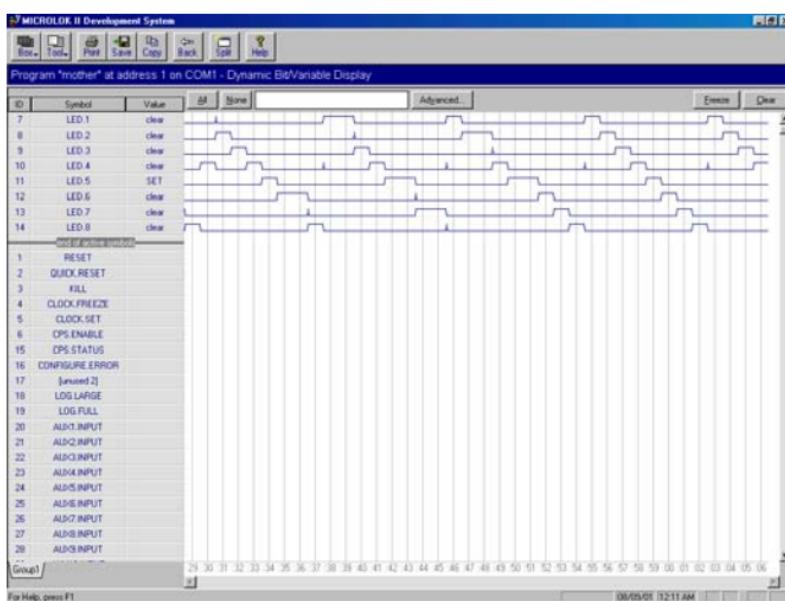
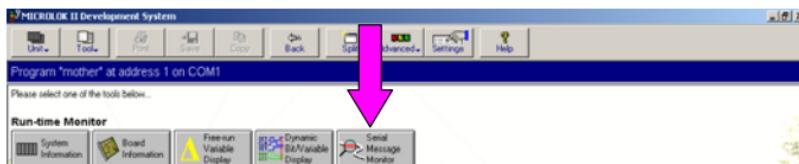


Figure 14-5.Dynamic Bit Variable Display

14.1.5 Serial Message Monitor



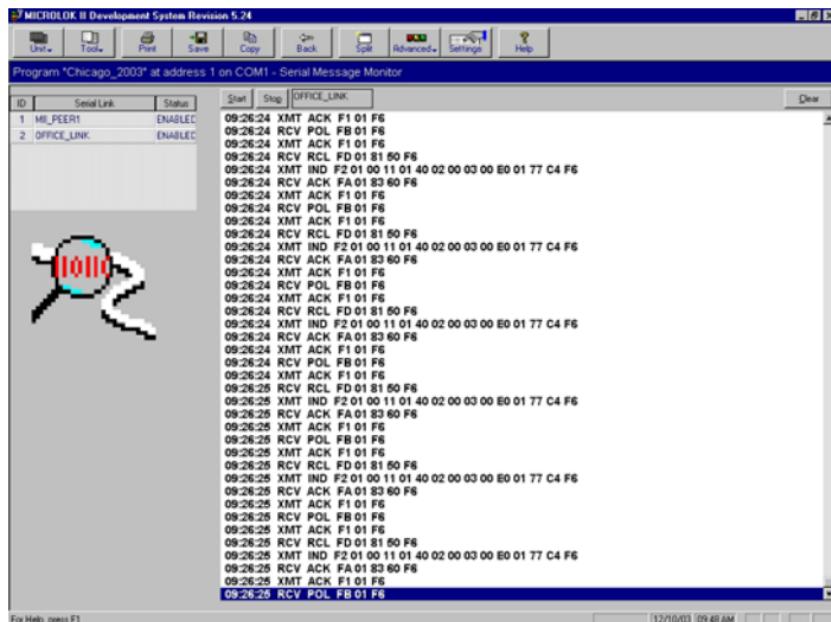
Enables the user to monitor the serial messages for a serial link; either a MICROLOK Master/Slave or GENISYS Master/Slave link.

- Select an enabled serial link to monitor from the list on the left and begin monitoring by clicking the "Start" button.
- Message traffic sent and received on the selected link will begin appearing on the right side of the serial monitor screen.
- Text contains the time the message was sent/received, the message type, and the message content in hexadecimal bytes. To stop the message display press the "Stop" button.
- "Clear" button clears the display.
- Monitor display runs in real time for data rates at or below 2400 BPS (Bits Per Second [data transfer rate]). At data rates higher than 2400 BPS message traffic is packaged in large blocks for transfer and is not displayed in real time.

NOTE

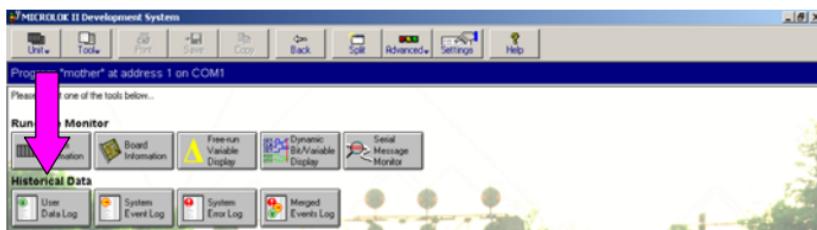
Links will not be displayed if the application does not define any serial links in the Communications section. Also, serial links may be listed but not enabled (the Status column shows the link as "disabled").

To enable links, go to System Configuration on the main launch menu, enter the appropriate password to make changes, and then press the appropriate link button. The links displayed may be Microlok Master and Slave links and/or Genisys Master and Slave links. Go into those link screens and check the Enabled checkbox. Then press "Done" and save the changes (answer "yes" when prompted to save the changes made). Return to the main screen and press the "Serial Message Monitor" button. The view will show the serial link enabled in System Configuration. Press the "Start/Stop" buttons to monitor serial message traffic.


Figure 14-6. Serial Message Monitor

14.2 Historical Data

Displays data that an operating MICROLOK II has collected and stored.



14.2.1 User Data Log

14.2.1.1 User Data Log Dialog Box

The user has the choice of entering no start/end time, which will download the entire user data log. Or enter a start and/or end date/time in the format MM/DD/YY HH (AM/PM) where M is month, D is day, Y is year, and H is hour, e.g., 01/01/00 2 PM represents January 1st, 2000, 2:00pm. If the AM/PM option is not specified, the program will assume the user request is in 24-hour clock format.

- If there are no records for the start time specified, the program will start at the next latest hour that contains records.
- If no records exist on or after the specified start time the program will display a message to let the user know that no records were available.
- If there are no records before the specified end time, the entire log is downloaded.

Syntax for the date/time string:

Month(1 or 2 digits) / Day (1 or 2 digits) / Year (2 digits) Hour (1 or 2 digits) AM or PM (optional).

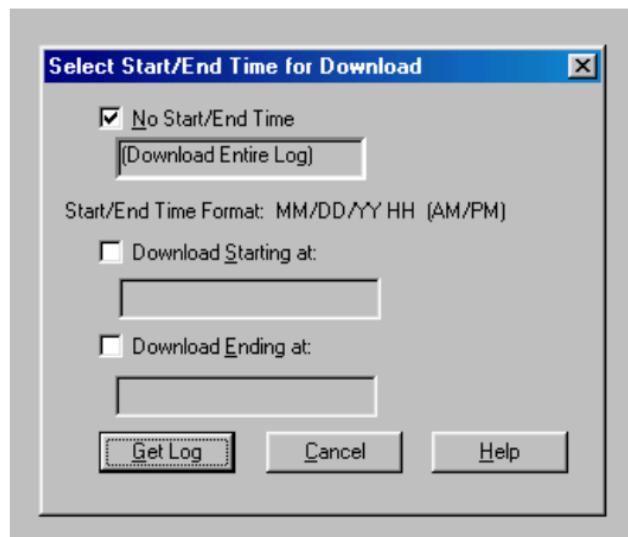


Figure 14-7.User Data Log Dialog Box

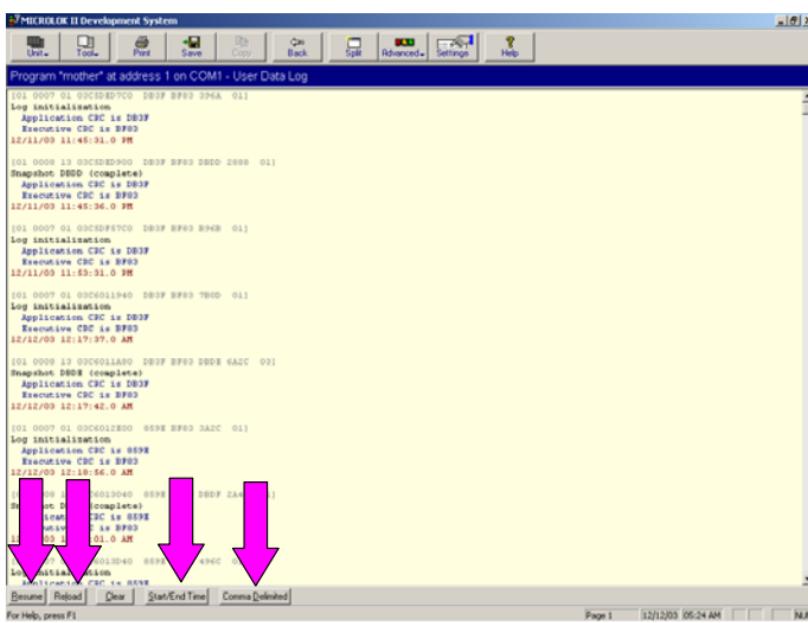


Figure 14-8. User Data Log Display

User Data Log displays changes of selected bit and numeric variables as requested by the application or configuration.

The user data log text will scroll down the screen as it is being downloaded from the MICROLOK II Unit. Pressing the "Freeze" button will stop this process and allow the user to scroll up and down the current log listing using the vertical scroll bar on the right side of the screen. The user can use the scroll box to scroll up and down more quickly. Note that the current page number will be displayed at the bottom of the screen. A page begins at the top of the screen. Page numbers allow the user to print out specific pages or a range of pages of the user data log. The page number will change as the user uses the vertical scroll bar. The vertical scroll bar can be used as it is in any standard Windows application.

Pressing Resume continues the user data log download and text will again scroll down the screen. To clear the user data log press the "Clear" button. The user will be prompted for confirmation. Pressing the "Reload" button will reload the user data log from the beginning. The "Start/End Time" button will allow the user to specify a time range so the user doesn't have to wait for a long period of time to get to the data he/she wants.

14.2.1.2 Viewing Raw Data

To see the raw header data for each record, go into the Program Settings and check the appropriate checkbox under the View Property Page.

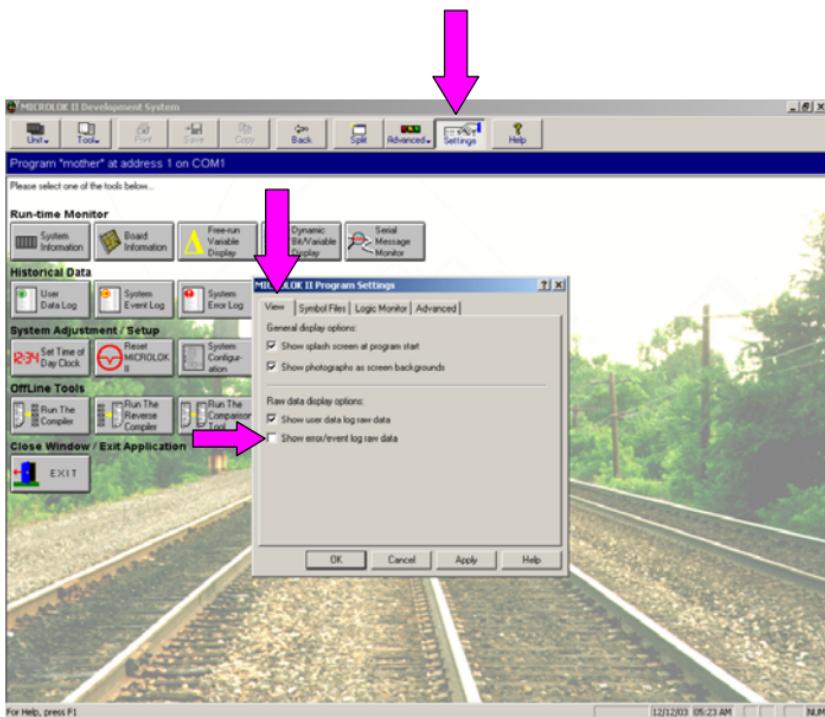


Figure 14-9. Program Settings Dialog Box View Tab

To show the user data log raw data press the "Program Settings" button on the main launch screen (See Figure 14-9) and go to the View property tab (the first and default tab). Under "Raw data display options," check "Show user data log raw data" by left clicking the checkbox with the mouse and then press the "OK" button to finalize the choice.

Figure 14-8 shows the log with the raw data appearing above each user data log record.

The display assumes 80 characters across the screen, which is also true when printing out the user data log. Because of this, the rest of the data for that line will continue on the next line if it exceeds 80 characters.

14.2.1.3 Saving the Log

Click on the "Comma Delimited" button to save the user data log to a comma delimited file format suitable for Microsoft Excel.

The user can save the file via the diagnostics serial port link, or directly from the PCMCIA card in the card reader on the individual PC. To download from the diagnostics serial port link, click on the "Save From Unit" button. To download from the PCMCIA card reader in the PC, choose a socket from the pull down menu, and click on the "Save From PCMCIA" button.

Press the "Save" button to save the log to the hard drive.

Current limitations: A download from the PCMCIA card reader in the PC will only work with the Windows 9X (95 and 98) operating system because the current device driver is not compatible with Windows NT/2000/XP/ME.

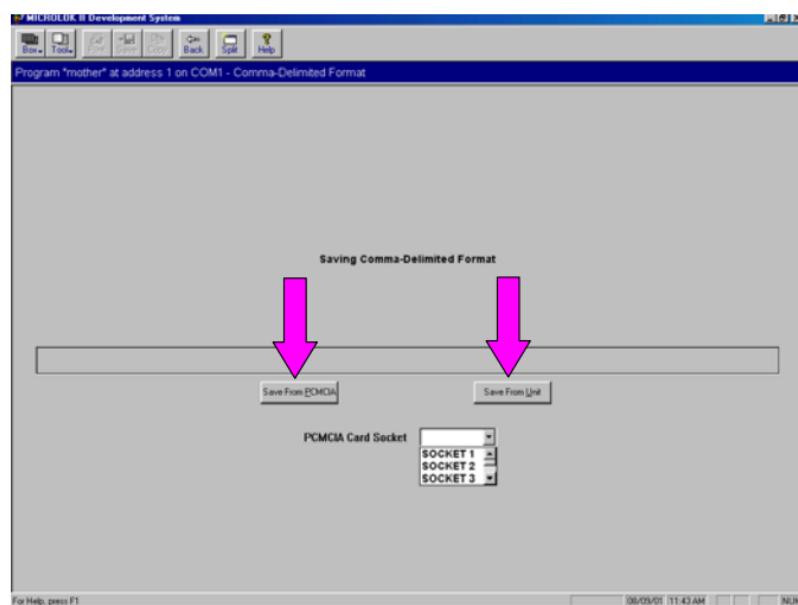
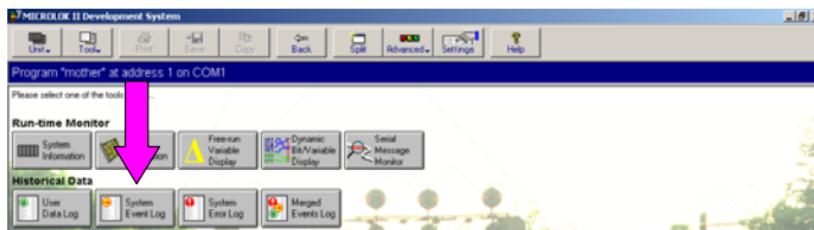


Figure 14-10. Save Comma Delimited View

14.2.2 System Event Log

Displays the most recent 5000 critical errors, warnings or events saved in the system log.



Any system critical error or warning will be logged in the system log. Events are used to relay miscellaneous system information and may be limited by use of the configuration.

- Clicking on the column heading will cause the list to be sorted by that column. Clicking on it a second time will cause the sort order to be reversed.
- To get help on any particular event, error, or warning, highlight the time of the event by clicking on it and then press the F1 key. A help box on that event, error, or warning will appear.
- "Reload" button – refresh the display with the current event data stored on the MICROLOK II.

- "Clear" button – clears the system event log. A confirmation dialog box will appear.
- "Abort" button – stops process while the system event log is being downloaded. The "Abort" button is only available when the log is being downloaded.
- Displaying codes – To display the Codes column on the Event and Error Log Views, go to the main menu and press the "Program Settings" button, now go to the View Property Page (See Figure 14-9).

Check "Show user click the "Show error/event log raw data" Now under "Raw data display options." Click the "OK" button.



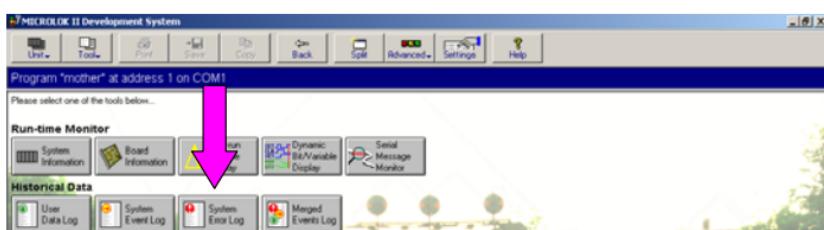
- This symbol represents an information event.
- This symbol represents a warning.
- This symbol represents an error.

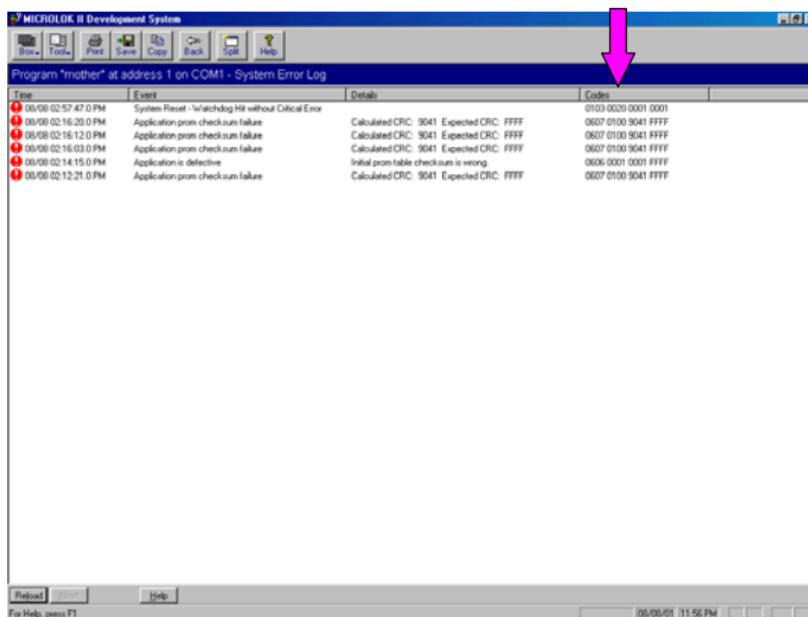
MICROLOK II Development System		
File	Edit	Print
Program "mother" at address 1 on COM1 - System Event Log		
Time	Event	Details
08/08/01 01:32:16.1 AM	MICROLOK_mst hdsl slave comm up-event	Logical port 4, Addr 2
08/08/01 01:32:16.1 AM	GENSYS_mst hdsl slave comm up	Logical port 2, Addr 2
08/08/01 01:32:16.0 AM	MICROLOK_slave hdsl slave comm up-event	Logical port 3, Addr 2
08/08/01 01:32:16.0 AM	GENSYS_slave hdsl slave comm up-event	Logical port 1, Addr 2
08/08/01 01:32:16.0 AM	MICROLOK_mst hdsl slave comm up-event	Logical port 4, Addr 1
08/08/01 01:32:16.0 AM	GENSYS_mst hdsl slave comm up	Serial link GEN_MASTER, Addr 1
08/08/01 01:32:16.0 AM	MICROLOK_slave hdsl slave comm up-event	Logical port 2, Addr 1
08/08/01 01:32:16.0 AM	GENSYS_slave hdsl slave comm up-event	Logical port 3, Addr 1
08/08/01 01:32:16.0 AM	System Reset	Logical port 1, Addr 1
08/08/01 01:32:16.0 AM	System Reset CPS UP	Serial link GEN_SLAVE
08/08/01 01:31:50.0 AM	PC Card not found - internal RAM only	Reset Completed
08/08/01 01:31:57.0 AM	System Reset CPS UP	System Bit CPS_ENABLE or CPS...
08/08/01 01:31:54.7 AM	Reset from diagnostic port	CPS Keys state CPS Up
08/08/01 01:31:54.5 AM	Vital config update event	cps clear flag is 0
08/08/01 01:31:14.0 AM	Unit entering Configuration Mode	from Maintenance Tool
08/08/01 01:31:09.0 AM	PC Card not found - internal RAM only	
08/08/01 01:31:09.0 AM	Configuration warning	saved configuration unusable
08/08/01 01:31:07.0 AM	System Reset CPS UP	CPS Keys state CPS Up
08/08/01 01:23:11.0 AM	System Reset	Reset Completed
08/08/01 01:23:09.0 AM	System Reset CPS UP	System Bit CPS_ENABLE or CPS...
08/08/01 01:23:04.0 AM	User Data Log cleared due to corrupted log	
08/08/01 01:23:04.0 AM	PC Card not found - internal RAM only	
08/08/01 01:23:04.0 AM	Configuration warning	saved configuration unusable
08/08/01 01:23:02.0 AM	System Reset - Watchdog Hit without Critical Error	CPS Keys state CPS Up
08/08/01 01:23:02.0 AM	System Reset CPS UP	Real Time Clock has been changed..
08/07/01 04:57:54.0 PM	Time changed	Time on event is old time when clic...
08/07/01 04:50:49.0 PM	Clock change pending	Logical port 2, Addr 2
08/07/11 10:34.1 AM	GENSYS_mst hdsl slave comm up	Logical port 4, Addr 2
08/07/11 10:34.1 AM	MICROLOK_mst hdsl slave comm up-event	Logical port 2, Addr 2
08/08/01 01:13:51.1 AM	GENSYS_mst hdsl slave comm up	Logical port 4, Addr 2
08/08/01 01:13:51.1 AM	MICROLOK_mst hdsl slave comm up-event	Logical port 4, Addr 2
08/08/01 01:13:51.0 AM	GENSYS_slave hdsl slave comm up-event	Logical port 1, Addr 2
08/08/01 01:13:51.0 AM	MICROLOK_slave hdsl slave comm up-event	Logical port 1, Addr 1
For Help, press F1		
08/08/01 02:01 AM		

Figure 14-11. Event Screen Display

14.2.3 System Error Log

The system error log follows the same rules as the system log, but is limited to a list of the most recent fifty time stamped critical system errors. It has no Clear Log feature.





Time	Event	Details	Code
09/09/02 17:47:00 PM	System Reset - Initializing HII without Critical Error		0003 0000 0000 0001
09/09/02 16:20:00 PM	Application prom checksum failure	Calculated CRC: 9041 Expected CRC: FFFF	0607 0100 9041 FFFF
09/09/02 16:12:00 PM	Application prom checksum failure	Calculated CRC: 9041 Expected CRC: FFFF	0607 0100 9043 FFFF
09/09/02 16:03:00 PM	Application prom checksum failure	Calculated CRC: 9041 Expected CRC: FFFF	0607 0100 9043 FFFF
09/09/02 14:15:00 PM	Application is defective	Initial prom table checksum is wrong.	0606 0001 0001 FFFF
09/09/02 12:21:00 PM	Application prom checksum failure	Calculated CRC: 9041 Expected CRC: FFFF	0607 0100 9041 FFFF

Figure 14-12. System Error Log

- Click on the column heading to sort by that column.
- Click on it a second time to reverse the sort order.
- Click the "Reload" button to refresh the display with the current error data stored on the MICROLOK II.
- Click the "Abort" button while the system error log is being downloaded to stop the process. The "Abort" button is only available when the log is being downloaded.

NOTE

No "Clear" button exists for this log. The System Error Log cannot be cleared because it contains important error information that should not be deleted.

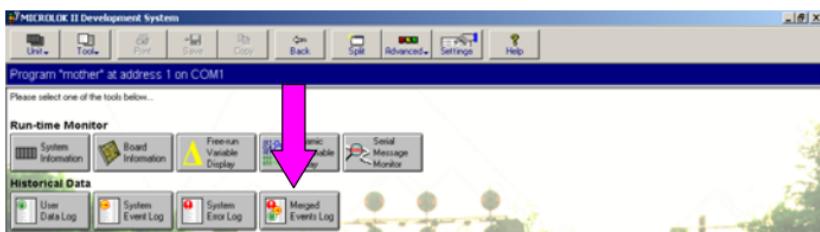
To get help on any particular error, highlight the time of the error by clicking on it and then press the F1 key. A help box on that error will appear.

14.2.3.1 Printing the log

The log will be printed based upon the existing column widths on the screen. If the printed text for a particular column is cut off, just increase the width of that column on the screen and then print out the log again.

14.2.4 Merged Event Log

Displays the User Data Log, System Event Log, System Error log, and Dynamic variable changes merged onto the same time axis.



- Displays only those variables monitored.
- No blank records are shown.
- The graph shown is a combination of all the logs in the system along with any symbol changes in the free run display.

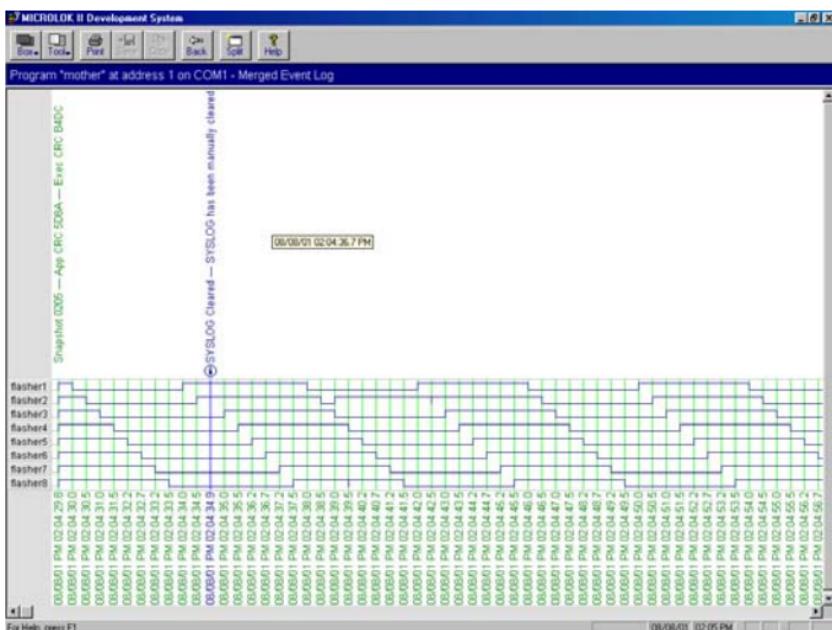
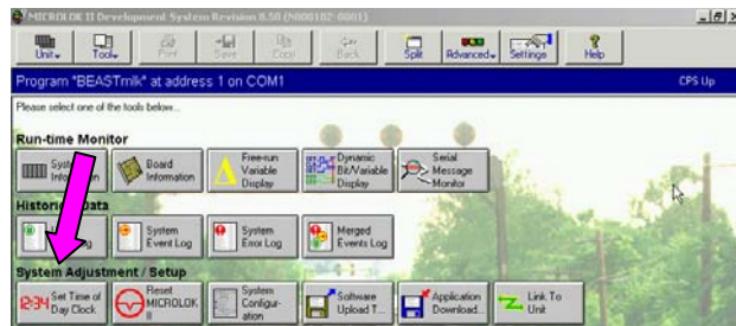


Figure 14-13.Merged Event Log

14.3 System Adjustment/Setup



14.3.1 Set time of Day Clock

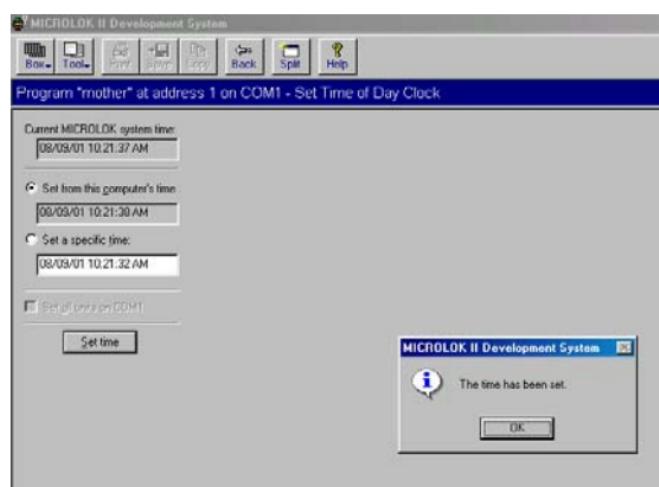


Figure 14-14. Set Time of Day Clock Display

Sets the MICROLOK II's on-board clock.

Select the time of day either from the PC clock or from the time entered manually by the user. Click on the "Set Time" button to transmit the time to the MICROLOK II unit. The date and time format is MM/DD/YY HH:MM:SS (AM/PM) where M is month, D is day, Y is year, H is hour, M is minute and S is second. An example is 01/01/00 2:05:00 PM which represents January 1st, 2000 at 2:05 PM in the afternoon. The Set all units on COMMx checkbox allows the user to set the time of day for multiple MICROLOK II units. To automatically adjust the time change for Daylight Saving Time ensure that rocker switch # 4 on the CPU PCB (See Figure 2-3) is set to the closed position.

Since the MICROLOK II internal clock provides the date stamping information for all logging functions it is important that its accuracy be checked routinely.

Ensure that the clock is set correctly after:

- All Resets
- After software upload or download
- After time changes (daylight savings time)
- After CPS failures

- Once a month as maintenance

14.3.2 System Configuration



Allows the user to change configurable parameters such as track length or lamp wattage. A password is required to modify parameters.

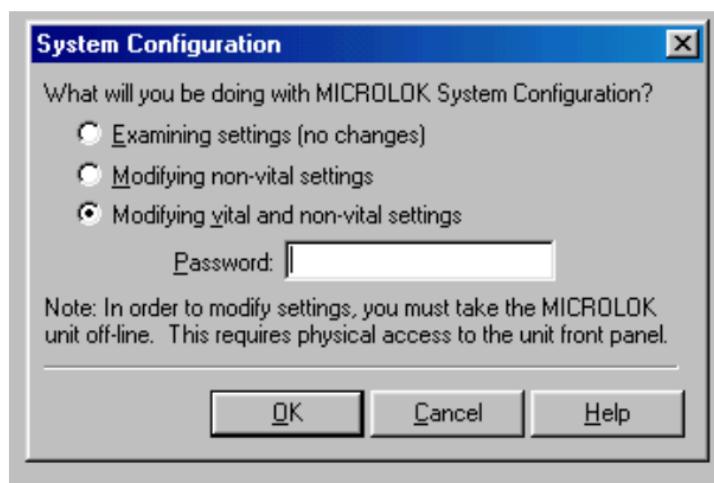


Figure 14-15.System Configuration Dialog Box

The dialog box shown in Figure 14-15 appears after the user clicks the "System Configuration" button on the main launch screen. This dialog presents the user with three choices and a password entry text box.

- Radio button labeled "Examine settings" allows the user to view the configuration of boards and links without making any changes (a read-only view).
- Radio button "Modify non-vital settings" allows the user to view and make changes to the non-vital settings of boards and links. This option requires a password.
- Radio button "Modify vital and non-vital settings" allows the user to view and make changes to the vital and non-vital settings of boards and links. This option also requires a password. The program will not allow access to modifications of configuration values without the correct password.

The main System Configuration screen is shown in Figure 14-16.

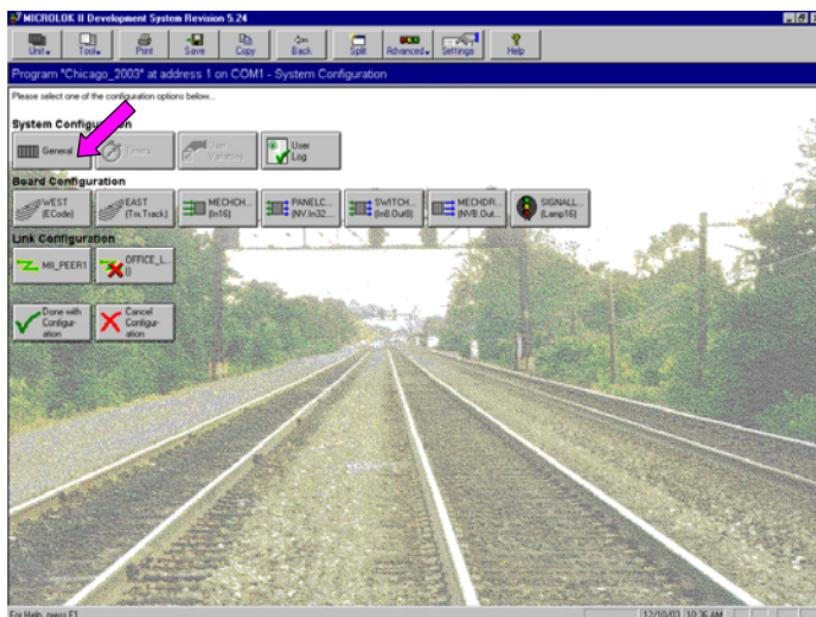


Figure 14-16.Typical System Configuration Display

Click on the "General" selection button on the system configuration selection display. There are several symbols used in the configuration displays that denote what data can and cannot be modified. The symbols include an X which indicates a fixed field with information that cannot be changed; an exclamation point, which indicates that the information is vital and cannot be left blank, and a check mark symbol, which indicates that the information can be changed as required.

=fixed	=vital	=adjustable
--------	--------	-------------

Check/adjust the general system settings on this display as follows:

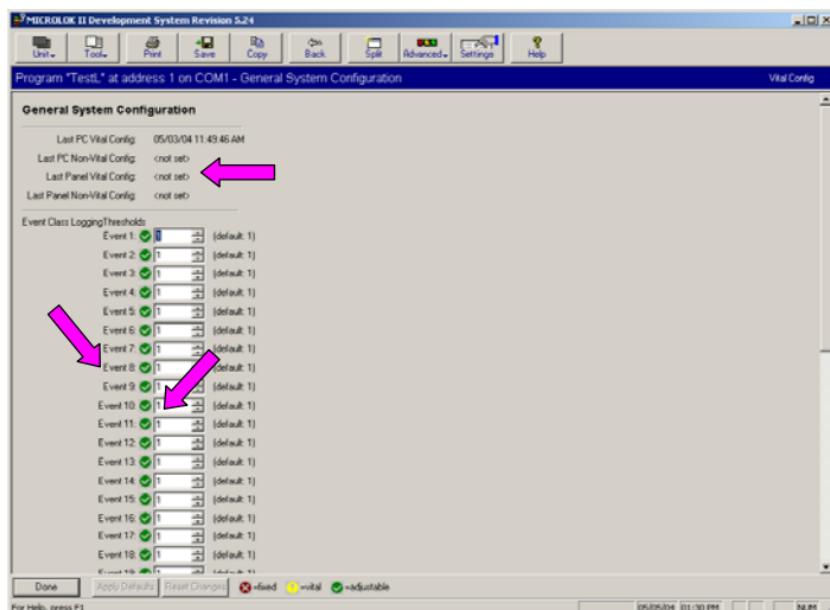


Figure 14-17.General System Configuration

- (1) The top four fields in this display show the dates on which the system vital and non-vital configuration settings were last modified.
- (2) The Event Class Logging Threshold fields are used to manage the amount of information placed in the event buffer during system operation. Each event listed on this display is a system event predefined in the MICROLOK II executive software. The default setting is Level 1 and normally this setting will not be changed.
- (3) Scroll the screen down to access the remaining configuration options on this display. The Timing parameters are set in the application program. These parameters specify delay periods in milliseconds that are used by the system during normal operation (Logic Time-out) and following a manual reset of the system (Delay Reset).
- (4) The PC Configuration fields are used to set the port address and baud rate for the MICROLOK II CPU PCB diagnostics serial port. The default settings are shown to the right of the individual fields.

After modifying the information in one or more fields, two pushbuttons near the bottom of the window become active:

- (1) The "Apply Defaults" button changes the data in all of the fields back to the default values as set in the application program. The default value is shown to the right of each data field.
- (2) The "Reset Changes" button "undoes" all the current changes so that the values revert to what they were when first accessed the configuration screen.

The board configuration selection display provides a number of selection buttons that enable the configuration of the MICROLOK II system printed circuit boards. Buttons are only provided on this display for circuit boards that are properly defined in the application software.

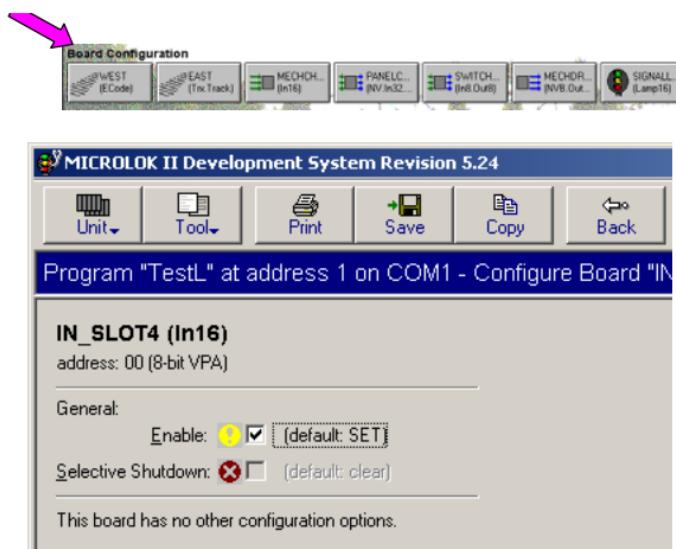


Figure 14-18.Typical PCB Configuration Screen

NOTE

The board enable option is user-configurable via the development system program only if the option is identified as an adjustable parameter in the application software.

The MICROLOK II system supports the operation of several types of serial links. These include MICROLOK system serial links (associated with the MICROLOK II CPU) and GENISYS master and slave links (associated with the code system interface board). Each serial link that is identified in the application program must be properly configured for operation.

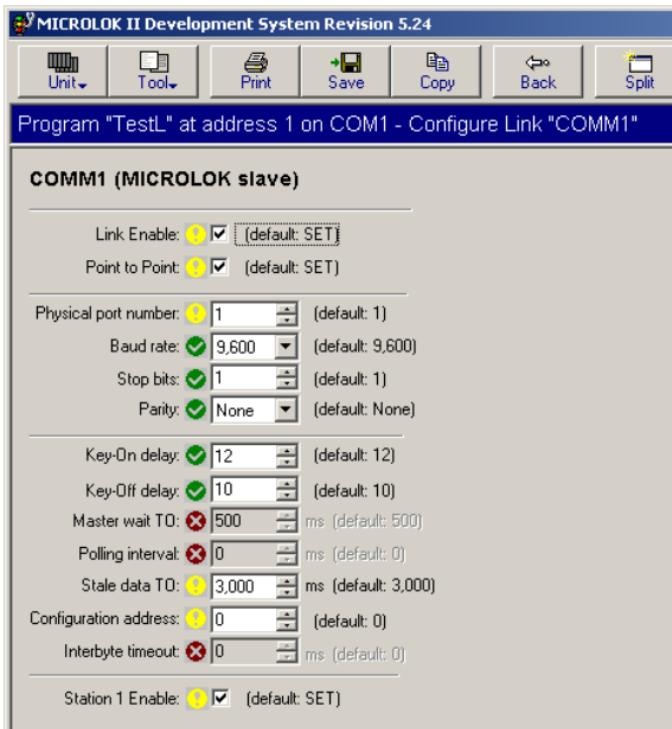


Figure 14-19.Typical Serial Port Configuration Screen

NOTE

Be careful on this screen as some values are in seconds and others are in milliseconds (one-thousandth of a second)!

14.3.3 Software Upload

Permits the user to change the application/executive program in the unit. This button allows the user to upload an application and/or executive program from disk to the MICROLOK II Unit.



The user must first press Reset on the front of the MICROLOK II unit to start the boot program. Once that is done the user can choose to upload an executive and/or an application file.

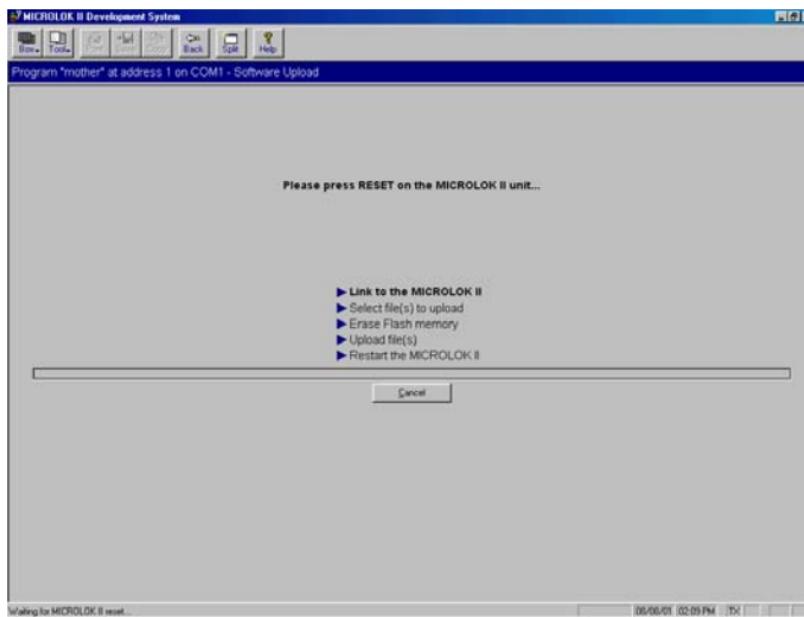


Figure 14-20. Software Upload Screen

After pressing reset, the user must choose a file to upload (See Figure 14-21). Choosing an executive file will automatically give the user a chance to choose an application file. The reverse is not true, if the user first chooses an application file an executive file choice will not be given.

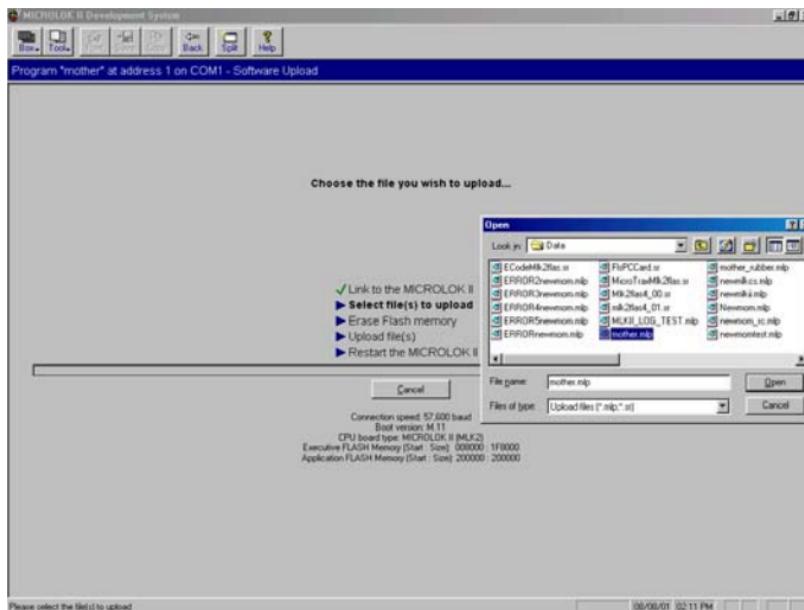


Figure 14-21. Software Upload File Open Dialog Box

NOTE

If S-Record (*.MLP) file is invalid, the program will abort the software upload. It will display the invalid S-Record line number and its contents (See Figure 14-22).

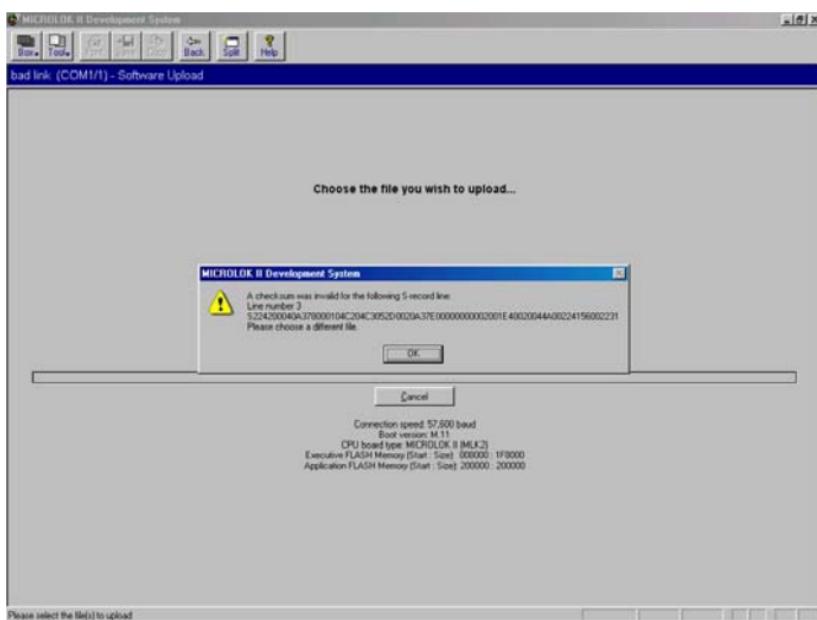


Figure 14-22. Software Upload Invalid File Dialog Box

Pressing the "Cancel" button displays a confirmation dialog box (See Figure 14-23). Since the program is erasing the flash, continuing at this point will render the box unusable.

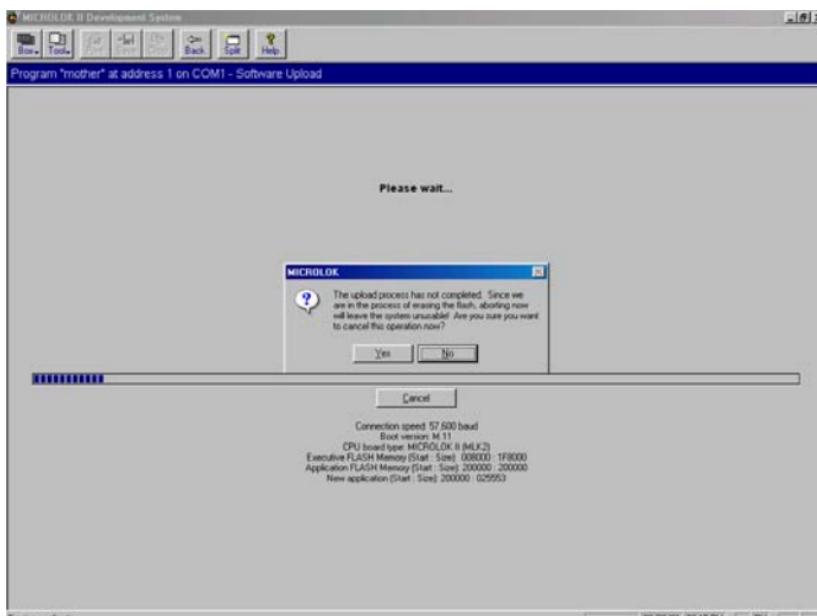


Figure 14-23. Software Upload Progress Dialog Box

After the upload has completed and the MICROLOK II restarts, the system must be reconfigured, or it will not run.

14.3.4 Application Download

This screen enables the user to download the application file that is currently in the MICROLOK II flash memory and place it on a disk (floppy or hard drive).



- The user chooses the filename.
- Program reads the application from flash memory and writes it to that filename.
- The process is automated and a progress bar will display how long the process will take.

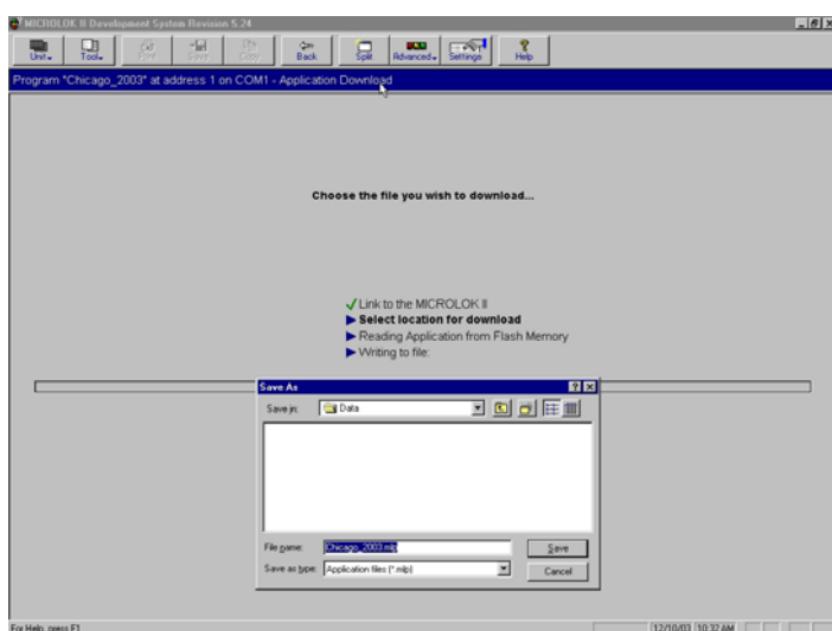
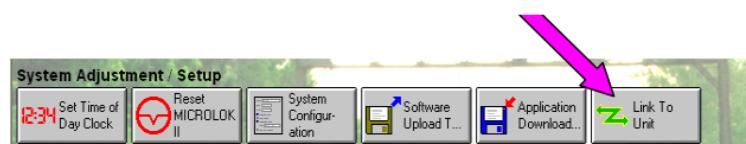


Figure 14-24.Application Download Screen

14.3.5 Link To Unit



Left-click on the "Link to Unit" button to re-establish the serial connection between the PC and the MICROLOK II unit. Clicking the button opens the pop-up screen shown in Figure 14-25 as the connection is established. Once connected, the program running on the unit is displayed on the top toolbar and the message box disappears.

NOTE

Ensure that the proper com port of the PC is connected to the MICROLOK II. Otherwise the reconnect will fail ("Bad Link" will appear in the top toolbar).

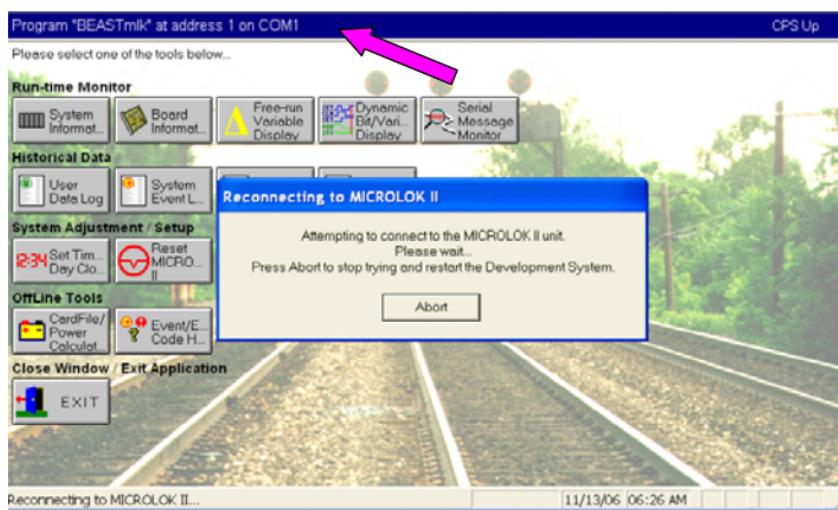
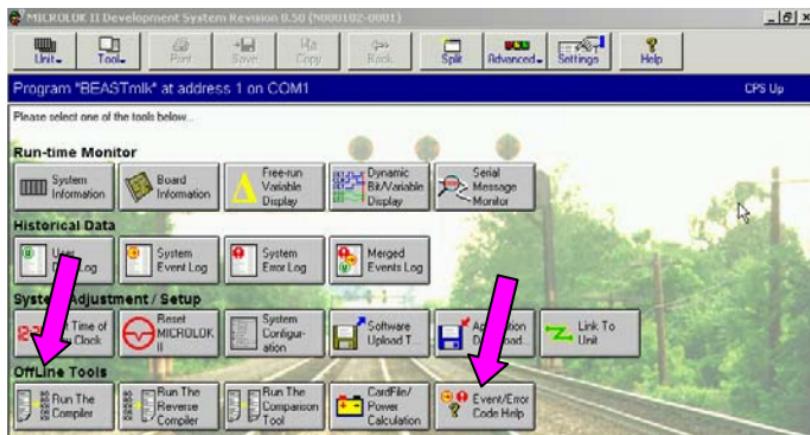


Figure 14-25.Reconnecting to the MICROLOK II

14.4 Off-Line Tools



14.4.1 Event/Error Code Help Screen

Press the "Event/Error Code Help" button on the Main Menu screen to open the Event/Error Code Help Screen shown in Figure 14-26.

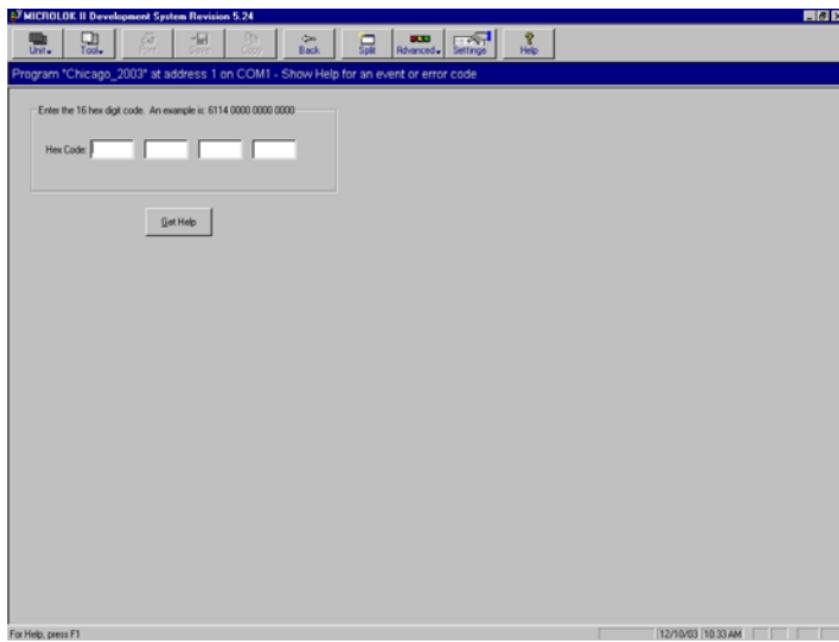


Figure 14-26. Event/Error Code Help Screen

Enter a 16-digit hex event or error code number then press the "Get Help" button. The help text displays what an event or error code actually means in plain English.

Enter four digits at a time as presented in the Codes column in the Event or Error Logs (See Figure 14-12).

NOTE

If the codes column is not present in those logs the user must activate it under the "Settings" button on the main launch screen (See Figure 14-1). On the View Tab check the box "Show Error/Event log raw data" (See Figure 14-9). The Codes column will show up as the last column on the Event or Error Log screen.

Valid hex digits are 0 through 9, A, B, C, D, E, and F.

NOTE

The user may enter a *valid* 16-digit hex code but receive unknown help text. This is because the help file has not been updated for the particular code. The functionality of this view is dependent on the validity and thoroughness of the help file.

15 MICROLOK II ERROR CODES

Table 15-1. Development System Error Codes

CODE	DESCRIPTION
0101	Missed 2 MS Interrupt
0103	PC Card information
0103	Reset from diagnostic port - cps clear flag is x
0103	System Reset
0103	System Watchdog Timeout – Check CPU board.
0104	System SHUTDOWN
0105	System Reset CPS status
0106	Reset CPS error
0107	RAM error - RAM: @reset PATTERN TEST : count:x WHICHRAM:y at:z
0107	RAM error – Check CPU board.
0107	Reset RAM stack Pattern Test error
0108	RAM error - RAM: @reset Walking1's test: count:x WHICHRAM: y at z
0108	RAM error – Check CPU board.
010A	Internal Error – Check CPU board.
010A	Keyboard error
010B	System Time Source error
010B	Time Source Error – Check CPU board.
010C	Logs Initialization--data corruption detected during reset. The System Event and Error Logs have been cleared.
010D	SYSLOG detected full during reset. The System Event log has been correctly adjusted.
010E	SYSLOG Cleared - SYSLOG has been manually cleared
010F	ERRORLOG detected full during reset. The Error Log has been correctly adjusted.
0110	Application set INVALID time
0110	Time change pending - Time on error is old time when clock changed.
0110	Time Changed. Real Time Clock has been changed. Front panel maintenance tool or application.
0111	CPS flag cleared

CODE	DESCRIPTION
0112	Invalid User Log Snapshot status - Snapshot Status = x
0113	User Data Log information
0114	User Data Log record truncated. Too many bits changed at once. Snapshot logged.
0115	Year is changing from 'x' to 'y'. - The year for this event timestamp is 'z'.
0116	Application has set the clock. Application has set RTC with it's clock settings.
0117	Lamp board not supported in this executive.
0118	Audible alarm error
0119	PC Card Error – Check or replace Card.
0119	PC Card Information - Code: x y z
0201	Data Bus error
0201	Data Bus Error – Check CPU board.
0202	Address Bus error
0202	Address Bus Error – Check CPU board.
0203	Internal Error – Check CPU board.
0203	QSPI error - request larger than buffer
0207	CPU Error – Check CPU board.
0207	CPU Hardware error
0208	CPU Watchdog failure – Check CPU board.
0208	Hardware error - Watchdog Failed to Timeout
0209	Internal Error – Check CPU board.
0209	Unable to allocate memory for data bus memory effects test
020A	CPU Register Test error - count = x actual value = y expected value = z
0280	Diagnostic port error
03#0	Diagnostic Watchdog error -
0301	CRC16 error
0301	Executive PROM Error – Check CPU board.
0302	Executive PROM Error – Check CPU board.
0303	RAM Diagnostics Pattern Test error - RAM: On-line RAM PATTERN TEST failure at: W4x
0303	RAM error – Check CPU board.
0303	SUM16 error

CODE	DESCRIPTION
0304	RAM Diagnostics Walking 1s Test error
0304	RAM error – Check CPU board.
0305	Diagnostic error - Diagnostic x Index Out Of Range (y) (z)
0305	Internal Error – Contact ASTS USA if repeated.
0306	Data Error – Check CPU board.
0306	Data verification error
0307	CPU Numeric Error – Check CPU board.
0307	Numeric Diagnostic error -
0308	Internal Error – Check CPU board.
0308	Stability Check error
0309	PC Card Diagnostics Error – Check PC Card.
0309	PC Card memory test error - Address = x Type = y
030A	Blank Executive Diagnostic error
04##	Executive loading error
0401	Executive error
0401	Internal Error – Check CPU board.
0402	Diagnostic Watchdog error
0402	Executive error
0402	Executive error
0402	Executive Loading error – Task x over-scheduled. P1 = 1 P2 = z
0402	Internal or Application Error – Check CPU board or Application.
0402	System Timer Watchdog Timeout
0403	Executive error
0403	Internal Error – Check CPU board.
0404	Executive error
0404	Internal Error – Check CPU board.
0405	Executive error
0405	Internal Error – Check CPU board.
0406	Executive error
0406	Internal Error – Check CPU board.
0406	Reset error - Quick Reset Timer flags do not match Path1 = x Path2 = y

CODE	DESCRIPTION
0407	Internal Error – Check CPU board.
0407	Interrupt/CPS Pick error
0408	Application Process error
0408	Internal Error – Check CPU board.
0409	Check Inputs
0409	Double store error - PC-high: x PC-low: y
0409	Internal Error – Check CPU board.
040A	Internal Error – Check CPU board.
040A	Stack error – at address: x
040B	Sequencing Error – Check CPU board.
040B	Trace error
040C	Internal Error – Check CPU board.
040C	ROM error
040D	Internal Vector error
040D	Interrupt Error – Check CPU board.
050#	Executive error
0501	Application Variable Database Error – Check CPU board.
0502	Application Variable Database Error – Check CPU board.
0503	Application Variable Database Error – Check CPU board.
0504	Numeric value for x out of range
060#	Application Specification error
0601	Application Startup Error – Check CPU board.
0602	Application Startup Error – Check CPU board.
0603	Application Startup Error – Check CPU board.
0604	Application checksum failed - assign equation number x
0604	Application checksum failed - block equation number x
0604	Application checksum failed - nv.assign equation number x
0604	Application checksum failed - nv.assign equation number x
0604	Application checksum failed on path 2 - assign equation number x

CODE	DESCRIPTION
0604	Application checksum failed on path 2 - block equation number x
0604	Application checksum failed on path 2 - nv.assign equation number x
0604	Application checksum failed on path 2 - nv.assign equation number x - Coded Outputs assignment Path 1
0604	Application Execution Error – Check CPU board.
0604	Application table error on path 2
0604	Assign statement corrupted - missing end flag in statement number x
0604	Assign statement corrupted on path 2 - missing end flag in statement number x
0604	Evaluate statement corrupted - missing end flag in statement number x
0604	Evaluate statement corrupted on path 2 - missing end flag in statement number x
0604	Executive function corrupt - invalid boolean parameter type in statement number x
0604	Executive function corrupt - invalid numeric parameter type in statement number x
0604	Executive function corrupt - missing end flag in statement number x
0604	Executive function corrupt on path 2 - missing end flag in statement number x
0604	Invalid Logic Equation - corrupted or invalid values
0604	Invalid Operand - invalid opcode - x
0604	Logic execution error - trigger list checksum failed
0604	Numeric expression error - invalid opcode - x
0604	Numeric expression error on path 2 - invalid opcode - x
0604	Nv.assign statement corrupted - missing end flag in statement number x
0604	Nv.assign statement corrupted on path 2 - missing end flag in statement number x
0604	Nv.evaluate statement corrupted - missing end flag in statement number x
0604	Nv.evaluate statement corrupted on path 2 - missing end flag in statement number x
0604	Unknown statement in block - equation number x

CODE	DESCRIPTION
0604	Unknown statement in block on path 2 - equation number x
0605	Configuration information
0605	Internal Error – Check CPU board.
0606	Application Defective
0606	Application is defective - Initial prom table checksum is wrong.
0606	Shared RAM I/O used to trigger logic.
0606	Wrong application compiler - Need version x. Application is version y.
0606	Wrong application compiler or application was corrupted – Check Application and then CPU board.
0607	Application CRC (Cyclic Redundancy Check [checksum]) error. Reload application then check CPU board.
0607	Application prom checksum failure - Calculated CRC: x Expected CRC: y
0701	Application Loading Error - Timer Change List Overflow
0701	Application Logic Queue Overflow – Check application program.
0701	Logic queue overflow error
0701	Result overflow in nv.assign statement - statement number x
0701	Result overflow in nv.evaluate statement - statement number x
0702	Application error - number of active outputs for coded output array too large
0702	Application error – Check application.
0702	Application math error
0702	Application table error
0702	Application table error on path 2
0702	Block/Table stale timeout - Timer number = x
0702	Coded Output error - coded output timer xref does not match
0702	Coded Output error - loop counter mismatch in coded output timer
0702	Executive function math error - statement number x
0702	Invalid executive function - statement: x function y

CODE	DESCRIPTION
0702	Invalid executive function on path 2 - statement: x function y
0702	Invalid time for Coded Output - Set and Clear times both 0
0702	Logic execution error - statement execution count mismatch
0702	Math error
0702	Shared Ram event queue executive function error - parameter count wrong. statement: x
0702	Shared Ram event queue executive function error – parameter out of range. statement: x parameter y
0703	Configuration error
0703	Internal Error – Check CPU board.
0704	Application caused reset.
0704	Reset Bit set by application logic
0705	Application killed system.
0705	Kill Bit set by application logic
0706	Application caused quick-reset.
0706	Quick Reset Bit set by application logic
0707	Application logic took too long to initialize – Check application.
0707	Logic Initialization Timeout
0708	CPS Reset Bit set by application logic
0709	Logic Initialization Error
0801	Internal Error – Check CPU board.
0801	Vital RAM error occurred on last echo. Board: x
0806	Incorrect board type x in application - (check application image)
0806	Internal Error – Check Application and CPU board.
0806	Unable to allocate memory for I/O board block
0901	IN16 Board x - Echo Error
0901	IN16 Echo Error – Check IN16 board.
0902	IN16 Board x - Type Error
0902	IN16 Type Error – Check IN16 board.
0906	IN16 Board Information
0906	IN16 Internal Error – Check CPU board.
0A0#	OUT16 Information
0A01	OUT16 Board x - Echo Error

CODE	DESCRIPTION
0A01	OUT16 Echo Error – Check OUT16 board.
0A02	OUT16 Board x - Type Error
0A02	OUT16 Type Error – Check OUT16 board.
0A04	OUT16 Hardware Failure – Check OUT16 board.
0A05	OUT16 Hardware Failure – Check OUT16 board or wiring.
0A06	OUT16 Internal Error – Check CPU board.
0B0#	IN8OUT8 Board Information IN8OUT8 Board x Input y - Input Good
0B01	IN8OUT8 Board x - Echo Error
0B01	IN8OUT8 Echo Error – Check IN8OUT8 board.
0B02	IN8OUT8 Board x - Type Error
0B02	IN8OUT8 Type Error – Check IN8OUT8 board.
0B04	IN8OUT8 Hardware Failure – Check IN8OUT8 board.
0B05	IN8OUT8 Hardware Failure – Check IN8OUT8 board or wiring.
0B06	IN8OUT8 Internal Error – Check CPU board.
0C0#	Lamp 16 Board Information
0C01	Lamp16 Board x Echo Failure
0C01	LAMP16 Echo Error – Check LAMP16 board.
0C02	Lamp16 Board x Type Failure - Board type y Detected
0C02	LAMP16 Type Error – Check LAMP16 board.
0C04	LAMP16 Output Error – Check LAMP16 board or wiring.
0C05	LAMP16 Output Error – Check LAMP16 board or wiring.
0C06	LAMP16 Internal Error – Check CPU board.
0C0A	Lamp Adjust Fail - Front panel lamp adjustment. EEPROM write failed.
0C0A	Lamp Adjusted - Lamp was adjusted from front panel. Successful write to EEPROM.
0C0A	Lamp Mode Reset Option CLEARED
0C0A	Lamp Mode Reset Option SET
0D0#	CODER Board Information
0D01	CODER Board x - Echo Error
0D01	CODER Echo Error – Check Cab CODER board.
0D02	CODER Board x - Type Error

CODE	DESCRIPTION
0D02	CODER Type Error – Check Cab CODER board.
0D04	CODER Hardware Failure – Check Cab CODER board.
0D05	CODER Hardware Failure – Check Cab CODER board.
0D06	CODER Internal Error – Check CPU board.
0E0#	NviN32OUT32 Board x - Information
0E01	NVIN32OUT32 Board x - Echo Error
0E01	NVIN32OUT32 Echo Error – Check NVIN32OUT32 board.
0E02	NVIN32OUT32 Board x - Type Error
0E02	NVIN32OUT32 Type Error – Check NVIN32OUT32 board.
0E06	NVIN32OUT32 Internal Error – Check CPU board.
0F0#	NVOUT12 Board Information
0F01	NVOUT12 Board x - Echo Error
0F01	NVOUT12 Echo Error – Check NVOUT12 board.
0F02	NVOUT12 Board x - Type Error
0F02	NVOUT12 Type Error – Check NVOUT12 board.
0F06	NVOUT12 Internal Error – Check CPU board.
100#	TRACK Board Information
1001	TRACK Board x - Echo Error
1001	TRX.TRACK Echo Error – Check TRX.TRACK board.
1002	TRACK Board x - Type Error
1002	TRX.TRACK Type Error – Check TRX.TRACK board.
1005	TRX.TRACK Hardware Failure – Check TRX.TRACK board.
1006	TRX.TRACK Internal Error – Check CPU board.
12##	Shared Ram Information
1201	Shared Ram Link Down
1201	Vehicle Control Shared RAM error – Check application.
13##	Serial link and port information
1301	Serial Link Internal Error – Check CPU board.
1302	Serial Link Internal Error – Check CPU board.
1303	Serial Link Internal Error – Check CPU board.
1304	Serial Link Internal Error – Check CPU board.

CODE	DESCRIPTION
1305	Serial Link Internal Error – Check CPU board.
1306	Serial Link Internal Error – Check CPU board.
1307	Serial Link Internal Error – Check CPU board.
1308	Serial Link Internal Error – Check CPU board.
1309	Serial Link Internal Error – Check CPU board.
130A	Serial Link Internal Error – Check CPU board.
130B	Serial Link Internal Error – Check CPU board.
130C	Serial Link Internal Error – Check CPU board.
130D	Serial Link Internal Error – Check CPU board.
130E	Serial Link Internal Error – Check CPU board.
1313	Serial Link Internal Error – Check CPU board.
1314	Serial Link Internal Error – Check CPU board.
1315	Serial Link Internal Error – Check CPU board.
1316	Serial Link Internal Error – Check CPU board.
1317	Serial Link Internal Error – Check CPU board.
1318	Serial Link Internal Error – Check CPU board.
1319	Serial Link Internal Error – Check CPU board.
131C	Serial Link Internal Error – Check CPU board.
131D	Serial Link Internal Error – Check CPU board.
131E	Serial Link Internal Error – Check CPU board.
1324	Serial Link Internal Error – Check CPU board.
1327	Serial Link Internal Error – Check CPU board.
14##	GENISYS master: information
1407	Serial Link Internal Error – Check CPU board.
140B	Serial Link Internal Error – Check CPU board.
140F	Serial Link Internal Error – Check CPU board.
1410	Serial Link Internal Error – Check CPU board.
1411	Serial Link Internal Error – Check CPU board.
1419	Serial Link Internal Error – Check CPU board.
141E	Serial Link Internal Error – Check CPU board.
141F	Serial Link Internal Error – Check CPU board.
1420	Serial Link Internal Error – Check CPU board.
1421	Serial Link Internal Error – Check CPU board.
1422	Serial Link Internal Error – Check CPU board.
1424	Serial Link Internal Error – Check CPU board.

CODE	DESCRIPTION
1426	Serial Link Internal Error – Check CPU board.
1428	Serial Link Internal Error – Check CPU board.
142A	Serial Link Internal Error – Check CPU board.
15##	GENISYS slave: information
1507	Serial Link Internal Error – Check CPU board.
150B	Serial Link Internal Error – Check CPU board.
150F	Serial Link Internal Error – Check CPU board.
1511	Serial Link Internal Error – Check CPU board.
1512	Serial Link Internal Error – Check CPU board.
151E	Serial Link Internal Error – Check CPU board.
151F	Serial Link Internal Error – Check CPU board.
1520	Serial Link Internal Error – Check CPU board.
1523	Serial Link Internal Error – Check CPU board.
1524	Serial Link Internal Error – Check CPU board.
1526	Serial Link Internal Error – Check CPU board.
1527	Serial Link Internal Error – Check CPU board.
1529	Serial Link Internal Error – Check CPU board.
152A	Serial Link Internal Error – Check CPU board.
16##	MICROLOK master: information
160C	Serial Link Internal Error – Check CPU board.
1610	Serial Link Internal Error – Check CPU board.
1611	Serial Link Internal Error – Check CPU board.
1613	Serial Link Internal Error – Check CPU board.
1619	Serial Link Internal Error – Check CPU board.
161E	Serial Link Internal Error – Check CPU board.
161F	Serial Link Internal Error – Check CPU board.
1620	Serial Link Internal Error – Check CPU board.
1624	Serial Link Internal Error – Check CPU board.
1626	Serial Link Internal Error – Check CPU board.
162A	Serial Link Internal Error – Check CPU board.
17##	MICROLOK slave: information
170B	Serial Link Internal Error – Check CPU board.
170C	Serial Link Internal Error – Check CPU board.
1713	Serial Link Internal Error – Check CPU board.
1717	Serial Link Internal Error – Check CPU board.

CODE	DESCRIPTION
1719	Serial Link Internal Error – Check CPU board.
171A	Serial Link Internal Error – Check CPU board.
171B	Serial Link Internal Error – Check CPU board.
1724	Serial Link Internal Error – Check CPU board.
1726	Serial Link Internal Error – Check CPU board.
172A	Serial Link Internal Error – Check CPU board.
18##	MII Peer - information
1C01	NV.OUT32 I/O Board Echo Error - Replace designated NV.OUT32 board.
1C01	NVOUT32 Board x - Echo Error
1C02	NV.OUT32 I/O Board Type Error - Check address switches on all physical I/O boards against application program listing and/or connector labels. If the problem persists replace the designated NV.OUT32 board.
1C02	NVOUT32 Board x - Type Error
1C04	NV.OUT32 Delivery Error - Replace designated NV.OUT32 board.
1C04	NVOUT32 Board information
1D##	NVIN32 Board information
1D01	NV.IN32 I/O Board Echo Error - Replace designated NV.IN32 board.
1D01	NVIN32 Board x - Echo Error
1D02	NV.IN32 I/O Board Type Error - Check address switches on all physical I/O boards against application program listing and/or connector labels. If the problem persists replace the designated NV.IN32 board.
1D02	NVIN32 Board x - Type Error
1D06	NV.IN32 Driver Internal Error - Replace CPU board; report this problem to ASTS USA.
1E##	NVIN32OUT16 Board information
1E01	NV.IN32.OUT16 I/O Board Echo Error - Replace designated NV.IN32.OUT16 board.
1E01	NVIN32OUT16 Board x - Echo Error
1E02	NV.IN32.OUT16 I/O Board Type Error - Check address switches on all physical I/O boards against application program listing and/or connector labels. If the problem persists replace the designated NV.IN32.OUT16 board.
1E02	NVIN32OUT16 Board x - Type Error

CODE	DESCRIPTION
1E03	NV.IN32.OUT16 I/O Input Error - Replace designated NV.IN32.OUT16 board.
1E06	NV.IN32.OUT32 Driver Internal Error - Replace CPU board; report this problem to ASTS USA.
1E1#	IN4OUT4 Board Information
1E11	IN4OUT4 Board x - Echo Error
1E12	IN4OUT4 Board x - Type Error
1E2#	ASES Board information
1E21	ASES Board x - Echo Error
1E22	ASES Board x Type Error
1E8A	ASES Board x Channel y - No Telegram Selected
1F0#	E CODE Board information
1F01	E CODE Board x - Echo Error
1F02	E CODE Board x - Type Error
1F1#	IN4OUT2 Board Information
1F11	IN4OUT2 Board x - Echo Error
1F12	IN4OUT2 Board x - Type Error
1F2#	COLOR Board information
1F21	COLOR Board x - Echo Error
1F22	COLOR Board x - Type Error
1F3#	SEARCH Board information
1F31	SEARCH Board x - Echo Error
1F32	SEARCH Board x - Type Error
1F8#	E CODE Board information
1FC#	E CODE Board x information
4240	Unsupported Diagnostic Port Interrupt - Replace the CPU board; report this warning to ASTS USA.
4440	Task Execution Time Warning - This warning is informational and indicates that the unit may be slow to respond under some circumstances; consult with ASTS USA if slowness is observed.
4504	Numeric Value Out of Range - Check application program.
4702	Application Math Error in Numeric or Boolean Expression - Check application program.



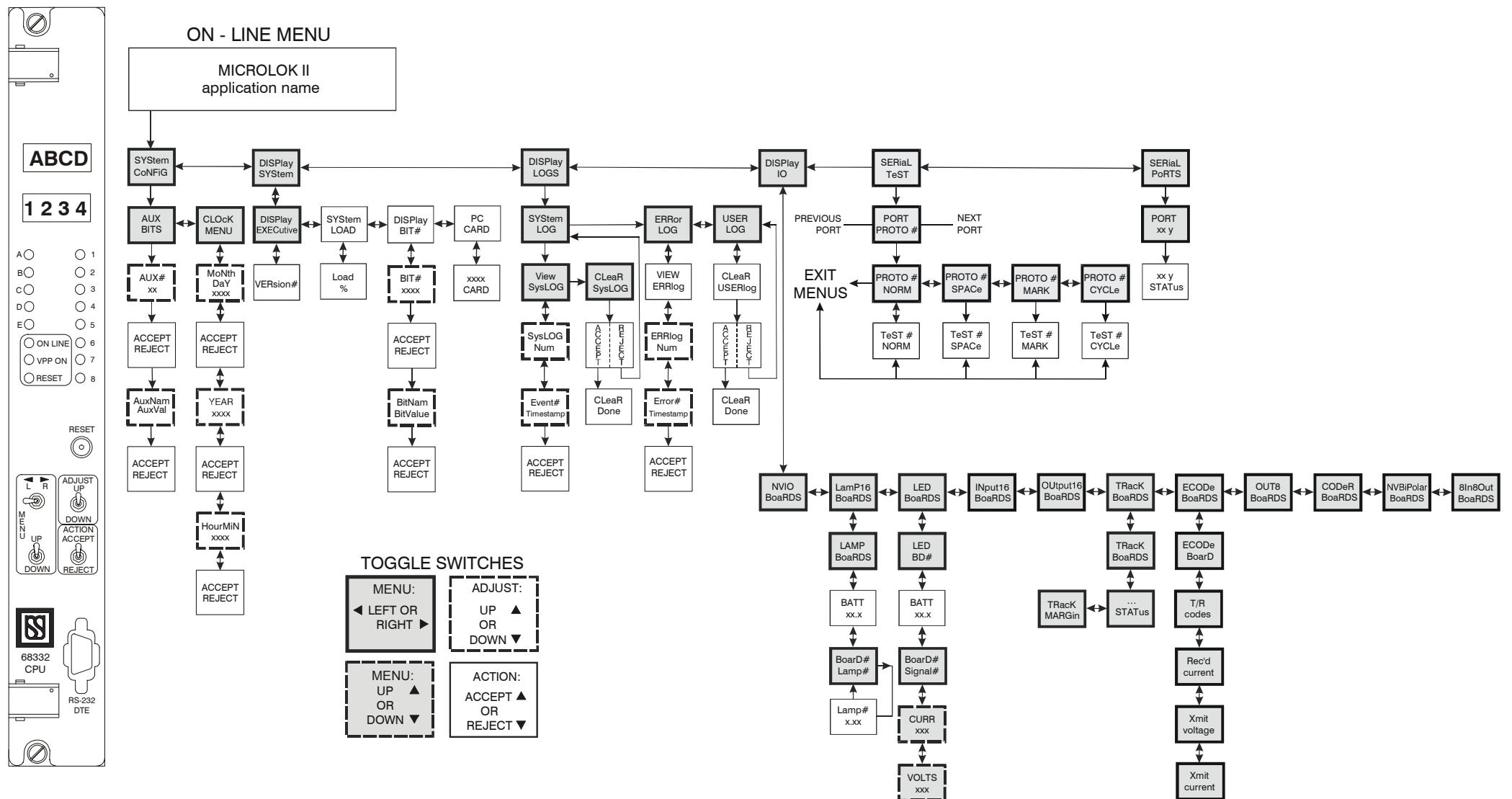


Figure 15-1. MICROLOK II CPU Menu Hierarchy

(Capital Letters Indicate the Letters Displayed on the Alphanumeric CPU Displays)

16 RAIL TEAM AND TECHNICAL SUPPORT

The Rapid Action Information Link (RAIL) team created in 1996 serves the technical needs of current and potential ASTS USA customers.

Convenient 24-hour access and a rapid resolution to customer problems are the trademarks of this organization. The RAIL team, which is staffed primarily by ASTS USA product and application engineers, is ready to assist and resolve technical issues concerning this or any ASTS USA product.

Direct any questions regarding the contents of this service manual to the RAIL team by telephone at 1-800-652-7276 or through Internet e-mail at, railteam@switch.com.



17 NOTES

Notes



End of Guide