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IRISET

S 18  
**ELECTRONIC  
INTERLOCKING**



Indian Railways Institute of  
Signal Engineering and Telecommunications  
SECUNDERABAD - 500 017



## S 18

### ELECTRONIC INTERLOCKING

**VISION:** TO MAKE IRISET AN INSTITUTE OF INTERNATIONAL REPUTE, SETTING IT's OWN STANDARDS AND BENCHMARKS

**MISSION:** TO ENHANCE QUALITY AND INCREASE PRODUCTIVITY OF SIGNALLING & TELECOMMUNICATION PERSONNEL THROUGH TRAINING

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## **Reference Books**

1. Signal Engineering Manual – I
2. Signal Engineering Manual – II
3. OEM EI Manuals
4. RDSO Policy circulars and EI Specifications

## Abbreviations

BRC	- Bonding Ring Conductor
CBN	- Common Bonding Network
CCIP	- Control Cum Indication Panel
COTS	- Commercially OFF The Shelf
CRC	- Cyclic Redundancy Check
CT Racks	- Cable Termination Racks
EMC	- Electro Magnetic Compatibility
EMI	- Electro Magnetic Interference
EPROM	- Erasable Programmable Read Only Memory
FAT	- Factory Acceptance Test
FMEA	- Failure Modes and Effects Analysis
MEEB	- Main Equipotential Earth Busbar
MTBF	- Mean Time Between Failure
MTTR	- Mean Time To Repair
NI	- Non Interlocking
OFC	- Optical Fiber Cable
PCB	- Printed Circuit Board
RAM	- Random Access Memory
RCC	- Route Control Chart
RI Card	- Read Interface Card
RO Card	- Relay Output Card
ROM	- Read Only Memory
SAT	- Site Acceptance Test
SEEB	- Sub Equipotential Earth Busbar
SIL	- Safety Integrity Level
SIP	- Signal Interlocking Plan
SQAP	- Software Quality Assurance Plan
ST	- Selection Table
TMS	- Total Management System
VDU	- Visual Display Unit
VPIM	- Vital Parallel Input Module
VROM	- Vital Relay Output Module
WESTRACE	- Westinghouse Train Radio and Advanced Control Equipment



# CHAPTER 1

## INTRODUCTION

### 1.1 INTRODUCTION TO ELECTRONIC INTERLOCKING

The era of interlocking had started with mechanical lever frames. As the size of yards & train movements increased, the size of lever frames also had increased. These lever frames not only increased in size, occupying more space but also necessitated intensive maintenance. With the advent of Electro-mechanical relays, these lever frames gave way to relay interlocking based installations. This development resulted in relatively faster operation, fail safety in operation and reduced the size of buildings required for the housing of interlocking installations. With further increase in traffic and expansion of railway network, large number of Relay based Interlocking installations were commissioned.

Relay based Interlocking installations use Electro-magnetic relays requiring complex wiring and inter-connections. The wiring diagrams for such installations run into hundreds of sheets. Individual relays, wiring and interconnections along with thousands of soldered joints are required to be physically examined and certified. This exercise requires traffic blocks of long durations and large manpower to manage the traffic. Even for remodelling of small yard like addition of a loop line, all the above activities are required to be done.

With development of modern fault tolerant and fail safety techniques, electronics and particularly microprocessors have found acceptance in the area of railway signalling world over. Railways in advanced countries of Europe, North America & Australia have gone for large scale introduction of microprocessor based Electronic Interlocking systems (EI). These systems occupy considerably less space, consume less power, more reliable, easy to install and easy to maintain. Also, initial commissioning and modifications on account of yard remodelling can be carried out in less time with less manpower.

EI is a microprocessor based system which controls Points, Signals, Level crossing gates etc, by centralized operation through Control Cum Indication Panel (CCIP) or Visual display Unit (VDU).

Based on a proposal for development of Electronic Interlocking System, as submitted by IIT Delhi to DOE, a project was initiated at IIT Delhi in July 1983. Two Officers from Railways were posted on this project to IIT, Delhi. Two industries (M/s DCM & CGL) were also associated in development and fabrication of the prototype. A design of the system was evolved in March 1985. The design was evaluated through software simulation at IIT, Delhi and a prototype based on this design was fabricated in 1987. RDSO and DOE jointly funded the project for design, development and prototype fabrication. The prototype was installed at Brar Square Station of Northern Railway for field evaluation. Based on field trial results, it was decided by Railway Board to manufacture four engineering models incorporating necessary improvements. Thereafter, design and fabrication of EI Mark-II system was taken up by RDSO in association with IIT, Delhi.

### 1.2 PURPOSE, ROLE, NECESSITY OF EI

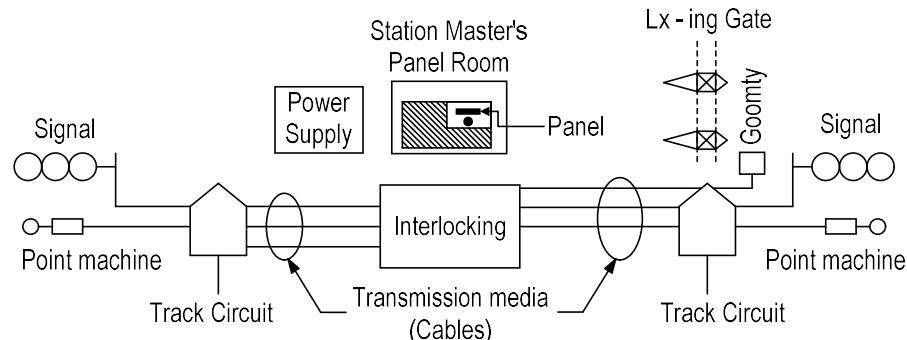


Fig 1.2 Basic Railway Interlocking diagram

### **1.2.1 Limitations of RRI**

A typical RRI installation requires:

- (a) Thousands of relays
- (b) Complex inter relay wiring
- (c) Hundreds of sheets of wiring diagram
- (d) Large traffic blocks required during initial installation and yard remodelling.

### **1.2.2 Need of Electronic Interlocking**

To overcome the limitations of mechanical and relay based interlocking systems, microprocessor based electronic interlocking systems have been introduced. They are more reliable, with less no. of relays, less power consumption and ease of installation and maintenance.

All the functions such as signals, points, track circuits etc. represent one bit memory element in electronic interlocking storage and logic processing of these bits ensure interlocking among the functions.

## **1.3 ADVANTAGES OF ELECTRONIC INTERLOCKING SYSTEM OVER RELAY INTERLOCKING**

- (a) Ease in installation and maintenance
- (b) Any yard layout changes with minimum non interlocking (NI) period
- (c) Simpler and faster operation with visual display units
- (d) Reduction in cable requirement
- (e) Inbuilt event logging and diagnostics
- (f) High Reliability and Availability
- (g) Remote monitoring and controlling of signaling functions
- (h) Centralized traffic control and Train Management System

#### 1.4 POLICY ON TYPE OF INTERLOCKING TO BE ADOPTED:

Board has decided the following policy to be adopted on IR vide Board's letter Nos. 2003/Sig/G/5 dt. 28-04-2016.

Sl. No	Type of Station	Avg. No. of Routes	Type of Interlocking to be provided
1	<ul style="list-style-type: none"> <li>a) "C" class Station</li> <li>b) Mid-section Interlocked LC gates</li> <li>c) IBS/IBH</li> <li>d) Stations on Double Line section without loop and with one emergency X-over and/or siding</li> <li>e) Stations on single line Sections with one loop</li> <li>f) Automatic Block Signalling with/without Mid-Section Interlocked LC gate</li> </ul>	Up to 10	Electronic Interlocking
2	Way-Station & Small Junction Stations	10 to 50 routes	Electronic Interlocking linked to Signal Control centre if required
3	Big stations and major Junction stations	50 to 500 routes	Electronic Interlocking with Distributed Architecture and/or Object Controllers
4	Very large stations/Junction Stations	More than 500 routes	Route Relay Interlocking with metal to metal type relays OR Electronic Interlocking with Distributed Architecture and Object Controllers

\* \* \*

## CHAPTER 2

### ELECTRONIC INTERLOCKING SYSTEM

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#### 2.1 BLOCK DIAGRAM

Electronic Interlocking System is a microprocessor based system. It consists of CPU (logic processor), Object controller (Input output gatherer), CCIP / VDU interface and maintenance terminal. The system diagram is as

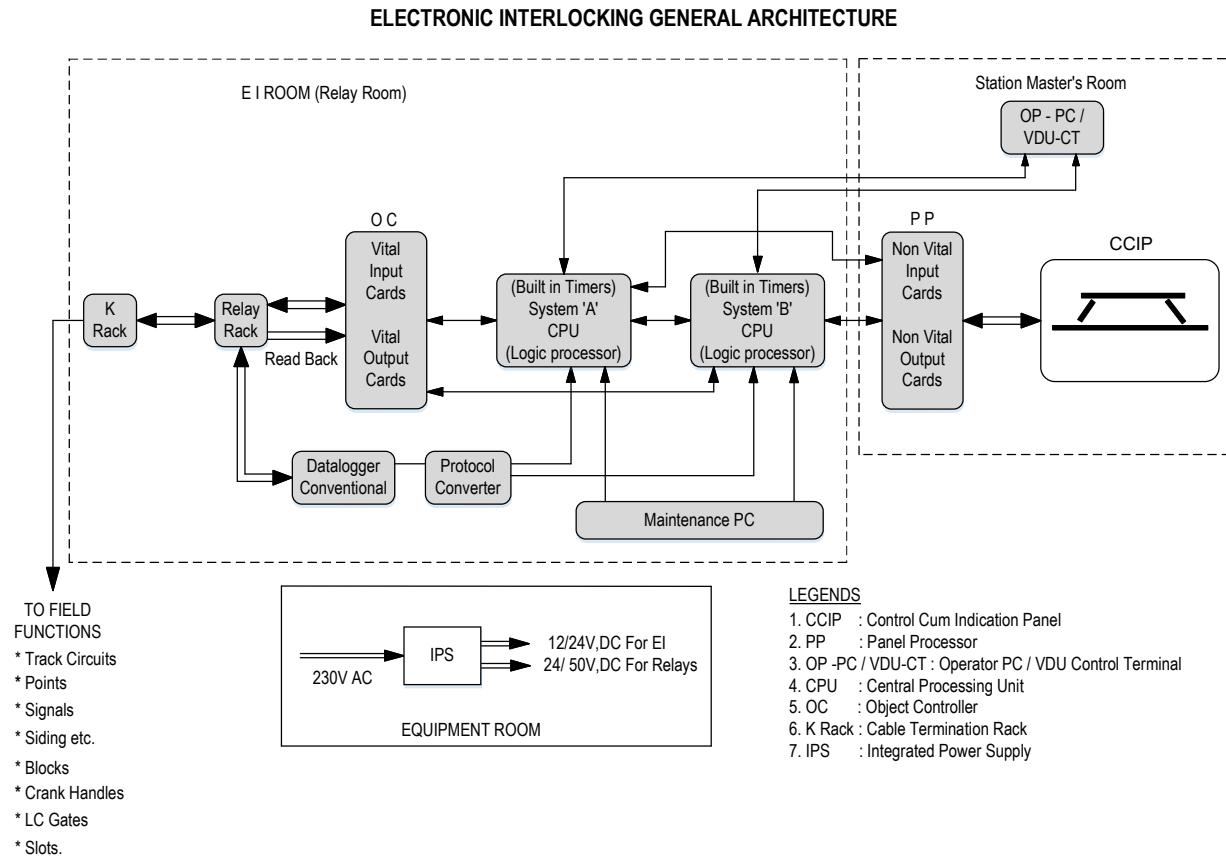


Fig 2.1 General Block diagram of EI

## 2.2 CLASSIFICATION OF FUNCTIONS

The Signalling functions are classified as Input and Output functions:

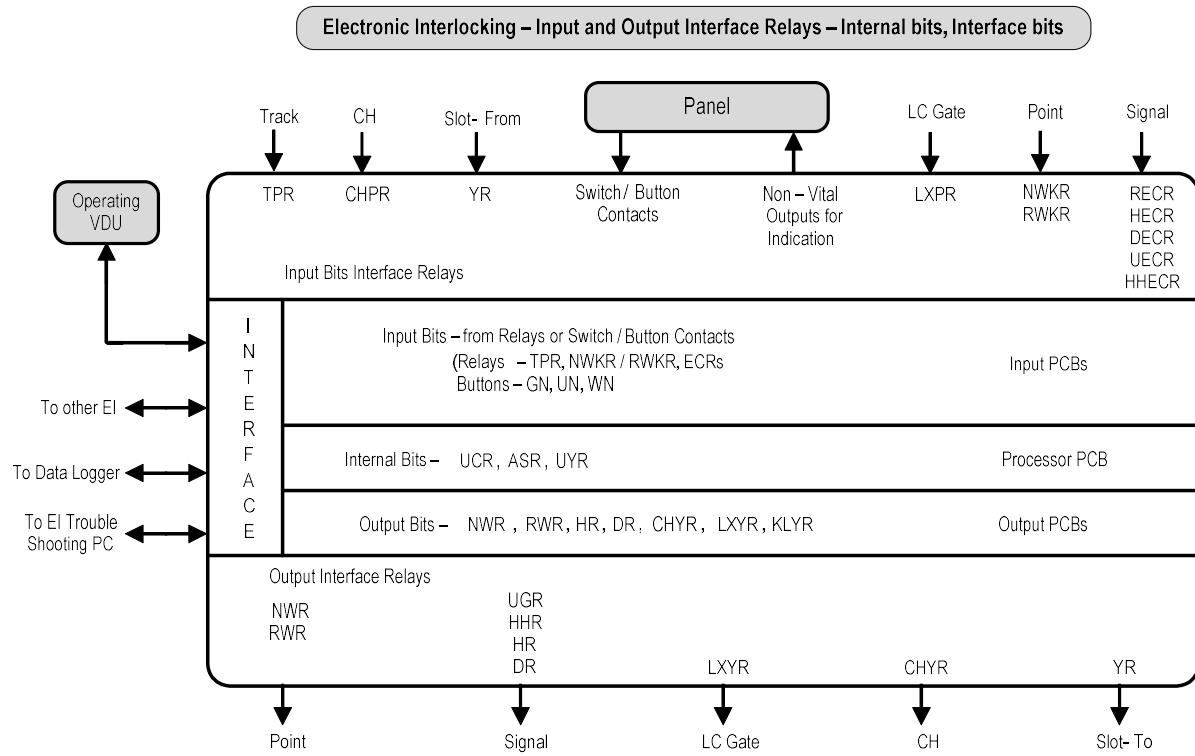


Fig 2.2 Electronic Interlocking Input and Output Interface Relays

- (a) Input Functions : Track detection indications (TPRs, VRs), Point position indications (WKRs), Signal aspect indications (ECRs), Interlocked gate, Siding and Crank handle controls and Block line clear indication are considered as vital input functions.

Panel button/ knob/ key controls or VDU commands are considered as Non-vital input functions.

- (b) Output Functions : Signal controls (HRs, DRs, UHR/UGR), Point controls (NWRs/ RWRs), Slot controls (YRs/ CHYRs/LXYRs/KLYRs) are considered as vital output functions.

All panel/ VDU indications, alarms, counters are considered as Non-vital output functions.

- (c) Read back inputs : Apart from above input output functions, the vital output functions are read back as inputs to the system for the purpose of ensuring integrity of the vital output commands generated by CPU.

- (d) Input Cards : These are printed circuit Boards (PCB's). Status of all the field functions, through concerned relay contacts, is connected to input cards via terminals or tag blocks. These input cards are named as vital Input card / Relay Input card / Read interface cards (RI card).

Panel controls are connected to Input cards via terminals or tag blocks. These input cards are named as Non-vital Input cards.

The No of inputs per Input card will vary from make to make. The total number of inputs will depend on the yard layout.

- (e) Output Cards : These are printed circuit Boards (PCB). Controls from output cards drive field functions through concerned relays. Output cards are generally named as vital output card / Relay output card (RO card)/ Relay Driver Card.

Panel indications, alarms and counters are driven by output cards via terminals or tag blocks. These output cards are named as Non-vital output cards. The No of outputs per output card will vary from make to make. The total number of outputs will depend on the yard layout.

- (f) CPU Card : Central Processing Unit (CPU) serves as Logic processor. It consists of microprocessor, RAM – Random accessible memory, ROM – Read only memory and EPROM – Erasable Programmable read only Memory.

There will be separate EPROM for Application software and Executive software.

The CPU receives commands from Panel /VDU and processes them as per the Application data stored in the EPROMs. It drives output field functions if the interlocking conditions are satisfied. It also drives requisite indications on the panel/ VDU.

### 2.3 WORKING PRINCIPLE OF EI SYSTEM

Station master on pressing entry exit buttons on the panel for taking of a particular signal, CPU reads this request. CPU processes the request by solving interlocking logic based on rules as given in route control chart. CPU drives concerned points to required position and further drives signal in the field provided interlocking conditions are satisfied. CPU receives the change of aspect of the concerned signal. CPU indicates the status on panel. On movement over the set route, CPU will drive the panel as and when the status changes.

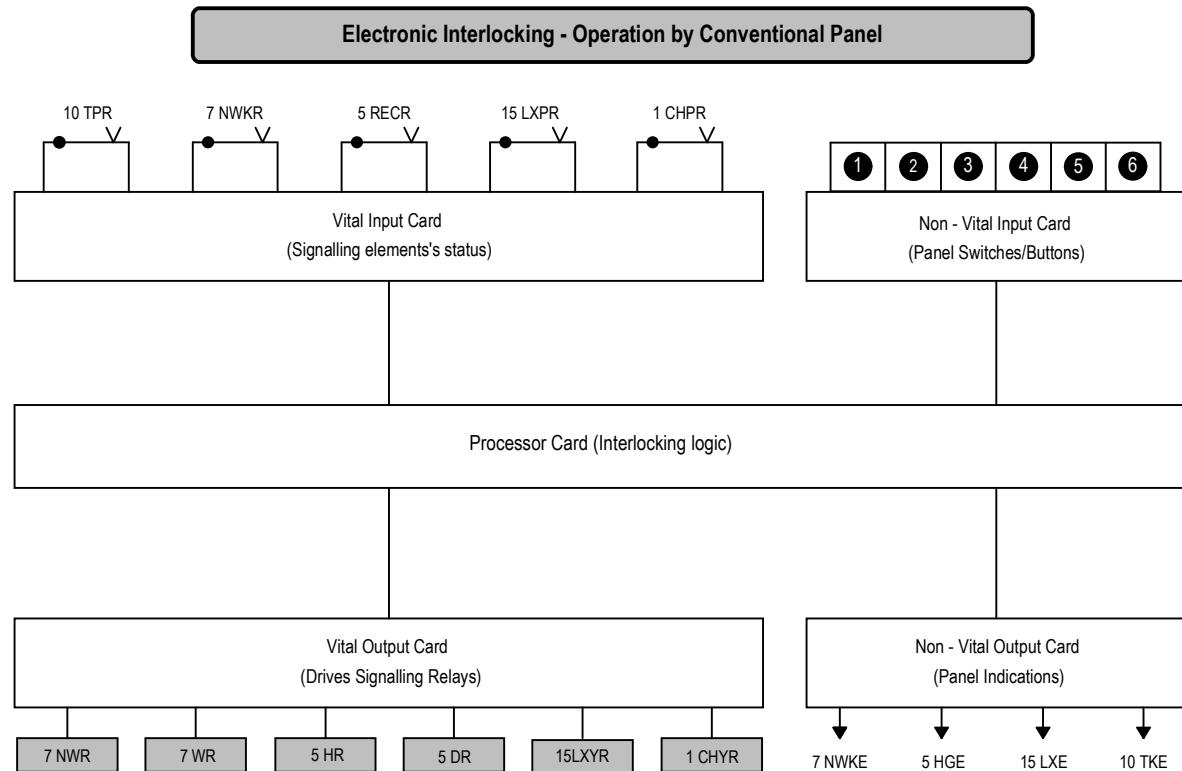


Fig 2.3 Electronic Interlocking Operation by Conventional panel

Alternately the operations can be performed from VDU

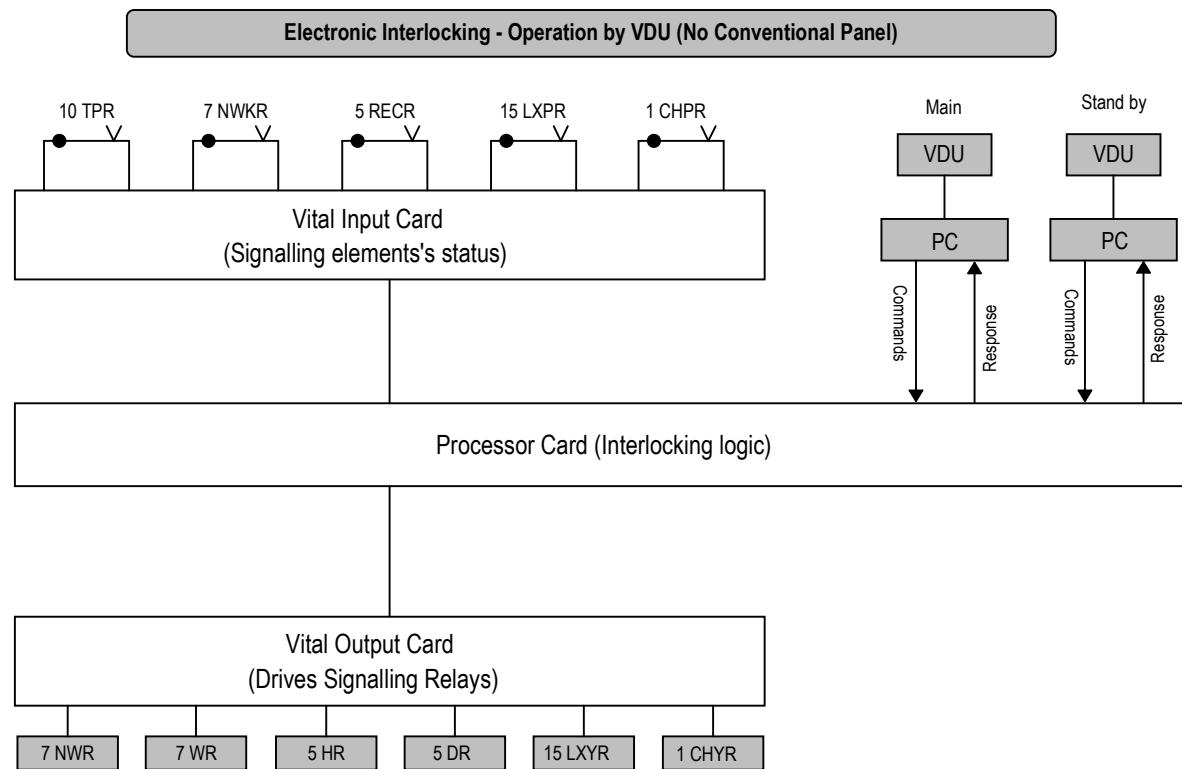


Fig 2.4 Electronic Interlocking Operation by VDU

\* \* \*

## CHAPTER 3

### CONFIGURATION OF ELECTRONIC INTERLOCKING SYSTEM

**3.1** Electronic interlocking systems are available in various configurations based on redundancy, architecture and standby.

#### **3.2 CLASSIFICATION BY REDUNDANCY**

Redundancy may be defined as the provision of more physical resources than required to perform a function if perfect reliability could be assumed

Depending on redundancy EI's are classified as :

- (a) Software Redundant.
- (b) Hardware Redundant.

#### **3.3 CLASSIFICATION BY ARCHITECTURE**

To ensure safety and reliability there are three approaches to the hardware (redundancy) design of EI's globally.

- (a) Single Hardware (processor) with diversity in software – (1 out of 1)
- (b) Dual Hardware with single/diverse software – (two out of two)
- (c) Majority voting system / Triple Modular redundancy – (two out of three)

##### **(a) SINGLE HARDWARE WITH DIVERSIFIED SOFTWARE (software redundant) :**

Single Hard ware with diversified Software

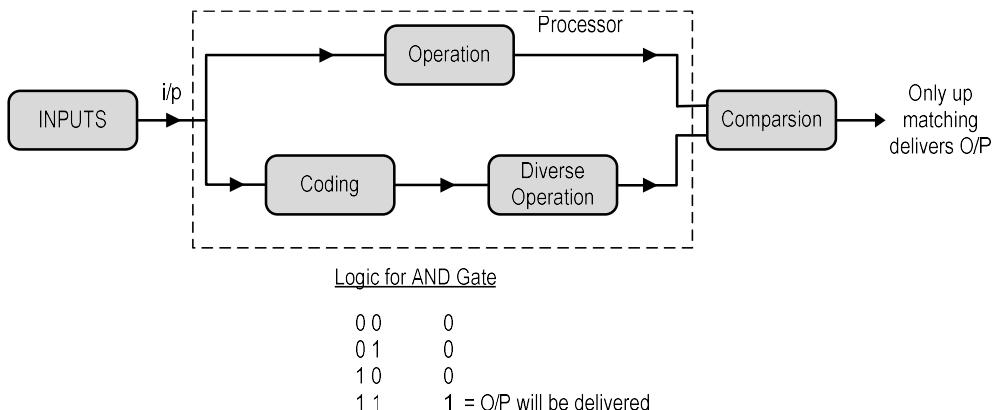


Fig 3.1 Single Hardware with diversified software

Ex : 1. MICROLOK - II US & S (M/S. ANSALDO)

2. M/s WESTRACE – Westinghouse Train Radio and Advanced Control Equipment (Now Name changed as M/s Siemens Rail Automation Private Limited)

With this configuration either hot standby with seamless changeover or warm standby with auto changeover arrangement is required (as per latest guide lines in future works only Hot Standby is to be used).

(b) HARDWARE REDUNDANCY – 2 out of 2 systems with single /diversified software:

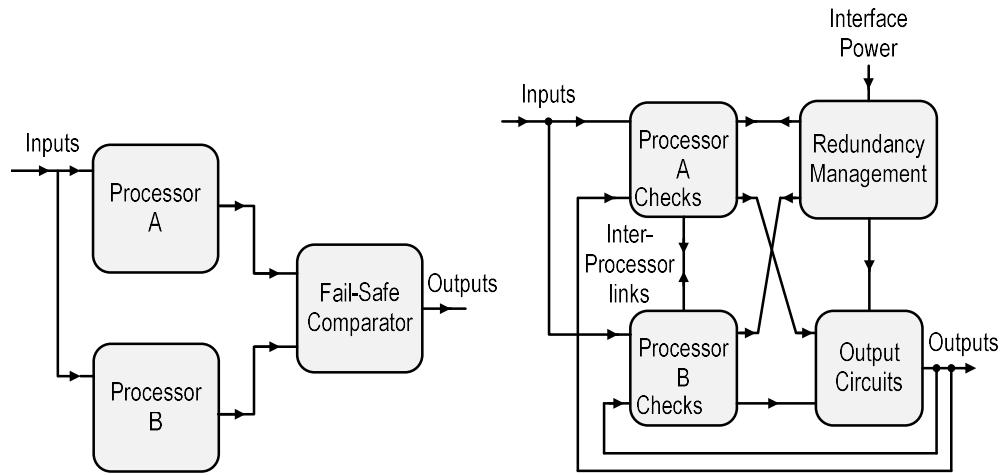


Fig 3.2 Duplication for Safety – Basic Concept

Fig 3.3 Duplication for Safety – Practical System

Ex: 1. MEI 633 (M/s Medha - EI)

2. VHLC (M/s GE - EI)

3. KYOSAN EI

(c) TRIPLE MODULAR REDUNDANCY - HARDWARE REDUNDANT - 2 OUT OF 3 SYSTEM

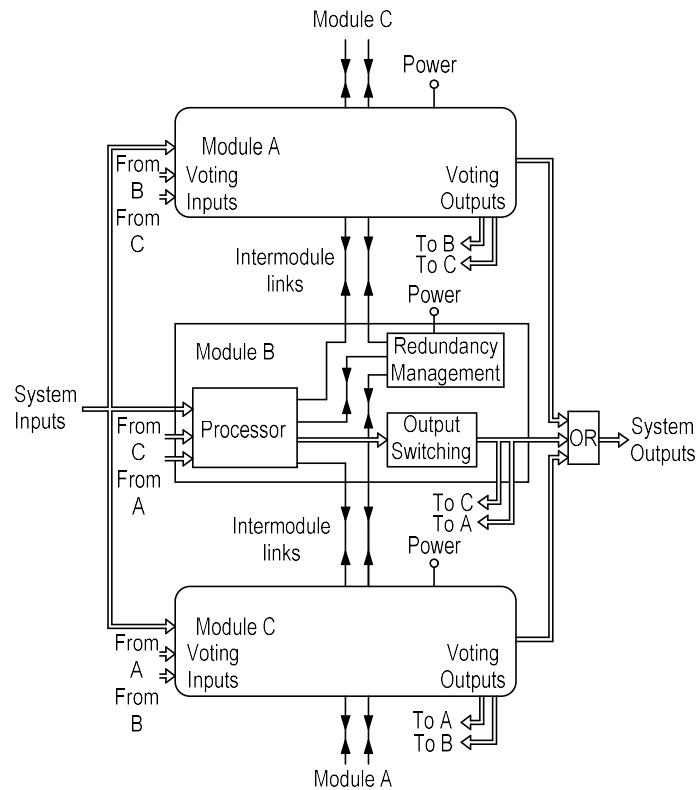


Fig 3.4 Triple modular redundancy – TMR (2 out of 3)

Ex : 1. ALSTOM – EI

2. SIMIS –W – SIEMENS

3. SICAS – SIEMENS

4. ESTWL90 – ALCATEL

In this TWO out of THREE, hardware is identical & system Software used may be identical or diverse.

### 3.3.1 Electronic Interlocking systems available on Indian Railways

- (a) Ansaldo-MLKII — 1 out of 1 – Hot / Warm standby.
- (b) Westrace- VLM6 — 1 out of 1 – Hot standby.
- (c) GE - VHLC — 2 out of 2 – Warm standby only.
- (d) Medha-MEI633 — 2 out of 2 – Hot standby only.
- (e) Kyosan-K5BMC — 2 out of 2 – Hot standby only.
- (f) AZD Praha- ESA 11-IR — 2 out of 2 – Hot standby only.
- (g) Westrace- MarkII — 2 out of 2 – Hot standby.

### 3.3.2 Criteria for the Selection of EI System

The main criteria for the selection of EI System is its reliability, availability, maintainability & safety apart from meeting full functional requirements.

The main features are:

- (a) System should meet functional requirements and have future expandability.
- (b) Meet the requirements of environmental conditions, electromagnetic interference, etc.
- (c) System should be user friendly and economical (example – object controller for yards).
- (d) System architecture should be such as to give very high overall availability while ensuring high degree of safety.
- (e) System validation to international standards to meet safety integrity level -SIL-4 (defined in CENELEC Standards).

To meet above main requirements, various architectures have been suggested in Para 7.1 of the specification No. RDSO/SPN/192-2005.

## 3.4 CLASSIFICATION OF STANDBY CONFIGURATIONS

Any Signal Interlocking System can be reliable only when it gives uninterrupted service .To achieves this objective, duplicate systems are provided. Separate CPU, Power Supply Boards are provided in duplicated systems. All the Vital and Non-vital boards may also be duplicated. Duplicated systems are identified as "SYSTEM-A" and "SYSTEM-B". When one system fails due to any reason, it is ensured that, the other system is available to take care of Station Interlocking. Normally there are three types of STANDBY concepts are employed for availability purpose.

In case of EI systems either Hot or Warm standby arrangements are used.

**Hot Standby arrangement :** In this arrangement both main and standby units run simultaneously Both the systems read Inputs independently and O/P data from online system gets mapped to standby system at regular intervals. Outputs will be driven by online system only.

Advantages: Due to Seamless changeover there is no down time during system changeover

Disadvantages: As both the systems are ON line always, during lightning surge both the systems may be damaged

**Warm Standby arrangement :** In this arrangement one system is ON line and another one is OFF line. Power is extended to ON line system only and it processes the input data and delivers outputs. When the ON line system fails, power supply is switched over to the standby system by means of an external auto changeover circuit and it starts delivering the outputs.

Advantages: Both the systems are not on at the same time, so probably surge may not affect the standby system.

- 1) There will be a down time when ever systems change over takes place. Hence Traffic interruption for about 3 to 5 minutes is inevitable..
- 2) The integrity of the OFF line system is not known unless it is switched on.

### 3.5 BLOCK DIAGRAMS OF VARIOUS AVAILABLE SYSTEMS IS GIVEN BELOW

(a) Single Hardware with diversified software



Fig 3.5 (a) Single processor without any standby

(b) Single processor with warm standby

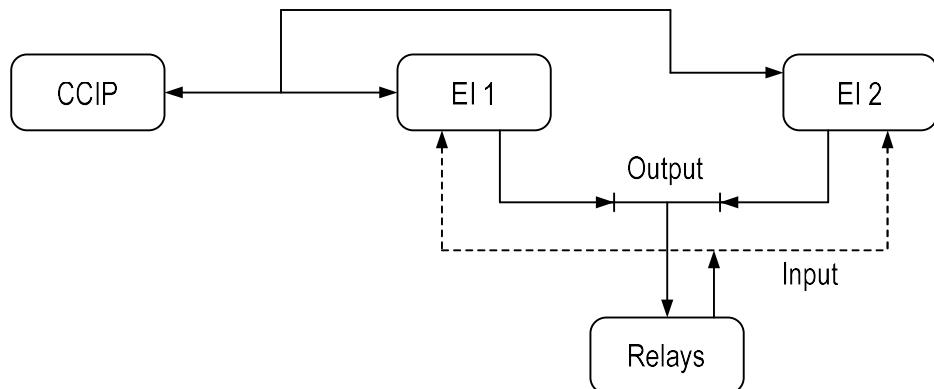


Fig 3.5 (b) Single processor with standby

(c) Single processor with hot standby

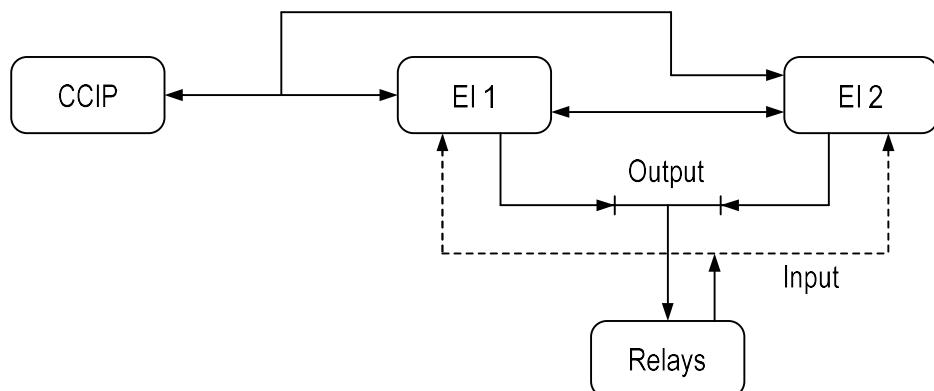


Fig 3.5 (c) Single processor with standby

(d) 2 out of 2 systems without standby

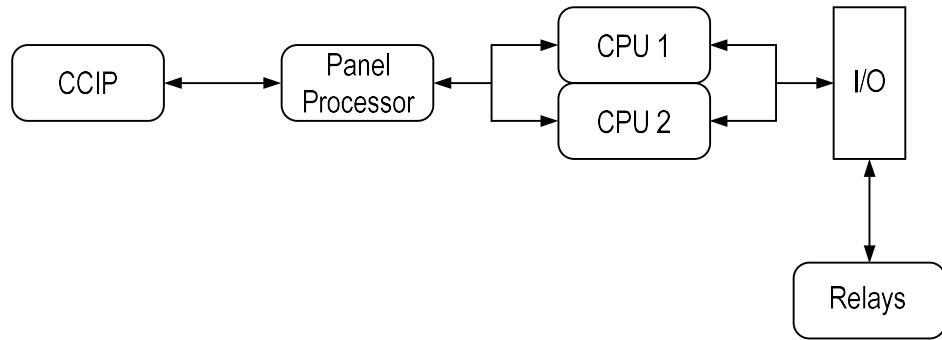


Fig 3.5 (d) 2 out of 2 without standby

(e) 2 out of 2 with warm standby

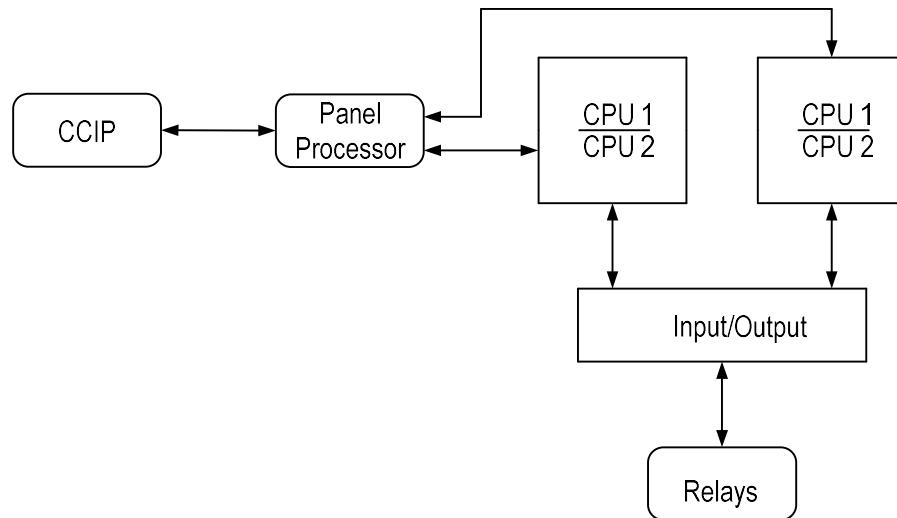


Fig 3.5 (e) 2 out of 2 with warm standby

(f) 2 out of 2 with hot standby

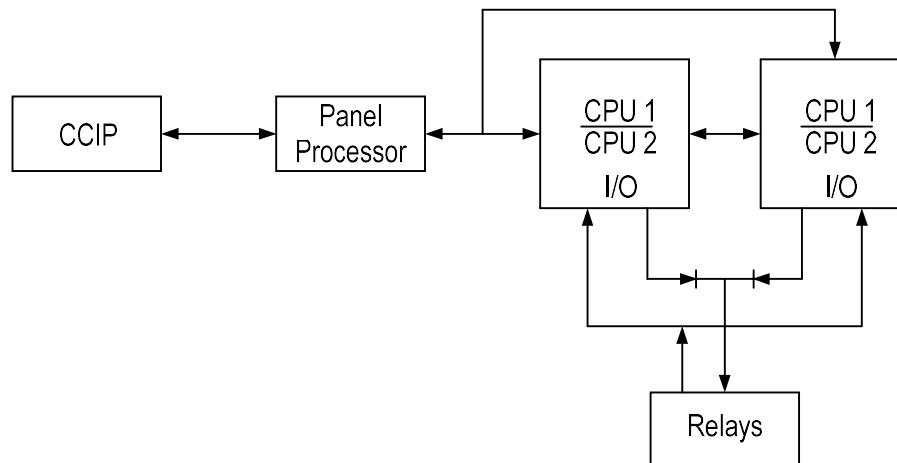


Fig 3.5 (f) 2 out of 2 with hot standby

(g) 2 out of 2 with object controllers (OC) and hot standby

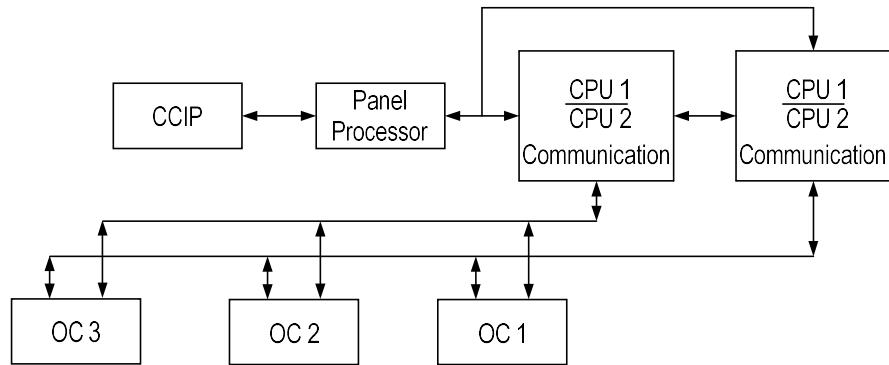


Fig 3.5 (g) 2 out of 2 with object controllers (OC) and hot standby

(h) Triple modular redundancy (TMR) 2 out of 3 systems

(i) TMR with relay interface

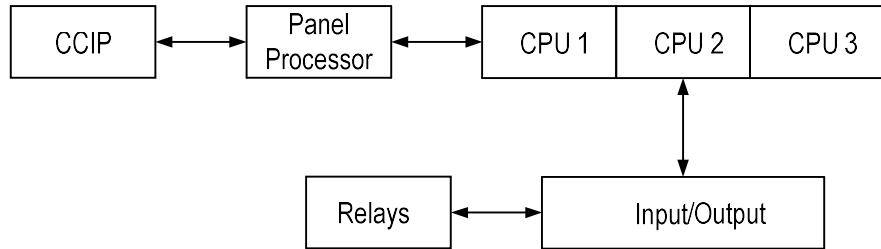


Fig 3.5 (h) (i) TMR with relay interface

(ii) TMR with object controllers

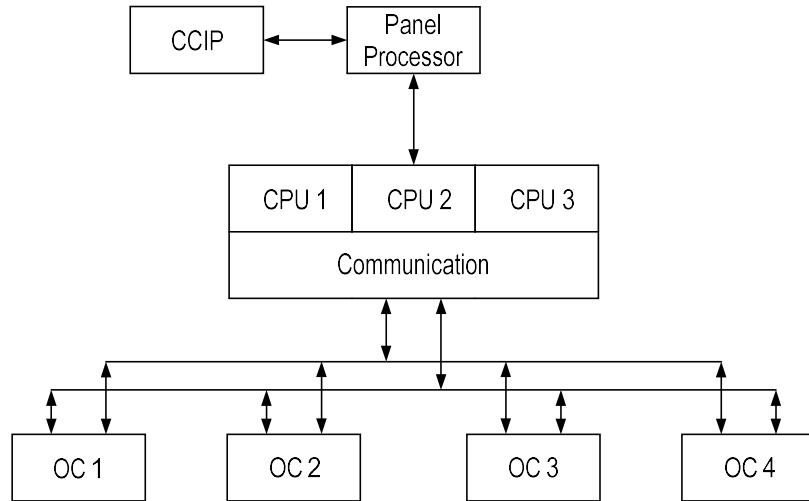


Fig 3.5 (h) (ii) TMR with object controllers

For medium size yards having routes more than 50, distributed interlocking architecture employing Object controllers in field near the signaling gears shall only be used.

\* \* \*

## **CHAPTER 4**

### **INSTALLATION OF ELECTRONIC INTERLOCKING SYSTEM**

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#### **4.1 DESIGN OF EI**

EI Design normally consists of

- (a) Interface Design.
- (b) Application Program Design.
- (c) VDU Software Design.

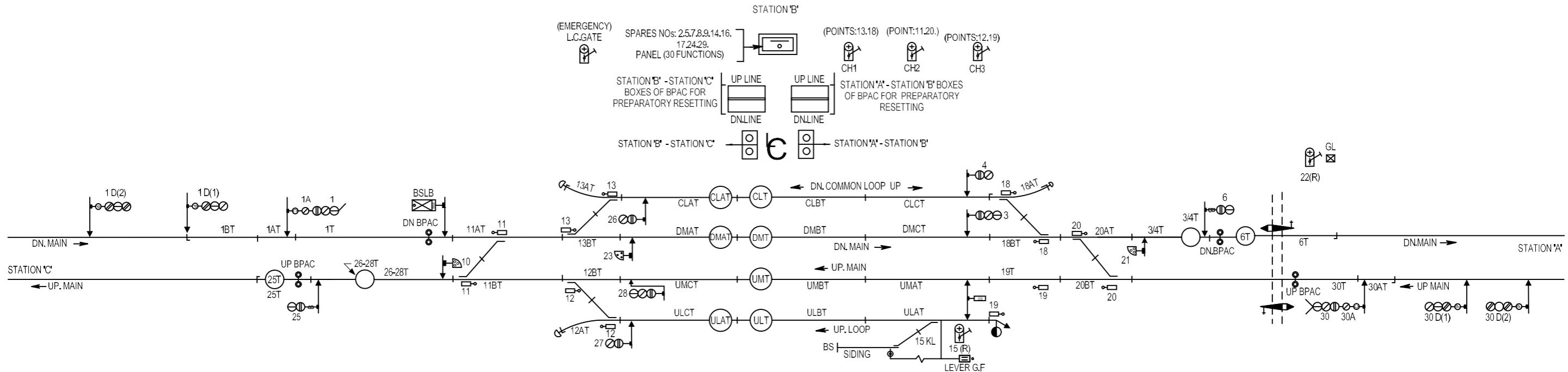
Pre-requisites for design of EI

- (a) Approved Signal Interlocking Plan.
- (b) Approved Front Plate Diagram.
- (c) Approved Route Control Chart/ Selection Table.
- (d) Power Supply scheme.
- (e) Relay room, SM room, Power Equipment Room layouts.
- (f) Details of any additional interlocking equipment to be interfaced with EI.

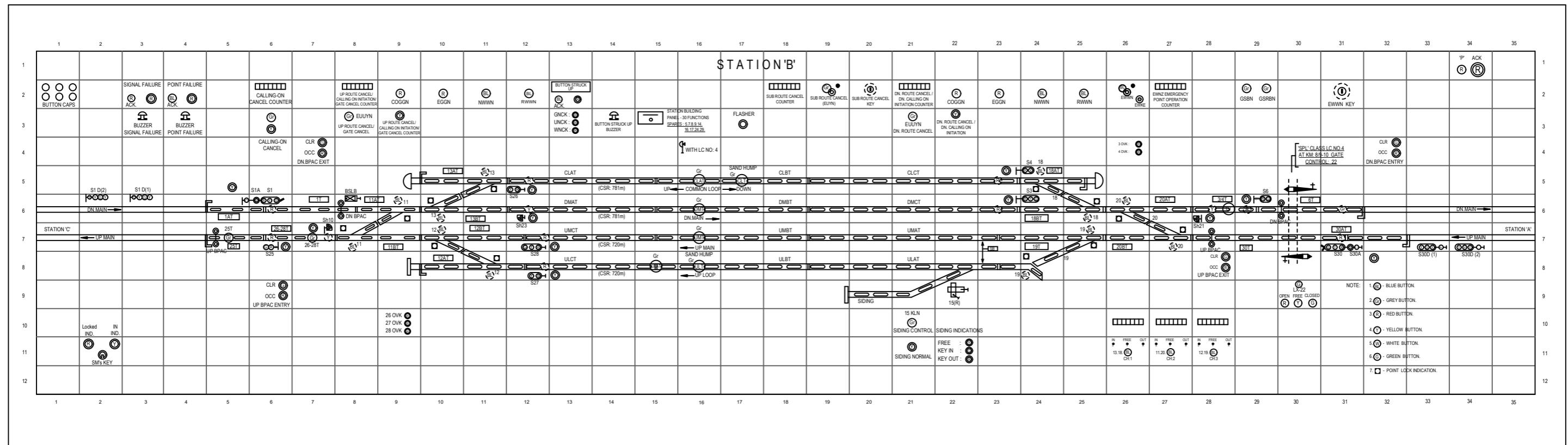
##### **4.1.1 Steps Involved in Interface Design**

- (a) Assessment of Vital and Non-vital I/O bits.
- (b) Assessment of Vital and Non-vital I/O boards.
- (c) Assessment of number of Card files/ Housings.
- (d) Preparation of System Configuration and Communication arrangement.
- (e) Calculation of No. of Relays, Relay Racks and Cable Termination (CT)Racks.
- (f) Calculation of No. of PCB Connector Assemblies and Terminals.
- (g) Interconnection of various racks and interlocking equipment.
- (h) Preparation of Manuscript of complete wiring diagram.
- (i) Power supply arrangement.

#### 4.1.2 Signal Interlocking Plans



## Yard diagram



## Front plate diagram

Fig 4.1 Signal Interlocking Plans

Table 4.1 Table of Control / Selection Table / Route Control Chart

Sn.	Sig No.	Leading to	Press Button		Approach locked by	Back locked by Tracks	Controlled by Tracks	Detect Points		Lock Signal/Route	Remarks
			Signal	Route				Normal	Reverse		
1	1D(2)	1D(1)	—	—	—	—	—	—	—	—	DG Controlled by 1D(1) DG/HHG with points 13 Normal
2	1D(1)	S1	—	—	—	—	—	—	—	—	DG Controlled by 1DG and HHG Controlled by 1HG
3	1	Common loop (Set to SH)	1	CLT	1AT,1BT	1T,11AT,13BT,13AT	1T, 11AT, 13BT,13AT,CLT,18AT	11,18	13	1A,21	Time Release 120 sec. 1UG,CH1,CH2,4RG
4	1	Common loop (Set to Main)	1	CLAT	1AT,1BT	1T,11AT,13BT,13AT	1T, 11AT, 13BT, 13AT, CLT, 18AT, 18BT, 20AT, 3/4T	11,20	13,18	1A,21	Time Release 120 sec. 1UG,CH1,CH2,4RG/HG
5	1	DN Main	1	DMT	1AT,1BT	1T,11AT,13BT	1T,11AT,13BT, DMT, 18BT,20AT,3/4T	11,13,18,20	-	1A,21	Time Release 120 sec. DG Controlled by 3DG,CH1,CH2,3RG/HG/DG
6	1A	Common loop	1 & COGGN	CLT	Dead Approach	—	1AT(Occupied)	11	13	1,4,21,(30A-CLT)	Time Release 240 sec. Approach cleared after 120 sec. CH1,CH2
7	1A	DN Main	1 & COGGN	DMT	Dead Approach	—	1AT(OCCUPIED)	11,13	-	1,3,4,21, (30,30A-CLT)	Time Release 240 sec. Approach cleared after 120 sec. CH1,CH2
8	3	DN Main	3	3/4T	DMT(1W,13N)	18BT,20AT	18BT,20AT,3/4T	18,20	-	(1A,10-DMT), 21,23	Time Release 120 sec. DG Controlled by6DG,CH1,CH2, 6RG/HG/DG
9	4	DN Main	4	3/4T	CLT	18AT,18BT, 20AT	18AT,18BT,20AT,3/4T	20	18	1A,(10-DMT), (10-CLT),21,26	Time Release 120 sec. CH1,CH2, 6RG/DG

Sn.	Sig No.	Leading to	Press Button		Approach locked by	Back locked by Tracks	Controlled by Tracks	Detect Points		Lock Signal/Route	Remarks
			Signal	Route				Normal	Reverse		
10	6	DN Main	6	6T	—	—	6T,DN.BPAC	20	—	21	Controlled by Station "A"- Station "B" Section Block Instrument and Controlled by LX-22,CH2
11	10	UP Loop	10	ULT	26-28T	11BT,12BT, 12AT	11BT,12BT,12AT	11	12	25,27, (30A-UMT), (30A-ULT), (30-ULAT)	Controlled by 15KL,CH2,CH3, Time Release 120 sec.
12	10	UP Main	10	UMT	26-28T	11BT,12BT	11BT,12BT	11,12	—	25,28,30,30A	Time Release 120 sec. CH2,CH3
13	10	DN Main	10	DMT	26-28T	11BT,11AT, 13BT	11BT,11AT,13BT	13	11	3,4,(21-DMT), 23, 25, (30,30A-CLT), (30A-UMT), (30A-ULT W 12R)	Time Release 120 sec. CH1,CH2
14	10	Common loop	10	CLT	26-28T	11BT,11AT, 13BT,13AT	11BT,11AT,13BT,13AT	-	11,13	4,(21-CLT),25, 26, (30CLAT), (30A-CLT), (30A-UMT), (30A-ULTW12R)	Time Release 120 sec. CH1,CH2
15	21	DN Main	21	DMT	3/4T	20AT,18BT	20AT,18BT	20,18	-	1,1A,3,6, (10-DMT),26	Time Release 120 sec. CH1,CH2
16	21	Common loop	21	CLT	3/4T	20AT,18BT, 18AT	20AT,18BT,18AT	20	18	1,1A,4,6, (10-CLT),26	Time Release 120 sec. CH1,CH2
17	23	UP Main	23	26-28T	DMT	13BT,11AT, 11BT	13BT,11AT,11BT	13	11	3,10,25, (30A-UMT), (30A-ULT W12R	Time Release 120 sec. CH1,CH2

Sn.	Sig No.	Leading to	Press Button		Approach locked by	Back locked by Tracks	Controlled by Tracks	Detect Points		Lock Signal/Route	Remarks
			Signal	Route				Normal	Reverse		
18	25	UP Main	25	25T	—	—	25T,UP,BPAC	—	—	10,23	Controlled by Station 'B'- Station 'C' Section Block Instrument
19	26	UP Main	26	26-28T	CLT	13AT, 13BT, 11AT, 11BT	13AT, 13BT, 11AT, 11BT, 26-28BT	12	11,13	4, 10, 21, (30A-CLT), (30A-UMT)	Time Release 120 sec. CH1,CH2,CH3,25RG/DG
20	27	UP Main	27	26-28T	ULT	12AT, 12BT, 11BT	12AT,12BT,11BT,26-28BT	11	12	10,(30A-ULT), (30A-UMT)	Controlled by 15KL,CH2,CH3,25RG/DG, Time Release 120 sec.
21	28	UP Main	28	26-28T	UMT, (S30W, 19N, 20N)	12BT, 11BT	12BT,11BT,26-28BT	11,12	-	10,(30A-UMT)	Time Release 120 sec. CH2,CH3,'DG' Controlled by 25DG,25RG/DG
22	30A	UP loop	30 & COGGN	ULT	Dead Approach	—	30AT (Occupied)	20,15	19	(10-CLT W 12R), (10-DMT W 12R), (10-UMT), (10-ULT), (23W12R), 27, 30	Time Release 240 sec. Approach cleared after 120 sec.,CH2,CH3, Controlled by LX-22,15KL
23	30A	UP Main	30 & COGGN	UMT	Dead Approach	—	30AT (Occupied)	19,20	-	10,23,26,27,28,30	Time Release 240 sec. Approach cleared after 120 sec.,CH2,CH3, Controlled by LX-22
24	30A	Common loop	30 & COGGN	CLT	Dead Approach	—	30AT (Occupied)	19	18,20	1A,(10-CLT), (10-DMT), (10-UMT),26,30	Time Release 240 sec. Approach cleared after 120 sec.,CH1,CH2,CH3, Controlled by LX-22
25	30	UP loop (Set to SH)	30	ULT	Dead Approach	30T, 20BT, 19T	30T, 20BT, 19T, ULT, 12AT	12,20,15KL	19	(10-UMT), 30A	Time Release 120 sec. 30UG,CH2,CH3,27RG, Controlled by LX-22,15KL
26	30	UP loop (Set to Main)	30	ULAT	Dead Approach	30T, 20BT, 19T	30T, 20BT, 19T, ULT, 12AT, 12BT, 11BT, 26-28T	20, 11, 15KL	19,12	10, 30A	Time Release 120 sec. 30UG,CH2,CH3,27RG/HG, Controlled by LX-22,15KL

Sn.	Sig No.	Leading to	Press Button		Approach locked by	Back locked by Tracks	Controlled by Tracks	Detect Points		Lock Signal/Route	Remarks
			Signal	Route				Normal	Reverse		
27	30	UP Main	30	UMT	Dead Approach	30T, 20BT, 19T	30T, 20BT, 19T, UMT, 12BT, 11BT, 26-28T	11, 12, 19, 20	-	10,30A	Time Release 120 sec. DG Controlled by 28DG,CH2,CH3,28RG/HG/DG, Controlled by LX-22
28	30	Common loop (Set to SH)	30	CLT	Dead Approach	30T, 20BT, 20AT, 18BT, 18AT	30T, 20BT, 20AT, 18BT, 18AT, CLT, 13AT	13, 19	18,20	1A, (10-DMT), (10-UMT), 30A	Time Release 120 sec. 30UG,CH1 ,CH2,CH3,26RG, Controlled by LX-22
29	30	Common loop (Set to Main)	30	CLAT	Dead Approach	30T, 20BT, 20AT, 18BT, 18AT	30T, 20BT, 20AT, 18BT, 18AT, CLT, 13AT, 13BT, 11AT, 11BT, 26-28T	19	11,18, 20,13	10,30A	Time Release 120 sec. 30UG,CH1, CH2, CH3, 26RG/ HG, Controlled by LX-22
30	30D(2)	30D(1)	—	—	—	—	—	—	—	—	DG Controlled by 30D(1) DG/HHG with points 19 Normal& 20 Normal
31	30D(1)	30	—	—	—	—	—	—	—	—	DG Controlled by 30DG,HHG Controlled by 30 HG

POINTS CONTROL TABLE

Sn.	Points No.	Track locked by	locked by Signals	Remarks
1	11	11AT,11BT	1,1A,10,23,26,27,28,(30W 19N20N) (30W19R12R)(30W20R13R)	CH2
2	12	12AT,12BT	(10W11N),26,27,28,(30W20N)	CH3
3	13	13AT,13BT	1,1A,(10W11R),23,26,(30W20R)	CH1
4	18	18AT,18BT	1,3,4,21,(30,30AW 20R)	CH1
5	19	19T	30,30A	CH3
6	20	20AT,20BT	(1W13N OR 18R),3,4,6,21,30,30A	CH2
7	15 KL	—	30, 30A, 27 (SH-10 W 12R)	—

#### 4.1.3 Assessment of Vital Inputs and Vital Outputs

To assess the Vital Inputs and outputs gather the following information from Interlocking plan of the station then list out the vital inputs and vital output bits referring to the Table No.4.2.

- (a) Type of signals (2A/3A/4A Aspect, Shunt, Calling-on etc...)
- (b) Slots
- (c) Points and Cross overs.
- (d) Motor operated points / Hand operated points.
- (e) Level Crossings, Siding Control and Crank Handles.
- (f) Track circuits
- (g) AFTCs.
- (h) Axle counters.
- (i) Type of block working with adjacent stations.

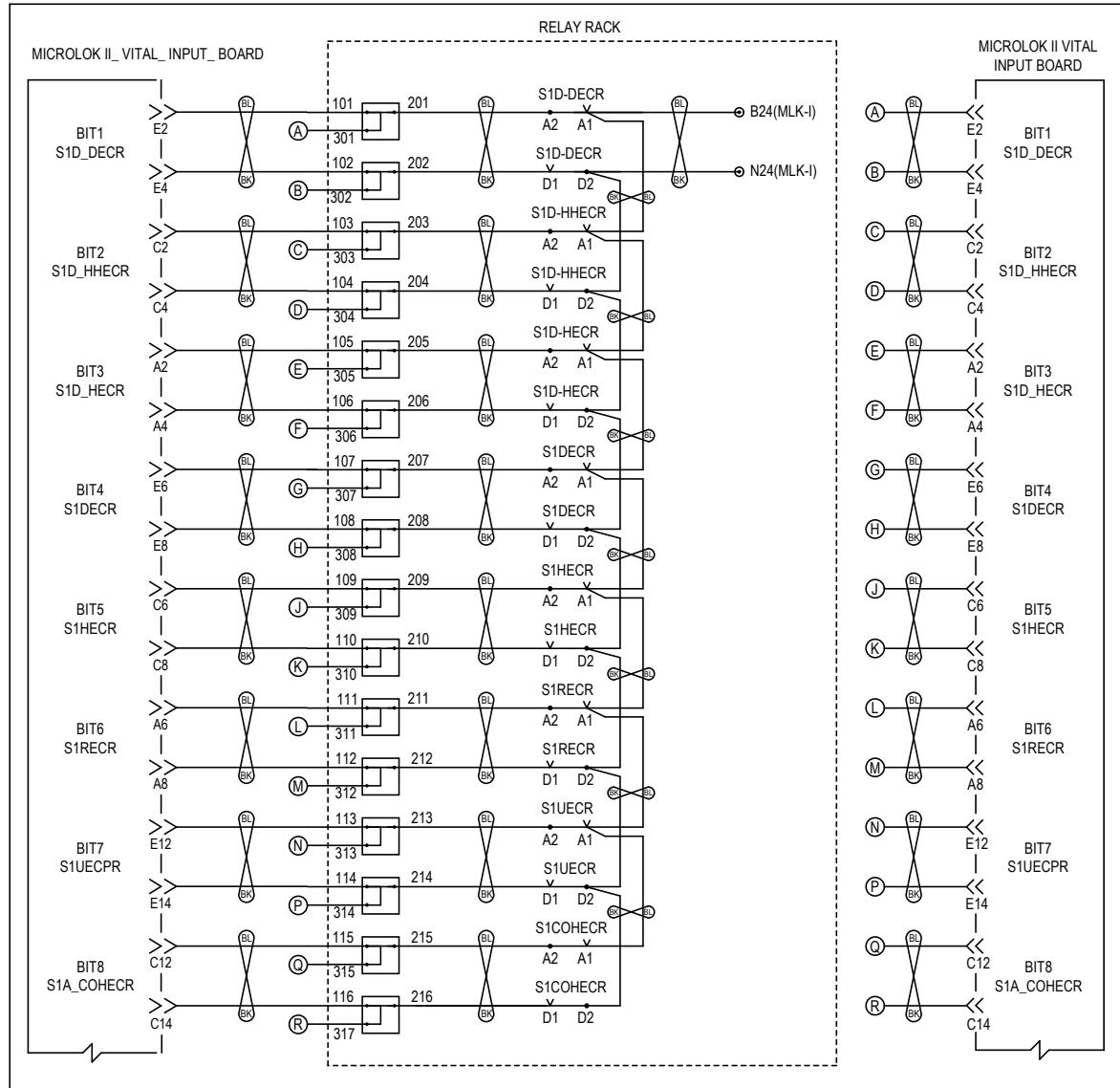


Fig 4.2 Vital Input wiring diagrams

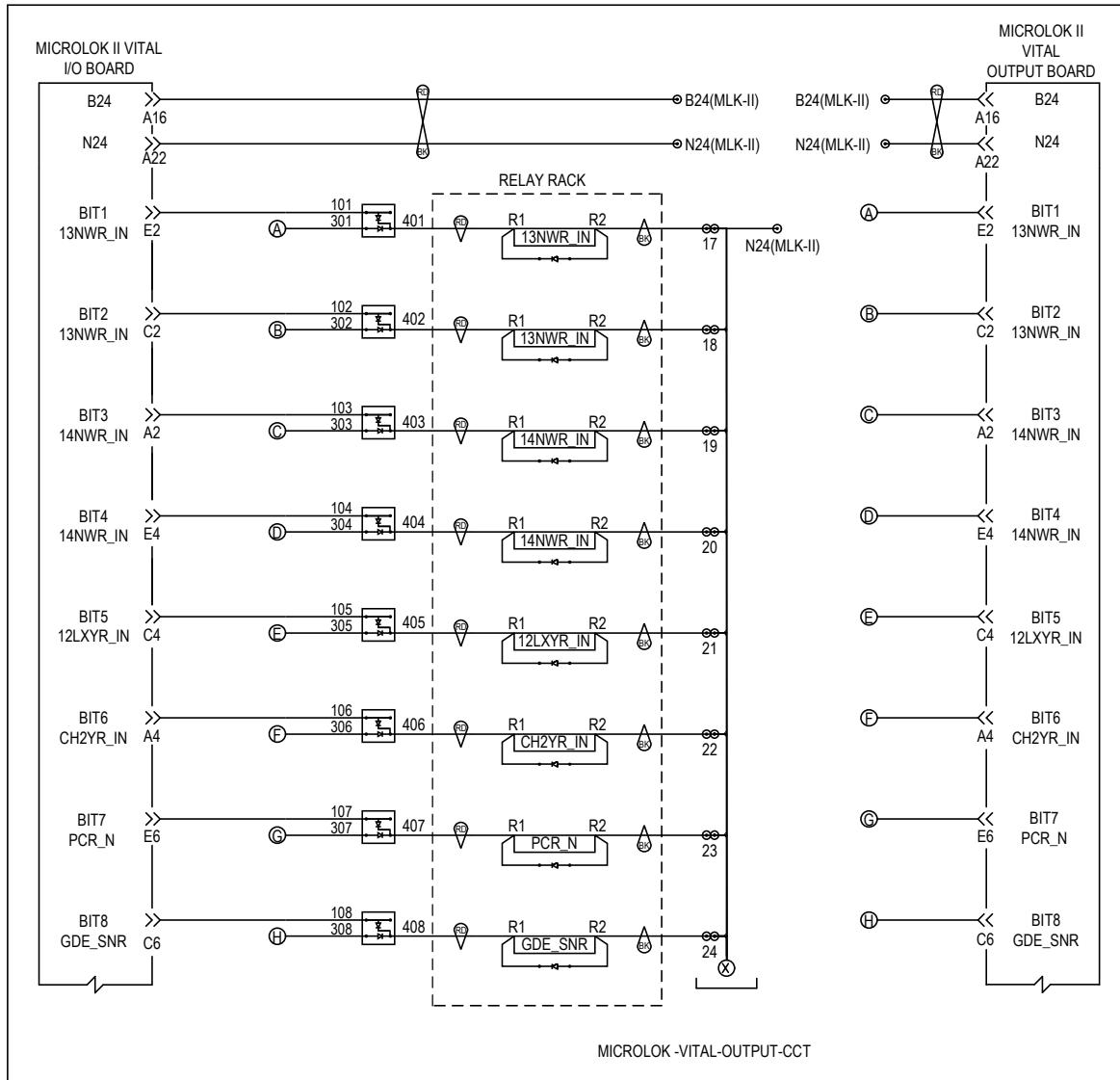


Fig 4.3 Vital Output wiring diagrams

#### 4.1.4 Assessment of Non vital Inputs and Outputs

Gather following information from Front Plate Diagram and list out Non-Vital inputs and Outputs by referring the table No.4.2

- (a) Number of push buttons/ knobs and keys.
- (b) Number of indications, counters, buzzers etc.

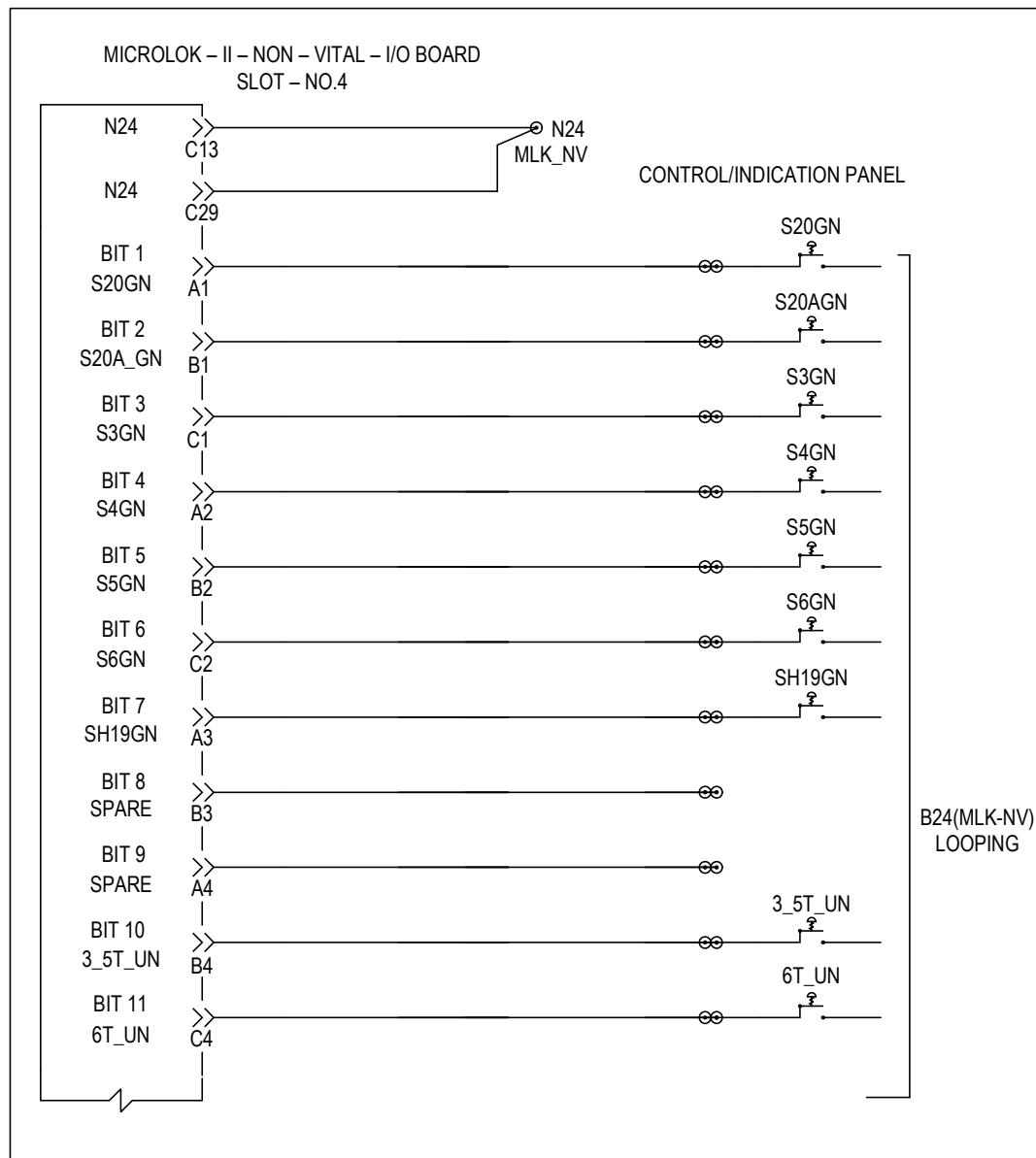


Fig 4.4 Non Vital Input wiring diagrams

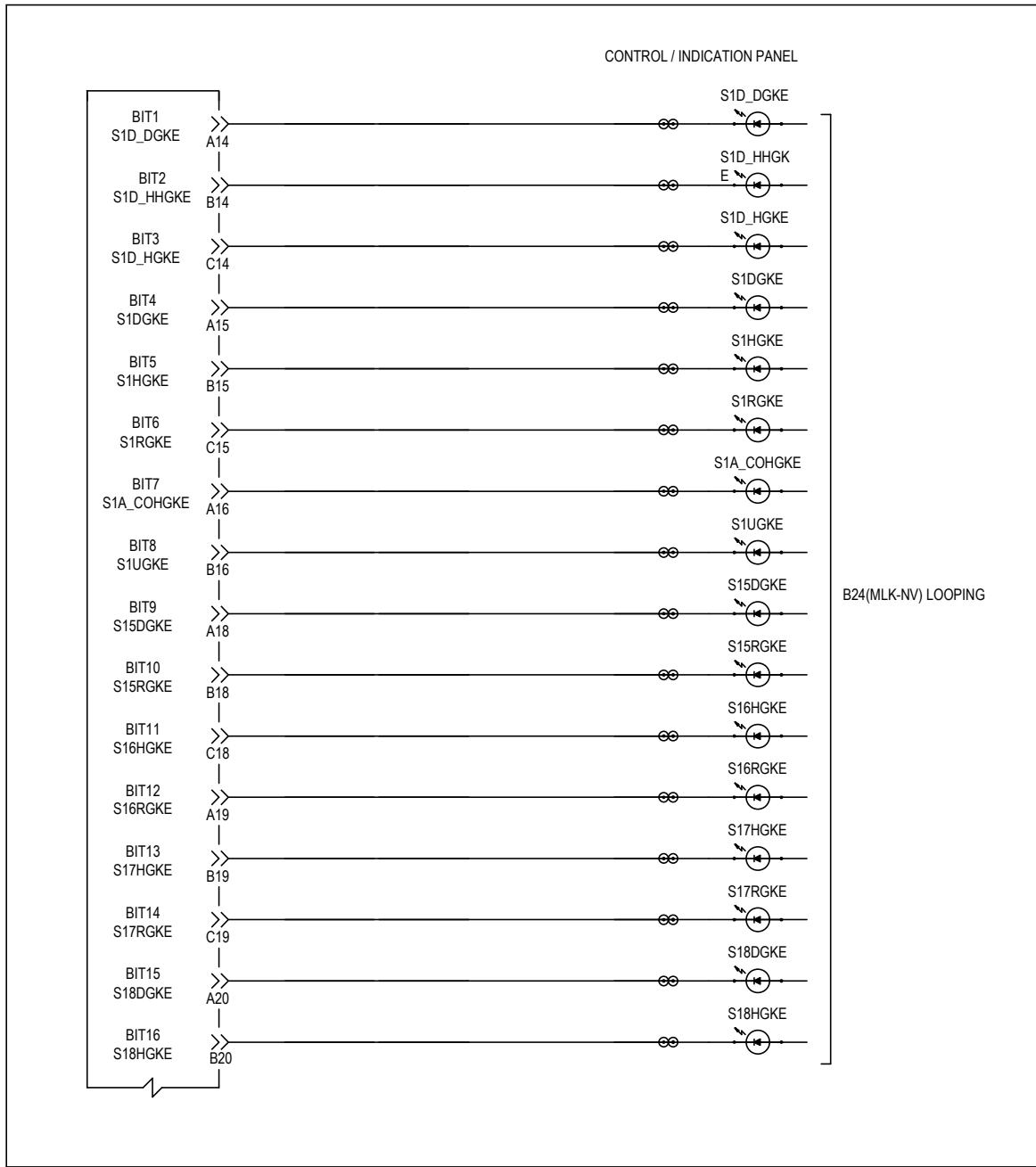


Fig 4.5 Non Vital Output wiring diagrams

#### 4.1.5 Assessment of Read Back BITS

Read back of the status of vital output relay is used to ensure the correspondence between vital output bit delivered and the physical output relay.

While assessing read back bits, Front/ Back/ Both contacts of vital output Relays are taken in to the consideration as per the EI Manufacturer. Further these Read back contacts are considered as vital or Non-Vital inputs depending upon make to make.

##### (a) Nomination of I/O Bits

The Information gathered from "Signal Interlocking Plan" and "Front plate diagram" is used to nominate Vital I/O and Non-Vital I/O bits as shown in the table below.

Outdoor Gear	Vital Output	Vital Input	Non-vital Input	Non-Vital Output	Relays
3A Signal with Calling-on and Route Indicator	DR, HR CO_HR, UHR/ UGR/UR	DECR,HECR, RECR, CO_HECR, UECR	GN	DGKE,HGKE, RGKE,COKE, UGKE, AJKE,	ECR-5, QN1-4
3A Signal	DR HR	DECR,HECR RECR	GN	DGKE,HGKE, RGKE,AJKE	ECR-3, QN1-2
2A Signal	HR	HECR,RECR	GN	HGKE,RGKE, AJKE	ECR-2, QN1-1
Points	WNR/ NWR WRR/ RWR	NWKR/ RWKR	WN	ANWKE,ARWKE, ACKE, ACKRE, ANKE, ANKRE, AT_NKE,AT_NKRE, BT_NKE,BT_NKRE, BNWKE,BRWKE, BCKE, BCKRE, BNKE, BNKRE, WLKE,	QN1-2, QNA1-2
Track Circuit	-	TPR	-	TKE,TKRE	QNA1-1
Crank Handle	CHYR	CHLR	CHYN,YYN/GSBN, YRN/ GSRBN	CHKE,CHKRE	QN1-2
Siding Control	KLR	KLCR	KLN,KLR	KLKE,KLKRE	QN1-2
Level Crossing	LXYR	LXCR	LXN,LXR	LXKE,LXKRE	QN1-1, QNA1-1
Block Inst.	-	LCPR,TOLR	-	-	-

Table 4.2 Nomination of I/O Bits

I/O Bit calculation:

Calculated Vital I/O, Non-vital I/O and read back inputs for the lay out shown in Fig no. 4.1 and appended below in a table form.

(b) NOMINATION OF I/O INPUT, OUTPUT & SPARE BITS

Gear	Vital Output	Vital Input	Non-Vital Input	Non-Vital Output	Relays			
					QN1	QEcx	QNA1	QBCA
S1	S1 DR, S1 HR, S1UGR.	S1 DECR, S1 HECR, S1UECR, S1 RECR.	S1 GN	S1 DGKE, S1 HGKE, SI UGKE, S1 RGKE.	3	4		
S1A	S1A COHR	S1A COHECR		S1A COHGKE	1	1		
S1D1	S1D1 DR, S1D1 HHR.	S1D1 DECR, S1D1 HHECR, S1D1 HECR.		S1D1 DGKE, S1D1 HHGKE, S1D1 HGKE.	2	3		
S1D2	S1D2 DR, S1D2 HHR.	S1D2 DECR, S1D2 HHECR, S1D2 HECR.		S1D2 DGKE, S1D2 HHGKE, S1D2 HGKE.	2	3		
S25 (LSS)	S25 DR	S25 DECR, S25 RECR,	S25 GN	S25 DGKE, S25 RGKE.	1	2		
SH10	SH10 HR	SH10 OFFECR, SH10 ONECR.	SH10 GN	SH10 OFFKE, SH10 ONKE.	1	2		
S27	S27 HR	S27 HECR, S27 RECR.	S27 GN	S27 HGKE, S27 RGKE.	1	2		
S28	S28 DR, S28 HR.	S28 DECR, S28 HECR, S28 RECR.	S28 GN	S28 DGKE, S28 HGKE, S28 RGKE	2	3		
S26	S26 HR	S26 HECR, S26 RECR.	S26 GN	S26 HGKE, S26 RGKE.	1	2		
SH23	SH23 HR	SH23 OFFECR, SH23 ONECR.	SH23 GN	SH23 OFFKE, SH23 ONKE.	1	2		
S3	S3 DR, S3 HR.	S3 DECR, S3 HECR, S3 RECR.	S3 GN	S3 DGKE, S3 HGKE, S3 RGKE	2	3		
S4	S4 HR	S4 HECR, S4 RECR.	S4 GN	S4 HGKE, S4 RGKE.	1	2		
SH21	SH21 HR	SH21 OFFECR, SH21 ONECR.	SH21 GN	SH21 OFFKE, SH21 ONKE.	1	2		
S6 (LSS)	S6 DR	S6 DECR, S6 RECR,	S6 GN	S6 DGKE, S6 RGKE	1	2		
S30	S30 DR, S30 HR, S30UGR1, S30UGR2.	S30 DECR, S30 HECR, S30 UECR, S30 RECR.	S30 GN	S30 DGKE, S30 HGKE, S30 UGKE, S30 RGKE.	4	4		
S30A	S30A COHR	S30A COHECR		S30A COHGKE	1	1		

Gear	Vital Output	Vital Input	Non-Vital Input	Non-Vital Output	Relays			
					QN1	QECX	QNA1	QBCA
S30D1	S30D1 DR, S30D1, HHR.	S30D1 DECR, S30D1 HHECR, S30D1 HECR.		S30D1 DGKE, S30D1 HHGKE, S30D1 HGKE.	2	3		
S30D2	S30D2 DR, S30D2 HHR.	S30D2 DECR, S30D2 HHECR, S30D2 HECR.		S30D2 DGKE, S30D2 HHGKE, S30D2 HGKE.	2	3		
Block		UP LCPR/ASCR DNLCPR/ASCR			2			
BPAC		UP VPR, UP PPR, DN VPR, DN PPR.					4	
Point No.11	11 WNR, 11 WRR, 11 NWLR, 11 RWLR.	11 NWKR, 11 RWKR.	11WN	11ANWKE, 11ARWKE, 11ACKE, 11ACKRE, 11anke, 11ANKRE, 11AT_NKE, 11AT_NKRE, 11BT_NKE, 11BT_NKRE, 11BNWKE, 11BRWKE, 11BCKE, 11BCKRE, 11BNKE, 11BNKRE, 11WLKE,	4		2	
Point No.12	12 WNR, 12 WRR, 12 NWLR, 12 RWLR.	12 NWKR, 12 RWKR.	12WN	12ANWKE, 12ARWKE, 12ACKE, 12ACKRE, 12anke, 12ANKRE, 12AT_NKE, 12AT_NKRE, 12BT_NKE, 12BT_NKRE, 12BNWKE, 12BRWKE, 12BCKE, 12BCKRE, 12BNKE, 12BNKRE, 12WLKE	4		2	
Point No.13	13 WNR, 13 WRR, 13 NWLR, 13 RWLR.	13 NWKR, 13 RWKR.	13WN	13ANWKE, 13ARWKE, 13ACKE, 13ACKRE, 13anke, 13ANKRE, 13AT_NKE, 13AT_NKRE, 13BT_NKE, 13BT_NKRE, 13BNWKE, 13BRWKE, 13BCKE, 13BCKRE, 13BNKE, 13BNKRE, 13WLKE,	4		2	
Point No.18	18 WNR, 18 WRR, 18 NWLR, 18 RWLR.	18 NWKR, 18 RWKR.	18WN	18ANWKE, 18ARWKE, 18ACKE, 18ACKRE, 18anke, 18ANKRE, 18AT_NKE, 18AT_NKRE, 18BT_NKE, 18BT_NKRE, 18BNWKE, 18BRWKE, 18BCKE, 18BCKRE, 18BNKE, 18BNKRE, 18WLKE,	4		2	

Gear	Vital Output	Vital Input	Non-Vital Input	Non-Vital Output	Relays			
					QN1	QECX	QNA1	QBCA
Point No.19	19 WNR, 19 WRR, 19 NWLR, 19 RWLR.	19 NWKR, 19 RWKR.	19WN	19 NWKE, 19 RWKE, 19 CKE, 19CKRE, 19NKE, 19NKRE, 19T_NKE, 19T_NKRE, 19WLKE	4		2	
Point No.20	20 WNR, 20 WRR, 20 NWLR, 20 RWLR.	20 NWKR, 20 RWKR.	20WN	20ANWKE, 20ARWKE, 20ACKE, 20ACKRE, 20ANKE, 20ANKRE, 20AT_NKE, 20AT_NKRE, 20BT_NKE, 20BT_NKRE, 20BNWKE, 20BRWKE, 20BCKE, 20BCKRE, 20BNKE, 20BNKRE, 20WLKE,	4		2	
Point Power control	PCR_1 PCR_2							2
KL15	15 KLYR	15 KLCR	15 KLN	15KLFKE, 15KL_INKE, 15KL_OUTKE.	2			
LC22	22 LXYR	22 LXCR	22 LZN	22LXFKE, 22LX_INKE, 22LX_OUTKE.	1		1	
CH1	CH1YR	CH1CR	CHIYN	CH1FKE, CH1_INKE, CH1_OUTKE	2			
CH2	CH2YR	CH2CR	CH2YN	CH2FKE, CH2_INKE, CH2_OUTKE	2			
CH3	CH3YR	CH3CR	CH3YN	CH2FKE, CH2_INKE, CH2_OUTKE	2			
Track Circuits		1ATPR, 1TPR, 26-28TPR, 25TPR, ULTPR, UMTPR, DMTPR, CLTPR, 3-4TPR, 6TPR, 30TPR, 30ATPR, 11ATPR, 11BTPR, 12ATPR, 12BTPR, 13ATPR, 13BTPR, 18ATPR, 18BTPR, 19TPR, 20ATPR, 20BTPR.		1ATKRE, 1TKE, 1TKRE, 26-28TKE, 26-28TKRE, 25TKE, 25TKRE, ULTKE, ULTKRE, UMTKE, UMTKRE, DMTKE, DMTKRE, CLTKE, CLTKRE, 3-4TKE, 3-4TKRE, 6 TKE, 6TKRE, 30 TKE, 30TKRE, 30 TKRE,				
Route Buttons		CLAT, CLT, DMT, UMT, ULAT, ULT, 25T, 26-28T, 3-4T, 6T.						

Gear	Vital Output	Vital Input	Non-Vital Input	Non-Vital Output	Relays			
					QN1	QECX	QNA1	QBCA
Common Point Buttons			NWWN, RWWN, EWWN.					
Signal Cancel Button			EGGN					
Route Cancel Buttons			EUYN, EUYN.	EUUYKE, EUYKE,				
Co-ON Buttons			COGNN, COCAN.	COGGKE, COCANKE.				
Slot Buttons			GSBN, GSRBN.					
Other Buttons			GXYN, WXYN, NNCYN POWER ACK,	GNCKE, WNCKE, UNCKE, PWRFLKE.				
SM Key			SM_KEY	SMKEY_INKE, SMKE_OUTKE.				
Panel-PC KEY			PANEL_P CKEY	PANELKE, PCKE.				
Counters				UP_EUUYZ, DN_EUUYZ, EUYZ, EWYZ.				
Overlap Indication				26 OVKE, 27 OVKE, 28 OVKE, 3 OVKE, 4 OVKE.				
System Indication				SYSA_H, SYSA_F, SYSB_H, SYSB_F, SYSFAILBUZ.				
Flasher				Flash_KE				
Total	60	100	40	196				

Table 4.3 Nomination of input, output & spare bits

*Note : The system shall have provision for accommodating additional 10% of I/Os as spares for future modifications.*

(c) READBACK CONTACTS

Gear	Vital Output	Vital Input	Non-Vital Input	Non-Vital Output
S1			S1 DR_F/ S1 DR_B, S1 HR_F/ S1HR_B, S1UGR_F/S1UGR_B.	
S1A			S1A COHR_F/S1A COHR_B.	
S1D1			S1D1 DR_F/ S1D1 DR_B, S1D1 HHR_F/ S1D1 HHR_B.	
S1D2			S1D2 DR_F/ S1D2 DR_B, S1D2 HHR_F/ S1D2 HHR_B.	
S25			S25 DR_F/ S25 DR_B.	
SH10			SH10 HR_F/ SH10 HR_B.	
S27			S27 HR_F/ S27 HR_B.	
S28			S28 DR_F/ S28 DR_B, S28 HR_F/ S28 HR_B.	
S26			S26 HR_F/ S26 HR_B.	
SH23			SH23 HR_F/ SH23 HR_B.	
S3			S3 DR_F/ S3 DR_B, S3 HR_F/ S3 HR_B.	
S4			S4 HR_F/ S4 HR_B.	
SH21			SH21 HR_F/ SH21 HR_B.	
S6			S6 DR_F/ S6 DR_B.	
S30			S30 DR_F/ S30 DR_B, S30 HR_F/ S30 HR_B, S30UGR_F/ S30UGR_B.	
S30A			S30A COHR_F/ S30A COHR_B	
S30D1			S30D1 DR_F/ S30D1 DR_B, S30D1 HHR_F/ S30D1 HHR_B.	
S30D2			S30D2 DR_F/ S30D2 DR_B, S30D2 HHR_F/ S30D2 HHR_B.	
Point No.11			11 WNR_F/11 WNR_B, 11 WRR_F/11 WRR_B.	
Point No.12			12 WNR_F/12 WNR_B, 12 WRR_F/12 WRR_B.	
Point No.13			13 WNR_F/13 WNR_B, 13 WRR_F/13 WRR_B.	
Point No.18			18 WNR_F/18 WNR_B, 18 WRR_F/18 WRR_B.	
Point No.19			19 WNR_F/19 WNR_B, 19 WRR_F/19 WRR_B.	
Point No.20			20 WNR_F/20 WNR_B, 20 WRR_F/20 WRR_B.	

Gear	Vital Output	Vital Input	Non-Vital Input	Non-Vital Output
KL15			15 KLYR_F/ 15 KLYR_B	
LC22			22 LXYR_F/ 22 LXYR_B	
CH1			CH1YR_F/ CHIYR_B	
CH2			CH2YR_F/CH2YR_B	
CH3			CH3YR_F/CH3YR_B	

Table 4.4 Readback contacts

#### 4.1.6 Assessment of Cards, Card files and Panel processors

- (a) After finding out final quantity of Vital and Non-vital I/O bits including 10% of spare bits, quantity of various boards is calculated as below:
  - (i) No of Vital Input Cards Required = Total Vital Inputs divided by Capacity of the vital input card.
  - (ii) No of Vital output Cards Required = Total Vital outputs divided by Capacity of the vital output card.
  - (iii) No of Non-Vital Input Cards Required = Total Non-Vital Inputs divided by Capacity of the Non-vital input card.
  - (iv) No of Non-Vital output Cards Required = Total Non-Vital outputs divided by Capacity of the Non-vital output card.
- (b) Depending upon No. of Vital Input, Vital output, Non-Vital Input, Non-Vital output cards, the No. of Card files are to be calculated. The no of cards to be accommodated in each card file will vary from make to make.

#### 4.1.7 EI Configuration

The following parameters have to be considered for Configuration of EI System,

- (a) Hot standby or Warm standby
- (b) Centralised or Distributed Interlocking
- (c) Inter subsystem Communication – Serial, Ethernet, OFC or Combination of these.
- (d) Type of Operating console- CCIP, VDU or both

### 4.2 EI APPLICATION LOGIC

Application Program Design :

Application Program is written based on the conventional Relay Interlocking Circuits prepared from the Route control chart (RCC) or Selection table (ST). Steps involved in preparation of Application Program varies from make to make. Application Program may be in the form of Boolean logic. Bits of Boolean logic correspond to the relays used in conventional Interlocking circuits.

Application Program Development:

Every EI system has development tools. These tools are used to develop, compile, debug and upload the application program into the system CPU.

## Application Program Development

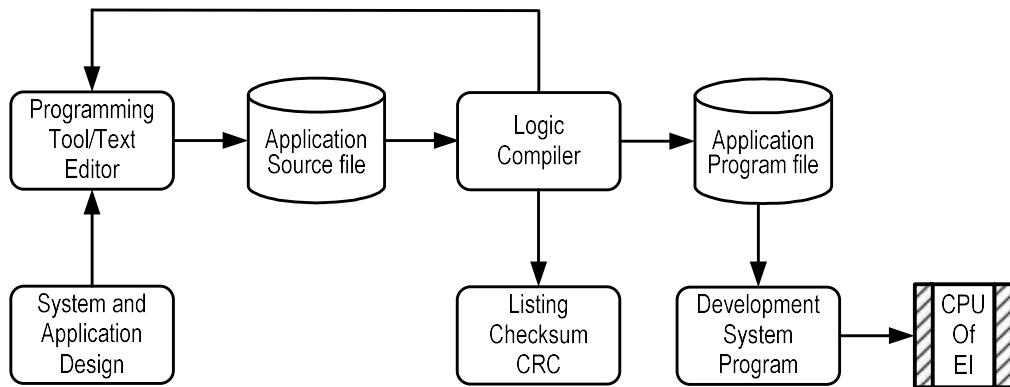


Fig 4.6 Application program development

There are three main steps involved in development of EI system.

- (a) Application source file is created with a predefined file structure. File structure will vary from make to make.
- (b) The logic Compiler is a PC - based tool. It checks the Application source file for syntax errors. After correction of these errors, it further generates the appropriate Application program file in Machine Language. The compiler also generates warnings, program listings, tables, and installation information etc.
- (c) This Application Program is loaded in to the CPU board.

### 4.2.1 Transformation of Circuit

The Relay Interlocking circuits are transformed as Boolean equations. The Symbols for Translating Relay Interlocking circuits to Boolean Equations in Microlok are as:

Parentheses, NOT, AND, OR and Comma.

The precedence of these operators from highest to lowest is as :

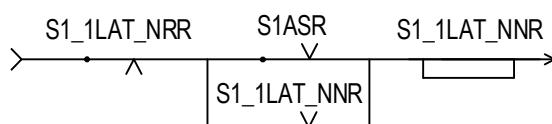
( ) Parentheses

$\sim$  NOT

\* AND

+ OR

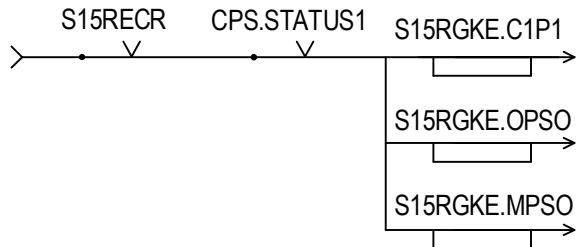
Example 1 :



ASSIGN  $\sim$  S1\_1LAT\_NRR \* ( S1ASR + S1\_1LAT\_NNR )TO S1\_1LAT\_NNR ;

Fig 4.7

Example 2 :



NV. ASSIGN 15RECR \* CPS.STATUS1 TO S15RGKE.C1P1,  
S15RGKE.OPSO,  
S15RGKE.MPSO;

Fig 4.8

#### 4.2.2 Compilation

Compiler :

The Application Program written with the help of any text editor/user friendly tool supplied by EI manufacturer is called as Application source file.

A compiler is a computer program that converts application source file written in a programming language like any text editor / tool into another computer language (the target language), often having a binary / Hexa decimal form. The most common reason for converting a source code is to create an executable program.

The application Program (in target language) is flashed into EPROMs of CPU.

Compilation Process :

The interlocking requirements of a station are going to be written in the pre defined format called application program. It will be in the high level language.

To flash this application program in to Application program EPROM of CPU it should be converted in to the machine language.

In computer programming, the translation of source code (application source file) into object code (machine language) is done by using a compiler.

#### 4.2.3 Verification and validation

Verification and validation of a microprocessor based safety system is carried out in four stages as described below :

Stage-1 : Theoretical designs of the hardware and program structure of the software are examined for reliability and fail safety at the initial design level.

Stage-2 : Each card or the circuit module of the hardware is tested under normal as well as fault conditions. In the case of software, each routine is tested with diverse test data.

Stage-3 : Overall system, after integration of hardware and software is tested under different input data conditions. Testing at this stage can be carried out by simulation for accelerated testing using computers.

Stage-4 : Exhaustive field trials of the equipment is conducted under the field conditions.

## TESTING OF EI SYSTEM

As explained above, extensive testing and validation of both hardware and software of the EI system have been carried out. The details are given below.

### (a) Hardware Testing

#### (i) Testing of PCB Cards

Each PCB card has been tested for its correct functioning. Fail safety tests have also been conducted on each PCB card/circuit for checking that no unsafe condition is created by opening and short-circuiting of individual components used in the PCB card/circuit.

#### (ii) Computerized Testing of EI System

Initially No availability of suitable testing methods has been the main problem in introduction of EI system in the field.

RDSO has developed special testing software and created computerized testing facilities to validate the prototype.

A PC with suitable interface cards has been used to give the panel command to the EI prototype. Status of the track circuits was also fed through the PC Miniature relays, which were used to simulate points, slots, level crossings, signals etc.

The output of EI was used to operate a set of miniature relays, which was checked by the PC to ensure that the outputs are correct.

First, all the conditions required for taking OFF a signal were set up to check whether the EI gives an output for operation of the signal. Thereafter, the controlling conditions were varied in different permutations and combinations to check their effect on the route and the signal.

The same exercise was repeated on all the signals/routes. A total of about two lakhs permutations and combinations were covered for testing of 20 routes provided on the EI.

#### (iii) Software Validation

Software validation is as important as hardware testing of the equipment. Like hardware is tested for its correct functioning under different conditions and different inputs, software is also required to be tested for different possible combination of input data.

The executive software for the EI system has been validated by RDSO through independent V & V wing after obtaining source code from the manufacturer.

#### General Guidelines for Software Validation

Software validation should be performed keeping in view the overall safety and reliability of the system. Following points should be considered while validating the software.

- Each routine is preceded by a header comment. This comment should be examined to verify that the programme has understood the problem correctly.
- The source code should be examined line by line to verify that the algorithm given in the comment has been implemented truthfully.
- It should be ensured that under normal circumstances as well as under conditions of faulty data, there should be no possibility of hanging of the software.

- A general principle of safety has been adopted while writing the software viz. safe state of the system should automatically be achieved by default. In order to take the system to less restricted state, repeated action is required to be taken by the respective routines. For example, if no positive step is taken by any routine, the corresponding signal should automatically go back to danger. This aspect should be verified.
- The routines are called in an infinite loop. Output generated by one routine serves as input to the next routine. As a general principle, the input data, after being utilised by a particular routine should be erased so that same command is not available in the next cycle i.e. one command one operation principle is observed.

Methodology Adopted for Validation :

The source listing of the software program has been studied to make out the data structure and calling tree. Thereafter, the listing for each routine has been examined vis-à-vis., data structure and the calling tree. While examining the software, basic principles of interlocking have been kept in mind.

During validation, certain changes required to be carried out in the software to meet the operational requirements, have been carried out by the firm.

The software for EI system after validation has been found to meet the basic requirements of safety and complies with the principles of interlocking.

#### Field trials

After exhaustive testing in the firm's premises and RDSO as described above, the EI Mark - II system was installed at Duskheda station of Bhusawal division of Central Railway. The system was installed in parallel with the existing panel Interlocking installation (Siemen's type)

The outputs of EI as well as PI were monitored with the help of a data logger for a period of about 15 months. The monitoring of the system was jointly done by RDSO, Bhusawal division and the firm.

Data logger output has been analyzed in detail and the mismatches between EI & PI have been identified. Problems arising out of teething troubles have been taken care of by minor changes in the software. Scrutiny of the mismatches has not revealed any malfunctioning of EI and the system has performed satisfactorily during the field trial.

#### 4.2.4 Reverse Compiler

A reverse compiler (De compiler) is a computer program that performs the reverse operation to that of a compiler.

That is, it translates program code at a relatively low level language which is usually computer readable rather than human readable into a form of higher level language usually human readable.

Reverse compiler usually do not perfectly reconstruct the original source code, and can vary widely in the intelligibility of their outputs. Nonetheless, Reverse compiler remains an important tool in software reverse engineering. A Reverse compiler takes as input an executable file, and attempts to create a high level, compilable, possibly even maintainable source file that does the same thing. It is therefore the opposite of a compiler, which takes a source file and makes an executable. However, a general Reverse compiler does not attempt to reverse every action of the compiler; rather it transforms the input program repeatedly until the result is high level source code.

#### 4.2.5 CRC and CHECKSUM

Network must be capable of transferring data from one device to another device with Acceptable Accuracy. Generally a system should ensure that the data Received is identical to data Transmitted. During Transmission a bit is changed from 1 to 0 OR 0 to 1. Some applications can tolerate few errors, for example random error in audio or video transmission may be tolerable but when we transfer text or command in EI for operation we expect a very Accuracy.

To achieve required Accuracy CRC and Checksum are used in data transmission. By using CRC and Checksum the data at receiving end is accepted when errors are not detected. If Errors are detected at receiving end data is rejected.

##### (a) Cyclic Redundant Check

Some standard polynomials used by popular protocols for CRC generation are

Name	Polynomial	Application
CRC-8	$x^8 + x^2 + x + 1$	ATM header
CRC-10	$x^{10} + x^9 + x^5 + x^4 + x^2 + 1$	ATM AAL
CRC-16	$x^{16} + x^{12} + x^5 + 1$	HDLC
CRC-32	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + 1$	LANs

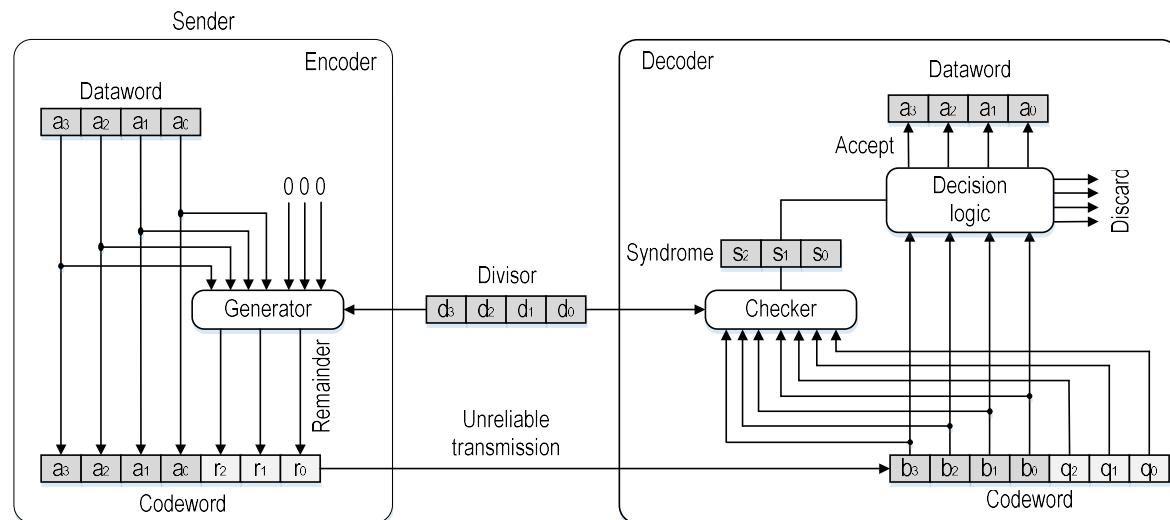


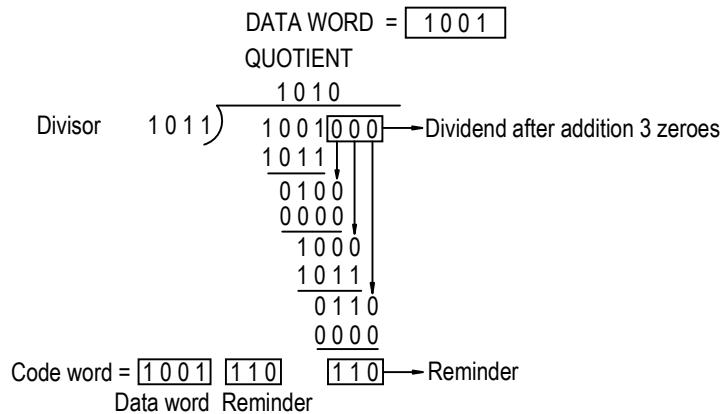
Fig 4.9 Encoder & decoder for cyclic redundant bits

The data to be transmitted is called as data word. In the diagram above the data word has 4 bits ( $K$  bits), the code word has 7 bits ( $n$  bits). The size of the data word is increased by adding 3 zeros ( $n-K$  zeros) to right hand side of the word and fed into generator. The divisor uses 4 bits ( $n-K+1$ ) word. The generator divides the augmented data word by the divisor. The remainder ( $r_2 \ r_1 \ r_0$ ) is appended to the data word to create codeword. The quotient is discarded.

At receiving end  $n$  bits code word is fed into the checker. The remainder produced is called Syndrome- 3 bits ( $n-K$ ) fed into analyser. If the syndrome bits are all 0s, the left most bits of the codeword are accepted as the data word or else the 4 bits are discarded.

EXAMPLE :

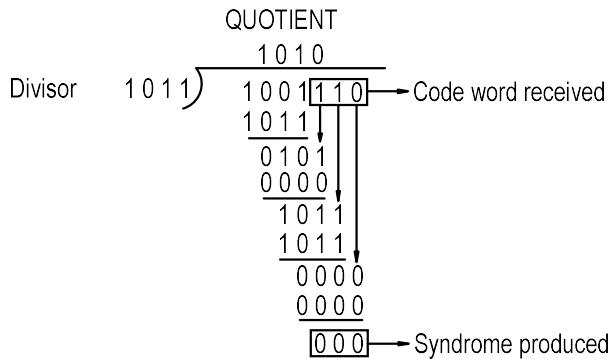
At Sending End



At Receiving End

Case.1 Code word Received = 1 0 0 1 1 1 0

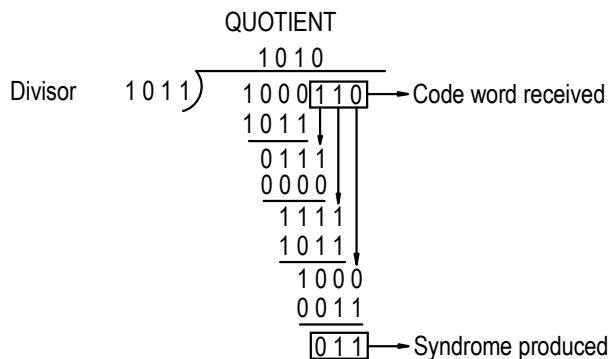
DIVISION



Data word accepted = 1 0 0 1

Case.2 Code word Received = 1 0 0 0 1 1 0

DIVISION



Data word discarded

The divisor in a cyclic code is selected by generator polynomial. The Cyclic codes have capacity to detect single bit errors, double bit errors, an odd number of errors and burst errors. They can easily be implemented in hardware and software.

### (b) CHECKSUM

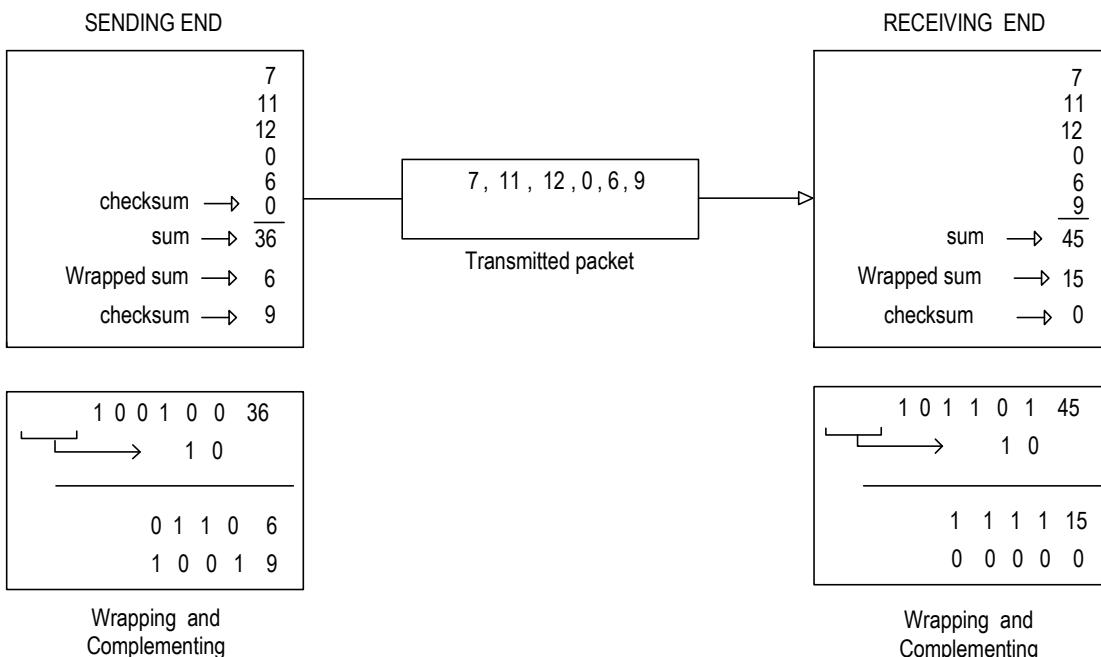
Checksum is also an error detection method. It is based on concept of redundancy.

Suppose our data is a list of five 4-bit numbers that we want to send to a destination. In addition to sending these numbers, we send the sum of the numbers. For example, if the set of numbers is (7, 11, 12, 0, 6), we send (7, 11, 12, 0, 6, 36), where 36 is the sum of the original numbers. The receiver adds the five numbers and compares the result with the sum. If the two are the same, the receiver assumes no error, accepts the five numbers and discards the sum. Otherwise, there is an error and the data are not accepted.

We can make the job of the receiver easier if we send the negative (complement) of the sum, called the checksum. In this case, we send (7, 11, 12, 0, 6, -36). The receiver adds all the numbers received. If the result is 0, it assumes no error; otherwise, there is an error.

All our data except checksum can be written as 4 bit word. We use one's complement to solve this. We can represent unsigned numbers between 0 and  $2^n - 1$  using n bits. If the number has more than n bits, the extra left most bits are added to the n right most bits by wrapping.

For example, the number 22 in binary is 10110 with five bits. We can wrap the leftmost bit and add it to the four rightmost bits. We have  $(0110 + 1) = 0111$  or 7.



The Internet has been using a 16 – bit checksum. The sender calculates the checksum by following steps

Sending end :

1. The message is divided into 16-bit words.
2. The value of the checksum word is set to 0.
3. All words including the checksum are added using one's complement addition.
4. The sum is complemented and becomes the checksum.
5. The checksum is sent with the data.

At receiving end the following steps are used for error detection.

Receiving end:

1. The message (including checksum) is divided into 16-bit words.
2. All words are added using one's complement addition.
3. The sum is complemented and becomes the new checksum.
4. If the value of checksum is 0, the message is accepted; otherwise, it is rejected.

## 4.3 SIMULATION

### 4.3.1 Testing Methods

Testing of electronic interlocking system is carried out in two phases.

- (a) System testing at factory premises called as Factory Acceptance Test.
  - (b) System testing at site called as Site Acceptance Test.
    - (a) Factory Acceptance Test
      - (i) Factory Acceptance Test (FAT) for EI system shall be tested in Factory environment with simulation setup to validate application software.
      - (ii) The purpose of Factory Acceptance Test is to:
        - Ensure that the Interlocking system fulfils the station Interlocking & Route Control Chart requirements and workings in safe manner even if any false inputs / information received.
        - Minimises the site errors & risks and reduces the corrections at site. This results in saving of time at site testing.
      - (iii) FAT is carried out through simulation set up (using Simulator Panel with toggle switches or Simulator PC with Interlocking Simulation Setup - software) in which all field inputs are simulated.
      - (iv) FAT is carried out for each station interlocking installation separately.
      - (v) After designing the Application Software, designer issues it to the validation department for carrying the Factory Acceptance Test.
      - (vi) It is carried out only through VDU panel, whereas Site Acceptance Test (SAT) is carried out through CCIP and VDU panels, if both the options are available at site.
      - (vii) During FAT Timers in Application logic are modified for the FAT testing for Timer values used for signal, point, overlap and cancellation are reduced from 120 secs to 12 secs to speed up the testing. It is essential that the original values of timers are reinstated and validated at the completion of testing.
      - (viii) In FAT setup, the I/O boards are not physically present and the same are simulated using the test setup. Therefore, field inputs and outputs delivered by Input and Output card will be disabled and will be directly delivered into simulation VDU. However this will not affect the interlocking part of the application logic.
    - (ix) To carry out FAT, the following inputs are required:
      - Signal Interlocking Plan (SIP).

- Route Control Chart (RCC).
- Control cum Indication Panel Diagram.
- Cross Table/Square sheet.
- Station Interlocking Application Software files as designed (example in case of MicrolokII.ML2, .MLL, .MLP).

(x) After carrying out FAT, the following are the outputs:

- Station Interlocking Application Software files as tested (example in case of MicrolokII.ML2, .MLL, .MLP).
- Total Management System (TMS) Forms.
- FAT Certificate.

If Railways/Customer testing is completed, then the Check sum and CRC values of the FAT simulated application logic will be recorded as per the Application Logic and it is to be jointly signed by OEM and Railways representative.

(a) Site Acceptance Test (SAT)

- (i) Site Acceptance Test (SAT) defines the procedure for Site testing of Station Interlocking System, where tests are executed at site environment.
- (ii) SAT mainly involves the System integrity and functional testing of all equipments and interlocking testing also shall be carried out with full setup except the trackside equipments.
- (iii) SAT is carried out for each station separately.
- (iv) Results of the tests are observed and documented in a Test Report.
- (v) The Site Acceptance Test ensures that all the equipments installed at site i.e. EI Hardware, Communication equipments, Power supply equipments, Relays and Control cum Indication Panel are functioning correctly as per approved system configuration & station interlocking requirements and working in safe manner and failsafe even if any equipment fails / false inputs/information received.
- (vi) SAT ensures the overall system safety and error free system is being delivered to the client.

(vii) To carry out SAT, the following inputs are required:

- Application source file, Application listing file, Application program file (in case of Microlok II .ml2, .mll & .mlp file (Hardcopy & Read-only Softcopy)
- Station SIP
- Station Route control chart
- Station Control cum indication panel diagram
- Square Sheets/Cross tables
- Wiring circuits

(viii) All the equipments involved for station working is being installed before proceeding SAT, so there is no need of separate set up is required except to simulate the field inputs with Simulation panel.

- (ix) All the field inputs are simulated by using simulation panel through toggle switches and inputs are sent to EI via relays and the field outputs are sent to lamps through relays.
- (x) The following testing shall be carried out while doing SAT
  - Visual test
  - Wire count test
  - Bell test
  - Insulation resistance test
  - Earthing test
  - Power On
  - VCOR
  - Communication testing
  - Correspondence Test
  - System Integrity Test
  - Interlocking testing
  - Change over test

#### 4.4 EARTHING AND SURGE PROTECTION

All electronic interlocking equipment are functioning round the clock and controls the entire signaling system and hence it is very important to safeguard the system to ensure uninterrupted service against lightning and surges.

Hence lightning and surge protection along with proper earthing should be provided for proper functioning of the equipment.

The EI system communicates with the outdoor gears through Interface relays and as such gets isolated from any surge which may come from outdoor gears. However, still it may get surges from power input side, control panel side or due to improper earth. Thus suitable protection is required to be provided.

For EI, Air Termination type of protection is to be provided in the form of Lightning arrestor at the roof of the building housing the EI system. Type A & Type B protections will be provided at the input of the IPS (as part of IPS) system feeding to the EI system. Preferably class B & class C should be of same firm to fulfill energy co-ordination. In addition to the above, Type C protection is to be provided at 24volt DC incoming (from IPS) to EI system and control panel. This will ensure that if due to any reason (say non-functioning of upstream protection devices) surge travels up to the EI system, then some form of protection will be available to take care of the equipment. All SPDs should be provided close to equipment.

It is recommended that the connection of Control Panel to EI system should be OFC only. If Control panel is in the different room requiring outdoor cable laying from extending the supply to it from Power room, then class – D protection is required if cable is laid underground and also class C protection if cable is taken above the ground.

Ring earthing or perimeter earthing may be provided to bring the earth resistance value to less than  $1 \Omega$ . Instead of providing different earths for EI system, control panel & IPS which may have different earth values, only one earthing system of ring type with equi-potential bonding should be provided with earth resistance  $< 1 \Omega$ . All equipments in power room as well as in EI room should be connected to this earth system though respective Room Earth Bar.

Therefore it is absolutely necessary to provide suitable protection arrangement against lightning and surges, as discussed above, so that dangerous voltages can be diverted to the ground and EI system can be protected.

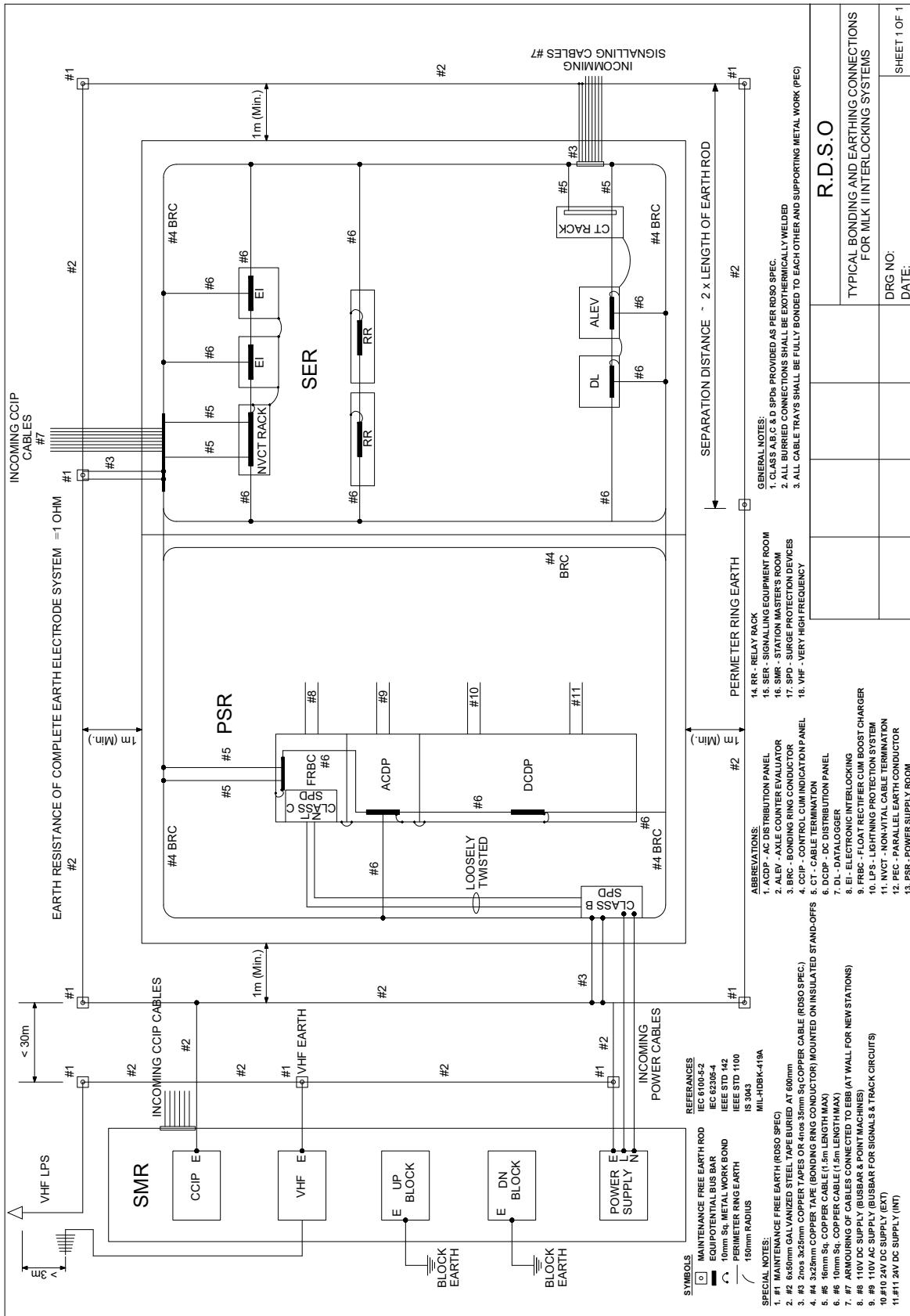


Fig 4.10 Typical Bonding and Earthing connections for MLK II Interlocking Systems

## EMC (ELECTRO MAGNETIC COMPATIBILITY)

It is ability of an electronic equipment or a system to operate reliably in an EM environment without being a source of, and susceptible to interference.

## EMI (ELECTRO MAGNETIC INTERFERENCE)

Degradation of desired signal by presence of undesired electrical signals (electrical noise) is EMI.

Railway Electro Magnetic compatibility (EMC) is concerned with ensuring electrical/electronic equipment and systems installed with railway environment do not interfere with each other or outside world. EMI mitigation technique should be applied to all stages of design. Adhere to EMC standards to achieve compliance. Verify that EMC has been achieved by final on site EMC testing.

All electronic Interlocking equipment manufactured should be electro magnetically compatible and the Earthing value for EI should be less than  $1\Omega$ .

IEC 62305 – 3 recommends,  $10\ \Omega$  for A&B type lightning earthing termination.

Sources of Emission :

1. Internal sources of EM noise :

- Static elements.
- Mobile elements.
- Auxiliary power convertor.
- Track side equipment.

2. External sources of EM noise :

- Neighboring railway station.
- Track side radio station.
- Portable radios.
- Industrial plants which disturb electrical supply network.

3. Rolling stock :

- Harmonics from AC/DC converters, inverters or choppers.
- Arcing to pantograph bounce.
- ACs, Wi-Fi, infotainment, hand held devices.

Requirements of EMC directives :

The earthing and bonding system should be as per RDSO specn no. RDSO/SPN/197/2008.

(\* Extract of RDSO Guidelines vide L.No.STG/IH/ML dt.10.07.09)

Consequent to damage of Microlock-II EI due to lightning at a few stations on ECoR, implementation of an earthing improvement scheme comprising of following three stages was decided. Zonal Railways and the firm were accordingly advised vide this office letter of even no. dated 14.03.2008.

Stage 01      • Shielded cable between Termination Rack and Control Panel is to be properly grounded at the Termination side.

- Microlock-II Racks which are having epoxy coating be provided with copper foil.
  - Separate DC 24V supply to be used for Microlock-II cooling fan.
  - Ensuring proper copper connection of Room Earth Bar and Earth points Ensuring earth resistance value < 1 Ω.
- Stage 02      The serial port of one Microlock-II to another Microlock-II will be isolated (using opto-isolators) if the stations is located in high hazard lightning area (having more than 50 Average thunder Storm days per year).
- Stage 03      Provision of augmented surge protection arrangement for the non-vital output board lines in case the operating panel room (SM's room) and the equipment room (EI room) are located in two different buildings.
- Complete Earthing, lightning and Surge Protection with Ring Earth scheme is done by the OEM as per the guidelines laid out in RDSO/SPN/197/2008. All the 24V input power supplies are protected by custom designed & validated Class D filter.
- As per RDSO spec no. RDSO/SPN/197/2008, good earthing system should have excellent electrical conductivity, high corrosion resistance and should be mechanically robust and reliable and the acceptable earth resistance at earth busbar shall not be more than 1 Ω. For achieving the above value, provision of loop earth consisting of more than one earth shall be done. The distance between two successive earth electrodes shall be minimum 3 m and max upto twice the length of the earth electrode ie. 6 mtrs approx. and linked using 25 x 2 mm copper tape(buried not less than 50mm below the ground level.) to form a loop using exothermic welding technique
- For equipotential earth busbar and its connection to equipments and surge protection devices in the equipment room refer drawing no. SDO/RDSO/E&B/002.
- Supplier shall be responsible for complete supply, installation & commissioning of the earthing and bonding system. The warranty of such system shall be 60 months from date of commissioning. Any failure during the above period shall be attended free of cost by the supplier.
- Copper strip of 150mm x 25mm x 6mm shall be exothermically welded to main earth electrode for taking the connection to the main equi-potential earth busbar (MEEB) in equipment room.
- Inspection chamber (300 x 300 x 300mm) shall be provided on top of the pit with lid (value should be written on the lid).
- Main equipotential earth busbar (MEEB) (300 x 25 x 6mm), SEEB (150 x 25 x 6mm) on individual rooms are to be provided.
- Main equipotential earth busbar (MEEB) to MAIN EARTH : 35sqmm multi strand single core PVC insulated cu cable as per IS:694 (duplicated)
- Main equipotential earth busbar (MEEB) TO Sub equipotential earth busbar (SEEB) : 16sqmm multi strand single core PVC insulated cu cable as per IS:694
- Sub equipotential earth busbar (SEEB) TO INDIVIDUAL EQPTS : 10sq. mm multi-strand single core PVC insulated cu cable as per IS:694
- MAIN EARTH to other EARTH PIT : in case of loop earth copper tape 25 x 2 mm other should be used.

#### Protection devices comparison

Types of Protection	Device used	Clamping voltage	Energy capacity	Responsive time	Cost
Class B	Spark gap	High	High	Slow	Moderate to high
Class C	MOV	medium	High	Medium	less
Class D	TVSS or Transzorb	Low to medium	Low	Fast	moderate

Following are the guidelines given by RDSO regarding earthing and bonding requirements for EI installations :

Equi-potential bonding of all the equipments is an essential requirement for effective lightning and surge protection.

For external lightning protection system for the building/structure normal franklin rods of 3m height made of copper are to be provided.

At some locations it may not be possible to form a perimetric ring earth around the EI room, power supply room and station room. In such situations, parallel earthing arrangements consisting of inter connected multiple earth electrode may be made at the free space near the station building such that following requirements are made:

- (a) Single point entry of main earth bond with all other cables to the EI room shall be adhered.
- (b) The earth connections to the perimetric ring earthing for all the items shall be made using the shortest possible path and preparation of drawing for perimetric earthing and bonding depending upon the locations.

The Bonding Ring Conductor (BRC) has an objective to maintain the low inductance common Bonding Network (CBN), hence it is not necessary that a complete closed loop has to be formed for bonding ring conductor in the rooms, specially near the doors, windows. BRC can be terminated on the walls without crossing the doors and windows. However, all the equipments shall be connected to BRC using shortest possible path.

All electrical connections to the earth electrode at the rods and on the GI or copper tapes should be suitably welded for high conductivity, long term reliability and reduced maintenance.

Internal earthing network must be very low inductance to pass high unwanted surge currents, without developing high voltages at any point in equipment/power room and so prevent damage to persons and equipment.

All metal work and equipment must be bonded equi-potentially to prevent possibility of unwanted surge currents creating differential voltages at equipment either due to unwanted inductive or capacitive coupling.

All earth bonds, cables, wires etc. must be as short and straight as possible to maintain low inductance. This is essential for surge protection devices to work correctly.

Unwanted surge currents entering equipment room must be dissipated to the earth electrode as close as possible to their point of entry.

Ideally, there should only ever be one point of entry from external environment into equipment room for all cables, e.g. power, signaling, telecommunication.

All earth bonds, cables and wires are classified as "dirty" and must not be run through cable trays carrying "clean" signaling and "clean" power circuits.

Conductors entering the building could be carrying lighting currents or voltage transient and are considered to be "dirty". Internal conductors after the earth bonding point, and surge protection where appropriate are considered "clean". All other circuits should be classified as "clean" or "dirty" and segregated accordingly.

The wires of all circuits including power circuits should be twisted or at least bundled ensuring that for every B (positive), there is the complementary N (Negative) in the twist or bundle and for every BX there is the complementary NX in the twist or bundle. All wiring twisted wherever possible so opposite poles are always in close Proximity.

Wherever the distance between the respective rooms of Station Equipment Room, Power Supply Room and Station Master Room is greater than 25 meters, the room/part of building away from the main building or its part should have a dedicated earthing system.

Earthing is an installation related job, there may be factors related to workmanship, quantity and quality of material used, installation procedure, season of installation etc. which may result in slight increase in resistance beyond  $1\Omega$  after some period of installation, but this slight increase will not have major impact on dissipation of fault/surge currents by the earthing system.

Earth enhancement compound with resistivity less than  $0.2\Omega$  meter consisting mainly of Portland cement and graphite but not bentonite (or any other chemical) has to be used to improve the conductivity and reduce the soil resistivity around the earth electrode and 30-35 Kg of earth enhancement compound has to be used for one earth pit where the augured hole dia is 100-125 mm. Value of earth resistance of less than  $1\Omega$  can be achieved by using 2-3 pits.

Hence, it is considered that on most of the installations on Indian Railways, 2 - 3 earth pits going upto 4 earth pits is sufficient for achieving earth resistance less than  $1\Omega$ . There may be specific installations having rocky area, sandy soil etc. where more than 4 pits may be required for achieving earth resistance less than  $1\Omega$ .

#### 4.5 POWER SUPPLY REQUIREMENTS

Non-regulated 230 Volts, 50 Hz single phase or three phase, multiple supply shall be provided for EI functioning subsequently other power supply requirements for MT, VDU, OC etc. including backup of at least four hours (to prevent shutting down of system due to fluctuations in main supply) are provided . The system shall work satisfactorily with input voltage variation from 150V to 275V AC and frequency variation from 48 Hz to 52 Hz. Auto change over arrangement for selection of available multiple Power Supply sources are provided. The details of Power supply are specified by the purchaser.

- (a) Separate power supplies are used to drive EI equipment and other Signalling Gears
- (b) DC-DC converters shall be capable of working in non-air conditional environment and ambient temperature range between  $-10^\circ\text{C}$  to  $+70^\circ\text{C}$  and Relative Humidity upto 95% at  $40^\circ\text{C}$ .
- (c) Over voltage & short circuit protection with self restoring type arrangement to be provided.
- (d) The required protection shall be provided to protect from any malfunctioning due to false/ spurious feed.
- (e) Suitable surge protection and proper earthing arrangement shall be provided in the power supply system to protect against transient voltages, lightning and spikes etc. As per IEC norms Firm shall provide a document capturing the installation, maintenance methods and working instruction prior to installation. The compliance of the following standards shall be evidenced in the above such document

IEC 61000-5-2

IEC 62305-3 & 4

IS 3403

RDSO/SPN/165/2012

RDSO/SPN/197/2014

- (f) The EI shall work on 110V/ 60V/ 24V/12V DC power supply.

- (g) If CCIP and CIU are in separate building, then lightning and surge protection has to be provided for each core of copper cable connecting CCIP and CIU or else OFC cable shall be used to connect CCIP & CIU.
- (h) A detailed Power supply arrangement diagram/ circuit shall be provided.
- (i) Power supply arrangement for individual processor should be such that, in case of fault in power supply of one processor, all processors should not cease to function simultaneously. It should be possible to switch off and take out faulty processor for repairing/replacement without affecting working of the balance system.

#### 4.5.1 Power supply features

- (a) The Power supplies for the different sub-systems have been designed to have adequate safety factors.
- (b) Power supply cards are provided with input under voltage and over voltage protection.
- (c) Power supply cards are provided with output overload and over voltage protection.

#### 4.5.2 Power Supply arrangement (From TAN)

- (a) 110 volt DC supply from IPS room to EI rack shall be provided with duplicated Cable with suitable gauge for redundancy, ensure that voltage drop in cable shall not to be More than 1 Volt from IPS(integrated power supply). Cable voltage drop is restricted to 1 volt to avoid overloading of cable & also ensure correct AWG quality of wires.
- (b) DC-DC converters provided for Electronic Interlocking system shall be segregated for 'A' & 'B' systems along with segregation of cabling and termination for power supply up to DC-DC converters, all the converters shall be in N+1 Configuration. It is also advised that more reliable (RDSO Approved) DC-DC Converters shall be considered for better reliability. This is provided for the better supply arrangement with redundancy for main/standby EI system to get high availability and reliability. Also the segregation between CIU & OC or other peripherals of EI provides redundancy so that in case of failure of one set of DC-DC converter whole EI equipment will not shut down.
- (c) DC-DC converter shall be installed near to EI rack or in the EI rack itself to avoid the line drop. The line drop shall not be more than 0.5 volt. This arrangement is provided to avoid high drop in line voltage so that full operating voltage is available to the system.
- (d) It is advised for better reliability that each OC, CIU shall have separate DC- DC Converter preferably near the CIU, OC rack and shall be in N+1 configuration. 110 V DC supply shall be taken from IPS battery bank to CIU, OC and PPM rack in Redundant manner with separate core of wires.
- (e) Where ever Panel Processor module is installed in the SM room, 110 volt DC power supply shall be provided from EI or from IPS room with duplicated cable arrangement. Panel Processor module shall have separate DC-DC converter in N+1 configuration. It is seen normally that 12V/24V power supply is directly taken from IPS room to Station Master's room which are normally more than 25 meters away. This lead to lot of voltage drop in cables as well as in heating of the cable.
- (f) 24 V or 110 V DC supply for CPU fan shall be fed with separate external supply(from IPS), which should be completely isolated from Electronic interlocking supply and same shall be provided with fuse to avoid effect of inductive loading of DC-DC supply of main EI equipment which normally results in resetting of the system and it also avoids failure of DC-DC converters in case the fan become short-circuit.

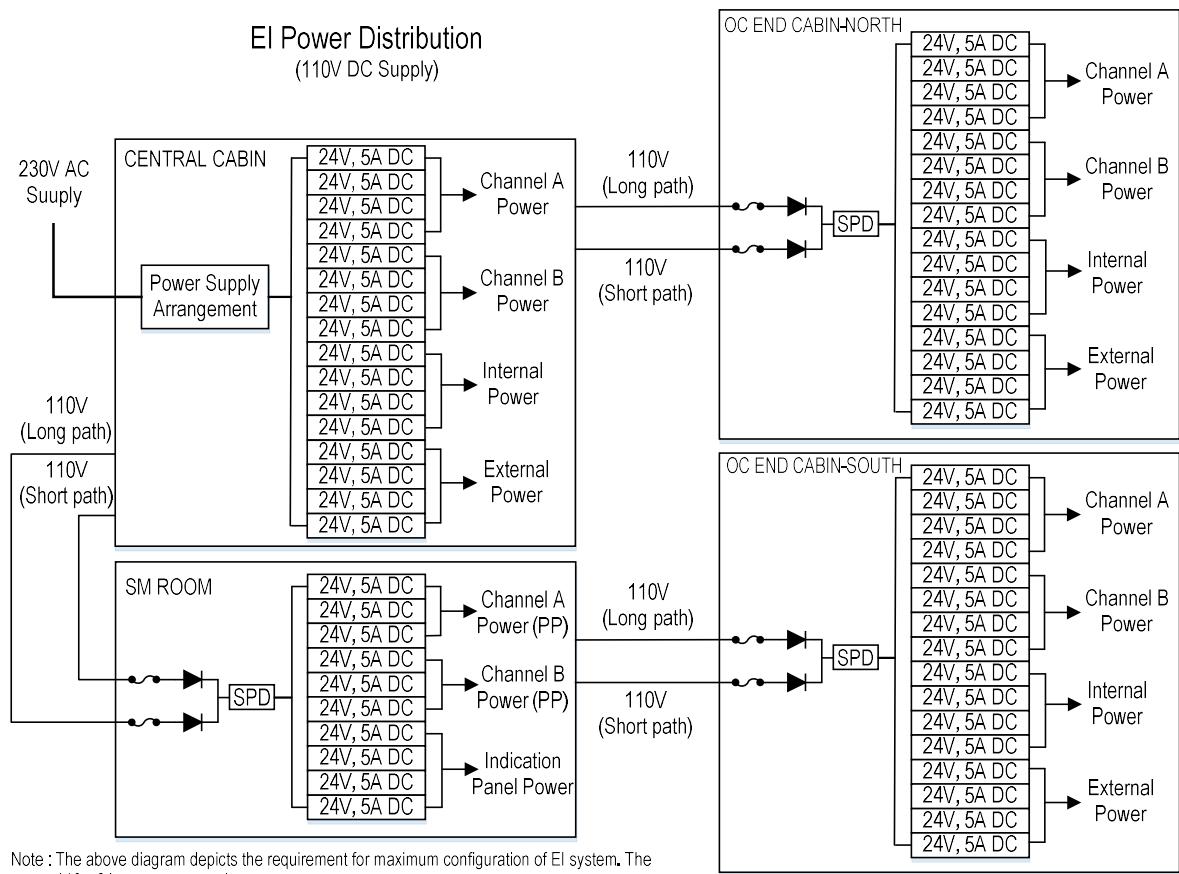


Fig 4.11 EI Power distribution

#### 4.5.3 Ansaldo Electronic Interlocking (MLK-II)

ANSALDO requires power supply of 12 V DC for Card File, 24 V DC for INPUT/OUT cards and 5 V DC for RTC (Real Time Clock) &Event Log Modules. The Power supply to the Embedded Computer is taken from IPS separate modules with Suitable size of the cable and it is done as per the Interface circuits with suitable surge suppresser. The required power supply to the Card file modules is 12V DC to be wired separately for Systems A and B. i.e one pair for System A and another pair for System B. Power bus bars to be duplicated from IPS room to relay room. i.e single failure (wire cut) should not affect the system. Separate DC-DC Converter for Input/output Boards & Panel power (24V) provided with N+1 configuration. DC-DC converter shall not be earthed. Provide redundant power supply terminal parallel for input/output module for B/N 24V supply.

Power supplies and wiring connection for vital input and output board should be isolated from the other power supplies of EI. Separate DC-DC Converter for RTC & Event Log Backup (5V) for MLK warm stand-by configuration to be provided with N+1 configuration separately for Systems A and B.

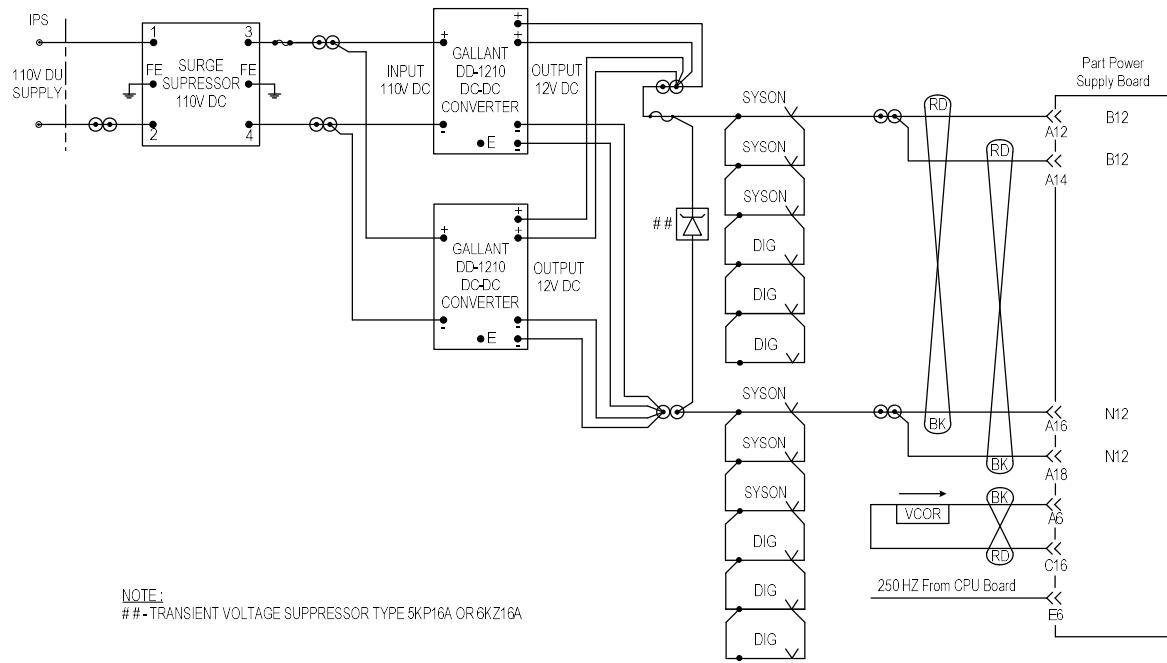


Fig 4.12 MLK-II Card file Power Supply Arrangement

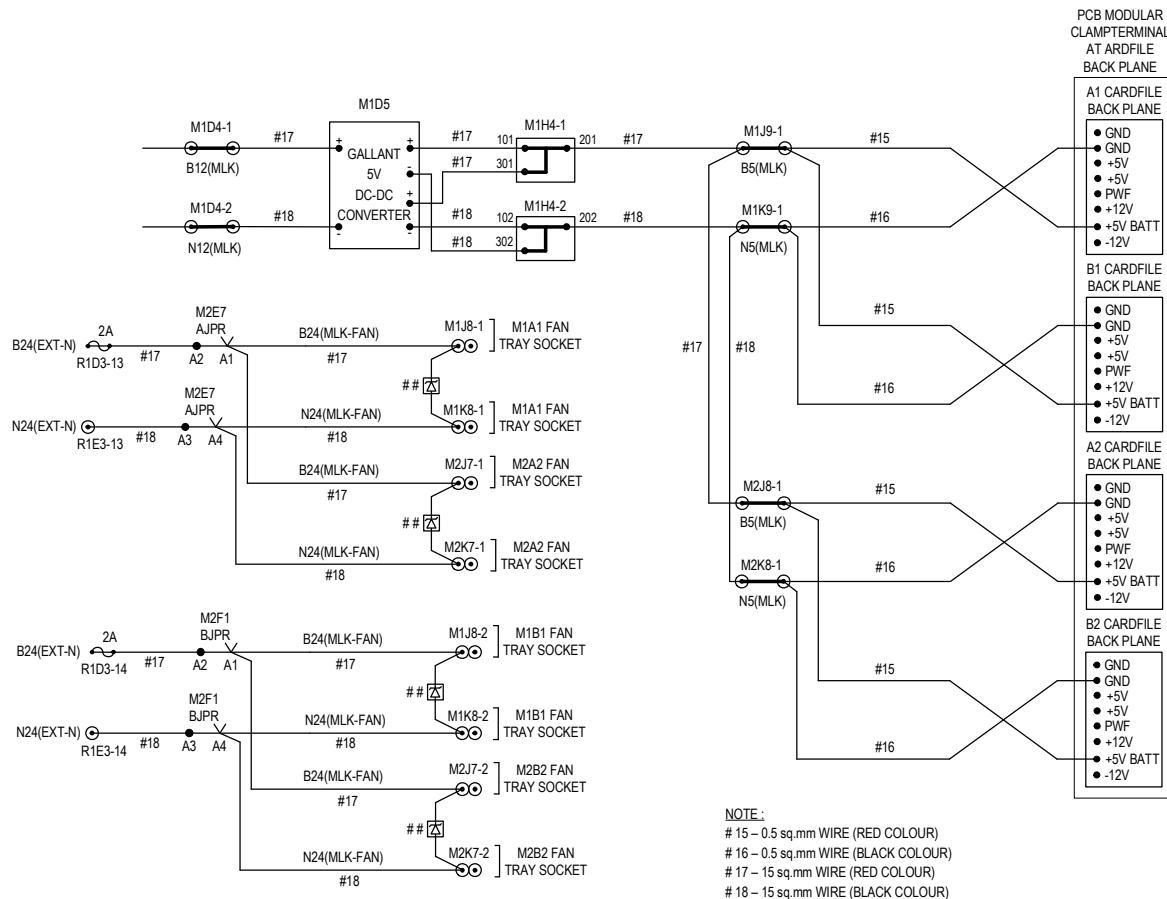


Fig 4.13 MLK-II Other than Card file Power Supply Arrangement

#### 4.5.4 Westrace Electronic Interlocking

WESTTRACE requires 24V DC for system operation busbar voltages shall be within the range 22V to 25.8V and 50 V DC supply for powering up VPIM (Vital Parallel Input Module) and VROM(Vital Relay Output Module) modules, 50V busbar voltage shall be within the range 48V to 52V. This is usually taken from a float charging Battery. It can be taken from other reliable power supply source like AC-DC converter, DC-DC Converter or IPS.

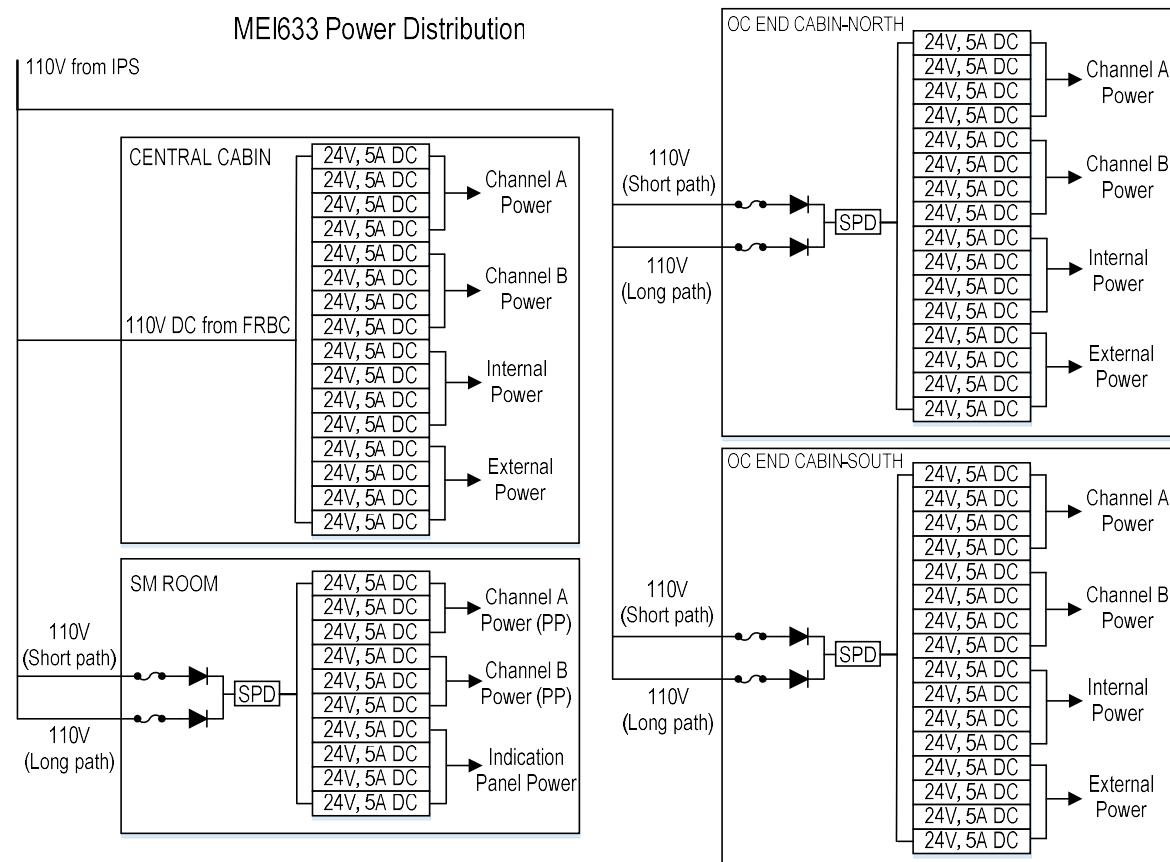
All the fuses are provided with LED indications. If any fuse is blown off then the particular LED in the fuse terminal will glow. Replace the fuse with the correct rating.

#### 4.5.5 Medha Electronic Interlocking (MEI633)

Medha Integrated Power supply (MIP100) is used as power source for MEI633. As per the requirement power source is customized. If 110 V DC is available then 110 V - 24 V DC-DC converters are provided otherwise 230 V AC supply with FRBC and DC-DC converters are provided. If entire station is need to be powered by IPS, full set of IPS (FRBC, ACDP and DCDP) is supplied. System power supply wiring should be as short as possible and must be isolated from noisy wiring of 230VAC.

Power supply (230 V AC) wiring for Maintenance/Operator PC shall be isolated from 24V DC supply to avoid noise. System Power wiring is to be done as per the interface circuits in terms of wire thickness and Standard colour code.

Use proper Terminal & Lugs according to the wire thickness. Sharp bending should be avoided when routing into the equipment backplane. Proper Terminals / Connectors to be used as per the Interface circuits. Each terminal group is to be separated by using end stopper terminal.



Note : The above diagram depicts the requirement for maximum configuration of MEI633 system. The No. of 110V-24V converts in n+1 configuration will be decided according to the actual load condition.

Fig 4.14 MEI633 Power distribution

## **4.6 COMMISSIONING**

### **4.6.1 OEM Certification**

For the fool proof commissioning of Electronic Interlocking systems, RDSO has issued following guidelines vide letter No STS/E/AC/Digital/Genl. dt 22.06.2011.

- 1) The commissioning of any electronic interlocking system has to be carried out only by a RDSO approved vendor.
- 2) The installation has to be inspected as per the pre commissioning check list issued by RDSO for the EI systems and has to be submitted before commissioning.
- 3) The OEM has to issue a certificate in a format circulated with the above mentioned letter by RDSO.

In the certificate issued by the OEM, it will be stated that the execution of EI system installation has been carried with all arrangements like earthing, surge protection, power supply, power/communication cables and equipment wiring as per the standard practices of engineering to ensure trouble free functioning of the EI system.

The format for the OEM certification issued in this regard by RDSO is provided in Annexure-2.

### **4.6.2 Check list**

The manufacturer shall supply the Installation and maintenance manual with pre-commissioning check list. Before issuing safety certificate all the contents to be verified as per pre-commissioning check list.

A pre commissioning check list is issued by RDSO for each make of EI System. Every EI installation has to be inspected jointly by the representative of OEM and an authorized Railway official before commissioning .It has to be ensured that all the works mentioned in the pre commissioning check list are completed without any deviations and lapses. The completely verified check list has to be signed jointly by the representative of OEM and an authorized Railway official who carried out such inspection.

The pre commissioning check list issued by RDSO as per the make enclosed in IRISSET notes S18-A, S18-B, S18-C etc.

### **4.6.3 Safety certificate**

Both hardware & executive software of EI must meet SIL-4 as defined in CENELEC standards. The certificate of Independent safety assessor certifying that the system is equivalent to SIL-4 compliant shall also be submitted.

The EI system executive software should have been independently verified and validated including its offered configuration by third party. User Railway shall verify application software pertaining to yard data.

The firm manufacturing EI, when applying for type approval or cross acceptance approval shall submit documentary proof of independent validation as per CENELEC Standards or equivalent standards, along with complete safety case.

The software of VDU must meet SIL-2 as defined in CENELEC Standards. The certificate of third party Validator certifying that the VDU software is equivalent to SIL-2 compliant shall also be submitted.

**Fax:** 91-522-2452332  
**Telephone:** 2451200 Ext.42656  
0522-2465748 (DoT)  
**E-mail:** [dsig6@rdso.railnet.gov.in](mailto:dsig6@rdso.railnet.gov.in)  
[dsig6rdso@gmail.com](mailto:dsig6rdso@gmail.com)



मार्त सरकार – रेल नियंत्रण  
**Government of India – Ministry of Railways**  
अनुसंधान अधिकाल्य और मानक संगठन  
**Research Designs & Standards Organisation**  
लखनऊ-226011  
**LUCKNOW – 226011**

No. STS/E/AC/Digital/Genl  
नं० एसटीएस/ई/एसी/डिजिटल/जनरल

Dated: 22.06.2011  
दिनांक: 22.06.2011

1. M/s Central Electronics Ltd., 4. Industrial Area, Sahibabad (U.P)-201010.
2. M/s Elyne Electro Systems Pvt. Ltd., P-21 Old Ballygunge Road, Kolkata -700019.
3. M/s G.G.Tronics India Private Ltd., # 143/16, 4<sup>th</sup> Main, Industrial Town, Rajajinagar, Bangalore - 560 044
4. M/s Siemens Ltd, Mobility Division, R&D Technology Centre, Thane - Belapur Road, Near Airoli Rly Station, P.O. Bag No.: 85, Thane - 400 601
5. M/s Stesalit Limited, Park Plaza (N), 71. Park Street, Kolkata - 700016
6. M/s Kernex Microsystems(India) Ltd., 'Rajvistas'. # H, Avanthi Colony, Karkhana. Secunderabad-500 009.
7. M/s Webfil Limited, "YULE HOUSE", 8, Dr. Rajendra Prasad Sarani, Kolkata-7nnnm
8. M/s Deltron Equipment & Systems Pvt. Ltd., 26, Convent Road, Kolkata -700014

Sub: OEM certification for the installation before commissioning.

Please find attached a letter issued by RDSO to all Zonal Railways which necessitates that any commissioning of Electronics Equipment is only carried out by RDSO approved vendors. The letter also requires that a certificate to this effect is issued by approved vendors in the enclosed format.

Sd/-

Phone : Off - 0522-2450762 Rly. Off - 42650 Fax: 0522-2452332 e-mail: sredsignal@gmail.com		Senior Executive Director(Signal) Annexe-I Building, RDSO, Ministry of Railways, Manak Nagar, LUCKNOW – 226011(U.P.) INDIA
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No. STS/E/AC/Digital/Genl	Chief Signal & Telecom Engineer,	21.06.2011
		मुख्य सिग्नल एवं दूरसंचार अभियन्ता,
Central Rly., Mumbai, CST – 400001	मध्य रेलवे मुम्बई सी.एस.टी. - ४०० ००१	
Western Rly., Churchgate, Mumbai – 400020	पश्चिम रेलवे, चर्च गेट, मुम्बई - ४०० ०२०	
Eastern Rly., Fairlie Place, Kolkata 700001	पूर्व रेलवे, फेरिली प्लेस, कोलकाता - ७०० ००१	
South Eastern Rly., Garden Reach, Kolkata – 700043	दक्षिण पूर्व रेलवे, गार्डन रीच, कोलकाता - ७३	
Northern Rly. Baroda House, New Delhi-110001	उत्तर रेलवे, बड़ीया हाउस, नई दिल्ली - ०१	
North Eastern Rly., Gorakhpur- 273012	पूर्वोत्तर रेलवे, गोरखपुर - २७३ ०१२	
North East Frontier Rly., Maligaon, Guwahati – 781011	पूर्वोत्तर सीमान्त रेलवे, मालिगाँव, गुवाहाटी - ७८१ ०११	
Southern Rly. Park Town, Chennai – 600003	दक्षिण रेलवे, पार्क टाउन, चेन्नई - ६०० ००३	
South Central Rly., Secunderabad – 500371	दक्षिण मध्य रेलवे, सिकन्दराबाद - ५०० ३७१	
East Central Railway, Hajipur.	पूर्व मध्य रेलवे, हाजीपुर।	
East Coast Railway, Rai Vihar BDA Rental Colony, Chandrasekharpur, Bhubneshwar – 751023	पूर्व तटीय रेलवे, रेल विहार बी.डी.ए. रेन्टल कालोनी, चन्द्रशेखरपुर, भुवनेश्वर-७५१०२३	
North Central Railway, Block A-1, 2 <sup>nd</sup> Floor, Subedarganj, Allahabad-211033.	उत्तर मध्य रेलवे, ब्लॉक ए-१, २ <sup>nd</sup> फ्लोर, सुबेदारगंज, इलाहाबाद-२११०३३.	
North Western Railway, Jaipur – 300206	उत्तर पश्चिम रेलवे, जयपुर-३००२०६	
South Western Railway, Club Road, Keshavapur, Hubli – 23	दक्षिण पश्चिम रेलवे, केशवपुर, हुबली-२३	
West Central Railway, GM Office, Jabalpur	पश्चिम मध्य रेलवे, जी.एम. कार्यालय, जबलपुर	
South East Central Railway, R.E. Office Complex, Bilaspur – 495004	दक्षिण पूर्वमध्य रेलवे, आर.ए.ओ. ऑफिस काम्पलेक्स, बिलासपुर - ४९५००४	
Chief Signal & Telecom Engineer, Metro Railway, 23-A, Jawaharlal Nehru Road, Kolkata – 700071	मुख्य सिग्नल एवं दूरसंचार अभियन्ता, मेट्रो रेलवे, २३-ए, जवाहर लाल नेहरू रोड, कोलकाता - ७०० ०७१	
Chief Signal & Telecom Engineer, CORE, Nawab Yusuf Road, Civil Lines, Allahabad-211001	मुख्य सिग्नल एवं दूरसंचार अभियन्ता, कोर, इलाहाबाद - २११ ००१	
Director, IRISET, Secunderabad.	निदेशक, ईरीसेट, सिकन्दराबाद	

## Sub OEM Certification for the installation before commissioning.

It has been noticed that there are large number of failures of electronic systems on the Indian Railways and whenever joint inspections have been done to investigate the failure, it has come to the notice that there were number of deficiencies in the installations in regard to earthing, surge protection, power supply and adjustment of various system resulting in to the failures.

In order to ensure that equipment is properly installed and commissioned by adhering to pre-commissioning check-list and procedure as defined by OEM in its installation manual, it is necessary that electronic signaling systems, as defined below, are installed and commissioned by RDSO approved vendor and a certificate is issued to railways in the given format:

- a) EI
- b) SSDAC/MSDAC
- c) UFSBI/BPAC
- d) AFTC
- e) IPS
- f) Data Logger

RDSO has already issued pre-commissioning check-list for each of the above items and the same is required to be meticulously followed We are also advising all the RDSO approved vendors of above items to ensure compliance of the above.

Sd/-

OEM's Site Installation Certificate

To

CSTE/ Railway

This is to certify that verification of system installation (details given below) has been completed by undersigned (OEM representative) and all necessary arrangements like earthing, surge protection, power supply, power & communication cables, and equipment wiring meet the required standards of engineering for trouble free working of installed system.

1. System being commissioned :-
2. Station/Section :-
3. Division :-
4. Date of commissioning :-

---

Name of RDSO approved Original Equipment manufacturer:

---

Name of OEM representative with Designation:

---

Signature of OEM representative with Date:

**OEM's Site Installation Certificate**

To,

Date: 20-05-2012

DY.CSTE/CN/BNC

This is to certify that verification of system installation has been completed by Ansaldo and all necessary arrangement like earthing, surge protection, powers up pty, power & communication cables and equipment wiring meet the required standards of engineering for trouble free working of the installed system, subject to the points mentioned in the annexure.

System being commissioned : Electro nit Interlocking (Microtek II)  
Executive Version-CC3.0

Station/Section : SETTIHALLI(SET)

Division : BANGALORE

Expected Date of Commissioning : 20-May-2012.

**ANSALDO STS Transportation Systems India Pvt. Ltd.**

Name of the RDSO Approved Original Equipment Manufacturer

**ASTS Construction & Commissioning Engineer.**

Name of the OEM Representative with Designation

SIVA KUMAR.R

*Ramurthy 20/05/12  
(Site Engr.)*

Signature of the OEM Representative with Date

Attached: Annexure on observations

Annexure of OEM certificate

Observation on installation

Station: SETTIHALLI(SET), Division: Bangalore (SBC division)

Region: South western railway.

Equipment installed: Electronic interlocking (Microlok-II) version-CC3.0 warm stand by with dual operator VDU.

Consideration:

- All Earthing connections shall be checked periodically according to the maintenance schedule to ensure satisfactory operation of the system. Based on the contract earthing scheme has been done as per the old scheme specified to Spec, No. RDSO/SPN/197/2008 and the new earthing scheme is not implemented.
- The installation has been carried out based on the drawings and application logic approved by railway. This certificate only verifies and assures that the installation has been carried out based on the documents approved by Railway.(Indoor only)
- This certificate is valid for the system configuration and application logic approved by ansaldo and also by railway. Any change in either of the system configuration application logic and interface circuits without the knowledge of ansaldo in writing will make this certificate null and void.

## CHAPTER 5 SAFETY ISSUES

### 5.1 RAMS

This Standard defines a systematic Process for the Specification and Demonstration of the Dependability requirements for the Railway industries. Dependability is a characteristic of a System's long term Operation and is achieved by the application of established Engineering Concepts, Methods, Tools and Techniques throughout the Life-cycle of the System. The Dependability of a System can be characterised as a Qualitative Indicator of the degree up to which, the System / Subsystem / Components, can be relied upon to function as Specified, and to be both Available and Safe. For the Railways, Dependability is a generic term, which includes all aspects of Reliability, Availability, Maintainability and Safety (RAMS) and the interactions between them.

Reliability is the Probability that an Item can perform a required Function under given Condition for a given Time Interval  $t_1$  to  $t_2$ .

Availability : is the Ability of a Product to be in a state to perform a required Function under given Condition at a given instant of Time or over a given Time Interval assuming that the required External Resources are provided.

Maintainability : is the Probability that a given active Maintenance action, for an Item under given Conditions of use can be carried out within a stated Time Interval, when the Maintenance is performed under stated Conditions and using stated Procedures and Resources.

Unacceptable Risk

Safety is the freedom from of harm.

Relationship of RAMS to Railway Dependability is shown in the following figure:

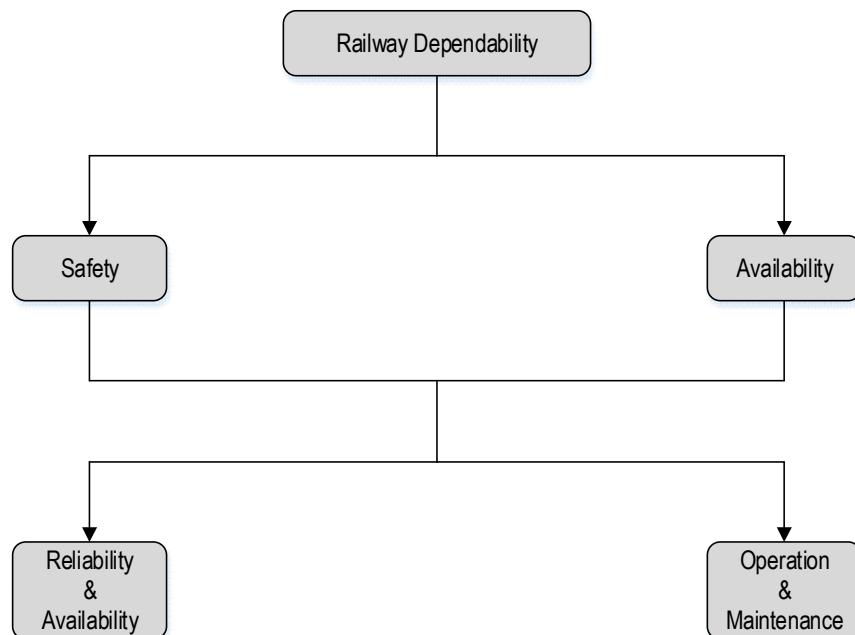


Fig 5.1 Relationship of RAMS to Railway Dependability

Safety are inter-linked : A weakness in either of them or the mismanagement of their conflicting requirements may result in an inability to achieve a Dependable System. The achievement of in-service Availability and Safety Targets can be possible by meeting ongoing Reliability and Maintainability requirements and controlling the long-term Maintenance activities and Operational environment.

## 5.2 FAIL SAFE MECHANISM

### 5.2.1 The Technical concepts of Reliability and Availability are based on the knowledge of

- (a) All possible System / Subsystem / Component Failure Modes, in the specified Application Environment.
- (b) The Probability of Occurrence of a System / Subsystem / Component Failure Mode.
- (c) The Cause of each Failure and its Effect on the Functionality of the System.
- (d) Efficient Failure Detection and Location.
- (e) Efficient Restorability of a Failed System.
- (f) Economic Maintenance over the required Life of the System.
- (g) Human Factors involved.

### 5.2.2 Safety and Risk are based mainly on the knowledge of

- (a) All Safety-related System Functions.
- (b) All possible Safety-related System Failure Modes in the specified Application and Environment.
- (c) All possible Hazards to the safe operation of the System and their Frequency of occurrence.
- (d) The Probability or the Rate of Occurrence of a Safety-related Failure Mode.
- (e) The Consequence of a Hazardous Event or a Safety-related Failure Mode.
- (f) The Probability that the Hazardous Event or a Safety-related Failure Mode will lead to an Undesirable Event or Accident when found in conjunction with, a Chain of other simultaneously occurring Incidents.
- (g) The Safety Protective Features and Risk Reduction Measures.
- (h) Influence of Human Factors, on the Safe Operation of the System.

### 5.2.3 Factors affecting Railways Dependability

The Dependability of a Railways System is influenced in three ways:

- (a) By Sources of Failure introduced internally within the System, at any Phase of the Life-cycle (System Conditions).
- (b) By Sources of Failure imposed on the System, during Operation (Operating Conditions)
- (c) By Sources of Failure imposed on the System, during Maintenance Activities (Maintenance Conditions)

The following Charts show the different factors affecting Dependability:

(a)

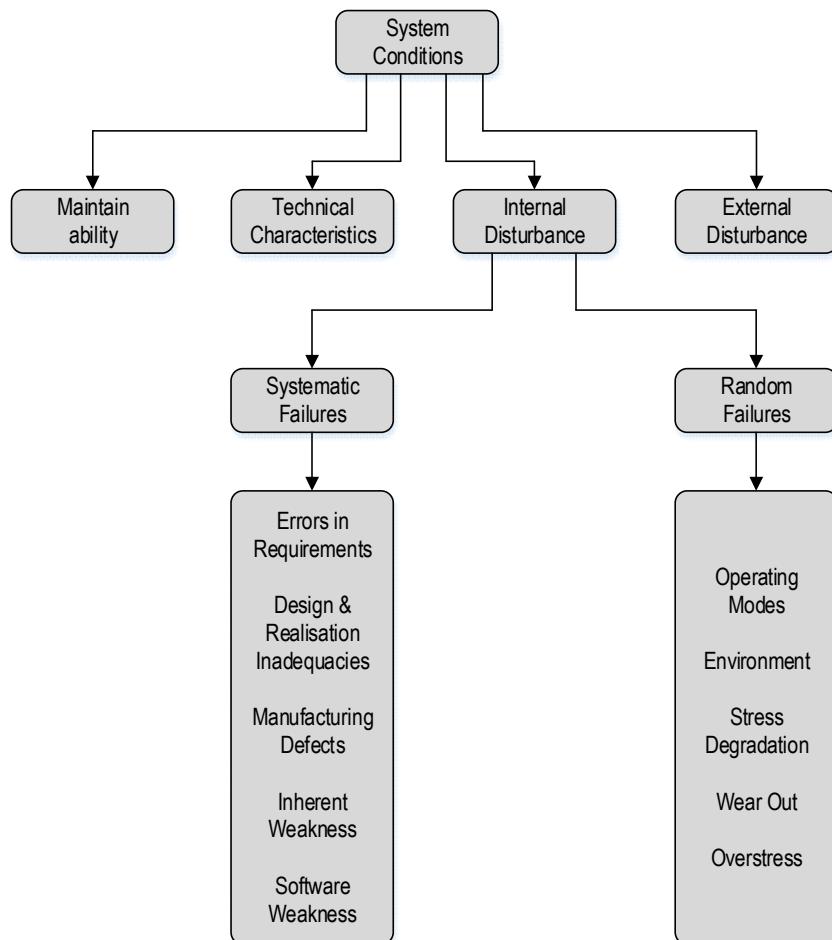


Fig 5.2

(b)

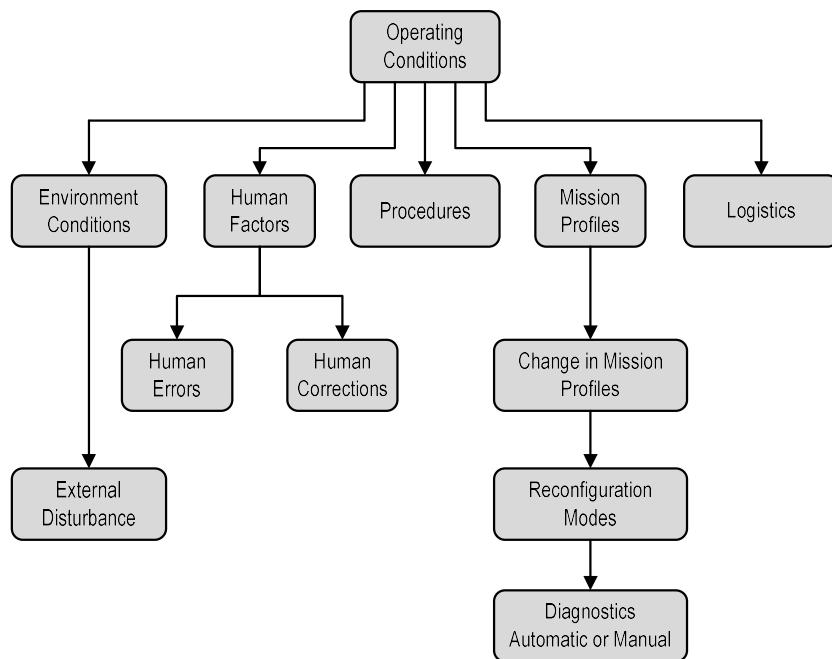


Fig 5.3

(c)

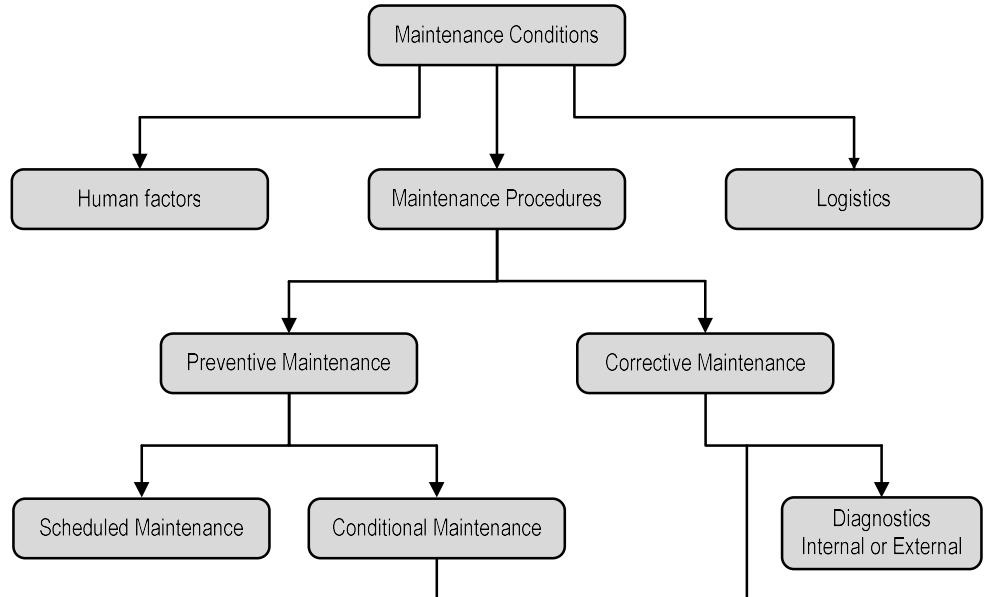


Fig 5.4

The potential effect of each Influencing Factor on the Dependability of the Railway System shall be evaluated, including the effect on each Phase of the Life-cycle, at a level appropriate to the System under consideration. The Process of Evaluation shall be repeated, when necessary and regularly reviewed to ensure that Evaluation remains valid and the Control Measures are adequate and effective. The Results of the Derivation, Assessment and Evaluation shall be documented along with any Assumptions or Justifications, made during the Tasks.

The Management Process for control on the Dependability supports the :

- Definition of Dependability Requirements
- Assessment and Control of threats to Dependability
- Planning and Implementation of Dependability Tasks
- Demonstration of Dependability Requirements Compliance
- On-going Monitoring of Compliance

Within all Systems, there is a possibility that an acceptable RAMS Performance will not be achieved. The Tolerable Risk of a Railway System is dependent upon the Safety Criteria, set by the Safety Regulatory Authority (RDSO in India). The Railway Authority shall define the specific requirement of the Process for the System under consideration. A Justification of the Adequacy of the Process adopted shall be recorded.

#### 5.2.4 System Life-cycle

The System Life-cycle process is a sequence of Phases, each containing Tasks, covering the Total Life of the System, from Initial Concept to Decommissioning and Disposal. The Life-cycle provides a Structure for Planning, Managing, Controlling and Monitoring all aspects of the System, including Dependability. This Standard acknowledges the balance between the RAMS Performance and the Life-cycle Costs. Responsibilities for all RAMS Tasks within each Phase, including the Interfaces between the Tasks, shall be defined and agreed to by the Project Organisation, where all Personnel involved must be competent to discharge their responsibilities.

Constraints on the RAMS Activities may be different for different Tasks.

For Reliability, Availability and Maintainability Tasks, Cost considerations are likely to be the Prime Mover, whereas, for Safety Tasks, achievement of an adequate Safety Level is most important. In this context, RAM and Safety requirements may conflict. RAMS Planning Documentation shall include these Conflicts. An adequate and effective Configuration Management System shall be established and implemented, addressing all RAMS Tasks within all Life-cycle Phases.

System Life Cycle contains the following phases :

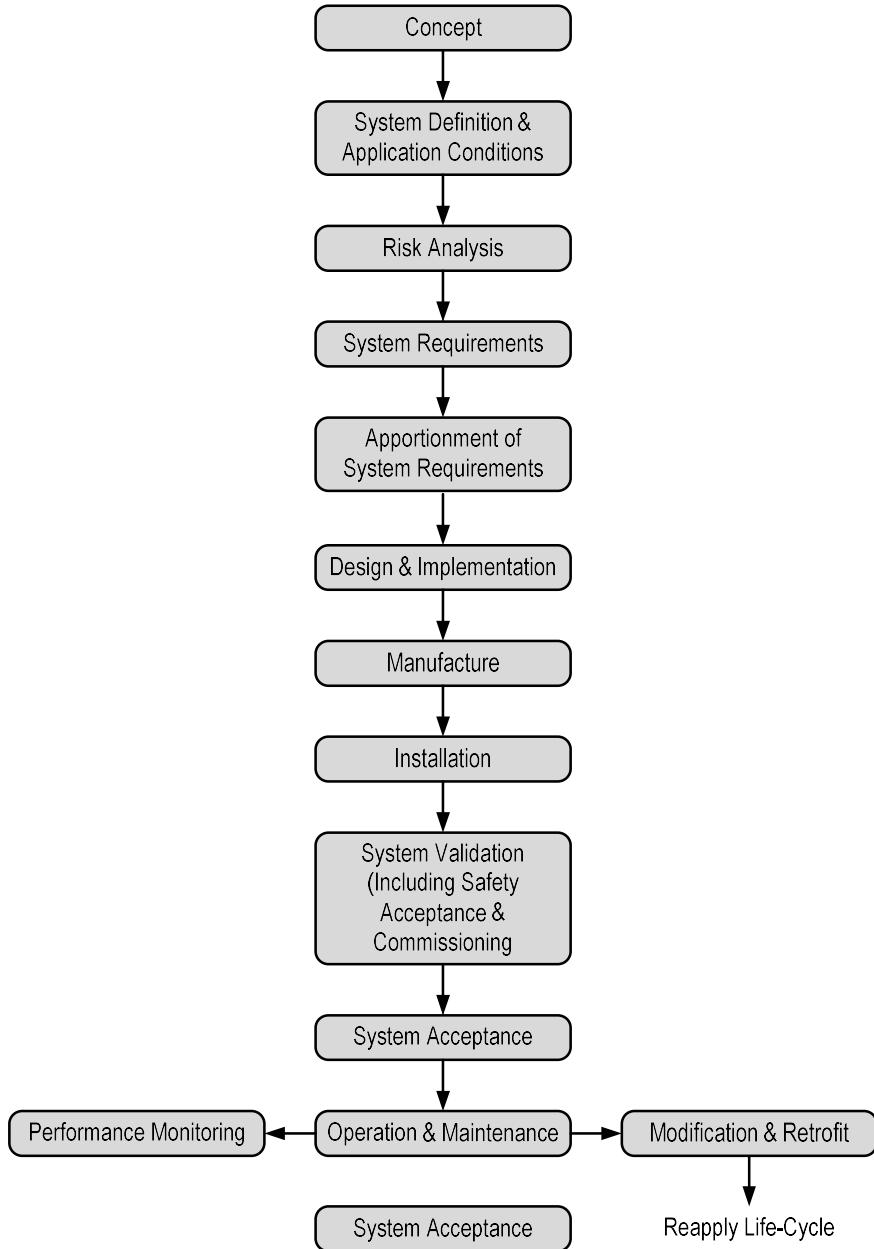


Fig 5.5

Concept Phase develops a level of understanding of the System sufficient to enable all subsequent RAMS Life-cycle Tasks to be satisfactorily performed. Input to this Phase are all the relevant Information, and if necessary Data, required for meeting the Requirements of this Phase, which are :

- Understanding of Scope, Context, Purpose and Environment of the System.
- Reviewing the RAMS Implication of any Financial Analysis and System Feasibility Studies.

- Identifying the Sources of Hazards
- Obtaining Information about any previous RAMS Requirements and achieved RAMS Performance of similar / related System.

System Definition & Application Conditions Phase defines the Mission Profile, Boundary and Scope of System Hazard Analysis. It also establishes the Application Conditions, RAMS Policy and Safety Plan of the System. Output of Concept Phase is the Input to this Phase.

Risk Analysis Phase identifies Hazards and Events leading to the Hazards, determines the Risks associated with the Hazards and establishes the process for Risk Management. This Phase classifies the Acceptability of the Risks and establishes the Hazard Log.

System Requirements Phase specifies the overall RAMS requirements of the System and the Acceptance Criteria for RAMS and also establishes RAM Program to control RAMS Tasks.

The next Phase, Apportionment of System Requirements, allocates the Functional and Safety Requirements (include Safety Integrity Level) of the designated subsystem, component and external facilities, it reviews Safety Plan to ensure the planned Tasks are consistent with the System Requirements.

Design & Implementation Phase creates and demonstrates Subsystems and Components conforming to RAMS Requirements, it defines, verifies and establishes a Manufacturing Process capable of producing RAMS validated Subsystems and Components. An important part of this Phase is the development of a Safety Case for the System.

Jobs done in Manufacturing and installation Phases are explained by their names themselves.

System Validation (including Safety Acceptance & Commissioning the Phase, which Validates that the total combinations of Sub system & Components and External Risk Reduction measures comply with the RAMS Requirement of the System.

System Acceptance Phase does the Assessment of the compliance of Total combination of Subsystems, Components and External Risk Reduction measures, with the RAMS Requirement of the System. It formally Accepts the System for Entry in to the Service, if found Appropriate.

Operation & Maintenance Phase Operates, Maintains and Supports the Total combination of Subsystems, Components and External Risk Reduction measures, such that compliance with System RAMS Requirements is maintained. This Phase regularly Reviews and Updates Operation and Maintenance Procedures. System Training Documentation and Hazard Log and Safety Case.

The objective of the Performance Monitoring Phase is to Maintain confidence in RAMS Performance of the System. It does Performance Analysis on a regular basis.

The Modifications & Retrofit controls System Modification and Retrofit Tasks to maintain System RAMS Requirements.

The last Phase in the Life-cycle is Decommissioning and Disposal, and it controls System Decommissioning and Disposal Tasks. It plans a safe closing down of the System and any associated external facility.

### 5.2.5 Parameters of RAM

Reliability Parameters are:

- Mean Time Between Failure (MTBF)
- Failure Rate
- Failure Probability
- Useful Life

Availability Parameters are:

- Adherence to Schedule
  - Passenger based Proportion Index
  - Downtime

Maintainability Parameters are:

- Mean Time To Repair (MTTR)
  - Time for Replacement
  - Time for Preventive Maintenance
  - Time for Corrective Maintenance
  - Fault Coverage
  - Repair Coverage

## 5.3 READ BACK CONTROLS

All vital outputs of EI are read back into the system continuously to monitor integrity, detection of false/foreign feeds etc. Comment: The following RDSO guidelines to be followed for read back the status of output relays in Electronic Interlocking (EI). (RDSO Policy Letter No. STS/L/SSI/CA/IRSI dated 05.09.2011)

Firm Name	EI Model	Reading back of Front/Back contact of the relay adopted
M/s Ansaldo, Bangalore	Mocolok II	Reading back Front contact only
M/s GETS, Bangalore	VHLC	Reading back Front contact only
M/s Siemens Ltd., Mumbai	SIMISS	Reading back Front & Back both contacts
M/s Medha Servo Drives (P) Ltd. , Hyderabad	MEI633	Reading back Front & Back Both contacts.

Interlocking have the capacity to work at complete safety as per their design, however, to consider against inadvertent operations, it is advised that in metal to carbon relays used in conjunction with Electronic interlocking at least front contact should be read back by Electronic interlocking for the output relays and in case of any non-conformity, the Electronic Interlocking shall go in shut down mode.

Sd/

## 5.4 CENELEC SPECIFICATIONS FOR RAILWAY SIGNALLING

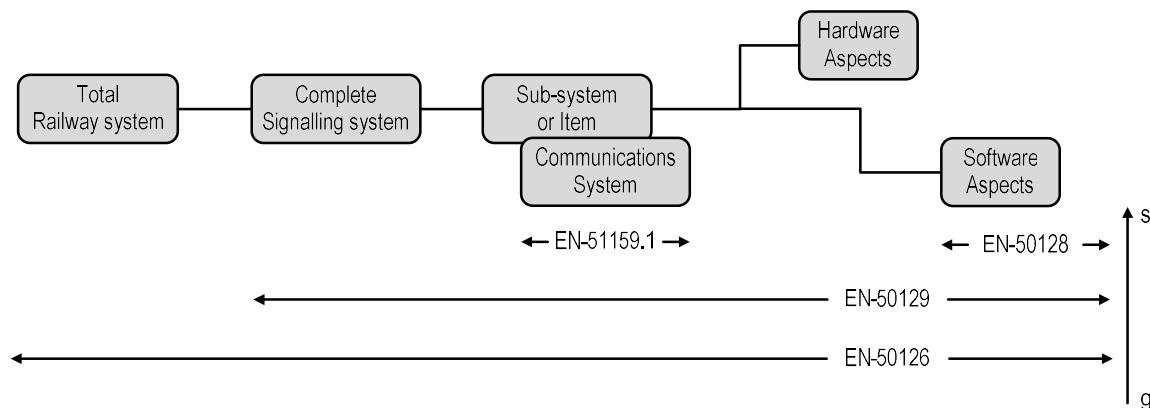


Fig 5.6 CENELEC Specification for Railway Signalling

The Electromechanical components like Relays, used in Railway Signalling for Interlocking, have some inherent fail-safe characteristics of their own. A Relay releases if the operational circuit is either open or short circuit. Again, a Relay cannot operate if intended or unintended (induced) current passes through the operating coil. But as we use any electronic component like a Transistor or an IC, there is a probability of stuck-at fault (due to open or short circuit failure of Junction) Moreover, due to their complex designs, failure modes of VLSI Chips like Microprocessors Microcontrollers, Field Programmable Gate Arrays, Complex Programmable Logic Devices etc. cannot be fully predicted.

This needs some guidelines in using these components in fail-safe safety critical Railway Signalling equipment. While designing these equipment, both Hardware as well as Software aspects are to be considered. Railway Signalling also must consider Reliability, Availability and Maintainability in addition to the Safety requirements. This is known as RAMS. Some International guidelines in the form of Standards are needed for safety related Hardware, Software and RAMS Design.

European Committee for Electro technical Standardization (CENELEC) has come up with several Standards, out of which, the following are to be considered for any Electronic component-based Railway Signalling equipment.

- EN 50121 – Electromagnetic Compatibility (EMC).
- EN 50126 – The Specification & Demonstration of Reliability, Availability, Maintainability and Safety (RAMS).
- EN 50128 – Software for Railway Control and Protection Systems.
- EN 50129 – Safety Related Electronic Systems for Signalling.

Besides these Standards if Communication Line is used in Railway Signalling as in the case of Block Signalling or Axle Counter, another Standard.

- EN 50159 – Signalling and Communications – Safety-related Communication – is also to be considered

Here we discuss the features of Standards EN 50126, 50128 and 50129

#### EN 50128

This Standard is applicable exclusively to Software and the interaction between Software and the System, in which the Software is used. It applies to all Software used in the development and implementation of Railway Control and Protection Systems including Application Programming, Operating Systems, Support Tools and Firmware. The use of Standard Commercially available Software and Tools is addressed by this Standard.

#### 5.5 SIL STANDARDS

The Software Safety Integrity Level shall be specified following the general process for obtaining the SIL as per CENELEC Standard EN 50126. The required Software Safety Integrity Level shall be decided on the basis of Level of Risk associated with the use of the Software in the System and the System Safety Integrity Level. Except at Software Safety Integrity Level 0, the safety process shall be implemented under the control of an appropriate Safety Organization, which is compliant with EN 50129. All Personnel involved in all the Phases of the Software Life-cycle, including Management Activities, shall have the appropriate Training, Experience and Qualifications, justified with the requirement of the particular application.

An Independent Assessor of the Software shall be appointed and he / she shall be authorised to perform the Assessment of the Software. The Assessor shall be approved by the Software Authority. The Designer / implementer, Verifier and Validator can all belong to the same Company but with the following restraints:

At SIL 1 & 2, Verifier and Validator can be the same person but they shall not be the Designer / Implementer.

At SIL 3 & 4, there are two options :

- (a) Verifier and Validator can be the same person but they shall not be the Designer / implementer. In addition, the Verifier and Validator shall not report through the Project Manager as is done by the Designer / Implementer. Moreover, they will have the Authority to prevent the release of the Software.
- (b) Designer / Implementer, Verifier and Validator must all be different persons. The Validator shall not report through the Project Manager and will have the Authority to prevent the release of the Software.

The parties responsible for various Tasks are as given in the Table below :

Task	Responsible Party
Software Requirements specification	Designer
Software Requirements Test specification	Validator
Software Architecture	Designer
Software Design and Development	Designer
Software Verification and Testing	Verifier
Software / Hardware Integration	Designer
Software Validation	Validator
Software Assessment	Assessor

A Life-cycle Model for the Development of Software shall be selected and shall be detailed in the Software Quality Assurance Plan (SOAP). Quality Assurance procedures shall run in parallel with the Life-cycle activities and use the same terminology. All activities to be performed in a particular Phase, shall be defined prior to the starting of that Phase. SOAP shall describe which Verification steps and Reports are needed. Traceability of all Documents, with Reference Number shall be provided for each Document.

Software Requirement Specification :

It describes a Document that defines a complete set of Requirements for the Software meeting all System Requirements to the extent needed by the Software Safety Integrity Level. It shall express the required properties of the Software being developed, but not the procedures to develop. The properties shall include — Functionality, Reliability, Safety, Efficiency, Usability and Portability. Software Requirement Specification shall identify and document all Interfaces with any other Systems, either within or outside the Equipment under control. All relevant modes of behavior of the Programmable Electronics, shall be detailed in this document. It shall also indicate the degree of Self-checking and the specified degree of Hardware checking by the Software. Requirements for all Safety Functions to be Testable, shall be included in the Software Requirement Specification. Further, a Software Requirement Test Specification shall be developed for verifying all the Requirements.

Software Architecture :

Software Architecture Specification shall consider the feasibility of achieving the Software Requirement Specification at the required Software Safety Integrity Level. It shall Identify, Evaluate and Detail the significance of all Hardware / Software Interactions. If any commercially off the Shelf (COTS) Software is to be used, that shall be included in Validation Testing and analysis of possible failures shall be carried out, keeping a validated Error Log.

If any previously developed Software is to be used, then it shall be clearly identified and documented. The suitability of this Software in satisfying the Software Safety Integrity Level must be justified. If the Software contains components of different Software Safety Integrity Levels, then all the components shall be treated as belonging to the highest Software Safety Integrity Level, unless there is documented evidence of Independence between the higher and lower Levels.

### Software Design and Implementation :

This helps in designing Software, which are Analysable, Testable, Verifiable as well as Maintainable. Module Testing is also included in this Phase. It shall describe the Software Design based on a decomposition in to Modules, with each one having a Software Module Design Specification and a Software Module Test Specification. When applicable, Automatic Software Test Tools and Integrated Software Development Tools shall be used. This shall take in to account the requirements of the Verifier and the Validator.

### Software Design Specification shall address :

- Software Components traced back to Software Architecture and SIL.
- Interfaces of Software Components with the Environment
- Interfaces between the Software Components
- Data structures
- Partitioning of requirements on components
- Main algorithms and sequencing
- Diagrams

### Software Verification and Testing :

A Software Verification Plan shall be created so that verification activities may be properly directed and that particular design or other verification needs may be suitably provided. This Plan shall document all the Criteria, Techniques and Tools to be utilised in the Verification Process for that Phase. It shall also describe the activities to be performed to ensure Correctness and Consistency with respect to the products and Standards provided as input to that Phase. Verification shall be carried out by an Independent Party to the extent required by the Software Safety Integrity Level and the result of each Verification shall be retained in a form defined or referred in the Software Verification Plan, in an Auditable way.

### Software Integration Test Plan shall document :

- Test Cases and Test Data,
- Types of Tests to be Conducted,
- Test Environment along with Tools. Configuration and Programmes and
- Test Criteria on which the completion of the Test will be declared.

Once the Software Requirements Specification has been established, Verification shall address the adequacy of Software Requirements Specification in fulfilling the System Requirement Specification, the System Safety Requirements Specification and the Software Quality Assurance Plan. After the Software Architecture Specification and the Software Design Specification are established, Verification shall address the internal Consistency of these Specifications and their fulfilling the Software Requirements Specification.

To the extent demanded by the Software Safety Integrity Level, the Software Source Code shall be verified to ensure conformance to the Software Module Design Specification and the Software Quality Assurance Plan. The results shall be recorded in a Software Module Verification Report. A Software Integration Test Report shall be produced in an Auditable form, stating the test Results and whether the Objectives and Criteria of the Software Integration Test Plan has been met.

### Software / Hardware Integration :

For SIL greater than Zero, a Software / Hardware Integration Test Plan shall be created early in the Software Development life cycle, so that the Integration activities may be properly directed and that particular Design or other Integration needs may be suitably provided. The Software / Hardware Integration Test Plan shall address :

- Test cases and Test Data.
- Types of Tests to be performed.
- Test Environment including Tools, Support Software and Configuration Description.
- Test Criteria on which the completion of the Test shall be declared.

The Software / Hardware Integration Test Plan shall distinguish between those activities which can be carried out by the Developer on his / her Premises and those which need access to the User's Site. It shall also distinguish between merging of Software on to the Target Hardware and System Integration. Tools and Facilities identified in the Software / Hardware Integration Test Plan should be available at the earliest practicable Time.

#### Software Validation :

It analyses and tests the Integrated System to ensure Compliance with the Software Requirement Specification with particular emphasis on the Functional and Safety aspects according to the Software Safety Integrity Level. Analysing and Testing shall be the main Validation activities. A Software Validation Plan shall be established and detailed in a suitable and Auditable Documentation. This Plan shall include a Summary, justifying the Validation Strategy (Manual and / or Automatic Technique, Static and / or Dynamic Technique and A analytical and / or Statistical Technique) chosen. The Software Validation Plan shall also identify the steps needed to demonstrate the adequacy of the Software Requirement Specification, Software Architecture Specification, Software Design Specification and Software Module Design Specification.

Validation Results shall be documented in the Software Validation Report, in an Auditable form. Once Hardware / Software Integration is finished, the Software Validation Report shall

- State whether the Objectives and Criteria of the Software Validation Plan has been met
- State the Test Results and whether the whole Software on the Target Hardware fulfils the requirements set out in the Software Requirement Specification.
- Ensure that the Test Cases and their Results shall be recorded in a Machine-readable form for subsequent Analysis.
- Ensure that the Tests should be Repeatable and be performed by Automatic means, if practicable.

The Software Validation Report shall document the Identity and Configuration of the Hardware and Software used, the Equipment used, Calibration of the Equipment, the Simulation Models used, the Discrepancies found and the Corrective Actions taken.

#### Software Assessment

This stage evaluates that the Life-cycle Processes and Products resulting are such that the Software is of the Software Safety Integrity Level and is fit for its intended application. The Software Assessor, who shall be Independent of the Design Team, shall have access to the Design and Development Process and all Documents, related to the Project. Assessor shall decide whether appropriate methods have been selected and applied at each Phase of the Software Life-cycle. If needed, Assessor may ask for additional Verification and Validation work. The final Software Assessment Report shall include a statement as to the Software Safety Integrity Level, achieved by the Software.

#### Software Maintenance :

It ensures that the Software performs as required, preserving the required Software Safety Integrity Level and Dependability when making Corrections, Enhancements or Adaptations to the Software itself. Procedures for the Software Maintenance shall be established and Recorded in the Software Maintenance Plan. Maintenance shall be performed with the same level of Expertise, Tools, Documentation, Planning and Management as the initial development of the System. A Software Maintenance Record shall be established for each Software Item before its first release, and it shall be maintained. A Software Change Record shall be established for each Maintenance Activity.

The following Table shows various Software Assessment Techniques :

Techniques	SIL 0	SIL 1	SIL 2	SIL 3	SIL 4
Check-lists	HR	HR	HR	HR	HR
Static Software Analysis	R	HR	HR	HR	HR
Dynamic Software Analysis	—	R	R	HR	HR
Cause & Consequence Diagrams	R	R	R	R	R
Event Tree Analysis	-	R	R	R	R
Fault Tree Analysis	R	R	R	HR	HR
Software Error Effect Analysis	—	R	R	HR	HR
Common Cause Failure Analysis	—	R	R	HR	HR
Markov Modelling	—	R	R	R	R
Reliability Block Diagram	—	R	R	R	R
Field Trial before Commissioning	R	HR	HR	HR	HR

R – Recommended,

HR – Highly Recommended

Table 5.1 Various Software Assessment Techniques

EN 50129

The conditions for Safety Assurance are presented in this Standard under three headings evidence of Quality Management, Evidence of Safety Management and Evidence of Functional and Technical Safety. All these conditions must be satisfied at Equipment, Sub-system and System levels, before the Safety-related System can be accepted as adequately safe. The Documentary Evidence that these Conditions have been satisfied shall be included in a Structured Safety Justification Document called Safety Case. This document must be submitted to the relevant Safety Authority to obtain the Safety Approval for a Product, or Application.

The Safety Case shall be structured in six parts :

- Definition of System / Sub-system / Equipment.
- Quality Management Report
- Safety Management Report
- Technical Safety Report
- Related Safety Cases
- Conclusion

Evidence of Quality Management :

The first condition of the Safety Assurance shall fulfill that the Quality of the System / Sub-system / Equipment Has been and shall continue to be controlled by an effective Quality Management System throughout the Life-cycle. The purpose of the Quality Management System is to minimise the incidence of Human Errors at each stage of the Life-cycle. Compliance with the requirements for Quality Management is mandatory for Safety Integrity Levels 1 to 4.

The aspects to be covered by the Quality Management system and included in the Quality Management Report are organizational structure quality planning and procedures specification Requirements, Design Control, Design Verification and Reviews, Application Engineering, Procurement and Manufacture, Product, Identification and Traceability, Handling and Storage, Inspection and Testing, Non-conformance and Corrective Action, Packaging and delivery Installation and Commissioning, Operation and Maintenance, Quality Monitoring and Feedback, Documentation and Records, Configuration Management / change control personnel competency and training, quality audits and follow-up decommissioning and disposal.

Evidence of Safety Management :

The safety of the System / Sub-system / Equipment has been, and shall continue to be, managed by an effective Safety Management process, which should be consistent with the Management process for Dependability (RAMS), described in EN 50126. Documentary evidence of compliance with all elements of the Safety Management process throughout the Life-cycle shall be provided in the Safety Management report. The use of this Safety Management process mandatory for Safety Integrity Levels 1 to 4. Safety Management process shall consist of a number of phases and activities, which are linked to form the safety life-cycle.

Safety Management process shall be implemented under the control of an appropriate safety organisation using competent personnel assigned to specific roles. Assessment and documentation of personnel competence, including technical knowledge, qualifications, relevant experience and appropriate training, shall be carried out in accordance with recognised standards. A Safety Plan shall be drawn up at the start of the Life-cycle. This Plan shall identify the Safety Management Structure, Safety-related activities and Approval milestones throughout the Life-cycle and shall include requirements for review of the Safety Plan at appropriate intervals. The Safety Plan shall deal with all aspects of the System / Sub-system / Equipment, including both Hardware and Software.

A Hazard Log shall be created and maintained throughout the Safety Life-cycle and include a List of Identified Hazards together with associated Risk Classification and Risk Control information for each Hazard. The specific safety requirements for each System / Sub-system / Equipment, including safety functions and safety integrity, shall be certified and documented. This shall be done by Hazard identification and analysis risk assessment and classification and allocation of safety integrity levels as explained in EN 50126.

System / Sub-system / Equipment Design phase create a Design, which satisfies the specified Operational and Safety requirements. A Top-down structured design approach shall be used with rigorous controlled and reviewed Documentation. Safety Reviews shall be carried out at appropriate stages of the Life-cycle. The Safety Plan shall include plans for Verifying that each Phase of the Life-cycle satisfies the specific Safety Requirements, identified in the previous Phase and for Validating the complete System / Sub-system / Equipment against its original Safety Requirements Specification. The degree of independence necessary for the Verifier and the Validator shall be in

- Results of Single Faults
- Independence of Items
- Detection of Single Faults
- Action following Detection of Faults
- Effects of Multiple Faults
- Defence against Systematic Faults

The Chapter Operation and External Influences shall demonstrate that when subjected to the external influences defined in the System Specification the System / Sub-system / Equipment continues to fulfill the specified Operational and Safety Requirements. The Safety Case is valid only when the specified range of external Influences as defined in the System Requirement Specifications. The methods used to withstand specified external Influences shall be fully explained and justified.

Safety-related Application Conditions shall specify the rules, Conditions and Constraints which shall be observed in the application of the System / Sub-system / Equipment. The final Chapter Safety Qualification Tests shall contain evidence to demonstrate successful completion of the Safety Qualification Tests, under operational conditions.

#### Action Following Detection of a Fault :

The First Fault (Single), which could be hazardous, either alone or if combined with a second Fault, shall be detected and a Safe-state shall be enforced in a sufficiently short time to fulfill the Specified Quantified Safety Target. This shall be demonstrated by a combination of Failure Modes and Effects Analysis (FMEA) and Quantified Assessment of Random Failure Integrity.

In the case of a Composite Fail-safety, this means that a First Fault shall be detected and a Safe-state shall be enforced in a sufficiently short time, to ensure that the Risk of a Second Fault occurring during the Detection and Negation period for the First Fault, is smaller than the specified Probabilistic Target. In the case of Reactive Fail-safety, this means that the maximum Total Time taken for Detection and Negation shall not exceed the specified time for the duration of a Transient potentially Hazardous condition.

After detection of the First Fault, the System / Sub-system / Equipment shall enter or continue in a Safe-state, which is generally more restrictive, in a sufficiently short time. Once the System / Sub-system / Equipment enters in to the Safe-state, any further Fault shall not cancel the Safe-state.

A Multiple Fault (e.g. a Double or even Triple Fault), which could be Hazardous, either directly or in combination with a further Fault, shall be detected and a Safe-state shall be enforced, in a sufficiently short time, to fulfill the specified Safety Target. A Common-Mode Failure Analysis (CMFA) shall be done to assure that a Multiple Fault could occur only by means of a combination of Random Single Faults, and not as the result of a Common-Mode Fault.

Technical precautions shall be taken so that if a Hazardous Systematic Fault exists, it would as far as reasonably practicable, be prevented from creating an unacceptable Risk. The following Table shows some Risk Reduction Techniques to be used for different Safety Integrity Levels :

Techniques	SIL 1	SIL 2	SIL 3	SIL 4
Preliminary Hazard Analysis	HR	HR	HR	HR
Fault Tree Analysis	R	R	HR	HR
Failure Modes & Effects Analysis	R	R	HR	HR
HAZOP	R	R	HR	HR
Cause & Consequence Diagrams	R	R	HR	HR
Markov & Chain Diagrams	R	R	R	R
Event Tree Diagrams	R	R	R	R
Reliability Block Diagrams	R	R	R	R
Zonal Analysis	R	R	R	R
Common Cause Failure Analysis	R	R	R	R
Historical Event Analysis	R	R	R	R

Table 5.2 Risk Reduction Techniques to be used for different Safety Integrity Levels

The following Table shows various Architectures for System /Sub-system/equipment :

Techniques	SIL 1	SIL 2	SIL 3	SIL 4
Separation of Safety-related and Non-Safety-related Systems	R	R	HR	HR
Single Electronic Structure with Self-test & Supervision	R	R	—	—
Dual Electronic Structure	R	R	—	—
Dual Electronic Structure based on Composite Fail- Safe comparison.	R	R	HR	HR
Single Electronic Structure based on Inherent fail safety	R	R	HR	HR
Single Electronic Structure based on Reactive fail-safety	R	R	HR	HR
Diverse Electronic Structure with Fail-safe comparison	R	R	HR	HR
Justification of the Architecture by a quantitative Reliability Analysis of the Hardware	HR	HR	HR	HR

Table 5.3 Architectures for System /Sub-system/equipment

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## **CHAPTER 6**

### **MAINTENANCE OF ELECTRONIC INTERLOCKING SYSTEM**

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#### **6.1 MAINTENANCE OF ELECTRONIC INTERLOCKING SYSTEM**

Unlike Mechanical Interlocking systems, the Electronic Interlocking systems do not need extensive maintenance .However some periodical and preventive maintenance is necessary to ensure safe and efficient functioning of the systems.

The maintenance of Electronic Interlocking System involves the following activities :

- (a) Checking of System Power supply.
- (b) Visual inspection of the EI system.
- (c) Checking of interface relays and cable terminations.
- (d) Verification of System change over from active to standby and vice versa.
- (e) Downloading and analysis of user log, event log and error log from Maintenance Terminal.
- (f) Verification of system clock.
- (g) Maintenance of earthing and surge protection arrangement.
- (h) Checking of communication links between system and peripherals.
- (i) Checking the function of peripherals like Operator VDU, Panel Processor etc.
- (j) Checking the function of cooling fans in the system racks.
- (k) Verification of the Checksum /CRC and version numbers of current software of the system.
- (l) Verification of correct logging of data in external data logger.
- (m) Testing the integrity of application program with the help of TOC.

#### **DETAILS**

- (a) Checking of System Power supply :
  - (i) Ensure that the DC –DC converters are in working order.
  - (ii) Check the fuses for proper housing and tightness.
  - (iii) Measure the output voltages at DC-DC Converters, fuses and at system terminals and ensure that they are within the specified limits.
  - (iv) Ensure that AC ripples of power supply modules are within the specified limits.
  - (v) Ensure that standby power supply modules are available and are in working order.
- (b) Visual inspection of the EI system :
  - (i) Ensure all the PCBs are properly housed and plugged in the system card file/housing/OC.
  - (ii) Ensure all the normal indications are available in all PCBs of the system.

- (iii) See that no abnormal indications are appearing in the system card file/housing/OC.
- (iv) Ensure that the EI equipment and its surroundings are dust free.
- (v) Ensure that there is no entry for rodents into the system.
- (vi) Ensure that all terminals and fuses inside the system racks are in proper tightness.
- (c) Checking of inter face relays and cable terminations :
  - (i) Ensure proper housing and fixing of Relays and connectors.
  - (ii) Measure the input and output interface voltages and ensure that they are within the specified limits.
  - (iii) Check that diodes across the vital output relays are in order.
  - (iv) Ensure particulars of relays and terminals are available &visible.
- (d) Verification of System change over from active to standby and vice versa : Where warm standby is available, reset the On line system and see that change over takes place properly and the stand by system is also working properly
- (e) Downloading and analysis of user log, event log and error log from Maintenance Terminal :
  - (i) Down load user data log, event log and error log from the EI system to the maintenance terminal at regular intervals.
  - (ii) Analyze the event and error log to identify system faults if any and take necessary corrective action.
- (f) Verification of system clock :
  - (i) Verify the current time of the system and see that it is correct or not.
  - (ii) If it is not matching then set the time of the system using maintenance Terminal.
  - (iii) If the system time is repeatedly lagging then check the 5V DC supply meant for internal memory backup.
- (g) Maintenance of Earthing and Surge protection arrangement:
  - (i) Measure the resistance of the ring/perimeter earth provided for the EI system and ensure that it is  $< 1 \Omega$ .
  - (ii) Check that all the earth electrode connections are properly welded and no rust formation is there at the terminals and joints.
  - (iii) Inside the EI equipment room check that all terminations and connections at the MEEB, SEEB and at the equipment racks are properly fixed and tightened.
  - (iv) See that cable armory /shield are connected to earth terminals properly.
  - (v) Check that all Surge protection devices are connected properly and are in working order.
- (h) Checking of communication links between system and peripherals :
  - (i) Check that all the communication links between system and peripherals are in working order.

- (i) Ensure that the equipment like converters, isolators, modems and hubs etc are all connected properly and are in working order.
- (ii) Ensure that the power supply and ground connections to the communication equipment are provided properly.
- (i) Checking the function of peripherals like Operator VDU ,Panel Processor etc :
  - (i) Verify that all field gears can be controlled and operated with the Operator VDU /CCIP.
  - (ii) Check that the changeover between Panel & VDU /VDU & standby VDU is taking place in proper sequence.
  - (iii) Verify that sufficient backup supply through UPS is available for VDU.
- (j) Checking the function of cooling fans in the system racks :
  - (i) See that the cooling fans provided inside the system rack are in working order.
- (k) Verification of the Checksum /CRC and version numbers of current software of the system :
  - (i) Run the maintenance tool and verify the Checksum, CRC and version of the current application logic and executive logic.
  - (ii) See that they are tallying with the past record.
- (l) Verification of correct logging of data in external data logger :
  - (i) Check the serial com connections between EI System & Protocol converter and between Protocol converter & Data logger.
  - (ii) See that normal indications are available in protocol converter.
  - (iii) Ensure that the user data log is logging properly in the external data logger.
- (m) Testing the integrity of application program with the help of TOC :
  - (i) This test has to be conducted when ever any modification has been done in the existing application logic.
  - (ii) It has to be conducted periodically also to ensure proper functioning of the existing logic as per the TOC.

Besides these general maintenance activities, some specific tasks prescribed in the maintenance manuals of different makes of EI are also to be carried out .

## 6.2 MAINTENANCE TOOL

Every EI system is provided with a Maintenance Terminal, connected through a diagnostic port. It is an aid to maintenance staff and service engineers. Diagnostic software named as Maintenance tool is uploaded into the Maintenance Terminal. Using this software, field personnel can download or upgrade software, and perform extensive system diagnostics using the logged data.

Using the tools provided in this program, maintenance personnel and application engineers can perform a wide variety of EI system maintenance, configuration, and diagnostic functions. These include :

- (a) Viewing the user log ,event log and error log in on line and offline modes

- (b) Downloading and storing of past user log ,event log and error log'
- (c) Viewing the data related to the system hardware and software.
- (d) Reconfiguring some settings of the system
- (e) Failure diagnosis

Each Manufacturer issues a manual in which the features and usage of maintenance terminal is described.

### 6.3 PERIODICITY OF MAINTENANCE

As per the letter No.2010/SIT/SEM/WG dt 11/10/2013 issued by Railway Board the periodicity of different maintenance tasks for EI are as mentioned below :

Sn.	Maintenance work to be done	Paragraph Reference (SEM)	Periodicity		
			Technician (signal)	JE/SE-Signal (Incharge of section)	SE/SSE (Overall Incharge)
01	Voltages shall be checked at check points	21.31.1	M	M	Q
02	Cooling arrangements like Fans, dust, Filters etc.	—	M	M	Q
03	Check sum to be verified.	21.31.4	—	—	Q
04	Visual checks of indications on EI and subsystems.	—	M	M	Q
05	System change over.	21.31.3	—	M	Q
06	Tightness of all terminals and cables , Earth wires etc.	—	—	—	Q
07	Panel to VDU, VDU to VDU Changeovers etc.		—	M	Q
08	Surge protection devices including A,B,C,D class		—	M	Q
09	Redundancy in communication , DC-DC Converters etc.	21.31.3	—	M	Q
10	Cleanliness of Room and Equipment etc.		M	M	Q
11	Emergency crank handle etc.				Q
12	Checking of error log etc.			M	Q

Table 6.1 Periodicity of different maintenance tasks for EI

### 6.4 ALARMS AND WARNINGS

Electronic Interlocking systems have self diagnosis feature. The CPU continuously monitors the input and output interface, serial communication links with peripherals, functioning of system software and application software. In the event of failure of any diagnostic test the CPU will generate error report which will be displayed in the Maintenance Terminal and in the system display units in the form of Alarms and Warnings.

For example in the Microlok II EI system, the errors are generated with error code in the following manner :

Error code	Description	Action to be taken up.
1E06	NV.IN32.OUT32 Driver Internal Error	Replace CPU card. Report this problem to US & S
103	System Watchdog Timeout	Check CPU board
107	RAM error	Check CPU board
10A	Internal Error	Check CPU board
201	Data Bus Error	Check CPU board
207	CPU Error	Check CPU board
208	CPU Watchdog failure	Check CPU board
601	Application Startup Error	Check CPU board
604	Application Execution Error	Check CPU board
607	Application CRC error	Reload application then check CPU board.
701	Application Logic Queue Overflow	Check application program.
702	Application error	Check application
705	Application killed system	—
706	Application caused quick-reset	—
707	Application logic took too long to initialize	Check application
901	IN16 Echo Error	Check IN16 board
902	IN16 Type Error	Check IN16 board
A01	OUT16 Echo Error	Check OUT16 board
A02	OUT16 Type Error	Check OUT16 board
A04	OUT16 Hardware Failure	Check OUT16 board

Table 6.2 Error code list

## 6.5 TROUBLE SHOOTING

For the sake of trouble shooting the EI Installation can be divided into the following sections :

- (a) EI System Card file
- (b) Peripherals
- (c) Interface circuits
- (d) Power supply system
- (e) Communication cables and equipment
- (f) Outdoor gears
- (g) Software

For the easy rectification of a failure it is essential to localise the fault basing on the above classification.

The following things will give clues to identify and localise the fault:

- (a) Indications on System Card file
- (b) Indications on the CCIP/VDU
- (c) User log and Event & Error log in Maintenance Terminal

Flow charts are provided by each OEM for trouble shooting the failures in the respective EI systems. A general flow chart for trouble shooting the failures in EI system is as listed below :

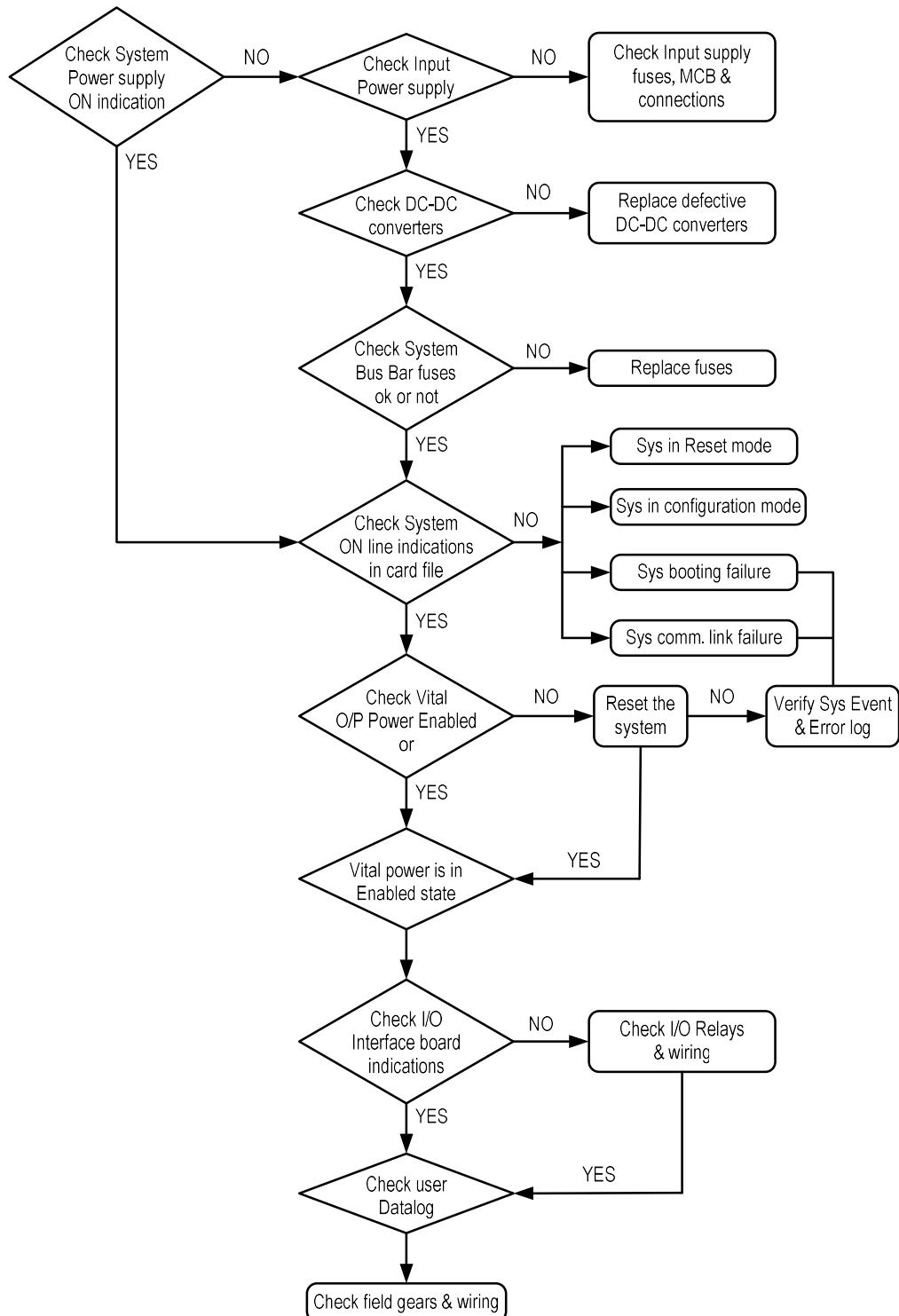


Fig 6.1 A general flow chart for trouble shooting the failures in EI system

## 6.6 IDENTIFYING FAULTS

The failures occurring in EI systems are broadly divided into two categories. They are System level faults and Card level faults.

### 6.6.1 System level faults:

All the faults other than the hard ware failures of system cards can be treated as system level faults. The system level faults may occur due to problem in any one of the following sections of the EI system.

- (a) System Power supply
- (b) Interface wiring
- (c) Interface Relays and Relay contacts
- (d) System changeover circuit
- (e) Panel/VDU
- (f) Application logic
- (g) Communication equipment

Most of system level faults as mentioned above can be identified either by physical inspection of the system or with the help of error log. These faults can be rectified at site either by repair or replacement of the defective component. If it is an error of application logic it can be rectified by uploading the correct software.

### 6.6.2 Card level faults

Most of the cards in the EI system are provided with some indications on the front panel. These indications reflect the normal or abnormal functioning of the respective cards.

Sometimes a card may fail to function due to a fuse failure. If the PCB has failed due to reasons other than fuse then it has to be replaced with a spare card and the defective card needs to be sent for repair. However as far as possible the reasons for the card failure are to be investigated and necessary preventive measures are to be taken to prevent further damage to the system.

A Log of the defective and repaired cards has to be maintained with appropriate remarks

Precautions:

DO:

1. Tighten the boards after insertion.
2. Ensure all terminations are fully tightened.
3. Place the removed boards with a tag into a conductive shielding bag.
4. Download user data log / Event log / Error log data periodically.
5. Maintain minimum 12V/24V DC at the card file back plane.
6. In case of Warm Standby System Ensure diagnostic switch in "NORMAL" position before starting the system.
8. Keep the EI room free from dust.

Don't:

1. Reset the system when working.
2. Remove or insert boards, VCOR relays, Fuses / Links and pin connectors when the system is on.
3. Forceable insertion of the boards in to the slots.
4. Change jumper settings in PCBs.
5. Touch the board components.
6. Repair boards on your own.
7. Alter EI system, Maintenance Terminal and Operator VDU setting without authorization.
8. Delete / Modify application program Logics without authorization.
9. Use blower for cleaning dust

Comment: Every EI manufacturer shall provide maintenance and diagnostic tool with above all feature for maintenance and troubleshooting process.

Refer IRISSET notes S18-A, S18-B, S18-C etc., to study concerned maintenance and diagnostic tool features.

\* \* \*

**Annexure 1**  
**TECHNICAL ADVISORY NOTE**

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TECHNICAL ADVISORY NOTE			
Subject	Use of embedded PC for Electronic Interlocking (F1)		
Document No	STS/E/TAN/3007	Version	1.0
Date	02.11.2012	Pages	01

Table A1.1 Technical advisory note

From the visits of RDSO to various EI installations and on receipt of feedback specially during failures it has been noted by RDSO that in most of the cases the VDU for train operation and maintenance Diagnostic Terminals have been found to be defective and non functional.

Sr.DSTE/Co-ord./BSP/SECR vide its letter no.ES/SSI/12/01 dated 25.01.2012 & CSE/SECR vide its letter no SECR/S&T/EI/2953 dated 19.03.2012 have also requested to provide the details of industrial grade fan less PCs to be used with EI.

The major cause of these systems getting defective is their continuous use in service, 24 hours a day without any break and these computers are put up in non-AC environment. Further it has been that these terminals are utilized for purposes other than their nominated use. The pen drives and CD drivers are used on these terminals making them vulnerable and faulty very easily.

It is noted that these terminals are required to be in operation round the clock to provide continuous service to the railways.

In order to provide expected level of reliability for these vital equipments, it is advised that only industrial grade embedded fan less PCs shall be used for EI installation for VDU and maintenance /diagnostic terminals. It is suggested that industrial grade fan less PCs rugged and reliable type like MOXA series V 2406, Kontron MPCX28R , MEN BC50M or similar ( General requirement is attached ), with compact of flash drives in non-AC and normal environment may be used. These models are certified to EN 50155 and are operable in very harsh conditions.

The railways may also plan to replace the existing VDU and maintenance terminals on expiring of their codal life by above mentioned industrial grade fan less PCs.

Sd/-

Minimum requirement of Embedded PC For Electronic Interlocking (EI) :

CPU	AMD T52R 1.5GHz or Intel Atom N270 1.6 GHz processor or Intel (R) Atom Z530 1.6 GHz or above or better
OS (Pre installed)	Linux or Windows Embedded standard 2009 or above / better version Os
System memory	1 x 200-pin DDR2 SODIMM socket support DDR2 533 up to 1GB , built-in 1GB Minimum
<b>Storage</b>	
Built-in	40 GB Onboard Industrial DOM to store OS minimum
<b>Other Peripherals</b>	
KB/MS	1 PS/2 interface supporting standard PS/2 keyboard and mouse through Y-type cable or USB Mouse
Audio	Line –in , Line-out interface
<b>Display</b>	
<b>Ethernet Interface</b>	
LAN	2 auto-sensing 10/100 Mbps ports(M12)
<b>Serial Interface</b>	
Serial standards	4 RS-232/422/485 ports*, software selectable (DB9 male)
<b>Environmental limits</b>	
Operating Temperature	Wide temp. models :- 10 to 70c (-40 to158F)
Ambient Relative Humidity	5 to 95% (Non condensing)
Anti-vibration	EN 50155 standard ,(Railway Applications-Electronic Equipment on rolling stock)
Anti-Shock	En 50155 standard ,(Railway Applications-Electronic Equipment on rolling stock)
<b>Power Requirements</b>	
Input Voltage	9-36 or 12-48 VDC Note: complaint with EN 50155 on 24 VDC
<b>Standards And Certifications</b>	
Rail Traffic	EN 50155 (Railway Applications-Electronic Equipment on rolling stock)
<b>Warranty</b>	
Warranty Period	2 years and supplier to give additional 3 years
Fan less	Yes

Table A1.2 Minimum requirement of Embedded PC For Electronic Interlocking (EI)

Specifications for RS232, RS423, RS422, and RS485:

Specifications	RS232	RS423	RS422	RS485
Mode of Operation	Single-Ended	Single-Ended	Differential	Differential
Allowed no. of Tx and Rx	1 Tx, 1 Rx	1 Tx, 10 Rx	1 Tx, 10 Rx	32 Tx, 32 Rx
Maximum cable length	50 Feet	4000 Feet	4000 Feet	4000 Feet
Maximum data rate	20 kbps	100 kbps /10 mbps	100 kbps/10 mbps	100kbpsi/10 mbps
Minimum driver output range	$\pm 5V$ to $\pm 15V$	$\pm 3.6V$	$\pm 2V$	$\pm 1.5V$
Maximum driver output range	$\pm 25V$	$\pm 6V$	$\pm 6V$	$\pm 6V$
Tx load impedance ( $\Omega$ )	3k to 7k	$>= 450$	100	54
Rx input sensitivity	$\pm 3V$	$\pm 200mV$	$\pm 200mV$	$\pm 200mV$
Rx input voltage range	+15V	+12V	+7V	-7V to +12V
Maximum Rx input resistance ( $\Omega$ )	3k to 7k	4k min	4k min	$>= 12k$

Table A1.4 Specifications for RS232, RS423, RS422, and RS4S5

#### SERIAL DATA TRANSMISSION :

Due to its relative simplicity and low hardware overhead (as compared to parallel interfacing), serial communications is used extensively within the electronics industry. Today, the most popular serial communications standard in use is certainly the EIA / TIA-232-E specification. This standard, which has been developed by the Electronic Industry Association and the Telecommunications Industry Association (EIA / TIA), is more popularly referred to simply as "RS-232" where "RS" stands for "recommended standard". In recent years, this suffix has been replaced with EIA /A" to help identify the source of the standard. This paper will use the common notation of "RS-232" in its discussion of the topic. The official name of the EIA / TIA-232-E standard is "Interface between Data Terminal Equipment and Data Circuit Termination Equipment Employing Serial Binary Data Interchange". Although the name may sound intimidating, the standard is simply concerned with serial data communication between a host system (Data Terminal Equipment, or "DTE") and a peripheral system (Data Circuit-Terminating Equipment, or "DCE"). The EIA / TIA-232-E standard which was introduced in 1962 has been updated four times since its introduction in order to better meet the needs of serial communication applications. The letter E" in the standard's name indicates that this is the fifth revision of the standard.

#### RS-232 specifications :

RS-232 is a 'complete' standard. This means that the standard sets out to ensure compatibility between the host and peripheral systems by specifying

1) Common voltage and signal levels 2) Common pin wiring configurations, and 3) a minimal amount of control information between the host and peripheral systems. Unlike many standards, which simply specify the electrical characteristics of a given interface, RS-232 specifies electrical, functional, and mechanical characteristics in order to meet the above three criteria. Each of these aspects of the RS-232 standard is discussed below.

#### Electrical characteristics :

The electrical characteristics section of the RS-232 standard includes specifications on voltage levels, rate of change of signal levels, and line impedance. The original RS-232 standard was defined in 1962. As this was before the days of TL logic, it should not be surprising that the standard does not use 5 volt and ground logic levels. Instead, a high level for the driver output is defined as being +5 to +15 volts and a low level for the driver output is defined as being between -5 and -15 volts. The receiver logic levels were defined to provide a 2 volt noise margin. As such, a high level for the receiver is defined as +3 to +15 volts and a low level is -3 to -15 volts. Figure 1 illustrates the logic levels defined by the RS-232 standard. It is necessary to note that, for RS-232 communication, a low level (-3 to -15volts) is defined as logic 1 and is historically referred to as "marking". Likewise a high level (+3 to +15volts) is defined as logic 0 and is referred to as "spacing".

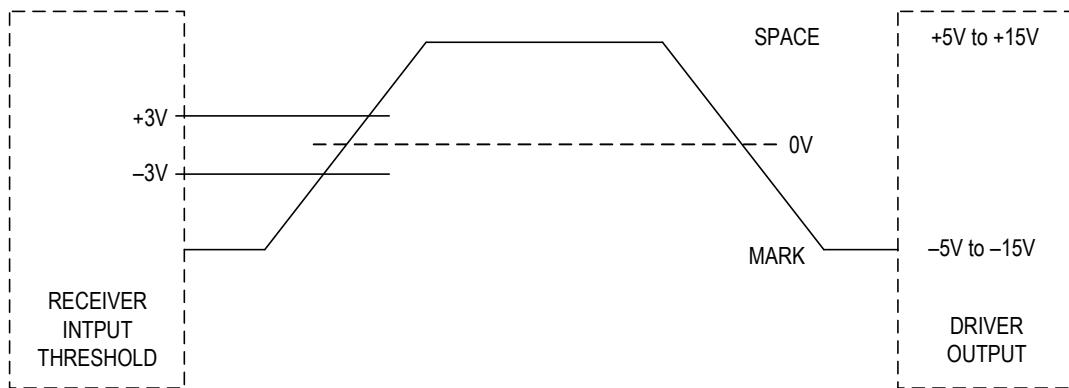


Fig A1-1 RS – 232 Logic level specifications

The RS-232 standard also limits the maximum slew rate at the driver output. This limitation was included to help reduce the likelihood of cross talk between adjacent signals. The slower the rise and fall times, the smaller the chance of cross talk. With this in mind, the maximum slew rate allowed is 30 V/ms. Additionally, a maximum data rate of 20k bits / second has been defined by the standard. The impedance of the interface between the driver and receiver has also been defined. The load seen by the driver is specified to be 3KW to 7KW. For the original RS-232 standard, the cable between the driver and the receiver was also specified to be a maximum of 15 meters in length. This part of the standard was changed in revision "D" (EIA/TIA-232-D). Instead of specifying the maximum length of cable, a maximum capacitive load of 2500 pf was specified which is clearly a more adequate specification. The maximum cable length is determined by the capacitance per unit length of the cable, which is provided in the cable specifications.

#### Functional characteristics :

Since RS-232 is a “complete” standard, it includes more than just specifications on electrical characteristics. The second aspect of operation that is covered by the standard concerns the functional characteristics of the interface. This essentially means that RS-232 has defined the function of the different signals that are used in the interface. These signals are divided into four different categories common, data, control, and timing. The Table below, illustrates the signals that are defined by the RS-232 standard. As can be seen from the table there is an overwhelming number of signals defined by the standard. The standard provides an abundance of control signals and supports a primary and secondary communications channel. Fortunately few applications, if any, require all of these defined signals. For example, only eight signals are used for a typical modem. Some simple applications may require only four signals (two for data and two for handshaking) while others may require only data signals with no handshaking. Examples of how the RS-232 standard is used in some “real world” applications are discussed later in this paper. The complete list of defined signals is included here as a reference.

CIRCUIT MNEMONIC	CIRCUIT NAME*	CIRCUIT DIRECTION	CIRCUIT TYPE
AB	Signal Common		Common
BA	Transmitted Data (DT)	To DCE	
BB	Received Data (RD)	From DCE	Data
CA	Request to send (RTS)	To DCE	
CB	Clear to send (CTS)	From DCE	
CC	DCE Ready (DSR)	From DCE	
CD	DTE Ready (DTR)	To DCE	
CE	Ring Indicator (RI)	From DCE	Common
CF	Received Line Signal Detector ** ( DCD )	From DCE	
CG	Signal Quality Detector	From DCE	
CH	Data Signal Rate Detector from DTE	To DCE	
CI	Data Signal Rate Detector from DCE	From DCE	

CIRCUIT MNEMONIC	CIRCUIT NAME*	CIRCUIT DIRECTION	CIRCUIT TYPE
CJ	Ready for Receiving	To DCE	
RL	Remote Loopback	To DCE	
LL	Local Loopback	To DCE	
TM	Test Mode	From DCE	
DA	Transmitter Signal Element Timing from DTE	To DCE	
DB	Transmitter Signal Element Timing from DCE	From DCE	
DD	Receiver Signal Element Timing from DCE	From DCE	Timing
SBA	Secondary Transmitted Data	To DCE	
SBB	Secondary Received data	From DCE	Data
SCA	Secondary Request to Send	To DCE	
SCB	Secondary Clear to Send	From DCE	
SCF	Secondary Received Line Signal Detector	From DCE	Control

\* Signals with abbreviations in parentheses are the eight most commonly used signals.

\*\* This Signal is more commonly referred to as carrier Detect (DCD)

Table A1.5 RS – 232 Defined Signals

#### MECHANICAL INTERFACE CHARACTERISTICS :

The third area covered by RS-232 concerns the Mechanical Interface. In particular, RS-232 specifies a 25-pin connector. This is the minimum connector size that can accommodate all of the signals defined in the functional portion of this standard. The pin assignment for this connector is shown in Figure 2. The connector for DCE equipment is male for the connector housing and female for the connection pins. Likewise, the DTE connector is a female housing with male connection pins. Although RS-232 specifies a 25-position connector, it should be noted that often this connector is not used. This is due to the fact that most applications do not require all of the defined signals and therefore a 25-pin connector is larger than necessary. This being the case, it is very common for other connector types to be used. Perhaps the most popular is the 9-position DB9S connector which is also illustrated in Figure 2. This connector provides the means to transmit and receive the necessary signals for modem applications, for example. This will be discussed in more detail later.

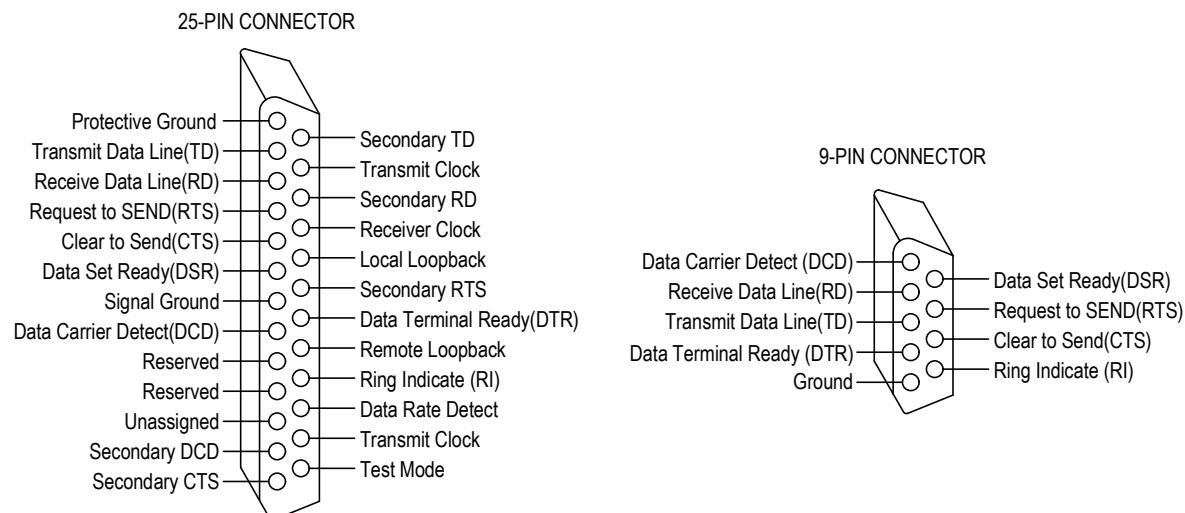


Fig A2-2 RS – 232 Connector Pin Assignments

### Practical RS-232 implementation :

Most systems designed today do not operate using RS-232 voltage levels. Since this is the case, level conversion is necessary to implement RS-232 communication. Level conversion is performed by special RS-232 IC's. These IC's typically have line drivers that generate the voltage levels required by RS-232 and line receivers that can receive RS-232 voltage levels without being damaged. These line drivers and receivers typically invert the signal as well since a logic 1 is represented by a low voltage level for RS-232 communication and likewise a logic 0 is represented by a high logic level. Figure 3 illustrates the function of an RS-232 line driver / receiver in a typical modem application. In this particular example, the signals necessary for serial communication are generated and received by the Universal Asynchronous Receiver/Transmitter (UART). The RS-232 line driver / receiver IC performs the level translation necessary between the CMOS / TTL and RS-232 interface.

The UART just mentioned performs the "overhead tasks necessary for asynchronous serial communication. For example, the asynchronous nature of this type of communication usually requires that start and stop bits be initiated by the host system to indicate to the peripheral system when communication will start and stop. Parity bits are also often employed to ensure that the data sent has not been corrupted. The UART usually generates the start, stop, and parity bits when transmitting data and can detect communication errors upon receiving data. The UART also functions as the intermediary between byte-wide (parallel) and bit-wide (serial) communication: it converts a byte of data into a serial bit stream for transmitting and converts a serial bit stream into a byte of data when receiving.

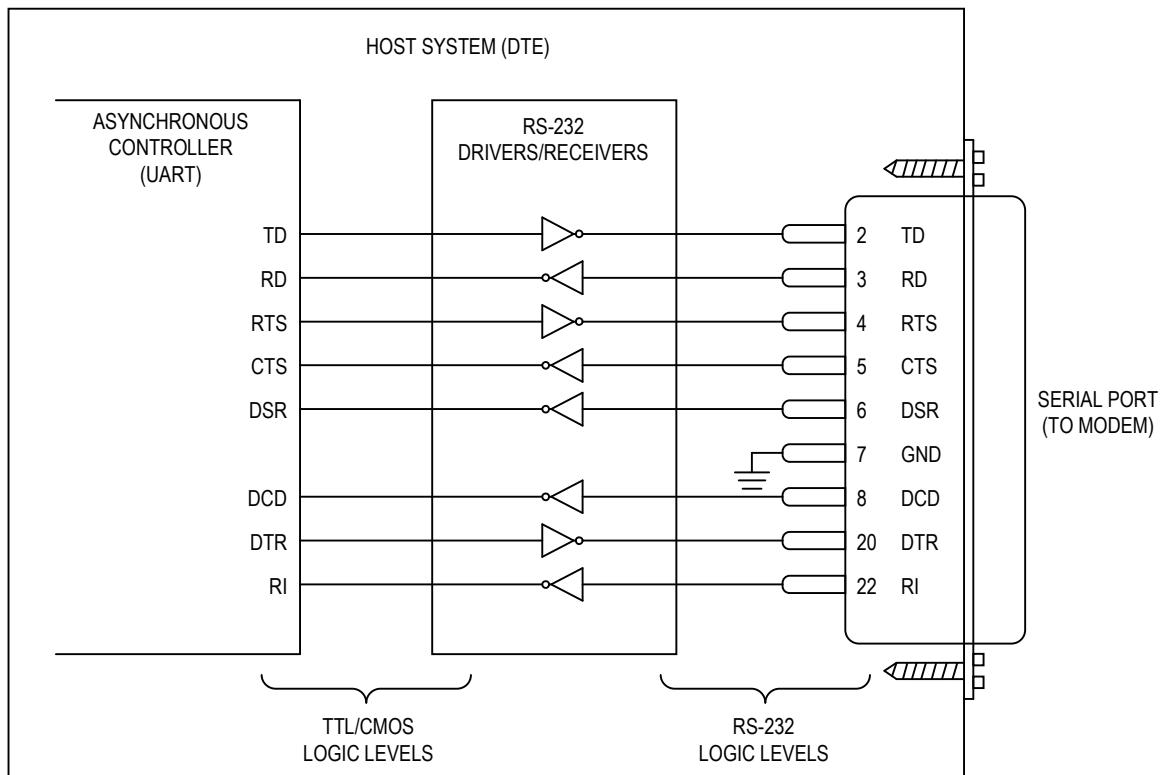


Fig A1-3 Typical RS – 232 Modem Application

Now that an elementary explanation of the TTL/CMOS to RS-232 interface has been provided we can consider some real world" RS-232 applications. It has already been noted that RS-232 applications rarely follow the RS-232 standard precisely. Perhaps the most significant reason this is true is due to the fact that many of the defined signals are not necessary for most applications. As such, the unnecessary signals are omitted. Many applications, such as a modem, require only nine signals (two data signals, six control signals, and ground). Other applications may require only five signals (two for data, two for handshaking, and ground), while others may require only data signals with no handshake control. We will begin our investigation of "real world" implementations by first considering the typical modem application.

\* \* \*

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