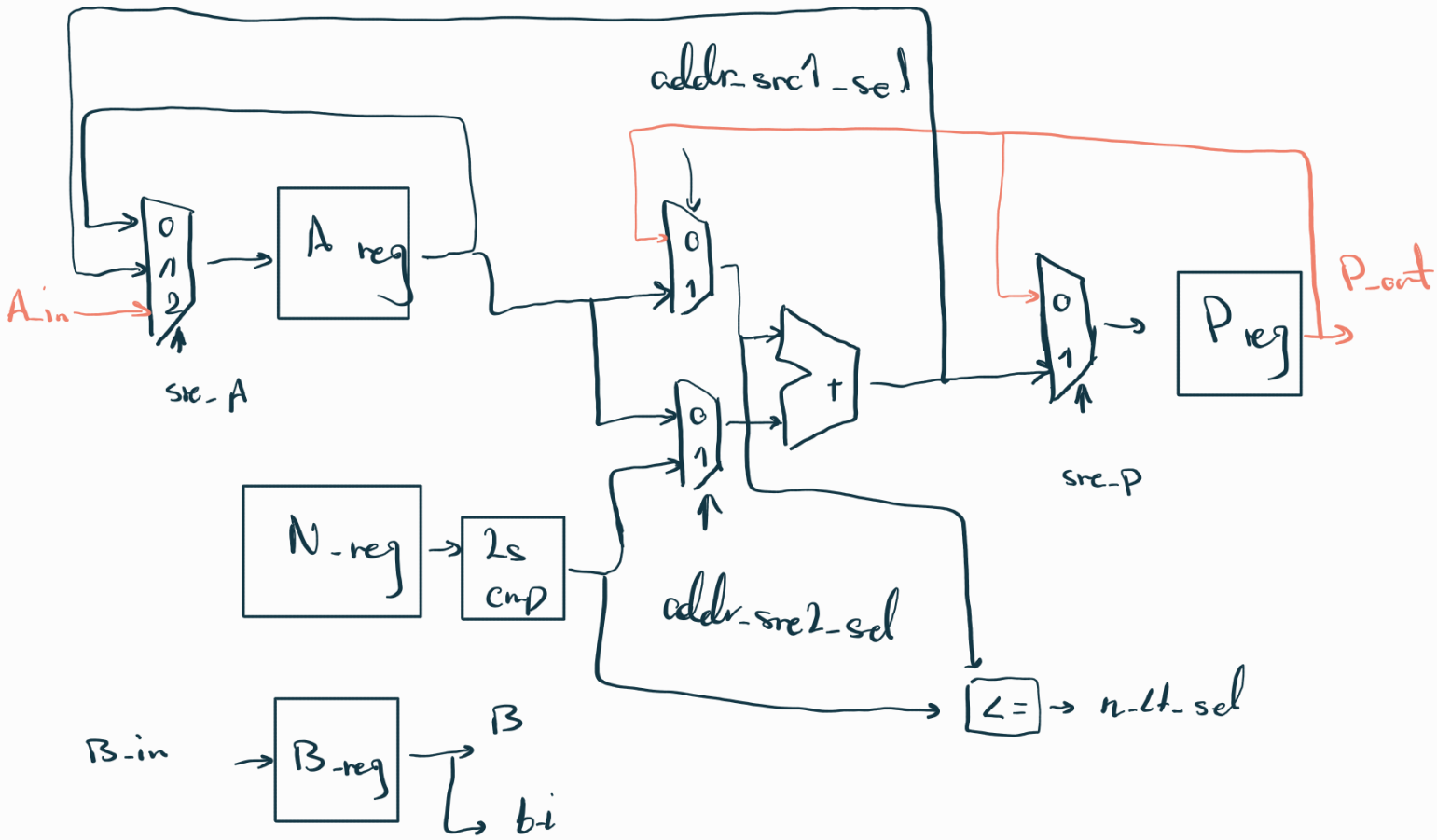
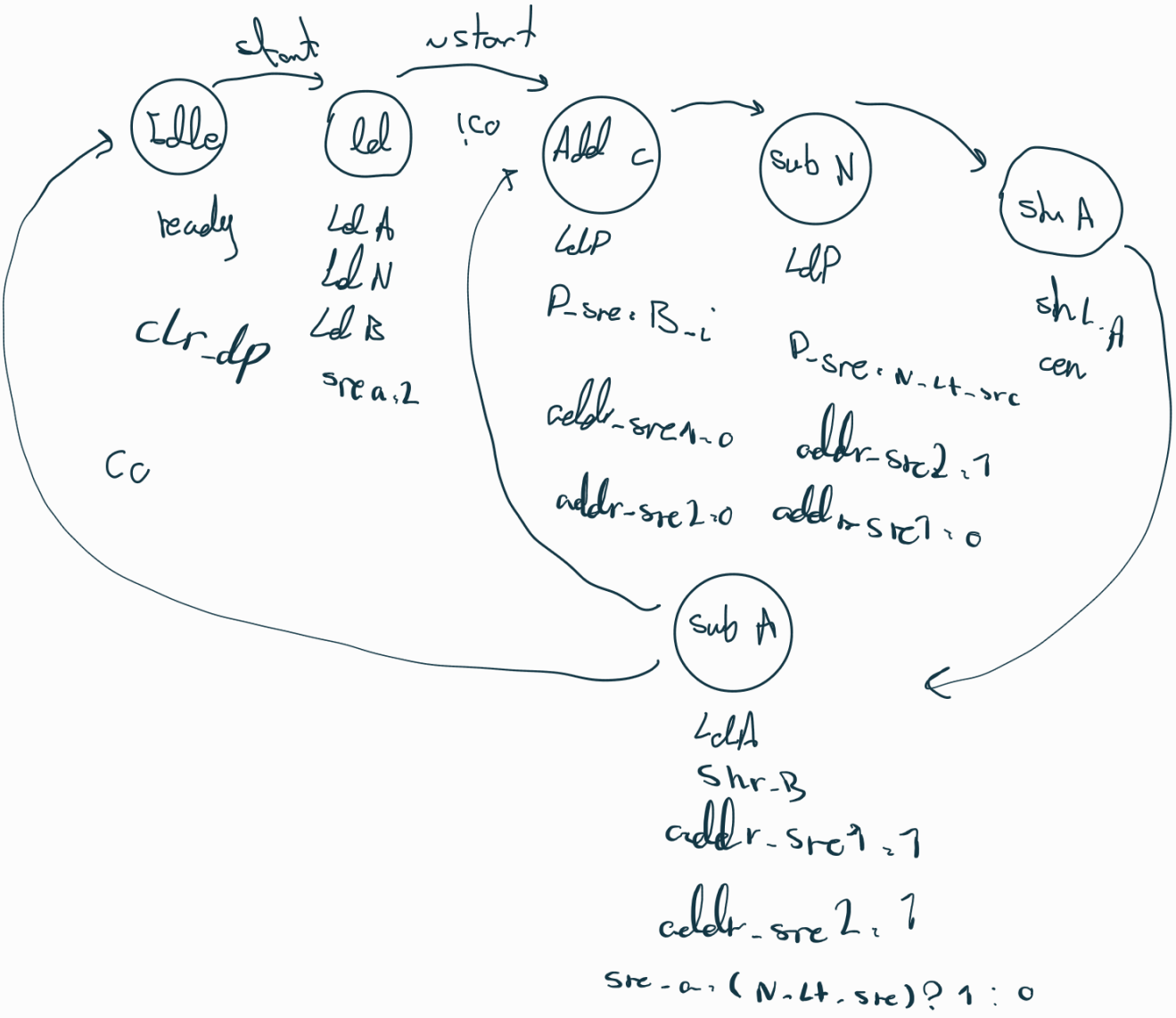

addr_src1_sel
A_in
0
1
2
A reg
src_A
0
1
0
1
+
0
1
P reg
P_out
src_P
N_reg
2s cmp
addr_src2_sel
<=
n_lt_sel
B_in
B_reg
B
b_i


start
!start
Idle
ready
clr_dp
Co
ld
Ld A
Ld N
Ld B
sre a,2
!Co
Add c
LdP
P_sre: B_i
addr_sre1,0
addr_sre2,0
Sub N
LdP
P_sre: N_lt_sre
addr_sre2,1
addr_sre1,0
Shr A
shL_A
cen
Sub A
LdA
Shr_B
addr_sre1,1
addr_sre2,1
sre_a,(N_lt_sre)?1:0