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Assignment 2

Subject: Computer System Architecture

Subject Code: CSEG 2004

Total marks: 50

Each Question carries different marks…

Ques 1:

i) A microprogrammed control unit uses a control memory of 1024 words of 2 bits each. The microinstruction has three fields. The microperation field has 16 bits. **(3 marks)**

a. How many bits are there in the branch address field and the select field?

b. If there are 16 status bits in the system. How many of the branch logic are used to select a status bit?

c. How many bits are left to select an input for the multiplexer

ii) Explain the steps that are performed during address sequencing in detail. **(7 marks)**

Ques 2: A computer uses RAM chips of 1024 X 1 capacity**.** **(1+1+2= 4marks)**

a. How many chips are needed, and how should their address lines be connected to provide a memory capacity of 1024 bytes?

b. How many chips are needed to provide a memory capacity of 16K bytes?

c. Explain in words how the chips are to be connected to the address bus?

Ques 3.

A digital computer has a memory unit 64K X 16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of four words. **(2+2+1=5 marks)**

a. How many bits are there in the tag, index, block and word fields of the address format?

b. How many bits are there in each word of cache and how are they divided into functions? Include a valid data.

c. How many blocks can the cache accommodate?

Ques 5:

The access time of a cache memory is 100ns and that of main memory 1000ns. It is estimated that 80% of the memory requests are for read and the remaining 20 % are for write. The hit ratio for read access only is 0.9. A write through procedure is used. **(2+2+1=5 marks)**

a. What is the average access time of the system for considering only memory read cycles?

b. What is the average access time of the system for both read and write requests?

c. What is the hit ratio taking into consideration the write cycle?

Ques 6:

i) How many characters per second can be transmitted over a 1200 baud line in each of the following modes? (Assume the character code of 8 bits) **(1+1+1 = 3 marks)**

a. Synchronous serial transmission

b. Asynchronous serial transmission with two stop bits

c. Asynchronous serial transmission with one stop bit.

ii) What are the different modes of Data Transfer? Explain in detail **(7 marks)**

Ques 7:

i) A DMA controller transfers 16 bits words to memory using CYCLE STEALING. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU slowed down because of the DMA transfer? **(5 marks)**

ii) Explain how DMA works with the help of suitable diagram? **(5 marks)**

Ques 8:

i) It is necessary to transfer 256 words from a magnetic disk to a memory section starting from 1230. The transfer is by means of DMA. **(1+1=2 marks)**

a. Give the initial values that the CPU must transfer to the DMA controller.

b. Give the step by step account of the actions taken during the input of the first two words.

ii) Differentiate between Strobe Control and Handshaking Mode of Asynchronous data transfer. **(4 marks)**