
PANIPAT INSTITUTE OF ENGINEERING & TECHNOLOGY

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# MPI

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# Minimum mode 8086 system

- In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its MN/MX pin to logic 1.
- In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum mode system.
- The remaining components in the system are latches, transceivers, clock generator, memory and I/O devices.
- The ***clock generator*** also synchronizes some external signal with the system clock.
- It has 20 address lines and 16 data lines, the 8086 CPU requires three octal address latches and two octal data buffers for the complete address and data separation.

# Minimum mode 8086 system continue…

*Latches : They* are generally buffered output D-type flip-flops like 74LS373 or 8282. They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086.

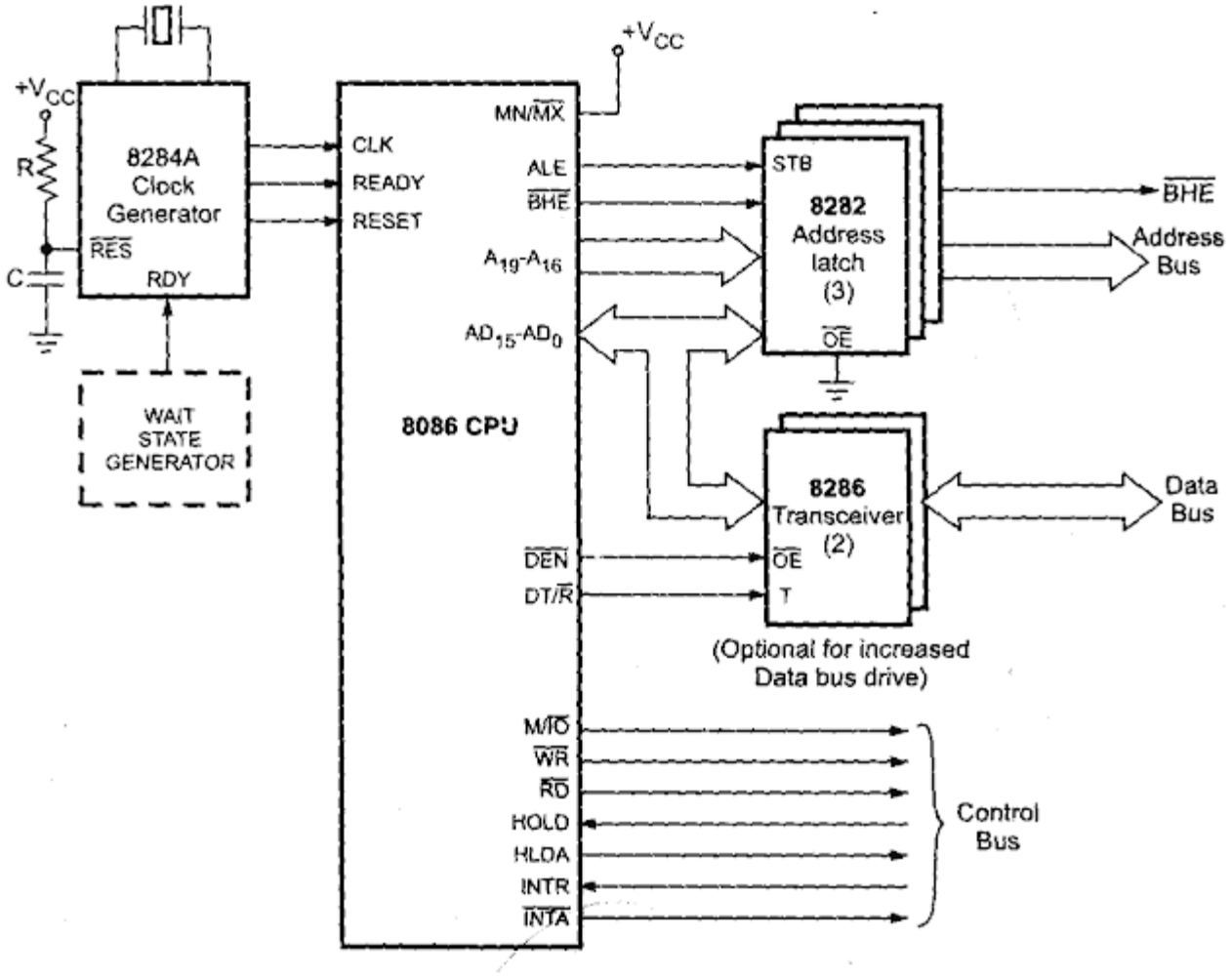
*Trans-receivers* are the bidirectional buffers and some times they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signals.

They are controlled by two signals namely, DEN and DT/R.

The DEN signal indicates the availability of valid data over the address/data lines. The DT/R signal indicates direction of data, i.e. from or to the processor.

Usually, EPROM are used for monitor storage, while RAM for users program storage. A system may contain *I/O devices*.

# 8086 in Minimum mode



# Time in µP

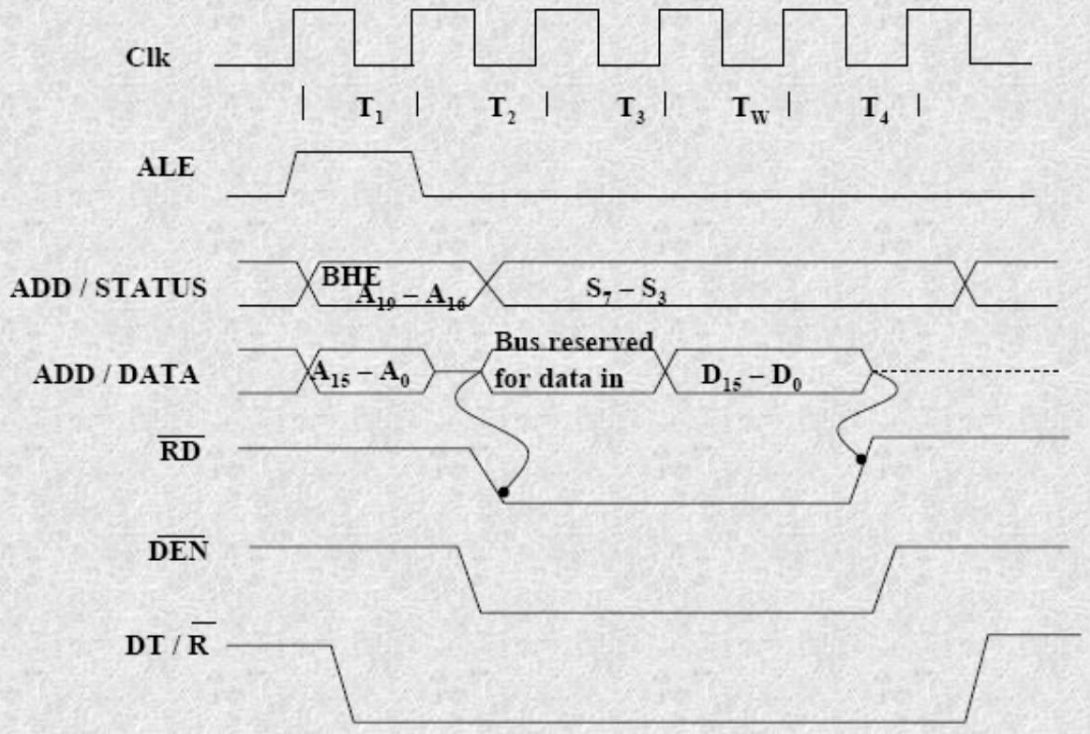
- T-state is the smallest unit of time in a µp
- 1 clock cycle = 1 T-state
- In 8086, 1 machine cycle = 4 T-states
- 1 machine cycle (or bus cycle) is the time required to
  - T1 – send out an address – on address bus
  - T2 – send out a signal (read/ write) – on control bus
  - T3 – read/ write data on that location – on data bus
  - T4 – release all buses
- 1 instruction cycle = *n* machine cycles

  (depends on the instruction)

# Memory Read Timing Diagram

- During **period T1**,
  - The 8086 outputs the **20-bit address** of the memory location to be accessed on its multiplexed **address/data bus**. **BHE** is also output along with the address during T1.
  - At the same time a pulse is also produced at **ALE**. The **trailing edge** or the **high level** of this pulse is used to **latch** the address in external circuitry.
  - Signal **M/IO** is set to **logic 1** and signal **DT/R** is set to the **0 logic level** and both are maintained throughout all four periods of the bus cycle.
- Beginning with **period T2**,
  - Status bits **S3** through **S6** are output on the upper four address bus lines. This status information is maintained through periods **T3** and **T4**.

# Minimum Mode 8086 System (cont..)




Read Cycle Timing Diagram for Minimum Mode

- On the other hand, address/data bus lines **AD0 through AD7** are put in the **high-Z state (means neither data nor address )** during **T2**.It
- Late in period **T2**, **RD** is switched to **logic 0**. This indicates to the memory subsystem that a read cycle is in progress. **DEN** is switched to **logic 0** to enable external circuitry to allow the data to move from memory onto the microprocessor's data bus.

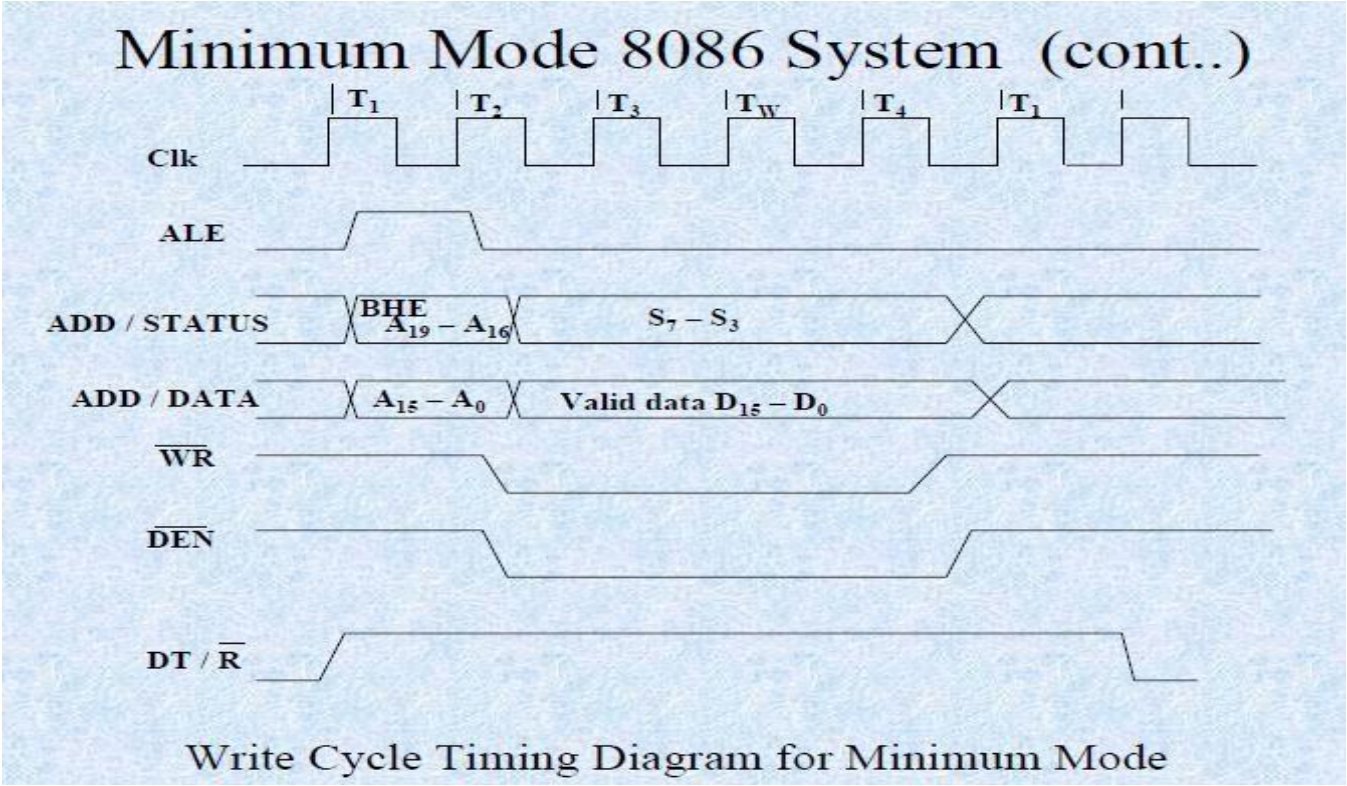
- During **period T3**,
  - The memory must provide **valid data** during **T3** and maintain it until after -the processor terminates the read operation. The data read by the 8086 microprocessor can be carried over all **16 data bus** lines
- During **T4**,
  - The 8086 switches **RD** to the inactive **1 logic level** to terminate the read operation. **DEN** returns to its inactive logic level late during **T4** to disable the external circuitry.

# Memory Write Timing Diagram

- During **period T1**,
  - The **address** along with **BHE** are output and latched with the **ALE** pulse.
  - **M/IO** is set to **logic 1** to indicate a memory cycle.
  - However, this time **DT/R** is switched to **logic 1**. This signals external circuits that the 8086 is going to **transmit data** over the bus.
- Beginning with **period T2**,
  - **WR** is switched to **logic 0** telling the memory subsystem that a write operation is to follow.
  - The 8086 puts the **data** on the bus late in **T2** and maintains the data valid through **T4**. Data will be carried over all **16 data bus lines**.
  - **DEN** enables the external circuitry to provide a path for data from the processor to the memory.

- During **period T3**,
  - The memory must receive **valid data** during **T3** and maintain it until after -the processor terminates the write operation. The data write by the 8086 microprocessor can be carried over all **16 data bus** lines

The 8086 switches **WR** to the inactive **1 logic level** to terminate the write operation. **DEN** returns to its inactive logic level late during **T4** to disable the external circuitry.



# 8086 in Maximum Mode

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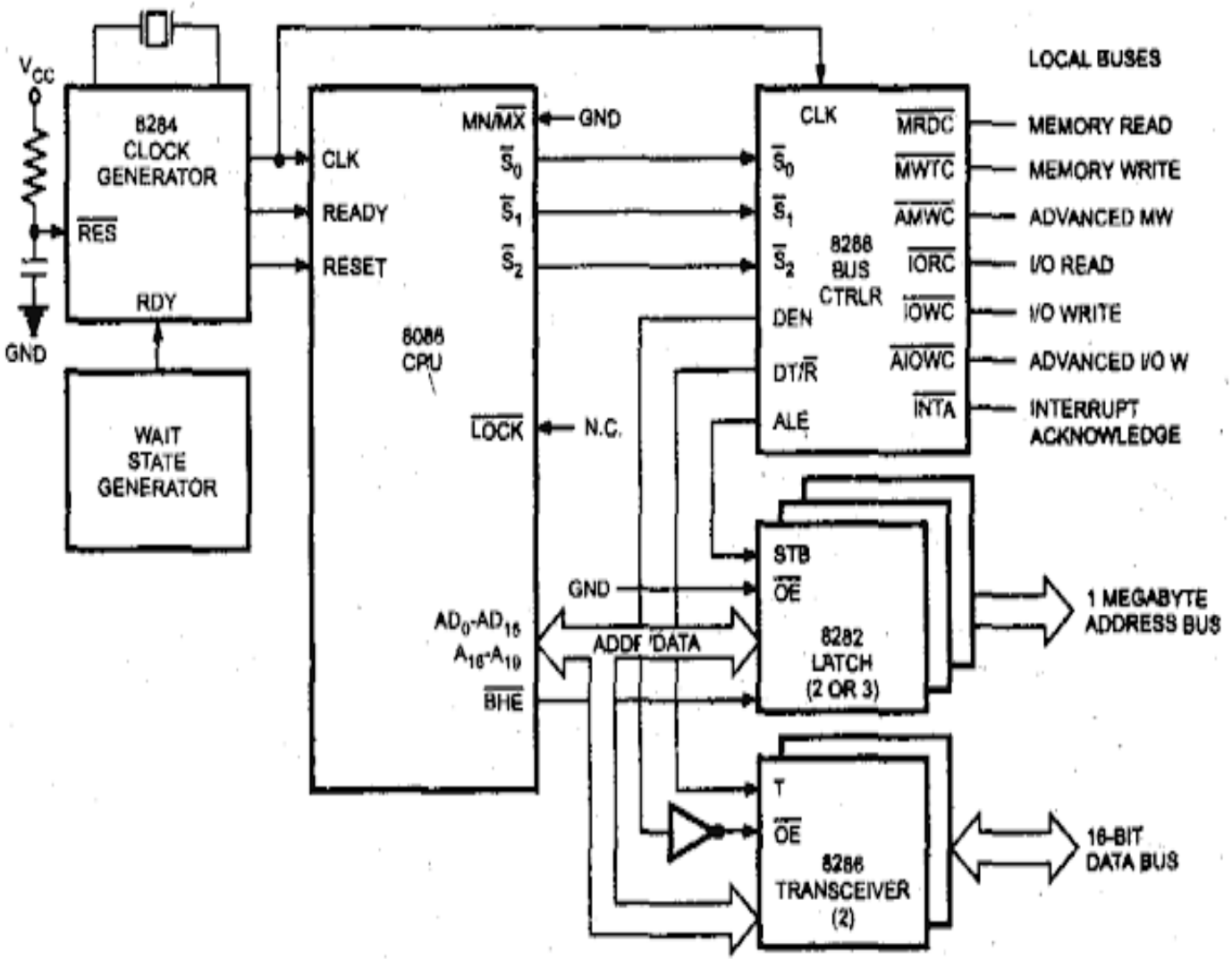
In the maximum mode, the 8086 is operated by strapping the MN/MX pin to ground. In this mode which shown in figure, the processor derives the status signal S2, S1, S0 and Another chip called bus controller derives the control signal using this status information . In the maximum mode, there may be more than one microprocessor in the system configuration.

The basic function of the bus controller chip IC8288, is to derive control signals like RD and WR ( for memory and I/O devices), DEN, DT/R, ALE etc. using the information by the processor on the status lines.

Bus controller chip has input lines S2, S1, S0 and CLK. These inputs to 8288 are driven by CPU. It derives the outputs ALE, DEN, DT/R, MRDC, MWTC, IORC, IOWC.

# 8086 in Maximum Mode



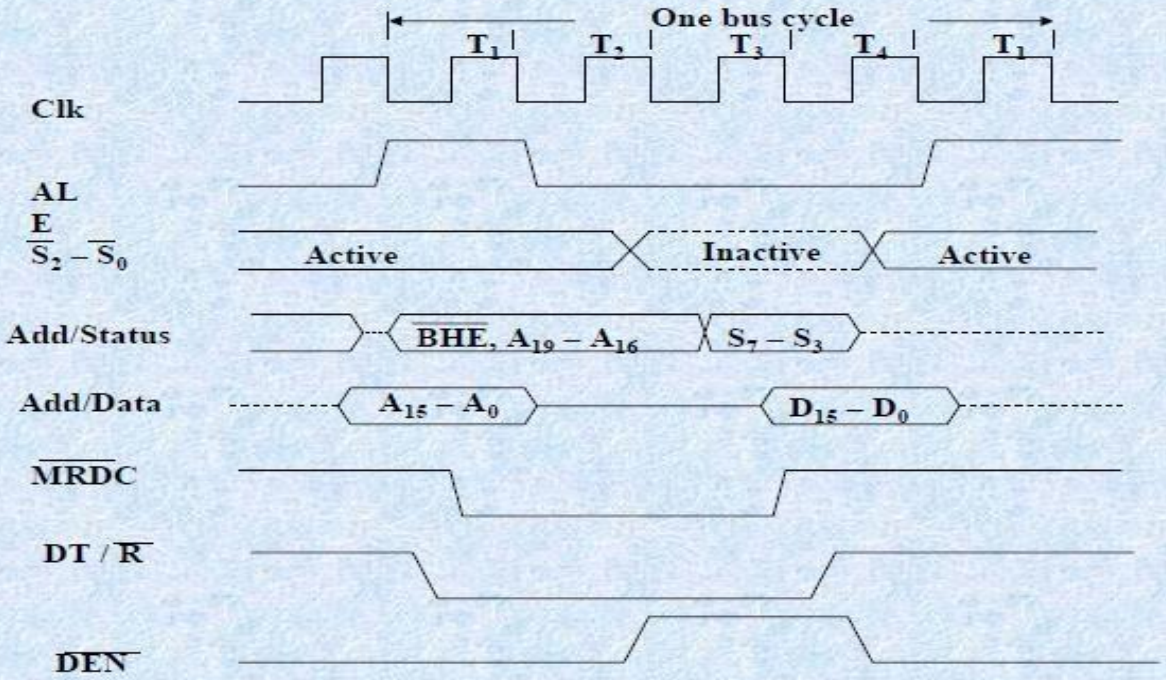
# Memory Read Timing Diagram in Maximum Mode

The difference between in timing diagram between minimum mode and maximum mode is the status signals used and the available control and advanced command signals. S0, S1, S2 are set at the beginning of bus cycle. The 8288 bus controller will output a pulse as on the ALE and apply a required signal to its DT / R pin during T1

In T2, 8288 will set DEN=1 thus enabling transceivers, and for an input it will activate MRDC or IORC. These signals are activated until T4.

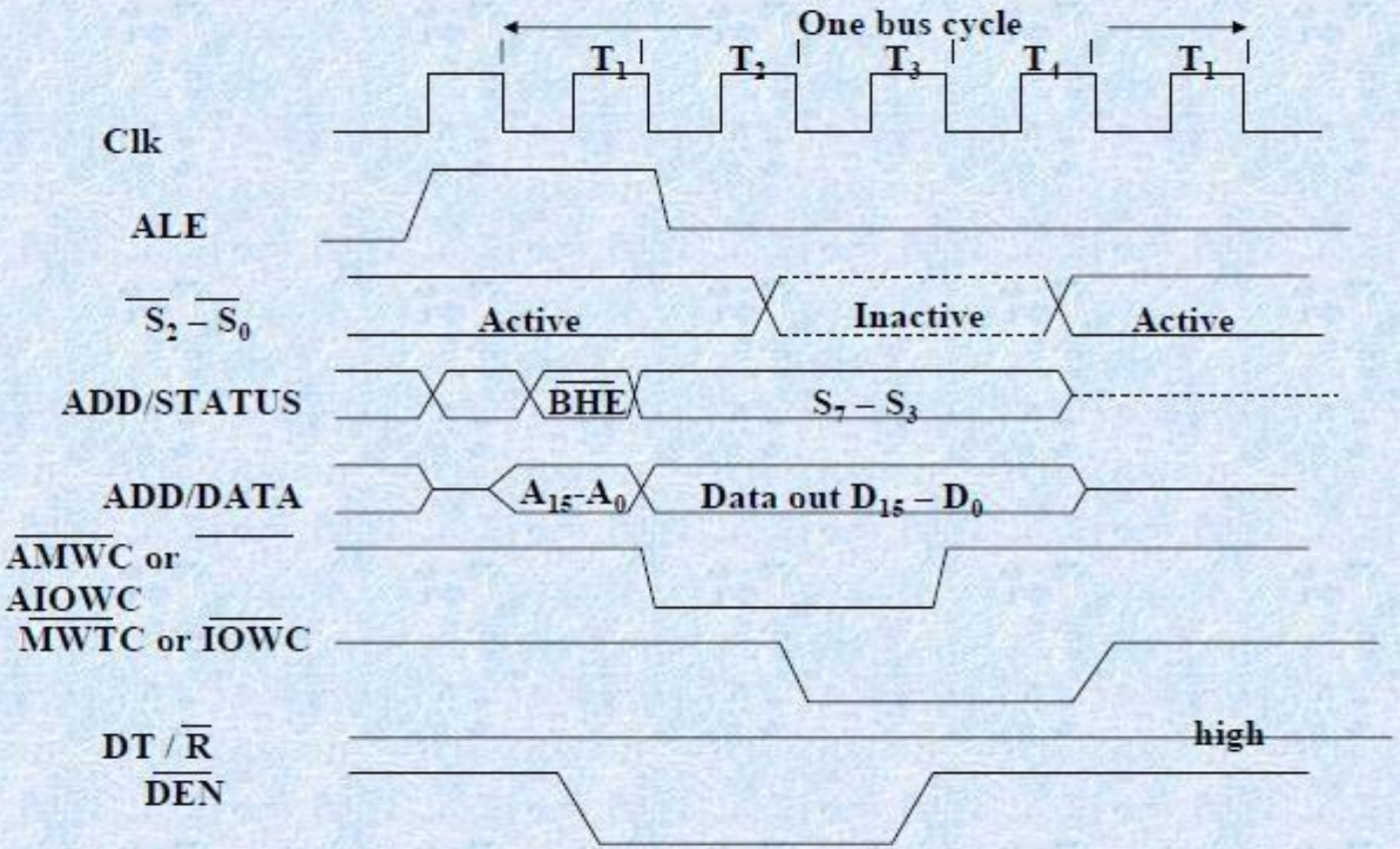
The status bit S0 to S2 remains active until T3 and become passive during T3 and T4 **and** If reader input is not activated before T3, wait state will be inserted between T3 and T4.

# Maximum Mode 8086 System ( cont..)




Memory Read Timing in Maximum Mode

# Maximum Mode 8086 System ( cont..)




Memory Write Timing in Maximum mode.