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Roll no. 2820208 Class CSE 3rd sem

Examination Center _____

Date of the Practical Examination _____

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S.no	Experiment Description	Page No.	Experiment Date	Submission Date	Remarks
1.	Familiarization with digital trainer kit and associated equipments.	3-4	25/10/21	8/11/21	X + P
2.	Study the TTL gates; AND ,OR, NOT, NOR ,NAND, EX-OR, EX-NOR .	5-7	8/11/21	29/11/21	X + P
3.	Study of universal gate and design of all gates using universal gate .	8-10	29/11/21	6/12/21	X + P
4.	To utilize and design a given function using k-map and verify its performance.	11-13	29/11/21	6/12/21	X + P
5.	To study the operation of a multiplexers & demultiplexers and verify the truth table.	14-16	6/12/21	13/12	X + P
6.	To design a full adder and half adder circuit.	17-18	6/12/21	13/12	X + P
7.	To design and verify 1-bit comparator using gates.	19-20	20/12/21	20/12	X + P

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8.	To verify the operation of seven segment display.	21-23	20/12/21	20/12/21	1st DD
9.	To verify truth table of T, K, T, D flip flop.	24-25	03/01/22		
10.	To design a 3-bit asynchronous & synchronous counters	26-28	10/01/22	-	
11.	4 bit ALU	29-31	10/01/22	-	

Experiment - 1

Aim :- Familiarization with digital kit and associative concepts.

Apparatus :- Digital trainer kit.

DC power supply	0 Max	DIGITAL LAB	Power
	0 min		0 0 0 0
			4 0 0 1
			5 0 1 0
			6 0 2 0
			7 0 3 0
Frequency	0		TTL
CMOS mode	0		CMOS mode selection
1.52	100K 1M		A 0
Pulse generator			B 0
			C 0
			D 0
			BCD2
			digital display
		D7 D6 D5 D4	
		8 bit data switches	
	0	GND	
Pulse switch	0	GND	
		GND	

Experiment - 1

Aim:- To study familiarization with digital
= trainers kit and associated equipment.

Apparatus:- Digital trainers kit,

Theory :-

DC power \Rightarrow This ~~block~~ provides fixed output
of +5V and -5V provided variable
DC output from +3 to +15V and -3V to -15V.

Pulse generation \Rightarrow This block generate stable
pulse of frequency range 10 Hz to 1 MHz
with TTL and CMOS mode. When TTL
mode is selected amplitude of pulse will
be compatible with TTL and when CMOS
mode is selected, it is compatible with CMOS

Pulse switches \Rightarrow Two pulse switches are
provided for triggering purpose.
Each has two output, normal and
complementary.

8-bits Data Switches \Rightarrow These switches
provides two state (i.e. High & Low)
TTL : High = +5V
Low = +0V

Logic Probe :-

- When input is high, the display will show 'H'.
- When it is low, it will show 'L'.
- When no input is given, it will show '0'
- 'F' in case of transition

Digital Display \Rightarrow Two digital displays are provided. These are BCD to 7-segment display, which converts BCD to equivalent decimal number.

Mode Selector Switch \Rightarrow When switch is put on 'TTL' or 'CMOS' position output of pulse generation, pulse switches, 8-bits data switches and inputs of digital probe 8-bits LED display will meet the high or low level of 'TTL' or 'CMOS'.

Mode Selector Switch to TTL positions \Rightarrow

~~Low level = 0 V~~
~~High level = +5 V~~

Transistor = HI $>$ LO or LO $>$ HI

Mode selector switch to CMOS positions \Rightarrow

~~Low level = 0 V~~, ~~High level = +3V to +15V~~

Transistor = HI $>$ LO or LO $>$ HI

8-Bits LED display \Rightarrow When input to this block

Size of Bread Board	172.5 mm x 128.5 mm
connections on bread board	1685
DC power supply on bread board	+5 V, 1A, -5V 500mA +3V, -15V 500mA -3V, +15V, 50 mA
Pulse generation on bread board	Frequency range: 1 Hz in steps variable in amplitude 3V-15V (CMOS)
Pusher switches	2NOS (Push to ON)
Data switches	8NOS (Toggle switches) TTL 2 (CMOS mode)
LED display	8NOS (TTL / CMOS mode)
BCD to 7 segment display	2NOS
Logic Probe	Logic level indicators for TTL (7 segment)
Weight	3 Kg Approx
Dimensions (mm)	W 490 x H 100 x D 25
Power requirement	230V +/- 10% 50Hz

is high, LED will glow red and when input is low, LED will glow green.

Operating Instruction and power control description

The trainer is equipped with built in DC power supply. When ON/OFF switch of the trainer kit is turned ON, the power LED indicator will be indicating that trainer is ON, the power LED when +V and -V potentiometer of DC power block one in their fully clockwise position, fully voltage +15V and -15V is obtained. +V and -V potentiometer can be varied to get variable positive and negative supply from +3V to +15V and -3V to -15V. When +V volt is varied CMOS voltage level will be varied proportionally CSO whenever CMOS mode is used carefully check the +V volt position. Frequency potentiometer of pulse generator is used for time setting of frequency of pulse range switch is used to vary frequency from 10 Hz to 1 MHz in steps frequency below 10 Hz can be obtained by freq, plot one moment only switches. As long as there are pressed indicated output are obtained and bits data switches when in position will give low output when ON/OFF switches of digital are turned ON, it will ON the display.

Result :

We have studied digital trainer kit and associated equipments.

When TTL / CMOS switch is put on TTL or CMOS position the output of pulse generator, pulse switches input of digital probes and bit, LED display will meet the high or low level of TTL or CMOS.

Result =

~~We have studied digital trainer kit and associated equipments.~~

~~10/11/21~~

Experiment - 2

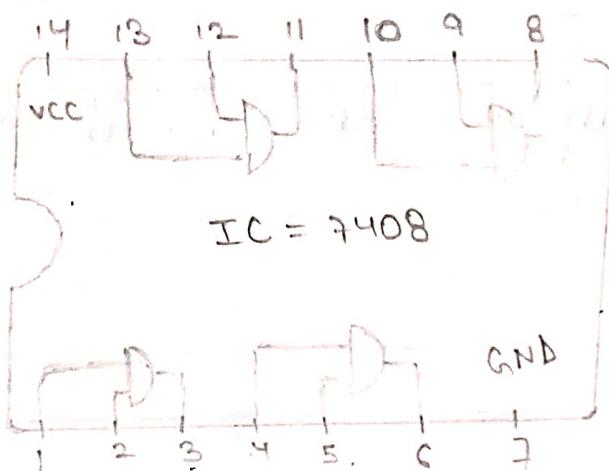
Aim :- Study of TTL gates - AND, OR, NOT, NOR, NAND, Ex-OR and Ex-NOR.

Apparatus :- Trainers kit, connecting wires.

AND Gate :-



$$Y = A \cdot B$$



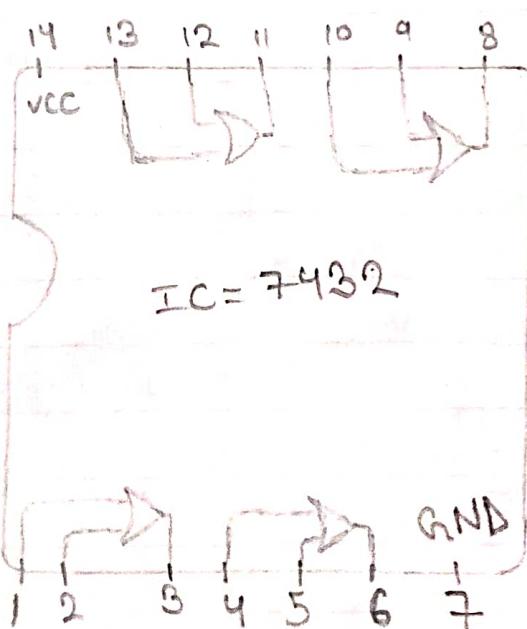
Truth Table

Input		Output
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate :-



$$Y = A + B$$



Truth Table

Input		Output
A	B	$Y = A + B$
0	1	1
0	0	0
1	0	1
1	1	1

Experiment -2

Aim :- Study of TTL gates: AND, OR, NOT, NOR
= NAND, EX-OR, EX-NOR.

Apparatus :- Trainers kit, connecting wires

Theory :-

AND gate \Rightarrow It is an electronic circuit that gives a true output only if all its input are true. Dot (.) is used to show AND operation.

$$Y = A \cdot B$$

OR gate \Rightarrow It is an electronic circuit that gives a true output if one or more of its input are true. Plus (+) is used to show OR operation. $Y = A + B$

NOT gate \Rightarrow It is an electronic circuit that produces an inverted version of input as its output. It is also known as inverted.

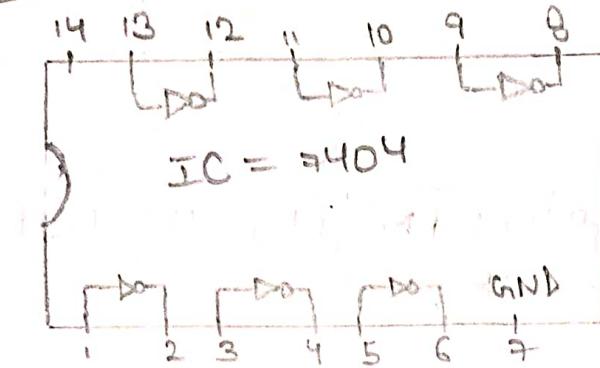
If the input variable is A, the inverted output is known as NOT A.

NOT A is represented by \bar{A}

$$Y = \bar{A}$$

NOR gate \Rightarrow It is a NOT-OR gate which is equal to an OR gate followed by a NOT gate.

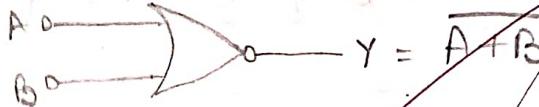
NOT Gate :- $A \rightarrow \neg A \rightarrow Y = \bar{A}$



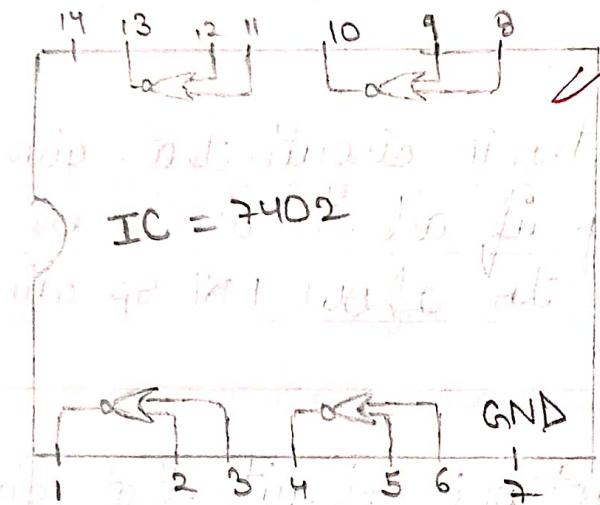
Truth Table

Input	Output
A	$Y = \bar{A}$
0	1
1	0

NOR Gate :-



Truth Table

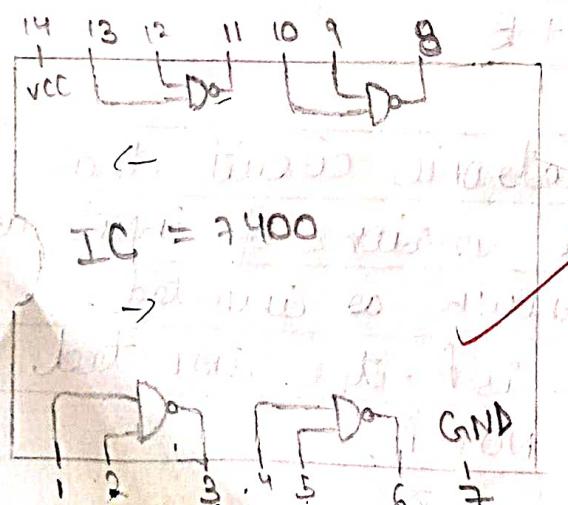


Input	Output
A	$Y = \bar{A} + B$
0	0
0	1
1	0
1	1

NAND gate :-



Truth Table



Input	Output
A	$Y = \bar{A} \cdot B$
0	1
0	0
1	0
1	1

Traps elimination of the NOT and NOR gate
Also call NOT gate to AND gate in other

The output of all NOR gate are false if any of the input are true. $y = \overline{A+B}$

NAND gate \Rightarrow It is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The output of all NAND gate is true if any of input are false. $y = \overline{A \cdot B}$

~~Ex-OR gate \Rightarrow The 'Exclusive-OR' gate is a circuit which will give a true output if either but not both of its two input are there.~~

An circled plus sign (\oplus) is used to show Ex-OR gate/operation

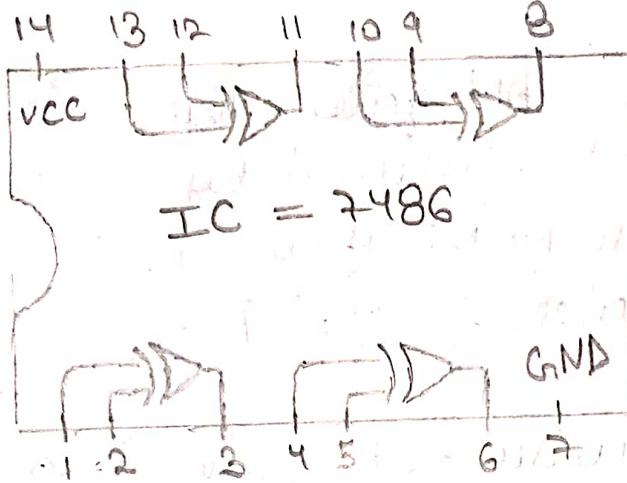
$$y = A \oplus B \Rightarrow \overline{A}B + A\overline{B}$$

~~Ex-NOR gate \Rightarrow The 'Exclusive-NOR' gate circuit does the opposite of Ex-OR gate. It will give a false output if either but not both of its input are true.~~

~~The symbol of Ex-OR is a small circle on output. $y = A \ominus B \Rightarrow \overline{A}\overline{B} + AB$~~

Result \Rightarrow We have studied TTL gates and verified them, and also studied their truth table.

Ex-OR Gate :- $A \oplus B = Y$

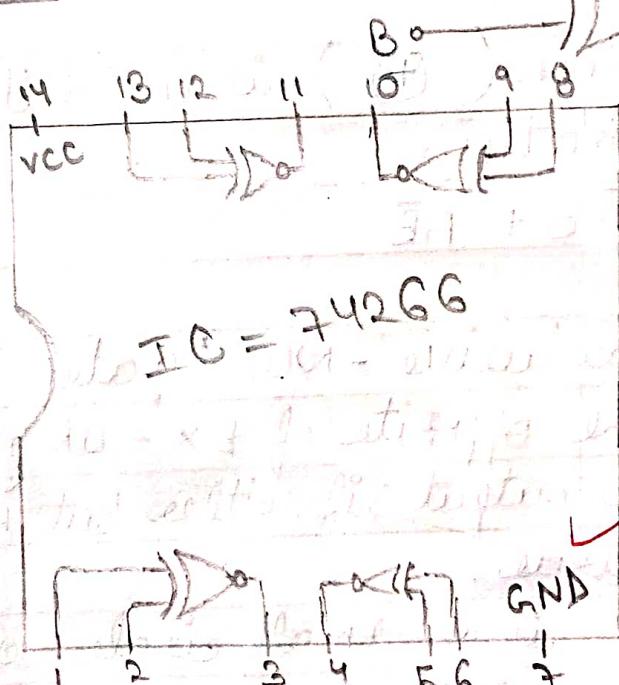


IC = 7486

Truth Table

Input		Output
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

Ex-NOR Gate :- $A \ominus B = Y$



IC = 74266

Truth Table

Input		Output
A	B	$Y = A \ominus B$
0	0	1
0	1	0
1	0	0
1	1	1

~~Result :- we have studied TTL gates and verified them, and also studied their truth table.~~

~~29/11/21~~

Experiment - 3

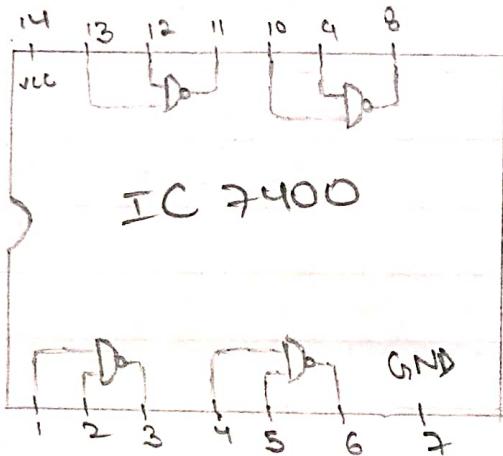
Aim :- design of all gates using universal gates.

Apparatus :- digital trainer kit , connecting wires, IC 7402 and IC 7400.

NAND gate \Rightarrow



Truth Table

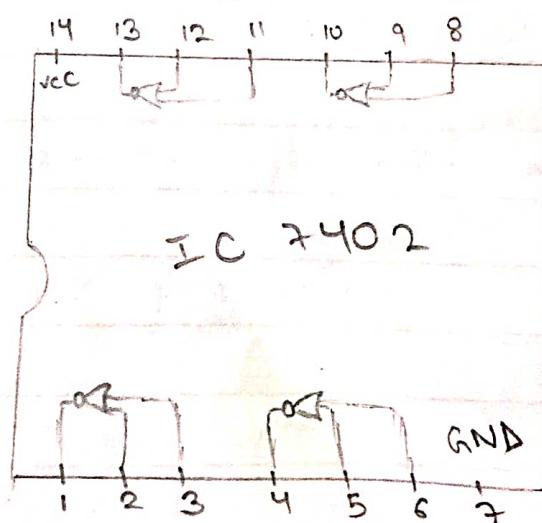


Input		Output
A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

NOR gate \Rightarrow



Truth Table



Input		Output
A	B	y
0	0	0
0	1	0
1	0	0
1	1	1

Experiment -3

Aim :- Study of universal gate and design of all gates using universal gate.

Apparatus :- Digital Trainer kit, connecting wires, IC 7402 (NOR) and IC 7400 (NAND).

Theory :-

Basic Gates \Rightarrow Among all the gates, AND, OR and NOT gate are called basic gates because these gates have basic operations.

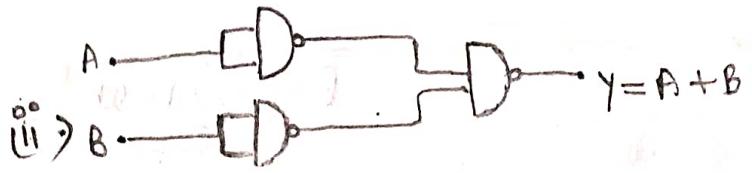
Universal Gates \Rightarrow NOR and NAND gates are known as universal gates because all the rest of six gates can be made by only NAND or only NOR gate.

- NOR gate \Rightarrow
- It is a NOT-OR gate which is equal to an OR gate followed by a NOT gate.
- The output of all NOR gates are false if any of the i/p are true.

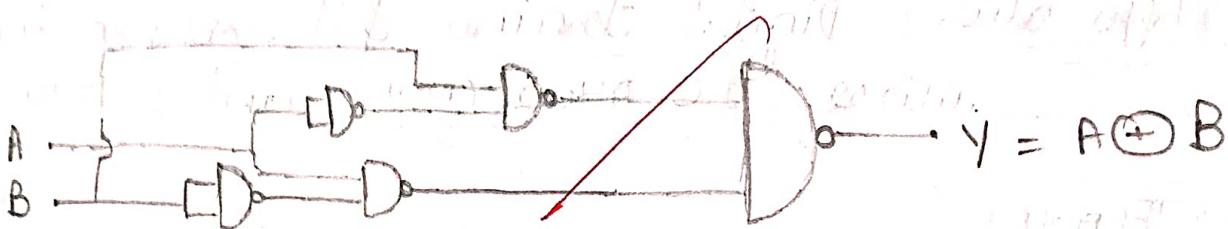
$$Y = \overline{A+B}$$

- Integrated chip '7402' represents NOR gate.

Using NAND gate

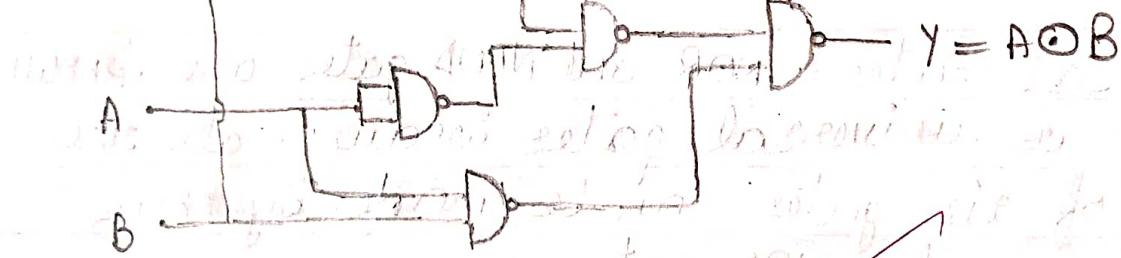


(iii) Using (OR) gate, we can make EX-OR gate:



(iv) EX-NOR gate: At the junction of two signals, one signal is in stop state and other signal is in start state.

Ex-NOR gate circuit diagram:

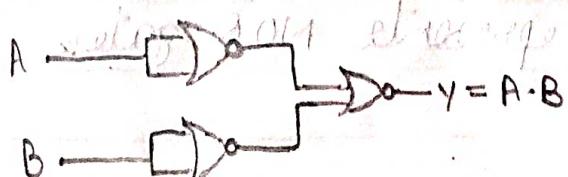


(v) NOT gate:

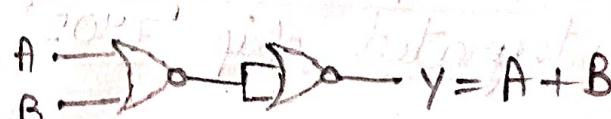


Using NOR gate

ii) (AND)

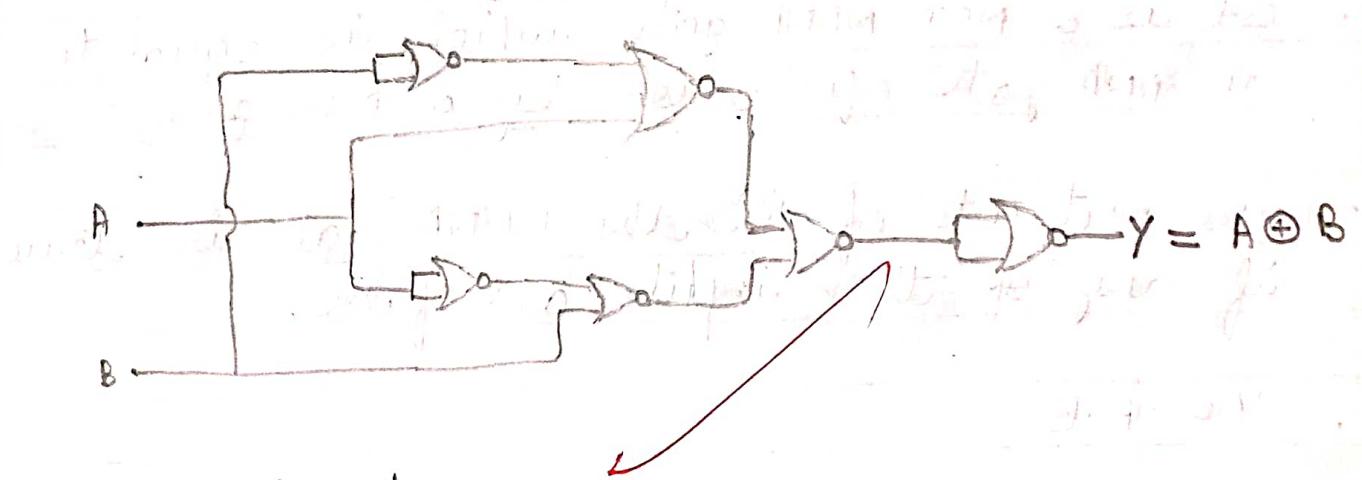


iii) (OR)

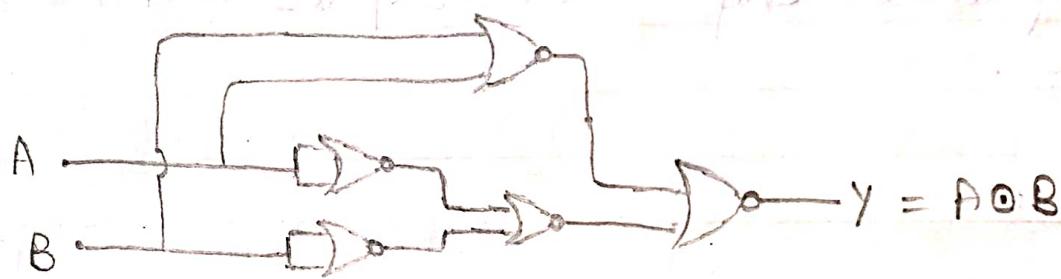


- NAND gate \Rightarrow
- It is a NOT-NAND gate which is equal to an AND gate followed by a NOT gate
- The output of all the NAND gate is true if any of the input are false.
- $Y = \overline{A \cdot B}$
- Integrated chip '7400' represents NAND gate.

iii) EX-OR gate:



(iv) EX-NOR gate:



(v) NOT gate:



Result :- We have studied universal gate.

Result :-

We have studied universal gates and implemented other gates using only NAND or only NOR gate.

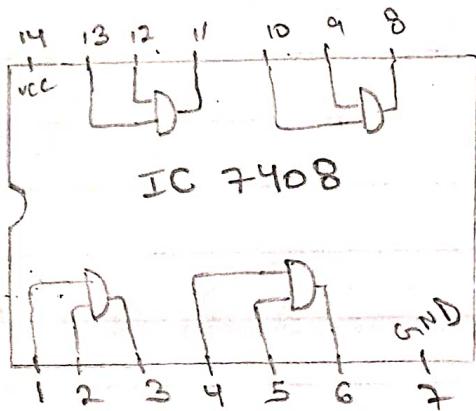
~~6/12/21~~

Experiment-4

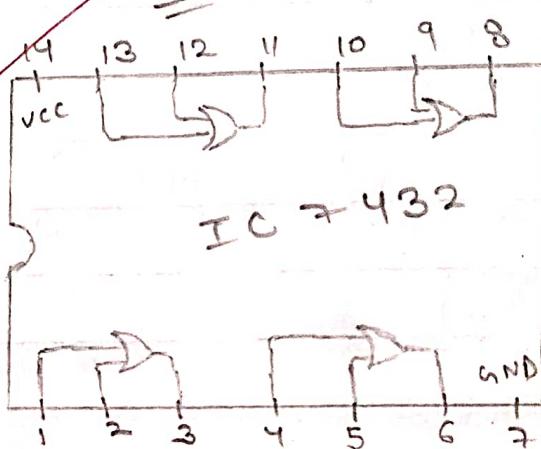
Aim:- To design and utilize a given function using K-map and verify its performance

Apparatus:- Digital trainers kit, cutters, pliers, ICS AND (7408), OR (7432), NOT (7404) and connecting wires.

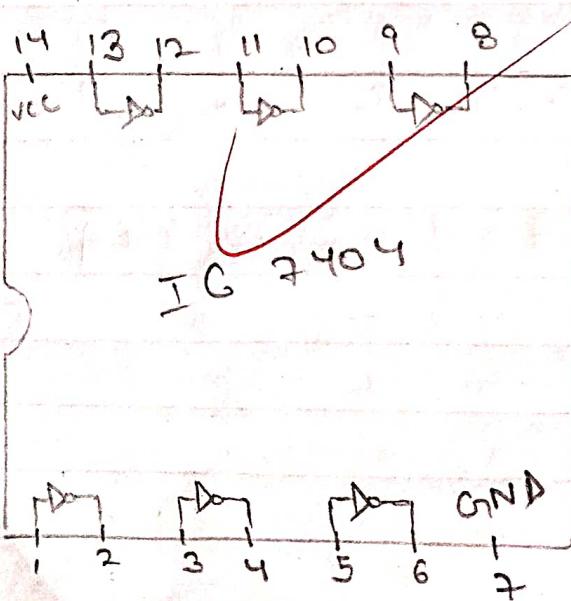
AND gate



OR gate



NOT gate



Experiment - 4

Aims:- To design and utilise a given function using K-map and verify its performance.

Apparatus :- Digital trainer kit, cutter connecting wires, plucker, ICs AND (7408), OR (7432), NOT (7404)

Theory :-

Boolean Algebra \Rightarrow It differs from both ordinary algebra & the binary number system. In boolean algebra, $A+A=A$ and $A \cdot A=A$ because variable A has only a logical value.

Karnaugh map (K-map) \Rightarrow

In this, we put the truth table in a compact form by labelling the rows and columns of a map. This is extremely useful and extensively used in minimization of function of 3, 4, 5 or 6 variable. The rows and columns are assigned a binary code (gray code) such that two adjacent rows or column differs in only 1 bit.

$$f = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$$

$\bar{A}B$	$C\bar{D}$	$\bar{C}D$	CD	$\bar{C}\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	1	1	1	1
$A\bar{B}$	1	1	1	1
AB	1	1	1	1
$\bar{D}\bar{C}$	1	1	1	1

$$\begin{aligned}
 F &\Rightarrow [m_0 + m_2 + m_8 + m_{10}] + [m_{12} + m_{13} + m_8 + m_9] \\
 &+ [m_0 + m_2 + m_4 + m_6] + [m_1 + m_3 + m_5 + m_7] \\
 &\Rightarrow A\bar{C} + \bar{B}\bar{D} + \bar{A}\bar{D} + \bar{C}\bar{B} \quad (\text{Ansatz})
 \end{aligned}$$

$$F = \pi M(2, 8, 9, 10, 11, 12, 14)$$

$\bar{A}+B$	$C+D$	$C+\bar{D}$	$\bar{C}+\bar{D}$	$\bar{C}+D$
$\bar{A}+B$	0	1	3	0
$\bar{A}+\bar{B}$	1	4	5	6
$\bar{A}+\bar{B}$	0	1	2	0
$\bar{A}+B$	0	0	10	0

$$\begin{aligned}
 F &\Rightarrow [m_2 \cdot m_8 \cdot m_{14} \cdot m_{10}] \cdot [m_8 \cdot m_9 \cdot m_6 \cdot m_{10}] \cdot [m_2 \cdot m_{10}] \\
 &\Rightarrow (\bar{A}+D) \cdot (\bar{A}+B) \cdot (\bar{C}+D+B)
 \end{aligned}$$

It consists of 16 of squares and each square is called cell.

Boolean functions \Rightarrow

\equiv A function of 'n' Boolean variables denoted by $F(x_1, x_2, \dots, x_n)$ is another variable of algebra and takes one of the two possible values 0 and 1.

(i) Sum of products (SOP) form \Rightarrow

It is also called Disjunctive Normal Form (DNF).

e.g.

$$F = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$$

By K-map, it reduces to

$$F = A\bar{C} + \bar{B}\bar{D} + \bar{A}\bar{D}$$

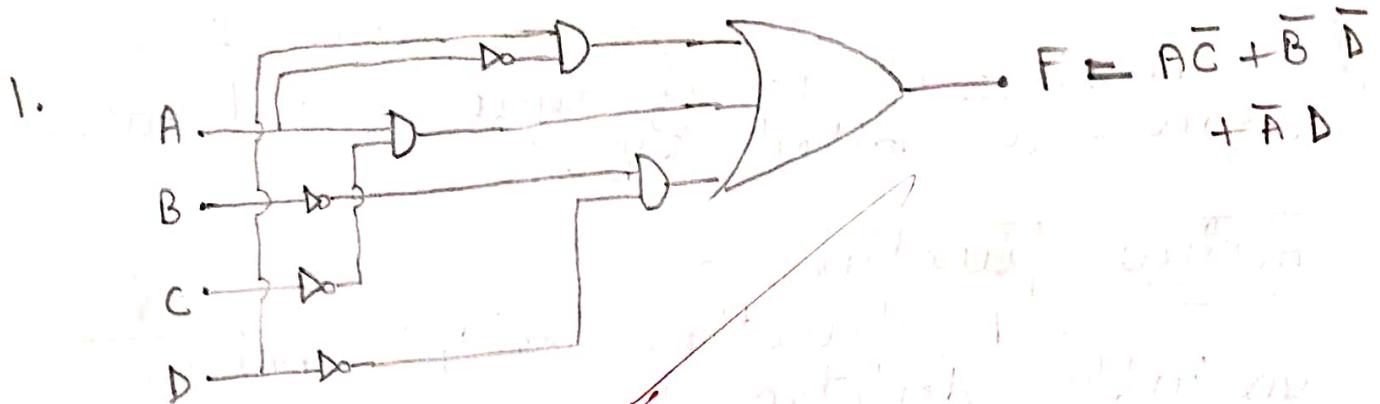
(ii) Product of Sum (POS) form \Rightarrow

It is also called conjunctive normal form (CNF).

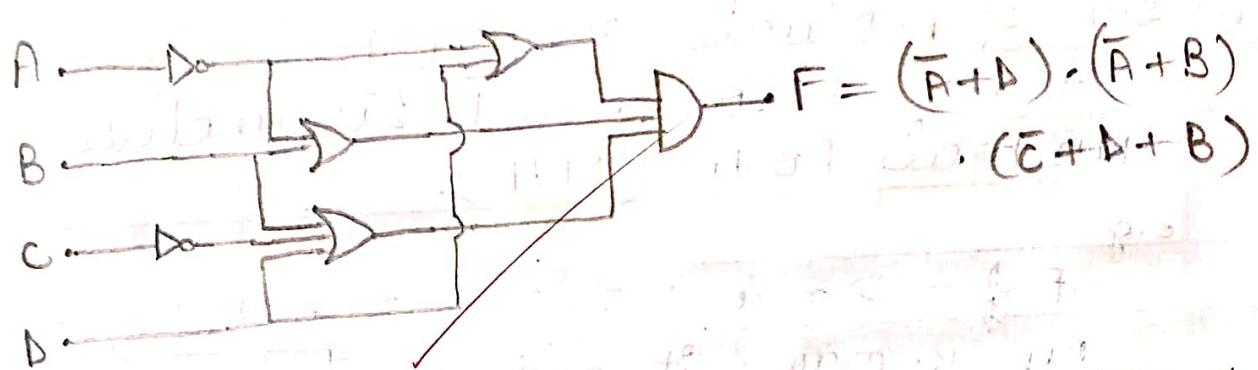
$$\text{e.g. } F = \prod M(2, 8, 9, 10, 11, 12, 14)$$

By K-map, it reduces to

$$F = (\bar{A} + B) \cdot (\bar{A} + D) \cdot (B + \bar{C} + D)$$



2.



Result :- A function is designed and utilized using K-map, and its performance is verified.

Result :-

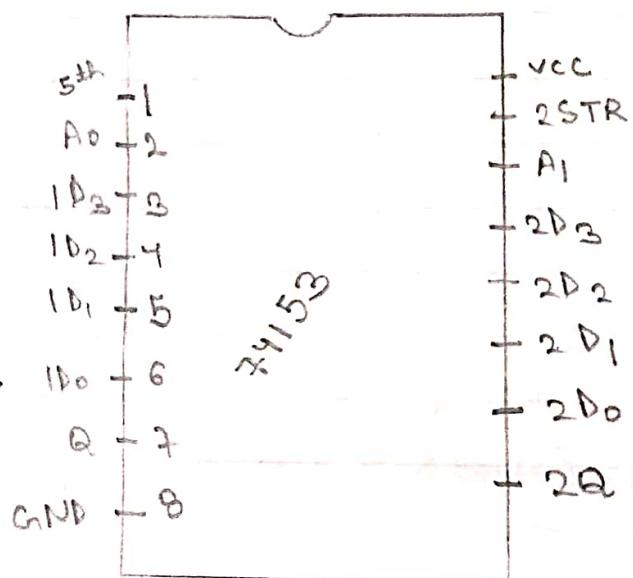
A function is designed and utilized using K-map and its performance is verified.

~~SP~~
06/12/21

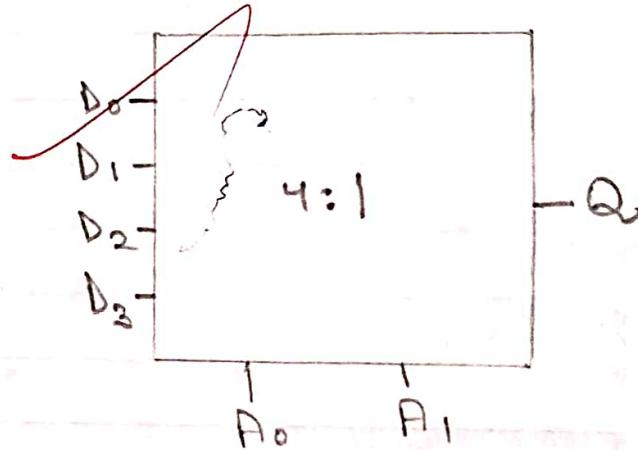
Experiment - 5

Aim : To study the operation of a multiplexer and demultiplexer, and verify the truth table.

Multiplexers :



M:1 (Multiplexers)



A ₀	A ₁	Y
0	0	D ₀
0	1	D ₁
1	0	D ₂
1	1	D ₃

✓ n = input line

n = select line

Experiment - 5

Aim:- To study the operation of a multiplexer & demultiplexer and verify the truth table.

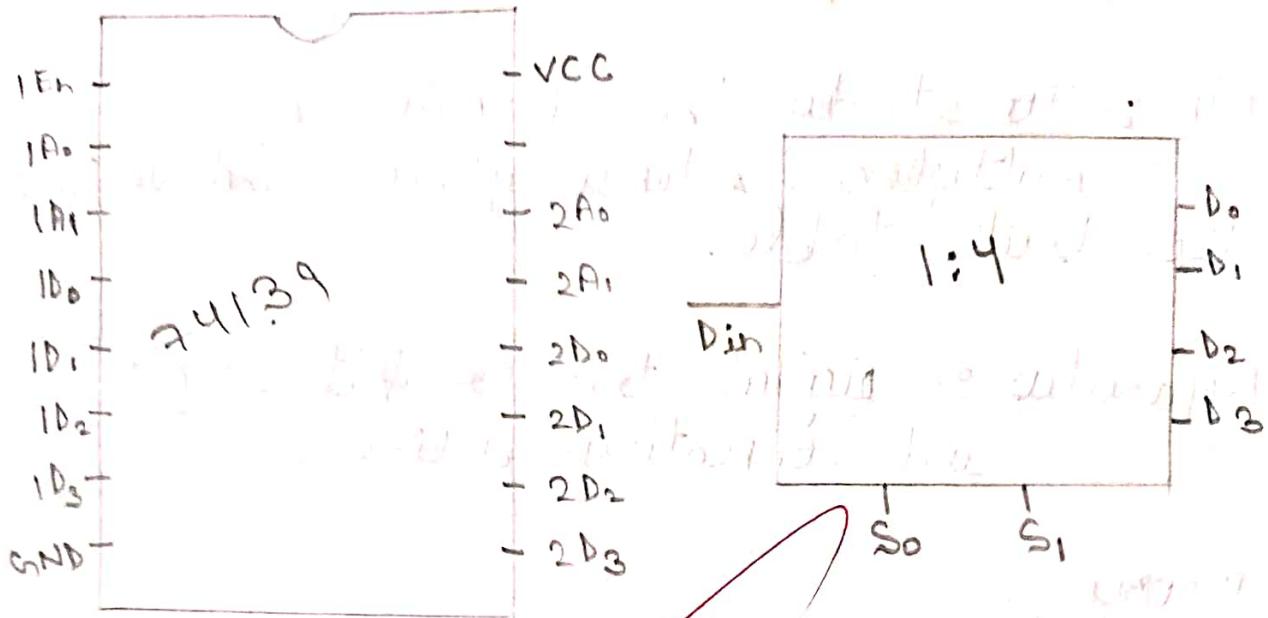
Apparatus :- digital trainer kit, IC's and connecting wires.

Theory :-

Multiplexer \Rightarrow Multiplexer is a combinational circuit that select binary information from one or many input channels and transmit to a single output channel.

Multiplexers are called data selectors because selection of particular input is selected by control lines. A multiplexer of 2^n input channel can be controlled by a no. of select lines and input lines is selected according to list combination of select lines. There are 'm' input lines and 'n' is the no. of select lines.

STROBE (str) / ENABLE \Rightarrow This pin is used for proper control operation of mux,



1:4 demux is selecting one output
and takes its time.

	IEn	Din	S0	S1	D0	D1	D2	D3
1	0	1	0	0	0	1	1	1
2	0	1	0	1	1	0	1	1
3	0	1	1	0	1	1	0	1
4	0	1	1	1	1	1	1	0

Result :- We have

We have studied the multiplexers and demultiplexers and verified them using truth table.

If have any doubt feel free to ask
exam is on 17/12/2019

It is a active low pin used to expand to a more mux with the large numbers of input. D_0, D_1, D_2, D_3 are input lines. A_0, A_1 are select lines and Q is the output.

Demultiplexer \Rightarrow A demultiplexer is a combinational circuit which means one input to many output. It is a logic circuit which gives information to a single input line and the same over, one of the possible 2^m output lines. The selection lines of specific output is controlled by bit combination of selection lines. ' n ' is the number of output lines and ' m ' is the no. of ~~select~~ ^{select} lines. D_0, D_1, D_2, D_3 are the ~~input~~ lines, output lines while A_0 and A_1 are select lines.

Procedure :

- a. For multiplexer \Rightarrow using the IC-74153, make connections as shown in figure (a) for different combination of inputs, find the output and verify the truth table.

- 1.b. For Demultiplexer \Rightarrow using the IC - 74139
make connections as shown in figure (b) for different combination of input, find the output and verify the truth table.

Precautions :-

- Circuit diagram should be neat and clear.
- Handle the kit carefully.
- All the connections should be tight.

Result :-

We have studied the multiplexer and demultiplexer and verified them using truth table.

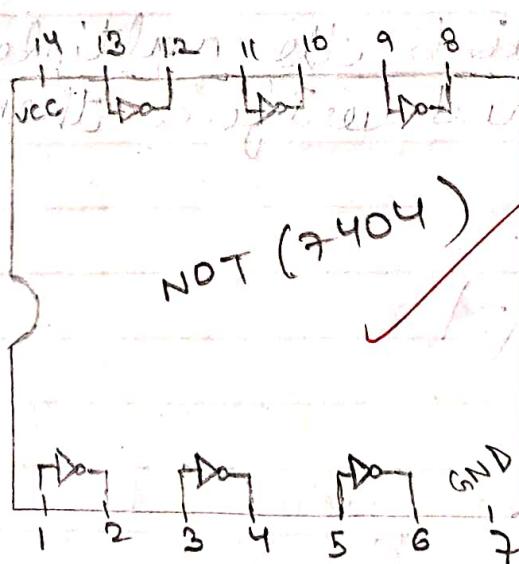
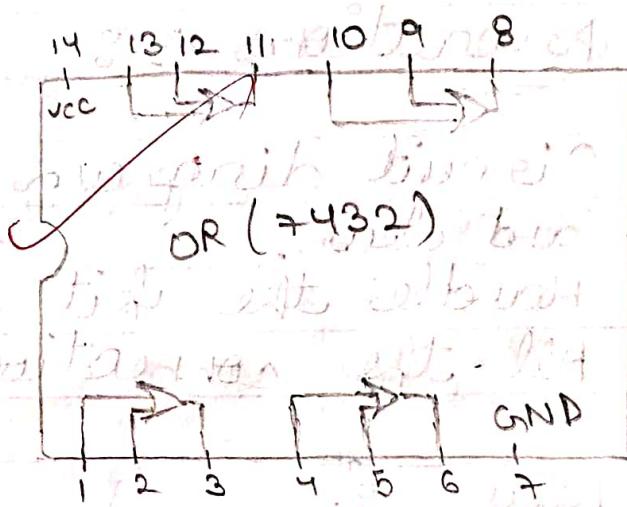
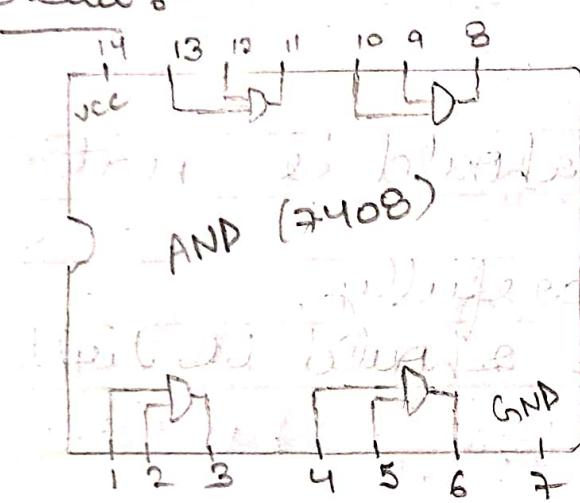
~~13/12/21~~

Experiment - 6

Aim :- To design a full adder and half adder circuit.

Apparatus :- Digital trainer kit, cutters, connecting wires, pliers, ICs, 7408 (AND), 7432 (OR), 7404 (NOT).

Circuit :-



Experiment - 6

Aims:- To design a full adder and half adder circuit.

Apparatus:- Digital Trainer kit, cutters, connecting wires, pliers, IC's 7408 (AND), 7432 (OR), and 7404 (NOR).

Theory :-

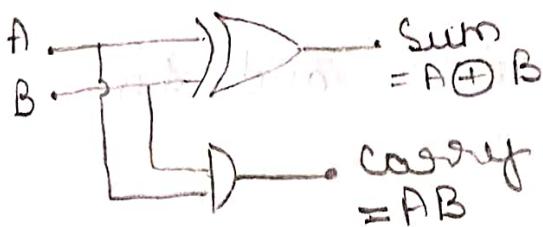
Karnaugh map \Rightarrow

- It is extremely useful and extensively used in minimisation of function of 3, 4, 5 or 6 variable.
- The rows or columns are assigned a grey code such that two rows or columns differ by 1 bit.
- It consists of no. of squares and each is called cell.

Adder \Rightarrow

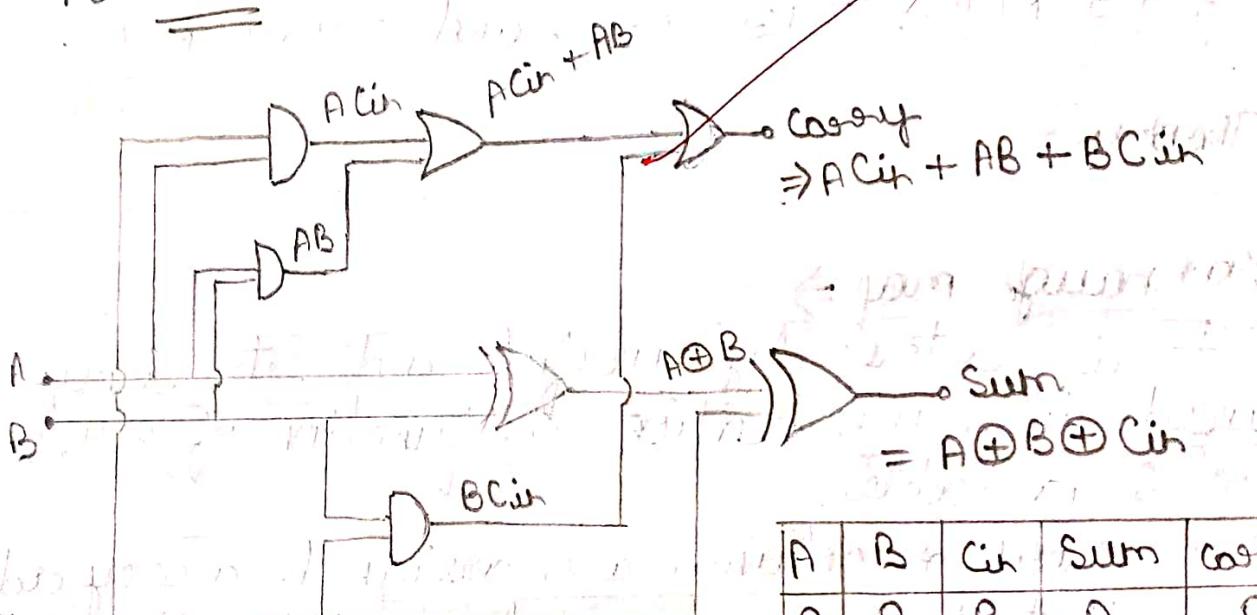
- An adder is a digital logic circuit in electronics that implements addition of numbers.
- In many computers and processors, adders are used to calculate addresses, similar operations of ALU etc.

Half adder circuit



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adder circuit



A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-Map

	AB	00	01	11	10
Cin	0	0	1	1	0
	0	0	1	1	0
	1	0	1	1	0
	1	1	0	0	1

Sum: $A \oplus B \oplus C$

	AB	00	01	11	10
Cin	0	0	1	1	0
	0	0	1	1	0
	1	0	1	1	0
	1	1	0	0	1

Carry = $AB + BC + CA$

Adders are classified into two types - half adder and full adder.

1. Half adder circuit \Rightarrow

It adds two binary digits called as augend and addend and produces two outputs as sum & carry. OR is applied to both inputs to produce sum and AND to produce carry.

Sum and carry are obtained by two inputs A & B.

$$\text{Sum} = A\bar{B} + \bar{A}B = A \oplus B$$

$$\text{carry} = AB$$

2. Full adder circuit \Rightarrow

It adds 3 one bit number, where two can be referred as operands and one can be referred to as bit carried in and produces 2-bit output and this can be referred to as output carry & sum. It has 3 inputs, A, B and C_{in} .

$$\begin{aligned}\text{By K-Map: Sum} &= \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C} + A\bar{B}\bar{C} \\ &= \bar{A}(\bar{B}C + B\bar{C}) + A(B\bar{C} + \bar{B}\bar{C}) \\ &= \bar{A}(B \oplus C) + A(\bar{B} \oplus C) \\ &= A \oplus B \oplus C\end{aligned}$$

$$\text{carry} = AB + BC + CA$$

Result :-

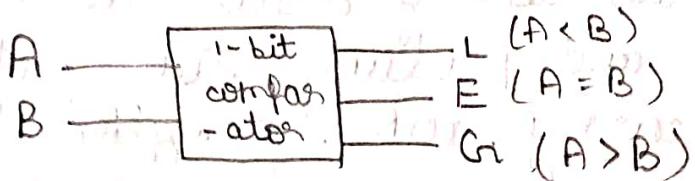
Full adder and half adder circuit are designed.

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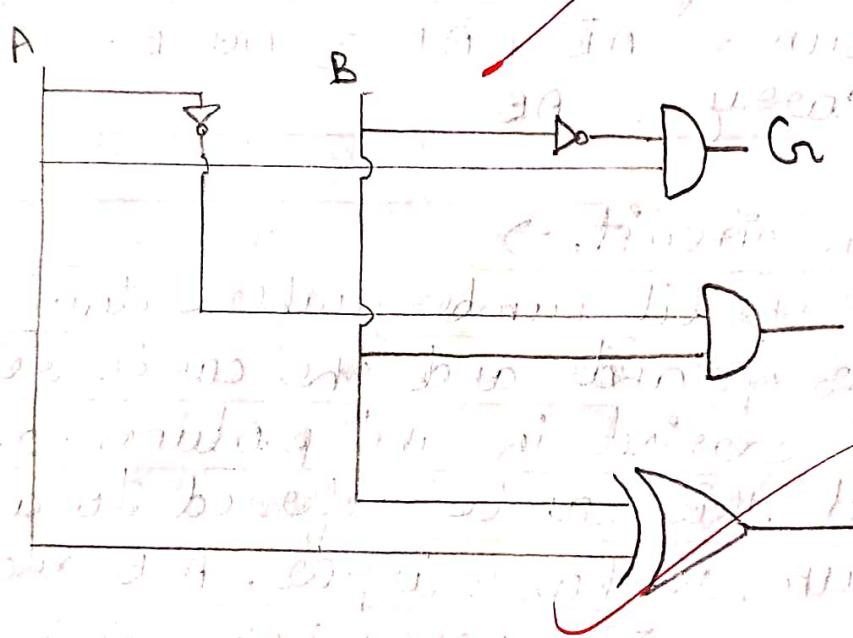
Experiment - 7

Aim :- To verify the operation of 1-bit comparator using gates.

Block Diagram :-



Circuit Diagram :-



Experiment-7

Aim:- To design and verify 1-bit comparator using gates.

Apparatus:- Digital trainer kit, IC's, connecting wires.

Theory :- A comparator is a logic circuit used to compare the magnitude of two binary numbers.

Depending on the design, it may either simply provide an output that is active when the two numbers are equal or additionally provide output that signify which of the number is greater when equality does not hold. The X-NOR gate is a basic comparator because its output is a one, only if its two input are equal i.e. the output is 1 if and only if the input bits coincide.

Procedure :-

1. Using IC (7408), (7404), (7486) [AND, NOT, X-OR]
Design the circuit for a 1-bit magnitude.

Truth Table :-

INPUT		OUTPUT		
A	B	L	E	G ₁
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

2. Verify the truth table of comparator for different combination of input.
3. observe the output.

Precautions

1. Handle the bits carefully.
2. All connections should be tight and made carefully.

Result :-

We have studied and verified the operation of comparator.

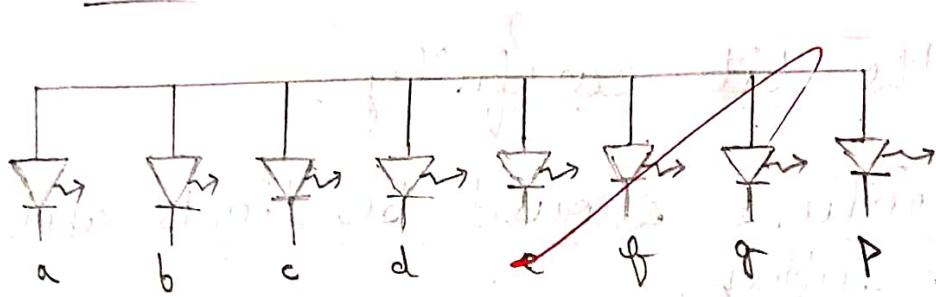

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Experiment - 8

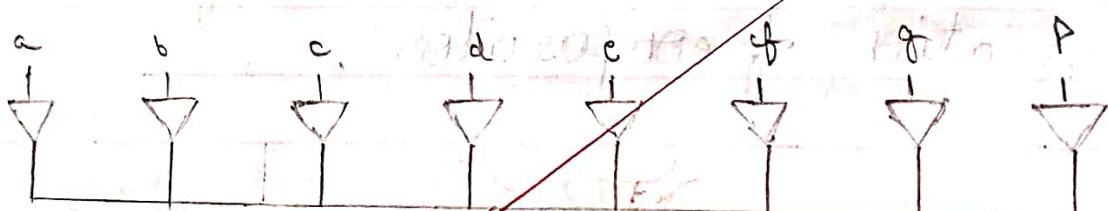
Aim :- To verify the operation of seven segment decoder.

Apparatus Required :- IC 7447, 7-segment display
mode - TTL 20 MHz

Common anode :-



common cathode :-



Experiment-8

Aim :- To verify the operation of seven segment display

Requirement :- IC 7447, 7-segment display

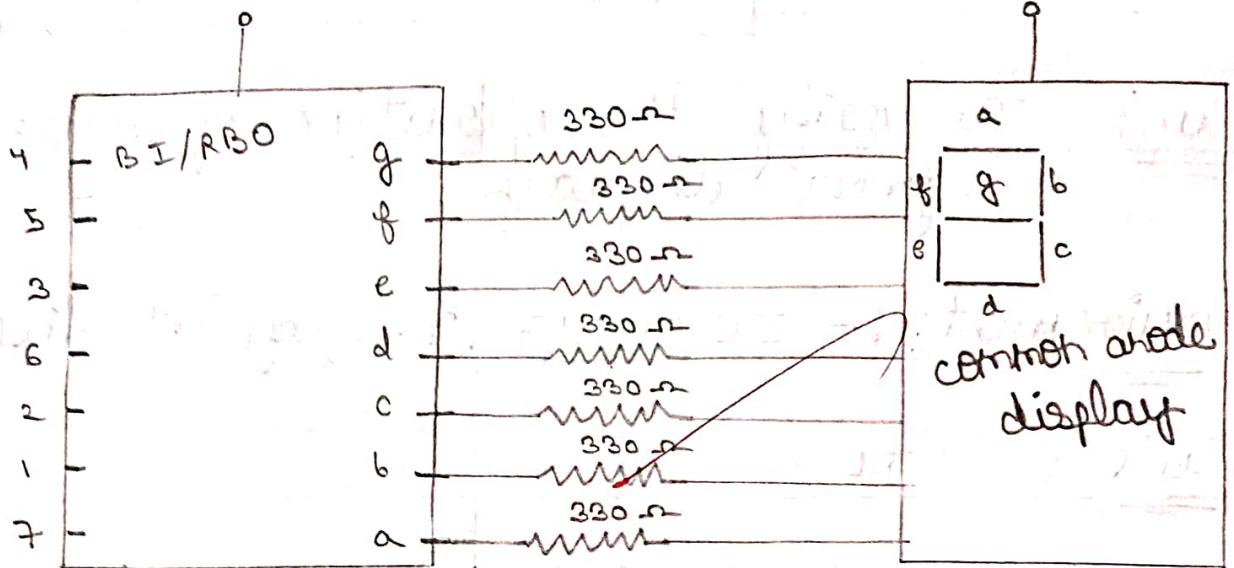
Mode :- TTL

Theory :- A seven segment decoder/driver is an IC decoder that can be used to drive a seven segment indicator.

There are two types of decoder: 1. driver, corresponding to common anode and common cathode indicators. Each decoder driver has 4 BCD input and 7 output pins segment.

BI / RBD :- When this pin is at low logic level all segment outputs are off regular of the level of any other input. It must be at high logic or open to get for 0000 to 1111.

BI / RBI :- The ribbon ripple blanking input must be open as high if blanking of a decimal zero is not observed if it is low, it will blink decimal zero.



control anode display

We successfully verified the result of BCD to 7-segment decoder, with R = 330 ohm's placed above each segment.

LT 8- When blanking inputs / ripple blanking output BI/RBO is open or held high and a low is applied to this output, all segment output are ON.

Procedure :-

1. connect all connection as like circuit diagram.
2. observe decimal output on common anode display given on the experiment board. output of individual pins can be seen logic probe or an LED display of digital lab STZ611 or an multimeter.
3. Connect different combinations of inputs as shown in truth table and prove that.
4. Repeat step 5, 6 and observe the result.
5. connection logic 0 to LT input, logic 1 to RBI and ~~BT/RBO~~ input.
6. Repeat steps and observe the result.
7. connect logic 0 to RBI input and ~~B C D~~ input logic 1 to LT & BI/RBO input and observe the result.

Result :-

We successfully verified the result of BCD to 7-segment decoder.

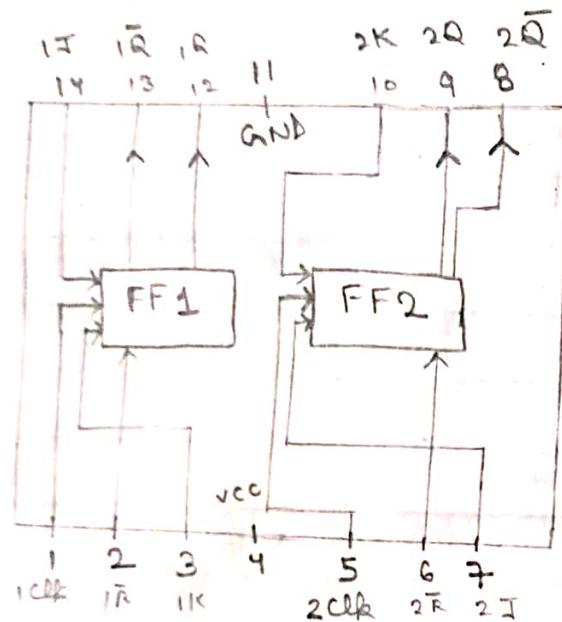
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Experiment - 9

Aim:- To verify truth table of JK, T and D flip flop.

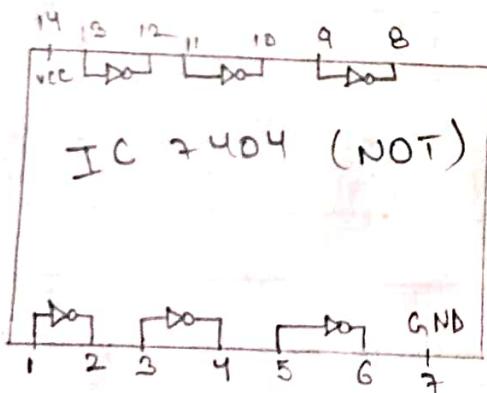
Apparatus :- Digital trainer kit, cutter, plucker, IC 7473 (JK flip flop) & connecting wires, IC (7404) NOT

Circuit Diagram :-

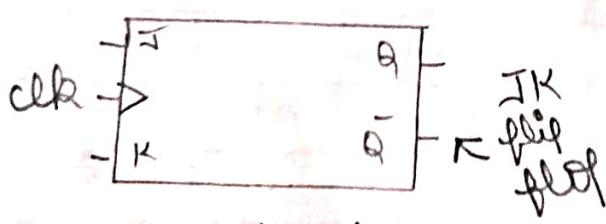


I C
7473
JK
flip flop
↔

I/P		O/P			
\bar{R}	Clk	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	D	L	L	No charge	
H	↑	L	H	L	H
H	↑	H	L	H	L
H	↑	H	H	H	L
				Toggle	



C	J	K	Q_n	Q_{n+1}	state
↑	0	0	0	0	No charge
↑	0	0	1	1	
↑	0	1	0	0	
↑	0	1	1	0	Reset
↑	1	0	0	1	
↑	1	0	1	1	Set
↑	1	1	0	1	
↑	1	1	1	0	Toggle



$C=0$, No change

Experiment - 9

Aim:- To verify truth table of J, K, T and D flip flop.

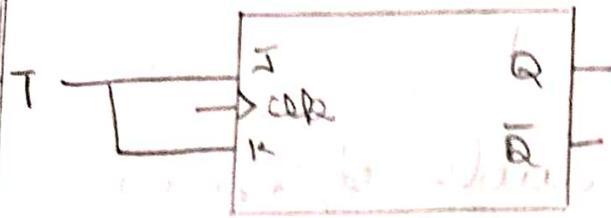
Apparatus:- Digital trainer kit, pliers, cutter, IC 7473 (JK flip flop), 7404 (NOT) and connecting wires.

Theory :-

Flip flop \Rightarrow It is the most important memory element made of logic gates. A flip flop known as bistable multivibrator has 2 stable states. Its state can be changed by applying proper triggering signal. It is also called binary or one-bit memory.

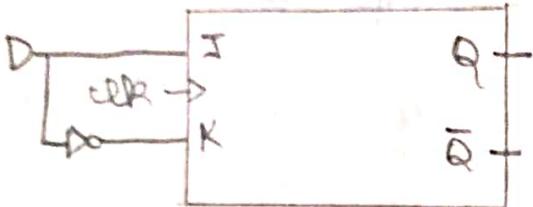
J-K flip flop \Rightarrow It is very versatile and also the most widely used.

- When $J=0$ & $K=0$, no change of state takes place.
- $J=0$ & $K=1$, flip flop resets at +ve going edge of clock pulse.
- $J=1$ & $K=0$, flip flop sets at positive going edge of clock pulse.



T flip flop from
JK flip flop

C	T	Q_n	Q_{n+1}	State
↑	0	0	0	No change
↑	0	1	1	No change
↑	1	0	1	Toggle
↑	1	1	0	Toggle



D flip flop from
JK flip flop

C	D	Q_n	Q_{n+1}	State
↑	0	0	0	Reset
↑	0	1	0	
↑	1	0	1	Set
↑	1	1	1	Set

$c=0$, No change

Result :- The truth table of JK, T & D flip flop are studied and verified.

• $J=1 \& K=1$, flip flop toggles.

T flip flop \Rightarrow It has a single control i/p labelled T for toggle.

When T is high, flip flop toggles on every new clock pulse & when T is low, flip flop remains in previous state.

D flip flop \Rightarrow It has only one i/p terminal. It may be obtained by putting inverter between J & K terminal.

Result :-

The truths table of JK, T and D flip flop are verified.

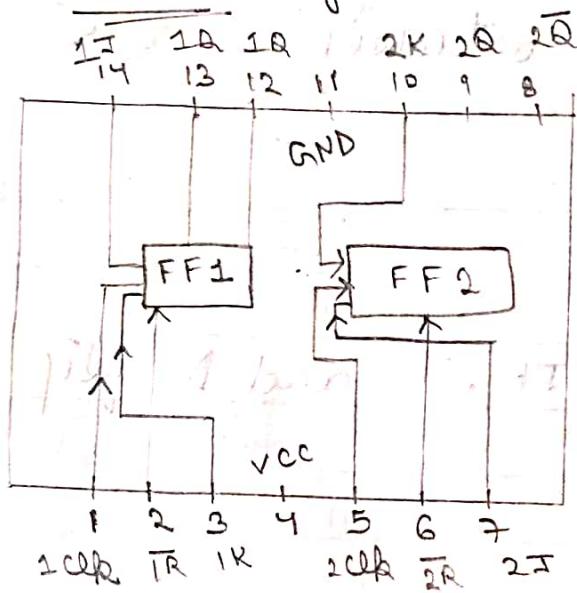
Experiment - 10

Aim :-

To design a 3-bit Asynchronous & synchronous counter

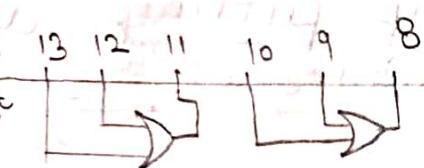
Apparatus :- Digital trainer kit, pliers, IC's 7473 (JK FF), 7408 (AND), 7404 (NOT), 7432 (OR) and connecting wires.

Circuit Diagram :-

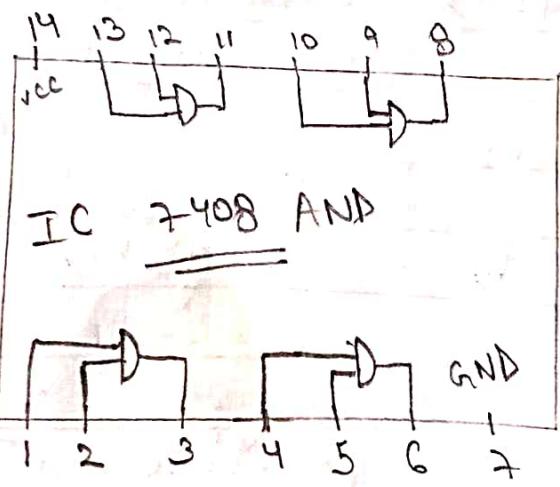
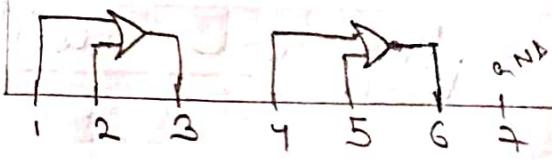


IC
7473

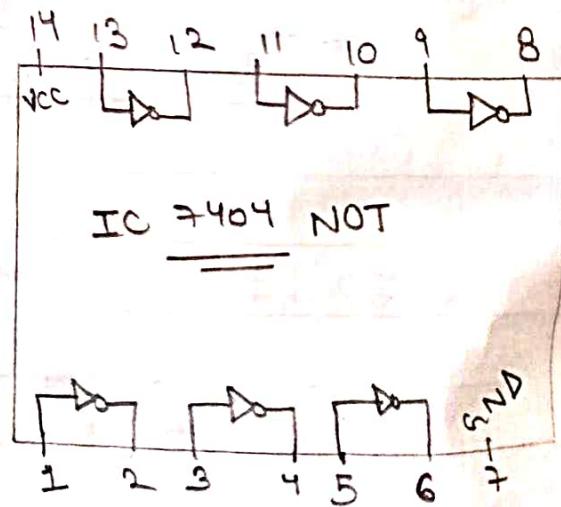
JK
FF



IC 7432 OR



IC 7408 AND



IC 7404 NOT

Experiment - 10

Aims :- To design a 3-bit Asynchronous & synchronous counter.

Apparatus :- Digital trainer kit, plucker, IC's 7473 (JK flip flop), 7408 (AND gate), 7432 (OR gate), 7404 (NOT gate) and connecting wires.

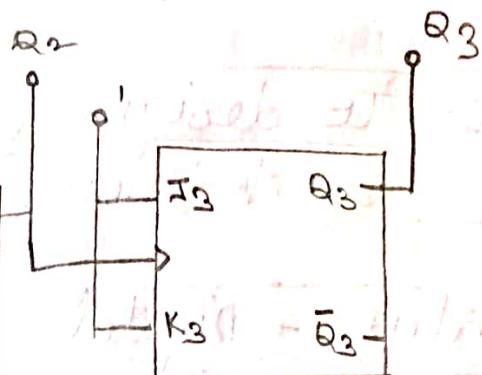
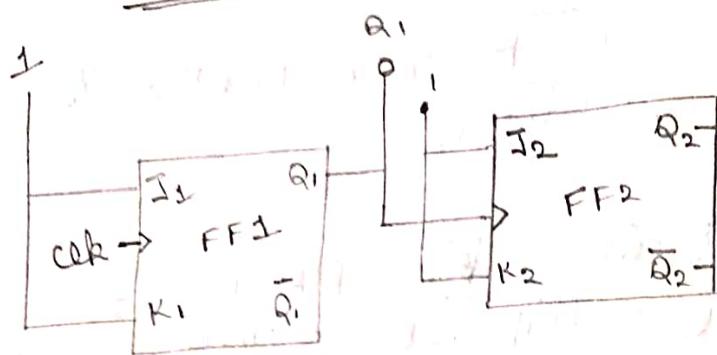
Theory :-

Counter \Rightarrow A digital counter is a set of flip flops whose states can change in response to pulse applied at the input to the counter.

Asynchronous Counter \Rightarrow Also called as ripple counter or serial or series counter, it is simplest type of counter, easiest to design and requires the least amount of hardware.

Synchronous Counter \Rightarrow They are the counters in which all the flip flops triggered simultaneously by the clock-input pulse. They are thus faster than asynchronous counter,

Asynchronous counter



A 3-bit UP Asynchronous counter

Synchronous counter

K-MAP for a 3-bit Synchronous UP counter

		Q ₃ Q ₂	00	01	11	10
		Q ₁	0	2	6	4
Q ₁	Q ₂	0	0	X	X	
		1	1	3	7	5

		Q ₃ Q ₂	00	01	11	10
		Q ₁	0	2	6	4
Q ₁	Q ₂	0	X	X	1	0
		1	X	X	1	0

$$J_3 = Q_2 \cdot Q_1$$

		Q ₃ Q ₂	00	01	11	10
		Q ₁	0	2	6	4
Q ₁	Q ₂	0	X	X	0	0
		1	X	X	1	0

		Q ₃ Q ₂	00	01	11	10
		Q ₁	0	2	6	4
Q ₁	Q ₂	0	X	1	0	0
		1	X	1	0	0

$$J_2 = Q_1$$

$$K_2 = Q_1$$

because propagation delay is involved less. But they are complex to design.

Result :-

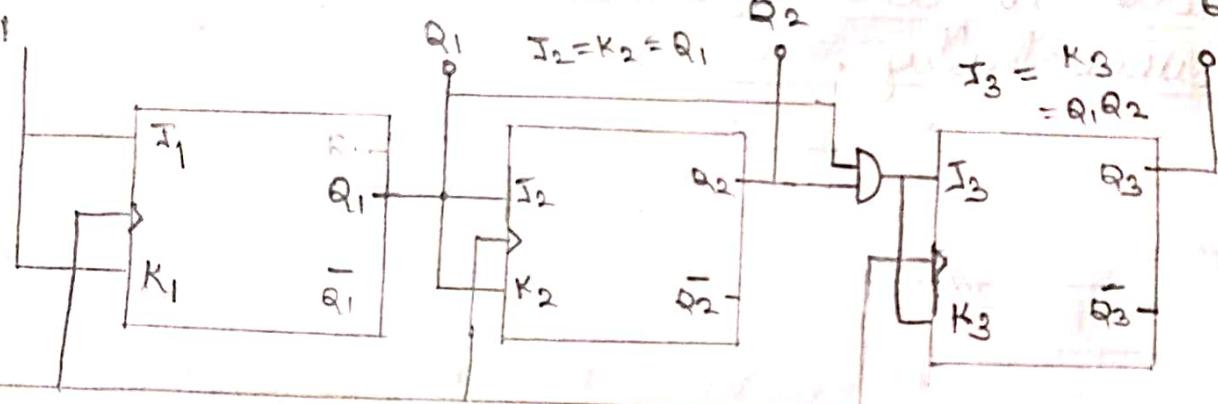
A 3 bit Asynchronous & synchronous counters are designed and verified successfully.

	Q_3	Q_2	Q_1	Q_0
	00	01	11	10
0	1	1	1	1
1	x	x	x	x

	Q_3	Q_2	Q_1	Q_0
	00	01	11	10
0	1	2	6	4
1	1	3	7	5

$$J_1 = 1 \quad K_1 = 1$$

$$J_2 = K_2 = Q_1 \quad J_3 = K_3 = Q_1 Q_2$$



clk

A 3-bit Synchronous UP Counter

Result :- A 3 bit Asynchronous & synchronous counters are designed and verified successfully.

Experiment :

Date _____
Page No. 28

Result :- A 3-bit Asynchronous &
synchronous counter are designed
& verified successfully.