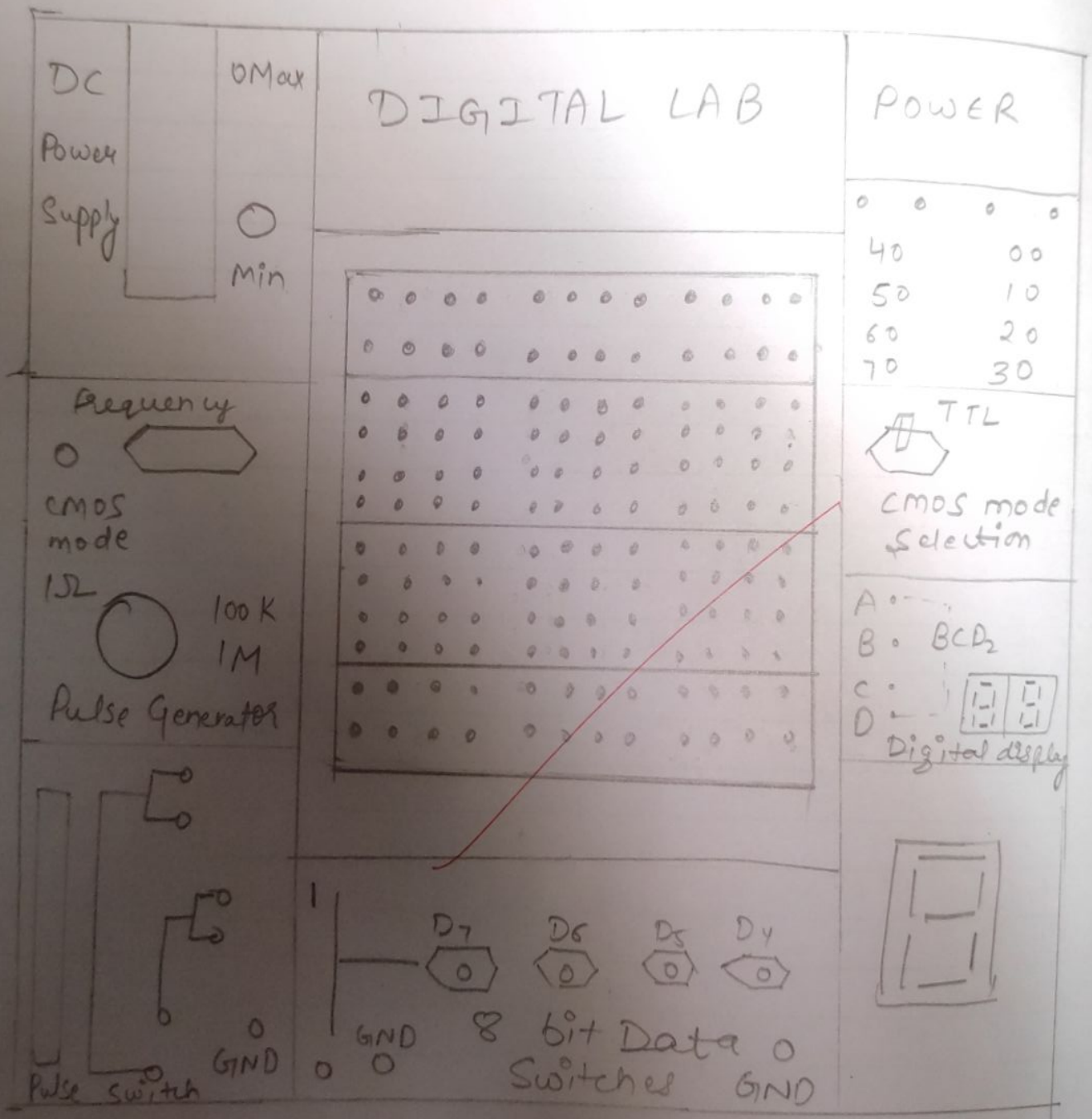
Exp-1

* **Aim** : Familiarisation with digital trainer kit and associative components.

* **Apparatus** :- Digital trainer kit



Expt. No. 1 Date 16/8/18

Page No. 1

EXPERIMENT-1

* **AIM** :- Familiarisation with digital trainer kit and associative components.

* **APPARATUS** :- Digital trainer kit

* **THEORY** :- ST2611 Digital lab

→ **DC Power** : It provides fixed DC o/p of +5V and -5V and variable DC o/p from +3V to +15V and -3V to -15V.

→ **Pulse Generator** : It generates stable pulse of frequency range 10 Hz to 1 MHz with TTL and CMOS mode. When TTL mode is selected, amplitude will be compatible with TTL & when CMOS is selected, it is compatible with CMOS.

→ **Pulse Switches** : Two pulse switches are provided for triggering purpose Each has two o/p normal and complimentary.

o/p level TTL : High - 5V, Low - 0V

CMOS : High = 3V to 15V

Low = 0V.

Teacher's Signature : _____

* 8-bits DATA SWITCHES :-

→ These switches provide two state i.e high & low.

TTL : high = +5V
low = +0V.

* Logic probe :-

→ When I/p is high, the display will show 'H'.
→ When it is low, it will show 'L'.
→ When no I/p is given, it ll show '0', and
→ 'P' in case of transition

* Digital Display :-

→ Two digital displays are provided. These are BCD to 7-segment display, which converts BCD to equivalent decimal no.

* MODE SELECTOR SWITCH :-

↝ When switch is put on "TTL" or "CMOS" posit" O/p of pulse generator, pulse switches, 8-bits data switches and inputs of digital probe 8-bits LED display ll meet the high or low level of "TTL" or "CMOS".

Teacher's Signature : _____

* RESULT → We have performed experiment at Trainer's kit

* MODE SELECTOR SWITCH to TTL POSITIONS :-

Low level : 0V
High level = +5V
Transistor = HI > LO or LO > HI

* MODE SELECTOR SWITCH to 'CMOS' POSITIONS :-

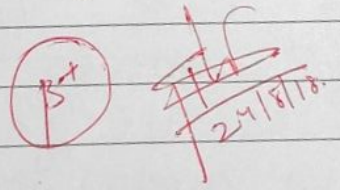
Low level = 0V
High level = +3V to +15V
Transist = HI > LO or LO > HI

* 8-bits LED DISPLAY :-

⇒ When o/p to this block is high, LED'll glow red & when o/p is low, LED'll glow green.

* RESULT :-

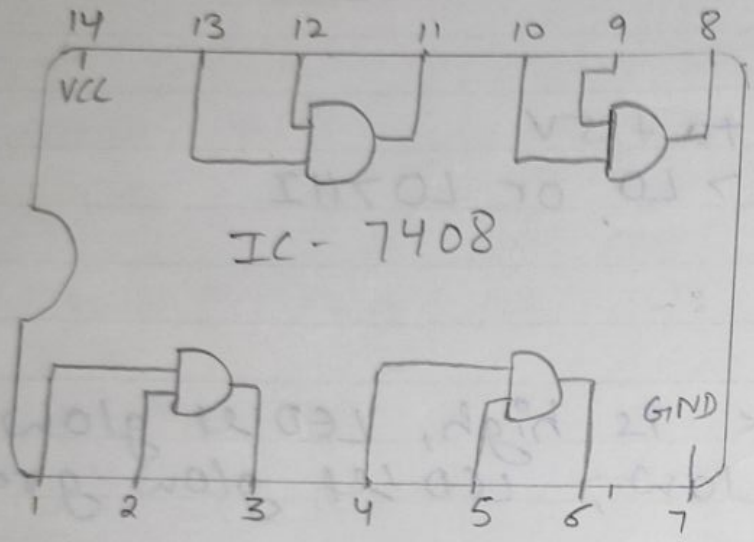
⇒ We have performed experiment at Trainee's Kit



Exp-2

* **Aim** → Study of TTL gates - AND, OR, NOT NOR, NAND, EX-OR and EX-NOR.
* **Apparatus** → Trainer kit, connecting wires

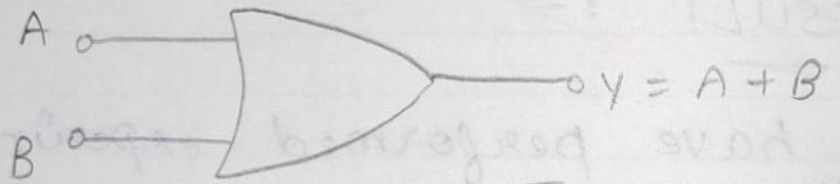
- **AND Gate :-**

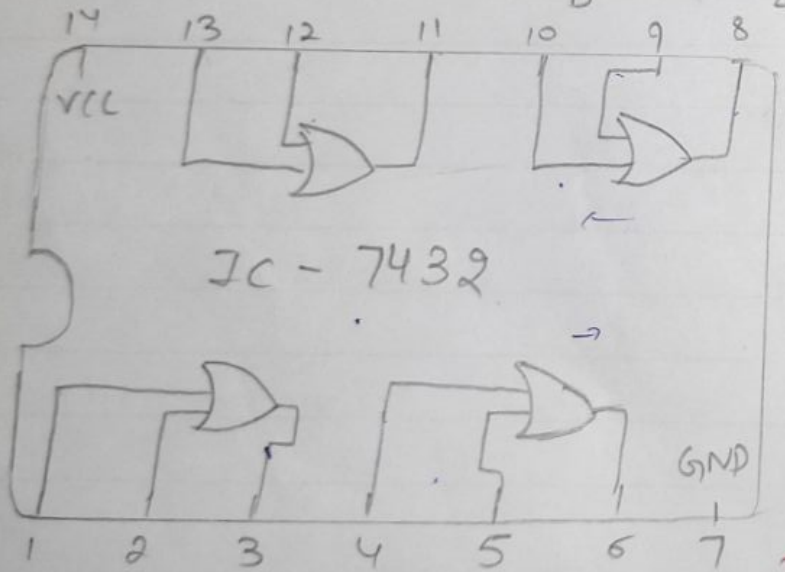


TRUTH TABLE.

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate :-





TRUTH TABLE

Input		Output
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

EXPERIMENT-2

* **Aim** : Study of TTL gates - AND, OR, NOT, NOR, NAND, EX-OR and EX-NOR.

* **APPARATUS** : Trainer kit, connecting wires

* **THEORY** :

- **AND** gate - It is an electronic ckt that gives a true o/p only if all its input are true. Dot (·) is used to show AND operation.

  $Y = A \cdot B$

- **OR** gate - It is an electronic ckt that gives a true o/p if one or more of its i/p are true. Plus (+) is used to show OR operation.

  $Y = A + B$

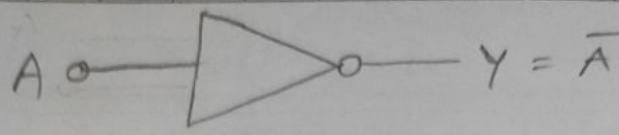
- **NOT** gate - It is an electronic ckt that produces an inverted versions of I/P as its o/p.

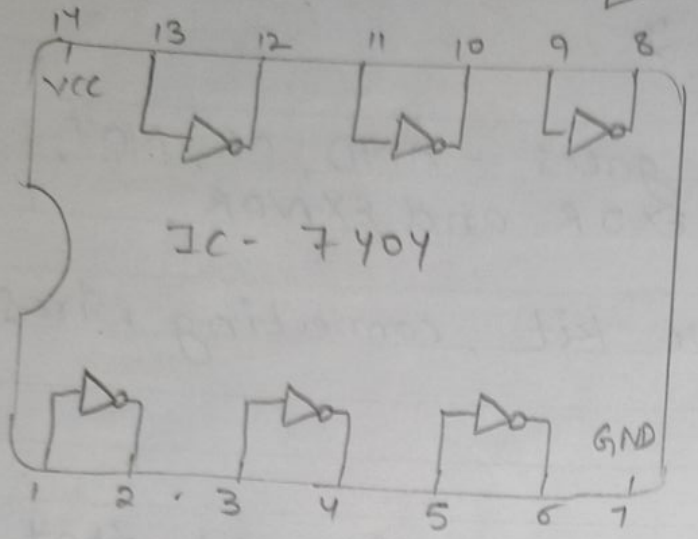
→ It is also known as inverted
→ If the i/p variable is A, the inverted o/p is known as NOT A.
→ NOT A is represented by $\overline{A}$.

$Y = \overline{A}$

Teacher's Signature : _____

NOT Gate -

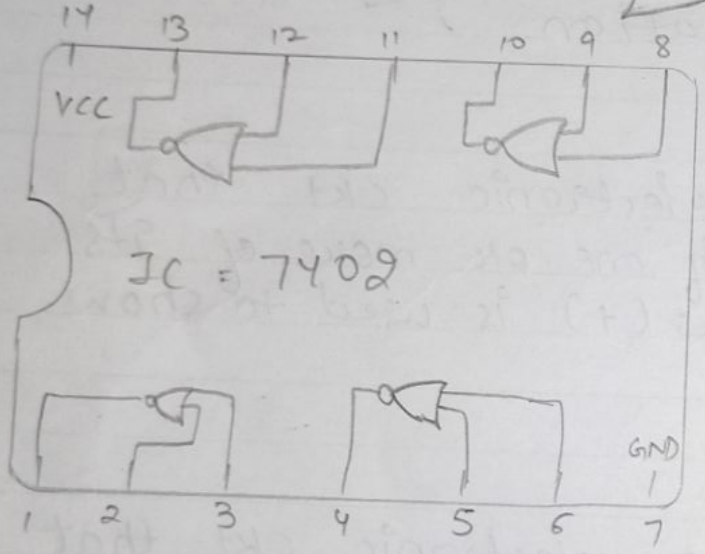




TRUTH TABLE

Input	Output
A	Y = Ā
0	1
1	0

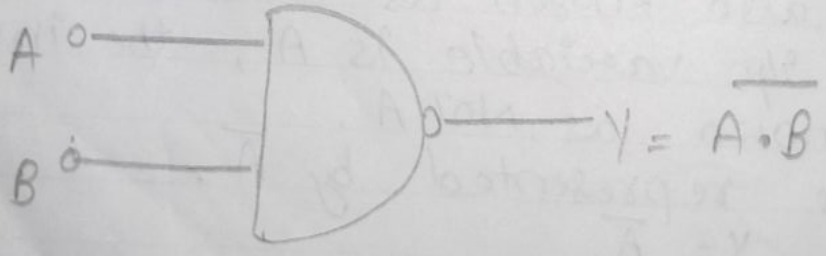
NOR Gate -



Truth Table

Input		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

NAND Gate -



NOR gate -

→ It is a NOT-OR gate which is equal to an OR gate followed by a NOT gate.
→ The o/p of all NOR gate are false if any of the input are true.

$$Y = \overline{A+B}$$

NAND gate -

→ It is a NOT-AND gate which is equal to an AND gate followed by a NOT gate.
→ The o/p of all NAND gate true if any of input are false.

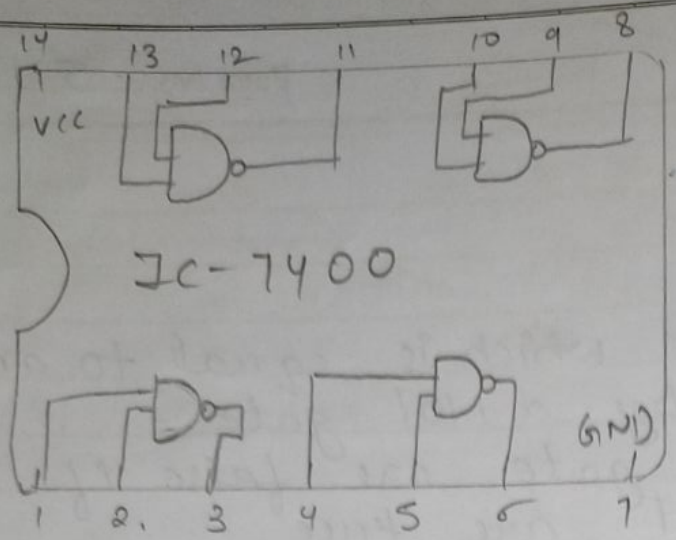
$$Y = \overline{A \cdot B}$$

EXOR gate -

→ The 'Exclusive-OR' gate is a circuit which will give a true o/p if either, but not both of its two i/p are there.
→ An encircled plus sign (⊕) is used to show Ex-OR operation

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$

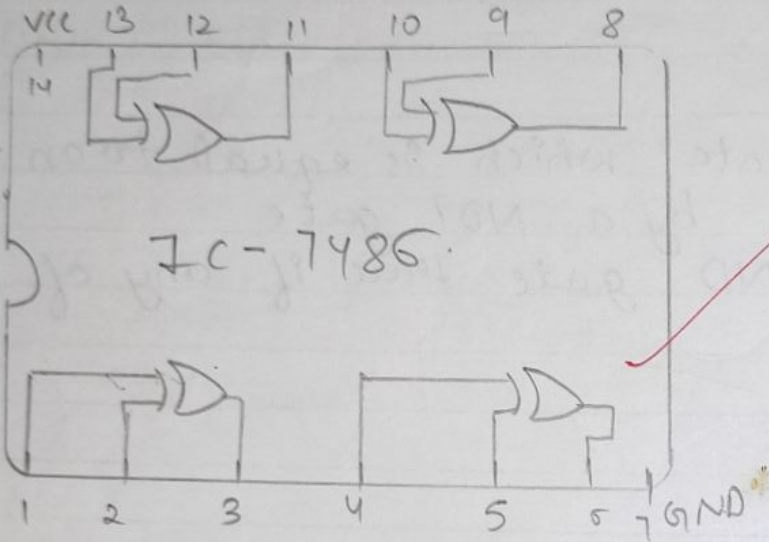
Teacher's Signature : _____



Truth Table.

I/P		O/P
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

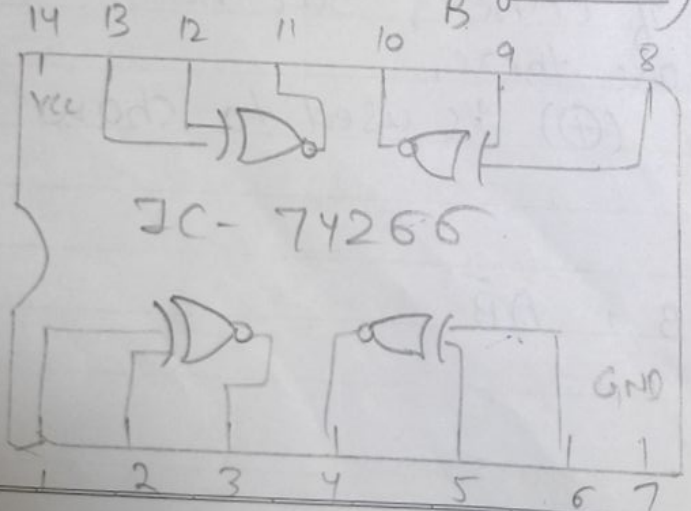
- Ex OR Gate



Truth Table

I/P		O/P
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

- Ex-NOR Gate.



Truth Table

I/P		O/P
A	B	$Y = A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

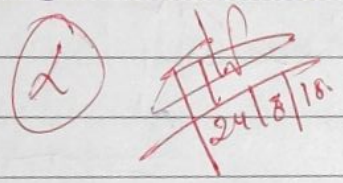
⑥ Ex-NOR gate

The "Exclusive - NOR" gate circuit does the opposite of EXOR gate.
It will give a false O/P if either, but not both of its I/p are true.
The symbol of Ex-OR is a small circle on O/P

$$Y = A \odot B = \bar{A}\bar{B} + AB$$

* RESULT :-

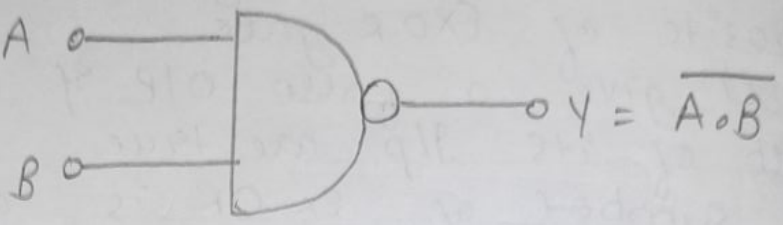
⇒ We have studied TTL gates and verified them and also studied their truth table.

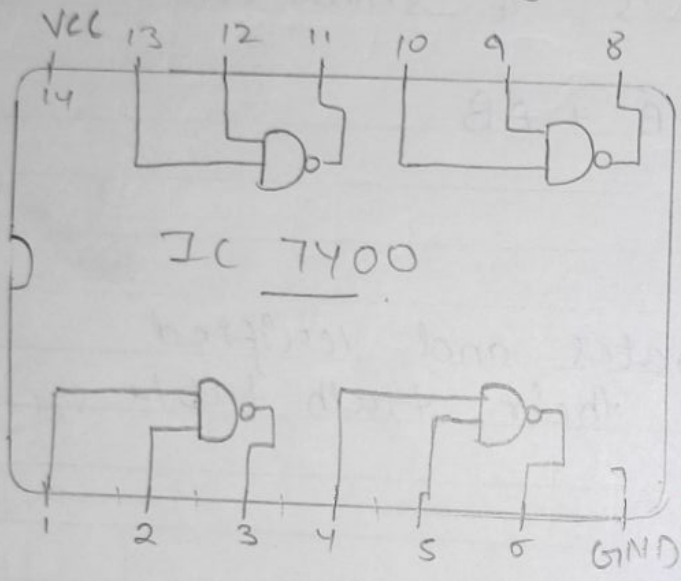


EXPERIMENT-3

* Aim - ~~Study~~ Design of all the gates using of Universal Gates
* Apparatus - Digital trainer Kit, connecting wires, ICs 7402 and IC 7400.

- NAND gate -

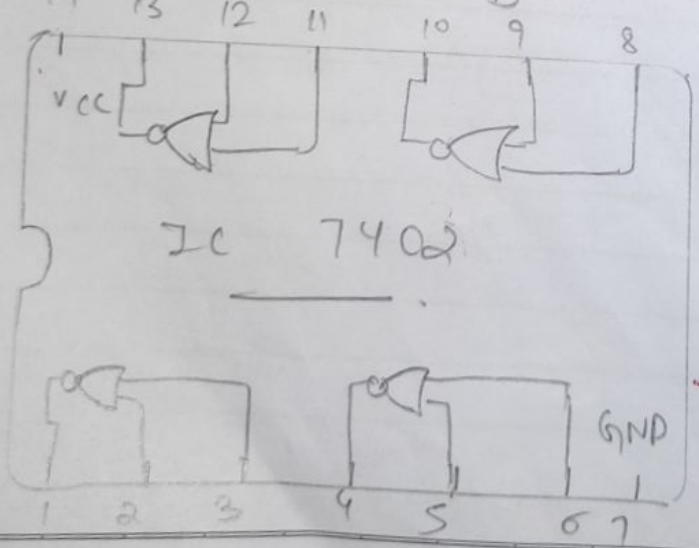




TRUTH TABLE

Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

- NOR gate



TRUTH TABLE

Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Date 23/8/18

Expt. No. 3 Page No. 7

EXPERIMENT - 3

* **Aim :-** study of universal gate and design of all gates using Universal gate.
* **Apparatus :-** Digital trainer kit, connecting wires, IC 7402 (NOR) and IC 7400 (NAND)

* **Theory :-**

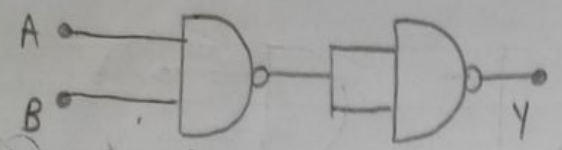
- **Basic Gates** - Among all the gates, AND, OR and NOT gate are called basic gates because these gates have basic operation.
- **Universal Gates** - NOR and NAND gates are known as Universal Gates because all the rest of six gates can be made by only NAND or only NOR gate.

→ **NOR gate -**

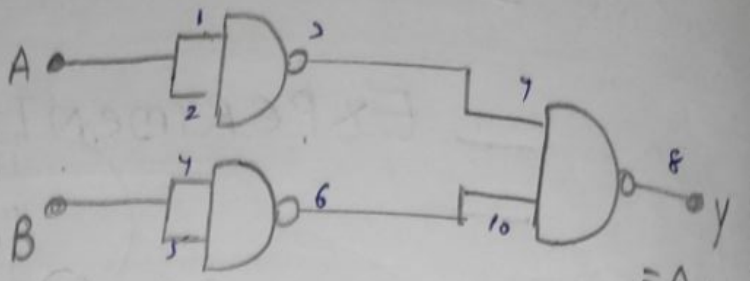
- It is a NOT-OR gate which is equal to an OR gate followed by a NOT gate.
- The output of all NOR gates are false if any of the i/p are true.
- $\overline{Y = A + B}$
- Integrated chip '7402' represents NOR gate.

Teacher's Signature : _____

→ Using NAND gate

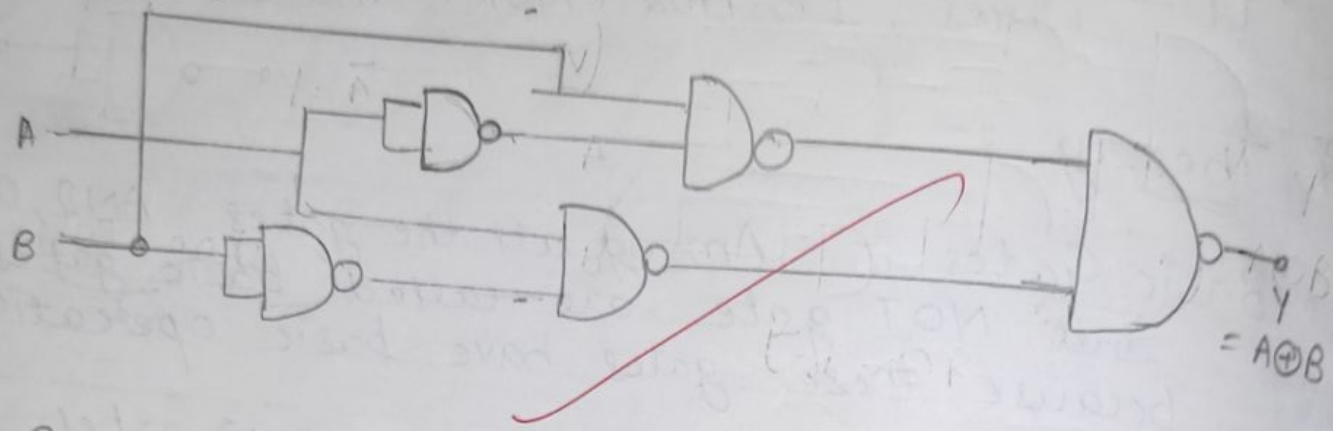
I) 

AND gate = A·B

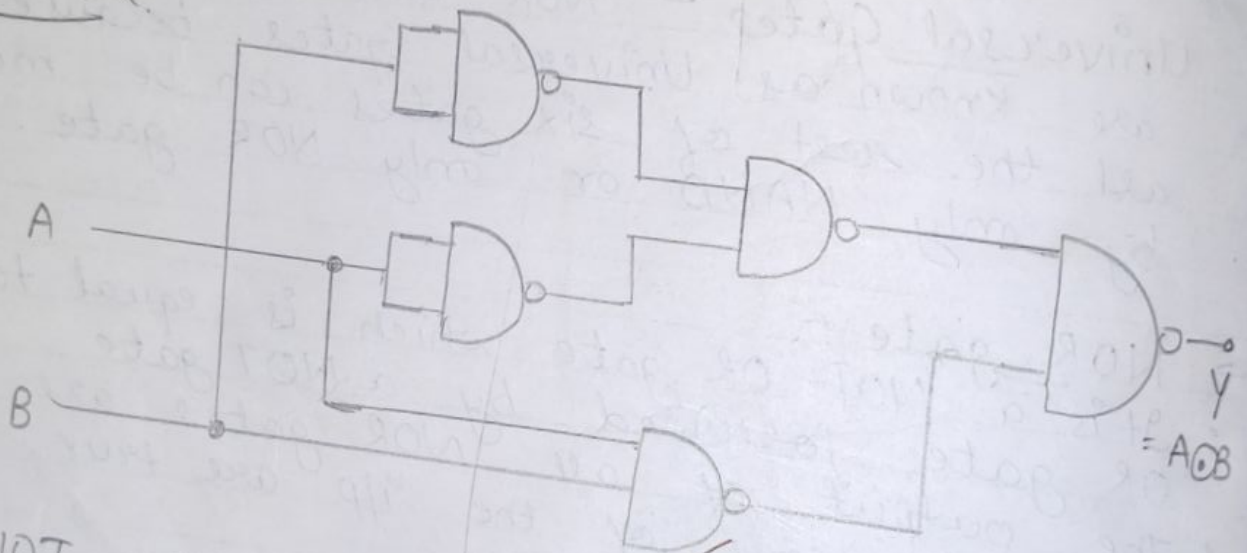
II) 

OR gate = A+B

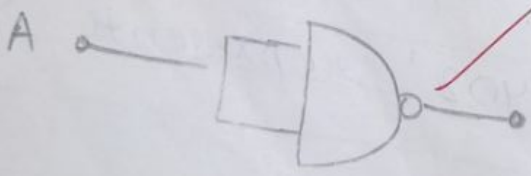
III) Ex-OR gate



IV) Ex-NOR



V) NOT gate

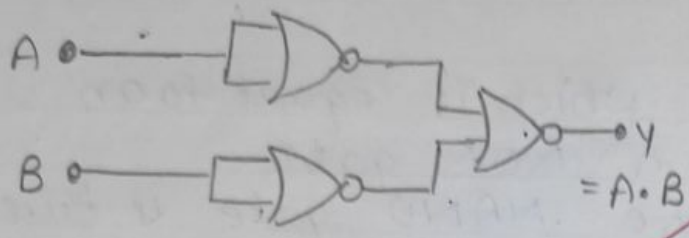


→ NAND gate -

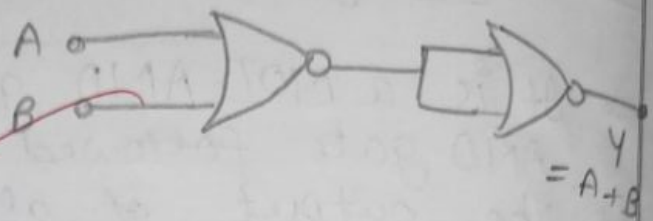
- It is a NOT-AND gate which is equal to an AND gate followed by a NOT gate.
- The output of all the NAND gate is true if any of the input are false.
- $Y = \overline{A \cdot B}$
- Integrated chip '7400' represents NAND gate.

→ Using NOR-gate

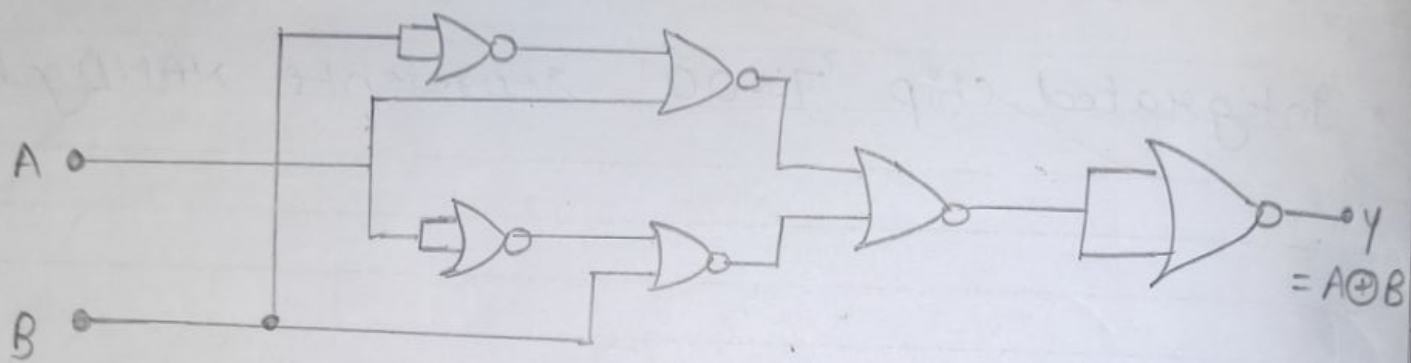
i) AND gate



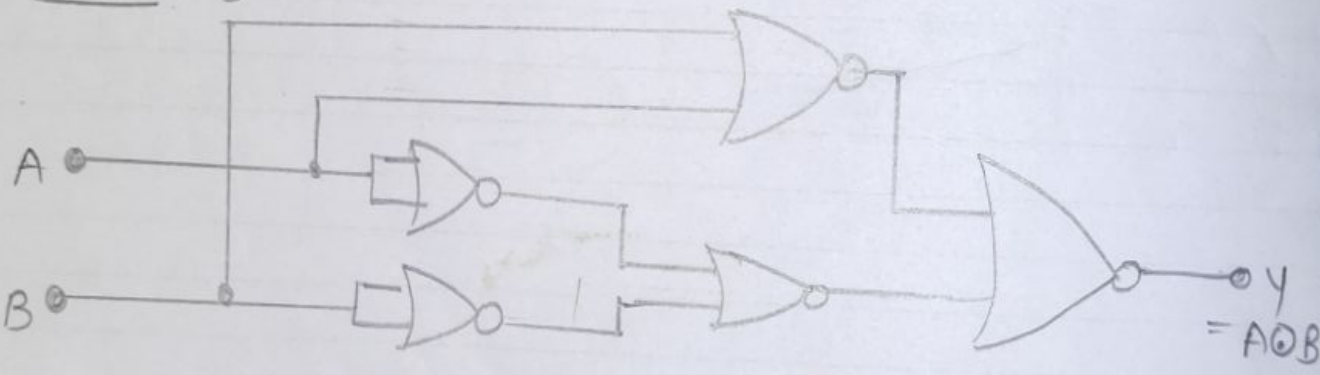
ii) OR gate



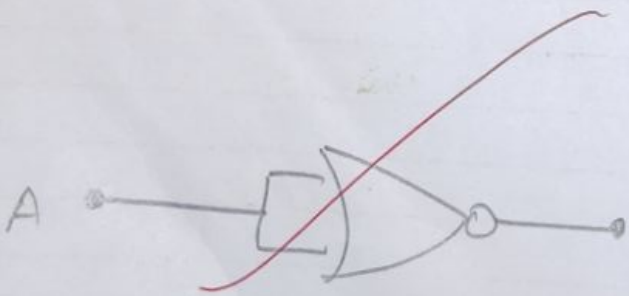
iii) Ex-OR gate



iv) Ex-NOR gate



v) NOT gate



* RESULT - We have studied universal gates

Date

Expt. No. Page No. 9

* RESULT –

→ We have studied universal gates and implemented other gates using only NAND or only NOR gate.

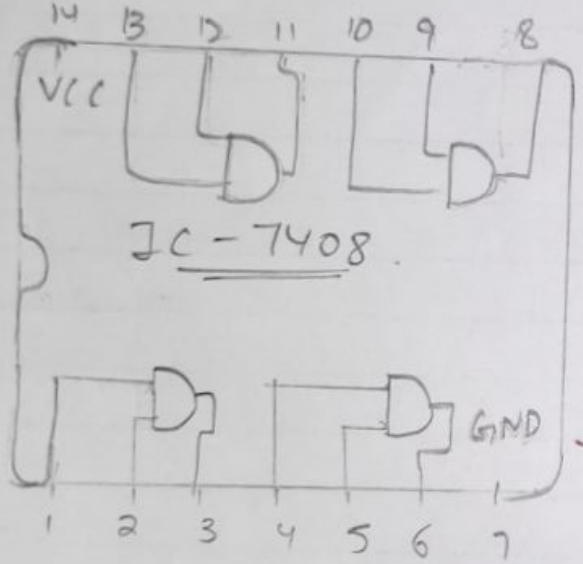
(2) 30/8/16

EXPERIMENT-4

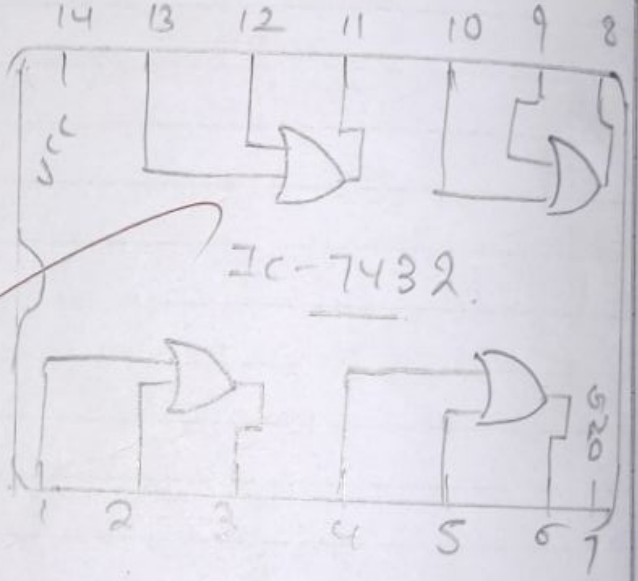
* **AIM** – To design and utilize a given function using k-map and verify its performance

* **APPARATUS** – Digital Trainer kit, cutter, plucker, ICs 7408 (AND), 7432 (OR), 7404 (NOT) and connecting wires

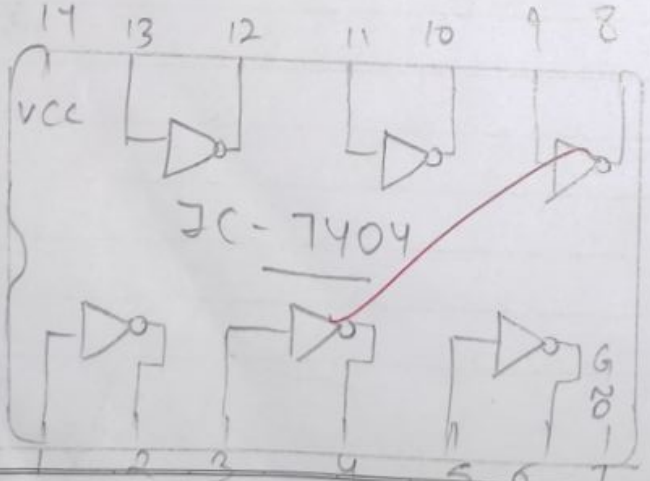
* **AND gate**



OR gate



NOT gate



Date 30/8/18

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EXPERIMENT-4

* Aim → To design and utilise a given function using K-map and verify its performance.

* Apparatus → Digital trainer kit, cutter, connecting wires, plucker, ICs AND(7408), OR(7432) and NOT(7404).

* Theory →

→ Boolean Algebra :-

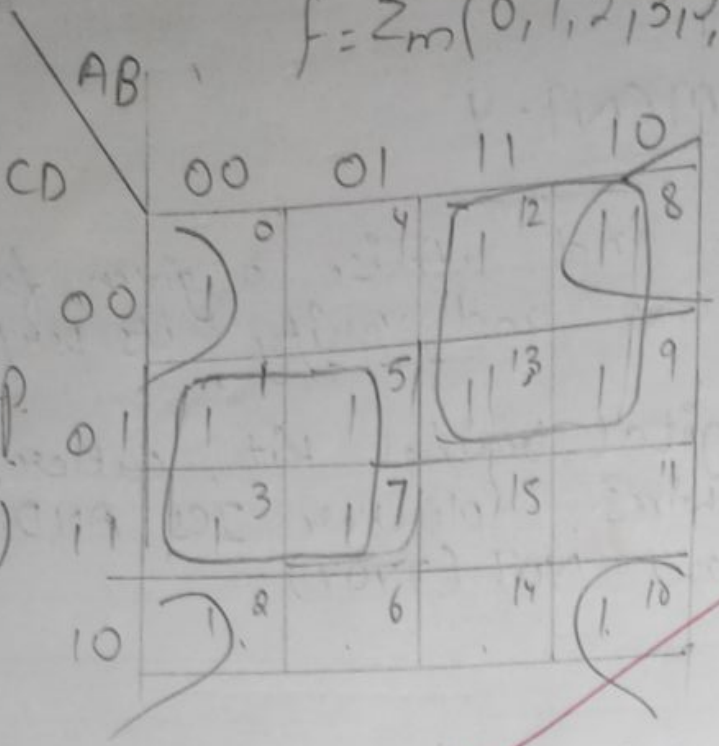
⇒ It differs from both ordinary algebra & the binary number system. In Boolean algebra, $A+A=A$ and $A \cdot A = A$ because variable A has only a logical value.

→ Karnaugh map (K-map)

⇒ In this, we put the truth table in a compact form by labelling the rows and columns of a map. This is extremely useful & extensively used in minimization of function of 3, 4, 5 or 6 variable. The rows & colums are assigned a binary code (gray code) such that two adjacent rows or column differ in only 1 bit. It consists of no. of squares & each square is called cell.

Teacher's Signature : _____

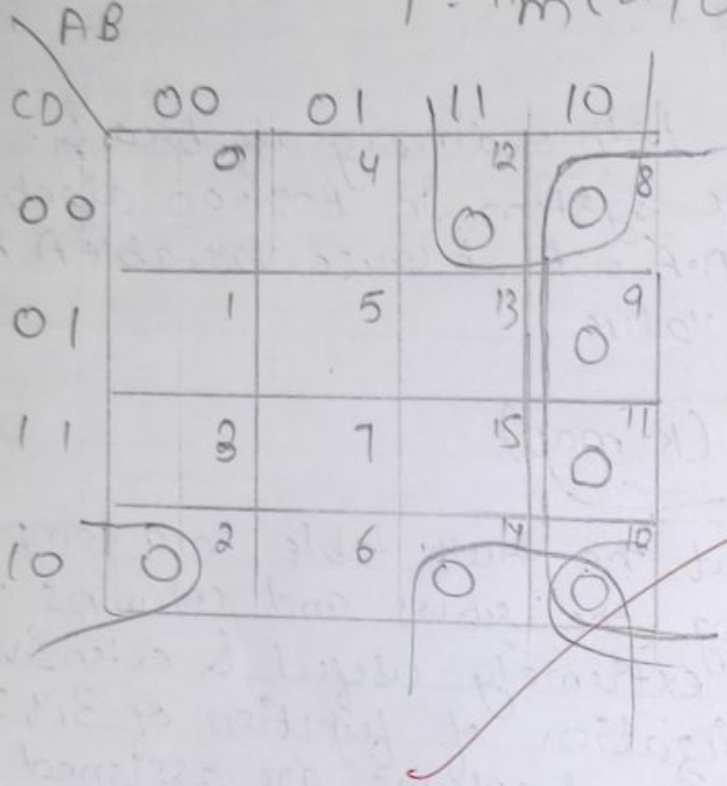
$f = \Sigma_m(0,1,2,3,5,7,8,9,10,12,13)$



K-Map (SOP)

$f = A\bar{C} + \bar{B}\bar{D} + \bar{A}D$

$f = \Pi_m(2,8,9,10,11,12,14)$



K-Map (POS)

$f = (\bar{A}+B)\cdot(\bar{A}+\bar{D})\cdot(B+C+D)$

Date

Expt. No. Page No. 11

* Boolean functions -

A function of 'n' Boolean variables denoted by $f(x_1, x_2 \dots x_n)$ is another variable of algebra and takes one of the two possible values 0 & 1.

1). Sum of- products (SOP) form - It is also called Disjunctive Normal Form (DNF).

Example 1 $f = \Sigma m \{0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13\}$.

⇒ By K-map, It reduces to

$$f = A\bar{C} + \bar{B}\bar{D} + \bar{A}D.$$

2) Product-of-Sum (POS) form - It is also called Conjunctive Normal form (CNF).

Example 2 $f = \Pi m \{2, 8, 9, 10, 11, 12, 14\}$.

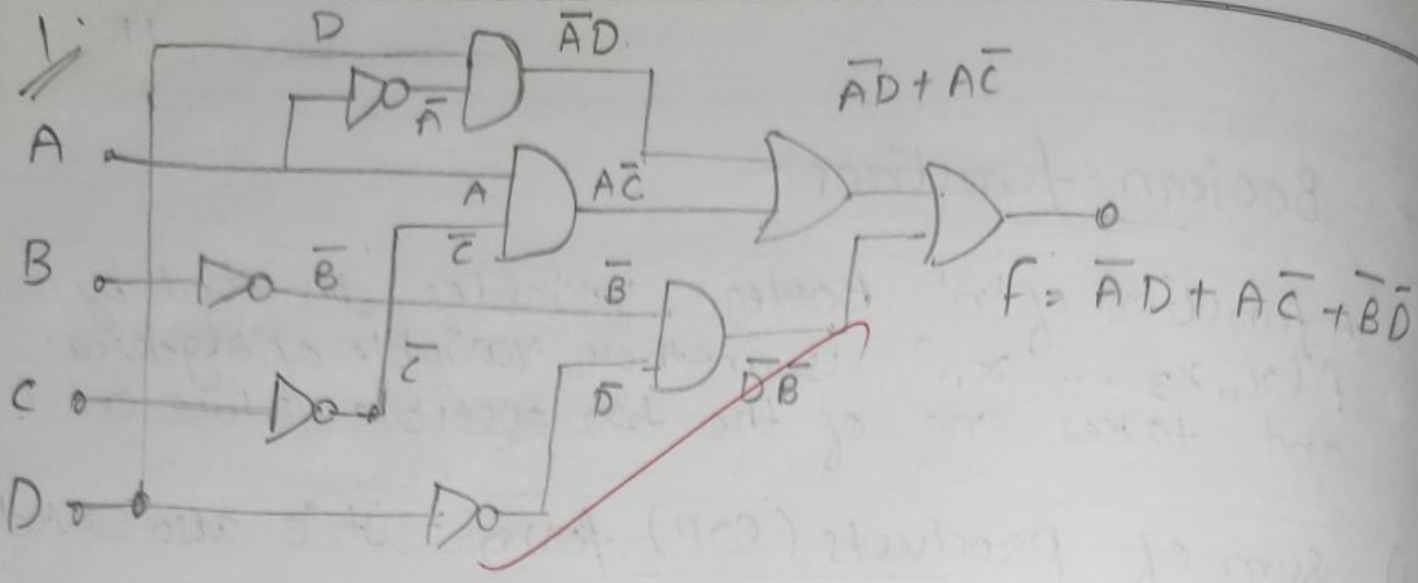
⇒ By K-map, it reduces to

$$f = (\bar{A} + B) \cdot (\bar{A} + D) \cdot (B + C + D).$$

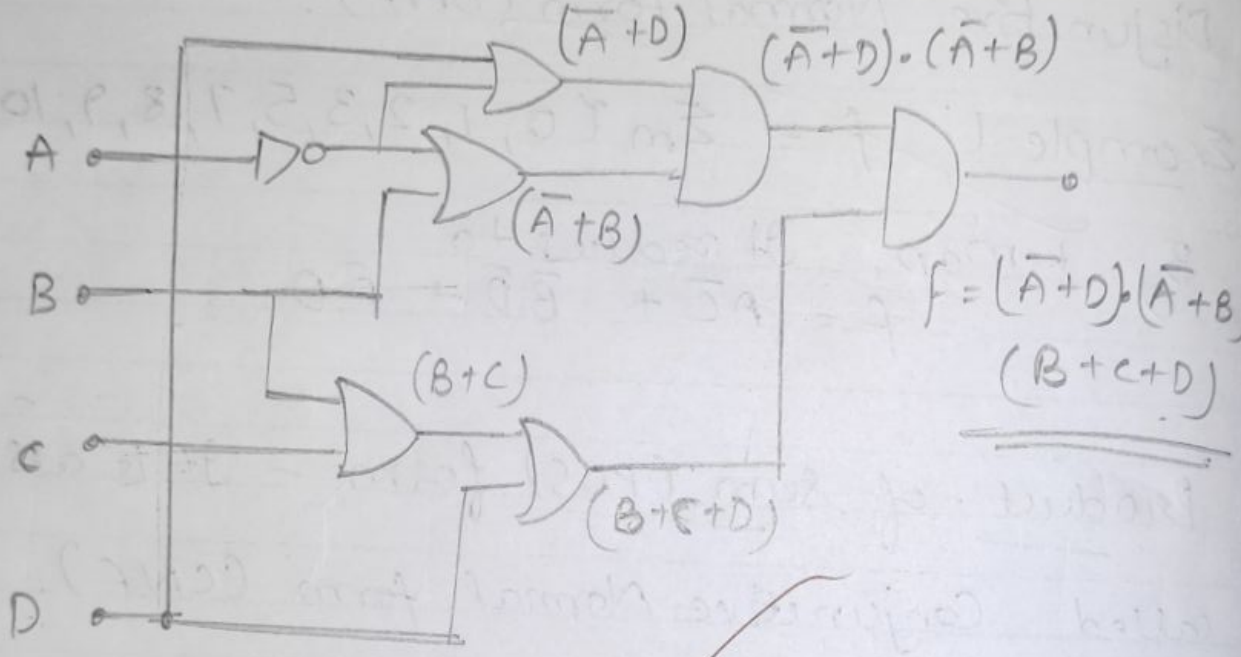
* RESULT - A function is designed & utilised using K-map & its performance is verified.

Teacher's Signature :

1.



2.



RESULT → A function is designed and utilized using K-map & its performance is verified

Date

Expt. No. Page No. 12

* RESULT →

→ A function is designed and utilized using K-Map. and its performance is verified.

(2) 13/9/18.

Teacher's Signature :

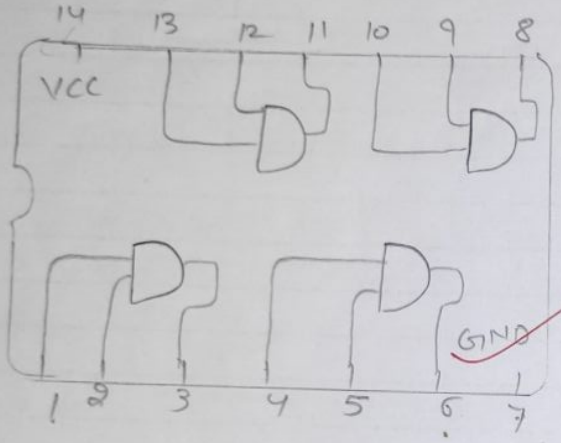
EXPERIMENT-5.

* **Aim** → To design a full adder and half adder circuit

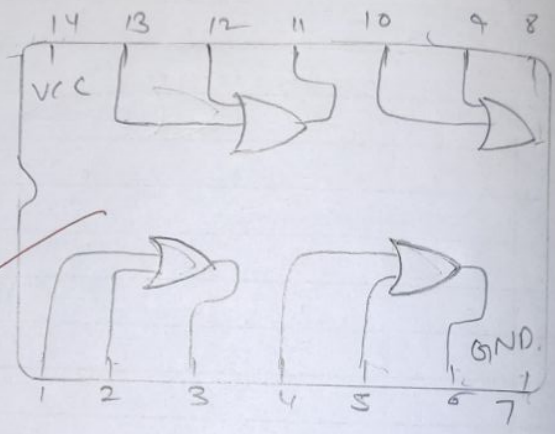
* **APPARATUS** → Digital trainer kit, cutter, connecting wires, plucker, ICs 7408 (AND), 7432 (OR), 7404 (NOT).

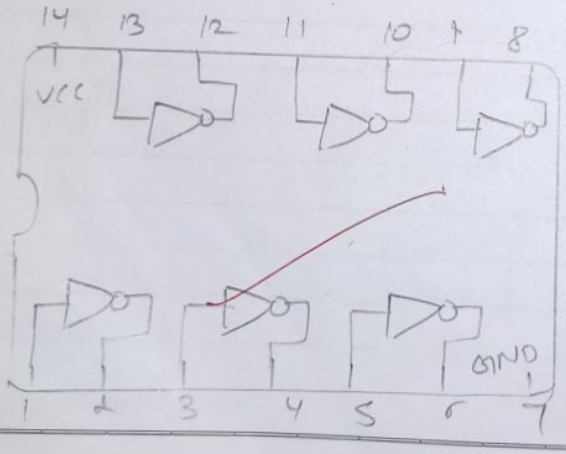
* **CIRCUIT** →

AND (7408).



OR (7432).





NOT (7404)

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EXPERIMENT-5

* Aim → To design a full adder and half adder circuit.

* APPARATUS → Digital trainer kit, cutter, connecting wires, plucker, ICs 7408 (AND), 7432 (OR), and 7404 (NOT).

* THEORY →

◦ Karnaugh map –

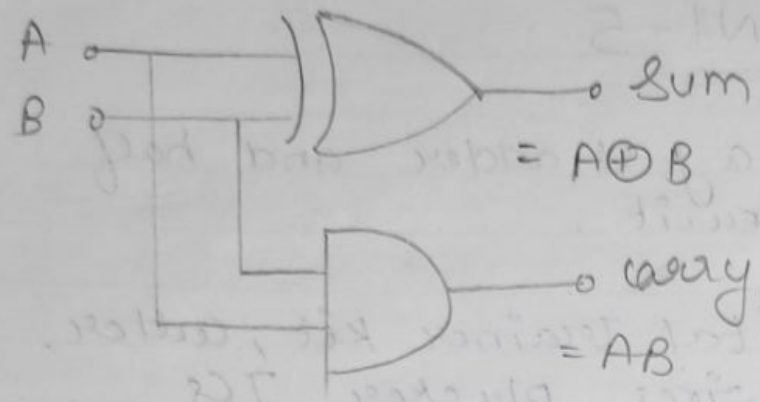
→ It is extremely useful & extensively used in minimisation of function of 3, 4, 5 or 6 variable.
→ The row or column are assigned a gray code such that two rows or column differ by one bit.
→ It consists of no. of squares & each square is called cell.

◦ Adder. →

→ An adder is a digital logic circuit in electronics that implements addition of numbers.
→ In many computers and processors, adders are used to calculate addresses, similar operations of ALU etc.

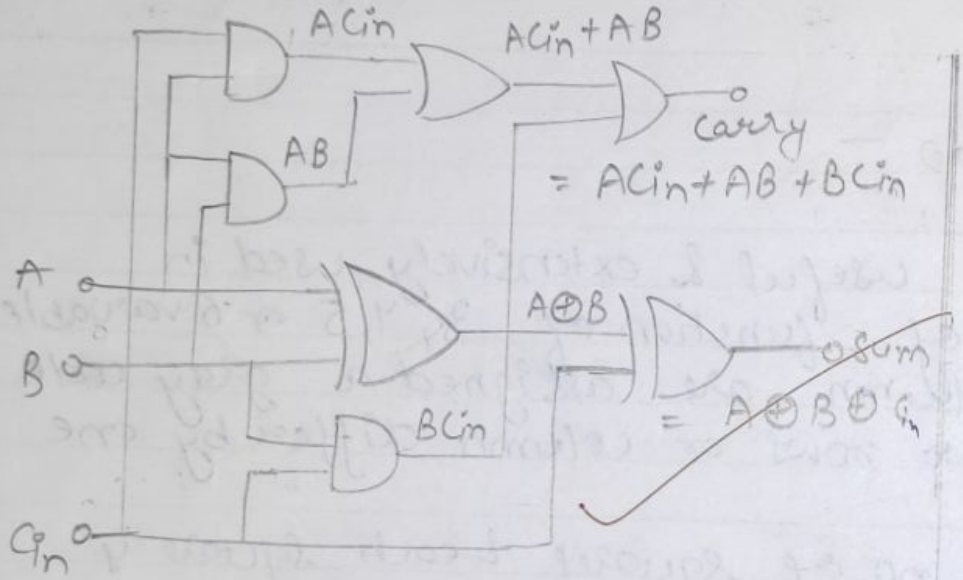
Teacher's Signature : _____

Half adder circuit



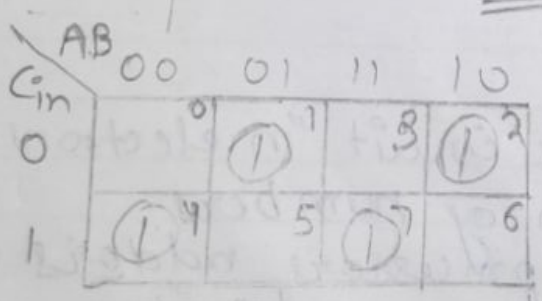
A	B	Sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full adder circuit

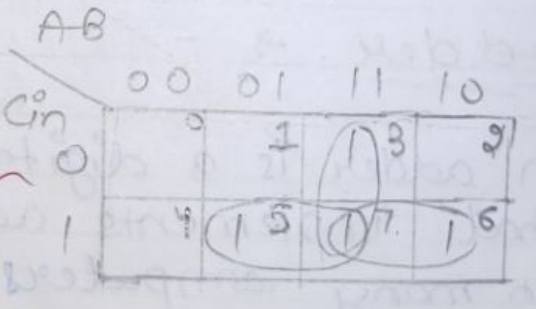


A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map



Sum = A⊕B⊕C



carry = AB + BC + CA

Adders are classified into two types :- half adder and full adder.

1) Half adder circuit.

→ It adds two binary digits called as augend & addend and produces two outputs as sum & carry. XOR is applied to both inputs to produce sum and AND to produce carry
Sum and carry are obtained by two inputs A & B
Sum = $A\bar{B} + B\bar{A} = A \oplus B$
Carry = AB

2) Full adder circuit

It adds 3 one bit number, where two can be referred as operands and one can be referred to as bit carried in. And produces 2-bit output and this can be referred to as output carry & sum. It has 3 inputs A, B and Cin. By K-Map :-
Sum = $\bar{A}\bar{B}C + AB\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C}$
$= \bar{A}(\bar{B}C + B\bar{C}) + A(BC + \bar{B}\bar{C})$
$= \bar{A}(B \oplus C) + A(\overline{B \oplus C}) = A \oplus B \oplus C$.
Carry = $AB + BC + CA$.

(2)

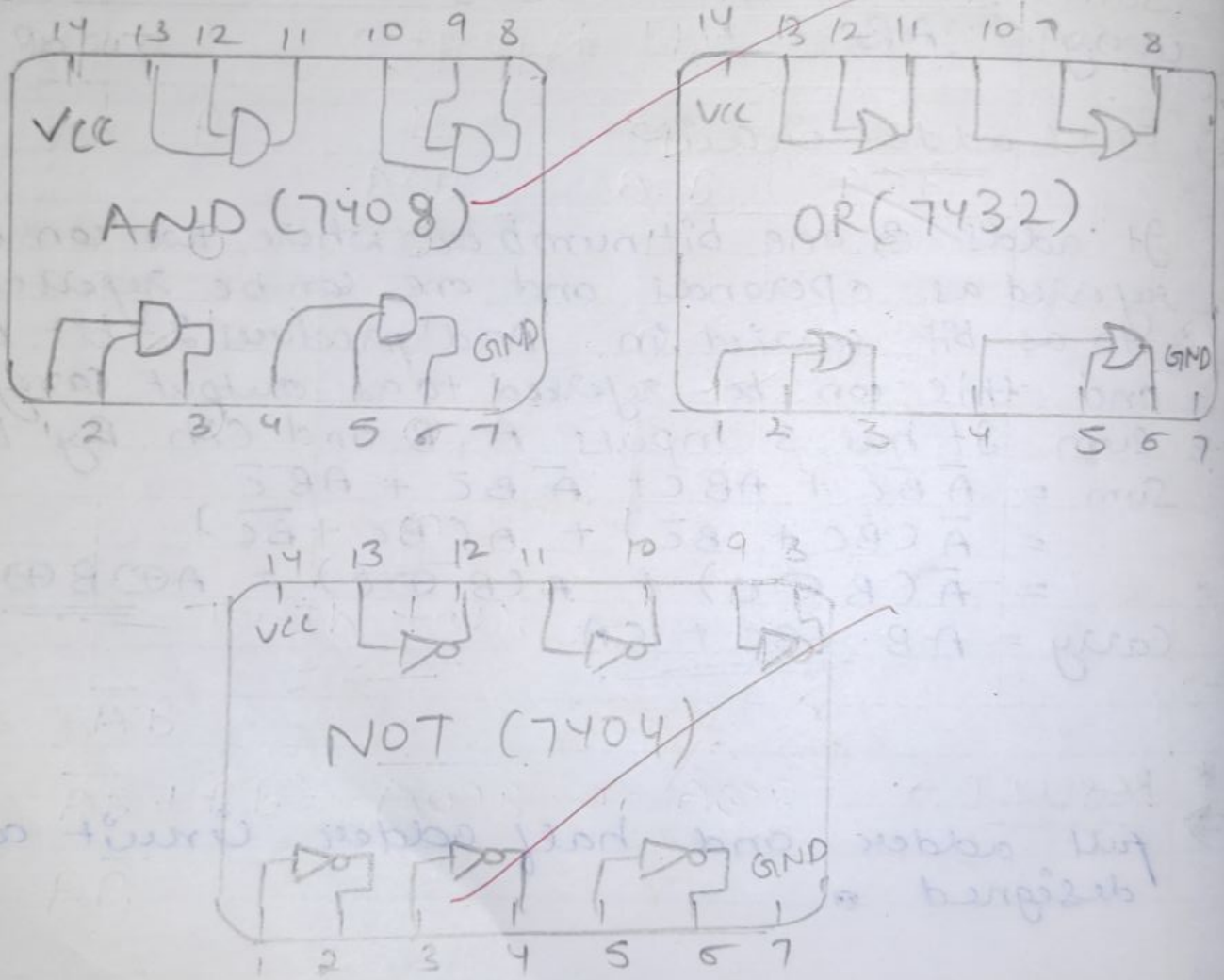
* RESULT →
Full adder and half adder circuit are designed.

Teacher's Signature :

EXPERIMENT - 6

* **Aim** - To design & verify 1-bit comparator
* **Apparatus** - Digital trainer kit, plucker, cutter, ICs - AND gate (7408), OR gate (7432), NOT gate (7404), connecting wires
* **CIRCUIT DIAGRAM :-**

ICs.



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EXPERIMENT-6

* **AIM** → To design and verify 1-bit comparator.

* **Apparatus** → Digital trainer kit, plucker, cutter, ICs :- AND gate (7408), OR gate (7432), NOT gate (7404), connecting wires.

* **Theory**

- **Comparator** - In digital system comparison of two numbers is an arithmetic operation that determines if one no. is equal to, greater than or less than the other no. So comparator is used for this purpose.

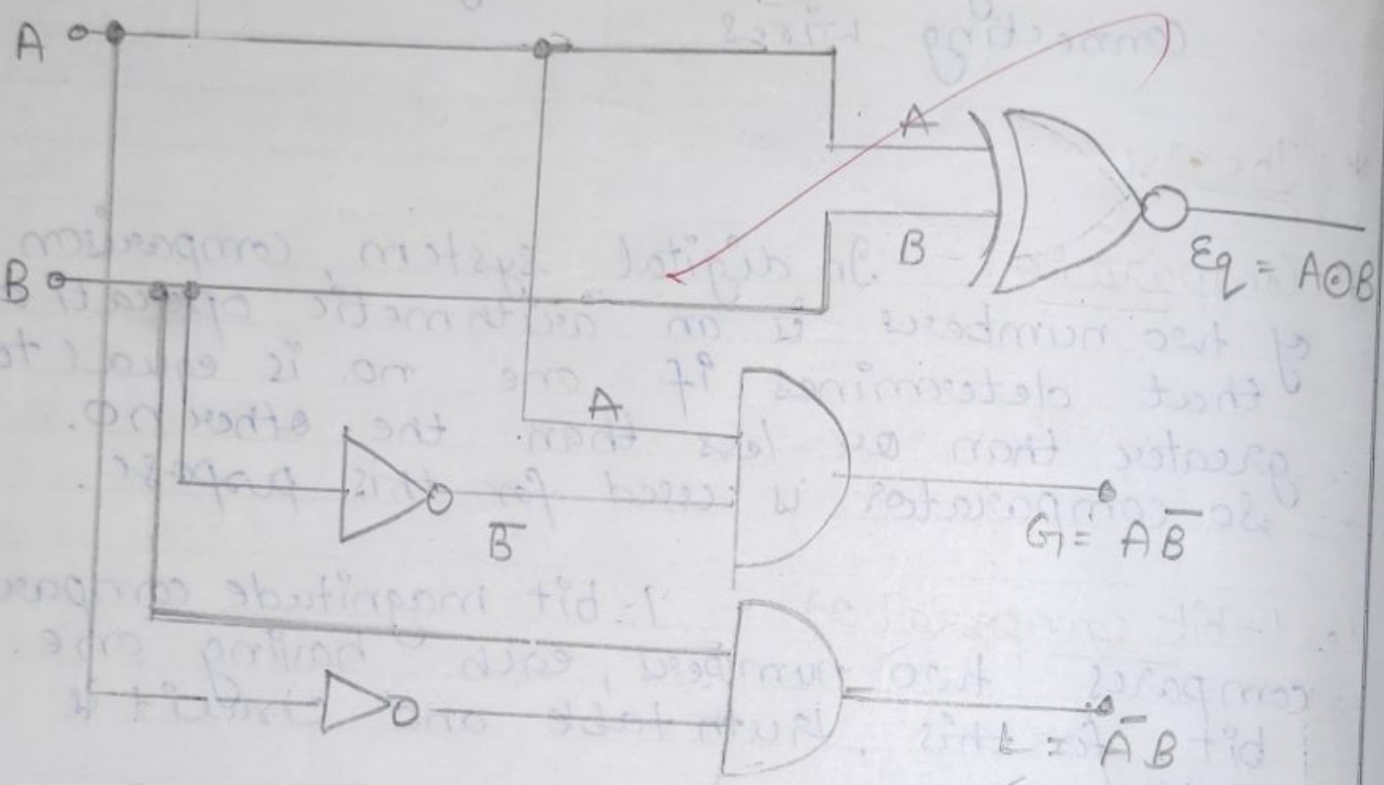
- **1-bit comparator** - 1-bit magnitude comparator compares two numbers, each having one bit. for this, truth table and circuit is shown.
Here expression for two input is (A & B) :-

$L = A < B = \bar{A}B$ = A is less than B
$Eq = A = B = \bar{A}\bar{B} + AB$ = A is equal to B = $A \odot B$.
$G = A > B = A\bar{B}$ = A is greater than B.

Teacher's Signature :

* CIRCUIT DIAGRAM & TRUTH TABLE :-

Input		Output		
A	B	L(A<B)	Eq(A=B)	G(A>B)
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0



* RESULT - One bit comparator is designed and verified successfully

- 2-bit comparator - 2 bit magnitude comparator compares two number each having two bits (A_1A_0 & B_1B_0). Expression is :-
for two signal of 2 bits, let A(A_1, A_0) & B(B_1, B_0).

$$A<B = \bar{A_1}B_1 + \bar{A_1}\bar{A_0}B_0 + \bar{A_0}B_1B_0$$

$$A=B = \bar{A_1}\bar{A_0}\bar{B_1}\bar{B_0} + \bar{A_1}A_0\bar{B_1}B_0 + A_1A_0B_1B_0 + A_1\bar{A_0}B_1\bar{B_0}.$$

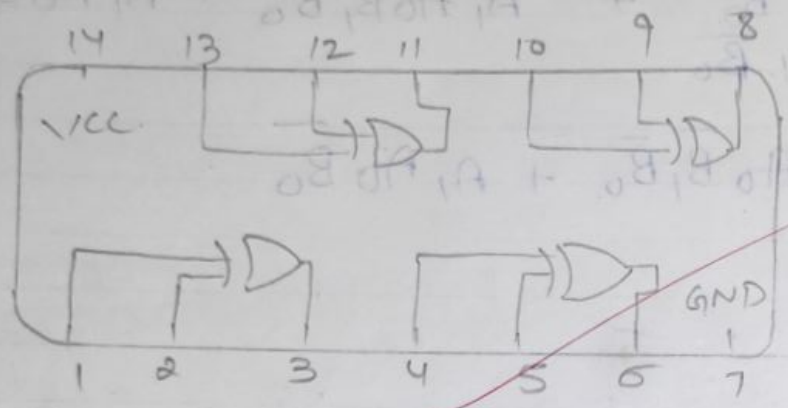
$$A>B = \bar{B_1}A_1 + A_0\bar{B_1}\bar{B_0} + A_1A_0\bar{B_0}$$

* RESULT :- one-bit comparator is designed and verified successfully.

(2) 27/9/18

EXPERIMENT-7

* **Aim →** To design a 4-bit even parity checker & verify them.
* **Apparatus →** Digital trainer kit, cutter, plucker, IC EXOR(7486), connecting wires.
* **CIRCUIT DIAGRAM:-**



EXOR (7486)

* **TRUTH TABLE →**

A	B	C	D	even parity bit
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Date

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EXPERIMENT-7

* Aim → To design a 4-bit even parity checker and varify them.

* Apparatus → Digital trainer kit, cutter plucker, IC - EXOR gate (7486) connecting wires

* Theory →

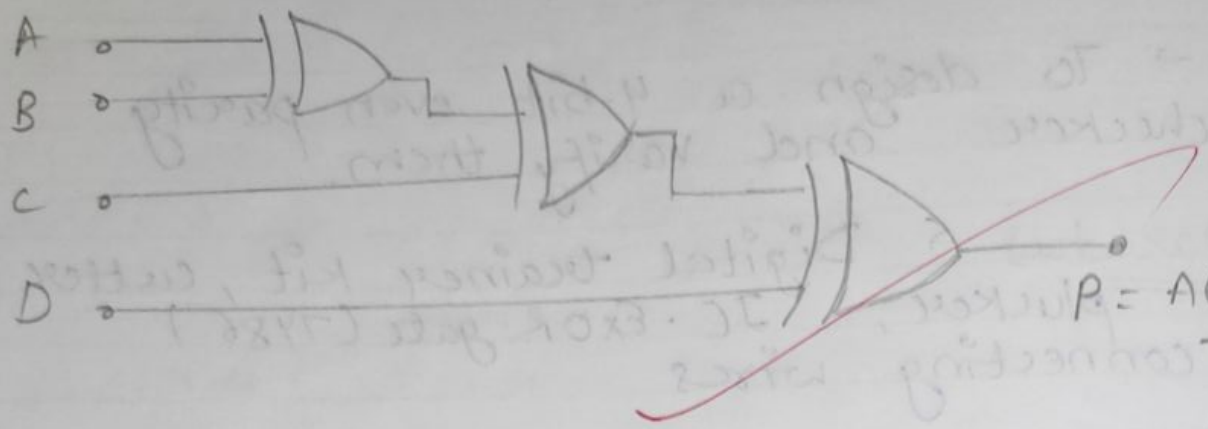
→ A parity bit or check bit is a bit added to a string of binary code to ensure that the total no. of 1-bits in the string is even or odd.

→ Even parity - for a given set of bits the occurences of bits whose value is 1. is counted. if count is odd, parity is 1. else 0.

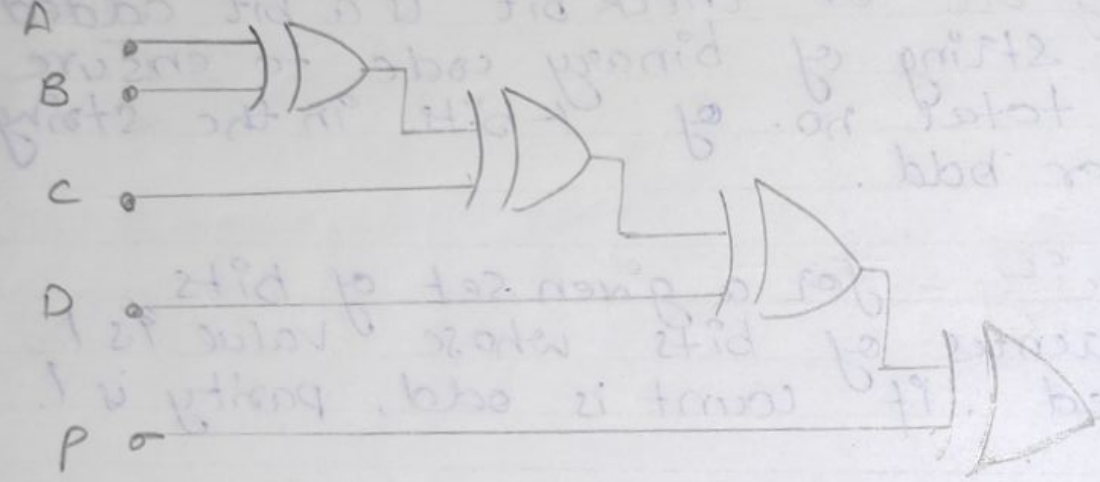
→ Even parity checker - In this at receiver side. if parity of transmitted string (including parity bit) is odd, then there is error in the transmitted string
It will not tell what the error is, hence called error detection method.

Teacher's Signature :

Parity bit (P) = A ⊕ B ⊕ C ⊕ D.



At receiver side, Y = A ⊕ B ⊕ C ⊕ D ⊕ P



If Y = 0, there is no error

If Y = 1, there is error while transmission

RESULT: A 4-bit even parity checker is designed & verified.

(d) 27/9/18

* RESULT - A 4 bit even parity checker is designed & verified.

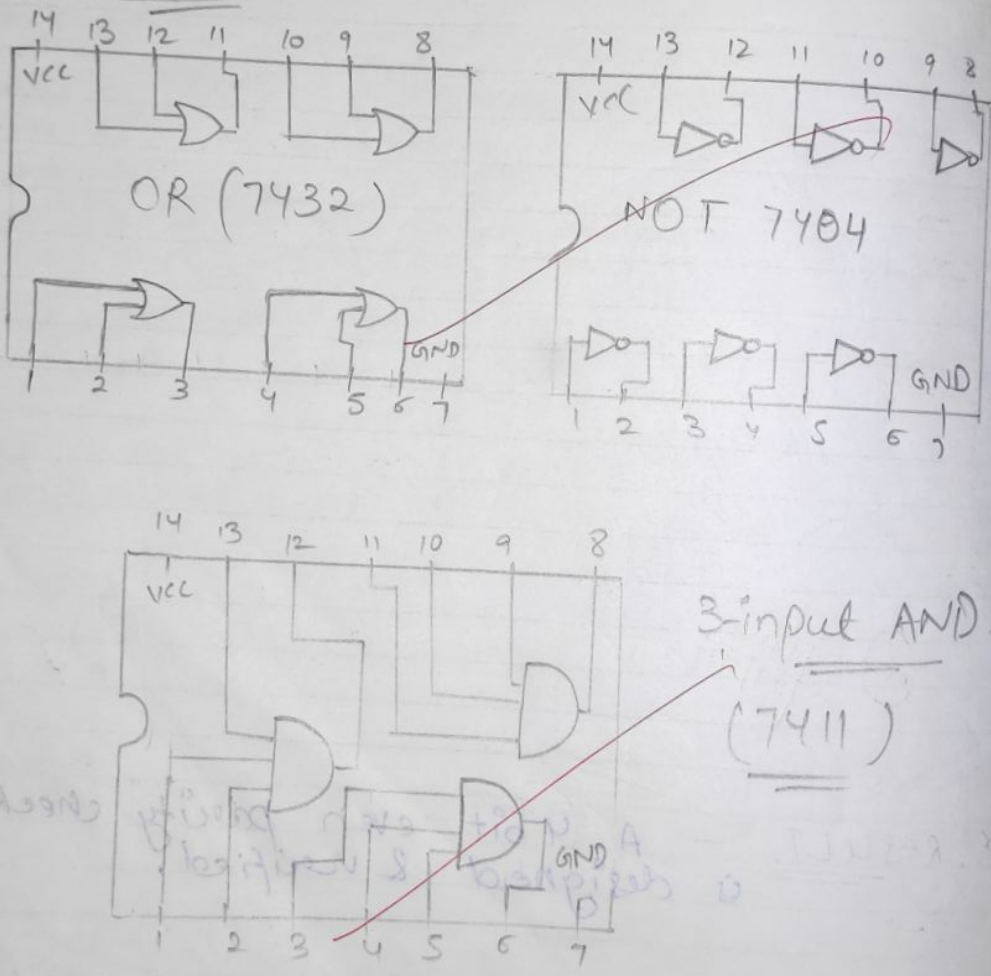
Teacher's Signature : _____

EXPERIMENT-8

* **AIM** - To design and verify 4:1 Multiplexer

* **Apparatus** - Digital trainer kit, plucker, cutter, IC's 4:1 Mux (74153), OR gate (7432), NOT gate (7404), 3-input AND gate (7411), connecting wires

* **CIRCUIT DIAGRAM** -



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EXPERIMENT - 8

* Aim → To design and verify 4:1 Multiplexer

* Apparatus → Digital trainer Kit, plucker, cutter IC's - 4:1 MUX (74153), OR gate (7432), NOT gate (7404), 3-input AND gate (7411), connecting wires.

* THEORY →

• Multiplexer - In electronics, a multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line.

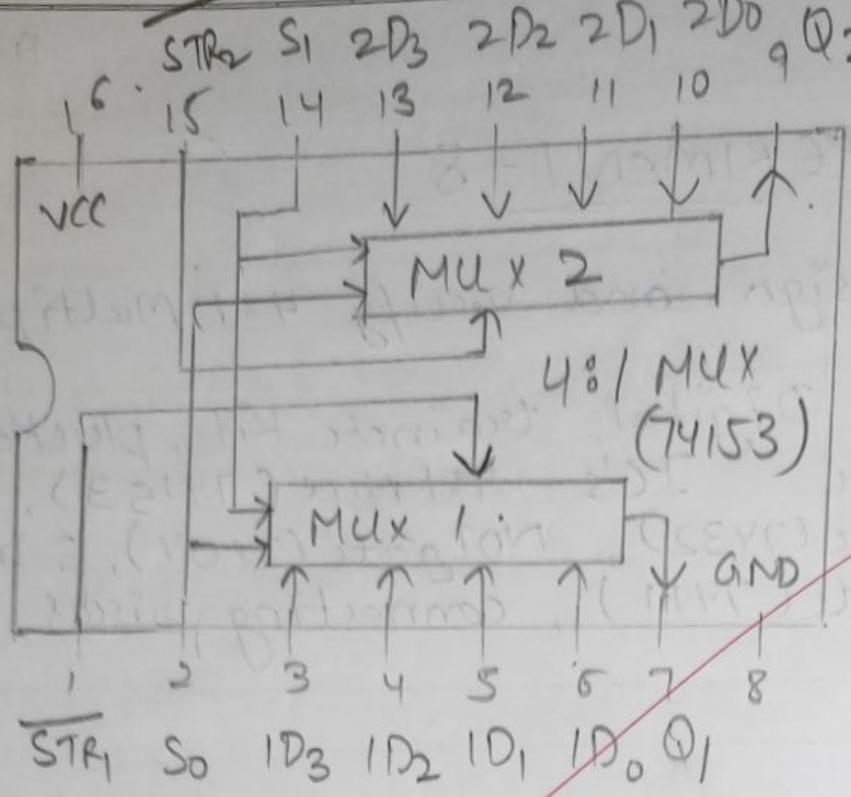
→ A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output.

→ It is also called a data selector.

→ It can also be used to implement Boolean functions of multiple variable.

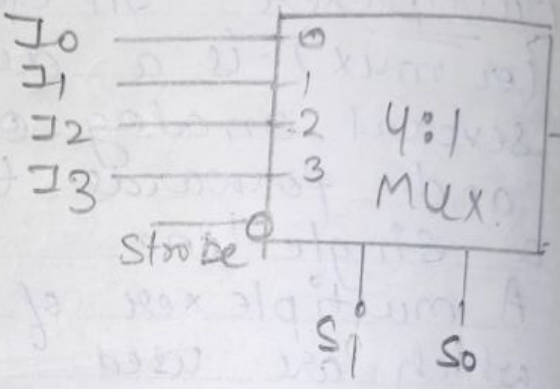
• 4:1 Multiplexer - It consists four data input lines as D_0 to D_3, two select lines as S_0 & S_1 and a single output line Y. The particular input combination on select lines select one of input (D_0 to D_3) to output.

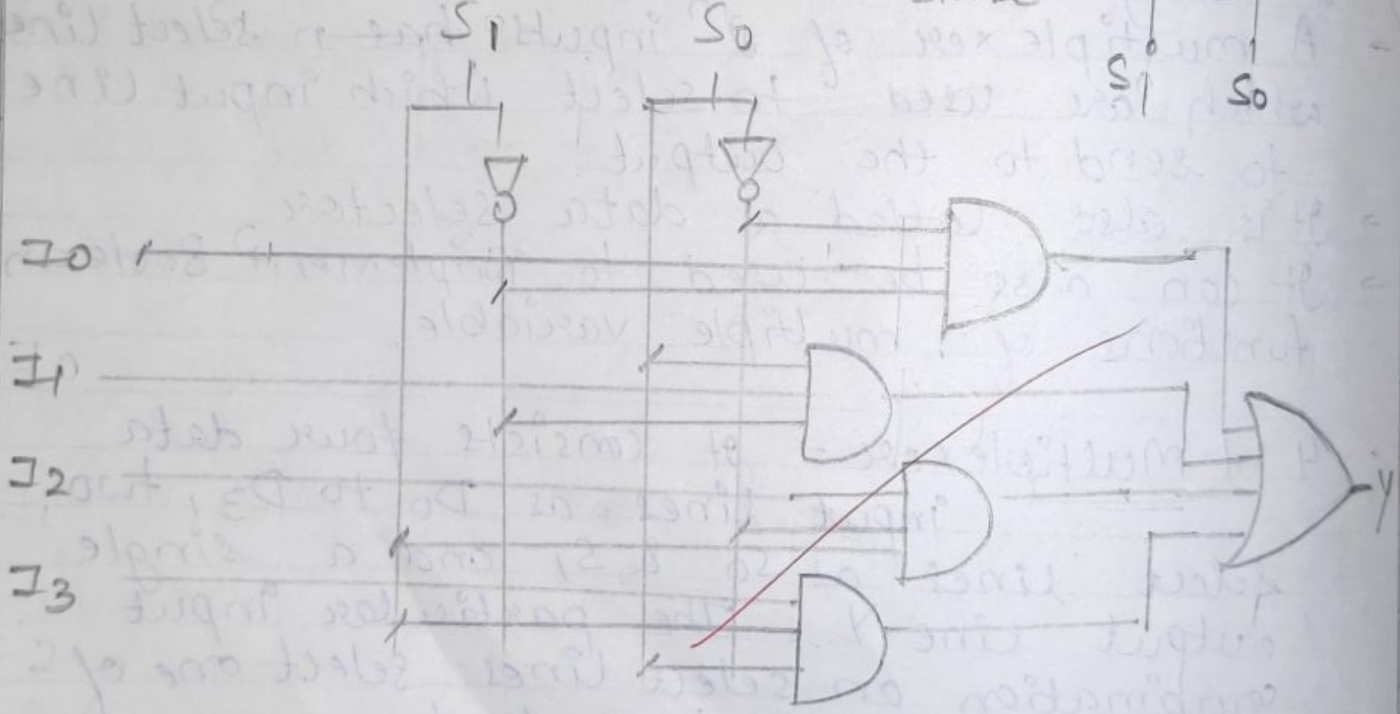
Teacher's Signature : _____



Input			O/P
$\overline{STR}$	S_1	S_0	Q
H	x	x	L
L	L	L	D_0
L	L	H	D_1
L	H	L	D_2
L	H	H	D_3

$$Y = \overline{S_1}\,\overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$





RESULT - 4:1 MUX is designed & verified

→ A 4:1 Mux can be implemented by using basic logic gates. figure shows the logic & circuit of MUX 4:1 which is implemented by four 3-inputs AND gates, two 1-input NOT gates, and One 4-input OR gate.

* RESULT :- A 4:1 MUX is designed and verified experimentally.

(2) 27/6/18

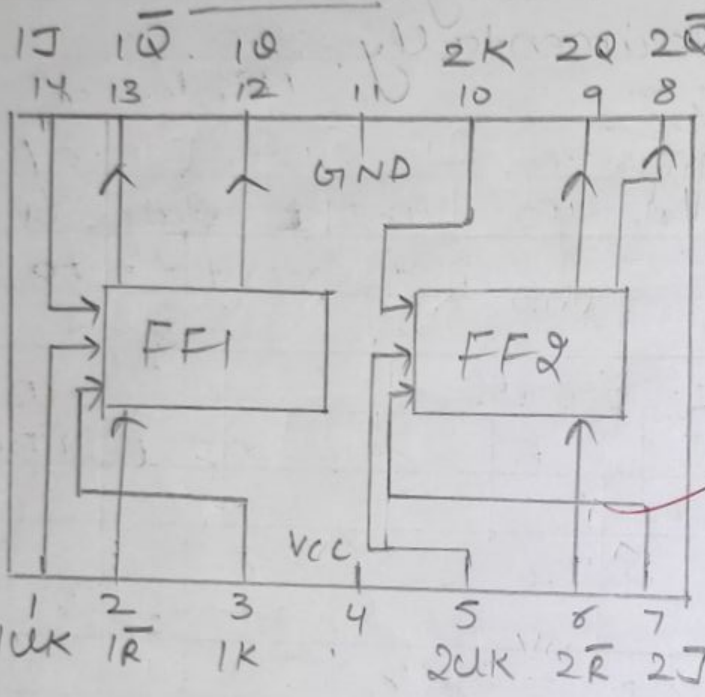
Teacher's Signature :

EXPERIMENT-9

* **Aim** → To verify truth table of JK, T and D flip flop.

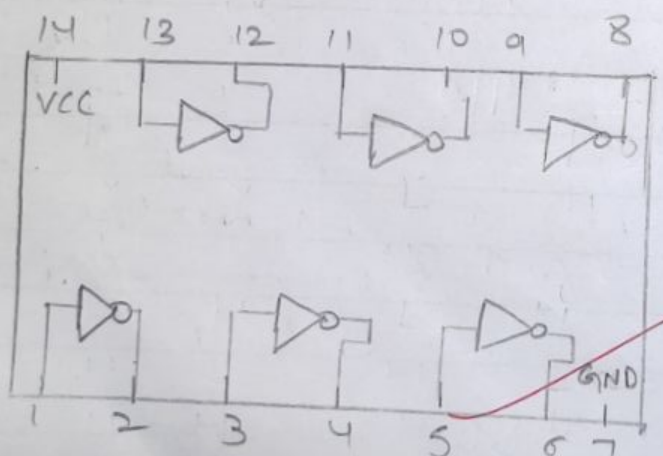
* **Apparatus** → Digital trainee kit, cutter plucker, IC 7473 (JK flipflop) & connecting wires, IC, 7404 (NOT)

* **CIRCUIT Diagram** →



IC 7473
JK flipflop

I/P				O/P	
$\bar{R}$	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	D	L	L	No change	
H	↑	L	H	L	H
H	↑	H	L	H	L
H	↑	H	H	Toggle	



IC 7404
(NOT gate)

EXPERIMENT-9

* **Aim** → To verify truth table of JK, T and D flip flop.

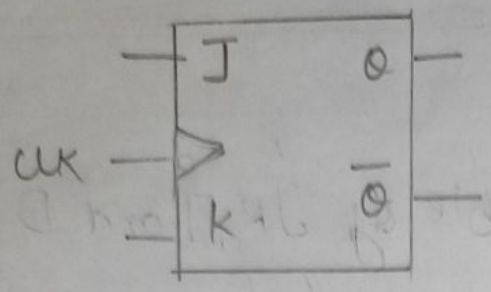
* **Apparatus** → Digital trainer kit, plucker cutter, IC 7473 (JK flip flop), 7404 (NOT) and connecting wires.

* **Theory** →

* **flip flop** - It is the most important memory element made of logic gates.
A flip flop known as bistable multivibrator has 2 stable states. Its state can be changed by applying proper triggering signal. It is also called binary or one-bit memory.

* J-K flip flop - It is very versatile & also the most widely used.
  - When J=0 & K=0, no change of state takes.
  - J=0 & K=1, flipflop resets at +ve going edge of clock pulse.
  - J=1 and K=0, flipflop sets at positive going edge of clock pulse.
  - J=1 & K=1, flipflop toggles.

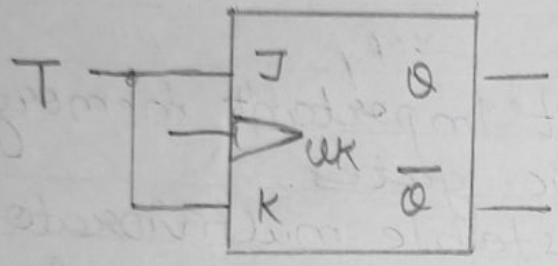
Teacher's Signature : _____



C = 0, No change.

C	J	K	Q_n	Q_{n+1}	State
↑	0	0	0	0	
↑	0	0	1	1	No change
↑	0	1	0	0	
↑	0	1	1	0	Reset
↑	1	0	0	1	
↑	1	0	1	1	Set
↑	1	1	0	1	
↑	1	1	1	0	Toggle

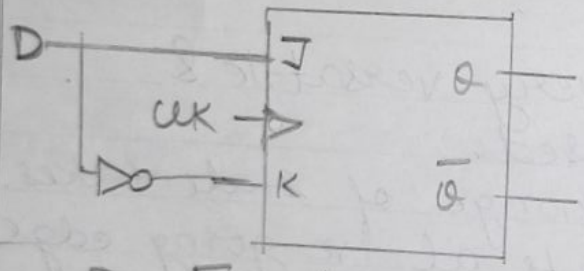
JK flip flop



T FF from JK FF

C	T	Q_n	Q_{n+1}	State
↑	0	0	0	
↑	0	1	1	No change
↑	1	0	1	
↑	1	1	0	Toggle

C = 0 No change.



D FF from JK FF

C	D	Q_n	Q_{n+1}	State
↑	0	0	0	Reset
↑	0	1	0	
↑	1	0	1	
↑	1	1	1	set

C = 0 No change

RESULT :- The truth table of JK, T & D flipflop are studied and verified.

* T flip flop - It has a single control i/p, labelled T for toggle. When T is high, flip flop toggles on every new clock pulse & when T is Low, flip flop remains in previous state.

* D- flip flop - It has only one i/p terminal It may be obtained by putting inverter between J & K terminals.

(2)

* RESULT - The truth table of JK, T and D flip flop are verified.

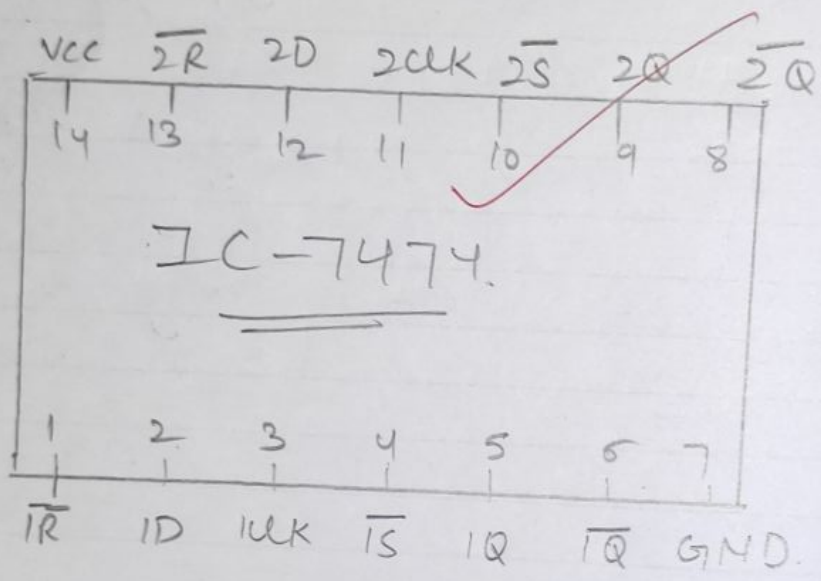
Teacher's Signature :

EXPERIMENT-10

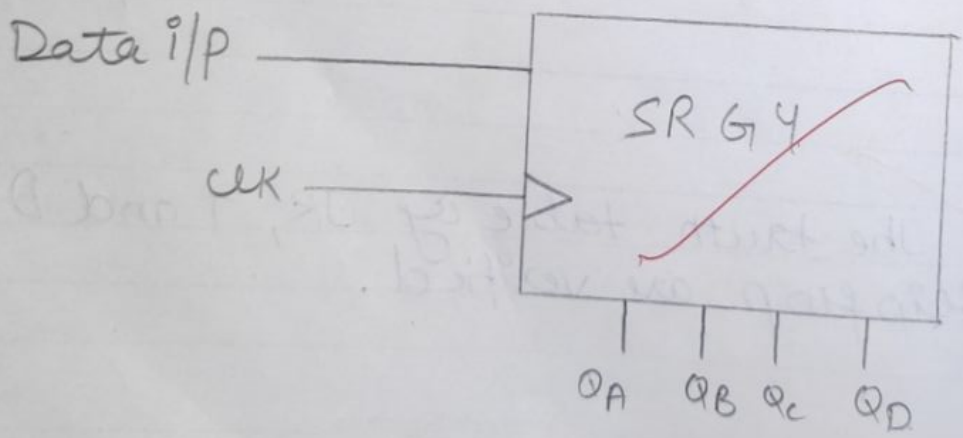
* **Aim-** To design a 4 bit shift register & verify its working.

* **APPARATUS →** Digital trainer kit, plucker, IC-7474 (D flipflop) and connecting wires.

* **CIRCUIT DIAGRAM**



D flip flop



Logic Symbol of SIPO Shift register

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EXP:→10

* **Aim** → To design a 4 bit shift register and verify its working.

* **APPARATUS** → Digital trainer kit, plucker, IC - 7474 (D flip flop) & connecting wires.

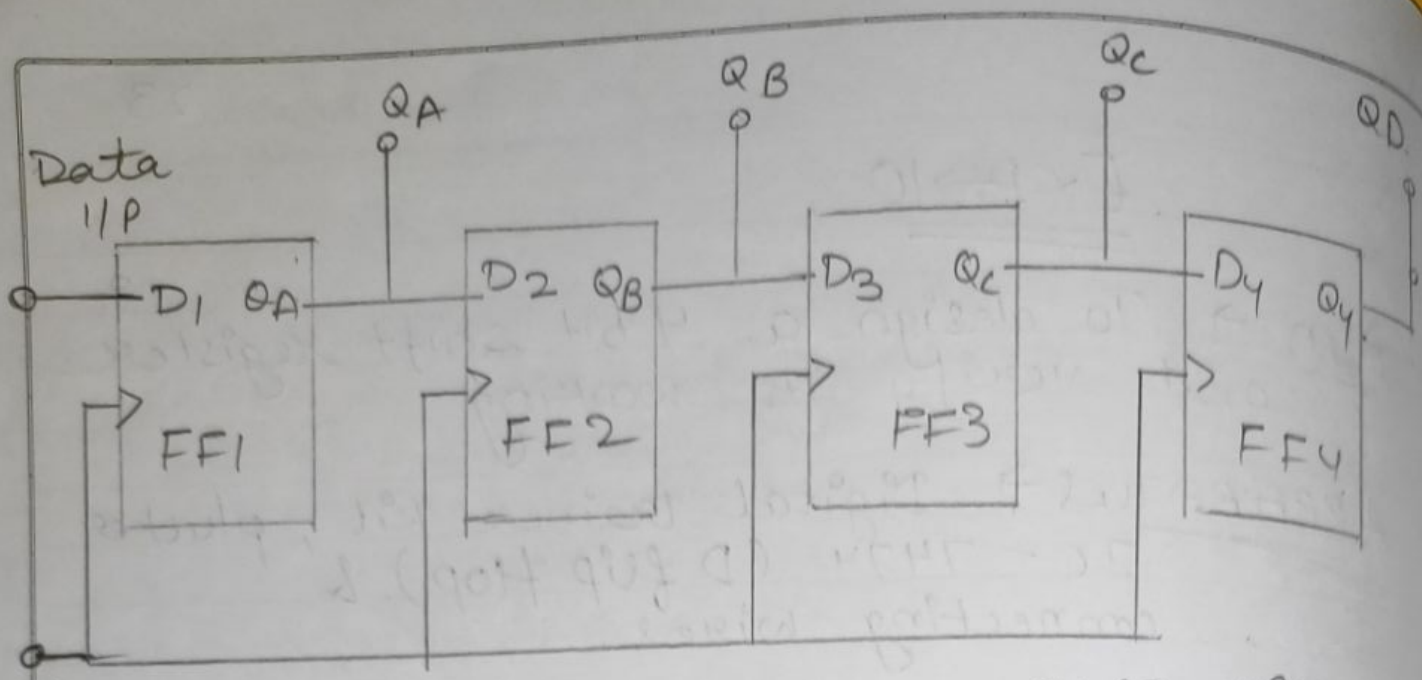
* **THEORY** →

→ **Register** - When more than one bits of data are to store, a no. of FFs are used. A register is a set of FFs used to store binary data.
The storage capacity of a register means no of bits (1s & 0s) of digital data it can retain.

→ **Serial in parallel out shift register**

- A number of FFs connected together s.t. data may be shifted into & shifted out of them is called a shift register.
- In Serial in parallel out shift register, the data bits are entered into the register serially, but the data stored in the register is shifted out in parallel form.

Teacher's Signature : _____



Logical Diagram of SIPO shift register

for eg. Data input is 1011, then at each clock pulse each input bit flows to next flip flop, and after 4 clock pulses, o/p will be.

	Q_D	Q_C	Q_B	Q_A
O/P =	1	0	1	1

* RESULT - A 4 bit shift register (SIPO) is designed and verified successfully

once the data bits are stored each bit appears on its resp. o/p line & all bits are available simultaneously.

(2)

* RESULT - A 4 bit SIPO shift register is designed & verified successfully.

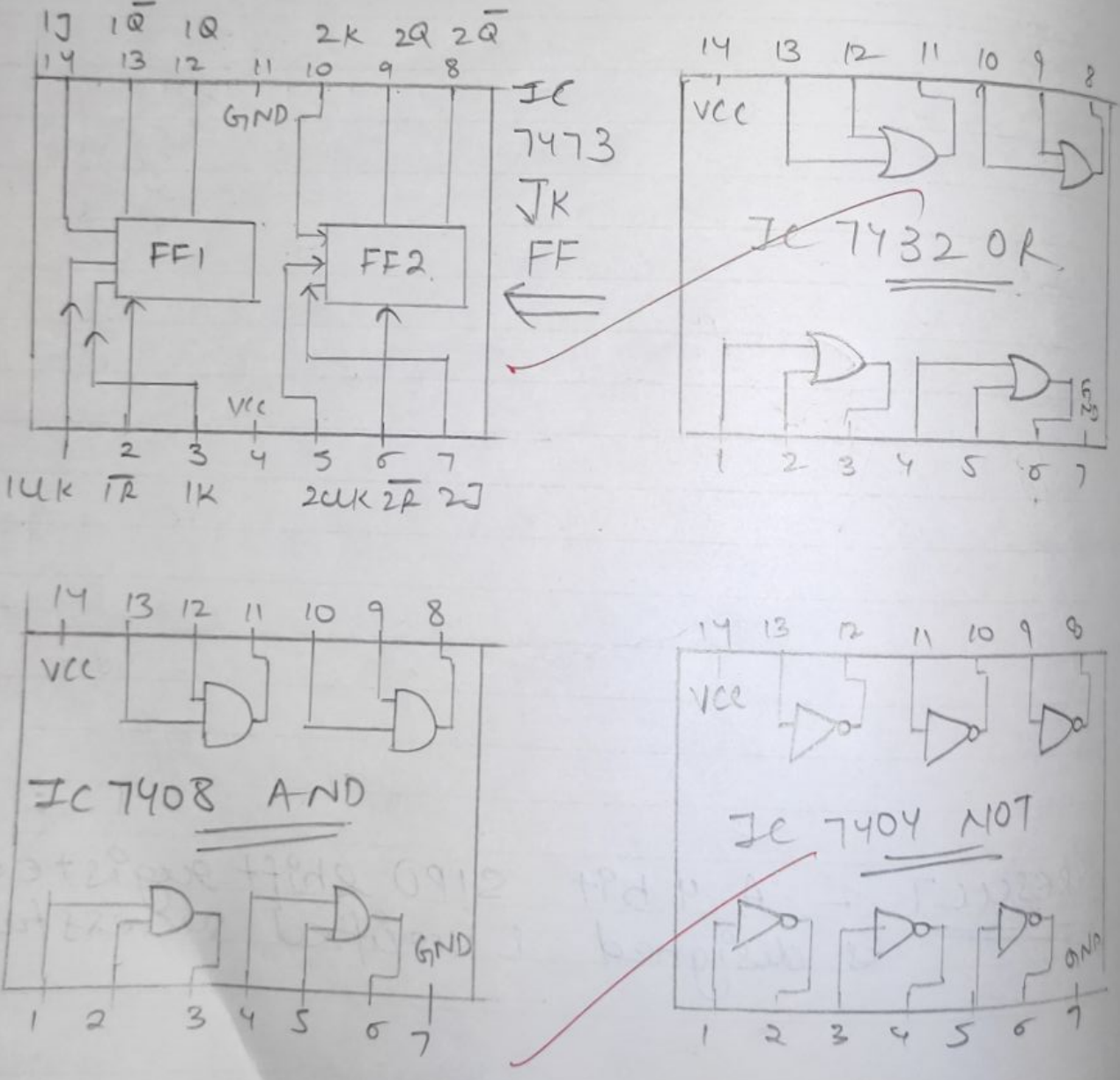
Teacher's Signature : _____

EXPERIMENT-11

* **Aim** → To design a 3 bit Asynchronous & synchronous counter

* **APPARATUS** → Digital trainer kit, plucker ICs 7473 (JK FF), 7408 (AND) 7404 (NOT), 7432 (OR) and connecting wires.

* **CIRCUIT DIAGRAM**



EXPERIMENT-11

* **Aim** → To design a 3-bit Asynchronous & Synchronous counter.

* **APPARATUS** → Digital trainer kit, plucker ICs 7473 (JK flip flop), 7408 (AND gate), 7432 (OR gate), 7404 (NOT gate), and connecting wires.

* **THEORY**

→ **COUNTER** – A digital counter is a set of flip flops whose states can change in response to pulse applied at the input to the counter

→ **ASYNCHRONOUS COUNTER** – Also called as Ripple counter or serial or series counter, it is simplest type of counter, easiest to design & requires the least amount of hardware.

→ **SYNCHRONOUS COUNTER** – They are the counters in which all the FFs triggered simultaneously by the clock-input pulse. They are thus faster than

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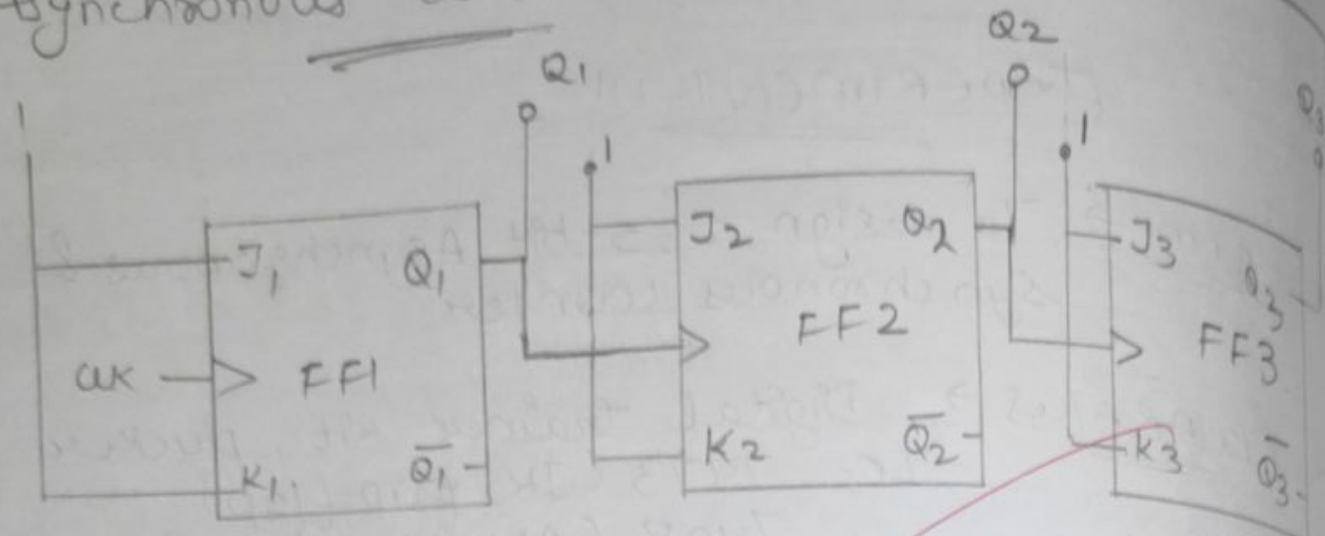
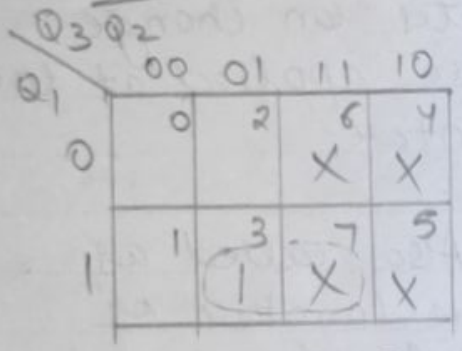
* Asynchronous counter



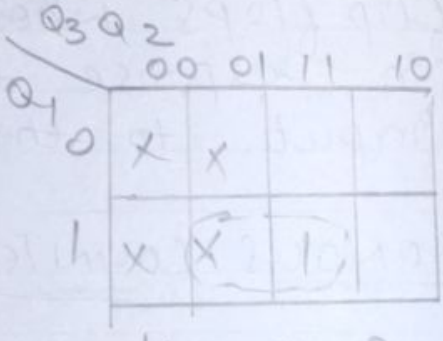
A 3-bit UP Asynchronous Counter

* SYNCHRONOUS COUNTER -

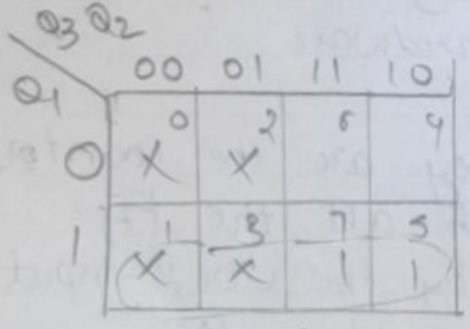
K-MAP for A 3bit Synchronous UP counter



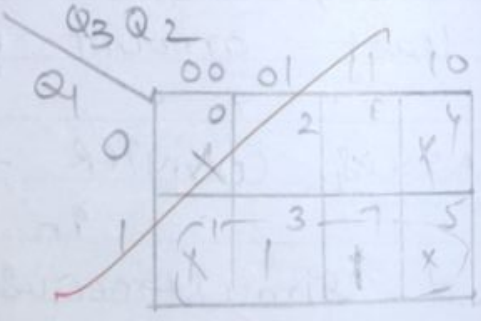
$J_3 = Q_2 Q_1$



$K_3 = Q_2 Q_1$



$J_2 = Q_1$



$K_2 = Q_1$

asynchronous counter, because propagation delay is involved less.
But they are complex to design.

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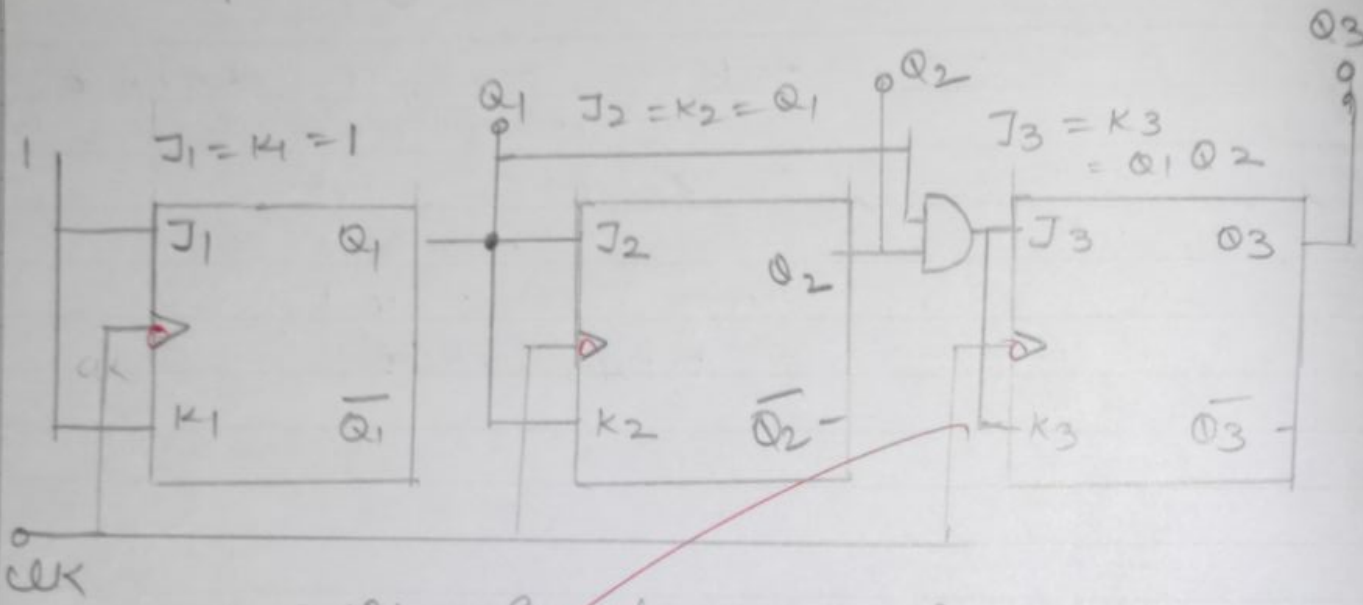
Q_1 \ Q_3Q_2	00	01	11	10
0	1 (0)	1 (2)	1 (6)	1 (4)
1	x (1)	x (3)	x (7)	x (5)

$J_1 = 1$

Q_1 \ Q_3Q_2	00	01	11	10
0	x (0)	x (2)	x (4)	x (6)
1	1 (1)	1 (3)	1 (5)	1 (7)

$K_1 = 1$



A 3 bit Synchronous UP counter

RESULT → A 3 bit Asynchronous & Synchronous counter are designed & verified successfully

* RESULT – A 3-bit Asynchronous & Synchronous counter are designed & verified successfully.

Teacher's Signature : _____

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2	AIM :- Study of TTL gates AND, OR, NOT, NOR, NAND, EOR and Ex NOR	4-6	16/8/18	24/8/18	A
3	Aim :- Design of all gates using universal gates (NAND & NOR)	7-9	23/8/18	30/8/18	A
4	Aim :- Design & utilise a fun'n using K-map & verify its performance	10-12	30/8/18	13/9/18	A-
5.	Aim :- To Design a half and full adder ckt	13-14	06/9/18	27/9/18	A
6.	Aim - To design & verify 1-bit comparator	15-16	20/9/18	27/09/18	A-
7.	Aim To design a 4-bit even parity checker & verify them	17-18	20/9/18	27/9/18	A

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Sl No.	Name of the Experiment	Page No.	Date of Experiment	Date of Submission	Remarks
8.	Aim - To design & verify a 4:1 mux.	19-20	4/10/18		
9.	Aim - To verify truth table of JK, T & D flip flop	21-22	25/10/18		
10	Aim - To design a 4 bit shift register & verify its working	23-24	25/10/18		
11	Aim - To design a 3 bit asynchronous synchronous counter.	25-27	15/11/18		