

Roll No.
Printed Pages : 2

33083

BT-3 / D-17

DIGITAL ELECTRONICS

Paper-CSE-207 N

Time allowed : 3 hours]

[Maximum marks : 75]

Note : Attempt five questions in all, selecting at least one question from each unit. All questions carry equal marks.

Unit-I

1. Explain Quine Mc-Clusky (QM) method of Minimization?
Simplify the following expression using QM method also verify the results by K map method. 15

$$F = \sum w, x, y, z \ m(0, 1, 2, 3, 7, 8, 10, 11, 15)$$

2. (a) Write the small note on the following:
 (i) CMOS/TTL compatibility
 (ii) Tristate gate. 10
 (b) Realize the following logic equation using only NAND gates: 5

$$AB + CD = \overline{\overline{AB}} \cdot \overline{\overline{CD}}$$

Unit-II

3. (a) Design a 2-bit comparator using gates. 4
 (b) Design a 1:40 De-multiplexer using BCD to binary decoder. 6
 (c) Design a 4-bit adder circuit with ADD control lines. 5

(2)

4. (a) Design a 40:1 multiplexer using 8:1 multiplexers. 5
 (b) Write brief note on adder with look ahead carry. 5
 (c) Design a BCD to Gray code convertor using NAND gates only. 5

Unit-III

5. (a) Explain the operation of twisted ring counter and give its state diagram. 6
 (b) Draw the state diagram of J-K flip flop. 4
 (c) Design a 3 bit synchronous counter using J-K flip flop. 5
 6. Write short note on the following:
 (i) Asynchronous up/down counter
 (ii) Modulo-n counter.
 (iii) Universal shift registers. 15

Unit-IV

7. Explain the following in brief:
 (i) ROM
 (ii) EEPROM
 (iii) EAPROM 15
 8. Write short note on the following:
 (i) Memory decoding
 (ii) PAL using ROM
 (iii) FPGA 15

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