

ADC'S AND DAC'S

Physical variable → Transducer → ADC → Digital input → Digital system (e.g. computer) → DAC → Analog output → Actuator → To control physical variable

Most physical variables are analog in nature and can take on any value within a continuous range of values, e.g. temperature, pressure, light intensity, audio signals, position, rotational speed and flow rate.

Digital systems perform all of their internal operations using digital circuitry and digital operations. Any information that has to be inputted to a digital system must first be put into digital form and the outputs are always in digital form. Therefore, it is necessary to convert these quantities from "Analog to Digital" and "Digital to Analog".

The process of converting an analog signal to a digital form involves a sequence of four process:

- (a) Sampling
- (b) Holding
- (c) Quantizing
- (d) Encoding

"Quantizing and Encoding" processes are done simultaneously using a circuit referred to as an "A/D converter or ADC". Now the digital output has to be converted back to the analog form and the circuitry used for this purpose is referred to as a "D/A converter or DAC".

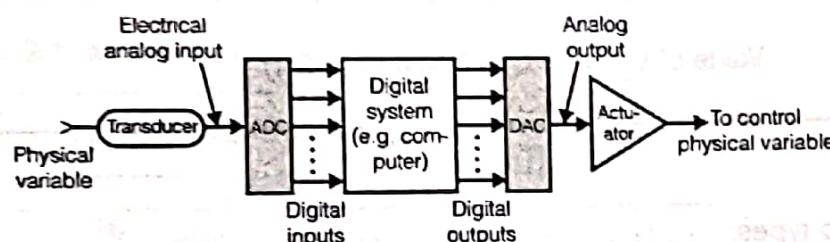


Fig. (9.1)

Digital to Analog Converter (DAC)

DAC as in figure (9.2) is the process of taking a value represented in digital code and converting it to a voltage or current which is proportional to the digital value.

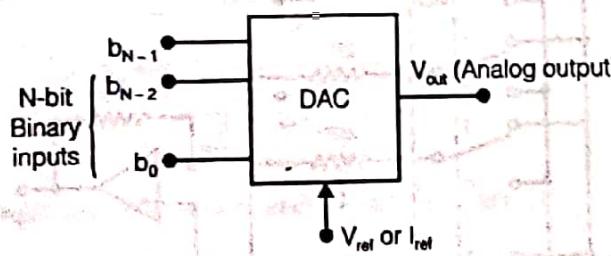


Fig. (9.2)

The analog output voltage "V₀" of an N-bit straight binary DAC is,

$$V_0 = K [2^{N-1} b_{N-1} + 2^{N-2} b_{N-2} + \dots + 2^2 b_2 + 2^1 b_1 + b_0]$$

↓
Analog output = K · Digital input

...(9.1)

where,

- K = Proportionality factor.
- $b_n = 1$; if the n^{th} bit of digital input is '1'.
- $= 0$; if the n^{th} bit of digital input is '0'.

Example 9.1

What is the largest value of output from an 8-bit DAC that produces 1.0 V for a digit input of 00110010?

Solution:

$$(00110010)_2 = (50)_{10}$$

$$1.0 \text{ V} = K \times 50$$

$$\therefore K = 20 \text{ mV}$$

The largest output will occur for an input of $(11111111)_2 = (255)_{10}$

$$V_{\text{OUT}}(\text{max}) = 20 \text{ mV} \times 255 = 5.10 \text{ V}$$

Example 9.2

A 5-bit D/A converter produces $V_{\text{out}} = 0.1 \text{ V}$ for a digital input of 00001. Find the value of V_{out} for an input of 11111.

Solution:

$$31 \leftarrow 0.1 = k \times 1 \Rightarrow k = 0.1$$

From the question, it is clear that, 0.1V is the weight of the LSB of 00001.

So, the weight of other bits must be,

$$V_o = 31 \times 0.1 = 3.1$$

16 × 0.1	8 × 0.1	4 × 0.1	2 × 0.1	0.1	(V)
≈ 1.6V	0.8V	0.4V	0.2V	0.1V	

$$\therefore \text{Value of } V_{\text{out}} = (1.6 + 0.8 + 0.4 + 0.2 + 0.1) \text{ V}$$

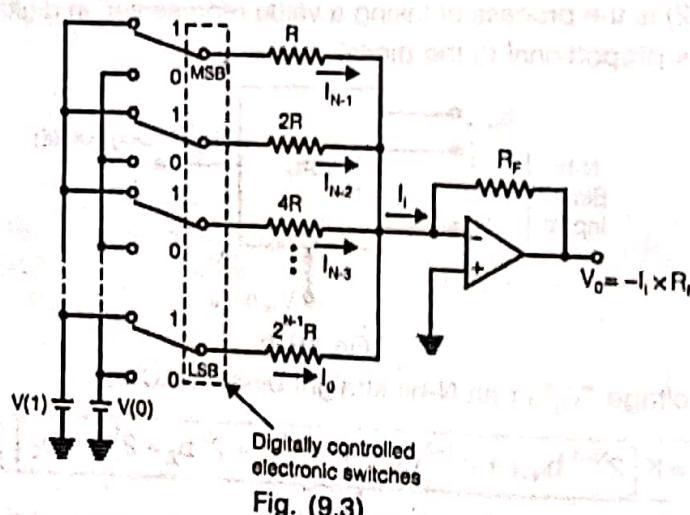
$$= 3.1 \text{ V}$$

Types of DAC

These are of two types:

- Weighted resistor D/A converter.
- R-2R ladder D/A converter.

Weighted-Resistor DAC



In the circuit given in figure (9.3) since the resistance values are weighted in accordance with the binary weight, so it is called "Weighted-resistor D/A converter".

Here operational amplifier is employed as a "summing amplifier".
The current I_i is given by:

$$I_i = I_{N-1} + I_{N-2} + I_{N-3} + \dots + I_2 + I_1 + I_0 \quad \dots(9.2)$$

$$\left. \begin{aligned} I_{N-1} &= \frac{V_{N-1}}{R} \\ I_{N-2} &= \frac{V_{N-2}}{2^1 \cdot R} \\ I_{N-3} &= \frac{V_{N-3}}{2^2 \cdot R} \\ I_0 &= \frac{V_0}{2^{N-1} \cdot R} \end{aligned} \right\}$$

...(9.3)

Since, OPAMP output $V_0 = -I_i R_F$ ✓
for straight binary input, $V(0) = 0$ and $V(1) = -V_R$,

$$V_0 = -(-V_R) \left[\frac{R_F}{R} \cdot b_{N-1} + \frac{R_F}{2R} \cdot b_{N-2} + \frac{R_F}{2^2 \cdot R} \cdot b_{N-3} + \dots + \frac{R_F}{2^{N-1} \cdot R} \cdot b_0 \right] \quad \text{DAG related RL-R}$$

$$V_0 = \frac{R_F}{2^{N-1} \cdot R} \cdot V_R [b_{N-1} + b_{N-2} + b_{N-3} + \dots + b_0] \quad \dots(9.4)$$

comparing equation (9.1) and (9.4),

$$\text{Proportionality factor} = K = \frac{R_F}{2^{N-1} \cdot R} \quad \checkmark \quad \dots(9.5)$$

$$V_0 = \frac{R_F}{2^{N-1} \cdot R} (2^{N-1} V_{N-1} + 2^{N-2} V_{N-2} + \dots + 2^1 V_1 + 2^0 V_0) \quad \dots(9.6)$$

The OP-AMP in the figure (9.3) is operated in negative feedback mode to work as an excellent "current to voltage converter"

$$I_i = \frac{V_R}{2^{N-1} \cdot R} [2^{N-1} \cdot b_{N-1} + 2^{N-2} \cdot b_{N-2} + \dots + 2^1 b_1 + 2^0 b_0]$$

$$I_i = \frac{V_R}{2^{N-1} \cdot R} \sum_{i=1}^{N-1} 2^i b_i \quad \dots(9.7)$$

The maximum output current will flow when all b_i coefficient are '1'.

i.e.

$$I_{\max} = \frac{V_R}{2^{N-1} \cdot R} (2^N - 1) \quad \dots(9.8)$$

$$\text{LSB - resistance} = 2^{N-1} \cdot \text{MSB resistance}$$

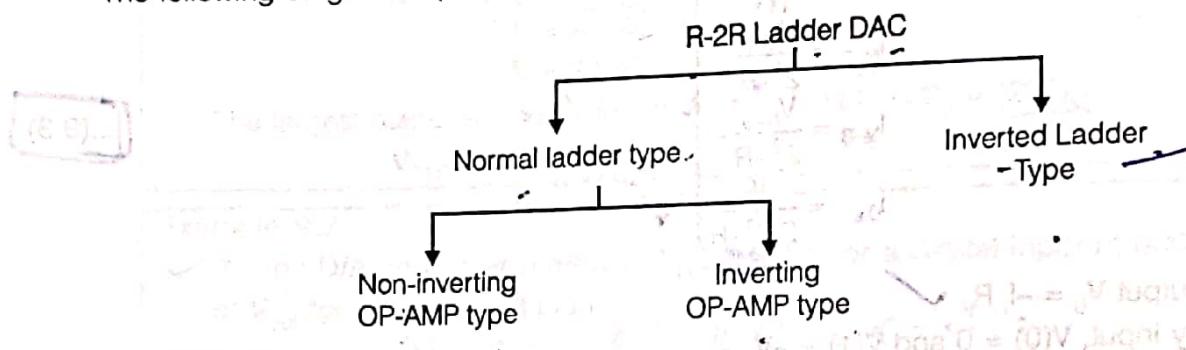
[SAIL, IES]

Disadvantages

- Due to the large difference in resistor values between the LSB and MSB, we cover a wide range of resistances and which track over a wide temperature range are difficult to produce.
- Due to "Loading effect" (input impedance will not remain constant), accuracy of the system is less.
- Linearity is less.

R-2R Ladder DAC

The following diagram depicts the various types of R-2R ladder DAC:

**R-2R Ladder DAC by using Non-inverting OP-AMP**

Here we consider a 3-bit ($b_2 b_1 b_0$) R-2R ladder DAC. We always consider the bit as MSB, where the input reference voltage or supply to be given

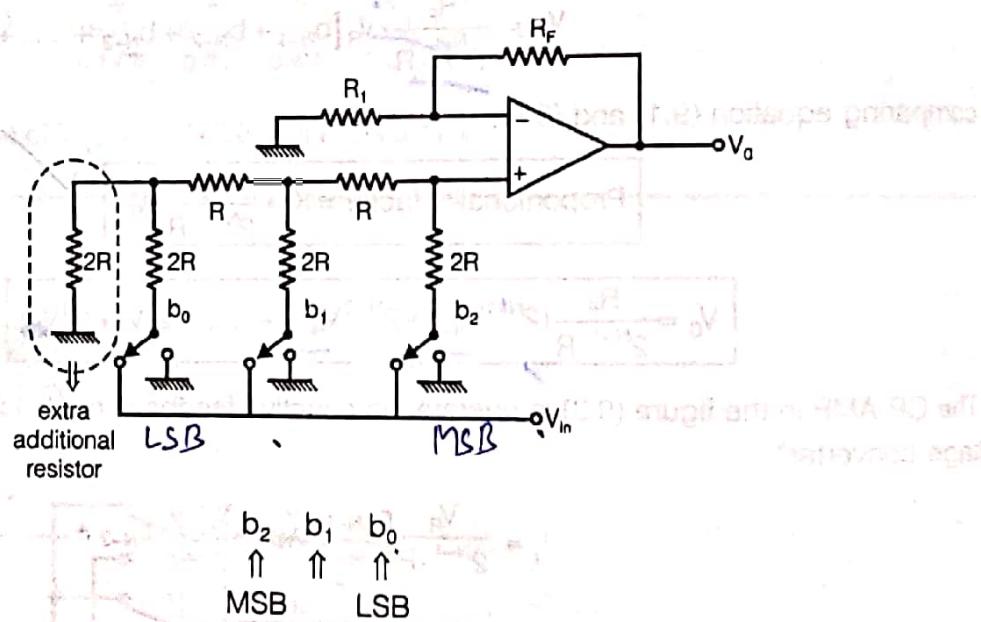


Fig. (9.4)

$$\text{Gain of the OP-AMP} = \frac{V_o}{V_i} = \left(1 + \frac{R_F}{R_1}\right)$$

The output analog voltage $V_o \approx V_a$ is given by,

$$V_o = \frac{V_i}{2^N} \left[\sum_{i=0}^{N-1} 2^i b_i \right] \times \left[1 + \frac{R_F}{R_1} \right]$$

$V_o = V_{\text{ref}} \times \text{decimal equivalent of binary data} \times \text{Gain of OP-AMP}$.

R-2R Ladder DAC by using Inverting OP-AMP

Here we consider a 3-bit ($b_2 b_1 b_0$) R-2R ladder DAC. It is preferable to have a circuit that uses resistances that are fairly close in value. In this DAC, the resistance values span a range of only 2 to 1, so that the problem arises in weighted-resistor DAC can be eliminated by using this DAC.

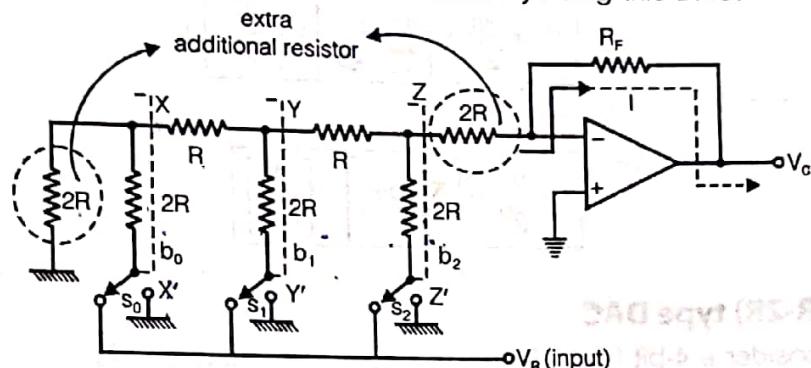


Fig. (9.5)

In this circuit, we have assumed the digital input as 001 i.e. switch "S₀" is closed. This circuit is simplified using "Thevenin's theorem". Applying Thevenin's theorem at XX', YY' and ZZ', we get the circuits of figure 9.6 (a), figure 9.6 (b) and 9.6 (c) respectively.

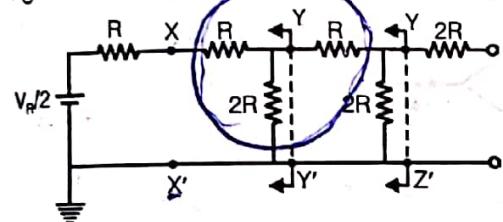


Fig. 9.6(a)

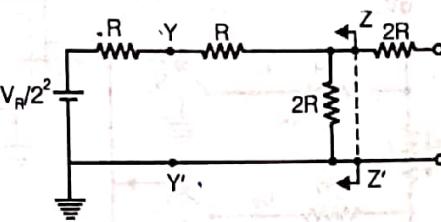


Fig. 9.6(b)

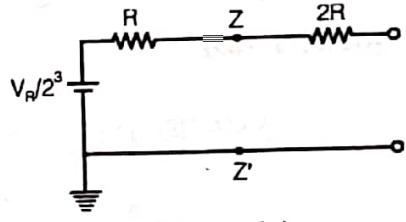


Fig. 9.6(c)

Here,

digital input \Rightarrow equivalent voltage

$$001 \Rightarrow \frac{V_R}{2^3}$$

$$010 \Rightarrow \frac{V_R}{2^2}$$

$$100 \Rightarrow \frac{V_R}{2^1}$$

The value of the "input impedance" or "equivalent resistance" is $3R$ in each case. The equivalent circuit of figure (9.6) is given in figure 9.6(6) as,

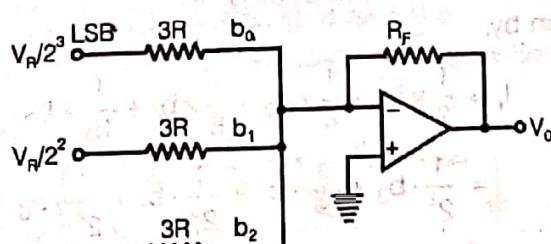


Fig. 9.6(d)

$$V_O = -\left(\frac{R_F}{3R} \cdot \frac{V_R}{2^3} \cdot b_0 + \frac{R_F}{3R} \cdot \frac{V_R}{2^2} \cdot b_1 + \frac{R_F}{3R} \cdot \frac{V_R}{2^1} \cdot b_2\right)$$

Digital Electronics

$$V_0 = -\left(\frac{R_F}{3R}\right) \left(\frac{V_R}{2^3}\right) [4b_2 + 2b_1 + b_0] \quad \dots(9.10)$$

Finally, for an N-bit DAC,

$$V_0 = \frac{V_R}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i \right] \times \left[\frac{-R_F}{3R} \right] \quad \dots(9.11)$$

Since,

∴

V₀

$$I_f = \frac{V_R}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i \right] \times \left[\frac{1}{3R} \right] \quad \dots(9.12)$$

Inverted Ladder (R-2R) type DAC

- Here we consider a 4-bit (b_3, b_2, b_1, b_0) R-2R DAC as in figure (9.7).
- ON-OFF switches (S_0, S_1, S_2, S_3) are at the same potential.
- Also, the bit stream ($b_3 b_2 b_1 b_0$) has MSB = b_3 and LSB = b_0 .

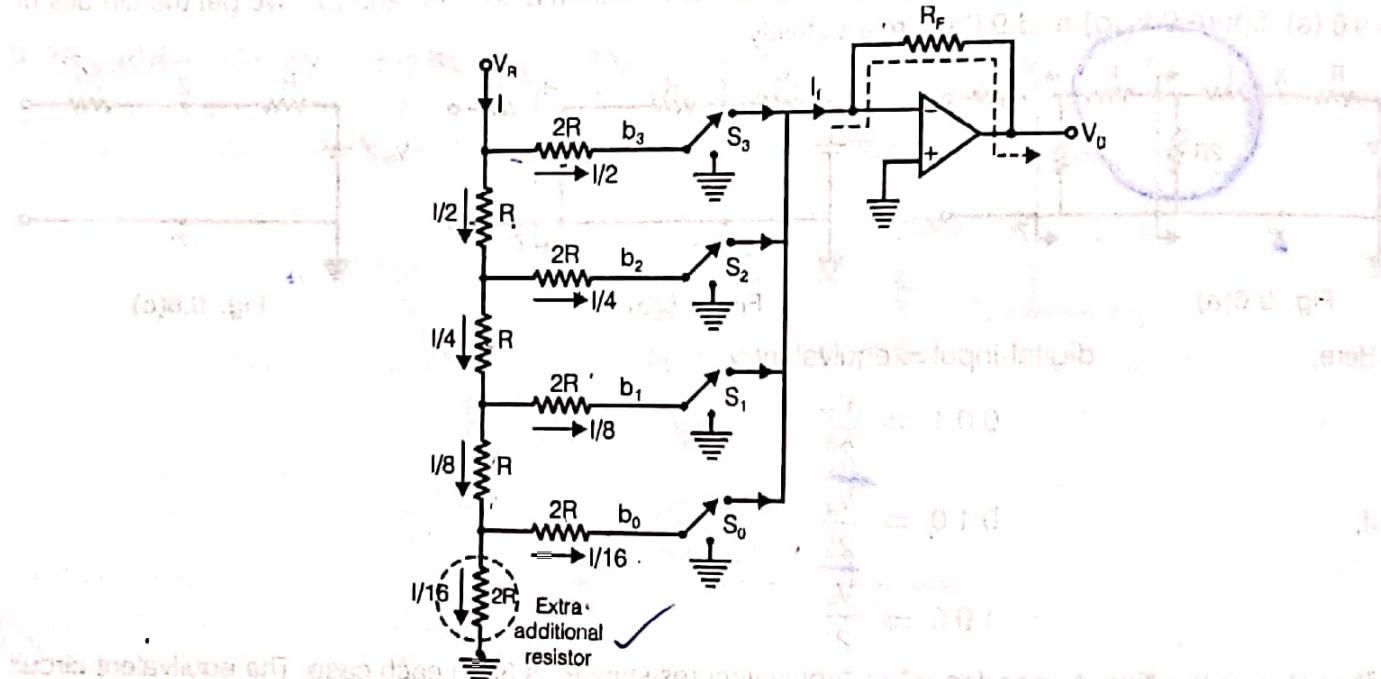


Fig. (9.7)

The forward current I_f is given by,

$$\begin{aligned} I_f &= \frac{1}{2} \times b_3 + \frac{1}{4} \times b_2 + \frac{1}{8} \times b_1 + \frac{1}{16} \times b_0 \\ &= \frac{1}{2^1} \cdot b_3 + \frac{1}{2^2} \cdot b_2 + \frac{1}{2^3} \cdot b_1 + \frac{1}{2^4} \cdot b_0 \end{aligned}$$

For an N-bit DAC,

$$I_f = \frac{1}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i \right] \quad \dots(9.13)$$

Since,

$$V_0 = -I_f \times R_F$$

Also,

$$V_o = \frac{V_R}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i \right] \times \frac{-R_F}{R}$$

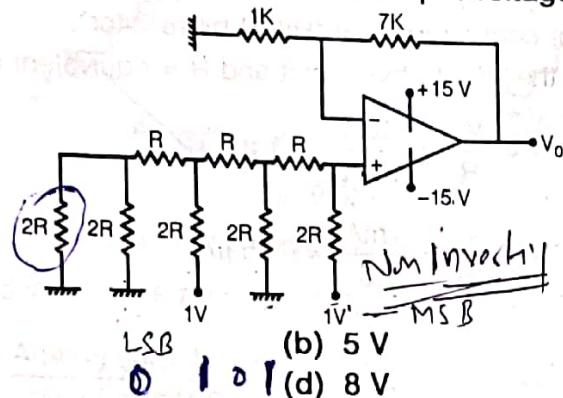
... (9.14)

$$I_f = \frac{V_R}{2^N} \times \left[\sum_{i=0}^{N-1} 2^i b_i \right] \times \frac{1}{R}$$

... (9.15)

Example 9.3

For the 4 bit DAC shown in the figure, the output voltage V_o is



- (a) 10 V
(b) 5 V
(c) 4 V
(d) 8 V

[GATE-2000]

Solution: (b)

This given circuit is a 4-bit R-2R ladder type DAC by using Non-inverting OP-AMP, we have,

$b_3 \quad b_2 \quad b_1 \quad b_0$
↓ ↓ ↓ ↓

MSB LSB

Given \Rightarrow

1 0 1 0

\therefore Decimal equivalent = 10 Volt

$$\text{Gain} = G = 1 + \frac{R_F}{R_1} = 1 + \frac{7k}{1k} = 8$$

(Given)

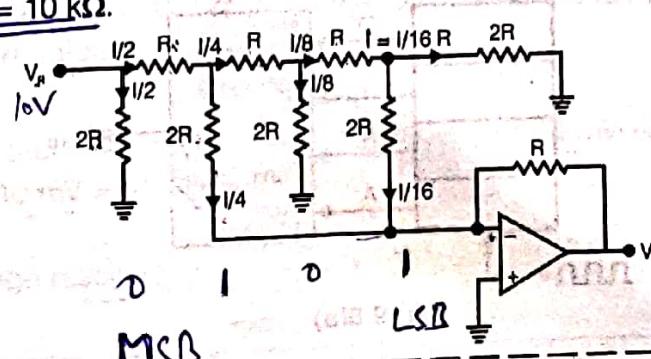
$$\therefore \text{Output voltage} = V_o = \frac{1}{2^4} \times 10 \times 8$$

$$\therefore \text{Output voltage} = V_o = 5 \text{ V}$$

Statement for Linked Answer Questions (9.4 and 9.5):

In the Digital-to-Analog converter circuit shown in the figure below,

$V_R = 10 \text{ V}$ and $R = 10 \text{ k}\Omega$.



Example 9.4

The current i is
 (a) $31.25 \mu\text{A}$
 (c) $125 \mu\text{A}$

(b) $62.5 \mu\text{A}$
 (d) $250 \mu\text{A}$

[GATE-2007]

Solution: (b)

This given circuit is a R-2R ladder DAC using inverted OP-AMP type.

Also, $V_R = 10 \text{ V}$ and $R = 10 \text{ k}\Omega$

Since, $V_0 = -I_f \times R$

where, I_f is the current coming from all "HIGH bit resistor".

Let "I" = current from the " V_R " to the circuit and R = equivalent resistance

$$I = \frac{V_R}{R} = \frac{10 \text{ V}}{10 \text{ k}\Omega} = 1 \mu\text{A}$$

and,

$$i = \frac{I}{16} = \frac{1 \text{ mA}}{16} = 62.5 \mu\text{A}$$

Example 9.5

The voltage V_0 is
 (a) -0.781 V
 (c) -3.125 V

(b) -1.562 V
 (d) -6.250 V

[GATE-2007]

Solution: (c)

Now,

$$I_f = \frac{I}{4} + \frac{I}{16} = \frac{5I}{16}$$

$$\therefore V_0 = -I_f \cdot R = \frac{-5I}{16} \times 10 \text{ k}\Omega = -3.125 \text{ V}$$

Specifications for DAC

They are generally specified by the manufacturers.

Resolution

It is defined as the smallest change that can occur in the analog output as a result of a change in the digital input. The "resolution" is always equal to the "weight of the LSB" and is also referred to as the "step size", since it is the amount that V_{out} will change as the digital input value is changed from one step to the next.

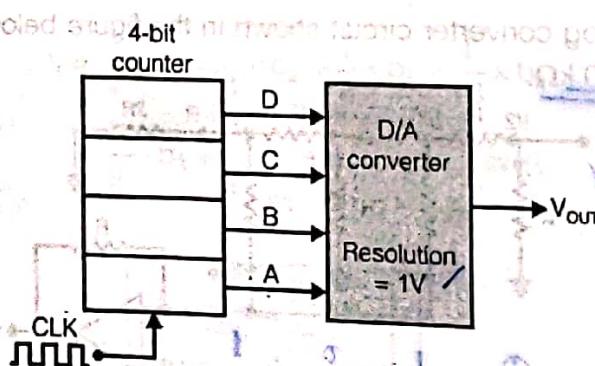


Fig. 9.8(a)

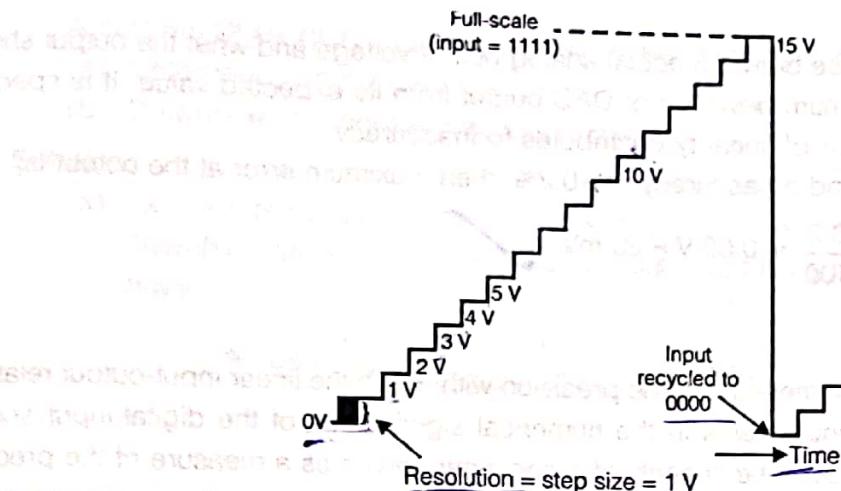


Fig. 9.8(b)

⇒ For an N-bit DAC the number of different levels = 2^N and the number of steps = $2^N - 1$.

Resolution (step size) is same as the proportionality factor "K" in the equation (9.1).

$$\text{Step size (Resolution)} = \frac{\text{Analog output}}{\text{No. of steps}}$$

$$\text{Resolution} = \frac{V_a}{2^N - 1} \quad \dots(9.16)$$

"Resolution" can also be expressed as the amount of voltage or current per step; so it is also useful to express it as a percentage of the full scale output.

$$\text{Percentage Resolution} = \frac{\text{Step size}}{\text{Full scale output}} \times 100\% \quad \dots(9.17)$$

$$\text{Percentage Resolution} = \frac{1}{2^N - 1} \times 100\% \quad \dots(9.18)$$

- ⇒ Only the number of bits (N) determines the percentage resolution.
- ⇒ From above equation we conclude that with the increase of number of bits, percentage resolution will decrease.

Example 9.6

A 10-bit DAC has a step size of 10 mV. Determine the full-scale output voltage and the percentage resolution.

Solution:

With 10-bits, there will be $2^{10} - 1 = 1023$ steps of 10 mV each. The full-scale output will therefore be $10 \text{ mV} \times 1023 = 10.23 \text{ V}$ and $\frac{10.23}{1023} \times 100\% \approx 0.1\%$

$$\text{Percentage resolution} = \frac{10 \text{ mV}}{10.23 \text{ V}} \times 100\% \approx 0.1\%$$

Accuracy

It is a measure of the difference between actual analog output voltage and what the output should be in the ideal case. Also, it is the maximum deviation of DAC output from its expected value. It is specified as a "% of full scale voltage (FSV)". Lack of linearity contributes to inaccuracy. e.g. If a DAC has 10 V FSV and an accuracy of $\pm 0.2\%$, then maximum error at the output is,

$$10 \text{ V} \times \frac{0.2}{100} = 0.02 \text{ V} \approx 20 \text{ mV}$$

Linearity

The linearity of a converter is a measure of the precision with which the linear input-output relationship is satisfied. In an ideal DAC, equal increments in the numerical significance of the digital-input should yield equal increments in the analog output. The linearity of a converter serves as a measure of the precision with which this requirement is satisfied. The "linearity" of a converter depends principally on the accuracy of the resistors. Also, the linearity may be adversely affected by substantial temperature changes.

Monotonicity

If the output of DAC increases as the digital input is incremented from one value to other, then it is "monotonic". In other words, the staircase output will have no downward steps when the binary input is incremented from 0 to FSV.

Temperature Sensitivity

At any fixed digital input, the analog output will vary with temperature, this is referred as "temperature sensitivity". The overall temperature sensitivity is due to the temperature sensitivity of the reference voltages, resistors, OP-AMP and even the amplifier offset voltage. Typical ranges from about $\pm 50 \text{ ppm}/^\circ\text{C}$ to $\pm 1.5 \text{ ppm}/^\circ\text{C}$. For a good quality of DAC, it should be minimum.

Settling Time

When the digital input to D/A converter changes, the analog output voltage does not change abruptly. Because of the presence of switches, active devices, stray capacitance, and inductance associated with the passive circuit components, the transients appear in the output voltage and oscillations may also occur. The time required for the analog output to settle to within $\pm 1/2 \text{ LSB}$ of the final value after a change in the digital input is usually specified by the manufacturers and is referred to as settling time.

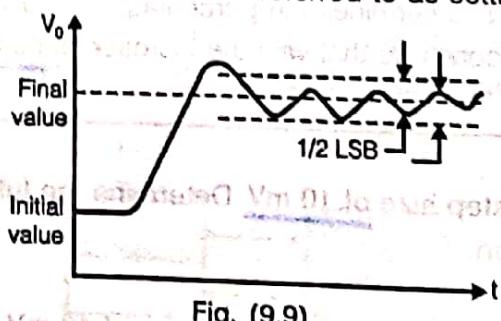


Fig. (9.9)

Offset Error

Ideally, the output of DAC will be zero volts when all binary input is 0s. But in practice, however, there will be a very small output voltage for this condition; this is called "offset error". If this error is not corrected, it will be added to the expected DAC output for all input cases.

Example 9.7

A certain 12-bit BCD digital-to-analog converter has a full-scale output of 9.99 V.

(a) Determine the percent resolution.

(b) Determine the converter's step size.

Solution:

(a) Twelve bits correspond to three decimal digits, i.e. decimal numbers from 000 to 999. Therefore the output of this DAC has 999 possible steps from 0 V to 9.99 V. Thus we have

$$\begin{aligned}\% \text{ resolution} &= \frac{1}{\text{Number of steps}} \times 100\% \\ &= \frac{1}{999} \times 100\% \approx 0.1\%\end{aligned}$$

$$\begin{aligned}\text{(b)} \quad \text{Step size} &= \frac{\text{FS}}{\text{Number of steps}} = 9.99 \text{ V}/999 \\ &= 0.01 \text{ V}\end{aligned}$$

Example 9.8

A 10-bit A/D converter is used to digitize an analog signal in the 0 to 5 V range. What is the approximate value of the maximum peak to peak ripple voltage that can be allowed in the d.c. supply voltage?

- (a) 100 mV
- (b) 50 mV
- (c) 25 mV
- (d) 5.0 mV

[IES-2006]

Solution: (d)

Maximum peak to peak ripple voltage

$$\begin{aligned}&= \frac{\text{FSV.}}{2^N} = \frac{5}{2^{10}} = \frac{5}{1024} \\ &\approx \frac{5}{1000} \approx 5 \text{ mV}\end{aligned}$$

Applications of DAC

- Control
- Automatic testing
- Signal reconstruction
- A/D conversion

Analog-to-Digital Convertor (ADC)

An ADC takes an analog input voltage and after a certain amount of time produces a digital output code which represents the analog input. ADC is generally more complex and time consuming than a DAC. A general diagram of ADCs is shown in figure (9.9) below.

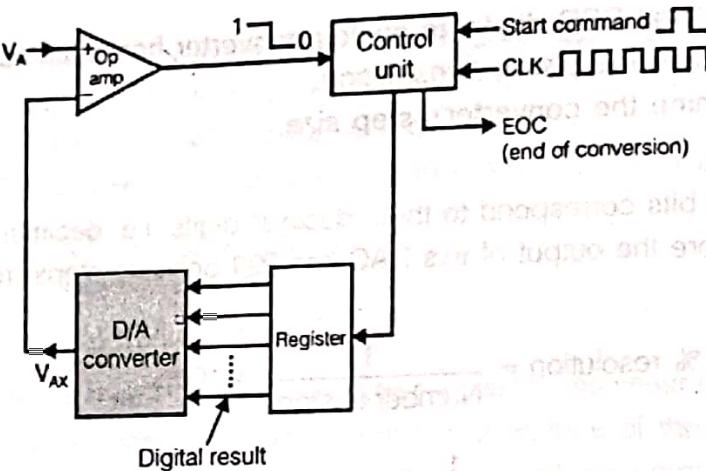


Fig. (9.10)

Basic operation of ADCs

The START command pulse initiates the operation. At a rate determined by the clock, the control unit continually modifies the binary number that is stored in the register. The binary number in the register is converted to an analog voltage, V_{AX} , by the DAC. The comparator compares V_{AX} with the analog input V_A . As long as $V_{AX} < V_A$, the comparator output stays HIGH. When V_{AX} exceeds V_A by at least an amount = V_T (threshold voltage), the comparator output goes LOW and stops the process of modifying the register number. At this point, V_{AX} is a close approximation to V_A . The digital number in the register, which is the digital equivalent of V_{AX} , is also the approximate digital equivalent of V_A , within the resolution and accuracy of the system. The control logic activates the end-of-conversion signal, EOC, when the conversion is complete.

Digital-Ramp ADC

It is also referred as a "Counter-Type ADC". Figure (9.11) shows the digital-ramp ADC, contains a counter a DAC, an analog comparator and a control AND gate. The comparator output serves as the active low end-of-conversion signal i.e. EOC.

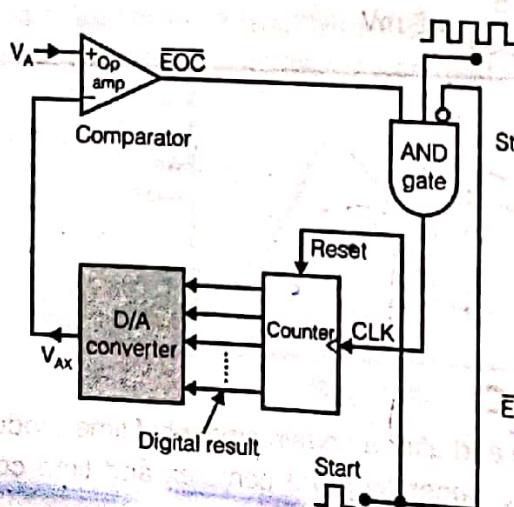


Fig. (9.11)

Operation of Counter-type ADC

A START pulse is applied to reset the counter to zero. The HIGH at START also inhibits clock pulse from passing through the AND gate into the counter. With all 0's at its input, the DAC's output will be $V_{AX} = 0$ V. Since $V_A > V_{AX}$, the comparator output, \overline{EOC} , will be HIGH. When START returns, LOW, the AND gate is enabled and clock pulse get through to the counter. As the counter advances, the DAC output, V_{AX} , increases one step at a time as shown in figure (9.10). This continues until V_{AX} reaches a step that exceeds V_A by an amount equal to or greater than V_T (typically 10 to 100 mV). At this point, \overline{EOC} will go LOW and inhibit the flow of pulses into the counter and the counter will stop counting. The conversion process is now complete as signified by the HIGH-to-LOW transition at \overline{EOC} , and the contents of the counter are the digital representation of V_A . The counter will hold the digital value until the next START pulse initiates a new conversion.

Conversion time

The conversion time (t_c) as shown in figure (9.11) is the time interval between the end of START pulse and activation of the \overline{EOC} output. It should be noted that the value of " t_c " depends on " V_A ". A larger value will require more steps before the stair case voltage exceeds " V_A ".

For an N-bit ADC,

$$t_{c(\max)} = (2^N - 1) \text{ CLK cycles} \quad \dots(9.19)$$

Also,

$$t_{c(\text{avg.})} = \frac{t_{c(\max)}}{2} = \left(\frac{2^N - 1}{2} \right) \text{ CLK cycles}$$

$$\therefore t_{c(\text{avg.})} \approx (2^N - 1) \cdot \text{CLK cycles} \quad \dots(9.20)$$

Disadvantages

- It has large conversion time (essentially doubles for each bit that is added to the counter).
- The resolution can be improved only at the cost of a longer " t_c ".
- It is used for low-speed application.

Note:

In this ADC, if the normal counter is replaced by "Up-Down Counter" then it is called Tracking-Type ADC.

Successive Approximation Type ADC

It is one of the most widely used types of ADC. It has more complex circuitry than the digital ramp ADC but a much shorter conversion time (t_c) i.e. it operates at faster rate. SACs have a fixed value of conversion time (t_c) i.e. " t_c " is independent of the value of the analog input voltage (V_A).

Circuit diagram

The 8-bit successive approximation A/D converter is shown below:

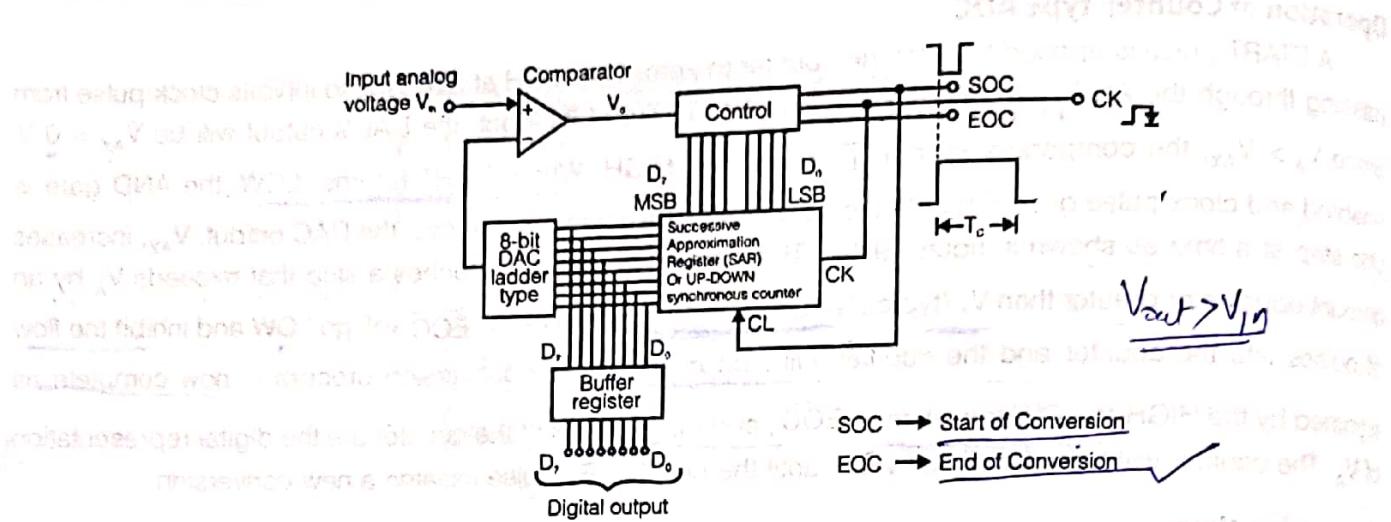


Fig. (9.12)

Operation

1. The SOC goes low, counter is cleared and the digital output is 0000 0000.
2. At the same time the input analog voltage is applied such that V_0 goes HIGH and the EOC signal goes HIGH and the conversion starts.
3. During the first clock pulse, the control circuit loads a HIGH MSB into the SAR whose output is then 1000 0000.
4. If $V_{out} < V_{in}$, the negative output of the comparator signals the control circuit to reset the MSB.
5. If $V_{out} > V_{in}$, the positive output of the comparator indicates that the MSB is to remain set.
6. If $V_{out} = V_{in}$, the conversion is complete.
7. The next lower bits are then handled in the same way. This process is continued until the SAR tries all the bits.
8. When the conversion is complete, the control circuit sends a low signal i.e. EOC.
9. At the falling edge of the EOC signal the digital equivalent is loaded into the buffer register.
10. Thus the buffer register contains the digital output.

Conversion time (t_c)

The processing of each bit takes one CLK cycle, so the total conversion time for a N-bit SAC will be N-CLK cycles.

i.e. If t_c be the time taken for one bit conversion step, then

$$t_c \text{ for SAC} = N \times 1 \text{ CLK cycle}$$

...(9.21)

Example 9.9

An 8-bit SAC has a resolution of 20 mV. What will its digital output be for an analog input of 2.17 V?

Solution:

$$\text{No. of steps} = 2.17 \text{ V}/20 \text{ mV} = 108.5$$

So that step 108 would produce $V_{Ax} = 2.16 \text{ V}$ and step 109 would produce 2.18 V. The SAC always produces a final V_{Ax} that is at the step below V_A . Therefore, for the case of $V_A = 2.17 \text{ V}$, the digital result would be $(108)_{10} = (01101100)_2$.

Example 9.10

An 8 bit successive approximation analog to digital converter has full scale reading of 2.55V and its conversion time for an analog input of 1V is 20 μ s. The conversion time for a 2V input will be

- (a) 10 ms
- (b) 20 ms
- (c) 40 ms
- (d) 50 ms

[GATE-2000]

Solution: (b)

In the SAC type ADC, t_c is independent of V_A .

So, t_c for 2 V = t_c for 1 V = 20 ms

Parallel-Comparator Type ADC

[IES-2003]

It is also called Flash type ADC or Simultaneous Converter. The Flash Type ADCs is the highest speed ADC available, but it requires much more circuitry than the other types. For an N-bit converter, the total number of flash or parallel comparator = $2^N - 1$. In this ADC, 2^N resistors and 1-priority encoder type ($2^n \times n$) are needed. A 3-bit flash converter is shown in figure (9.13) below.

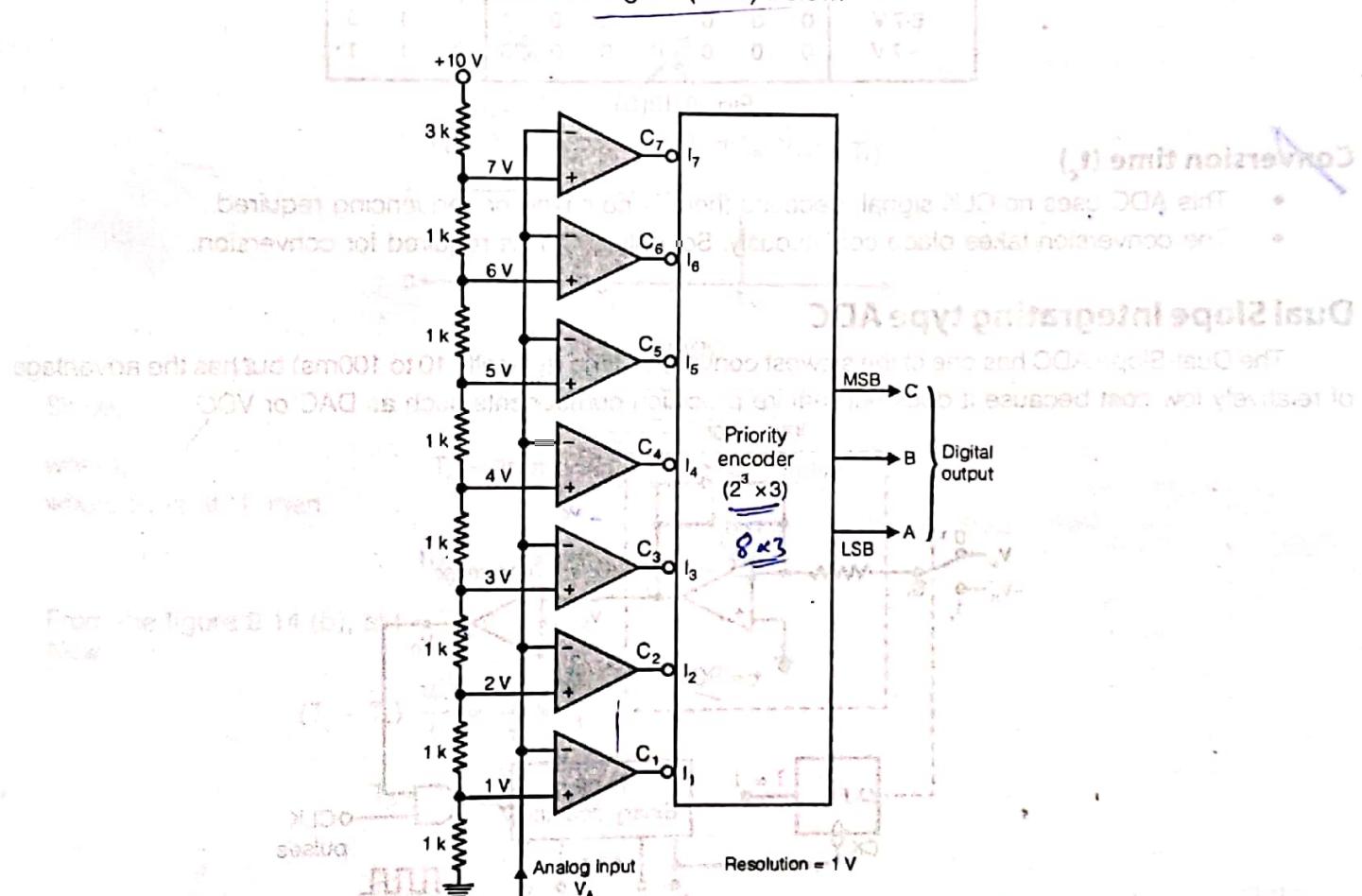


Fig. 9.13(a)

Operation

As in the truth table in figure 9.13(b), it is clear that 1-priority encoder gives the output as digital form.

- With $V_A < 1$ V, all the comparator outputs C_1 to C_7 , will be HIGH.
- With $V_A > 1$ V, one or more of the comparator outputs will be LOW. The comparator outputs are fed into an active-LOW priority encoder that generates a binary output corresponding to the highest-numbered comparator output that is LOW. For example, when $V_A = 3.5$ V, outputs C_1 , C_2 and C_3 will be LOW and all others will be HIGH. The priority encoder will respond only to the LOW at C_3 and will produce a binary output $CBA = 011$, which represents the digital equivalent of V_A , when the resolution of 1 V. When V_A is greater than 7 V, C_1 to C_7 will all be LOW, and the encoder will produce $CBA = 111$ as the digital equivalent of V_A .

Truth table of 3-bit flash ADC:

Analog input	Comparator outputs							Digital outputs		
	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C	B	A
0-1 V	1	1	1	1	1	1	1	0	0	0
1-2 V	0	1	1	1	1	1	1	0	0	1
2-3 V	0	0	1	1	1	1	1	0	1	0
3-4 V	0	0	0	1	1	1	1	0	1	1
4-5 V	0	0	0	0	1	1	1	1	0	0
5-6 V	0	0	0	0	0	1	1	1	0	1
6-7 V	0	0	0	0	0	0	1	1	1	0
> 7 V	0	0	0	0	0	0	0	1	1	1

Fig. 9.13(b)

Conversion time (t_c)

- This ADC uses no CLK signal, because there is no timing or sequencing required.
- The conversion takes place continuously. So, only 1 CLK is required for conversion.

Dual Slope Integrating type ADC

The Dual-Slope ADC has one of the slowest conversion time (typically 10 to 100ms) but has the advantage of relatively low cost because it does not require precision components such as DAC or VCO.

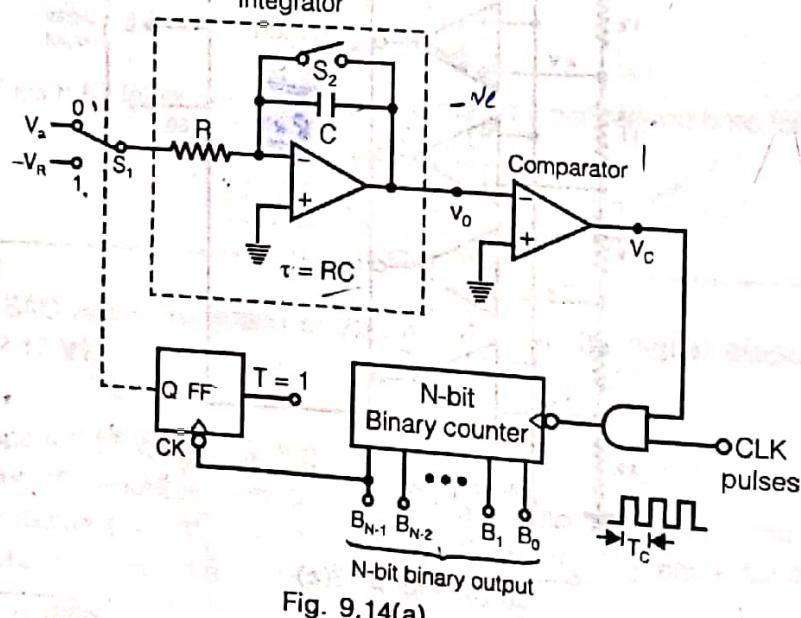


Fig. 9.14(a)

Operation

The basic operation of this ADC involves the linear charging and discharging of a capacitor 'C' using constant currents.

The integrator output is,

$$V_0 = -\frac{1}{\tau} \int_0^t V_a dt = -\left(\frac{V_a}{\tau}\right)t \quad \dots(9.22)$$

This results in HIGH V_c , thus enabling the AND gate and the clock pulses reach the CLK input terminal of the counter which was initially clear. The counter counts from 00 .. 00 to 111 ... 11 when $2^N - 1$ clock pulses are applied. At the next clock pulse 2^N , the counter is cleared and Q becomes 1. This controls the state of S_1 , which now moves to position 1 at T_1 , thereby connecting $-V_R$ to the input of the integrator. The output of the integrator now starts to move in the positive direction. The counter continues to count until $V_0 < 0$. As soon as V_0 goes positive at T_2 , V_c goes LOW disabling the AND gate. The counter will stop counting in the absence of the CLK pulses.

Waveforms of dual-slope ADC

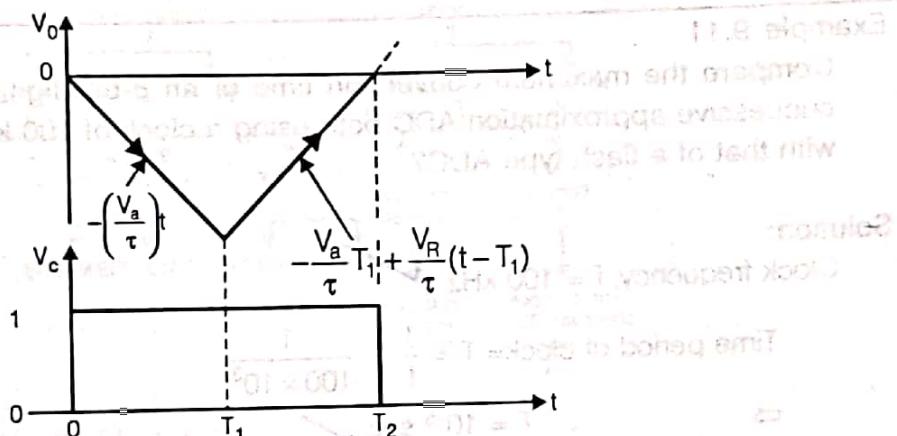


Fig. 9.14(b)

Since,

$$T_1 = 2^N \cdot T_C \text{ and } T_2 = N \cdot T_C$$

where,

when, S_1 is at '1' then,

$$V_0 = -\frac{V_a}{\tau} T_1 + \frac{V_R}{\tau} (t - T_1)$$

From the figure 9.14 (b), at $t = T_2$, $V_0 = 0$

Now,

$$(T_2 - T_1) \frac{V_R}{\tau} = \frac{V_a}{\tau} \times T_1$$

$$T_2 - T_1 = \frac{V_a}{V_R} \cdot T_1$$

$$T_2 - T_1 = \frac{V_a}{V_R} \cdot 2^N T_C$$

... (9.23)

Let the count recorded in the counter be 'n' at T_2 .

Then,

$$T_2 - T_1 = n \times T_C$$

... (9.24)

from (9.23) and (9.24) we get,

$$n \times T_C = \frac{V_a}{V_R} 2^N T_C$$

$$\Rightarrow n = \frac{V_a}{V_R} \cdot 2^N \quad \checkmark \quad \dots(9.25)$$

Equation (9.25) shows that the output of counter is proportional to the ' V_a '.
The count recorded in the counter is numerically equal to ' V_a ' if $V_R = 2^N$.

Conversion time (t_c)

Maximum total conversion time for an N-bit ADC is given by,

$$t_c = T_1 + T_2 = (2^N + N_{\max}) T_{CLK} \quad \dots(9.26)$$

Also,

$$t_c = (2^{n+1}) \text{ CLK cycles} \quad \dots(9.27)$$

It is most accurate but very slowest ADC. It is often used in "digital voltmeter" because of its good conversion accuracy and low cost.

Example 9.11

Compare the maximum conversion time of an 8-bit digital ramp ADC with that of a successive approximation ADC both using a clock of 100 kHz. How do these compare with that of a flash type ADC?

[IES-2003]

Solution:

Clock frequency, $f = 100 \text{ kHz}$

$$\text{Time period of clock} = T = \frac{1}{f} = \frac{1}{100 \times 10^3}$$

$$\Rightarrow T = 10^{-5} \text{ sec} \quad \checkmark$$

$$\text{Number of bits} = n = 8$$

Maximum conversion time of an 8-bit digital ramp ADC is

$$T_1 = 2^8 \times T = 2^8 \times 10^{-5} = 2560 \text{ m sec} \quad \checkmark$$

Maximum conversion time of successive approximation ADC is

$$T_2 = nT = 8 \times 10^{-5} = 80 \text{ m sec} \quad \checkmark$$

Maximum conversion time of a flash type ADC is

$$T_3 = T = 10^{-5} \text{ sec} \quad \checkmark$$

$$\frac{T_1}{T_2} = \frac{2560}{80} = 128$$

$$\frac{T_2}{T_3} = \frac{80}{10} = 8$$

$$\frac{T_1}{T_3} = \frac{2560}{10} = 256$$

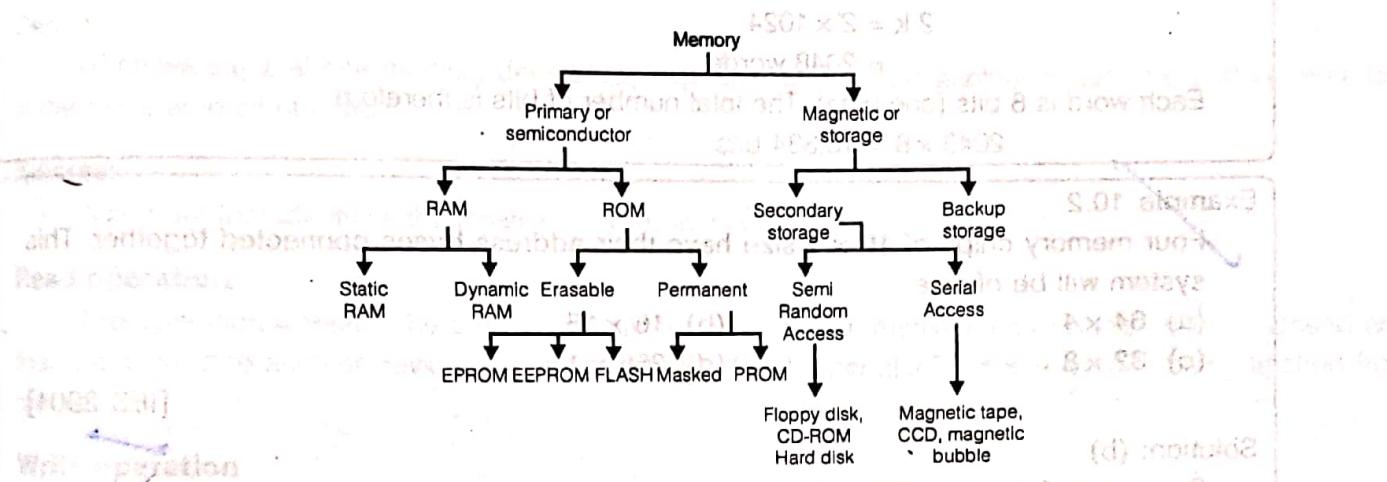
Thus, the maximum conversion time of an 8-bit digital ramp ADC is 128 times that of a successive approximation ADC and 256 times that of flash type ADC. Maximum conversion time of an 8-bit successive approximation ADC is 8-bit that of flash type ADC.

0000

SEMICONDUCTOR MEMORIES

Fig. 10.1 shows the classification of memory.

A digital processor generally requires a facility for storing information; the subsystem of a digital processor which provides this storage facility is called the "MEMORY". A memory stores data for processing and instructions for execution.



Semiconductor Memory

These memories are used as the "internal memory" of a computer, where fast operation is important. It is also called "main or working memory" and is in constant communication with the CPU as a program of instruction is being executed. The basic element of this memory is a flip-flop.

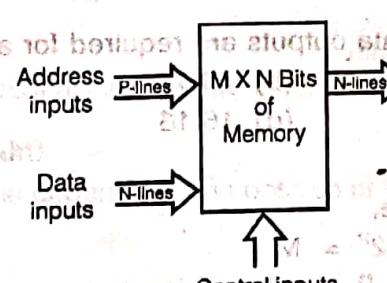


Fig. (10.1)

The size or capacity of a memory chip is specified as $(M \times N)$ bits.

where,

M = Number of locations available in the memory

N = Number of bits at each location

In other words, this means that M words of N bits each can be stored in the memory.

Assembler

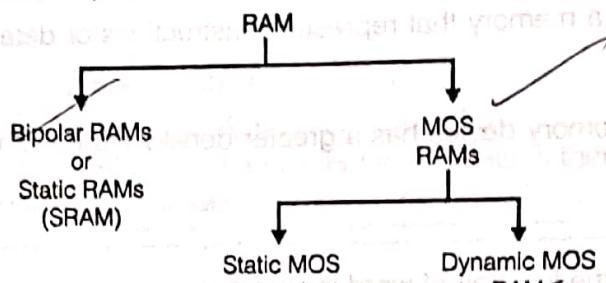
Program that translates an assembly language program from mnemonics to the binary machine code of a computer.

Direct Memory Access (DMA)

DMA interface is used for transferring data directly between an external device and memory.

Random Access Memory (RAM)

In RAM, the memory locations are organised in such a way so that any memory location requires equal time for writing or reading. It is generally called "Read-write memory" (RWM). It is a volatile memory. It can be easily programmed, erased and reprogrammed by the user. It is a "primary memory" of computer.



Static RAM (SRAMs)

- This is a semiconductor memory device in which data will be stored permanently.
- Data stored in flip-flops like structure.
- Implemented by BJT or MOSFET.
- It dissipates more power.
- It has low density.
- Operating speed is faster.
- It has fast access time of 5 to 50 ns order.
- No refreshment is required.
- It is a volatile memory.

Circuit diagram and Operation of BJT-RAM or STATIC RAM

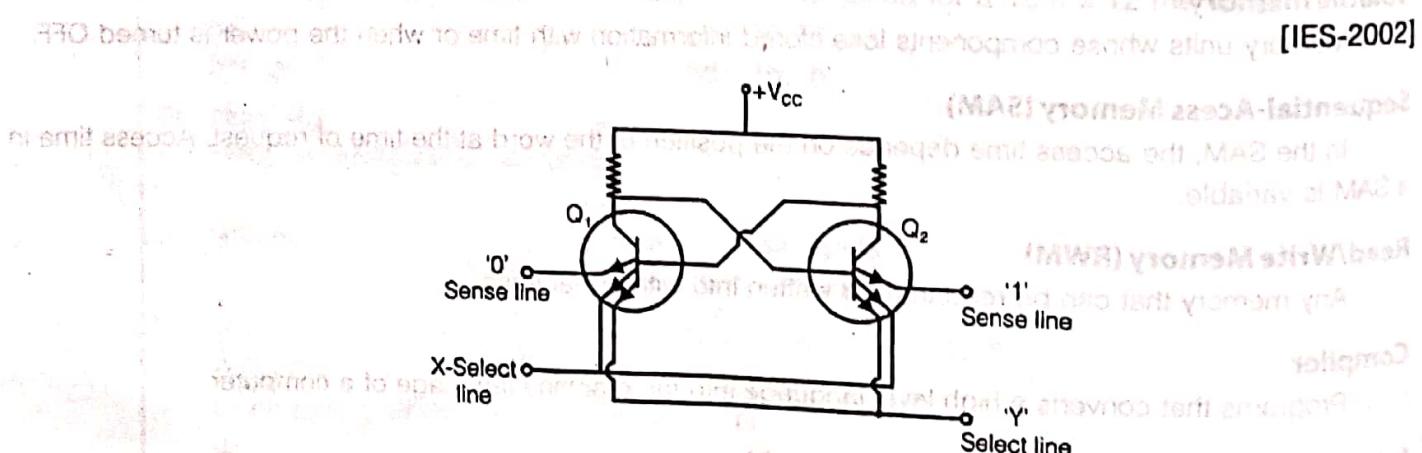


Fig. (10.2)

Storing the data in BJT RAM:

- The cell is first selected by keeping the X-and Y-select lines high.
- To write a '1' at position Y, the '1' sense line is grounded.
- Q_2 goes to saturation and then X and Y select lines are returned to low.
- A '1' is then latched in the cell so that a '1' is written into the cell at position Y.
- To write a '0' in the cell, the '0' sense line is grounded.

Retrieve the data in BJT RAM:

- The '0' and '1' sense lines are grounded.
- If the cell contains '1', then $Y = 1$. Transistor Q_2 goes to the saturation and the current will then be present in the '1' sense line.
- Q_1 remains in the cut-off condition and no current is present in the '0' sense line.
- The READ operation is non-destructive. Once the READ operation has been performed, the contents in the cell remain intact.
- The current present in a particular sense line is then amplified and the bit corresponding to that current will be stored in a shift register.

Note:

In SRAM cells it contains basically 6-BJTs (2 BJT \rightarrow flip-flop structure + 4 BJT \rightarrow control circuit).

Dynamic MOS RAM (DRAM)

- This is a semiconductor memory device in which stored data will not be permanently stored.
- Data is stored in capacitor.
- Implemented by MOSFET.
- It dissipates less power.
- Density is high.
- Operating speed is slower.
- It has less access time of 50 to 100ns order.
- Refreshment is required.
- It is a volatile memory.

Circuit Diagram and Operation of DRAM cells

Figure (10.3) shows the diagram of DRAM cells. The switches S_1 through S_4 are actually MOSFETs that are controlled by various address decoder outputs and R/W signal. The capacitor C of course is the actual storage cell.

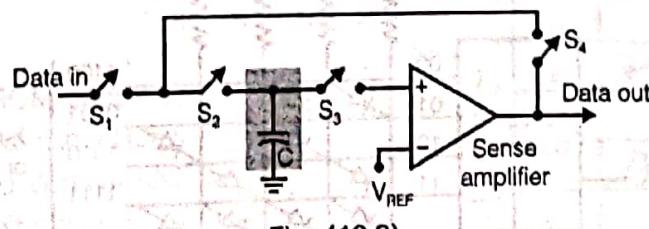
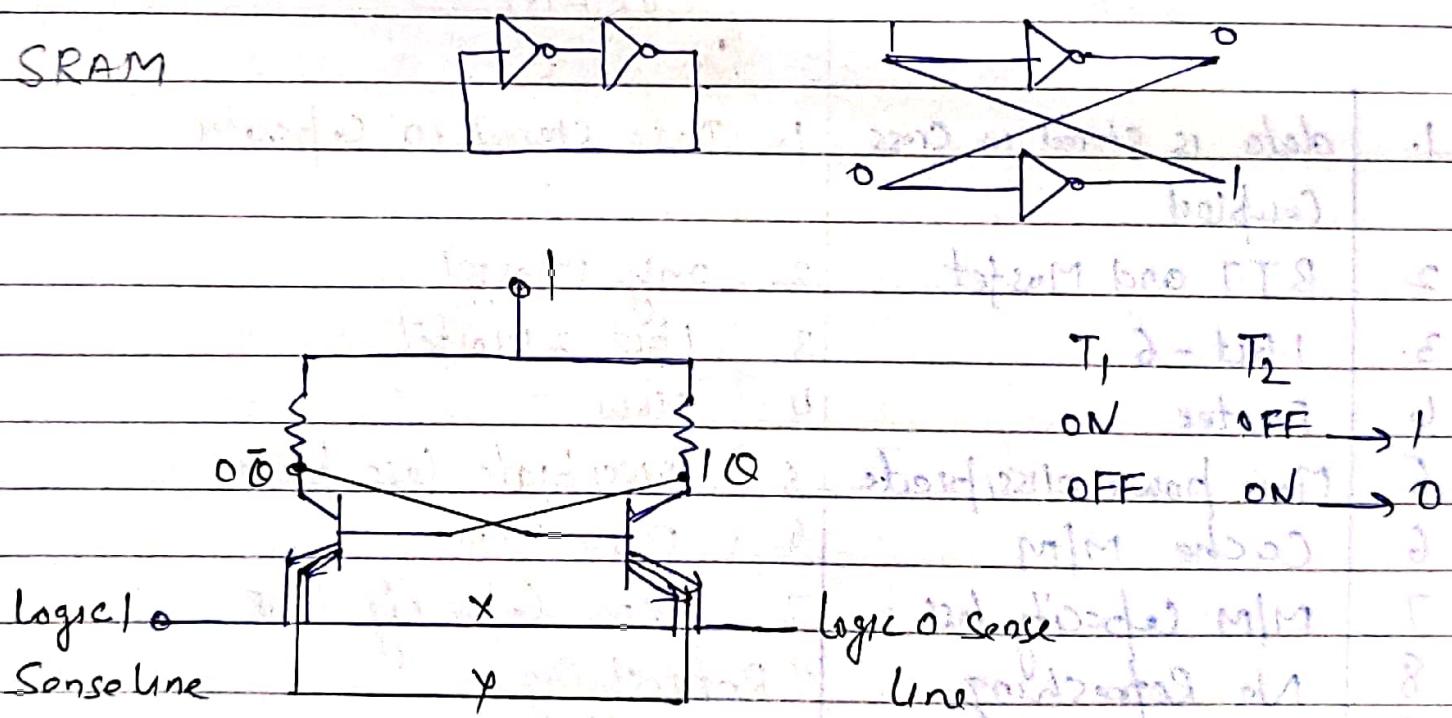
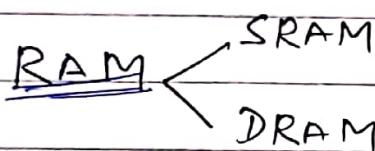
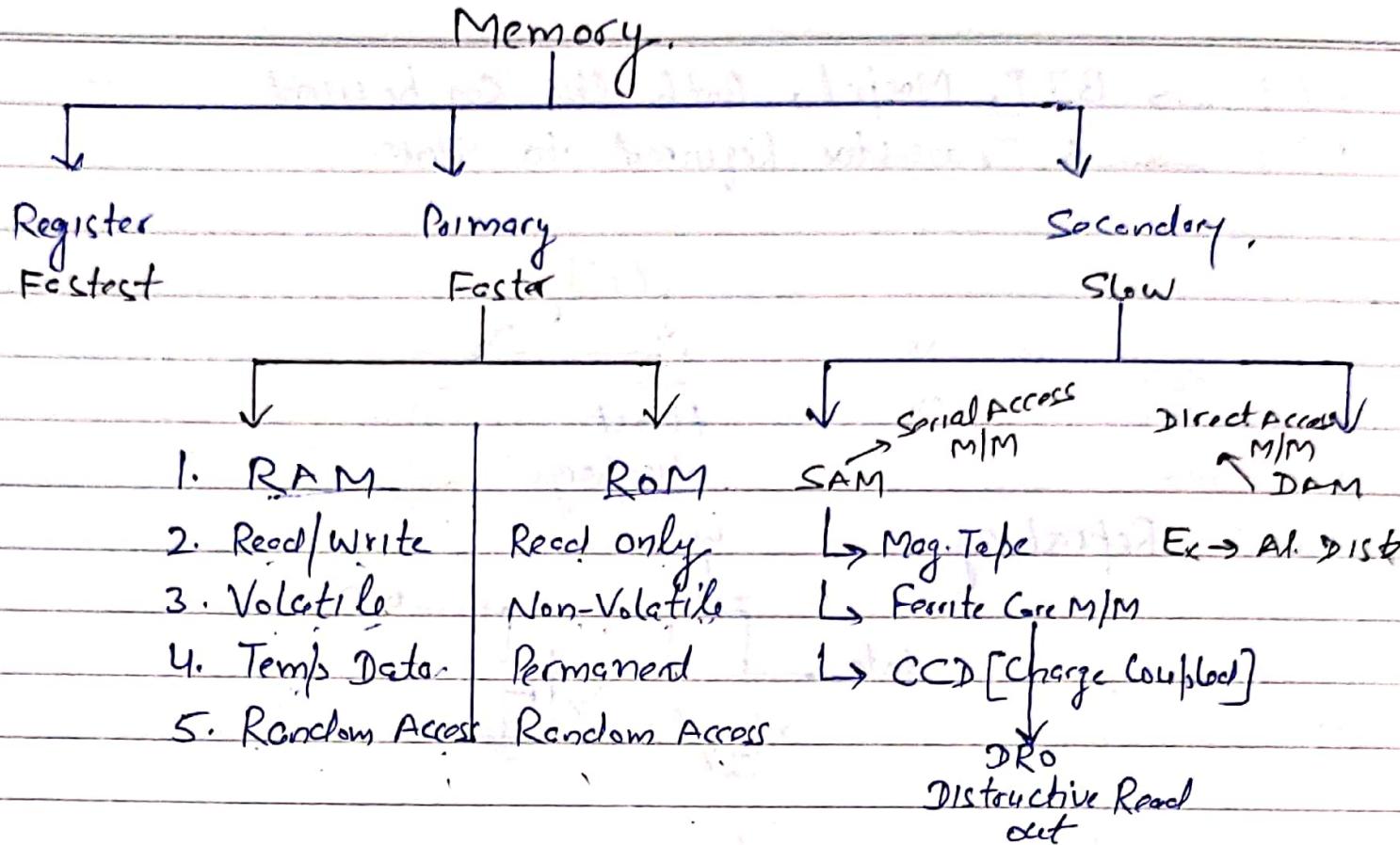


Fig. (10.3)

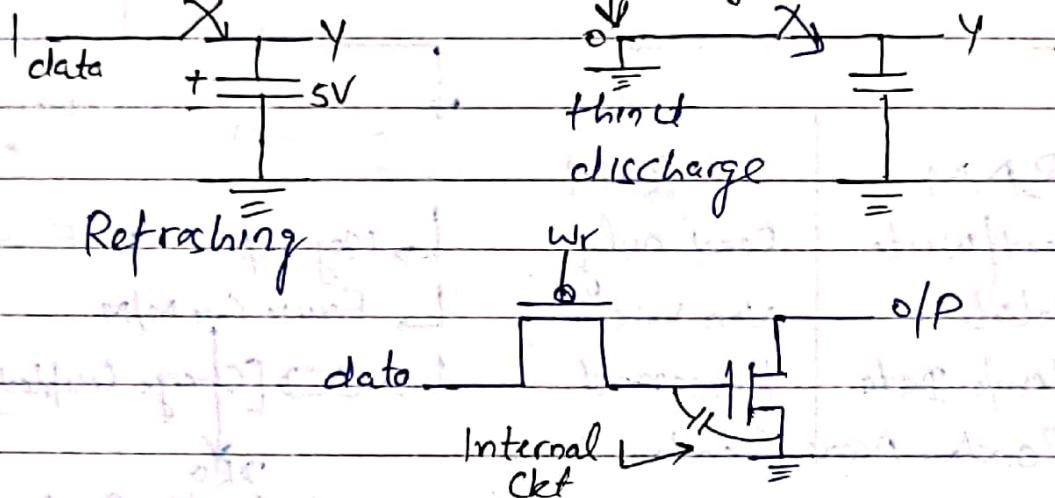
To write data to the cell, signals from the address decoding and read/write logic will close switches S_1 , and S_2 , while keeping S_3 and S_4 open. This connects the input data to C. A logic 1 at the data input charges C, and a logic 0 discharges it.

To read data from the cell, switches S_2 , S_3 , and S_4 are closed and S_1 is kept open. This connects the stored capacitor voltage to the sense amplifier. The sense amplifier compares the voltage with some reference



SRAM → BIT, Mosfet, Both Ckt Can be used
 1 Bit → 6 Transistor Required to store.

Dynamic RAM



Mosfet 1 Bit → 2 Mosfet

	SRAM	DRAM
1.	data is stored in Cross Coupled	1. Data stored in capacitor
2.	BJT and Mosfet	2. only Mosfet
3.	1 Bit - 6	3. 1 bit 2 Mosfet
4.	Faster	4. Slow
5.	More power dissipate	5. Dissipate less power
6.	Cache M/M	6. Main M/M
7.	M/M capacity less	7. M/M capacity More
8.	No Refreshing	8. Refreshing
9.	Volatile	9. Volatile