

8.15 Properties of pn Junction

To explain the properties of an *pn* junction, consider two types of materials; one *p*-type and the other *n*-type as shown in Fig 8.19. In this figure, left side material is a *p*-type semiconductor having *negative acceptor ions and positively charged holes. The right side material is *n*-type semiconductor having **positive donor ions and free electrons.

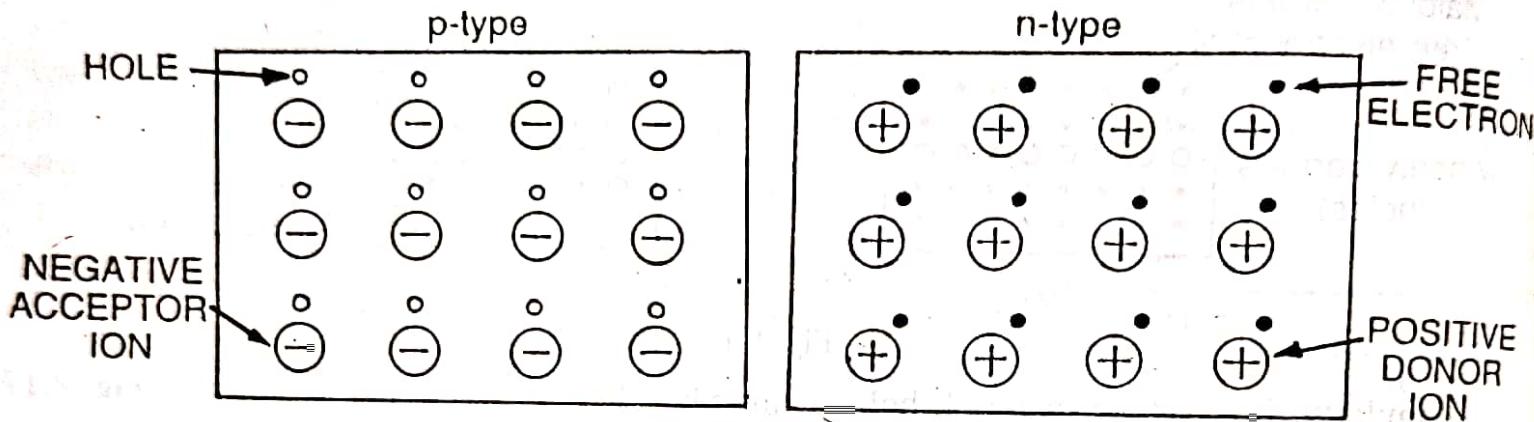


Fig 8.19

Now, suppose the two pieces are suitably treated to form *pn* junction. Keep in mind that *n*-type material has a high concentration of free electrons while *p*-type material has a high concentration of holes. Therefore, at the junction, there is a tendency for the free electrons to diffuse over to the *p*-side and holes to the *n*-side. This process is called diffusion. As the free electrons move across the junction from *n*-type to *p*-type, positive donor ions are uncovered i.e. they are robbed of free electrons. Hence, a positive charge is built on the *n*-side of the junction. At the same time, the free holes cross the junction and uncover the negative acceptor ions by filling in the holes. Therefore, a net negative charge is established on *p*-side of the junction. When a sufficient number of donor and acceptor ions is uncovered, further diffusion is prevented. It is because now positive charge on *n*-side repels holes to cross from *p*-type to *n*-type and negative charge on *p*-side repels free electrons to enter from *n*-type to *p*-type. Thus, a barrier is set up against further movement of charge carriers i.e. holes and electrons. This is called *potential barrier or junction barrier* V_o . The potential barrier is of the order of 0.1 to 0.3 volt. The potential distribution diagram is shown in Fig. 8.20. It is clear from the diagram that a potential barrier V_o is set up which gives rise to electric field. This field prevents the respective majority carriers from crossing the barrier region.

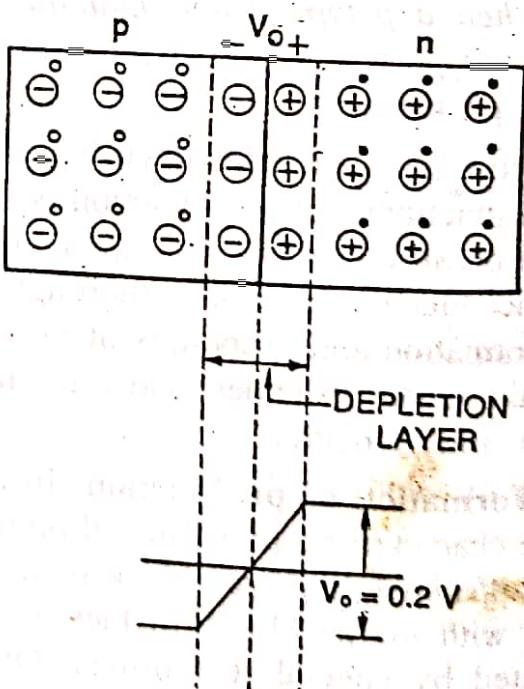


Fig. 8.20

* The acceptor impurity atom is short of one electron. Therefore, it becomes a negative ion.

** The donor impurity atom donates one electron to the crystal and becomes a positive ion.

It should be noted that outside this barrier on each side of the junction, the material is still neutral. Only inside the barrier, there is positive charge on *n*-side and negative charge on *p*-side. This region is called *depletion layer*. It is called so because the mobile charge carriers (*i.e.* free electrons and holes) have been depleted (*i.e.* emptied) in this region.

8.16 Applying Voltage Across pn Junction

The potential difference across a *pn* junction can be applied in two ways, namely; *forward biasing* and *reverse biasing*.

1. Forward biasing. When external voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called **forward biasing**.

To apply forward bias, connect positive terminal of the battery to *p*-type and negative terminal to *n*-type as shown in Fig. 8.21. The applied forward potential establishes an electric field which acts against the field due to potential barrier. Therefore, the resultant field is weakened and the barrier height is reduced at the junction as shown in Fig. 8.21. As potential barrier voltage is very small (0.1 to 0.3 V), therefore, a small forward voltage is sufficient to completely eliminate the barrier. Once the potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero and a low resistance path is established for the entire circuit. Therefore, current flows in the circuit. This is called *forward current*. With forward bias to *pn* junction, the following points are worth noting :-

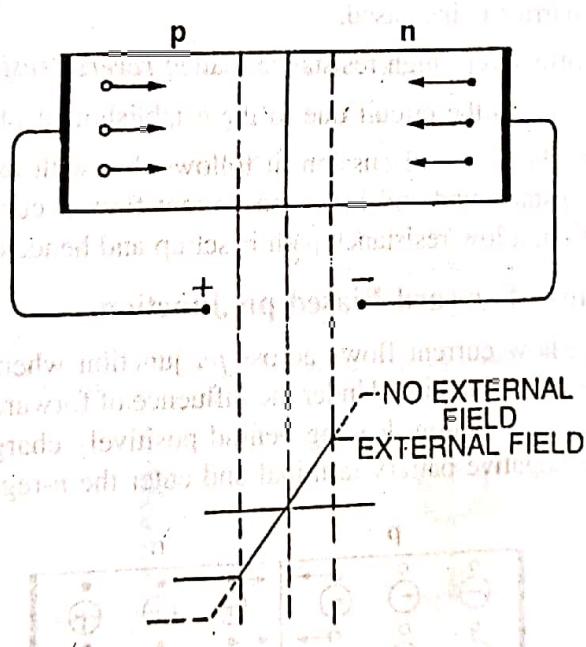


Fig. 8.21

(i) The potential barrier is reduced and at some forward voltage (0.1 to 0.3V), it is eliminated altogether.

(ii) The junction offers low resistance (called *forward resistance*, R_f) to current flow.

(iii) Current flows in the circuit due to the establishment of low resistance path. The magnitude of current depends upon the applied forward voltage.

2. Reverse biasing. When the external voltage applied to the junction is in such a direction that potential barrier is increased, it is called **reverse biasing**.

To apply reverse bias, connect negative terminal of the battery to *p*-type and positive terminal to *n*-type as shown in Fig. 8.22. It is clear that applied reverse voltage establishes an electric field which acts in the same direction as the field due to potential barrier. Therefore, the resultant field at the junction is strengthened and the barrier height is increased as shown in Fig.

8.22. The increased potential barrier prevents the flow of charge carriers across the junction. Thus, a high resistance path is established for the entire circuit and hence the current does not flow. With reverse bias to *pn* junction, the following points are worth noting :-

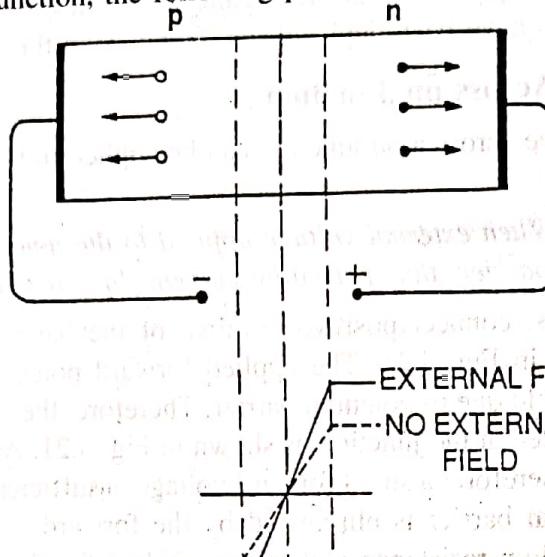


Fig. 8.22

- (i) The potential barrier is increased.
- (ii) The junction offers very high resistance (called *reverse resistance* R_r) to current flow.
- (iii) No current flows in the circuit due to the establishment of high resistance path.

Conclusion. From the above discussion, it follows that with reverse bias to the junction, a high resistance path is established and hence no current flow occurs. On the other hand, with forward bias to the junction, a low resistance path is set up and hence current flows in the circuit.

8.17 Current Flow in a Forward Biased pn Junction

We shall now see how current flows across *pn* junction when it is forward biased. Fig. 8.23 shows a forward biased *pn* junction. Under the influence of forward voltage, the free electrons in *n*-type move *towards the junction, leaving behind positively charged atoms. However, more electrons arrive from the negative battery terminal and enter the *n*-region to take up their places.

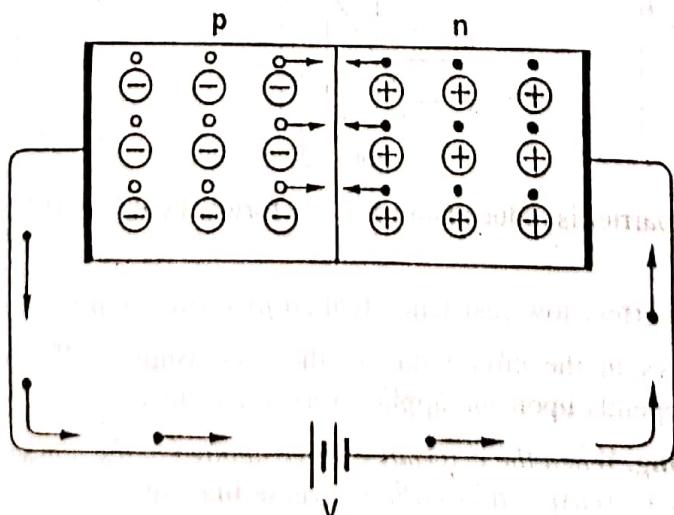


Fig. 8.23

* Note that negative terminal of battery is connected to *n*-type. It repels the free electrons in *n*-type towards the junction.

As the free electrons reach the junction, they become *valence electrons. As valence electrons, they move through the holes in the *p*-region. The valence electrons move towards left in the *p*-region which is equivalent to the holes moving to right. When the valence electrons reach the left end of the crystal, they flow into the positive terminal of the battery.

The mechanism of current flow in a forward biased *pn* junction can be summed up as under :

(i) The free electrons from the negative terminal continue to pour into the *n*-region while the free electrons in the *n*-region move towards the junction.

(ii) The electrons travel through the *n*-region as free-electrons i.e. current in *n*-region is by free electrons.

(iii) When these electrons reach the junction, they combine with holes and become valence electrons.

(iv) The electrons travel through *p*-region as valence electrons i.e. current in the *p*-region is by holes.

(v) When these valence electrons reach the left end of crystal, they flow into the positive terminal of the battery.

From the above discussion, it is concluded that in *n*-type region, current is carried by free electrons whereas in *p*-type region, it is carried by holes. However, in the external connecting wires, the current is carried by electrons.

8.18 Volt-Ampere Characteristics of pn Junction

Volt-ampere or *V-I* characteristic of a *pn* junction (also called a *crystal or semiconductor diode*) is the curve between voltage across the junction and the circuit current. Usually, voltage is taken along *x*-axis and current along *y*-axis. Fig. 8.24 shows the **circuit arrangement for determining the *V-I* characteristics of a *pn* junction. The characteristics can be studied under three heads, namely; zero external voltage, forward bias and reverse bias.

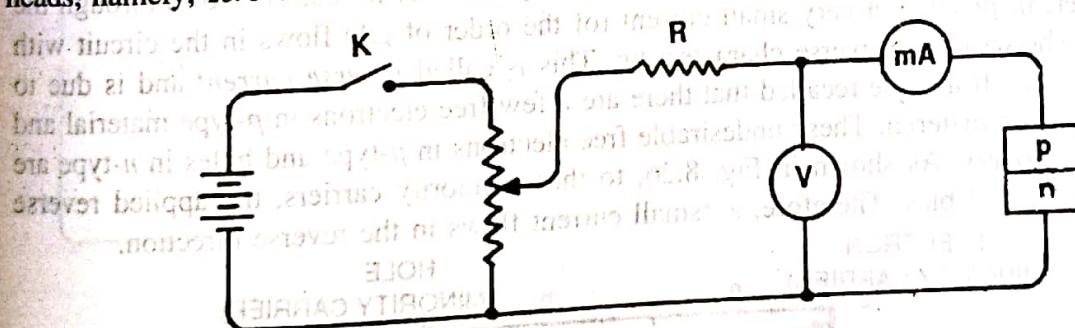


Fig. 8.24

(i) **Zero external voltage.** When the external voltage is zero, i.e. circuit is open at *K*, the potential barrier at the junction does not permit current flow. Therefore, the circuit current is zero as indicated by point *O* in Fig. 8.25.

(ii) **Forward bias.** With forward bias to the *pn* junction i.e., *p*-type connected to positive terminal and *n*-type connected to negative terminal, the potential barrier is reduced. At some forward voltage (0.7V for Si and 0.3V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit. From now onwards, the current increases with the increase in forward voltage. Thus, a rising curve *OB* is obtained with forward bias as shown in Fig. 8.25. From the forward characteristic, it is seen that at first (*region OA*), the current increases very

* A hole is in the co-valent bond. When a free electron combines with a hole, it becomes a valence electron.

** *R* is the current limiting resistance. It prevents the forward current from exceeding the permitted value.

slowly and the curve is non-linear. It is because the external applied voltage is used up in overcoming the potential barrier. However, once the external voltage exceeds the potential barrier voltage, the *pn* junction behaves like an ordinary conductor. Therefore, the current rises very sharply with increase in external voltage (*region AB* on the curve). The curve is almost linear.

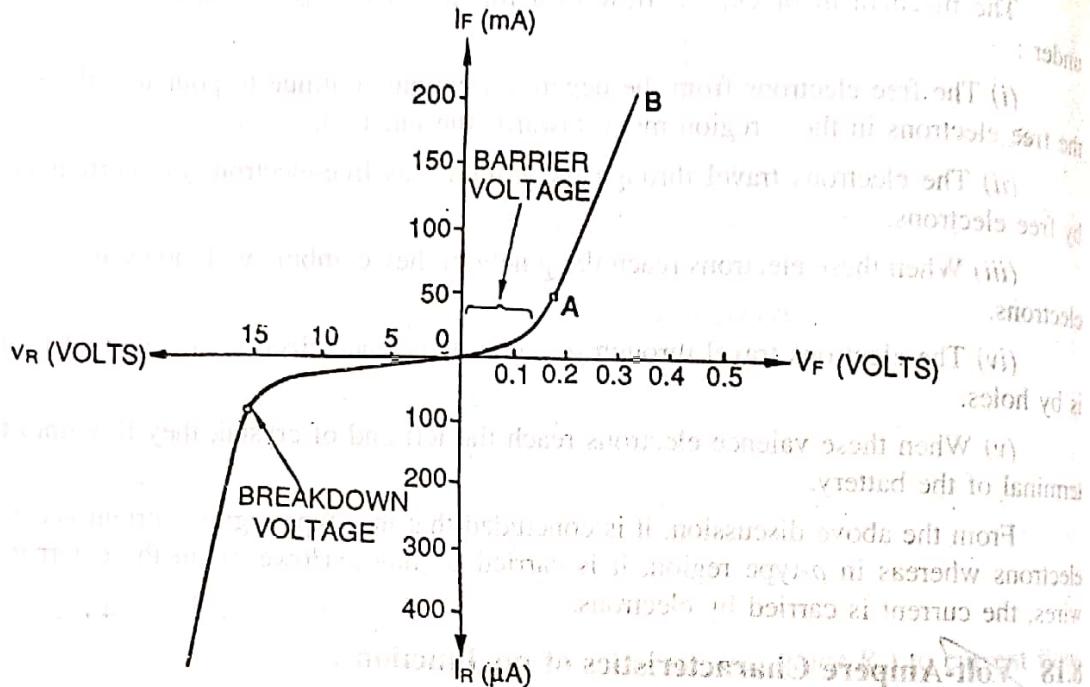


Fig. 8.25. Current-voltage characteristic of a *pn* junction.

(iii) **Reverse bias.** With reverse bias to the *pn* junction i.e. *p*-type connected to negative terminal and *n*-type connected to positive terminal, potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and practically no current flows through the circuit. However, in practice, a very small current (of the order of μA) flows in the circuit with reverse bias as shown in the reverse characteristic. This is called *reverse current* and is due to the minority carriers. It may be recalled that there are a few free electrons in *p*-type material and a few holes in *n*-type material. These undesirable free electrons in *p*-type and holes in *n*-type are called *minority carriers*. As shown in Fig. 8.26, to these minority carriers, the applied reverse bias appears as forward bias. Therefore, a *small current flows in the reverse direction.

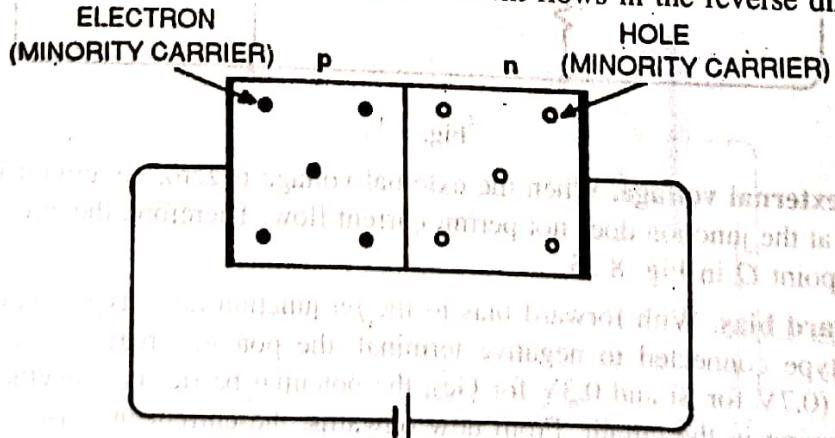


Fig. 8.26. Effect of reverse bias on minority carriers.

* Reverse current increases with reverse voltage but can generally be regarded as negligible over the working range of voltages.

If reverse voltage is increased continuously, the kinetic energy of electrons (minority carriers) may become high enough to knock out electrons from the semiconductor atoms. At this stage *breakdown* of the junction occurs, characterised by a sudden rise of reverse current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

Note. The forward current through a *pn* junction is due to the *majority carriers* produced by the impurity. However, reverse current is due to the *minority carriers* produced due to breaking of some co-valent bonds at room temperature.

8.19 Important Terms

Two important terms often used with *pn* junction (*i.e.* crystal diode) are *breakdown voltage* and *knee voltage*. We shall now explain these two terms in detail.

(i) **Breakdown voltage.** *It is the reverse voltage at which *pn* junction breaks down with sudden rise in reverse current.*

Under normal reverse voltage, a very little reverse current flows through a *pn* junction. However, if the reverse voltage attains a high value, the junction may breakdown with sudden rise in reverse current. For understanding this point, refer to Fig. 8.27. Even at room temperature, some hole-electron pairs (minority carriers) are produced in the depletion layer as shown in Fig. 8.27 (i). With reverse bias, the electrons move towards the positive terminal of supply. At large reverse voltage, these electrons acquire high enough velocities to dislodge valence electrons from semiconductor atoms as shown in Fig. 8.27 (ii). The newly liberated electrons in turn free other valence electrons. In this way, we get an *avalanche* of free electrons. Therefore, the *pn* junction conducts a very large reverse current.

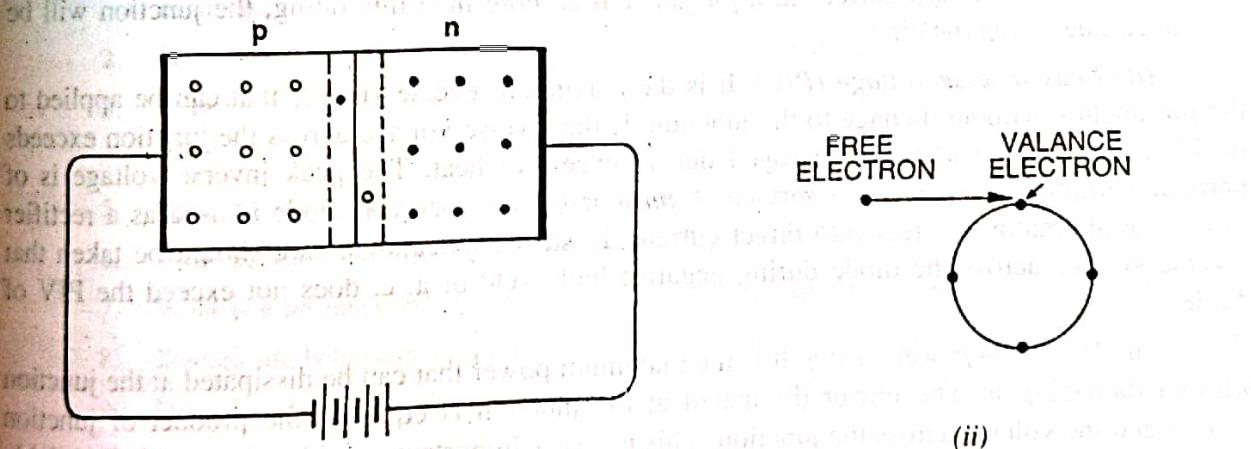


Fig. 8.27

Once the breakdown voltage is reached, the high reverse current may damage the junction. Therefore, care should be taken that reverse voltage across a *pn* junction is always less than the breakdown voltage.

(ii) **Knee voltage.** *It is the forward voltage at which the current through the junction starts to increase rapidly.*

When a diode is forward biased, it conducts current very slowly until we overcome the potential barrier. For silicon *pn* junction, potential barrier is 0.7 V whereas it is 0.3 V for germanium junction. It is clear from Fig. 8.28 that knee voltage for silicon diode is 0.7V and 0.3V for germanium diode.

Once the applied forward voltage exceeds the knee voltage, the current starts increasing rapidly. It may be added here that in order to get useful current through a *pn* junction, the applied voltage must be more than the knee voltage.

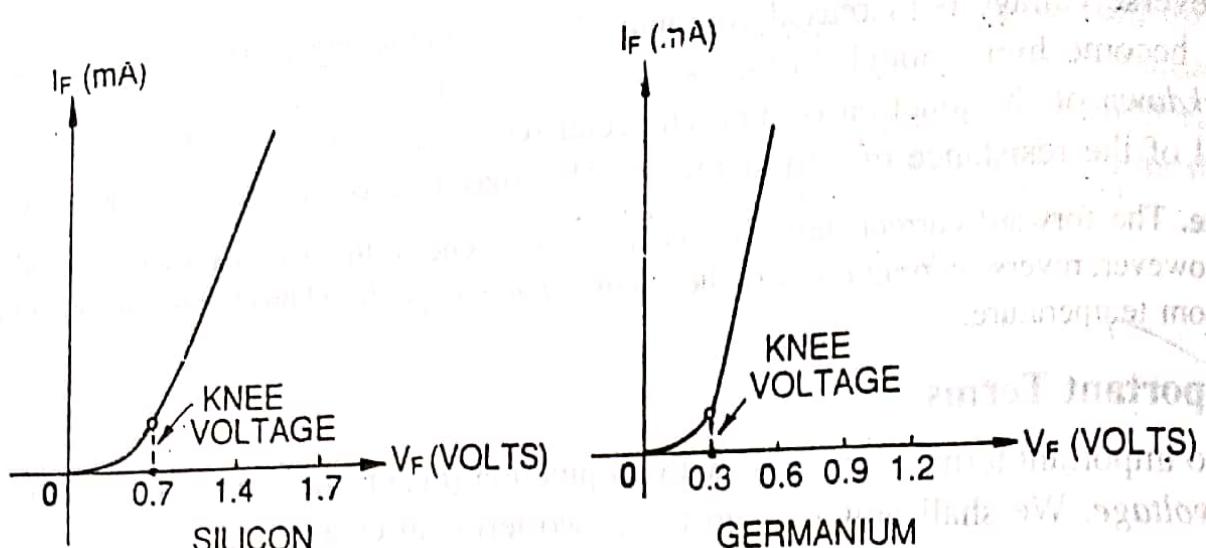


Fig. 8.28

Note. The potential barrier voltage is also known as *turn-on voltage*. This is obtained by taking the straight line portion of the forward characteristic and extending it back to the horizontal axis.

8.20 Limitations in the Operating Conditions of pn Junction

Every *pn* junction has limiting values of *maximum forward current*, *peak inverse voltage* and *maximum power rating*. The *pn* junction will give satisfactory performance if it is operated within these limiting values. However, if these values are exceeded, the *pn* junction may be destroyed due to excessive heat.

(i) *Maximum forward current*. It is the highest instantaneous forward current that a *pn* junction can conduct without damage to the junction. Manufacturers' data sheet usually specifies this rating. If the forward current in a *pn* junction is more than this rating, the junction will be destroyed due to overheating.

(ii) *Peak inverse voltage (PIV)*. It is the maximum reverse voltage that can be applied to the *pn* junction without damage to the junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier service. A *pn* junction i.e. a crystal diode is used as a rectifier to change alternating current into direct current. In such applications, care should be taken that reverse voltage across the diode during negative half-cycle of a.c. does not exceed the PIV of diode.

(iii) *Maximum power rating*. It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated at the junction is equal to the product of junction current and the voltage across the junction. This is a very important consideration and is invariably specified by the manufacturer in the data sheet.

TRANSISTORS

BJT (Bipolar Junction Transistor)

Introduction

When a third doped element is added to a crystal diode in such a way that two *pn* junctions are formed, the resulting device is known as a *transistor*. The transistor—an entirely new type of electronic device—is capable of achieving amplification of weak signals in a fashion comparable and often superior to that realised by vacuum tubes. Transistors are far smaller than vacuum tubes, have no filament and hence need no heating power and may be operated in any position. They are mechanically strong, have practically unlimited life and can do some jobs better than vacuum tubes.

Invented in 1948 by J. Bardeen and W.H. Brattain of Bell Telephone Laboratories, U.S.A.; transistor has now become the heart of most electronic applications. Though transistor is only slightly more than 45 years old, yet it is fast replacing vacuum tubes in almost all applications. In this chapter, we shall focus our attention on the various aspects of transistors and their increasing applications in the fast developing electronics industry.

10.1 Transistor

A **transistor** consists of two *pn* junctions formed by *sandwiching either *p*-type or *n*-type semiconductor between a pair of opposite types. Accordingly, there are two types of transistors, namely;

- (i) *n-p-n* transistor (ii) *p-n-p* transistor

An *n-p-n* transistor is composed of two *n*-type semiconductors separated by a thin section of *p*-type as shown in Fig. 10.1 (i). However, a *p-n-p* transistor is formed by two *p*-sections separated by a thin section of *n*-type as shown in Fig. 10.1 (ii).

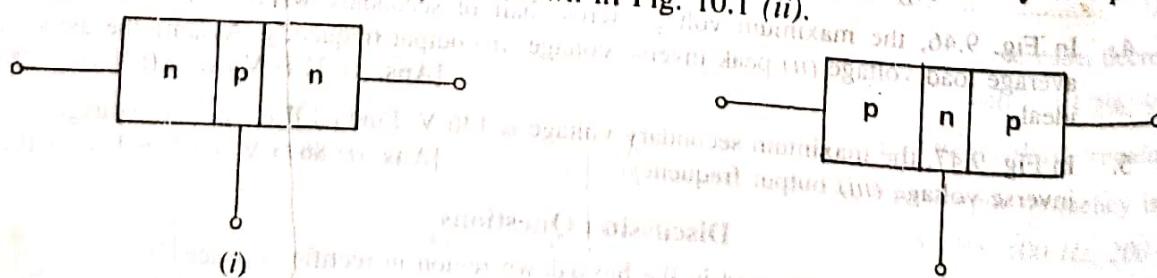


Fig. 10.1

* In practice, these three blocks *p*, *n*, *p* are grown out of the same crystal by adding corresponding impurities in turn.

(In each type of transistor, the following points may be noted :-

(i) These are two *pn* junctions. Therefore, a transistor may be regarded as a combination of two diodes connected back to back.

(ii) There are three terminals, taken from each type of semiconductor.

(iii) The middle section is a very thin layer. This is the most important factor in the function of a transistor.

Origin of the name "Transistor". When new devices are invented, scientists often try to devise a name that will appropriately describe the device. A transistor has two *pn* junctions. As discussed later, one junction is forward biased and the other is reverse biased. The forward biased junction has a low resistance path whereas a reverse biased junction has a high resistance path. The weak signal is introduced in the low resistance circuit and output is taken from the high resistance circuit. Therefore, a transistor *transfers* a signal from a low resistance to high resistance. The prefix 'trans' means the signal transfer property of the device while 'istor' classifies it as a solid element in the same general family with resistors.

10.2 Naming the Transistor Terminals

A transistor (*pnp* or *npn*) has three sections of doped semiconductors. The section on one side is the *emitter* and the section on the opposite side is the *collector*. The middle section is called the *base* and forms two junctions between the emitter and collector.

(i) **Emitter.** The section on one side that supplies charge carriers (electrons or holes) is called the *emitter*. The *emitter* is always forward biased w.r.t. *base* so that it can supply a large number of *majority carriers. In Fig. 10.2 (i), the emitter (*p*-type) of *pnp* transistor is forward biased and supplies hole charges to its junction with the base. Similarly, in Fig. 10.2 (ii), the emitter (*n*-type) of *npn* transistor has a forward bias and supplies free electrons to its junction with the base.

(ii) **Collector.** The section on the other side that collects the charges is called the *collector*. The *collector* is always reverse biased. Its function is to remove charges from its junction with the base. In Fig. 10.2 (i), the collector (*p*-type) of *pnp* transistor has a reverse bias and receives hole charges that flow in the output circuit. Similarly, in Fig. 10.2 (ii), the collector (*n*-type) of *npn* transistor has reverse bias and receives electrons.

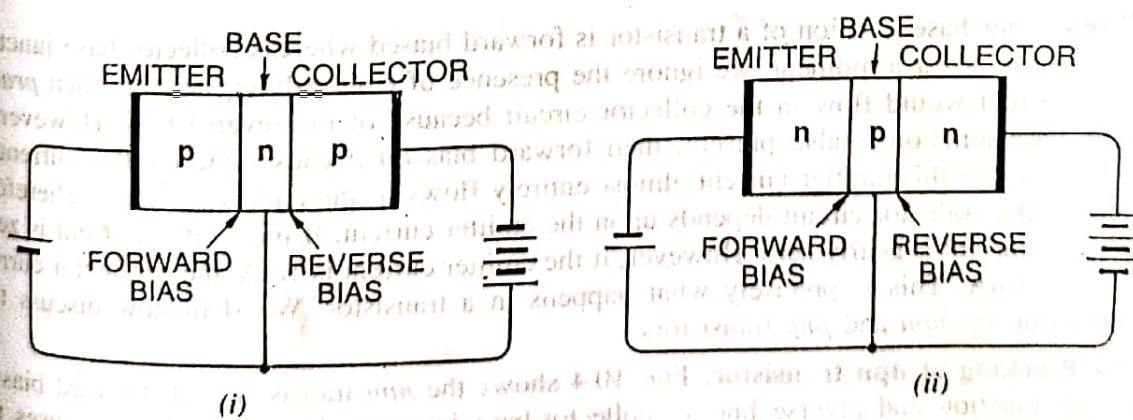


Fig. 10.2

(iii) **Base.** The middle section which forms two *pn*-junctions between the emitter and collector is called the *base*. The base-emitter junction is forward biased, allowing low resistance for the emitter circuit. The base-collector junction is reverse biased and provides high resistance in the collector circuit.

* Holes if emitter is *p*-type and electrons if the emitter is *n*-type.

10.3 Some Facts about the Transistor

Before discussing transistor action, it is important that the reader may keep in mind the following facts about the transistor :

(i) The transistor has three regions, namely ; *emitter*, *base* and *collector*. The base is much thinner than the emitter while collector is wider than both as shown in Fig. 10.3. However, for the sake of convenience, it is customary to show emitter and collector to be of equal size.

(ii) The emitter is heavily doped so that it can inject a large number of charge carriers (electrons or holes) into the base. The base is lightly doped and very thin; it passes most of the emitter injected charge carriers to the collector. The collector is moderately doped.

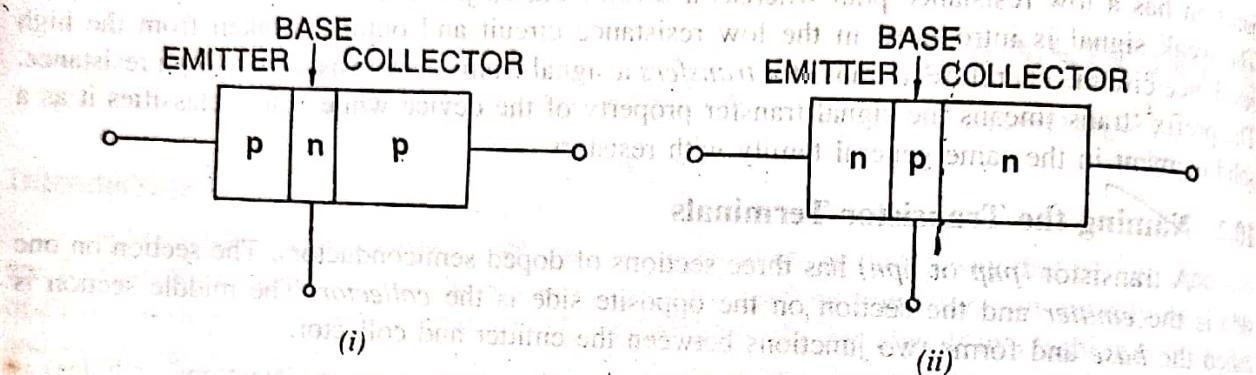


Fig. 10.3

(iii) The transistor has two *pn* junctions i.e. it is like two diodes. The junction between emitter and base may be called *emitter-base diode* or simply the *emitter diode*. The junction between the base and collector may be called *collector-base diode* or simply *collector diode*.

(iv) The emitter diode is always forward biased whereas collector diode is always reverse biased.

(v) The resistance of emitter diode (forward biased) is very small as compared to collector diode (reverse biased). Therefore, forward bias applied to the emitter diode is generally very small whereas reverse bias on the collector diode is much higher.

10.4 Transistor Action

The emitter-base junction of a transistor is forward biased whereas collector-base junction is reverse biased. If for a moment, we ignore the presence of emitter-base junction, then practically** no current would flow in the collector circuit because of the reverse bias. However, if the emitter-base junction is also present, then forward bias on it causes the emitter current to flow. It is seen that this emitter current almost entirely flows in the collector circuit. Therefore, the current in the collector circuit depends upon the emitter current. If the emitter current is zero, then collector current is nearly zero. However, if the emitter current is 1mA, then collector current is also about 1mA. This is precisely what happens in a transistor. We shall now discuss this transistor action for *npn* and *pnp* transistors.

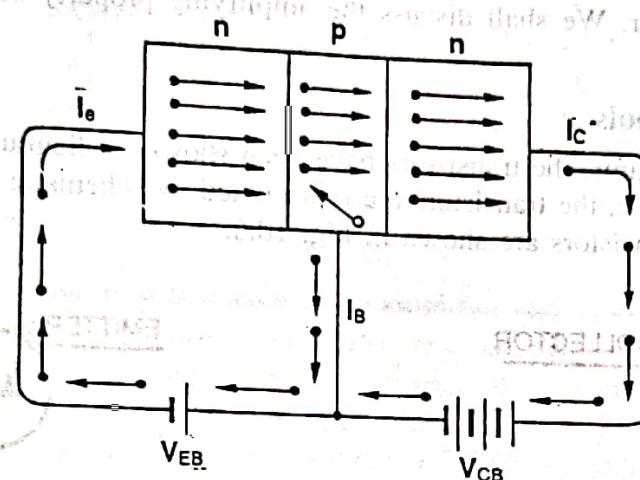
(i) **Working of *npn* transistor.** Fig. 10.4 shows the *npn* transistor with forward bias to emitter-base junction and reverse bias to collector-base junction. The forward bias causes the electrons in the *n*-type emitter to flow towards the base. This constitutes the emitter current I_E . As these electrons flow through the *p*-type base, they tend to combine with holes. As the base

* During transistor operation, much heat is produced at the collector junction. The collector is made larger to dissipate the heat.

** In actual practice, a very little current (a few μ A) would flow in the collector circuit. This is called collector cut off current and is due to minority carriers.

is lightly doped and very thin, therefore, only a few electrons (less than 5%) combine with holes to constitute base* current I_B . The remainder (**more than 95%) cross over into the collector region to constitute collector current I_C . In this way, almost the entire emitter current flows in the collector circuit. It is clear that emitter current is the sum of collector and base currents i.e.

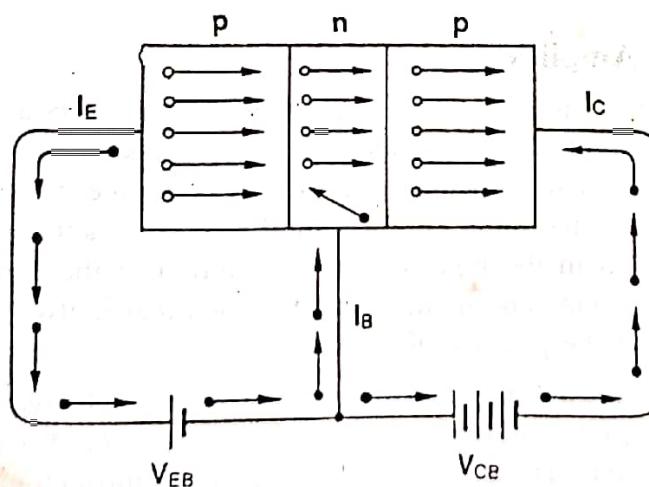
$$I_E = I_B + I_C$$



Basic connection of npn transistor

Fig. 10.4

(ii) Working of pnp transistor. Fig. 10.5 shows the basic connection of a pnp transistor. The forward bias causes the holes in the p-type emitter to flow towards the base. This constitutes the emitter current I_E . As these holes cross into n-type base, they tend to combine with the electrons. As the base is lightly doped and very thin, therefore, only a few holes (less than 5%) combine with the electrons. The remainder (more than 95%) cross into the collector region to constitute collector current I_C . In this way, almost the entire emitter current flows in the collector circuit. It may be noted that current conduction within pnp transistor is by holes. However, in the external connecting wires, the current is still by electrons.



Basic connection of pnp transistor

Fig. 10.5

* The electrons which combine with holes become valence electrons. Then as valence electrons, they flow down through holes and into the external base lead. This constitutes base current I_B .

** The reasons that most of the electrons from emitter continue their journey through the base to collector to form collector current are : (i) The base is lightly doped and very thin. Therefore, there are a few holes which find enough time to combine with electrons. (ii) The reverse bias on collector is quite high and exerts attractive forces on these electrons.

Importance of transistor action. The input circuit (*i.e.* emitter-base junction) has low resistance because of forward bias whereas output circuit (*i.e.* collector-base junction) has high resistance due to reverse bias. As we have seen, the input emitter current almost entirely flows in the collector circuit. Therefore, a transistor transfers the input signal current from a low-resistance circuit to a high-resistance circuit. This is the key factor responsible for the amplifying capability of the transistor. We shall discuss the amplifying property of transistor later in this chapter.

10.5 Transistor Symbols

In the earlier diagrams, the transistors have been shown in diagrammatic form. However, for the sake of convenience, the transistors are represented by schematic diagrams. The symbols used for *npn* and *pnp* transistors are shown in Fig. 10.6.

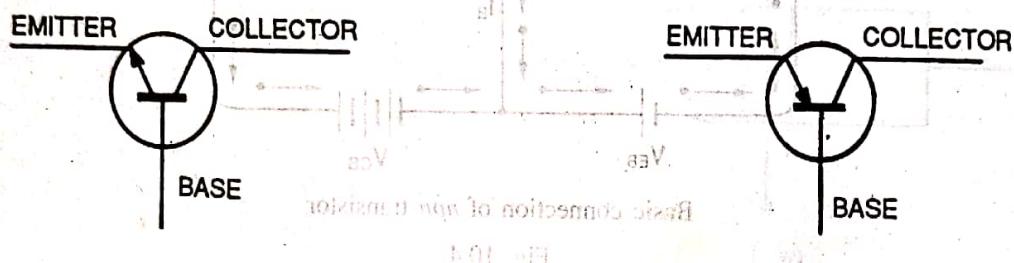


Fig. 10.6

Note that emitter is shown by an arrow which indicates the direction of conventional current flow with forward bias. Checking (see Fig. 10.4) for the *npn* connection, it is clear that electrons flow into the emitter. This means that conventional current flows out of the emitter as indicated by the outgoing arrow in Fig. 10.6 (i). Similarly, it can be seen that for *pnp* connection (see Fig. 10.5), the conventional current flows into the emitter as indicated by the inward arrow in Fig. 10.6 (ii).

10.6 Transistor as an Amplifier

A transistor raises the strength of a weak signal and thus acts as an amplifier. Fig. 10.7 shows the basic circuit of a transistor amplifier. The weak signal is applied between emitter-base junction and output is taken across the load R_C connected in the collector circuit. In order to achieve faithful amplification, the input circuit should always remain forward biased. To do so, a d.c. voltage V_{EE} is applied in the input circuit in addition to the signal as shown. This d.c. voltage is known as bias* voltage and its magnitude is such that it always keeps the input circuit forward biased regardless of the polarity of the signal.

As the input circuit has low resistance, therefore, a small change in signal voltage causes an appreciable change in emitter current. This causes almost the **same change in collector current due to transistor action. The collector current flowing through a high load resistance R_C

* It may be recalled that biasing is also necessary in vacuum tube amplifiers for faithful amplification (see Chapter 5). The reader may find the detailed discussion on transistor biasing in Chapter 11.

** The reason is as follows. The collector-base junction is reverse biased and has a very high resistance—of the order of mega ohms. Thus collector-base voltage has little effect on the collector current. This means that a large resistance R_C can be inserted in series with collector without disturbing the collector current relation to the emitter current *viz.* $I_C = \alpha I_E + I_{CBO}$. Therefore, collector current variations caused by a small base-emitter voltage fluctuations result in voltage changes in R_C that are quite high—often hundreds of times larger than the emitter-base voltage.

produces a large voltage across it. Thus, a weak signal applied in the input circuit appears in the amplified form in the collector circuit. It is in this way that a transistor acts as an amplifier.

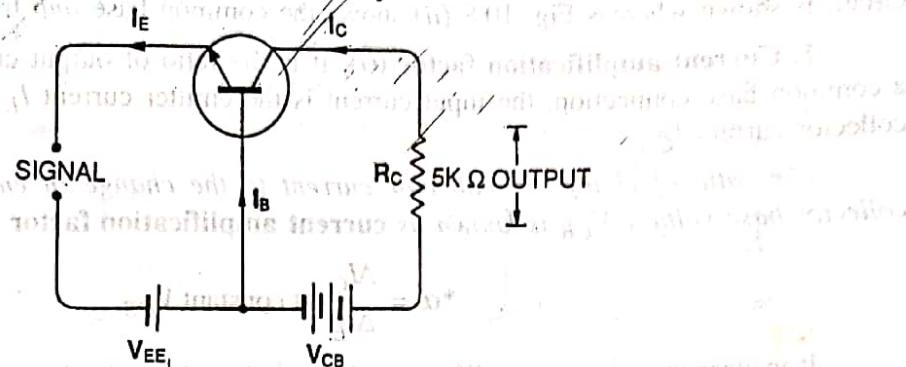


Fig. 10.7

Illustration. The action of a transistor as an amplifier can be made more illustrative if we consider typical circuit values. Suppose collector load resistance $R_C = 5\text{ k}\Omega$. Let us further assume that a change of 0.1V in signal voltage produces a change of 1mA in emitter current. Obviously, the change in collector current would also be approximately 1mA . This collector current flowing through collector load R_C would produce a voltage $= 5\text{ k}\Omega \times 1\text{ mA} = 5\text{V}$. Thus, a change of 0.1V in the signal has caused a change of 5V in the output circuit. In other words, the transistor has been able to raise the voltage level of the signal from 0.1V to 5V i.e. voltage amplification is 50.

10.7 Transistor Connections

There are three leads in a transistor viz emitter, base and collector terminals. However, when a transistor is to be connected in a circuit, we require four terminals; two for the input and two for the output. This difficulty is overcome by making one terminal of the transistor common to both input and output terminals. The input is fed between this common terminal and one of the other two terminals. The output is obtained between the common terminal and the remaining terminal. Accordingly; a transistor can be connected in a circuit in the following three ways;

- (i) common base connection
- (ii) common emitter connection
- (iii) common collector connection

Each circuit connection has specific advantages and disadvantages. It may be noted here that regardless of circuit connection, the emitter is always biased in the forward direction, while the collector always has a reverse bias.

10.8 Common Base Connection

In this circuit arrangement, input is applied between emitter and base and output is taken from collector and base. Here, base of the transistor is common to both input and output circuits

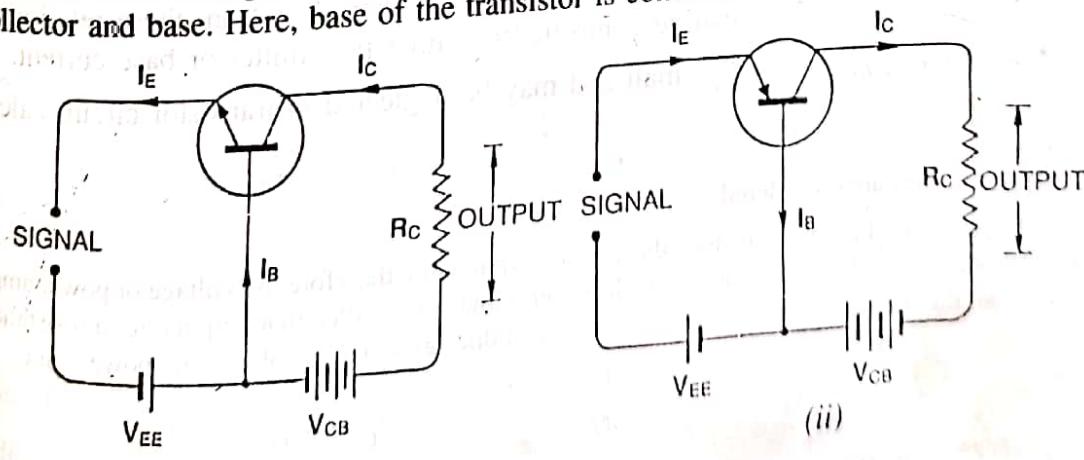


Fig. 10.8

and hence the name common base connection. In Fig. 10.8 (i), a common base *npn* transistor circuit is shown whereas Fig. 10.8 (ii) shows the common base *pnp* transistor circuit.

1. Current amplification factor (α). It is the ratio of output current to input current. In a common base connection, the input current is the emitter current I_E and output current is the collector current I_C .

The ratio of change in collector current to the change in emitter current at constant collector-base voltage V_{CB} is known as **current amplification factor** i.e.

$$*\alpha = \frac{\Delta I_C}{\Delta I_E} \text{ at constant } V_{CB}$$

It is clear that current amplification factor is less than **unity. This value can be increased (but not more than unity) by decreasing the base current. This is achieved by making the base thin and doping it lightly. Practical values of α in commercial transistors range from 0.9 to 0.99.

2. Expression for collector current. The whole of emitter current does not reach the collector. It is because a small percentage of it, as a result of electron-hole combinations occurring in base area, gives rise to base current. Moreover, as the collector-base junction is reverse biased, therefore, some leakage current flows due to minority carriers. It follows therefore that total collector current consists of :

(i) That part of emitter current which reaches the collector terminal i.e. *** αI_E

(ii) The leakage current $I_{leakage}$. This current is due to the movement of minority carriers across base-collector junction on account of it being reverse biased. This is generally much smaller than αI_E .

∴ Total collector current, $I_C = \alpha I_E + I_{leakage}$

It is clear that if $I_E = 0$ (i.e. emitter circuit is open), a small leakage current still flows in the collector circuit. This $I_{leakage}$ is abbreviated as I_{CBO} , meaning collector-base current with emitter open.

$$\therefore I_C = \alpha I_E + I_{CBO} \quad \dots (i)$$

Now

$$I_E = I_C + I_B$$

$$\therefore I_C = \alpha(I_C + I_B) + I_{CBO} \quad \dots (ii)$$

or

$$I_C(1 - \alpha) = \alpha I_B + I_{CBO}$$

or

$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{I_{CBO}}{1 - \alpha} \quad \dots (iii)$$

Relation (i) or (ii) can be used to find I_C . It is further clear from these relations that the collector current of a transistor can be controlled by either the emitter or base current.

The current I_{CBO} is usually small and may be neglected in transistor circuit calculations.

* If only d.c. values are considered, then $\alpha = I_C / I_E$

** At first sight, it might seem that since there is no current gain, therefore, no voltage or power amplification could be possible with this arrangement. However, it may be recalled that output circuit resistance is much higher than the input circuit resistance. Therefore, it does give rise to voltage and power gain.

$$\alpha = \frac{I_C}{I_E} \quad \therefore I_C = \alpha I_E$$

In other words, αI_E part of emitter current reaches the collector terminal

Applying Kirchhoff's voltage law to the collector-side loop, we have,

$$V_{CC} = I_C R_C + V_{CB}$$

$$\therefore V_{CB} = V_{CC} - I_C R_C = 18 \text{ V} - 4.8 \text{ mA} \times 1.2 \text{ K}\Omega = 12.16 \text{ V}$$

10.9 Characteristics of Common Base Connection

The complete electrical behaviour of a transistor can be described by stating the interrelation of the various currents and voltages. These relationships can be conveniently displayed graphically and the curves thus obtained are known as the characteristics of transistor. The most important characteristics of common base connection are *input characteristics* and *output characteristics*.

1. Input characteristics. It is the curve between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB} . The emitter current is generally taken along y -axis and emitter-base voltage along x -axis. Fig. 10.12 shows the input characteristics of a typical transistor in *CB* arrangement. The following points may be noted from these characteristics:

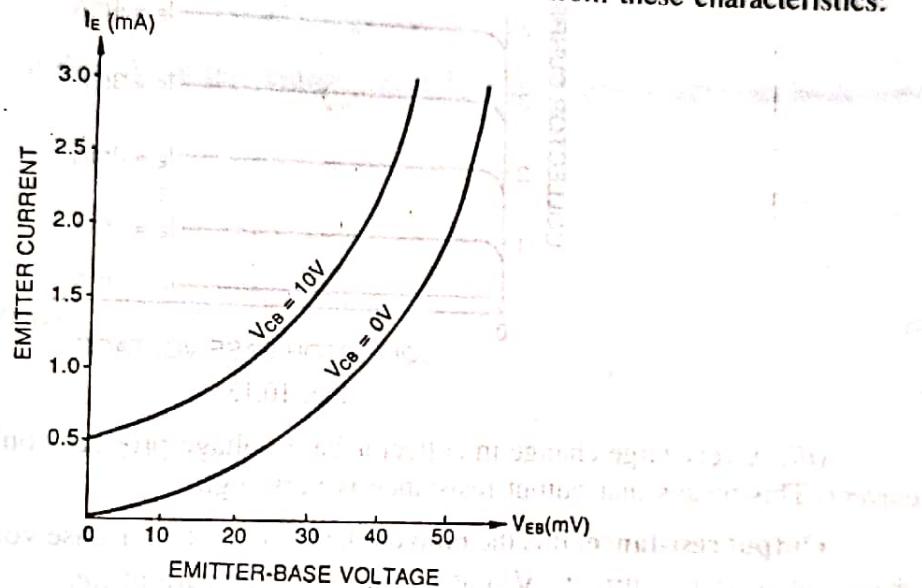


Fig. 10.12

(i) The emitter current I_E increases rapidly with small increase in emitter-base voltage V_{EB} . It means that input resistance is very small.

(ii) The emitter current is almost independent of collector-base voltage V_{CB} . This leads to the conclusion that emitter current (and hence collector current) is almost independent of collector voltage.

Input resistance. It is the ratio of change in emitter-base voltage (ΔV_{EB}) to the resulting change in emitter current (ΔI_E) at constant collector-base voltage (V_{CB}) i.e.

$$\text{Input resistance, } r_i = \frac{\Delta V_{EB}}{\Delta I_E} \text{ at constant } V_{CB}$$

In fact, input resistance is the opposition offered to the signal current. As a very small V_{EB} is sufficient to produce a large flow of emitter current I_E , therefore, input resistance is quite small, of the order of a few ohms.

2. Output characteristics. It is the curve between collector current I_C and collector-base voltage V_{CB} at *constant emitter current I_E . Generally, collector current is taken along y -axis and

* I_E has to be kept constant because any change in I_E will produce corresponding change in I_C . Here, we are interested to see how V_{CB} influences I_C .

collector-base voltage along x -axis. Fig. 10.13 shows the output characteristics of a typical transistor in CB arrangement.

The following points may be noted from the characteristics :-

- The collector current I_C varies with V_{CB} only at very low voltages ($< 1V$). The transistor is *never* operated in this region.
- When the value of V_{CB} is raised above 1–2 V, the collector current becomes constant as indicated by straight horizontal curves. It means that now I_C is independent of V_{CB} and depends upon I_E only. This is consistent with the theory that the emitter current flows *almost* entirely to the collector terminal. The transistor is always operated in this region.

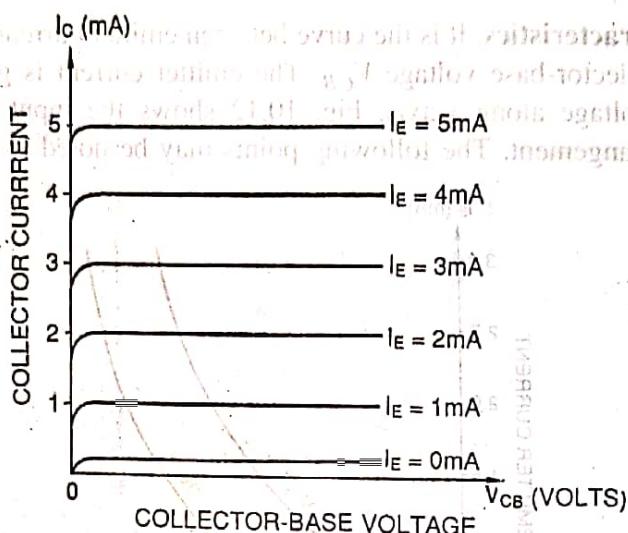


Fig. 10.13

- A very large change in collector-base voltage produces only a tiny change in collector current. This means that output resistance is very high.

Output resistance. It is the ratio of change in collector-base voltage (ΔV_{CB}) to the resulting change in collector current (ΔI_C) at constant emitter current i.e.

$$\text{Output resistance, } r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

The output resistance of CB circuit is very high, of the order of several tens of kilo-ohms. This is not surprising because the collector current changes very slightly with the change in V_{CB} .

10.10 Common Emitter Connection

In this circuit arrangement, input is applied between base and emitter and output is taken from the collector and emitter. Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter connection. Fig. 10.14 (i) shows common emitter *npn* transistor circuit whereas Fig. 10.14 (ii) shows common emitter *pnp* transistor circuit.

1. Base current amplification factor (β). In common emitter connection, input current is I_B and output current is I_C .

The ratio of change in collector current (ΔI_C) to the change in base current (ΔI_B) known as **base current amplification factor** i.e.

$$\beta^* = \frac{\Delta I_C}{\Delta I_B}$$

* If d.c. values are considered, $\beta = I_C / I_B$

10.11 Characteristics of Common Emitter Connection

The important characteristics of this circuit arrangement are the *input characteristics* and *output characteristics*.

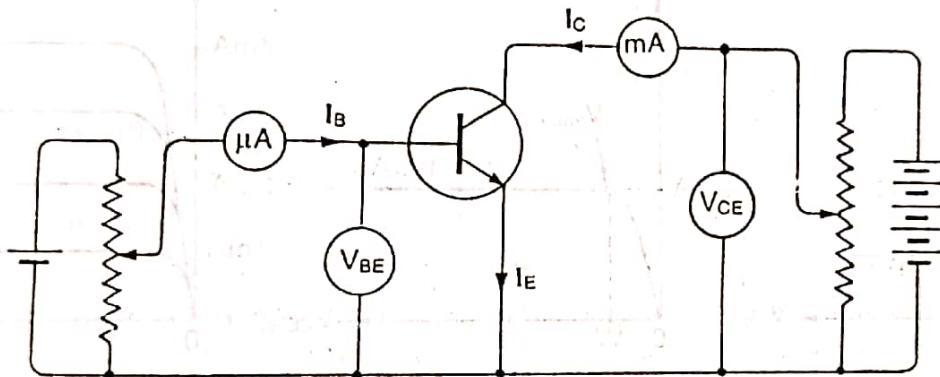


Fig. 10.19

1. Input characteristics. It is the curve between base current I_B and base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE} .

The input characteristics of a *CE* connection can be determined by the circuit shown in Fig. 10.19. Keeping V_{CE} constant (say at 10V), note the base current I_B for various values of V_{BE} . Then plot the readings obtained on the graph, taking I_B along Y-axis and V_{BE} along X-axis. This gives the input characteristic at $V_{CE} = 10V$ as shown in Fig. 10.20. Following a similar procedure, a family of input characteristics can be drawn. The following points may be noted from the characteristics :

- (i) The characteristic resembles that of a forward biased diode curve. This is expected since the base-emitter section of transistor is a diode and it is forward biased.

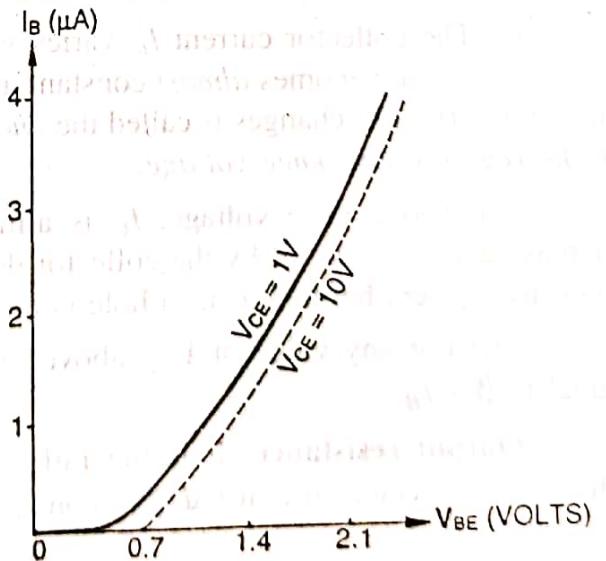


Fig. 10.20

(ii) As compared to *CB* arrangement, I_B increases less rapidly with V_{BE} . Therefore, input resistance of a *CE* circuit is higher than that of *CB* circuit.

Input resistance. It is the ratio of change in base-emitter voltage (ΔV_{BE}) to the change in base current (ΔI_B) at constant V_{CE} i.e.

$$\text{Input resistance, } r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

The value of input resistance for a *CE* circuit is of the order of a few hundred ohms.

2. Output characteristics. It is the curve between collector current I_C and collector-emitter voltage V_{CE} at constant base current I_B .

The output characteristics of a *CE* circuit can be drawn with the help of the circuit shown in Fig. 10.19. Keeping the base current I_B fixed at some values say, $5\ \mu A$, note the collector current I_C for various values of V_{CE} . Then plot the readings on a graph, taking I_C along Y-axis and V_{CE} along X-axis. This gives the output characteristic at $I_B = 5\ \mu A$ as shown in Fig. 10.21 (i). The test can be repeated for $I_B = 10\ \mu A$ to obtain the new output characteristic as shown in Fig. 10.21 (ii). Following similar procedure, a family of output characteristics can be drawn as shown in Fig. 10.21 (iii).

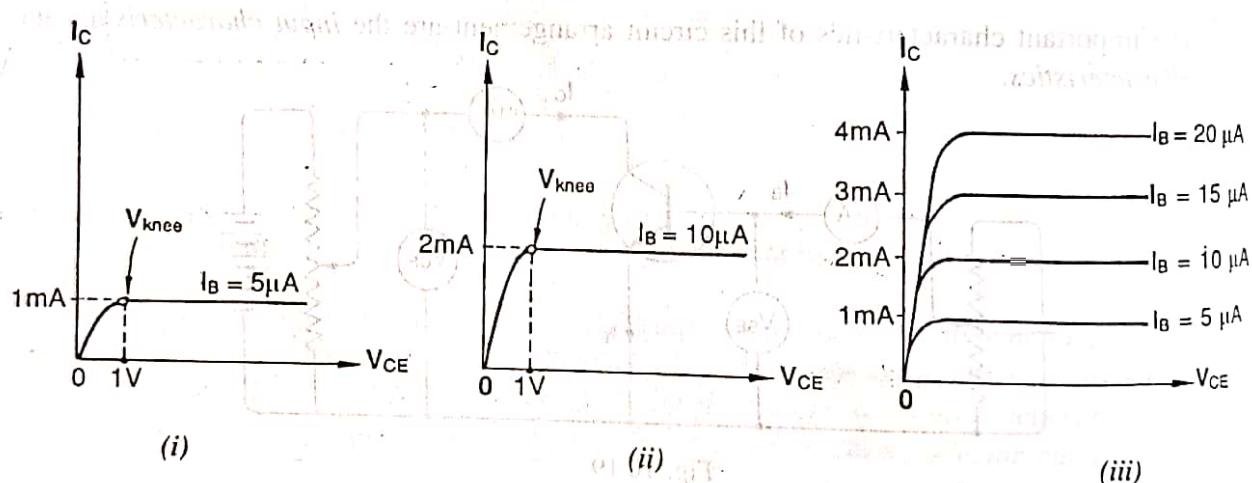


Fig. 10.21

The following points may be noted from the characteristics:-

(i) The collector current I_C varies with V_{CE} for V_{CE} between 0 and 1V only. After this, collector current becomes almost constant and independent of V_{CE} . This value of V_{CE} upto which collector current I_C changes is called the knee voltage (V_{knee}). The transistors are always operated in the region above knee voltage.

(ii) Above knee voltage, I_C is almost constant. However, a small increase in I_C with increasing V_{CE} is caused by the collector depletion layer getting wider and capturing a few more majority carriers before electron-hole combinations occur in the base area.

(iii) For any value of V_{CE} above knee voltage, the collector current I_C is approximately equal to $\beta \times I_B$.

Output resistance. It is the ratio of change in collector-emitter voltage (ΔV_{CE}) to the change in collector current (ΔI_C) at constant I_B i.e.,

$$\text{Output resistance, } r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

It may be noted that whereas the output characteristics of *CB* circuit are horizontal, they have noticeable slope for the *CE* circuit. Therefore, the output resistance of a *CE* circuit is less than that of *CB* circuit. Its value is of the order of $50\text{ k}\Omega$.

10.12 Common Collector Connection

In this circuit arrangement, input is applied between base and collector while output is taken between the emitter and collector. Here, collector of the transistor is common to both input and output circuits and hence the name common collector connection. Fig. 10.22 (i) shows common collector *npn* transistor circuit whereas Fig. 10.22 (ii) shows common emitter *pnp* circuit.

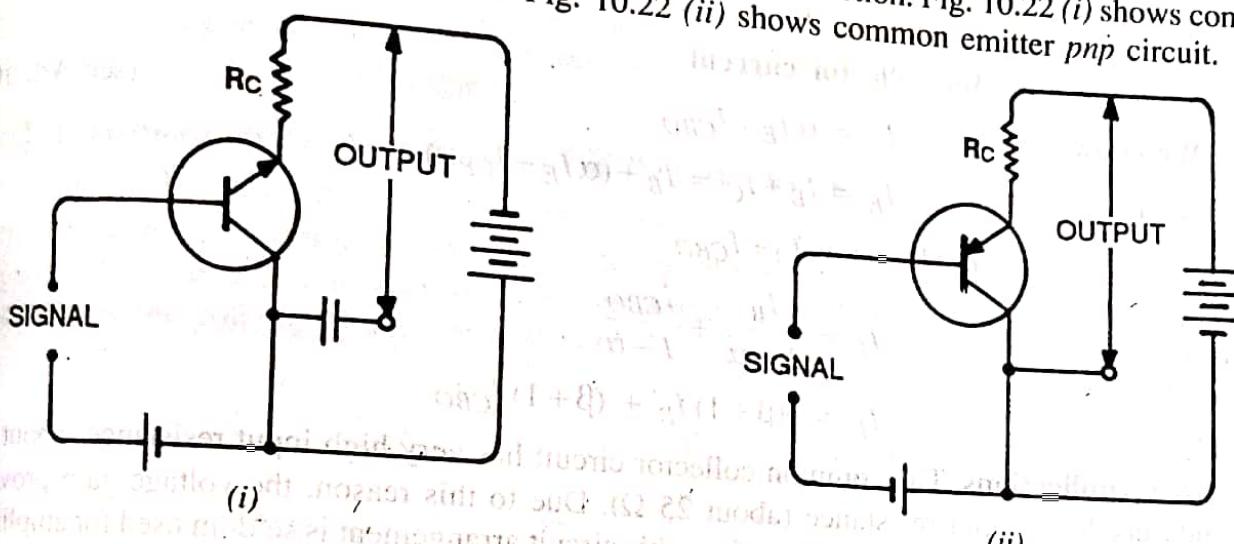


Fig. 10.22

(i) **Current amplification factor γ** : In common collector circuit, input current is the base current I_B and output current is the emitter current I_E . Therefore, current amplification in this circuit arrangement can be defined as under :

The ratio of change in emitter current (ΔI_E) to the change in base current (ΔI_B) is known as **current amplification factor in common collector (CC) arrangement i.e.**

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

This is also known as **emitter current gain** or **current gain** of the circuit.

Field Effect Transistor (FET)

→ FETs are second generation transistors.
They are used in Integrated Circuits.

Difference b/w BJT and FET

- (1) FET is a majority carrier device. But BJT Bipolar Junction transistor is the main function on which total operation of transistor depends i.e. when the + carriers are injected from the emitter to the base and in the base the charges which are injected from the emitter, they are in minority.
- eg. When we consider N-P-N transistor, the emitter is n-type and base is p-type i.e. electrons are injected from emitter to base. And electrons are minority carriers in p-region (base region). This is reason that BJT is called minority carrier device.

- (2) In BJT it is a bipolar device. Here we need holes and electrons both. So base region recombination of charges takes place which gives rise to base current.

FET is unipolar device i.e. either we need electrons or holes.

- (3) In BJT we always talk about current. The current flows because of diffusion of charge carriers. Concentration gradient

~~For more information, diffused is best process~~

In FET, operation depends upon drift of charge carriers under electric field.

So it is a drift device.

(4) FET's are voltage operated devices. But BJT is current operated device.

Reason for popularity of FET's:

(1) Operation of FET is very simple compared to BJT.

(2) Fabrication is much simpler. FET can be fabricated in few steps.

(3) The area required for a single FET on the chip is less than of BJT as it has very high density of devices on the chip.

(4) Besides as a amplifying device, can be used as resistors and capacitors.

FET's are of Two types

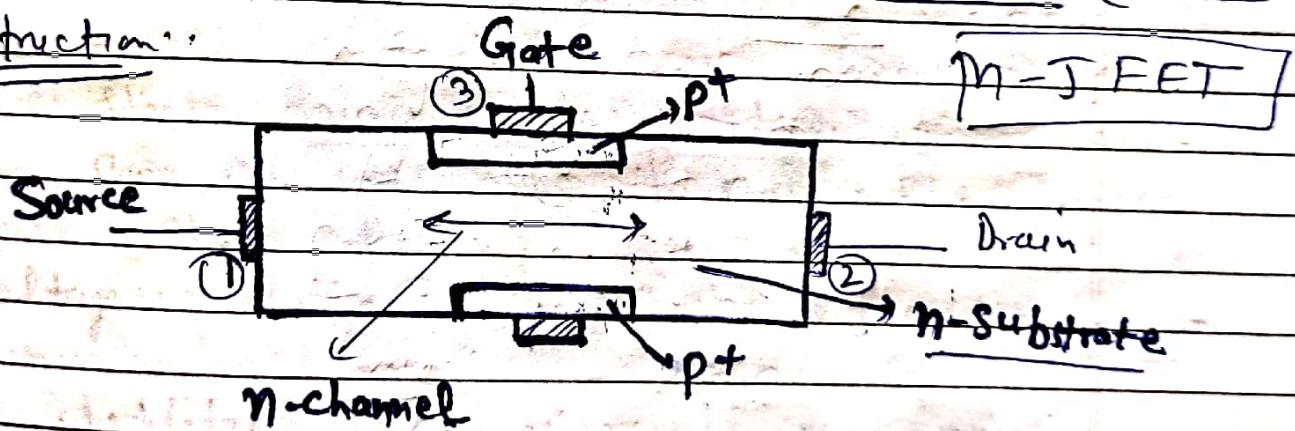
① Junction Field Effect Transistor (JFET) or FET

② Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

In integrated circuits mostly we see MOSFET.

Junction Field Effect Transistor (JFET)

Construction:



On n-Substrate heavily doped P⁺ regions on both sides are developed.

These two P⁺ type regions are shorted internally i.e., internally connected.

Electrode ① is called Source

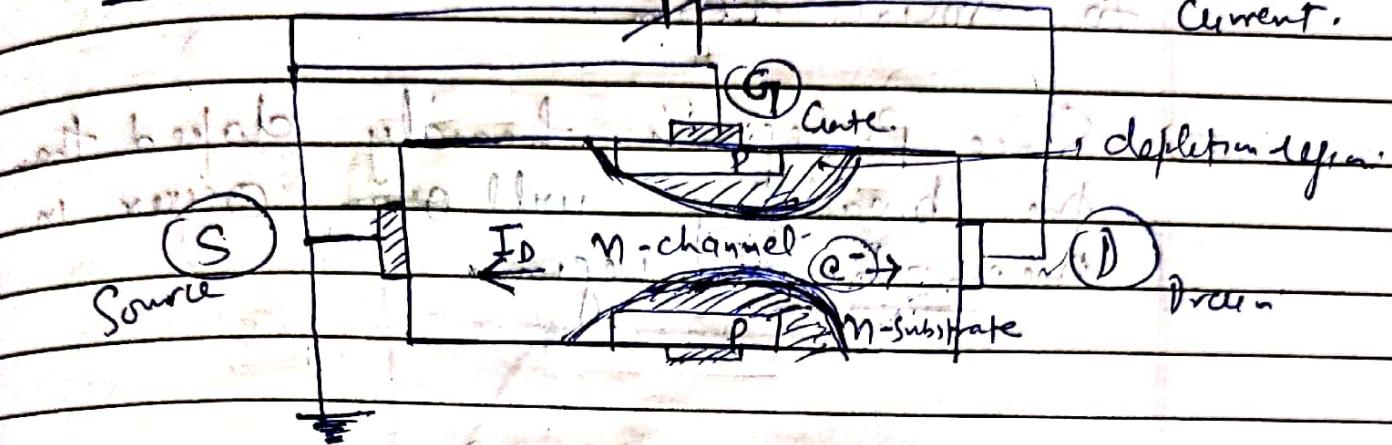
Electrode ② is called Drain

Electrode ③ is called Gate

→ In b/w Gate is called channel.

Substrate is n-type and over which two heavily doped p-type regions are developed.

So P-n junction will formed and hence two depletion regions will form due to diffusion followed by drift

Operations V_{DD} $I_D \rightarrow$ Drain Current.

Case I → Gate is kept at ground potential (zero).

Source is also grounded.

And b/w Source and drain we apply a voltage keeping drain side as +ve.

As we start Source-drain voltage from zero, the as soon as we move further the current will start flowing and larger the voltage larger will be the current.

→ The depletion region widened here.

Two ways.

(1) If we give negative potential to P-type gate the depletion region widened.

(2) +ve potential to n-substrate making gate grounded.

In drain region the depletion width will be larger than source region because near drain region the P-junction

will be more reverse bias as compare to source region.

\Rightarrow Since P-region is heavily doped than the broadening will occur in the n-channel region.

Now when we keep on increasing the Voltage V_{DD} . The depletion region will come closer and closer and the shape will be maintained.

And a situation will come when two depletion regions will meet. That voltage is called the pinch off voltage (V_p).

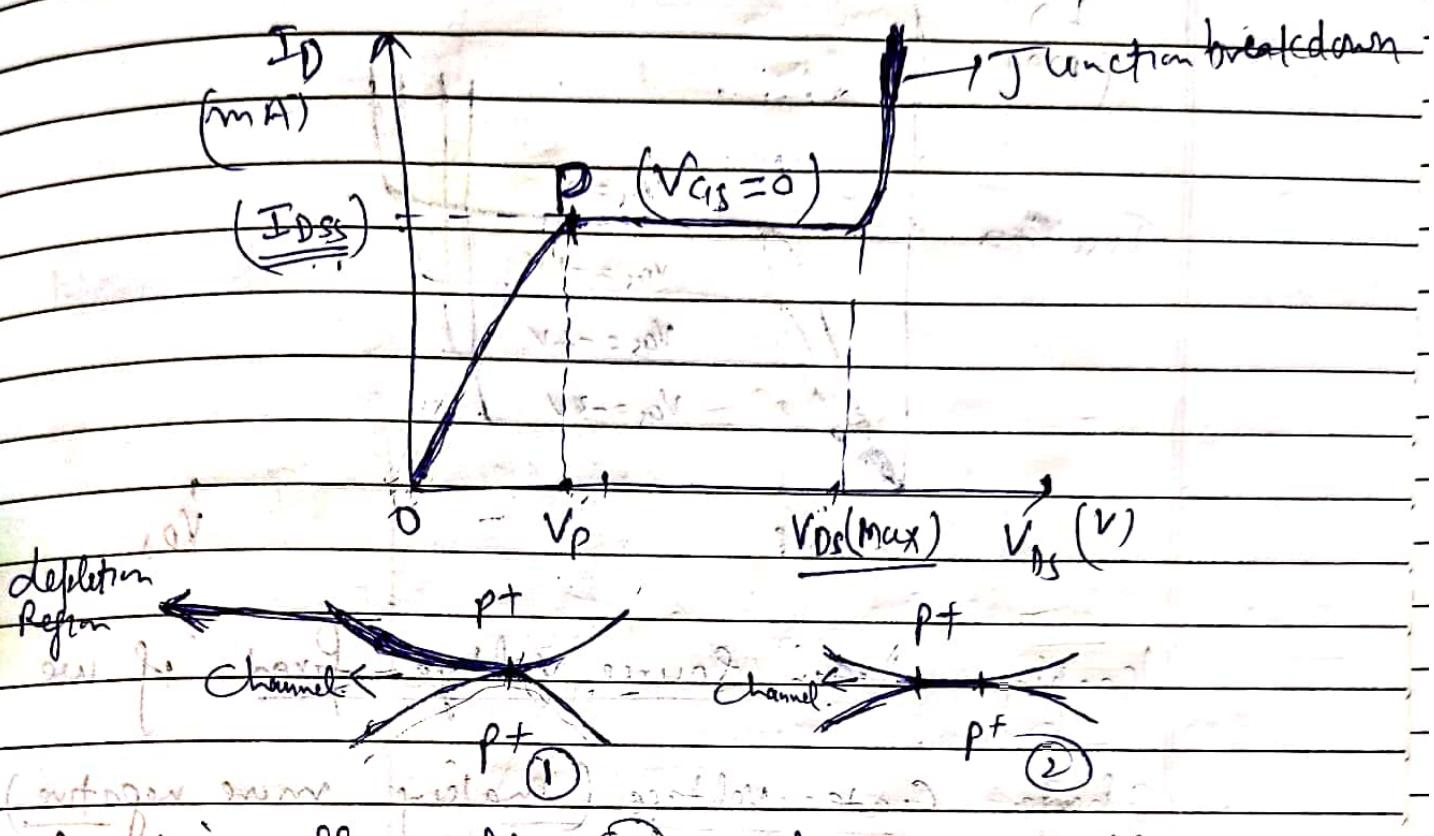
Pinch off voltage (V_p) \rightarrow That minimum voltage between Drain and Source which will make two depletion regions touch at one point.

\Rightarrow Because of the spread of depletion region the channel conductance is changing.

Depletion regions are high resistivity regions and because channel width falls and the resistance will ~~falls~~ and increase, so current levels off it becomes constant.

Date: _____

Drain Current (I_D) as a function of Drain Source Voltage



At pinch off Voltage (V_P) only very small region is in bias contact as (1). If we increase V_{DS} further it increases the contact region between depletion region and hence it stops the rise of current.

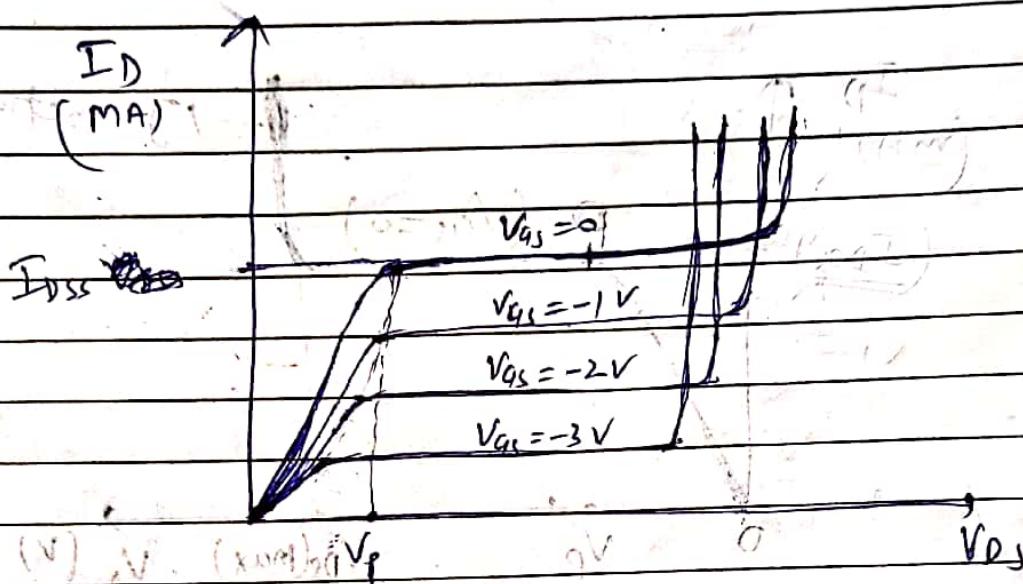
As we increase V_{DS} the contact region between depletion region increases as shown in diagram (2) and hence it stops the rise of current.

The effect of increased voltage V_{DS} to increase the current is leveled off by rise in the resistance of the channel i.e. the Conductance falls.

If we further increase V_{DS} then there is sudden increase in drain current. This is because of junction breakdown.

$I_{DSS} \rightarrow$ Maximum current

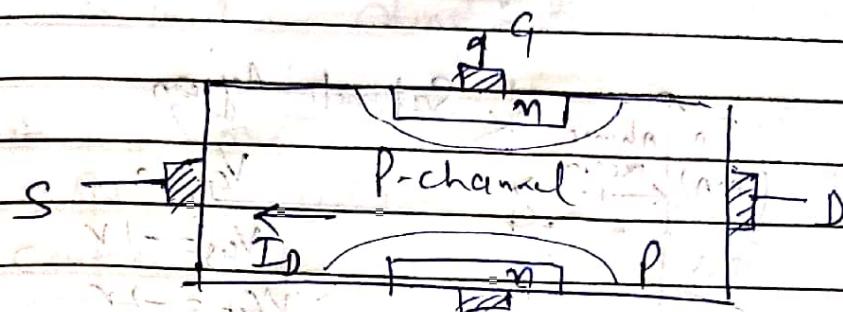
Drain characteristics:



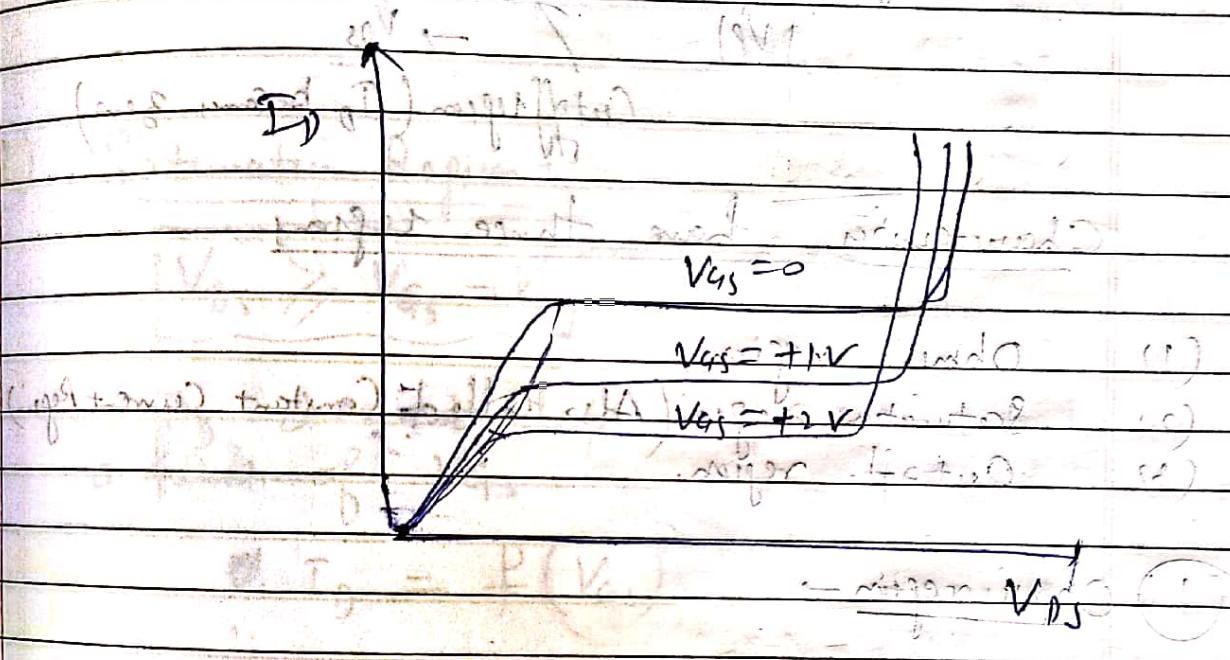
Keeping drain source voltage fixed. if we change gate voltage (making more negative).

→ The depletion will increase and it increase towards the channel. The conductance of the channel decreases. we increases V_{GS} because in the channel the most portion of depletion region exists. And hence on increasing the gate voltage the drain current decreases. and a situation comes where drain current becomes zero. This is known as $V_{GS(off)}$ which makes $I_D = 0$.

$$|V_{GS(off)}| = |V_p|$$

P-JFET

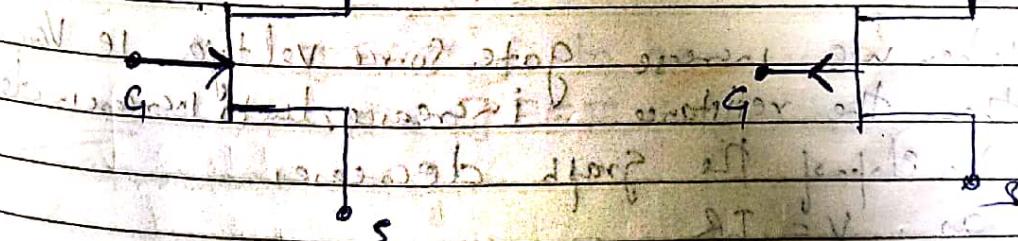
Here holes will give rise to drain current.



n-Type JFET is more popular than P-JFET.

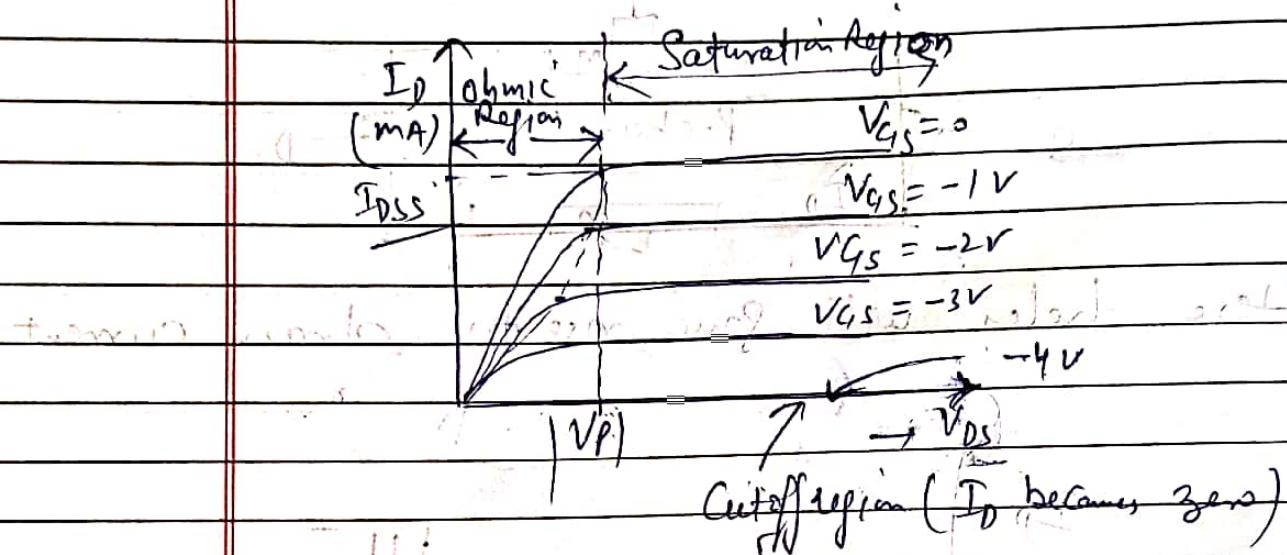
Circuit Symbols of JFET

It is similar to BJT NPN and PNP



n-JFET ————— P-JFET

Current - Voltage characteristic for n-JFET



Characteristic have three regions

- (1) Ohmic region
- (2) Saturation region (Also Called Constant Current Region)
- (3) Cutoff region.

① Ohmic region →

$$V_{DS} > 0, \quad V_{DS} < V_P$$

Current changes linearly as we increase V_{DS}
→ Here V_{DS} is small and no pinch off of the channel.

→ When we increase gate source voltage i.e. V_{GS} then the resistance increases due to increase in depletion width. The slope of the graph decreases as $V = IR$

$$\frac{1}{R} = \left(\frac{I}{V} \right) \rightarrow \text{slope of the graph}$$

Date _____

As $\rightarrow R$ increases slope of the graph decreases as shown in the diagram.

→ The resistance in the ohmic region from 10Ω to $10k\Omega$. It is a voltage controlled resistance V_{GS} is controlling the resistance.

→ JFET can be used as **Voltage controlled resistor** (VCR)

② Saturation Region:

$$|V_{DS}| \geq |V_{GS} - V_p|$$

→ I_D does not depend upon V_{DS} I_D is a function of V_{GS}

$$\bullet I_D = f(V_{GS})$$

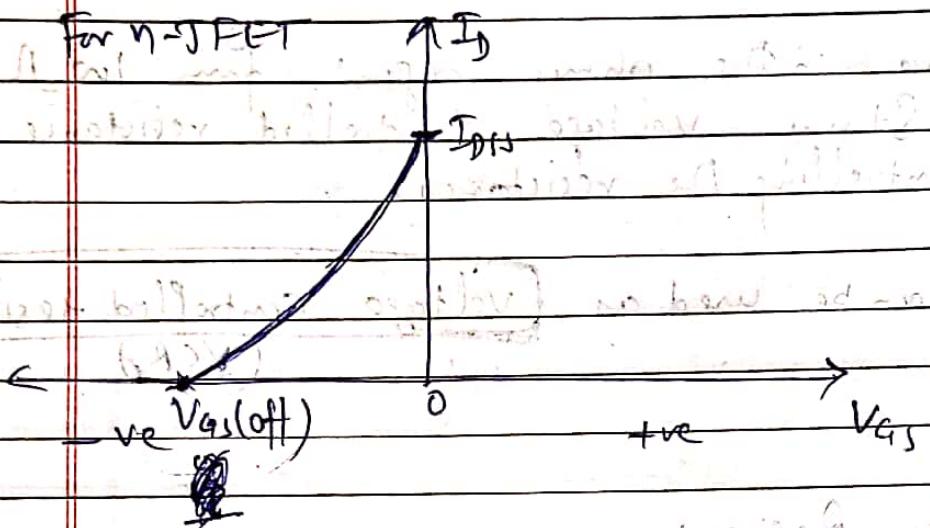
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$$

Drain Current

→ When the JFET is to be used as amplifying device than the JFET is to be used in saturation region.

Transfer characteristic of n-JFET:

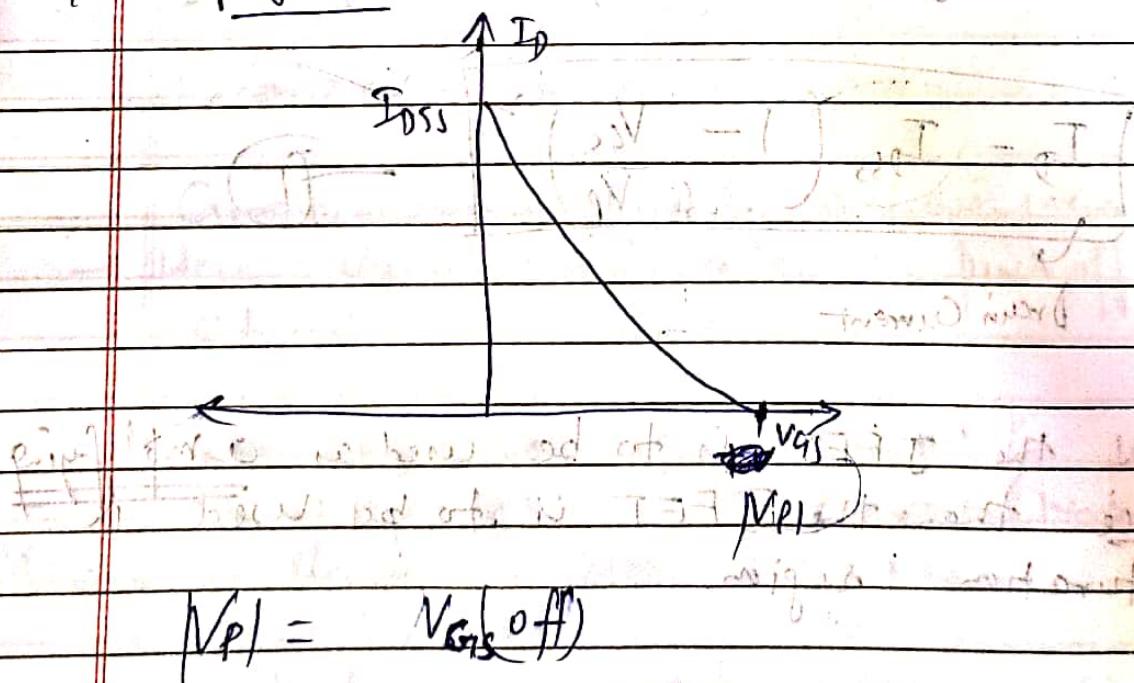
For n-JFET



$$\text{From eq. } I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right) \quad \textcircled{1}$$

$$\text{At } V_{GS} = 0, \quad I_D = I_{DSS}$$

For p-JFET



$$|V_P| = |V_{GS(off)}|$$

From eq. (1)

when $T_d = 0$

$$|V_{GS(0ff)} = V_p|$$

Equation (1) can be written as

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(0ff)}} \right) \quad (2)$$

I_{DSS} represents highest current in JFET

Since I_{DSS} is maximum current for JFET the quantity in bracket should be +ve.

(3) Cut off Region

For n-JFET $|V_{GS} < V_p|$

V_{GS} is more negative than V_p and in this region the drain current is zero and device is off



MOSFET

Metal-oxide Semiconductor Field Effect Transistor

In MOSFET the Gate is separated by insulating layer from the semiconductor SiO_2 or SiO layer.

Therefore MOSFET is sometimes called Insulated Gate FET

Two kinds of MOSFET

(1) Depletion MOSFET (D-MOSFET)

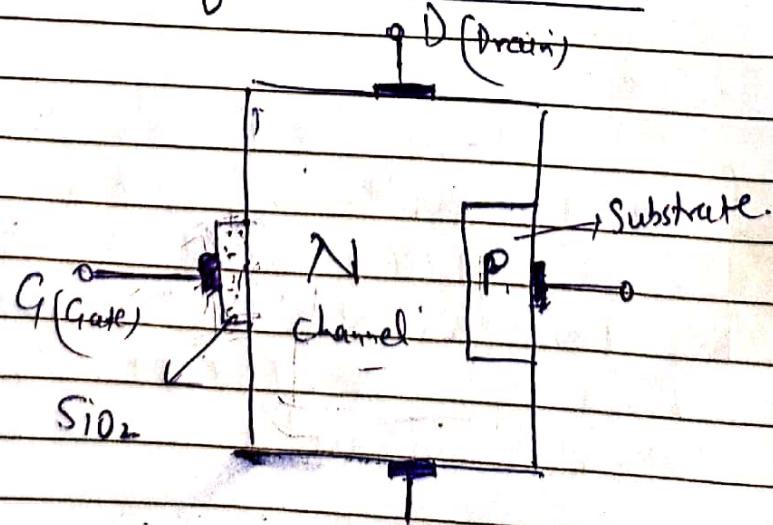
(2) Enhancement MOSFET (E-MOSFET)

D

Depletion MOSFET

Fabrication: It will not form N channel

Construction of a MOSFET

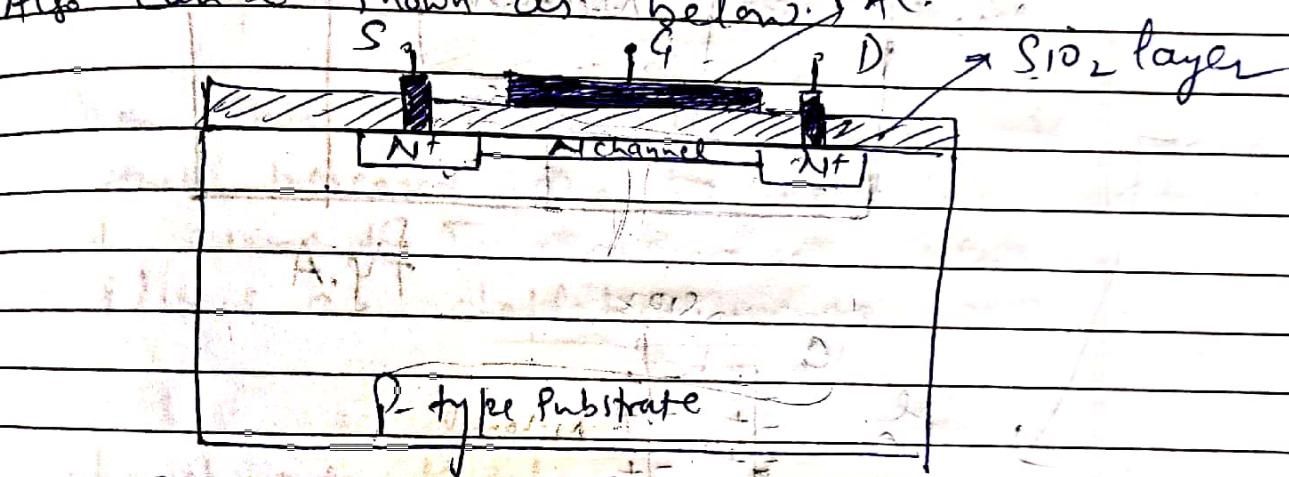


The construction of a MOSFET is a bit similar to the FET. An oxide layer is deposited on the substrate to which the gate terminal is connected.

The oxide layer acts as an insulator.

→ The lightly doped substrate is doped with heavily doped region, here N region is heavily doped, called channel.

Also can be shown as below:



This is N-channel MOSFET

→ Here Si_3N_4 layer will act as insulator.
if there is no P junction here.

Working of N-channel:

Depletion Mode \rightarrow

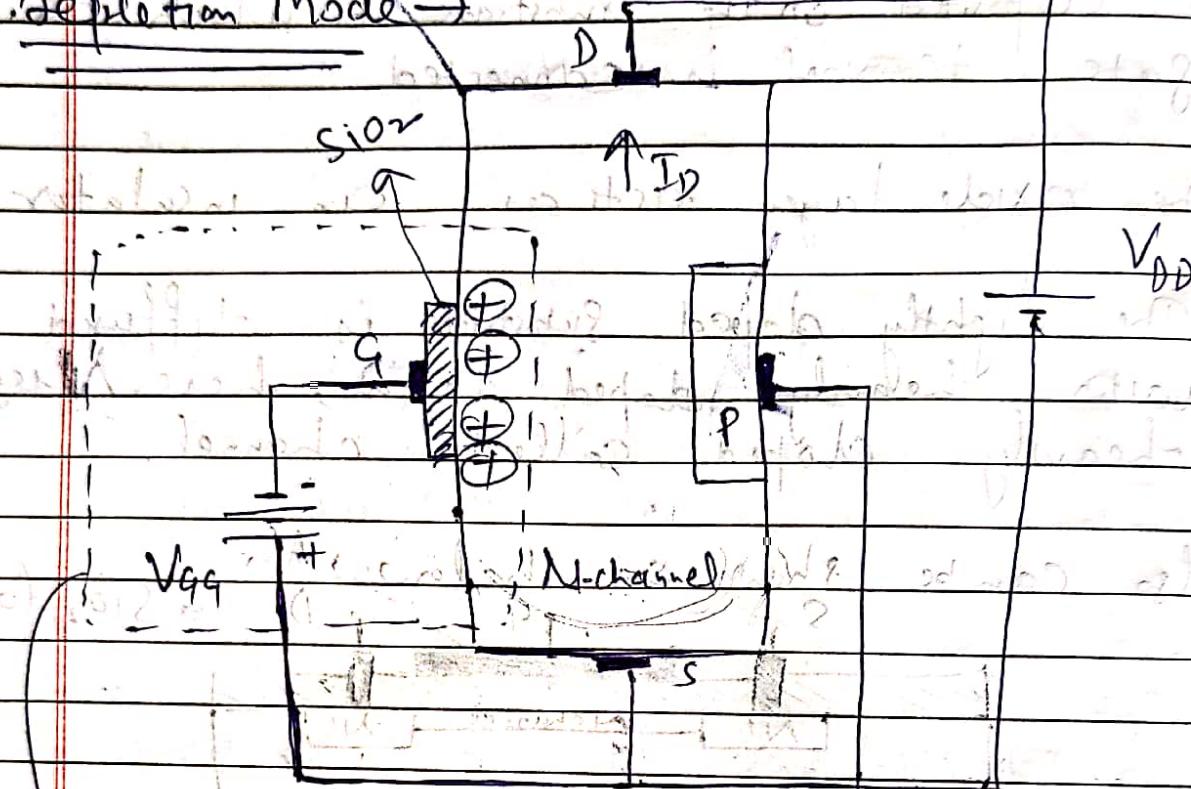


Fig.A

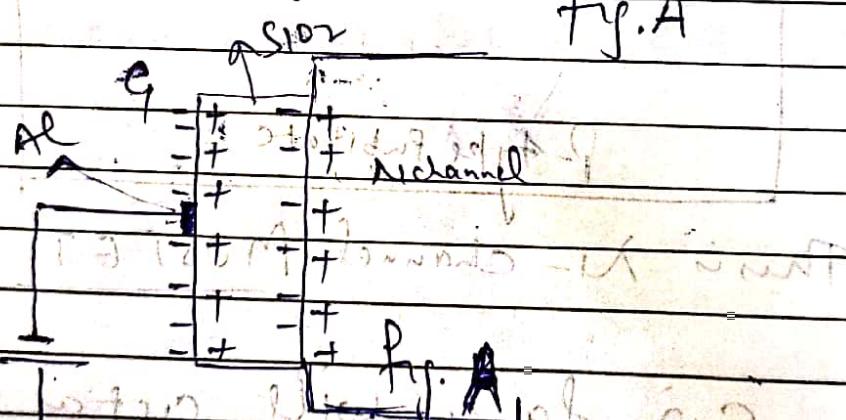


Fig.A

There is no PN junction present between gate and channel.

We can also observe that the ~~channel~~ channel is between N-channel, the SiO₂ layer and Aluminum metal together.

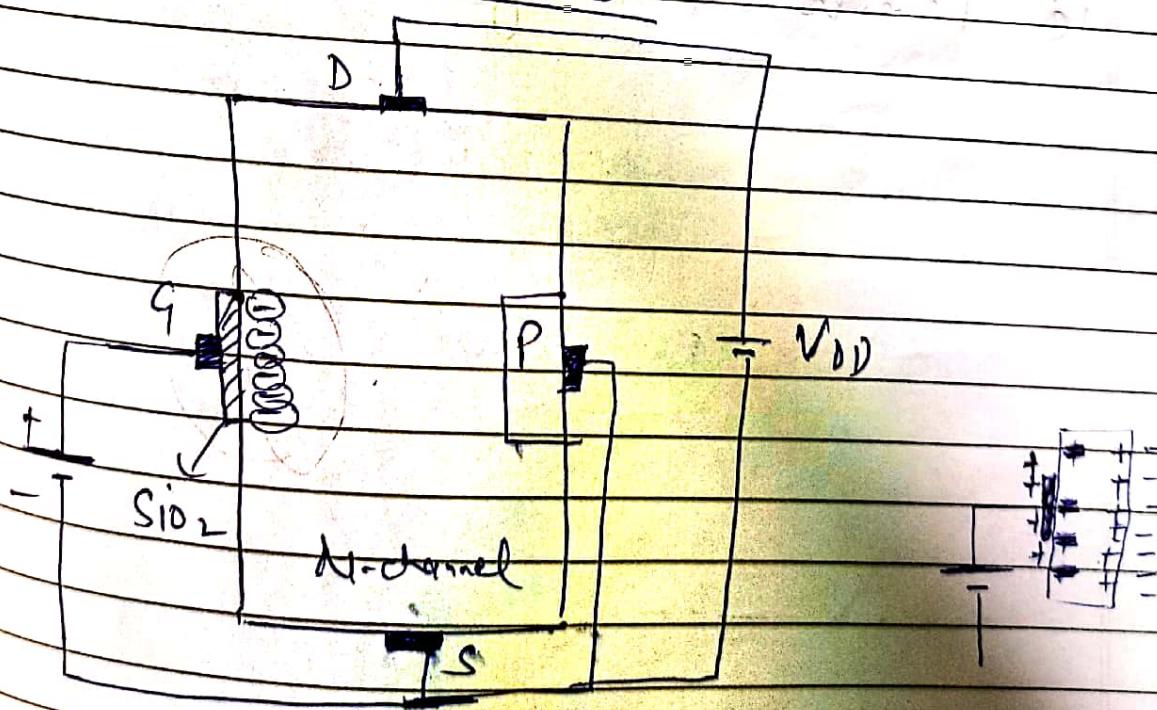
form a parallel plate capacitor as shown in the diagram.

So when -ve potential is applied then due to induced charges the charges will develop in the N-channel. But the majority carriers i.e. electrons get repelled.

With negative potential at V_{DS} , a certain amount of drain current I_D flows through source to drain.

When this negative potential at V_{DS} is further increased, the electrons get depleted and current I_D decreases. Hence it is called as depletion mode MOSFET.

Enhancement Mode



The same MOSFET can be worked in enhancement mode. If we change the polarity of V_{GG} , as shown above.

Here due to induced charges in N-channel we get no charges.

→ As V_{GG} increases no charges increase and hence I_D will increase.

Hence this mode is called enhancement mode MOSFET.

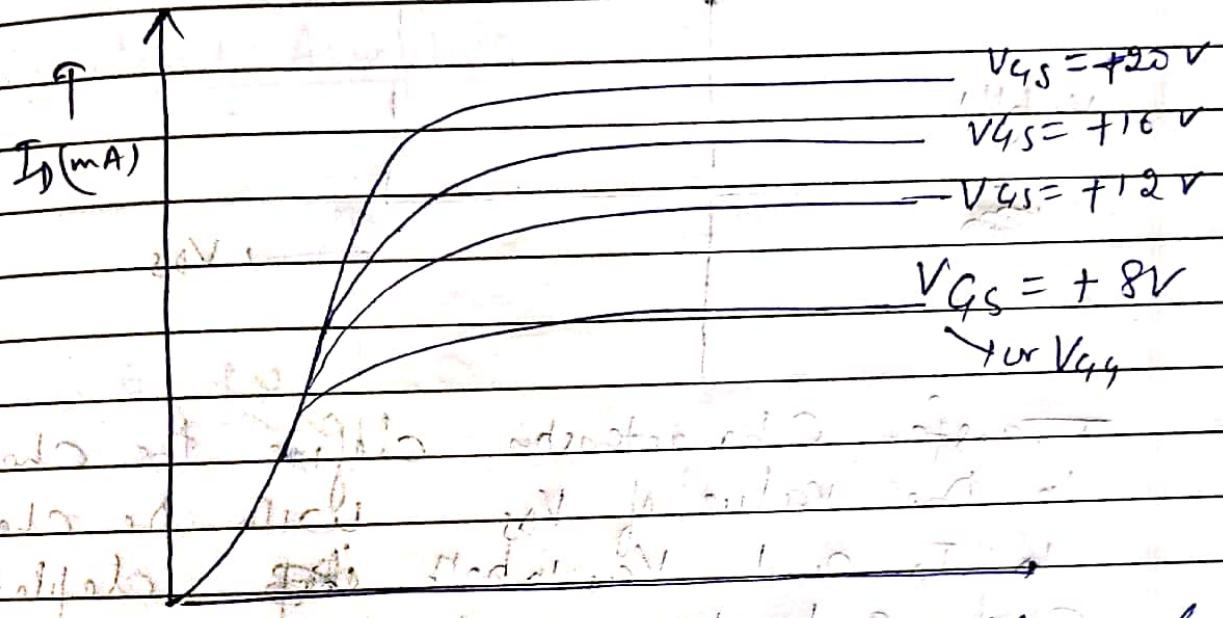
Similarly for P-channel MOSFET.

When Gate Voltage is +ve then we have enhancement mode and when Gate Voltage is -ve then we have depletion mode.

i.e. Reverse that of N-channel MOSFET.

Drain characteristics of MOSFET

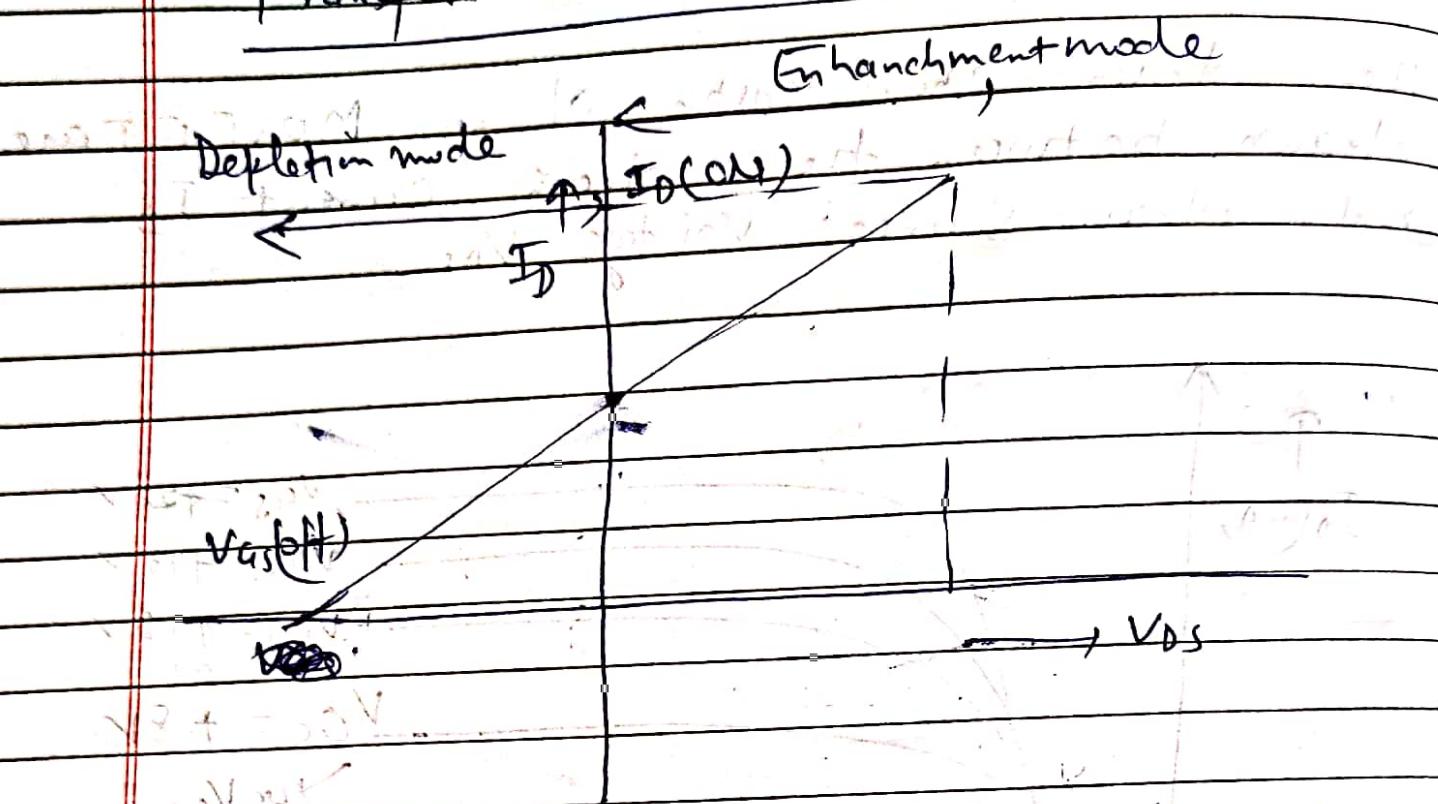
The drain characteristics of a MOSFET are drawn between the drain current I_D and drain source voltage V_{DS} .



Actually when V_{DS} is increased, the drain current I_D should increase, but due to the applied V_{GS} , the drain current is controlled at certain level.

Hence the gate current controls the output drain current.

Transfer Characteristics



Transfer Characteristics define the change in the value of V_{DS} with the change in I_D and V_{GS} in both depletion and enhancement modes.

Let's consider the case of an NMOS transistor with a drain-to-source voltage of 10V and a gate-to-source voltage of 5V. At this point, the drain current is 0. As we increase the drain-to-source voltage, the drain current increases. This is because the electric field between the drain and source is increased, which attracts more charge carriers from the drain towards the source. However, if we further increase the drain-to-source voltage beyond a certain point, the drain current begins to decrease. This is because the electric field between the drain and source becomes so strong that it begins to repel the charge carriers away from the drain, effectively reducing the drain current.

4.7.3. SEMICONDUCTOR LASER

Principle

In a semiconductor material when electron and hole recombine, excess of energy is either emitted as heat energy or light energy. In case of Ge or Si the emitted energy is in the form of heat, so of no use in laser action. Whereas in case of Gallium arsenide (GaAs), Cadmium sulphide (Cds), Cadmium selenide (CdSe), the energy is emitted in the form of light radiation near infrared region and can be of great importance in lasing.

Laser Action in Intrinsic Semiconductor

A pure semiconductor without any impurity is known as *intrinsic semiconductor*. For every conduction electron produced there must be a corresponding hole generated in valence band. The transition of electron from top of valence band to bottom of conduction band is viewed as generation of electron hole pair. The reverse

transition of electron from conduction band to valence band are also possible, when it happens, an electron meets a hole and process is viewed as electron and hole recombination.

When semiconductor material is illuminated by photons whose energy is equal to band gap energy of semiconductor or higher, such a photon can be absorbed by electron in the top of valence band. This excited electron then jumps to conduction band as shown in Fig. 4.14 (a). Practically the same probability exist for the photon to initiate the opposite process i.e. transfer of electron from bottom of conduction band to the valence band. When this transferred electron combines with the hole in valence band, a quantum of energy equal to difference in energy of two states is emitted. This secondary emitted photon is in phase with primary photon as shown in Fig. 4.14 (b).

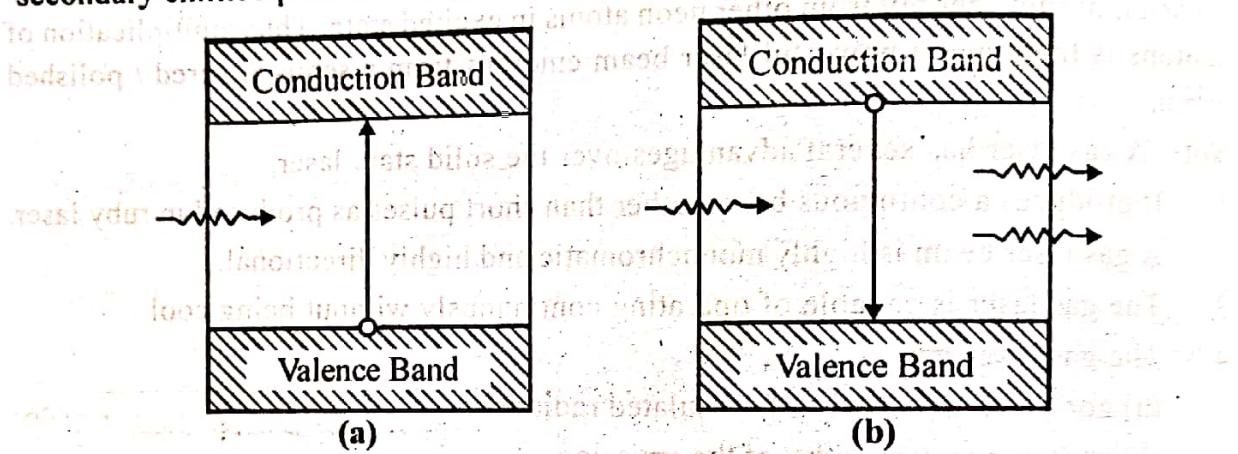


Fig. 4.14

Thermal excitation of a semiconductor moves electron from valence band to conduction band to very small extent so concentration of electron even at room temperature at bottom of conduction band is lower than that in valence band. Thus at reasonable temperature process of light absorption dominates over stimulated emission i.e. more and more electron in valence band absorbs incident photon and jumps over to conduction band. As a result of it, concentration of electrons at the bottom of conduction band becomes higher than at the top of valence band. In this state, semiconductor is said to be *inverted or degenerate semiconductor*. A semiconductor can be made degenerate in *p*-type carrier or in *n*-type carriers or in both types of carriers simultaneously.

Degenerate *n*-type and *p*-type semiconductor or laser action in extrinsic semiconductor

When a pure semiconductor is doped with impurity atoms which donates electrons is called *donor* or *n-type impurity* and those which accept electron from host material is called *acceptor* or *p-type impurity*. The energy level diagram of *n*-type and *p*-type semiconductor is as shown in Fig. 4.15 (a) and (b).

In Fig. 4.15 (a), the donor energy level is just below the bottom of conduction band at $\Delta E = 0.01$ eV. When temperature of *n*-type semiconductor is gradually increased from 0 K, the transition from donor energy level to conduction band takes whereas to 50 K, the donor energy level will be depleted i.e. all the donor atoms have donated their electrons in to conduction band. This makes the material as *n*-type degenerate.

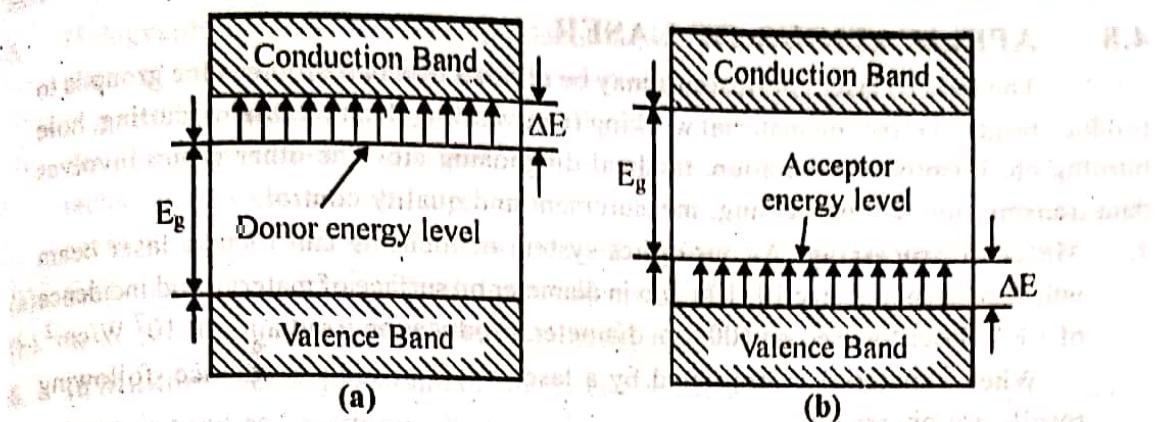


Fig. 4.15 (a) *n*-type semiconductor (b) *p*-type semiconductor

In Fig. 4.15 (b), the acceptor energy level is just above the top of valence band at $\Delta E=0.01$ eV. When temperature is gradually increased from 0 K, the transition of electrons from valence band to acceptor energy levels takes place. Around 20 to 50 K, the acceptor energy level will be completely filled and the electrons raised to this level leaves behind holes. This makes the semiconductor *p*-type degenerate.

Laser action in *p-n*-junction

The most common way of producing population inversion in the semiconductor is by joining a *p*-type and *n*-type material together as shown in Fig. 4.16, the resulting arrangement is known as *p-n* junction. When forward bias is applied to *p-n* junction, electrons from *n*-side and holes from *p*-side will be injected into junction area. The *p-n* junction will experience transition of electrons from the conduction band into valence band, the electrons and holes recombine there, and thus emits excess of energy as radiation. If active material is placed within suitable region

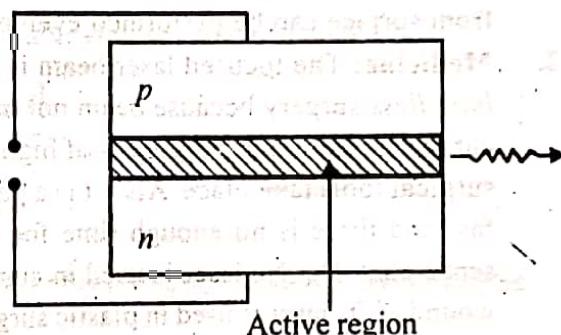


Fig. 4.16

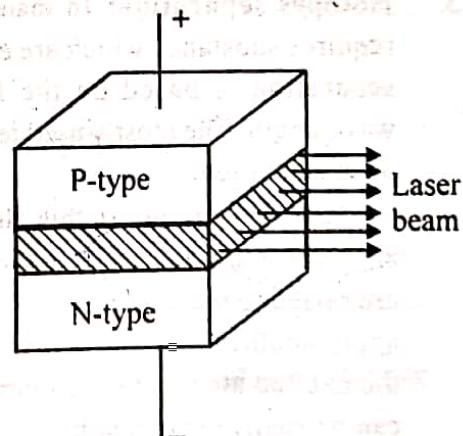


Fig. 4.17

Laser produced using *p-n* junction in forward biased is referred as injection laser. First semiconductor laser of this type was made in 1962 using GaAs material. The gallium arsenide was made *n*-type by adding tellurium. While *p*-region was achieved by diffusing zinc. For achieving laser action, two end faces are made parallel and other two surfaces are left rough to suppress oscillation in undesired direction. The thickness of *p-n*-junction is $2\ \mu\text{m}$. In semiconductor diode laser no mirrors are needed for feedback because refractive index is large enough to give considerable reflection at semiconductor air interface. The laser output of GaAs oscillates at wavelength 8500\AA to 9000\AA near infrared region.