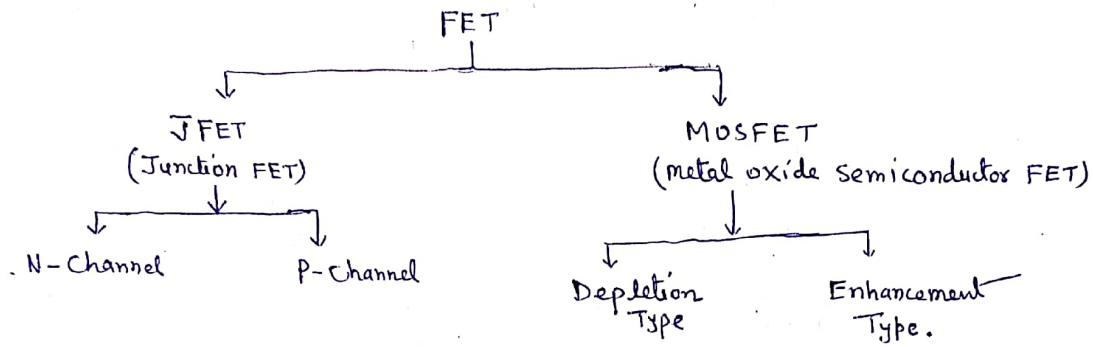
Field effect Transistors (FET) :→

It is a three terminal unipolar Semiconductor device in which Voltage is controlled by an electric Field. In FET the current Condution is by one type of majority Carriers.



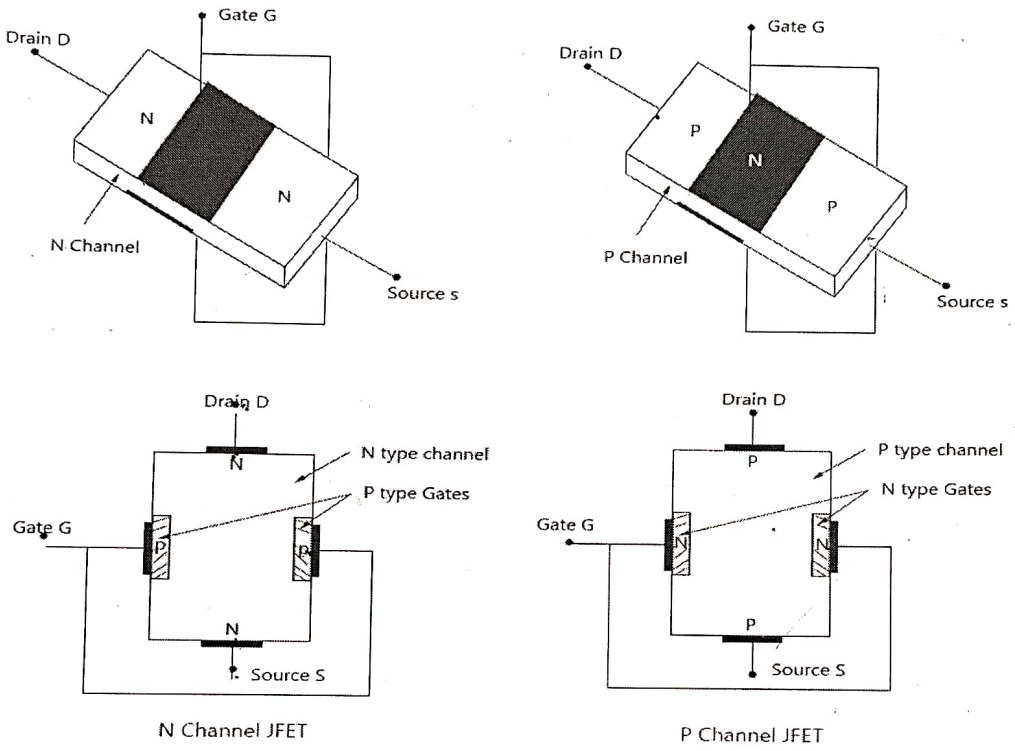
Difference between FET and BJT :→

FET	BJT
• It is unipolar device because current Conduction is only due to one type of Charge carrier either electron or hole.	• It is Bipolar device because current Conduction is due to both types of carriers.
• It is Voltage deriven device	• It is current deriven device
• High input impedance (in mΩ) due to reverse bias	• Low input impedance due to forward bias.
• Low Noise Level	• High Noise Level
• Better thermal Stability	• Less thermal Stability
• Gain is Characterised by transconductance	• Gain is Characterised by Voltage gain
• Has high Power gain	• Has low power gain.

Dinesh kumar
physics.

BASIC COSTRUCTION AND SYMBOLS:

JFET's are of two types, namely N-channel JFETs and P-channel JFETs. Generally N-channel JFETs are more preferred than P-channel. N-channel and P-channel JFETs are shown in the figures below.



JFET Junction Field Effect Transistors

The structure is quite simple. In an N-channel JFET an N-type silicon bar, referred to as the channel, has two smaller pieces of P-type silicon material diffused on the opposite sides of its middle part, forming P-N junctions, as illustrated in figure. The two P-N junctions forming diodes or gates are connected internally and a common terminal, called the gate terminal, is brought out. Ohmic contacts (direct electrical connections) are made at the two ends of the channel—one lead is called the Source terminal S and the other Drain terminal D.

The silicon bar behaves like a resistor between its two terminals D and S. The gate terminal is analogous to the base of an ordinary transistor(BJT). It is used to control the flow of current from source to drain. Thus, source and drain terminals are analogous to emitter and collector terminals respectively of a BJT.

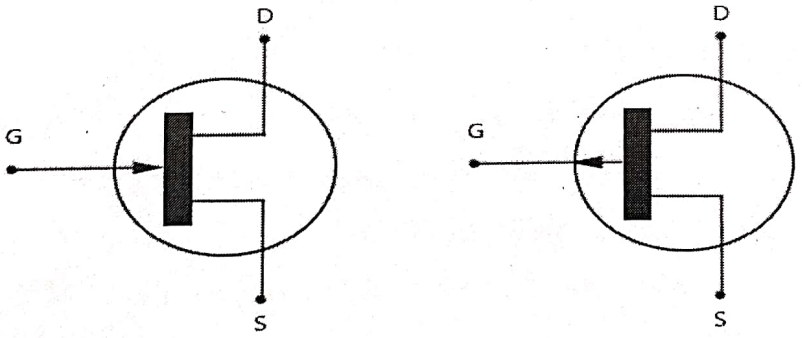
Source – The terminal through which the majority carriers enter the channel, is called the *source* terminal S and the conventional current entering the channel at S is designated as I_g.

Drain – The terminal, througih which the majority carriers leave the channel, is called the *drain* terminal D and the conventional current leaving the channel at D is designated as I_D.

The drain-to-source voltage is called V_{DS}, and is positive if D is more positive than source S

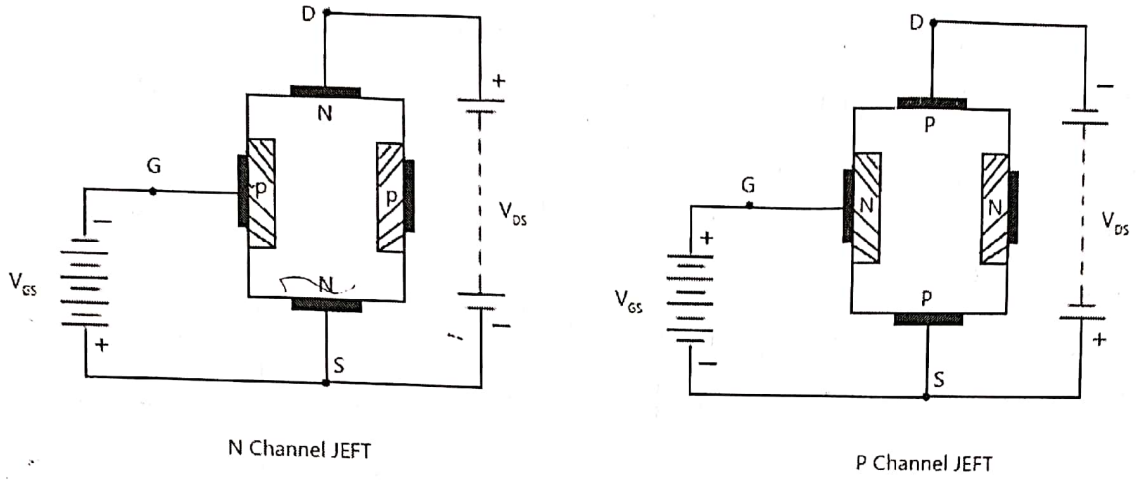
Gate – There are two internally connected heavily doped impurity regions formed by alloying, by diffusion, or by any other method available to create two P-N junctions. These impurity regions are called the gate G. A voltage V_{GS} is applied between the gate and source in the direction to reverse-bias the P-N junction. Conventional current entering the channel at G is designated as I_G.

Channel – The region between the source and drain, sandwiched between the two gates is called the *channel* and the majority carriers move from source to drain through this channel.



JFET-N-Channel and P-channel Schematic Symbol

Schematic Symbols of JFET



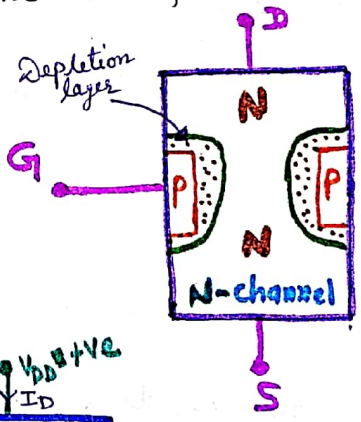
N Channel JEFT

P Channel JEFT

JFET Polarity Conventions

OPERATION OF N- CHANNEL FET

(i) When $V_{GS} = 0$ and $V_{DS} = 0$ then depletion layers in PN Junction is formed. These depletion layers are of equal thickness and symmetrical.



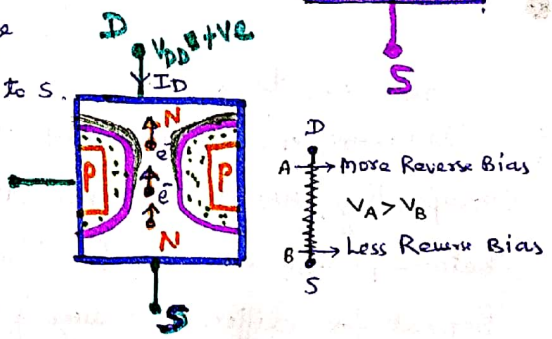
(ii) When $V_{GS} = 0$ and $V_{DD} = +ve$

Electrons start to flow from S to D and hence drain current I_D start to flow from D to S.

Due to this flow of current, there is a uniform voltage drop across the channel resistance as we move from D to S.

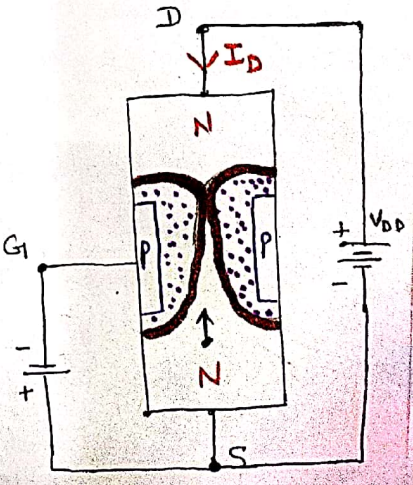
This voltage drop reverse biases the diode.

The gate is more −ve w.r.t. those points in the channel which are nearer to D than S. Thus, wedge shaped depletion regions are formed.



(iii) When V_{GS} = −ve and V_{DD} = +ve

Due to the reverse bias, the width of depletion regions increases. At a particular value of V_{GS} (−ve) and V_{DD} (+ve), the $I_D = 0$. This is because the two depletion regions touch each other and e^-s do not pass through the channel. The voltage at which drain current becomes zero is called pinch off voltage (V_P)



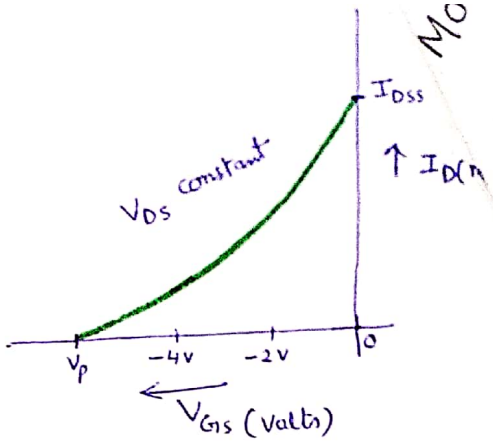
Since −ve gate voltage controls the drain current, FET is called a voltage controlled device.

Transfer Characteristics of N-channel FET :→

Adjust V_{DS} at a suitable value.

Now V_{GS} is increased in steps and note the corresponding drain current I_D. Then plot a graph between V_{GS} and I_D as shown in fig.

As V_{GS} is more and more -ve, the drain current I_D decreases (due to increase in width of the depletion layers) and becomes zero at V_p (Pinch off voltage)

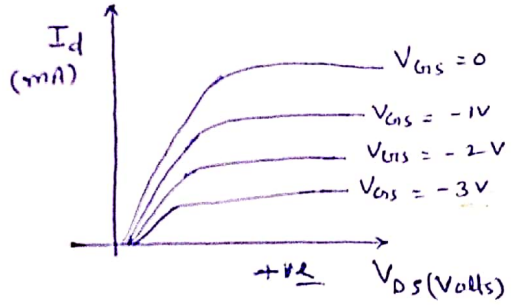


The transfer characteristics is a part of parabola & is expressed by the equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2, \quad I_{DSS} = \text{max. drain current at } V_{GS} = 0$$

Drain to source output Characteristics :→

At $V_{GS} = 0$, we get the highest value of I_D. Similarly when V_{GS} becomes more & more -ve, value of I_D decreases.

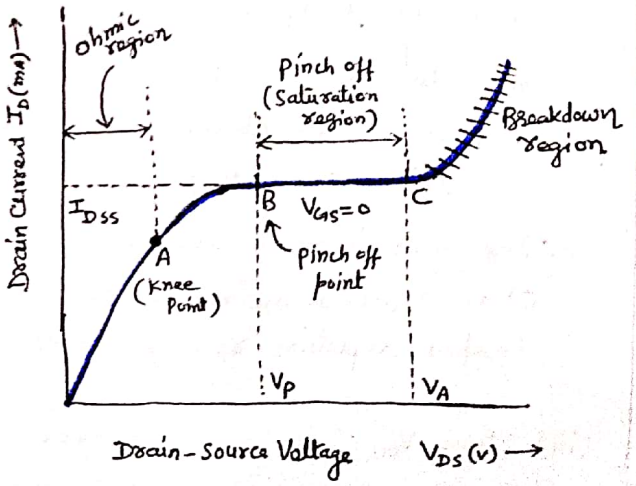


Static Characteristics curves of JFET :→

Set V_{GS} to Zero.

Increase V_{DS} in small steps and note the corresponding values of I_D. Then draw a graph between V_{DS} and I_D for $V_{GS} = 0$.

Repeat for different values of $V_{GS} = +0.5V, -1V, -2V$ etc.



MOSFET (Metal oXide Semiconductor Field Effect Transistor) :→

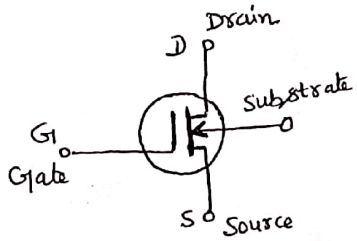
It is widely used for switching and amplifying electronic signals. Since it is constructed with the gate terminal insulated from the channel, it is sometimes called Insulated gate FET (IGFET). Like JFET, a MOSFET is also a three terminal (Source, gate and drain) device and drain current in it is controlled by gate bias.

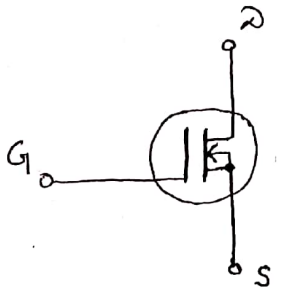
Types of MOSFET :→

1. Depletion mode MOSFET :→ The mode of MOSFET when gate is maintained at -ve pot. while drain is maintained at +ve pot. is known as depletion mode.
2. Enhancement mode :→ When gate is maintained at +ve while drain at -ve pot., then mode is known as enhancement mode.

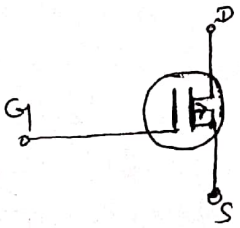
Symbols :→

- Depletion MOSFET (D-MOSFET) :-



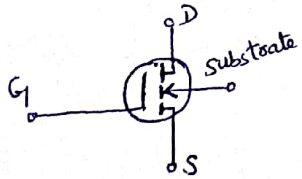


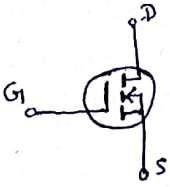
(N - Channel D- MOSFET)



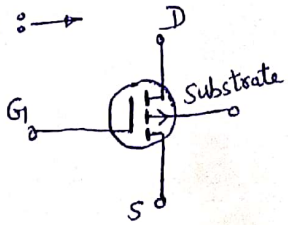
(P - Channel DE-MOSFET)

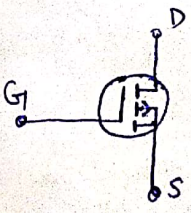
- Enhancement MOSFET (E-MOSFET) :→





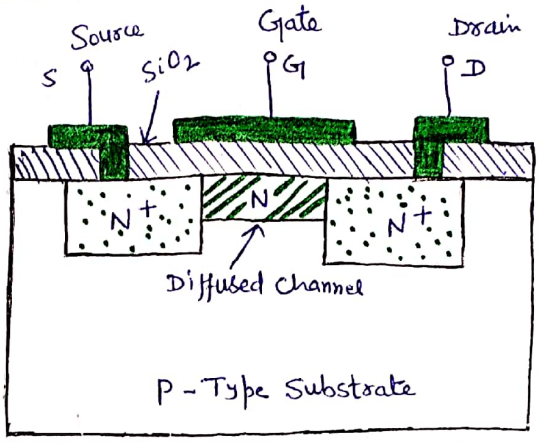
(N- Channel E-MOSFET)





(P - Channel E-MOSFET)

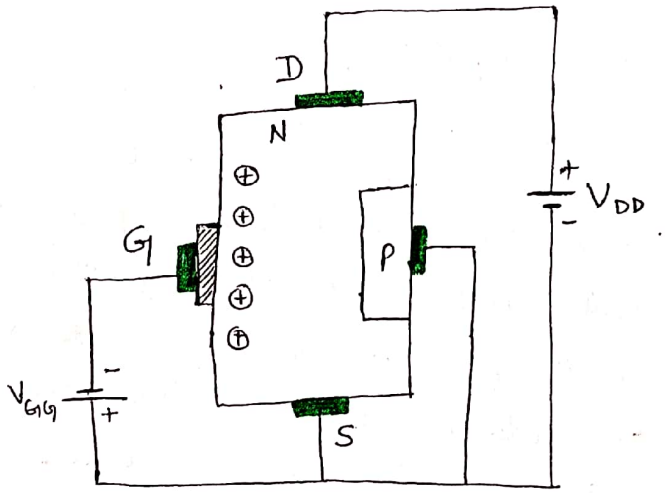
N- Channel Depletion type MOSFET :→



It consists of a lightly doped P-type substrate into which two highly doped N^+ regions are defused. These N^+ regions act as source and drain and are separated by about 5 to 10 μm. A thin (1,000 to 2,000 Å) layer of insulating Silicon dioxide (SiO_2) is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with source and drain. This layer constitutes the gate. This layer of SiO_2 results in an extremely high input resistance of the order of 10^{10} to 10^{15} ohm for this device.

The Chip area of MOSFET is 3 square miles or less.

Working :→

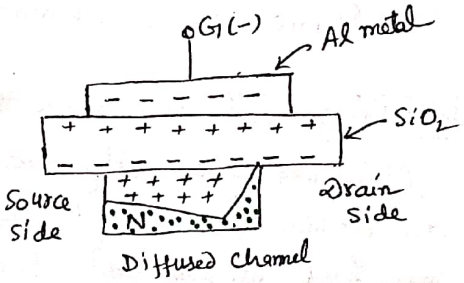


There is no PN Junction between gate and channel.

The diffused N channel, insulating dielectric SiO_2 and metal layer of gate forms a parallel plate capacitor.

For Depletion mode, Gate maintained at -ve pot
Drain maintained at +ve pot.

When $V_{GS} = 0$, a significant current flows for a given V_{DS} because +ve voltage applied to the drain, free e^-_s from channel are attracted

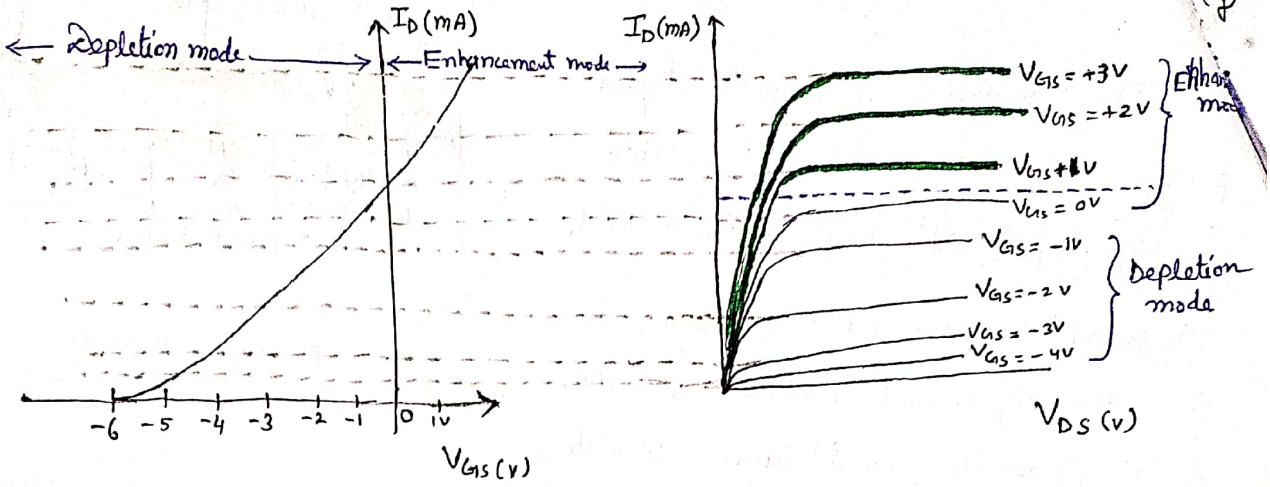


Let Gate is at -ve pot, +ve charges induced in N-channel through SiO_2 because gate repel these free e^-_s towards P-type substrate and attract hole. Now e^-_s & holes will combine. This serves to deplete the channel of majority carriers (e^-_s) and conductivity decreases.

Greater is -ve voltage on the gate, greater is the reduction in e^-_s number and hence lesser will be the conductivity.

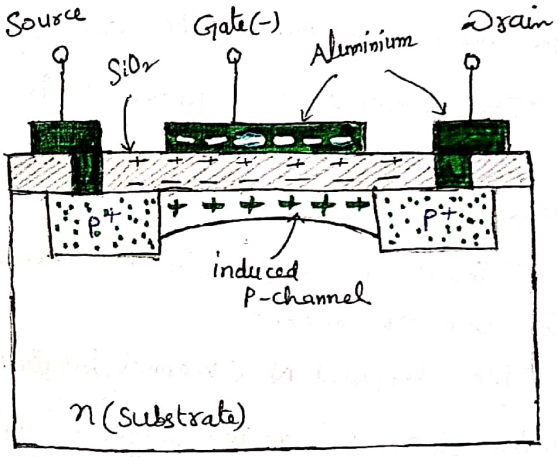
At high -ve voltage at gate, voltage can pinch off the channel, hence it act just like JFET.

· Drain and Transfer Characteristics of Depletion type MOSFET:-



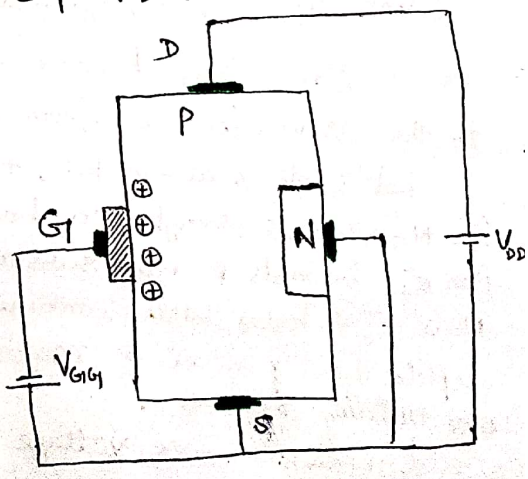
Enhancement mode MOSFET :→

(P-Channel MOSFET)



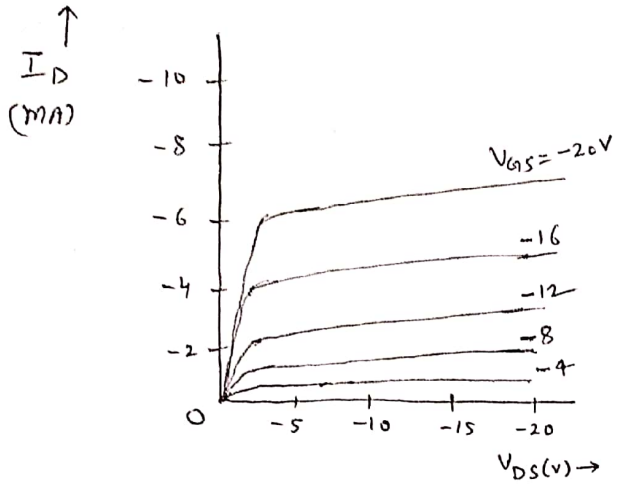
The P channel MOSFET consists of a lightly doped n-type substrate into which two highly doped p^+ regions are diffused. These p^+ sections which will act as the source and drain are separated by about 5 to 10 μm. A thin layer of insulating SiO_2 is grown over the surface of the structure, and holes are cut into the oxide layer, allowing contact with the source and drain.

The metal area of gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, form a parallel plate capacitor.

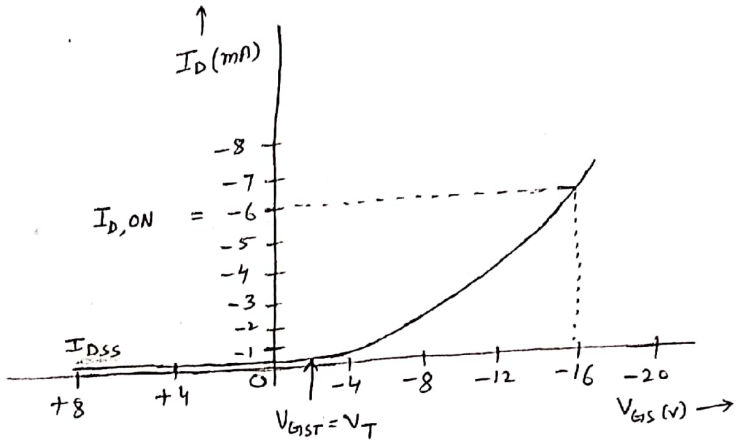


Working :- If we ground the substrate for the structure and apply -ve voltage at the gate, an electric field will be directed ⊥ through the oxide. This field will end on "induced" +ve charges on the semiconductor side. The +ve charges which are minority carriers in n-type substrate, form an "inversion layer" As the magnitude of -ve voltage on the gate increases, the induced +ve charges in the semiconductor increases. The region beneath the oxide now has p-type carriers, the conductivity increases, and current flows from source to drain through the induced channel Thus the drain current is "enhanced" by the -ve gate voltage and such a device is called an enhancement-type MOS.

Drain and Transfer Characteristics of Enhancement MOSFET :-



(Drain Characteristics)



(Transfer characteristics)

The current I_{DSS} at $V_{GS} \geq 0$ is very small, of the order of a few nanoamperes. As V_{GS} is made -ve, the current $|I_D|$ increases slowly at first, and then much more rapidly with an increase in $|V_{GS}|$.

The value of Threshold Voltage V_T is typically $-4V$ & is common to use a power supply voltage of $-12V$ for the drain supply.

The equation for the transfer characteristics of E-MOSFET is

$$I_D = K(V_{GS} - V_{GS(th)})^2$$, where $K = 0.3\ mA/V^2$, is a property of the device construction.

Do yourself :-

1) P- Channel Depletion type MOSFET
2) N- Channel enhancement type MOSFET
3) Comparison of JFET and MOSFET (5 points).
4) Applications of FETS