PANIPAT INSTITUTE OF ENGINEERING & TECHNOLOGY

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MPI

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Microprocessor

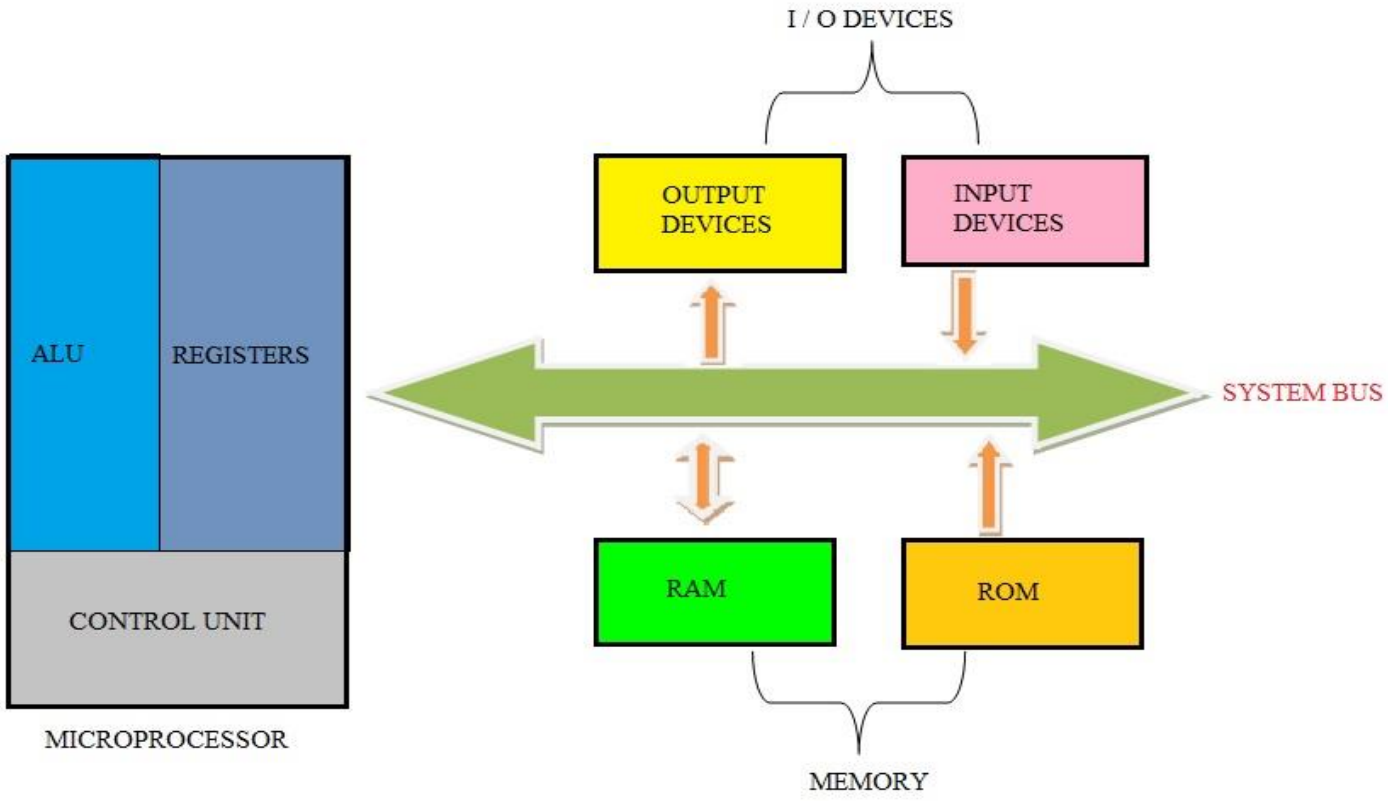
Microprocessors are the most-complicated ICs.

They are composed of billions of transistors that have been configured as thousands of individual digital circuits, each of which performs some specific logic function.

A microprocessor is built entirely of these logic circuits synchronized to each other.

Microprocessors typically contain the central processing unit (CPU) of a computer.

Block diagram of computer system



1.Microprocessor :

Microprocessor is a multipurpose programmable logic device that reads binary instruction from a storage device memory and accept binary data as input and processes the instruction for execution.

2. Memory

physical devices used to store data or programs (sequences of instructions) on a temporary or permanent basis for use in an electronic digital computer.

Computer main memory comes in two principal varieties: random-access memory (RAM) and read-only memory (ROM).

RAM can be read and written to anytime the CPU commands it, but ROM is pre-loaded with data and software that never changes, so the CPU can only read from it.

ROM is typically used to store the computer's initial start-up instructions.

In general, the contents of RAM are erased when the power to the computer is turned off, but ROM retains its data indefinitely.

In a PC, the ROM contains a specialized program called the BIOS that orchestrates loading the computer's operating system from the hard disk drive into RAM whenever the computer is turned

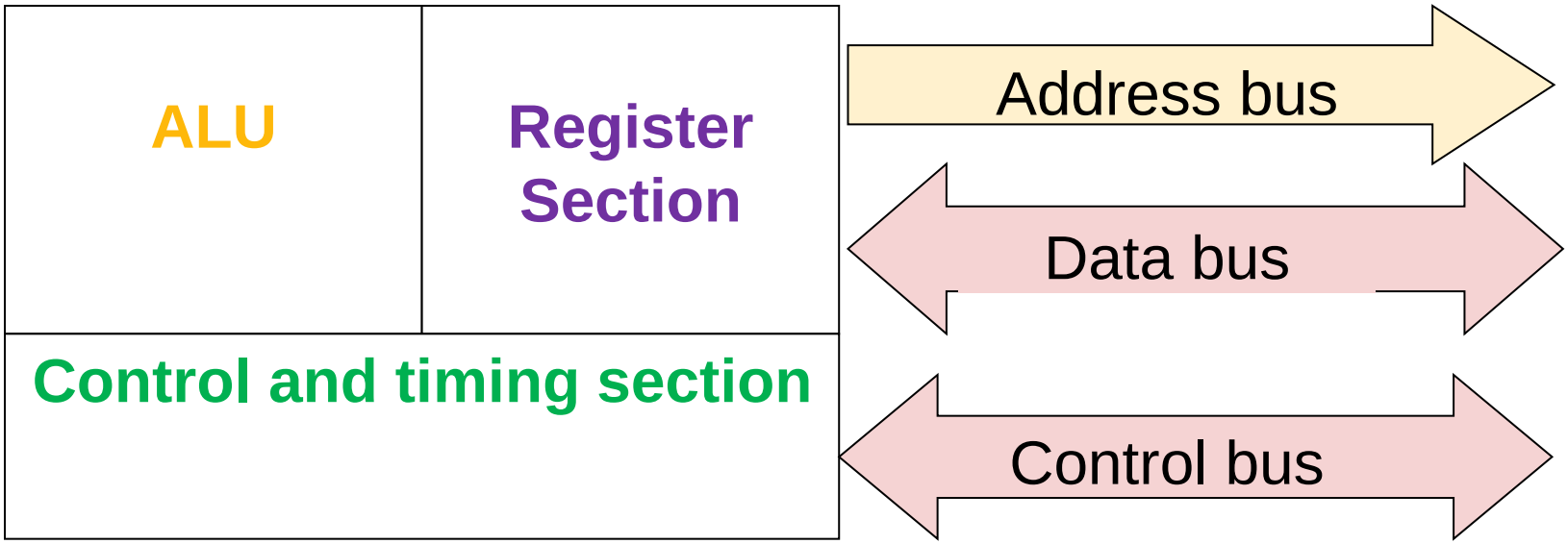
3. I/O Unit

Input/output (I/O), refers to the communication between an information processing system (such as a computer), and the outside world possibly a human, or another information processing system.

Inputs are the signals or data received by the system, and outputs are the signals or data sent from it

Devices that provide input or output to the computer are called peripherals

On a typical personal computer, peripherals include input devices like the keyboard and mouse, and output devices such as the display and printer. Hard disk drives, floppy disk drives and optical disc drives serve as both input and output devices. Computer networking is another form of I/O



Data Bus: A collection of wires in which data is transmitted from one computer to another external drive. The data bus carries digital information. The data bus is connected to the inputs of several gates and to the outputs of several gates. This is also called bi-directional bus because information may flow on the bus wires in both directions.

Address Bus An address bus is a computer bus (a series of lines connecting two or more devices) that is used to specify a physical address. The width of the address bus determines the amount of memory a system can address. It transfers the address of the location. It is called uni-directional because it transfers address from C.P.U to memory only.

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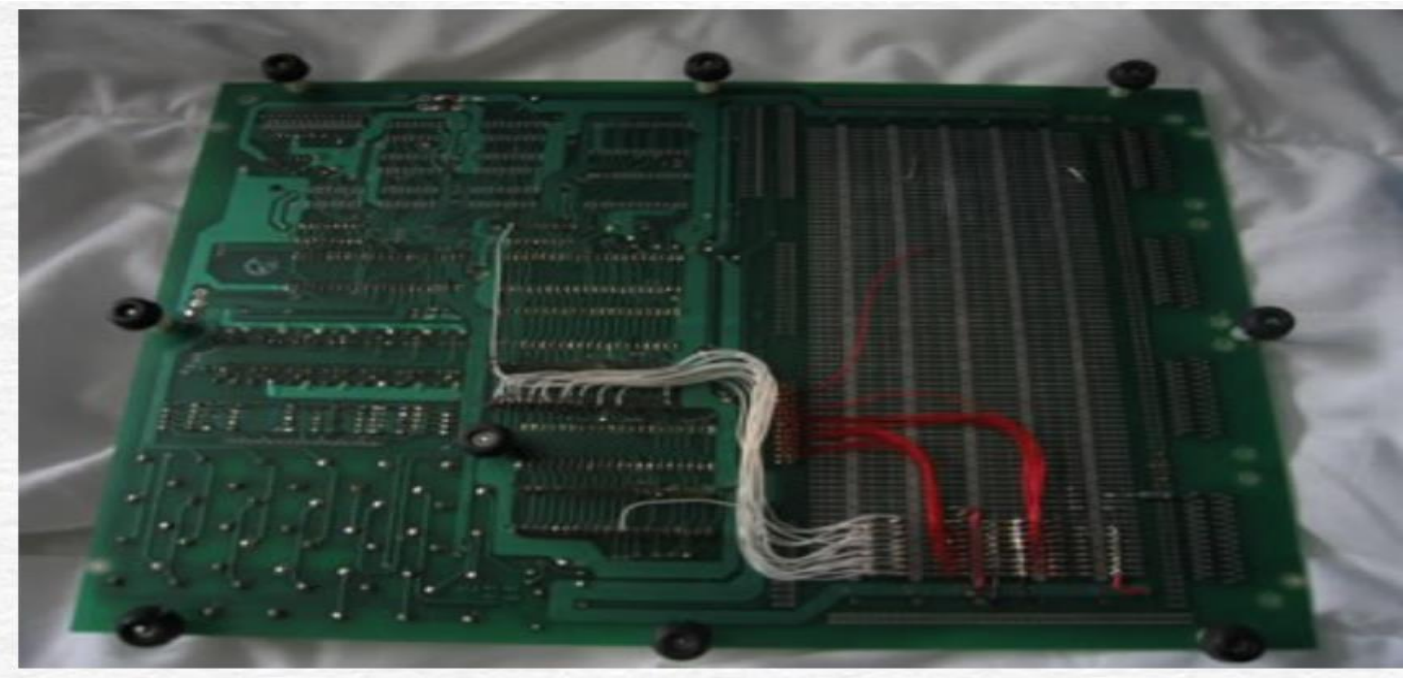


ALU and CU

An arithmetic-logic unit (ALU) is the part of a CPU that carries out arithmetic and logic operations on the operands in computer instruction words. The ALU includes storage places for input operands, operands that are being added, the accumulated result (stored in an accumulator), and shifted results. It performs arithmetic operations like addition, subtraction, increment, decrement etc. It also performs logical operations like AND, OR, X-OR, Complement etc

Control Unit: C.P.U is partitioned into A.L.U & C.U. The function of control unit is to generate the relevant timing & control signals to all operations in the computer. It controls the flow of the data between the processor & memory & peripherals.

CPU operation

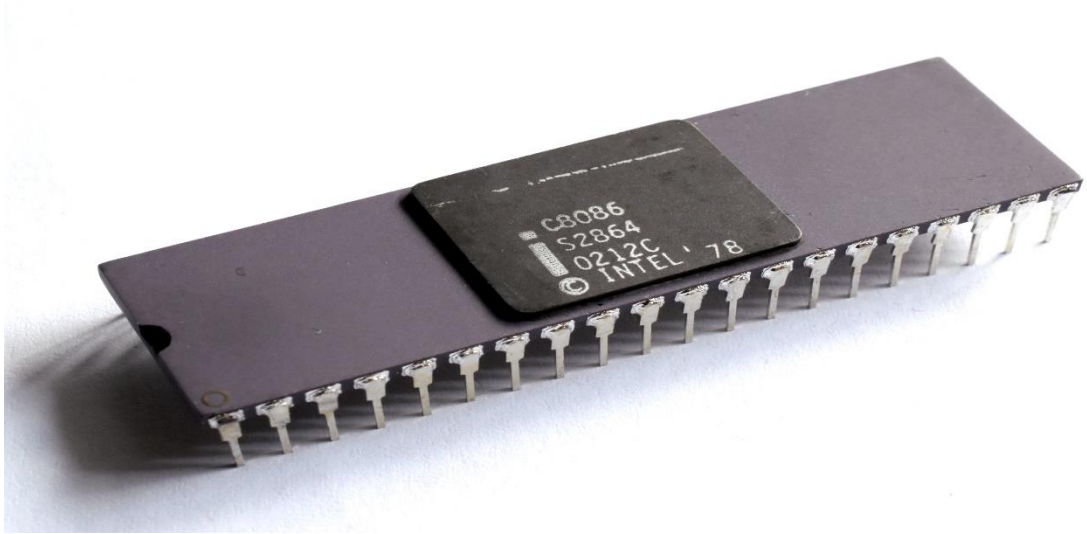
1.**Instruction Fetching**: To fetch instruction from memory microprocessor does the following steps

a. Processor sends address of instruction present in instruction pointer register on address bus.
b. Next memory read control signal is sent on control line by processor to activate /enable memory.

2.**Decoding the instruction:** Instruction is decoded into a series of simple actions by Instruction decoder.

3.**Execution:** Series of action are performed by processor. For example :arithmetic operations or data tranfer between registers,data input from port.

Overview of 8086 Microprocessor



- In April 1978, Intel introduced its first 16 bit microprocessor. Production started in May, eventually, the 8086 was officially released on June 8.

Features of 8086

The most prominent features of a 8086 microprocessor are as follows −

- **It is a 16-bit microprocessor.**
- **8086 has a 20 bit address bus can access up to** 2^20 **(1 MB) memory locations.**
- **It can support up to 64K I/O ports.**
- **It provides 14, 16 -bit registers.**
- **Word size is 16 bits.**
- **It has multiplexed address and data bus AD0- AD15 and A16 – A19.**

Features of 8086

- 8086 is designed to operate in two modes, Minimum and Maximum.
- It can pre fetches up to 6 instruction bytes from memory and queues them in order to speed up instruction execution.
- It requires +5V power supply.
- A 40 pin dual in line package.
- Address ranges from 00000H to FFFFFH
- Memory is byte addressable - Every byte has a separate address.

Intel 8086 Internal Architecture

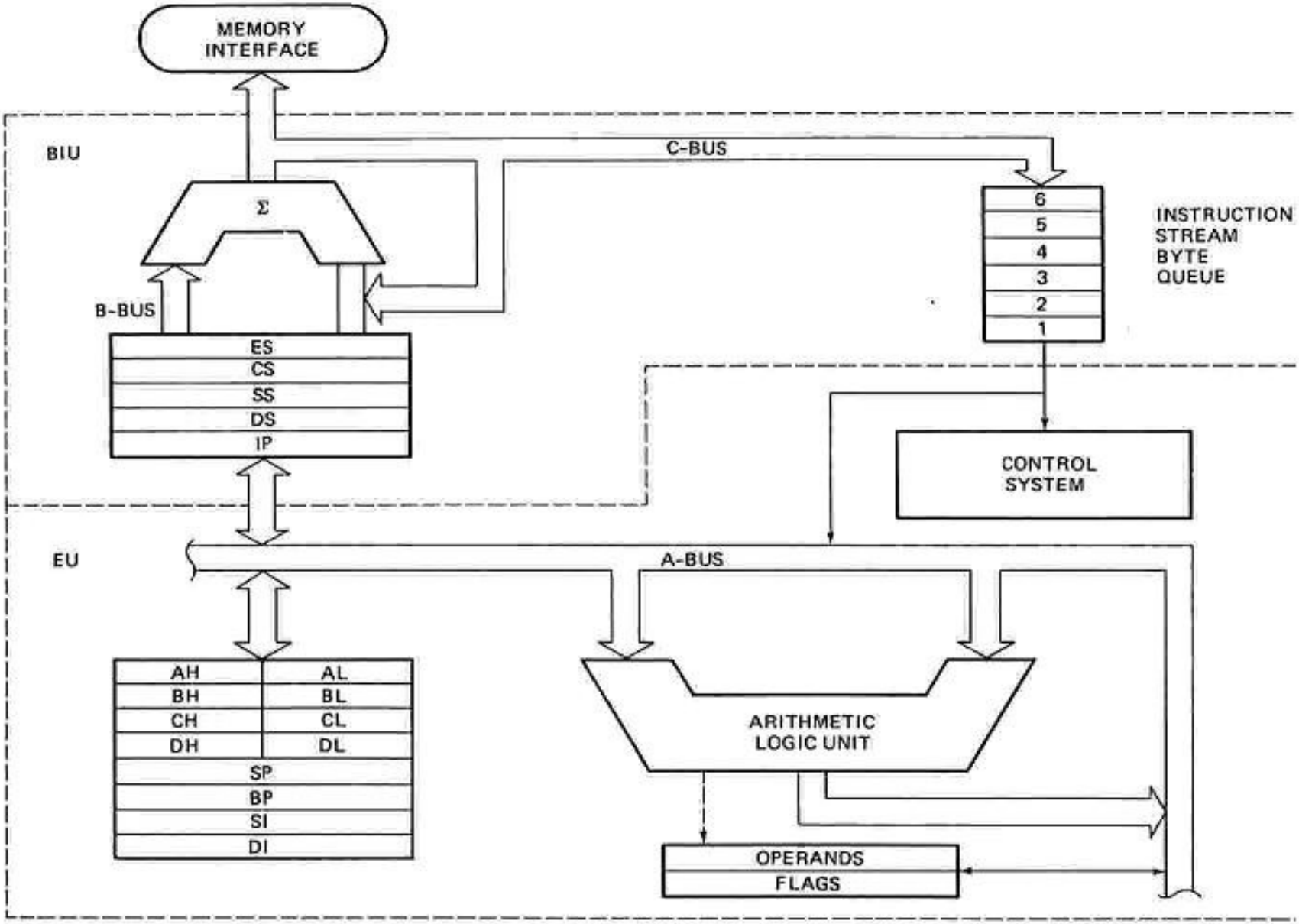
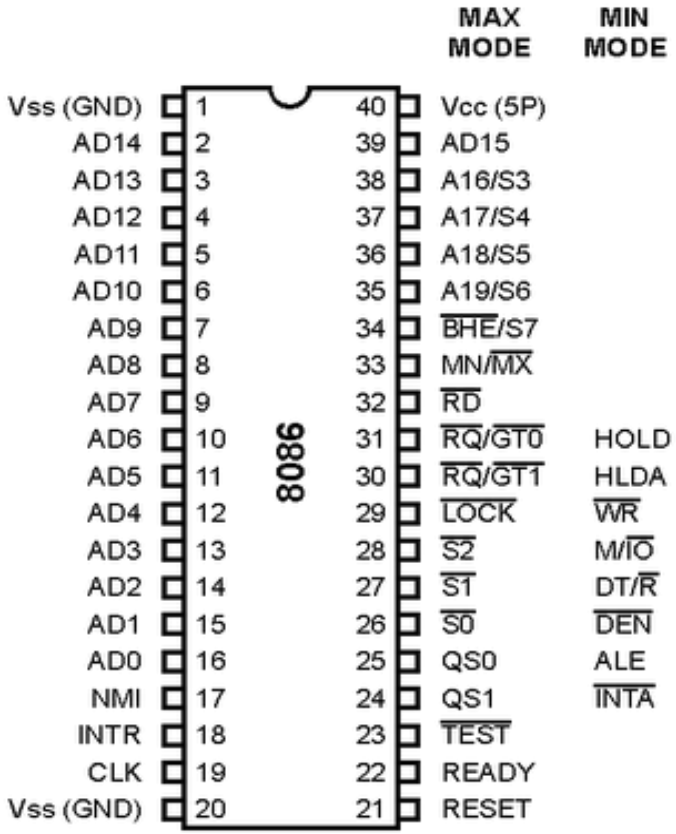


FIGURE 8086 internal block diagram. (*Intel Corp.*)

Architecture Diagram of 8086



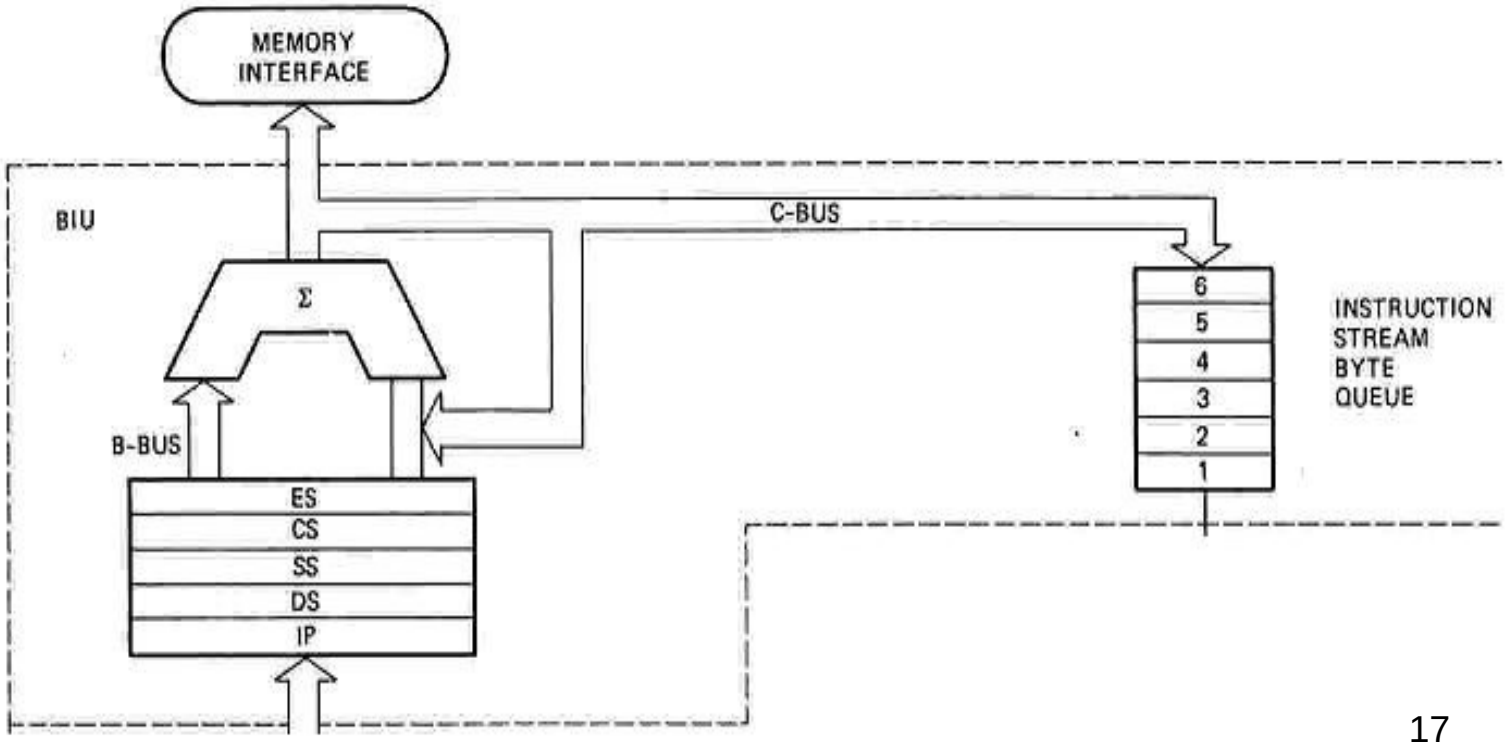
Internal architecture of 8086

- 8086 has two blocks BIU and EU.
- The BIU handles all transactions of data and addresses on the buses for EU.

- BIU fetches instructions, reads data from memory and I/O ports, writes data to memory and I/ O ports.
- Translates 16-bit Logical Address to 20 bit Physical Address.
- The instruction bytes are transferred to instruction queue.
- EU executes instructions from the instruction system byte queue

BUS INTERFACE UNIT (BIU)

- 6-byte Instruction Queue (Q)
- The Segment Registers (CS, DS, ES, SS). The Instruction Pointer (IP).
- The Address Summing block (Σ)



Instruction Queue

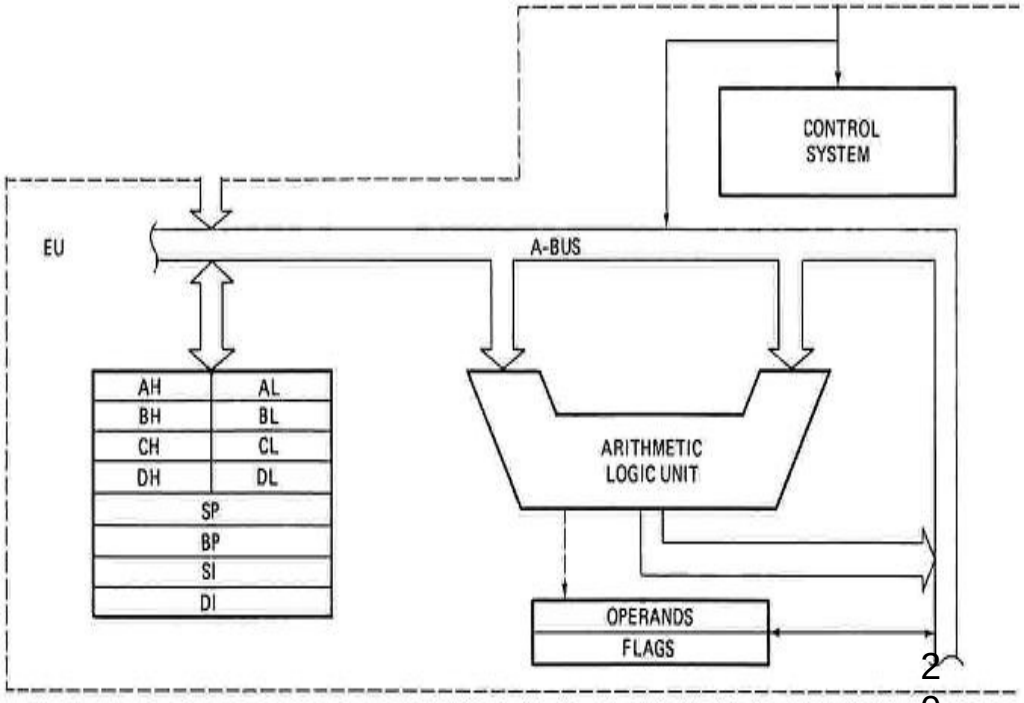
- 8086 employs parallel processing
- When EU is busy decoding or executing current instruction, the buses of 8086 **may not be** in use.
- At that time, BIU can use buses to fetch upto six instruction bytes for the following instructions
- BIU stores these pre-fetched bytes in a **FIFO** register called Instruction **Queue**
- When EU is ready for its next instruction, it simply reads the instruction from the queue in BIU

Pipelining

- EU of 8086 does not have to wait in between for BIU to
  fetch next instruction byte from memory
- So the presence of a queue in 8086
  speeds up the processing
- Fetching the next instruction while the current instruction executes is called pipelining

EXECUTION UNIT

- Decodes instructions fetched by the BIU
- Generate control signals,
- Executes instructions.



EU (Execution Unit)

- Main components are-
  - **Instruction Decoder**
  - **Control System**
  - **Arithmetic Logic Unit**
  - **General Purpose Registers**
  - **Flag Register**
  - **Pointer & Index registers**

Instruction Decoder

- Translates instructions fetched from memory into a series of actions which EU carries out

Control System

- Generates timing and control signals to perform the internal operations of the microprocessor

Arithmetic Logic Unit

- EU has a 16-bit ALU which can ADD, SUBTRACT, AND, OR, increment, decrement, complement or shift binary numbers

General Purpose Registers

- EU has 8 general purpose registers
- Can be individually used for storing 8-bit data
- AL register is also called Accumulator
- Two registers can also be combined to form 16-bit registers
- The valid register pairs are – AX, BX, CX, DX

AH	AL
BH	BL
CH	CL
DH	DL

AH	AL	AX
BH	BL	BX
CH	CL	CX
DH	DL	DX

Register	Name of the Register	Special Function
AX	16-bit Accumulator	Stores the 16-bit results of arithmetic and logic operations
AL	8-bit Accumulator	Stores the 8-bit results of arithmetic and logic operations
BX	Base register	holds base value in base addressing mode to access memory data
CX	Count Register	holds the count value in SHIFT, ROTATE and LOOP instructions
DX	Data Register	Used to hold data for multiplication and division operations
SP	Stack Pointer	Used to hold the offset address of top stack memory
BP	Base Pointer	Used to hold the base value in base addressing using SS register to access data from stack memory
SI	Source Index	Used to hold index value of source operand (data) for string instructions
DI	Data Index	Used to hold the index value of destination operand (data) for string operations

Flag Register

- 8086 has a 16-bit flag register
- Contains 9 active flags
- There are two types of flags in 8086
  - **Conditional flags – six flags, set or reset by EU on the basis of results of some arithmetic operations**
  - **Control flags – three flags, used to control certain operations of the processor**

Flag Register

U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF

1.	CF	CARRY FLAG	**Conditional Flags** **(Compatible with 8085, except OF)**
2.	PF	PARITY FLAG	
3.	AF	AUXILIARY CARRY	
4.	ZF	ZERO FLAG	
5.	SF	SIGN FLAG	
6.	OF	OVERFLOW FLAG	
7.	TF	TRAP FLAG	**Control Flags**
8.	IF	INTERRUPT FLAG	
9.	DF	DIRECTION FLAG	

EXECUTION UNIT – Flag Register

Flag	Purpose
Carry (CF)	Holds the carry after addition or the borrow after subtraction. Also indicates some error conditions, as dictated by some programs and procedures .
Parity (PF)	PF=0;odd parity, PF=1;even parity.
Auxiliary (AF)	Holds the carry (half – carry) after addition or borrow after subtraction between bit positions 3 and 4 of the result (for example, in BCD addition or subtraction.)
Zero (ZF)	Shows the result of the arithmetic or logic operation. Z=1; result is zero. Z=0; The result is 0
Sign (SF)	Holds the sign of the result after an arithmetic/logic instruction execution. S=1; negative, S=0

Flag	Purpose
Trap (TF)	A control flag. Enables the trapping through an on-chip debugging feature.
Interrupt (IF)	A control flag. Controls the operation of the INTR (interrupt request) I=0; INTR pin disabled. I=1; INTR pin enabled.
Direction (DF)	A control flag. It selects either the increment or decrement mode for DI and /or SI registers during the string instructions.
Overflow (OF)	Overflow occurs when signed numbers are added or subtracted. An overflow indicates the result has exceeded the capacity of the Machine

Execution unit – Flag Register

- Six of the flags are status indicators reflecting properties of the last arithmetic or logical instruction.
- For example, if register AL = 7Fh and the instruction ADD AL,1 is executed then the following happen

AL = 80h

CF = 0; there is no carry out of bit 7
PF = 0; 80h has an odd number of ones **AF = 1**; there is a carry out of bit 3 into bit 4 **ZF = 0**; the result is not zero

SF = 1; bit seven is one

OF = 1; the sign bit has changed

Memory Segmentation

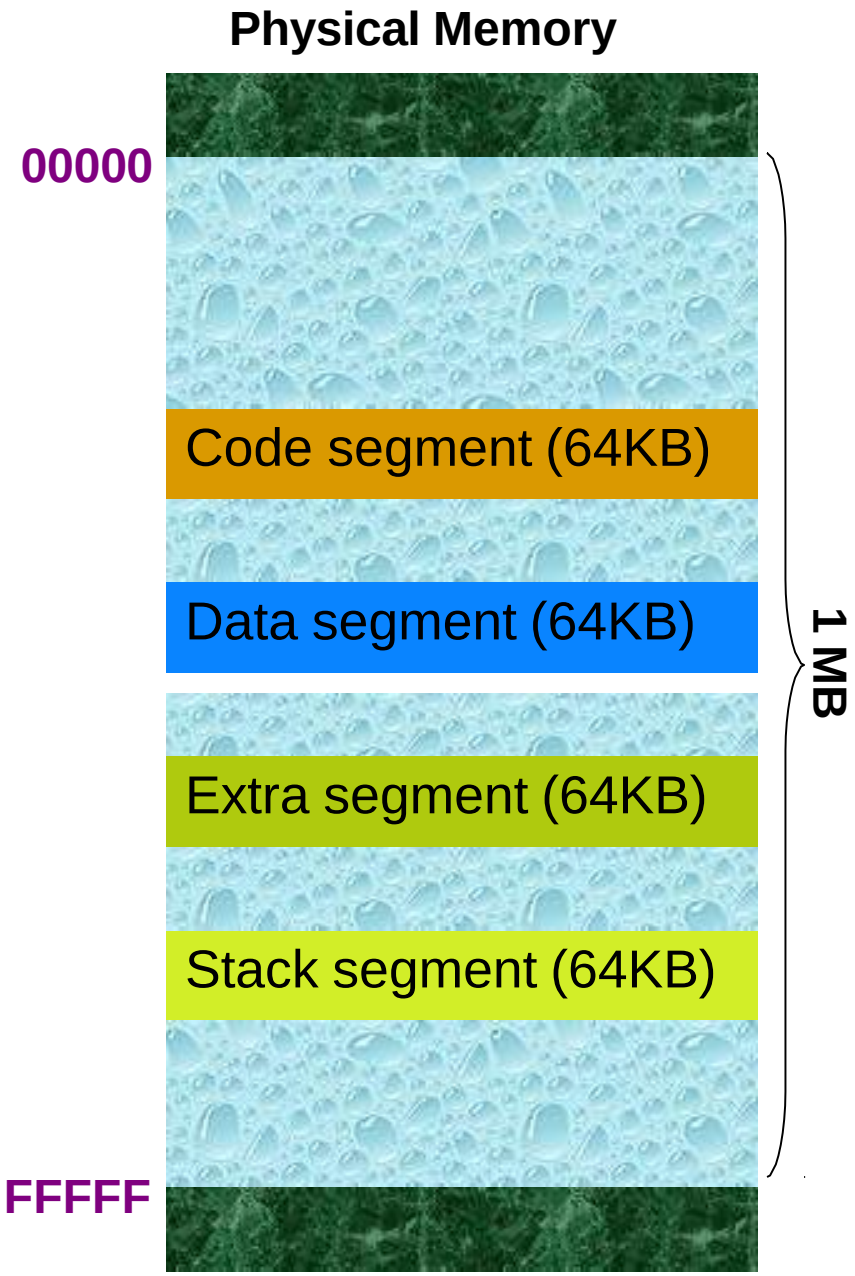
- 8086 has a **20-bit** address bus
- So it can address a maximum of **1MB** of memory
- 8086 can work with only **four 64KB segments** at a time within this 1MB range
- These four memory segments are called
  - **Code** segment
  - **Stack** segment
  - **Data** segment
  - **Extra** segment

Segmented Memory

The memory in an 8086/88 based system is organized as segmented memory.

The CPU 8086 is able to address 1Mbyte of memory.

The Complete physically available memory may be divided into a number of logical segments.



Code Segment

- Code segment is used for storing the instructions .From this **part of memory BIU fetches instruction code bytes.**

Stack Segment

- **A section of memory set aside to store return addresses and data while a subprogram executes**

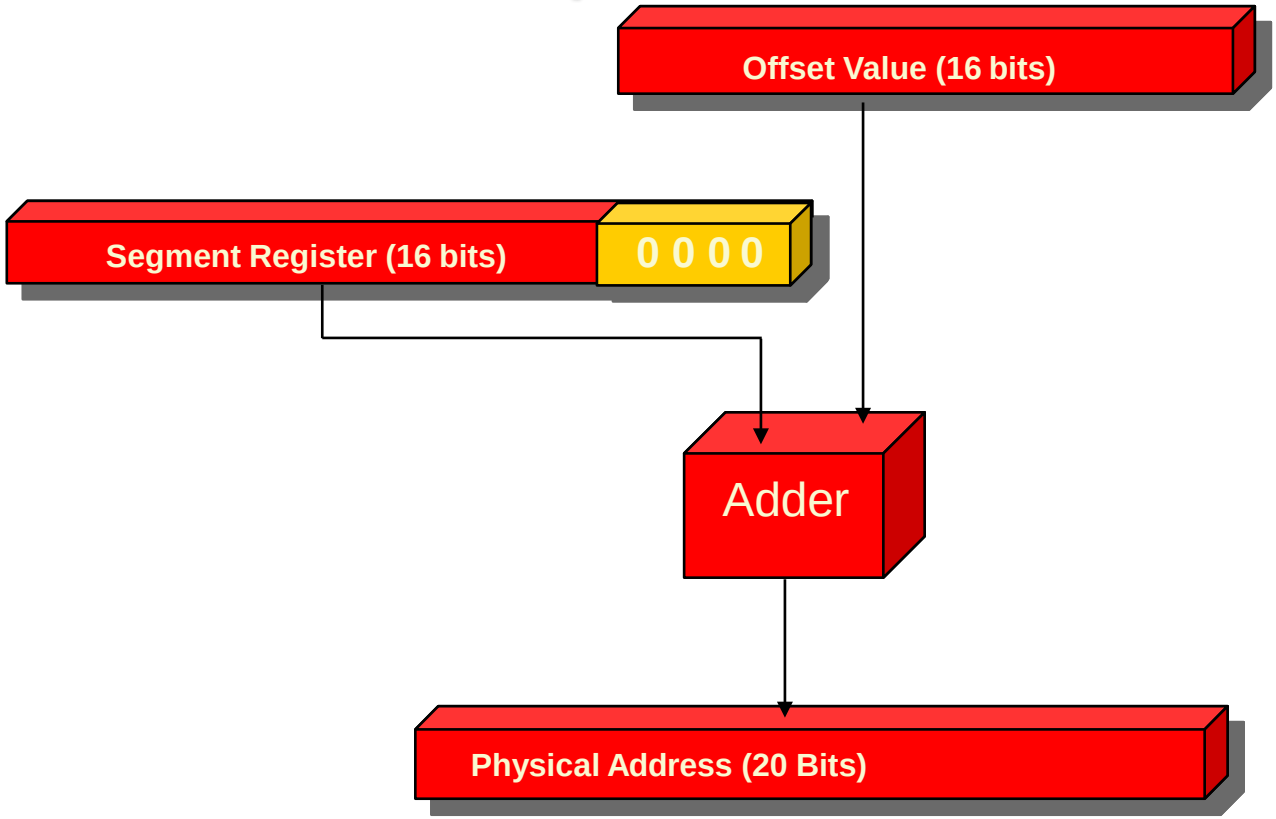
Data & Extra Segments

- **Used for storing data values to be used in the program**

Segment registers

- In 8086/88 the processors have 4 segments registers
- Code Segment register (CS), Data Segment register (DS), Extra Segment register (ES) and Stack Segment (SS) register.
- All are 16 bit registers.
- Each of the Segment registers store the upper 16 bit(OR 4 hexadecimal digit) address of the starting address(Base Address) of the corresponding segments.

Memory Address Generation



Segment Registers present in BIU

Code Segment register:
CS holds the base address for the Code Segment. All programs are stored in the Code Segment and accessed via the IP.
Data Segment register:
DS holds the base address for the Data Segment.
Stack Segment register:
SS holds the base address for the Stack Segment.
Extra Segment register:
ES holds the base address for the Extra Segment.
Address Generation Circuit:
•The BIU has a Physical Address Generation Circuit.
•It generates the 20 bit physical address using Segment and Offset addresses using the formula:`Physical Address = Segment Address x 10H + Offset Address`

Index and Pointer registers

Instruction Pointer (IP):
It is a 16 bit register. It holds offset of the next instructions in the Code Segment.

IP is incremented after every instruction byte is fetched.

IP gets a new value whenever a branch instruction occurs.

CS is multiplied by 10H to give the 20 bit physical address of the Code Segment.

Address of the next instruction is calculated as CS x 10H + IP.

8086 Microprocessor Architecture

Example:

```
CS = 4321H IP = 1000H then CS x 10H = 43210H
+ offset = 44210H
```

This is the address of the instruction.

Index and Pointer registers

Special purpose registers (16-bit):These registers contains the offset address of different segment presnt in memory

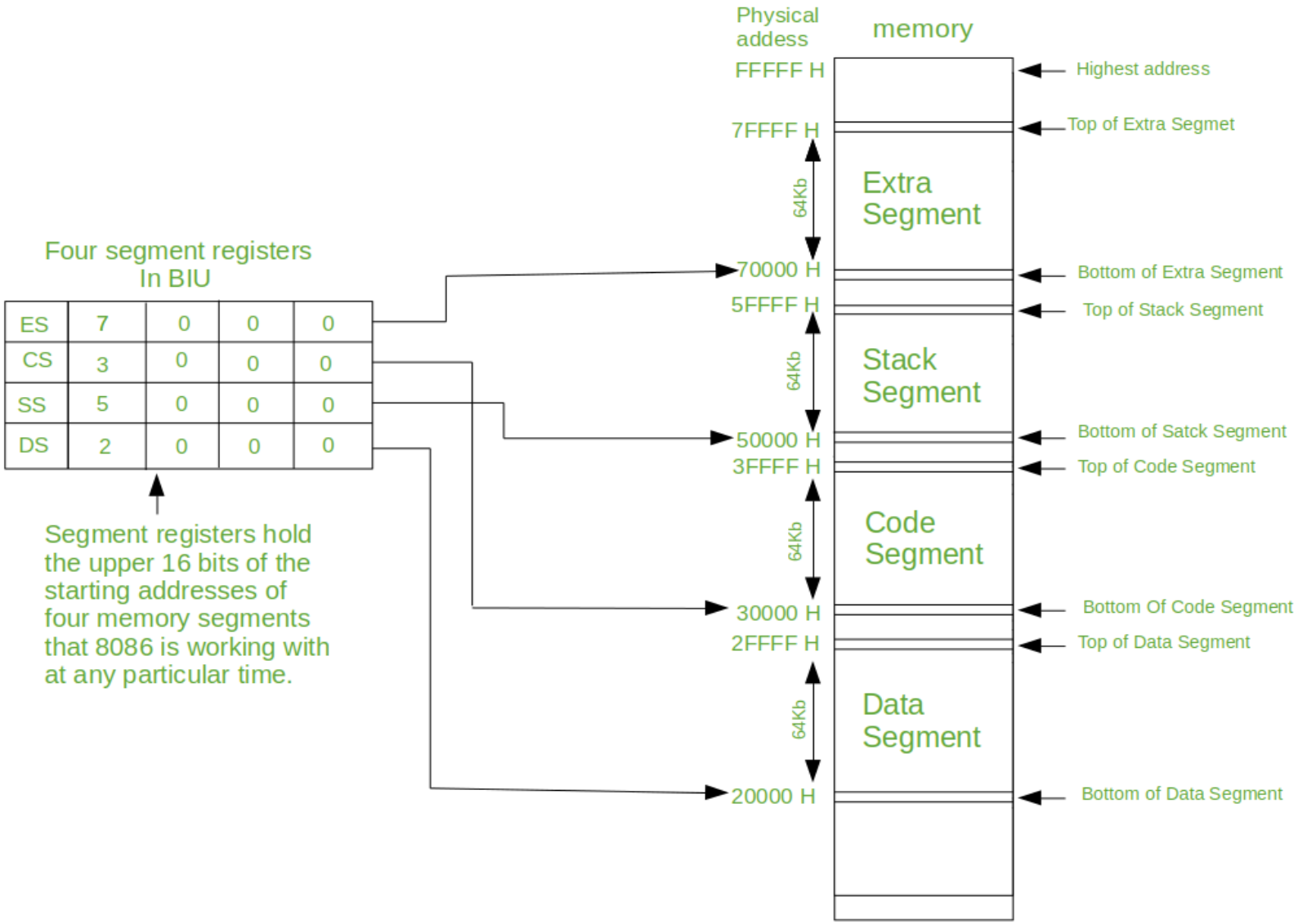
Stack Pointer:
Points to Stack top. Stack is in Stack Segment, used during instructions like PUSH, POP, CALL, RET etc.

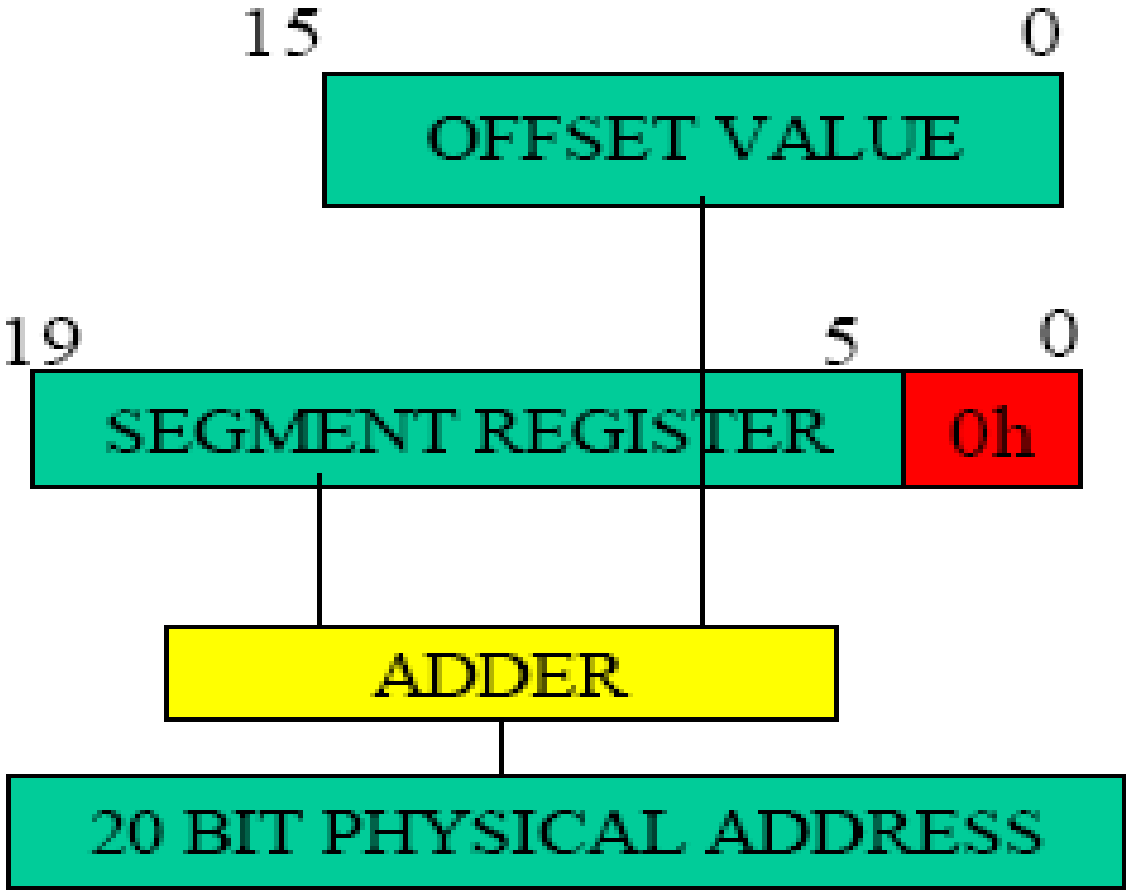
Base Pointer:
BP can hold offset address of any location in the stack segment. It is used to access random locations of the stack.

Source Index:
It holds offset address in Data Segment during string operations.

Destination Index:
It holds offset address in Extra Segment during string operations.

8086 Microprocessor Memory Segmentation



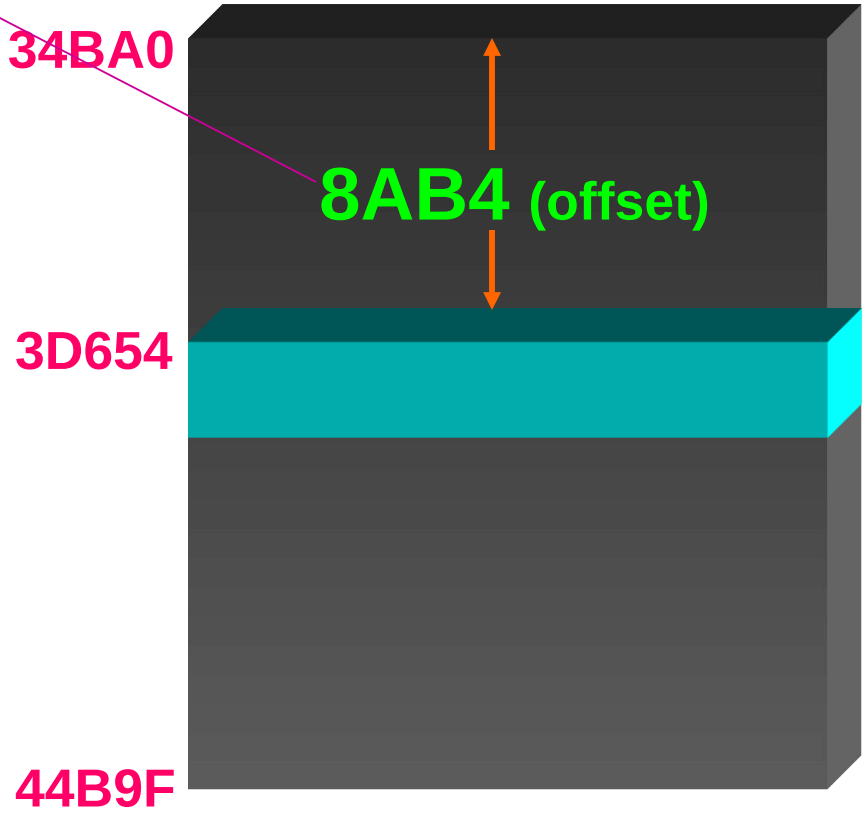

15
0
OFFSET VALUE
19
5
0
SEGMENT REGISTER
0h
ADDER
20 BIT PHYSICAL ADDRESS

The following examples shows the CS:IP

CS 34BA

IP 8AB4

Code segment

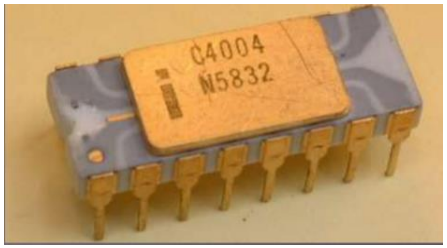


Inserting a hexadecimal 0H (0000B) with the CSR or shifting the CSR four binary digits left

3 4 B A 0 (C S) +
8 A B 4 (I P)
---
3 D 6 5 4 (next address)

Segment and Address register combination

- CS:IP
- SS:SP SS:BP
- DS:BX DS:SI
- DS:DI (for other than string operations)
- ES:DI (for string operations)


C4004
W5832


D8085AH-1
K031584
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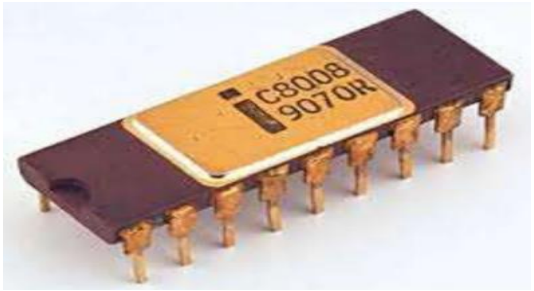
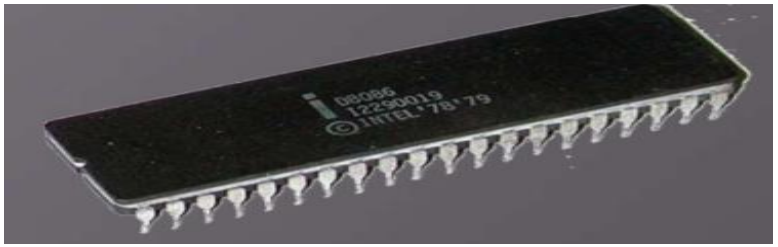

C8008
9070R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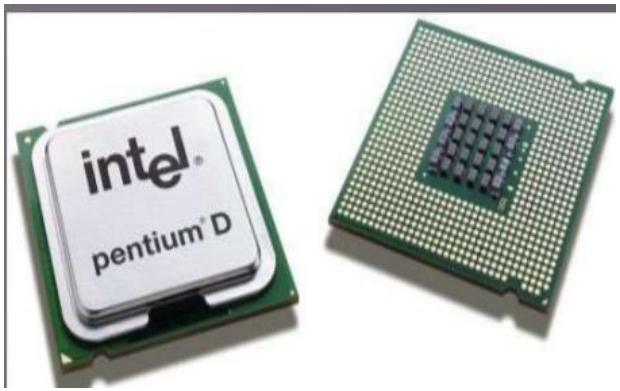
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