

Technical Specification

Aim: To study familiarization with digital trainers
kit and associated equipment

Size of Bread Board	172.5 mm x 128.5 mm
connection on Bread Board	1685
DC power supply on bread board	+5V 1A, -5V 500mA +3V, -15V 500mA -3V, -15V 50 mA
Pulse generation on bread board	Frequency range: 1Hz in steps variable in amplitude: 3V-15V (cmos)
Puller switches	2 NOS (push to on)
Data switches	8 NOS (Toggie switches TTL & CMOS made)
LED display	8 NOS (TTL/CMOS made)
BCD to 7 Segment display	2 NOS
Logic Probe	Logic level indicator for TTL (7 segment)
Weight	3 kg. approx
Dimension (mm)	W490 x H100 x D25
Power requirement	230V +/- 10%, 50 Hz

Aim :- To study familiarization with digital trainer kit and associated equipment

Apparatus:- Digital trainer kit .

Theory :-

- DC power:- This block provides fixed DC output of +5V and -5V provide variable DC output from +3V to +15V and -3V to -15V .

Pulse generation:- This block generate stable pulse of frequency range 10 Hz to 1MHz with TTL & CMOS mode . When TTL mode is selected amplitude of pulse will be compatible with TTL & when CMOS mode is compatible mode is selected it is compatible with CMOS .

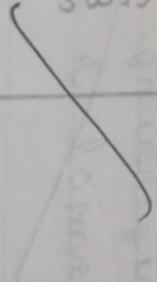
Pulse switch:- Two pulse switch are provided for triggering purpose . Each has two O/P normal & complementary .

Output levels = High = 5V , Low = 0V

CMOS: High = +3V to +15V

Low = 0V

DC power supply	Suen Teh ST2611	power
Pulse generator	Bread board	8-bit LED display
polar switches	8-bit data switcher	mode selector
	Digital trainer Kit	Digital display
		Logic probe



V21405 V21406 V21407 V21408 V21409 V21410 V21411 V21412 V21413 V21414

Normal

- 8 bit Data switches :- These switches provide 2 states high and low TTL.
high = 5V , Low = 0V
CMOS : High = 3V to 15V
Low = 0V
- Logic Probe :- When (output) input given to this block is high whether CMOS or TTL, the display will show H. When input is low, it will show L. When no input is given it will show 0 and in case of transmission V.
- Digital display :- Two digital displays we provide these are BCD to 7 segment displays which convert BCD to equipment display numbers.
- Made selector switch :- When the switch is put on TTL or CMOS position, the output of pulse generator pulses switch, 8 bits data switches and input of digital probes 8 bits LED display will meet the high or low level of TTL or CMOS.

~~Made selector switch to TTL position :-~~

~~Low level = 0V, High level = 5V~~

~~Transistor = HI > LO OR LO > HI~~

- 8 bits LED Display :- When Input to this block is high, LED will glow green. There will be no display for open.
- Made selector switch to CMOS position:
Low level = 0V
High level = 3V to 15V
 $T_{transit} = H_I > L_O \text{ or } L_O > H_I$
- Operating instruction and power control description:-
The trainer is equipped with built-in DC power supply. When ON/OFF switch of the trainer is turned on, the power LED indicator will be indicating that trainer is ON, the power LED when +V and -V potentiometer of DC power blocks one in their fully clockwise position, fully voltage +15V and -15V is obtained, +V and -V potentiometer can be varied to get variable position and negative supply from +3V to +15V and -3V to -15V. When +V volt is varied CMOS voltage level will be varied proportionally, so whenever CMOS mode is used carefully check the +V volt position.

Frequency potentiometer of pulse generator is used for time setting of frequency of pulse

Result :- we have studied digital trainer
kit and associated equipments

Experiment :

Date _____

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range switch is used to vary frequency from 10 Hz to 1 MHz in six steps freq. below 10 Hz can be obtained by freq. blot one moment only switches. As long as those are pressed indicated output are obtained. 8 bit data switches when in position will give low o/p when ON/OFF switches of digital are turned ON, it will on the display. When TTL/CMOS switch is put on TTL or CMOS position the O/P of pulse generator, pulses switches, input of digital brobe 8 bit, LED display will meet the high or low level of TTL or CMOS.

Result :-

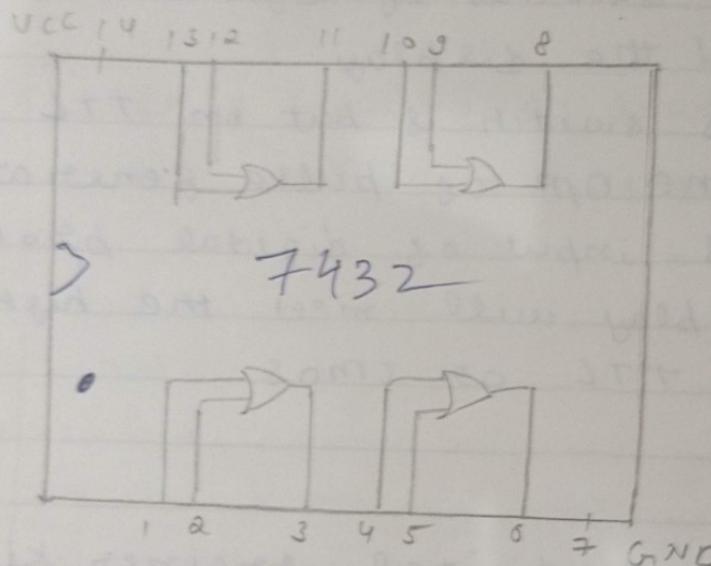
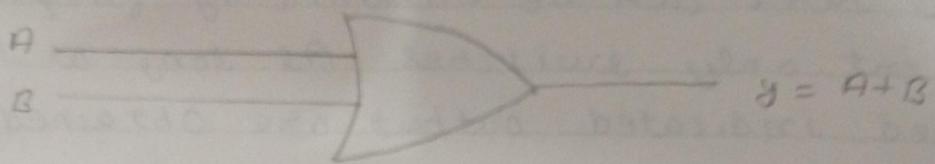
We have studied digital trainer kit and associated equipments.

Dence

Aim:- To study operations of all logic gates.

Apparatus:-

(i) OR gate:-



IC - 7432

	I/P	O/P
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Aim:- To study operation of all logic gate.

Apparatus required:-

component	quantity
IC 7408 = Input AND gate	1
IC 7432 = I/P OR gate	1
IC 7400 = I/P NAND gate	1
IC 7486 = I/P EXOR gate	1
IC 7402 = I/P NOR gate	1

Theory:-

- AND gate:- In this the o/p will be 1 only when all input will be high we can supply n no. of units.
- OR gate:- In this the o/p of OR gate is 0 only when if all the I/P one low. we can supply n. no. of units.
- NOT gate:- If perform the function of converter and has only one I/P. IC no. of this gate is 7404.

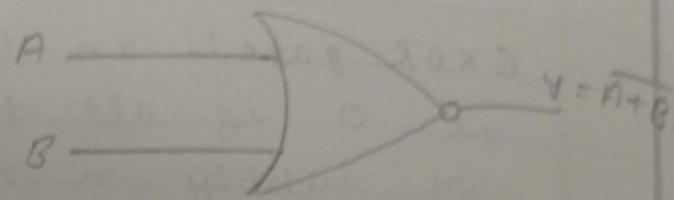
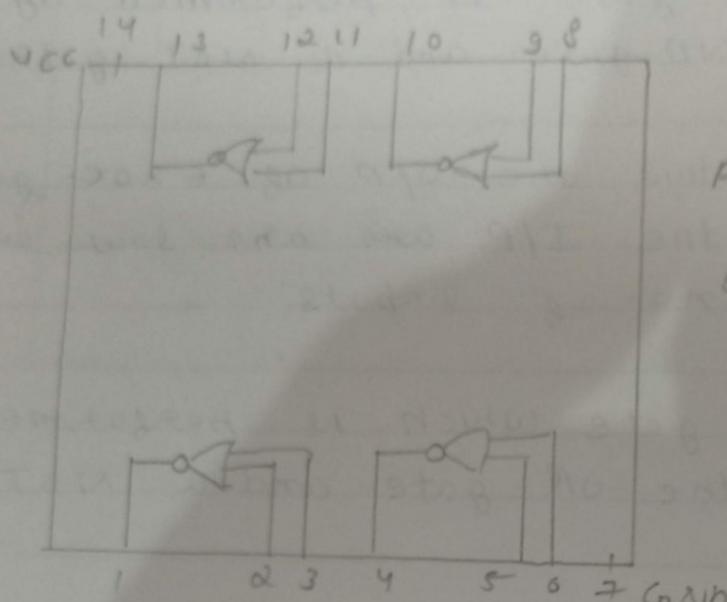
- NAND gate - This gate is performed by combining the AND gate and a NOT gate.
- XOR gate :- In this the O/P of XOR gate is 0 if all the I/P are low we can supply n no. of inputs.
- NOR gate :- The gate which is performed by combining the OR gate and a NOT gate.

PROCEDURE :-

- AND gate :-

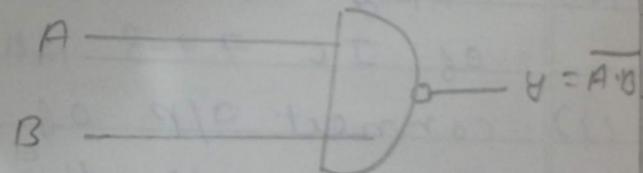
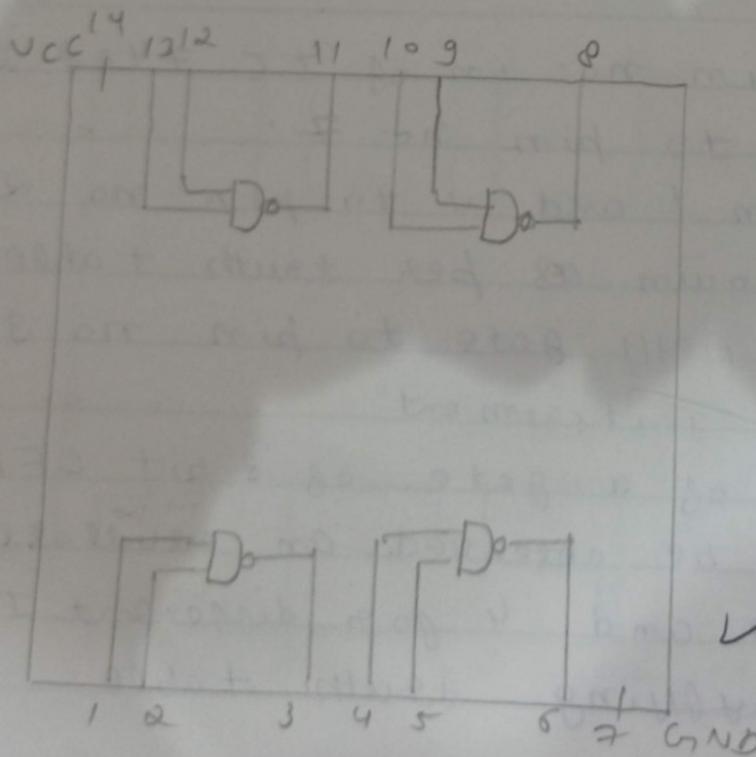
- (1) connect +5V to pin no. 14 of IC 7408 and connect ground to pin no. 7.
- (2) Apply OV to pin 1 and IV to pin no. 2 of IC 7408 shown as per truth table.
- (3) connect O/P of AND gate to pin no 3.
- (4) switch OV to the ~~Interconnect~~.
- (5) observe ~~output~~ of a gate of 8 bit LED display O/P can be observed on oscilloscope.
- (6) repeat step 2, 3 and 4 for different I/P combination varying truth table.

4. NOR Gate



	A	B	Y
	0	0	1
	0	1	0
	1	0	0
	1	1	0

5. NAND Gate



	A	B	Y
	0	0	1
	0	1	1
	1	0	1
	1	1	0

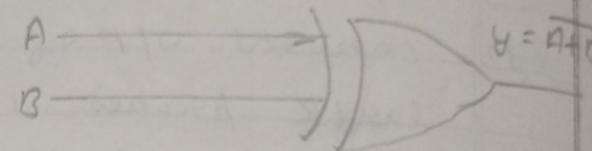
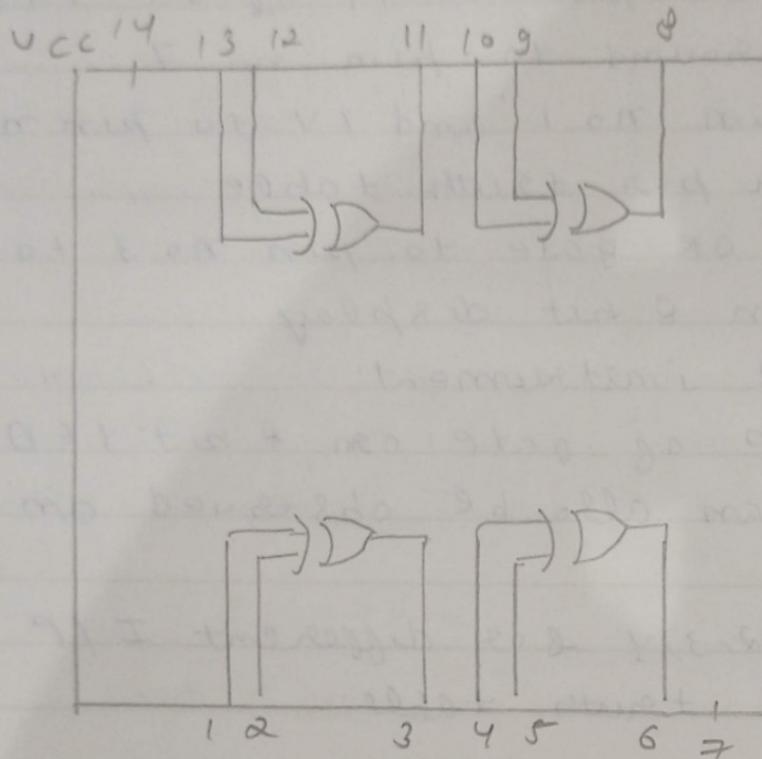
- OR gate:-

- (1) connect +5V to pin no. 14 of IC 7432 and connect ground to pin no. 7.
- (2) Apply OV to pin no. 1 and IV to pin no. 2 of IC 7432 as per truth table.
- (3) connect O/P of OR gate to pin no. 3 to of logic probe in 8 bit display.
- (4) Switch ON the instrument.
- (5) observe the O/P of gate on 8 bit LED display O/P can also be observed on oscilloscope.
- (6) Repeat step 2, 3, 4 & 5 for different I/P combination verifying truth table.

- NAND gate:-

- (1) connect +5V to pin no. 14 of IC 7400 and connect ground to pin no. 7.
- (2) Apply OV to pin no. 1 and IV to pin no. 2 of IC 7400 as per truth table.
- (3) connect O/P of NAND gate to pin no. 3 to I/P of logic probe or 8 bit display.
- (4) Switch ON the instrument.
- (5) observe the O/P of gate on 8 bit LED display O/P can also be observed on oscilloscope.
- (6) Repeat step 2, 3 and 4 for diff. I/P combination verifying truth table.

6. EXOR gate:



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

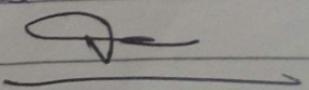
Result: We have studied operations of all logic gates.

EX-OR gate :-

- (1) connect +5V to pin no. 14 of IC 7486 and connect ground to pin no. 7.
- (2) Apply OV to pin no. 1 and IV to pin no. 2 of IC 7486 as per truth table.
- (3) connect o/p of Ex-OR gate to pin no. 3 to I/P of logic probe on 8 bit display.
- (4) switch ON the instrument.
- (5) observe the output of gate on 8 bit LED display O/P can also be observed on oscilloscope.
- (6) Repeat step 2, 3 and n for different I/P combination verifying truth table.

- NOR gate :-

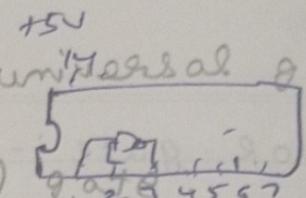
- (1) connect +5V to pin no. 14 of IC 7402 and connect ground to pin no. 7.
- (2) Apply OV to pin no. 2 and IV to pin no. 3 of IC 7402 as per truth table.
- (3) connect o/p of NOR gate to pin no. 1 to I/P of logic gate probe on 8 bit display.
- (4) ~~switch ON the instrument~~
- (5) ~~observe the o/p of gate on 8 bit display.~~
O/P can also be observed on oscilloscope.
- (6) Repeat step 2, 3 and je for different I/P combination verifying truth table'



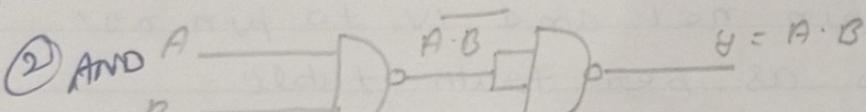
AIM: To study and verify universal gate

L NAND Gate $A = \overline{D} \cdot \overline{B}$

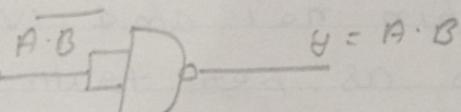
(1) AND gate using NAND



① NOT



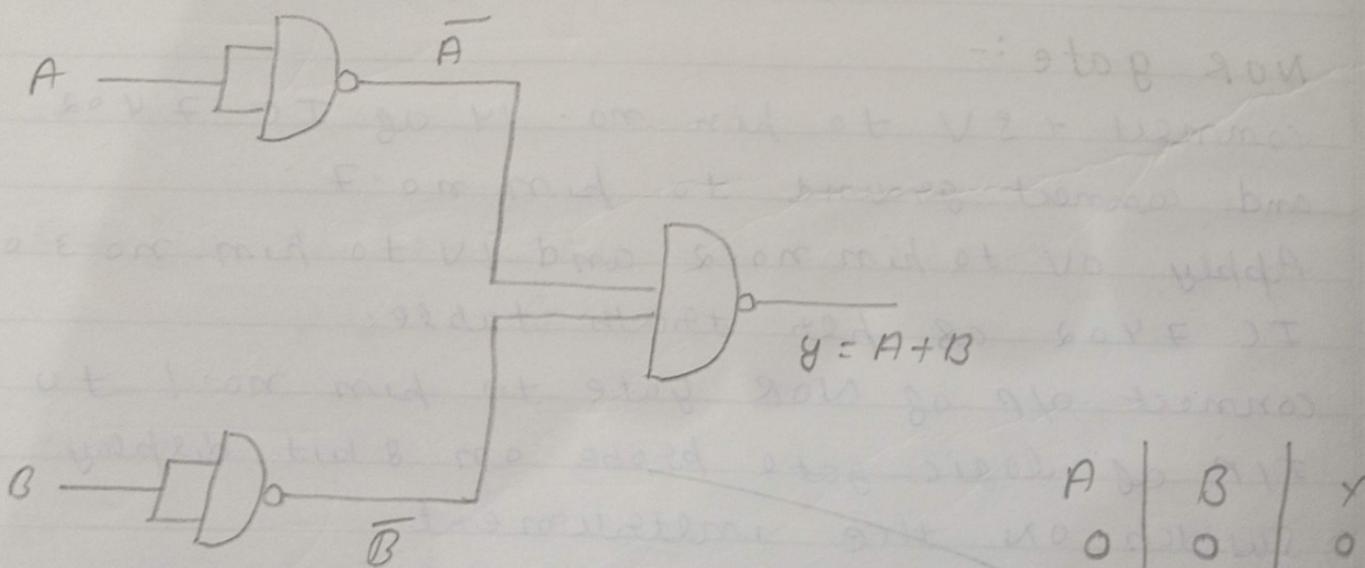
② AND



③ OR.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(2) OR gate using NAND gate:



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

-P

AIM:- To study and verify universal gates.

Apparatus:- Digital trainer kit, connecting wires
ICs of NAND and NOR gate.

Theory:-

(1) AND gate using NAND gate:-

1. The IC used in this NAND gate having
IC no 7400.

2. The input is given at pin no. 1, 2 and output
of 1, 2 is input at pin no. 4 and pins 4
and 5 are short circuited.

3. Pin no. 7 is grounded and 14 is connected
to power supply.

4. Output taken in AND gate from pin no. 6.

(2) OR gate using NAND gate:-

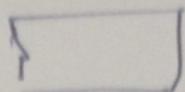
1. IC using in NAND gate having IC no 7400.

2. Input is given at 1, 4 and pin 1, 2 and
4, 5 are short circuited. Output of this pin
(1, 4) are input of pin (9, 10) and output
is taken from pin no. 8.

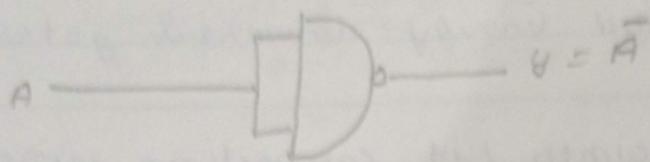
3. Output taken is equivalent to OR gate.

4. Pin no. 7 is connected to ground and
14 is connected to power.

NOR \Rightarrow

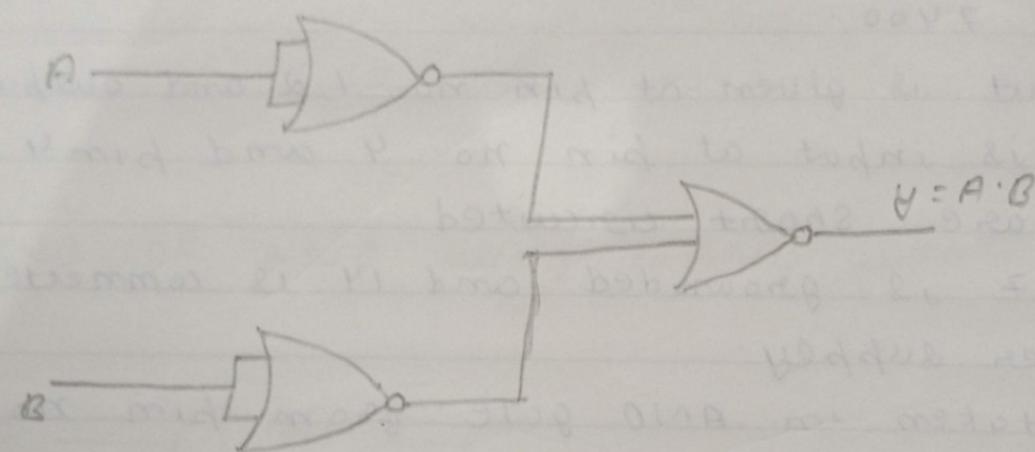


3. NOT using NAND gate



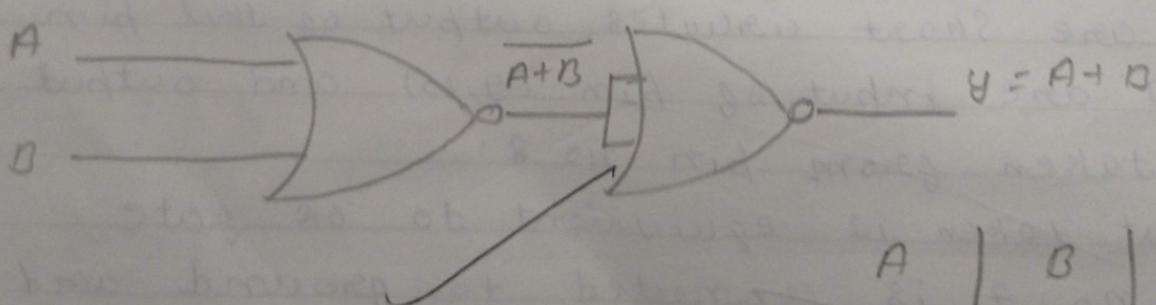
A	Y
0	1
1	0

4. AND gate using NOR gate:-



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

5. OR gate using NOR gate:-



A	B	Y
0	0	0
1	0	1
0	1	1
1	1	1

(3) NOT gate using NAND gate:-

1. IC used is NAND having IC no 7490.
2. Input is given at pin no. 1 and output taken from pin 3, having 1 and 2 pin no. short circuited.
3. The output taken is of NOT gate.
4. Pin no. 7 is grounded whereas 14 pin is connected to power supply.

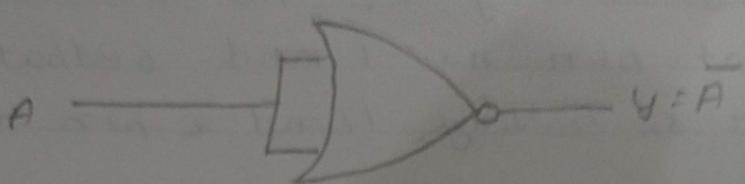
(4) AND gate using NOR gate:-

1. IC used is the type is of NOR gate having IC no. 7402.
2. Input is given at pin no. 1 and 4, where 1, 2 and 4, 5 are short circuited. Output of 1, 4 and 5 is input to pin no. 8, 9 and output is taken at pin no. 10.
3. 7 th pin is grounded whereas 14 th pin is connected to power supply.
4. Output taken is of AND gate.

(5) OR gate using NOR gate:-

1. IC used is of NOR gate using having IC no. 7402.
2. Input is given at pin no. 1, 2 & output from 3 is input of 4, 5.
3. Short circuited 4 output is taken from pin no. 6.

6. NOT gate using NOR gate:



A	Y
1	0
0	1

Result: Successfully studied the NAND & NOR gate as universal gate.

4. 7th pin is grounded whereas 14th pin is connected to power supply.
5. NOT gate using NOR gate:-
1. IC used is of NOR gate having IC no 7402.
 2. Input is given at pin no 2 and 2,3 pin are short circuited and output is taken from pin no 1.
 3. Output formed is of NOT gate.
 4. 7th pin is connected to ground and 14th pin is connected to power supply.

Result:-

Successfully studied the NAND & NOR gate as universal gate.

✓
Jan 18
13/9/18

Aim: Design and realize a given function using K-map and verify its truth table.

Apparatus: digital trainer kit, input supply, IC, bread board, connecting wires.

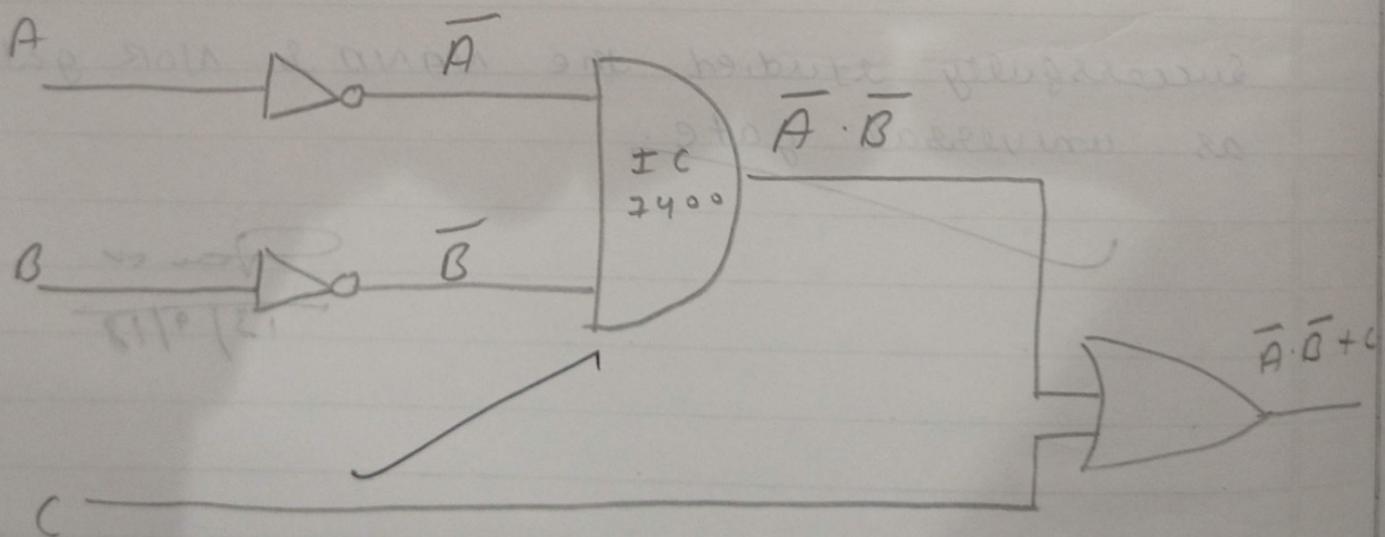
- K-map

$$F(A, B, C) = \Sigma(0, 1, 3, 5, 7)$$

	$\bar{A} \bar{B} \bar{C}$	$\bar{A} \bar{B} C$	$\bar{A} B \bar{C}$	$\bar{A} B C$
\bar{A}	0, 1	2, 3	4, 5	6, 7
A	0	1	0	1
B	0, 1	0, 1	1, 0	1, 0
C	0, 1	1, 0	0, 1	1, 0

$$F = \bar{A} \bar{B} + C$$

Circuit diagram:-



Aim:- Design and realise a given function using K-map and verify its truth table.

Apparatus:- It is a graphical chart, digital trainer, kit, input supply, IC, bread board, connecting wire.

Theory:- It is a graphical chart it contains boxes called cell. Each cell represent one of possible produce combination that can be formed from n-variable.

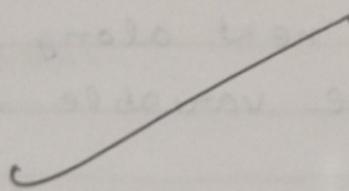
It is important to note that when we move from one cell to next along any row or column the one variable in product from changes.

Procedure:-

1. First using K-map, find the expression.
2. These IC, are connected in circuit i.e NOT, AND and OR.
3. Now make connection on digital kit as per logic circuit.

A	B	C	\bar{A}	\bar{B}	$\bar{A} \cdot \bar{B}$	$\bar{A} \cdot \bar{B} + C$
0	0	0	1	1	1	1
0	0	1	1	1	1	1
0	1	0	1	0	0	0
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	1	0	1	0	1
1	1	0	0	0	0	0
1	1	1	0	0	0	1

Result: The truth table has been verified



Experiment :

Date _____

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4. verify the truth table.

Procedure:-

1. Handle the digital trainer kit carefully.
2. connections should be tight.
3. Make sure that each Ic is properly grounded, and gets proper input supply.

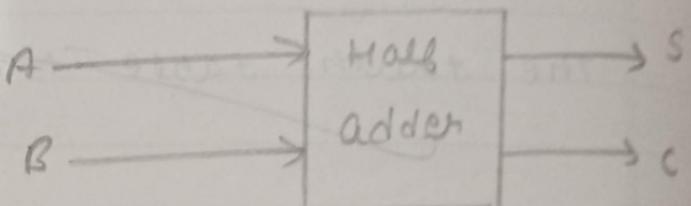
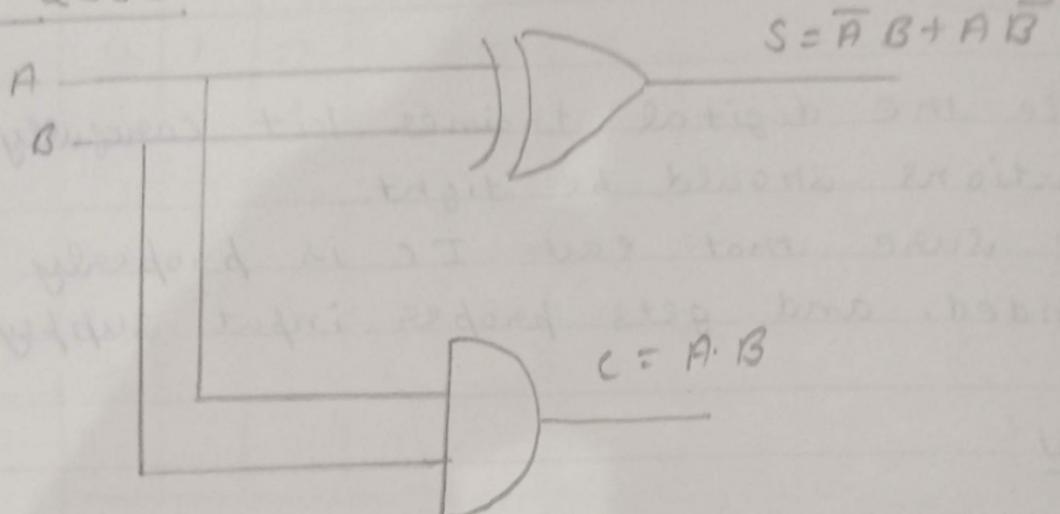
Result:

The truth table has been verified.

Ans-
15/09/18

Aim: To verify half adder and full adder using truth table.

Half adder:-



Truth table :-

A	B	sum	Cout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

A	B	0	1
0	0		
1	1		

A	B	0	1
0	0		
1	1		

$$\text{carry} = AB$$

$$\text{sum} = A\overline{B} + \overline{A}B = A \oplus B$$

Experiment -5

Aim:- To verify half adder and full adder using their truth table.

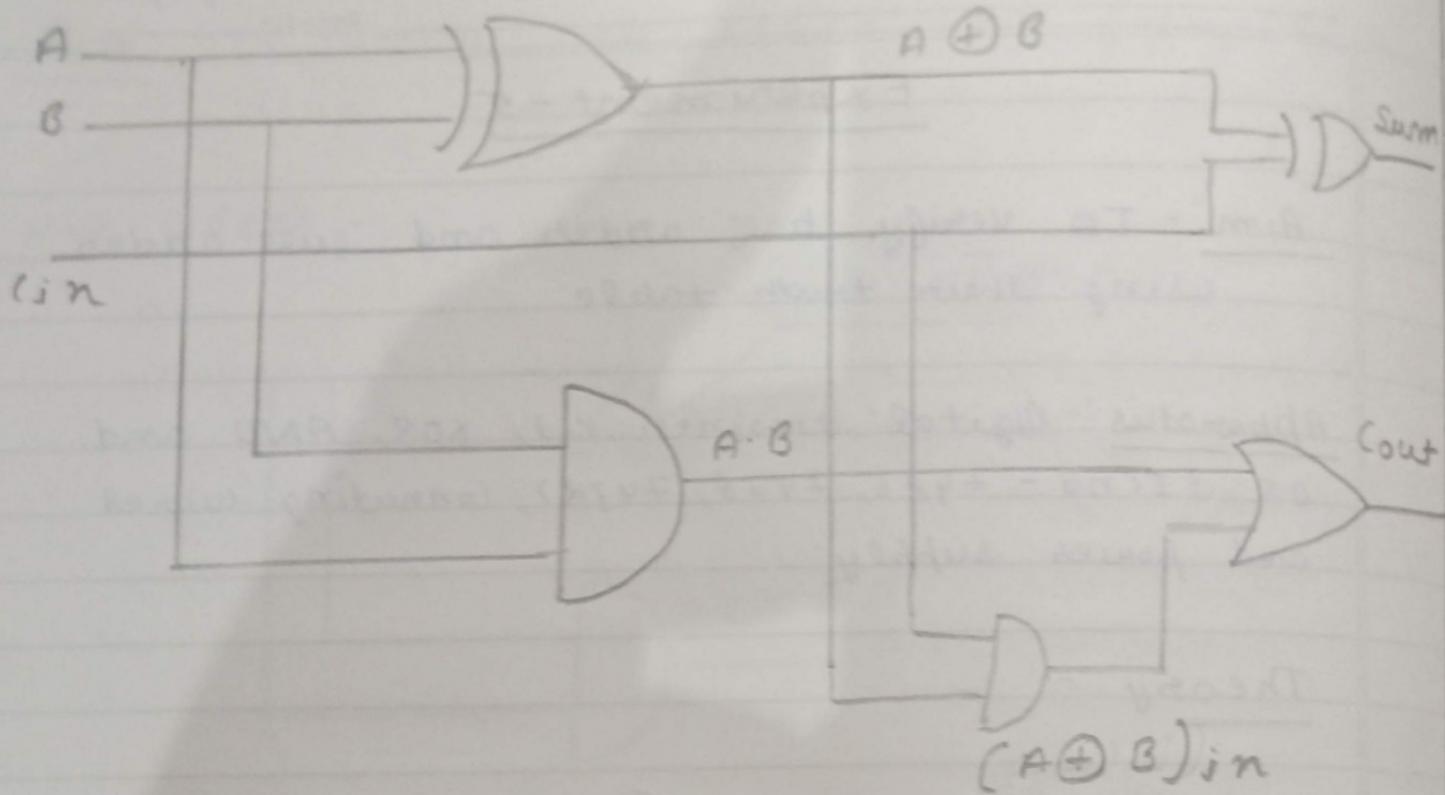
Apparatus:- Digital trainer kit, XOR, AND and OR (IC no - 7486, 7408, 7432), connecting wires and power supply.

Theory :-

Half adder:- It is a combinational logic circuit with 2 inputs and 2 outputs. It is basic building. The output produced one carry and sum. An half adder circuit is designed to add two single bit binary number.

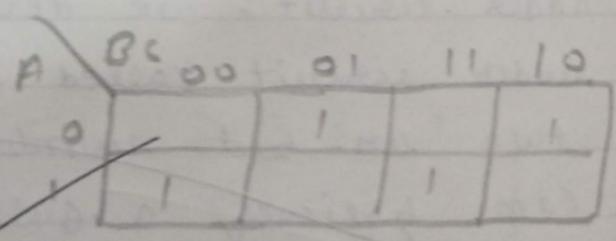
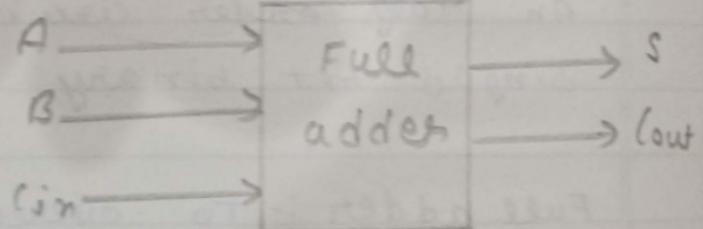
Full adder :- To overcome the drawbacks of half adder circuit, we develop a three single bit adder circuit called full adder, it can add two on bit numbers A and B and carry. ~~(in basically)~~ a full adder is a 3-input and 2 output combinational circuits.

Full adder :-



Truth table :-

A	B	Cin	S	$Cout$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



$$\begin{aligned}
 S &= \bar{A} \bar{B} \bar{C}_{in} + \bar{A} \bar{B} \bar{C}_{in} \\
 &\quad + A \bar{B} \bar{C}_{in} + A B \bar{C}_{in} \\
 &= A \oplus B \oplus C_{in}
 \end{aligned}$$

$$\text{Carry} = C_{in}(A \oplus B) + AB$$

$$= A \oplus B \oplus C_{in}$$

Experiment :

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Procedure :-

- (1) use the IC's of AND, OR and XOR gates and connect the wires along with gate in a specific design (reduced expression).
Collect the result from the LED display and verify it with truth table.
Also, draw the K-map of it.
These steps are repeated for both half adder and full adder.

Precautions :-

Handle the kit carefully.

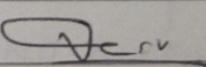
All the connection should be tight.

Kit should be off with making connections.

Circuit diagram should be neat and clean.

Result :-

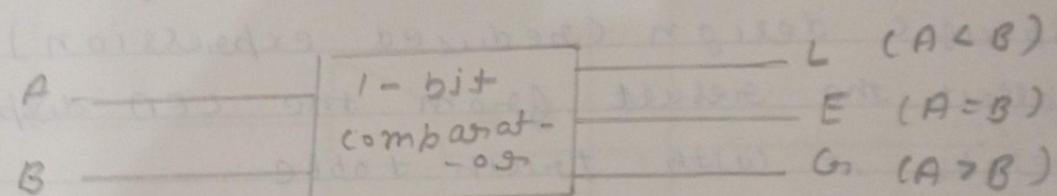
We have studied half adder and full adder circuits by using their truth table.

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4/10/14

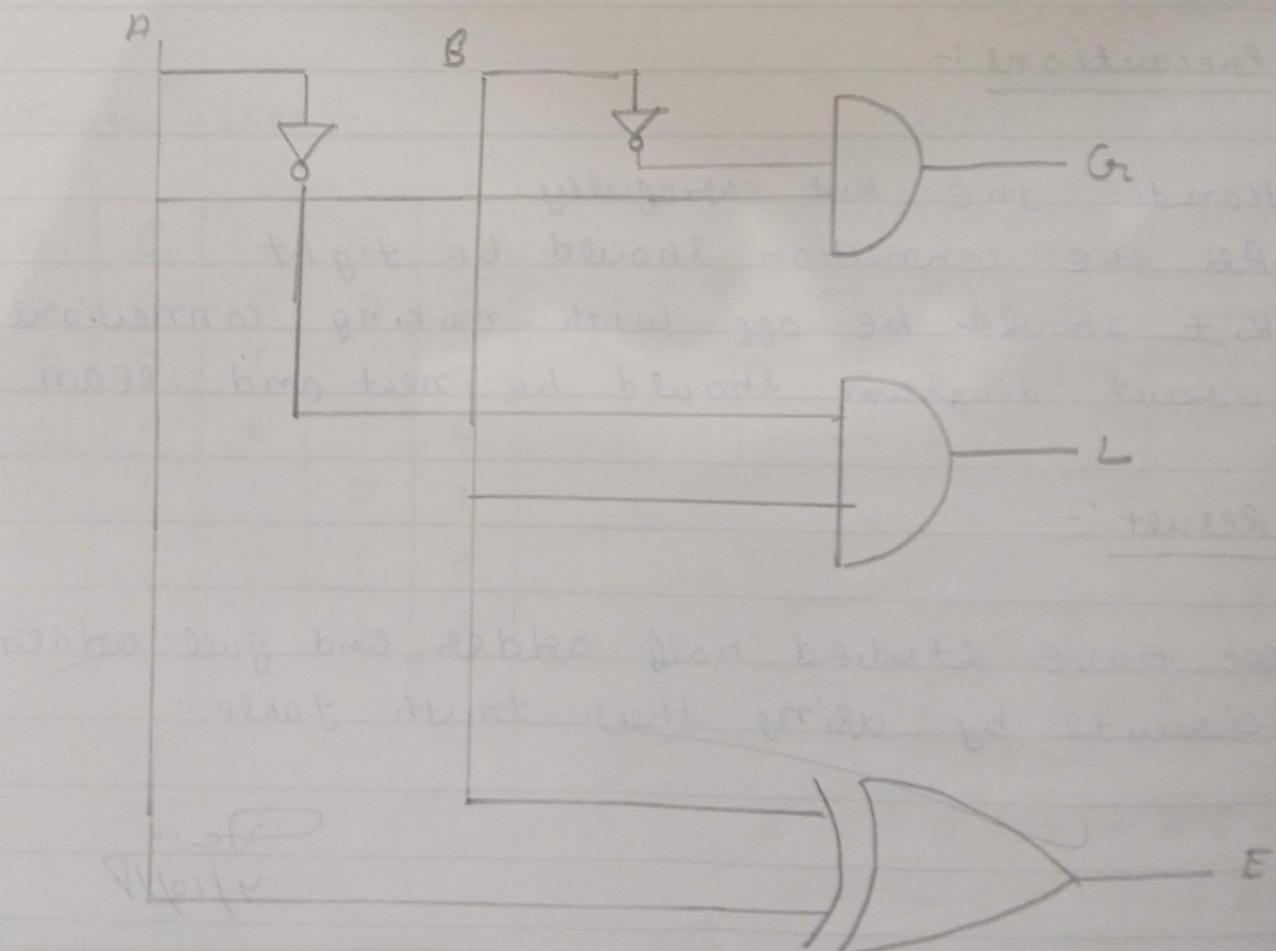
EXPERIMENT - 7

AIM:- To verify the operation of 1-bit comparison using gates.

BLOCK DIAGRAM:-



Circuit diagram:-



EXPERIMENT - 6

AIM :- To verify the operation of 1-bit comparator using gates

Apparatus :- Digital trainer kit, IC's, connecting wires

Theory : A comparator is a logic circuit used to compare the magnitude of two binary numbers. Depending on the design, it may either simply provide an output that is active when the two numbers are equal or additionally provide output that signify which of the number is greater when equality does not hold. The X-NOR gate is a basic comparator because its output is a one only if its two inputs are equal i.e. the output is a 1 if and only if the input bits coincide.

Procedure:

- (1) Using IC (7408), (7404), (7486) [AND, NOT, X-OR] Design the circuit for a 1-bit magnitude.
- (2) Verify the truth table of comparator for different combination of input.

TRUTH TABLE :-

INPUT		OUTPUT		
A	B	L	E	G
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Now we can see that if the inputs A & B are 0 & 0 then the output L is 0. If one of the inputs A or B is 1 then the output L is 1. So the output L is 1 if either A or B is 1. This is called OR gate.

From the given logic ($(A \oplus B) \oplus C$) we can see that if A & B are 0 & C is 1 then the output is 1. If A & B are 1 & C is 0 then the output is 1. So the output is 1 if either A or B is 1 & C is 0. This is called OR gate.

Experiment :

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(3) observe the output.

Precautions:

- (1) Handle the bit carefully.
- (2) All connections should be tight and made carefully.

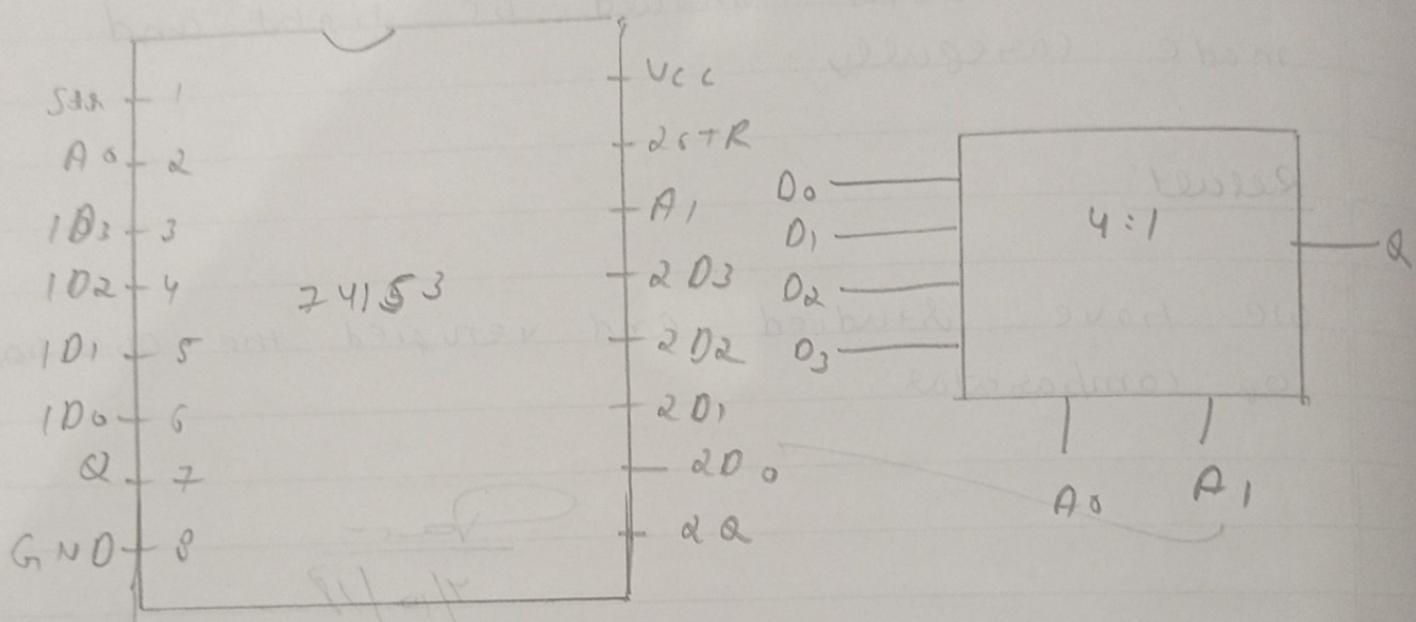
Result:

We have studied and verified the operation of comparator.

Dan
7/10/18

Aim: To study the operation of a multiplexer and demultiplexer & verify the truth table.

Multiplexer



m:1 (Multiplexers)

A ₀	A ₁	Y
0	0	D ₀
0	1	D ₁
1	0	D ₂
1	1	D ₃

m = input line

n = select line

$$m = 2^n$$

EXPERIMENT - 7

AIM:- To study the operation of a multiplexer and demultiplexer and verify the truth table.

APPARATUS:- Digital trainer kit, IC's and connecting wires.

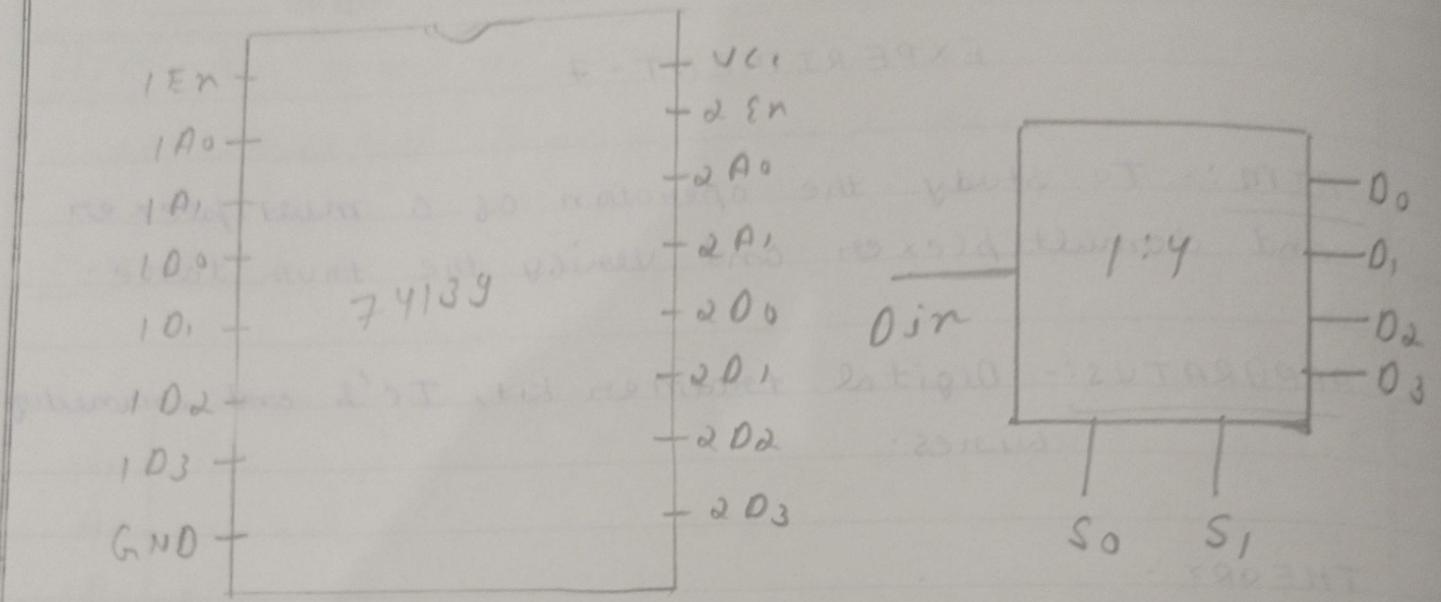
THEORY:-

MUX:- multiplexer is a combination circuit that select binary information from one or many input channels and transmit to single output channels.

Multiplexers are called data selectors because selection of particular input is selected by control lines. A multiplexer of 2^n input channel can be controlled by a no. of select lines and input lines is selected according to a different combination of select lines. These are (m) input lines and (n) is the no. of select lines.

STROBE (STR) / ENABLE:-

This pin is used for proper control operation of MUX, it is an active low pin used to expand to a more MUX with the large number of



E _n	D _{in}	S ₀	S ₁	O ₀	O ₁	O ₂	O ₃
0	1	0	0	0	1	0	1
0	0	0	1	0	1	0	1
0	1	0	0	1	0	1	0
0	0	1	0	0	1	0	0
1	1	1	0	1	0	1	0
1	0	0	1	0	1	0	0
1	1	0	1	0	0	1	0
1	0	1	0	0	0	0	1

~~74139 (Herrz) 3808~~

Die entzerrte Ladung wird nun zu einer 21 ms langen

25 Rechtecke mit einer Breite von 1 ms und einer

input D_0, D_1, D_2, D_3 are input lines. A_0 & A_1 are select lines and Q is the output.

DE MUX :-

A demultiplexer is a combination circuit which means one input to many outputs. It is a logic circuit which gives information to a single input line and the same over one of the possible 2^m output lines. The selection lines of specific output is controlled by bit combination of selection lines. 'n' is the no. of output lines and 'm' is the select lines. D_0, D_1, D_2, D_3 are the output lines. A_0 and A_1 are select lines.

PROCEDURE :-

(a) For Multiplexer :-

using the IC - 74153 make connections as shown in the fig (a) for different combination of inputs, find the output & verify the truth table.

(b) For Demultiplexer :- using the IC - 74139

make connections as shown in fig (b) for different combination of inputs, find the output and verify the truth table.

Experiment :

Date _____

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PRECAUTIONS:- circuit diagram should be
neat & clean Handle the
kit carefully.

All the connections should be tight.

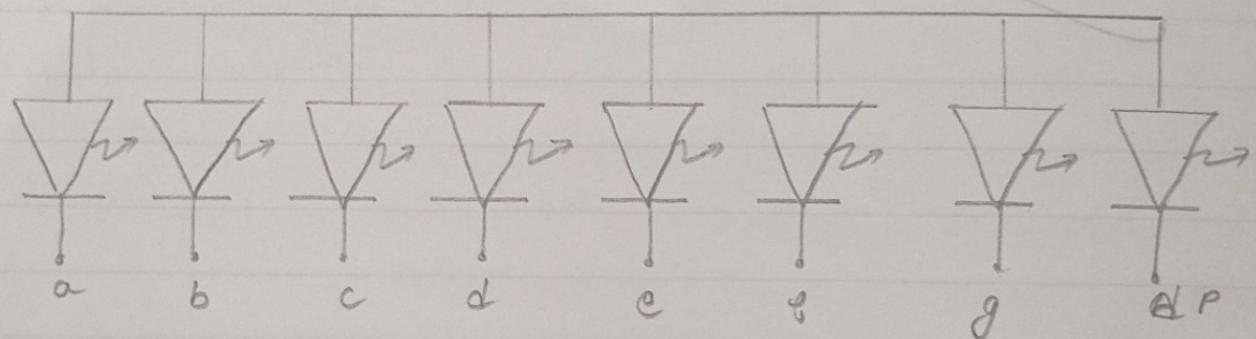
RESULT:- we have studied the multiplexers,
de-multiplexers and verified them using
truth table.

Done
21/10/18

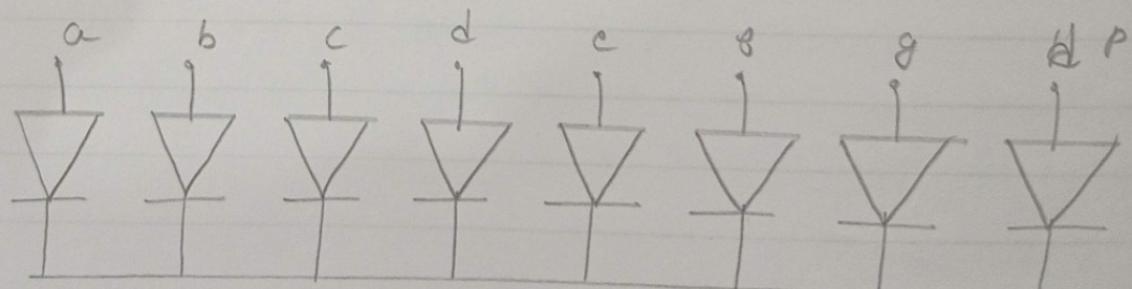
AIM: To verify the operation of seven segment decoder.

Requirement: IC 7447, 7-segment display

Common anode:



Common cathode:



Experiment - 8

AIM:- To verify the operation of seven segment decoder.

Requirement:- IC 7447, 7-segment display.

Mode:- TTL

Theory :-

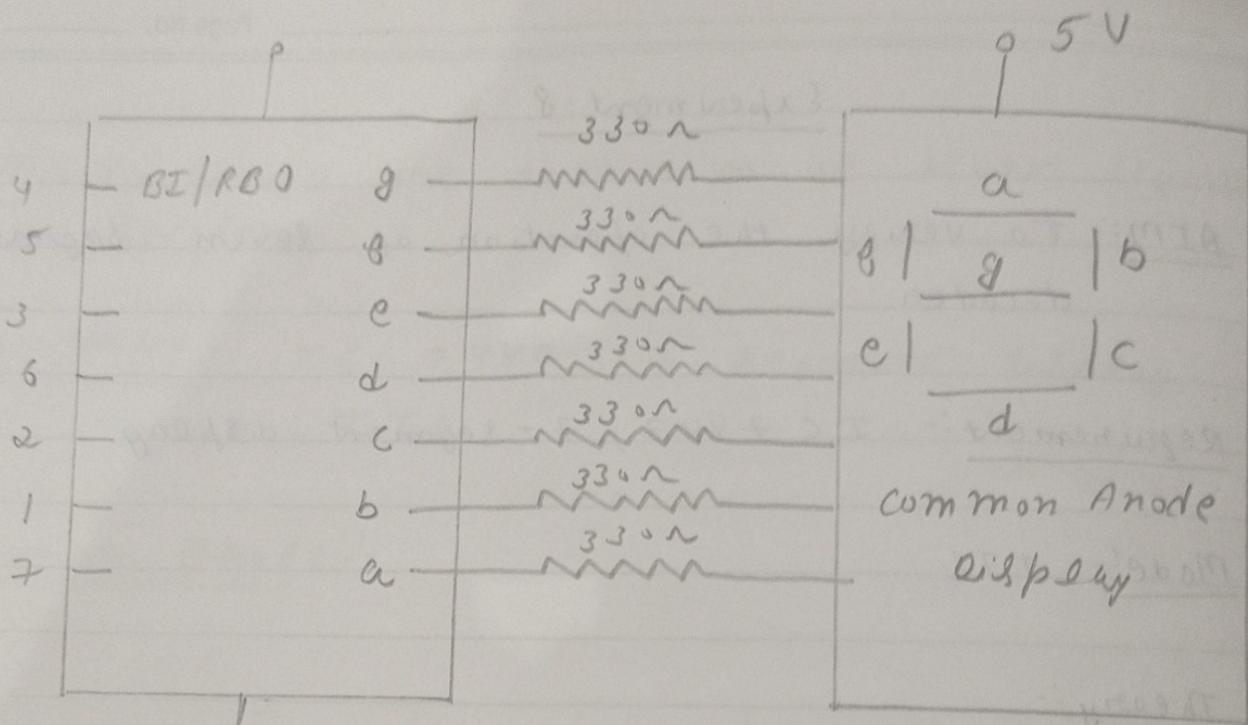
A seven segment decoder / driver is an IC decoder that can be used to drive a seven segment indicator. There are two types of decoder / drivers, corresponding to common anode and common cathode indicator. Each decoder driver has 4 BCD input and 7 output pins segment.

BI / RBO :-

When this pin is at low logic level all segment outputs are off regardless of the level of any other input. It must be at high logic or open to get function for 0000 to 1111.

BI / RBI :-

The ripple blanking input must be open or high if blanking of a decimal zero is not observed. If it is low it will blank decimal zero.



LT :- when blanking inputs / nibble blanking output BT/RBO is open or hold high and a low is applied to this output all segment output are off.

Procedure:-

- (1) connect all connection as like circuit diagram.
- (2) observe decimal output on common anode display given on the experiment board. outputs of individual pins can be seen logic probe or an LED display of digital lab STZ611 or an multimeter.
- (3) connect different combinations as inputs as shown in truth table and prove truth table.
- (4) Repeat steps 5, 6 and observe the result.
- (5) connection logic 0 to LT input, logic 1 to RBI and BT/RBO input.
- (6) Repeat steps and observe the result.
- (7) connect logic 0 to RBI input and BCD input logic 1 to LT & BI/RBO input and observe the result.

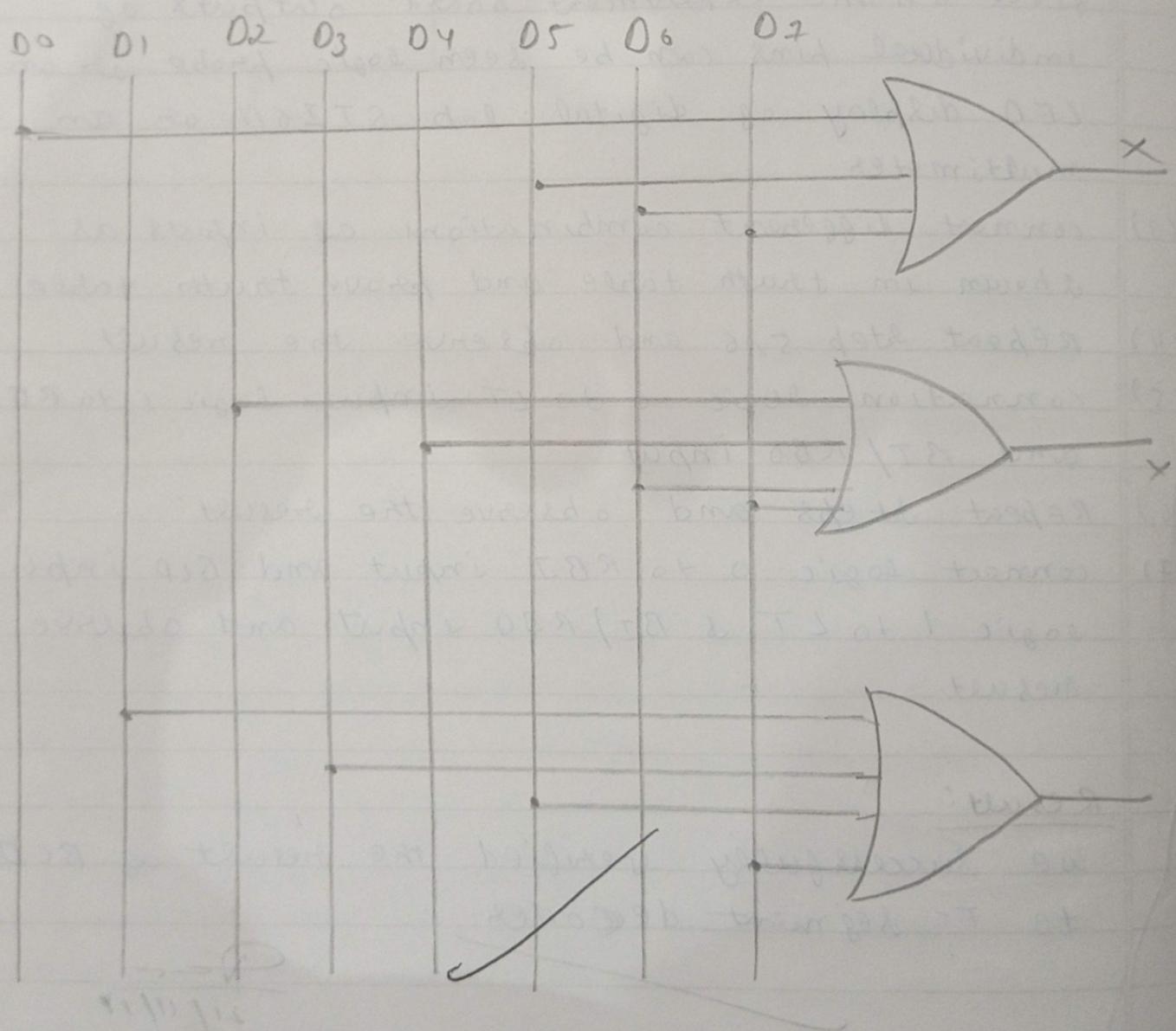
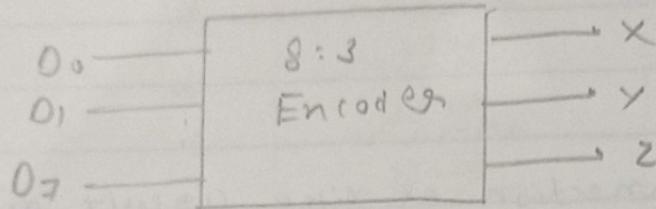
Result:-

We successfully verified the result of BCD to 7-segment decoder.

Ques
21/11/17

Aim: To study and verify the operation of 8:3 encoder and 3:8 decoder.

ENCODER:



Experiment - 9

AIM:- To study and verify the operation of 8:3 encoder and 3:8 decoder.

H/W Requirement:- D1309, DC +5V power supply connecting wires, trainer, etc.

Theory :-

Encoder :- An encoder is a device circuit that transduce software program algorithm that converts information from one format as code to another for the purpose of standardisation, speed or compression.

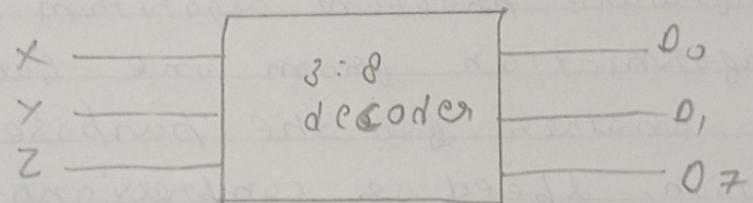
Decoder :- A binary decoder is a combinational logic circuit, that converts a binary integer value to an allocated pattern of output bits. They are used in a wide variety of application including data multiplexing, seven displays and memory address decoding.

Procedure :-

- (1) connect power supply as per requirement
- (2) connect all connection as like circuit diagram.

Truth Table:

Decoder:



Truth table:

Experiment :

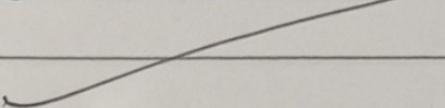
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(3) connect different combination of inputs of shown in truth table and prove that truth table one by one for both encoder and decoder.

Result :-

we successfully verified the operation of encoder and decoder.


Date
21/10/18