PANIPAT INSTITUTE OF ENGINEERING & TECHNOLOGY

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MPI

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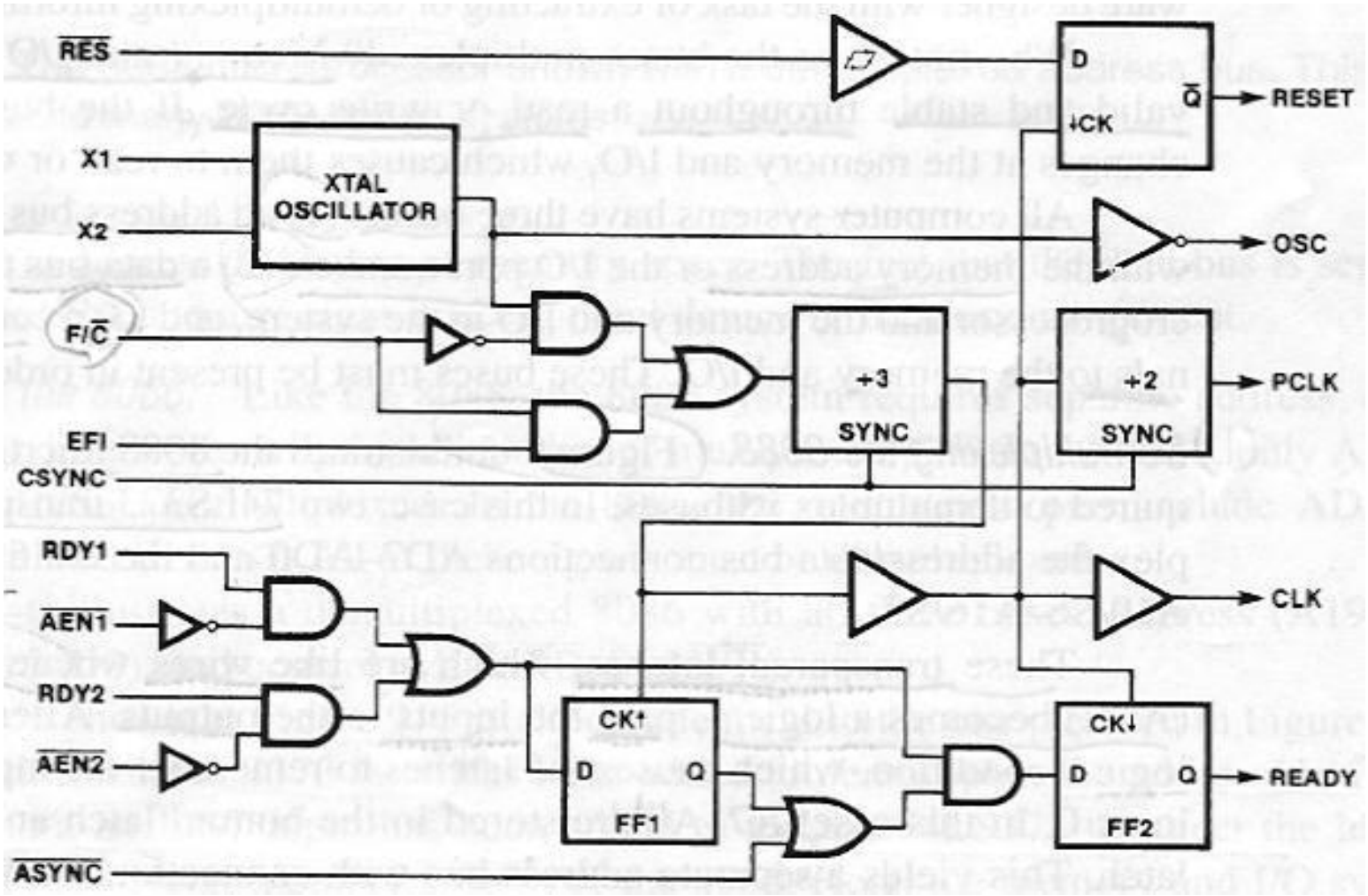
Clock Generator 8284

- The 8284*A* is an integrated circuit designed specifically for use with the 8086/8088 micro- processors.
- Without the clock generator, many additional circuits are required to generate the clock (CLK) in an 8086/8088-based system.
- The 8284 is an 18 pin integrated circuit , designed specifically for use with 8086 microprocessor.

This circuit provides the following basic functions or signals

- **clock generation,**
- **RESET synchronization,**
- **READY synchronization.**

internal block diagram of 8284A clock generator



Pin Diagram

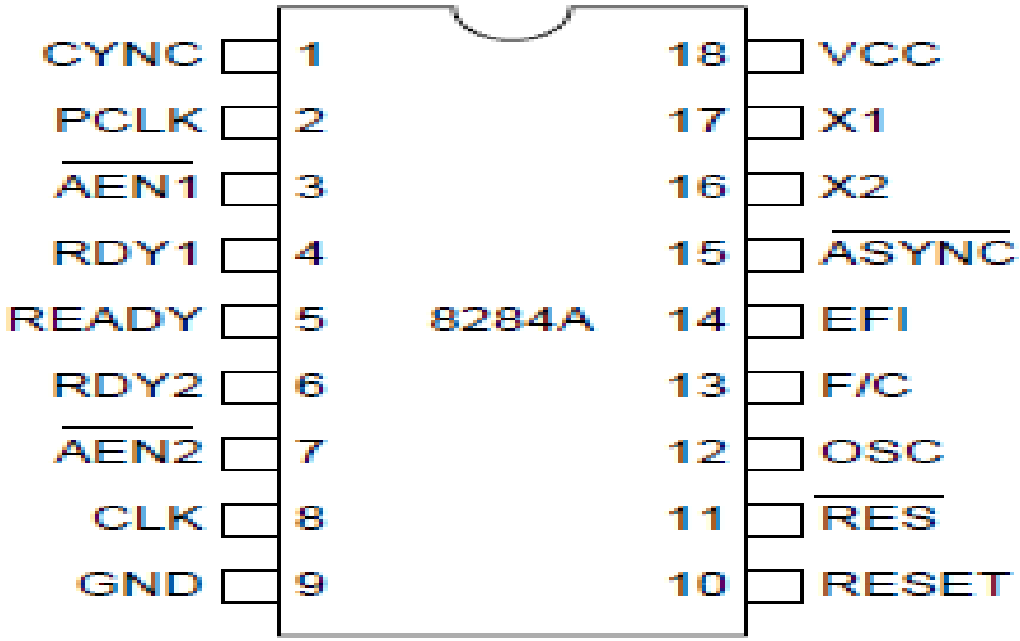


Figure 3.1 – 8284A pin diagram.

- **CSYNC:** The clock synchronization pin is used whenever the EFI input provides synchronization in systems with multiple processors. If the internal crystal oscillator is used, this pin must be ignored.

- **PCLK:** The peripheral clock signal is one-sixth the crystal or EFI input frequency, and has a 50-percent duty cycle. The PCKL output provides a clock signal; to the peripheral equipment in the system

AEN 1& AEN2: The address enable pins are provided to qualify the bus ready signal, RDY1 & RDY2 . These two pins are used to cause wait state, along with RDY1 & RDY2 inputs.

- Wait state are generated by the READY pin of the 8086 microprocessor which is controlled by these two pins.

- **RDY1 & RDY2:** The bus ready inputs are provided, in conjuction with the AEN1 & AEN2 pins, to cause wait state in 8086 based system.

- **RESET:** The RESET output connects to the 8086/8088 RESET input pin.

- **RES (Reset input):** Active low input. Often connects to an RC network that provides power -on- resetting.

- **OSC (Oscillator):** TTL level signal output. Provides an EFI input to other 8284A clock generators in some multiple processor systems

- **F/C(Frequency/Crystal select):** It chooses the clocking source for the 8284A.
- F/C=1(high),an external clock is provided to the EFI input pin.
- F/C=0(low),an external crystal oscillator connected to X1 and X2 provides the clock.
- **EFI(External Frequency Input):** It is used when F/C pin is set to high.
- It Supplies the timing whenever the F/C is high

ASYNC(Ready synchronization)

- The ready synchronization selection input selects either one or two stages of synchronization for the RDY1 and RDY2 inputs.

X1 nad X2(Crystal inputs)

- An external crystal oscillator is connected to these inputs.
- It is used as the timing source for the clock generator and all its functions

Operation of Clock Section

- F/C' = 0 : internal crystal oscillator
  - crystal is attached X1, X2, oscillator generate square-wave signal at the same frequency as crystal
  - square-wave signal : fed to AND gate, inverter(OSC)
  - OSC output : sometimes used as EFI to other 8284A
- AND gate : select oscillator or EFI
  - F/C'=0 : oscillator output → divide-by-3 counter
  - F/C'=1 : EFI → divide-by-3 counter
- output of divide-by-3 counter
  - timing for ready synchronization
  - signal for another divide-by-2 counter : PCLK
  - CLK signal : buffered before CLK output pin

Operation of the Reset Section

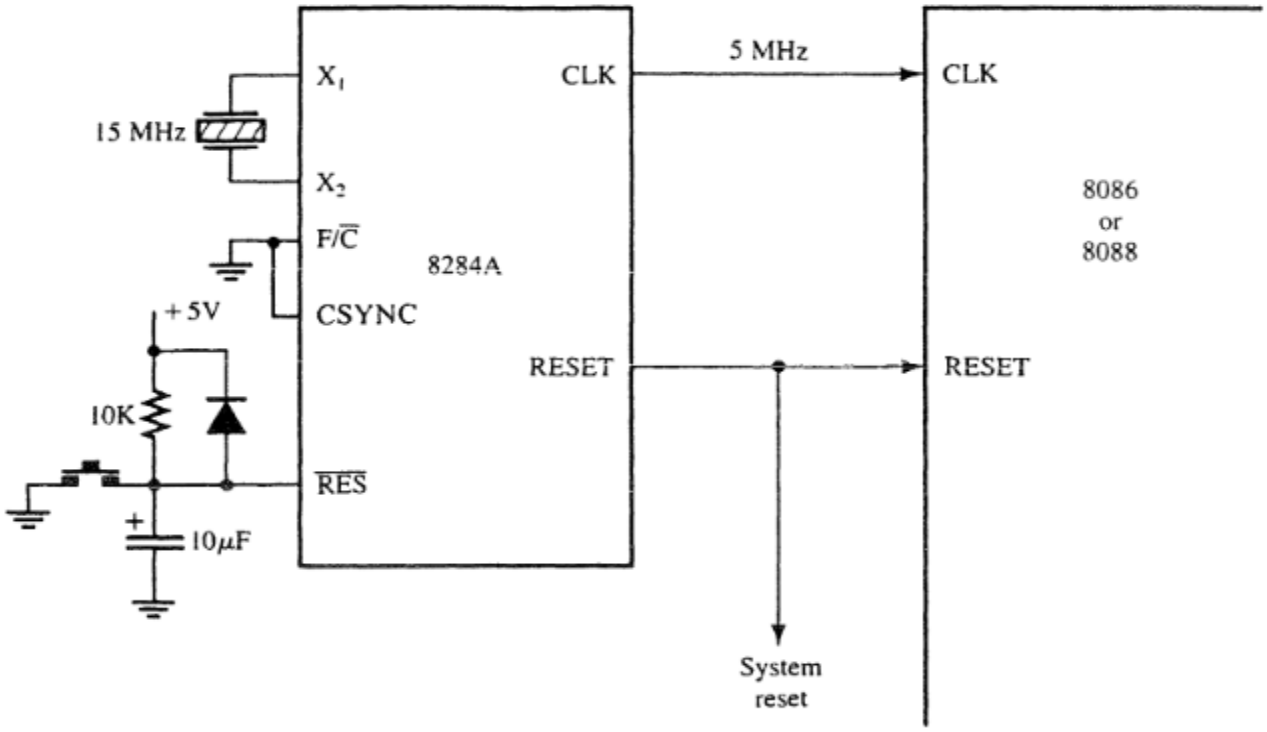
The ckt on next slide allows the processor to be rest in two ways.

1.The most obvious is to depress the switch. The RESET output will be held high for an integral number of clock pulses until the switch is released .

The CPU state following RESET

CPU	Content
Flags	Clear
Instruction Pointer	0000
CS register	FFFF
DS register	0000
SS register	0000
ES register	0000
Queue	empty

Reset signal generation



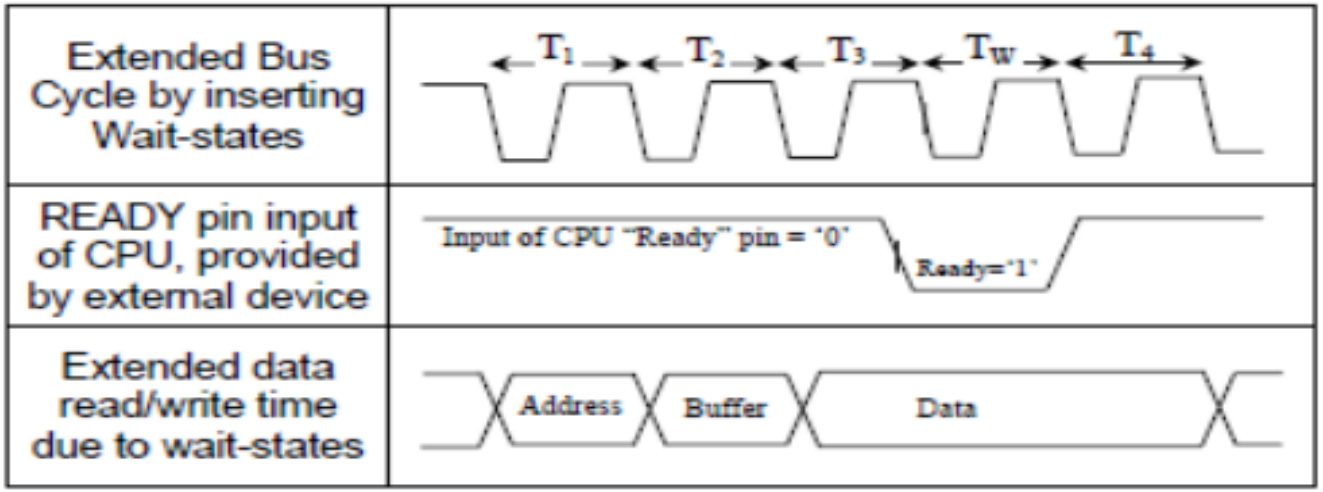
2. The other method is POWER ON RESET function . When power is first applied to system, the capacitor will charge toward 5v. RES input will be held low to generate high signal on RESET output through Schmitt trigger .So when voltage across capacitor becomes greater then 1.05 volt Reset signal becomes low.

Output of Schmitt triger
When Vin<1.05V then output is low
When Vin>1.05V then output is high

When power is removed capacitor discharges through diode.

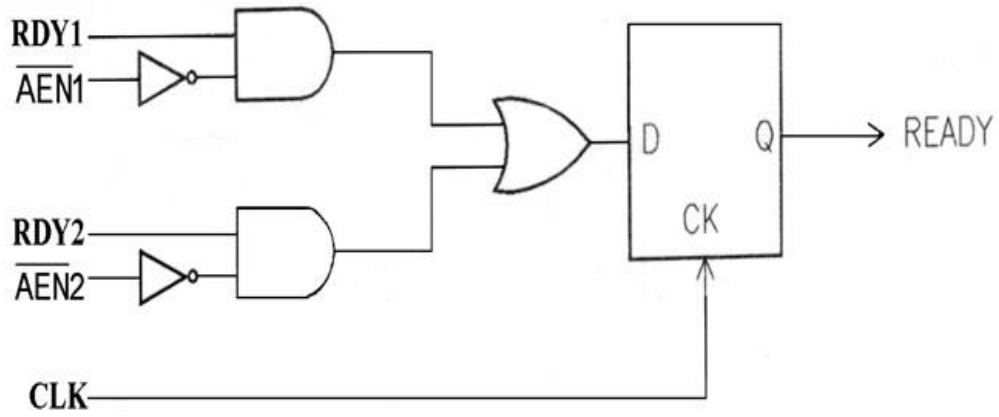
Ready Signal Generation

RDY1 and AEN1: provide a Ready signal to the mPro, which will insert a WAIT state to the CPU read/write cycle.
RDY2 and AEN2: For multiprocessor systems.
Slow devices (memory or I/O) must request extra time. The microprocessor inserts extra *wait states* between states T3 and T4. The alternatives are to slow down the system clock, or use faster devices



Ready Logic

The Ready Logic generates the Ready signal for the 8086/8088. If the Ready signal is made low by this circuit during T2 state of a machine cycle, the microprocessor introduces a wait state between T3 and T4 states of the machine cycle.



- **READY:** READY is an output pin that connects to the 8086/8088 READY input.
- This signal is synchronized with the RDY1 and RDY2 Inputs.
- **CLK:** Provides CLK input signal to the 8086/8088 microprocessors and other components in the system.
- **GND:** Connects to ground.
- **Vcc :** Connects to +5.0V