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BT-3/D-18 **33083**

DIGITAL ELECTRONICS

Paper : CSE-207(N)

Time : Three Hours] [Maximum Marks : 75

Note : Attempt *five* questions in all, selecting at least *one* question from each unit. All questions carry equal marks.

1. (a) State De-Morgan's Theorem. 3

(b) Discuss BCD adder design procedure. 4

(c) Draw pin configuration of 555 timer IC. 4

(d) Explain memory decoding. 4

UNIT–I

2. Discuss Quine Mc-Clusky (QMC) method of Minimization. Simplify the following expression using QMC method also verify the results by K map method

$F = \Sigma_{A,B,C,D}\, m\,(1, 4, 5, 6, 12, 13, 14) + \Sigma d(0, 8, 9, 11)$. 15

3. (a) Write the small note on the following :

(i) CMOS characteristics.

(ii) Principle of duality. 10

(b) Realize the following logic equation using only NAND gates :

$AB + CD = AB \cdot CD$. 5

UNIT–II

4. (a) Differentiate between serial adder and parallel adder with the help of full adder block diagram. 10

(b) Explain magnitude comparator. 5

5. Design a BCD-to-Gray code convertor using

(a) 8 : 1 multiplexer.

(b) Dual 4 : 1 multiplexers and some gates.

(c) NAND gates only. 15

UNIT–III

6. (a) Explain the operation of twisted ring counter and give its state diagram. 8

(b) Explain master slave flip-flop with the help of diagram. 7

7. Write short notes on the following :

(a) Shift register counter.

(b) Modulo-n counter.

(c) Sequence generator. 15

UNIT–IV

8. (a) What is dynamic RAM? Explain its cell structure. 7

(b) Explain the following in brief :

(i) EPROM.

(ii) EAPROM. 8

9. Write short notes on the following :

   (a) Memory expansion.

   (b) Implementation of PLA using ROM.

   (c) FPGA. 15
