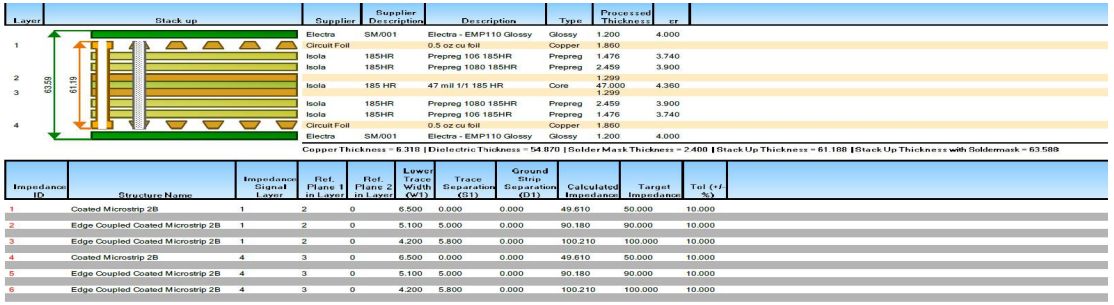
AIT1L

Major Revision History

PCB Rev.	Sch Rev.	Description	Date
2.0	1.1	- U2 --> DNP, U3 --> DNP - 47uF cap and TVS Diode on VUSB_CONN - Snubber added	31-Aug-2021
2.0	1.2	- DC-DC Regulator part changed	02-Sep-2021
2.0	1.3	- Internal review comments implemented.	03-Sep-2021
2.0	1.4	- DC-DC regulator replaced with LDO	07-Sep-2021
2.0	1.5	- Term "SPE" is replaced with "T1L"	20-Sep-2021
2.0	1.6	- Feedbacks from ADI team implemented.	30-Sep-2021
2.0	2.0	- Schematics baselined. - Gerber released for fabrication	08-Oct-2021
2.0	2.1	- C16 changed to 10 pF	25-Apr-2022

Layer Stack-up



Layer	Stack up	Supplier	Supplier Description	Description	Type	Processed Thickness	er
1		Electra	SM/001	Electra - EMP110 Glossy	Glossy	1.200	4.000
		Circuit Foil		0.5 oz cu foil	Copper	1.860	
		Isola	185HR	Prepreg 106 185HR	Prepreg	1.476	3.740
2		Isola	185HR	Prepreg 1080 185HR	Prepreg	2.459	3.900
						1.299	
3		Isola	185 HR	47 mil 1/1 185 HR	Core	47.000	4.360
						1.299	
		Isola	185HR	Prepreg 1080 185HR	Prepreg	2.459	3.900
		Isola	185HR	Prepreg 106 185HR	Prepreg	1.476	3.740
4		Circuit Foil		0.5 oz cu foil	Copper	1.860	
		Electra	SM/001	Electra - EMP110 Glossy	Glossy	1.200	4.000

Copper Thickness = 6.318 | Dielectric Thickness = 54.870 | Solder Mask Thickness = 2.400 | Stack Up Thickness = 61.188 | Stack Up Thickness with Soldermask = 63.588

Impedance ID	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width (W1)	Trace Separation (S1)	Ground Strip Separation (D1)	Calculated Impedance	Target Impedance	Tol (+/- %)
1	Coated Microstrip 2B	1	2	0	6.500	0.000	0.000	49.610	50.000	10.000
2	Edge Coupled Coated Microstrip 2B	1	2	0	5.100	5.000	0.000	90.180	90.000	10.000
3	Edge Coupled Coated Microstrip 2B	1	2	0	4.200	5.800	0.000	100.210	100.000	10.000
4	Coated Microstrip 2B	4	3	0	6.500	0.000	0.000	49.610	50.000	10.000
5	Edge Coupled Coated Microstrip 2B	4	3	0	5.100	5.000	0.000	90.180	90.000	10.000
6	Edge Coupled Coated Microstrip 2B	4	3	0	4.200	5.800	0.000	100.210	100.000	10.000

Page Description

Page1: Cover Page
Page2: Block Diagram
Page3: Power Supply & MCU Section
Page4: 10Base-T1L Interface
Page5: RJ45 Ethernet Interface
Page6: Revision History

PCB MECHANICAL DETAILS :

1. PCB Size: 50mm x 50mm
2. PCB Material: FR4
3. Number of Layers: 4
4. Impedance Control: Yes

NOTES, UNLESS OTHERWISE SPECIFIED :

1. Resistance values are in Ohms.
2. Capacitance values are in micro-Faradays.
3. Parts not installed are indicated with "DNP".
4. Signal net names with "#" suffix are active low signals

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Block Diagram

10BASE-T1L Media Converter Dongle Hardware Architecture

Rev-1.2

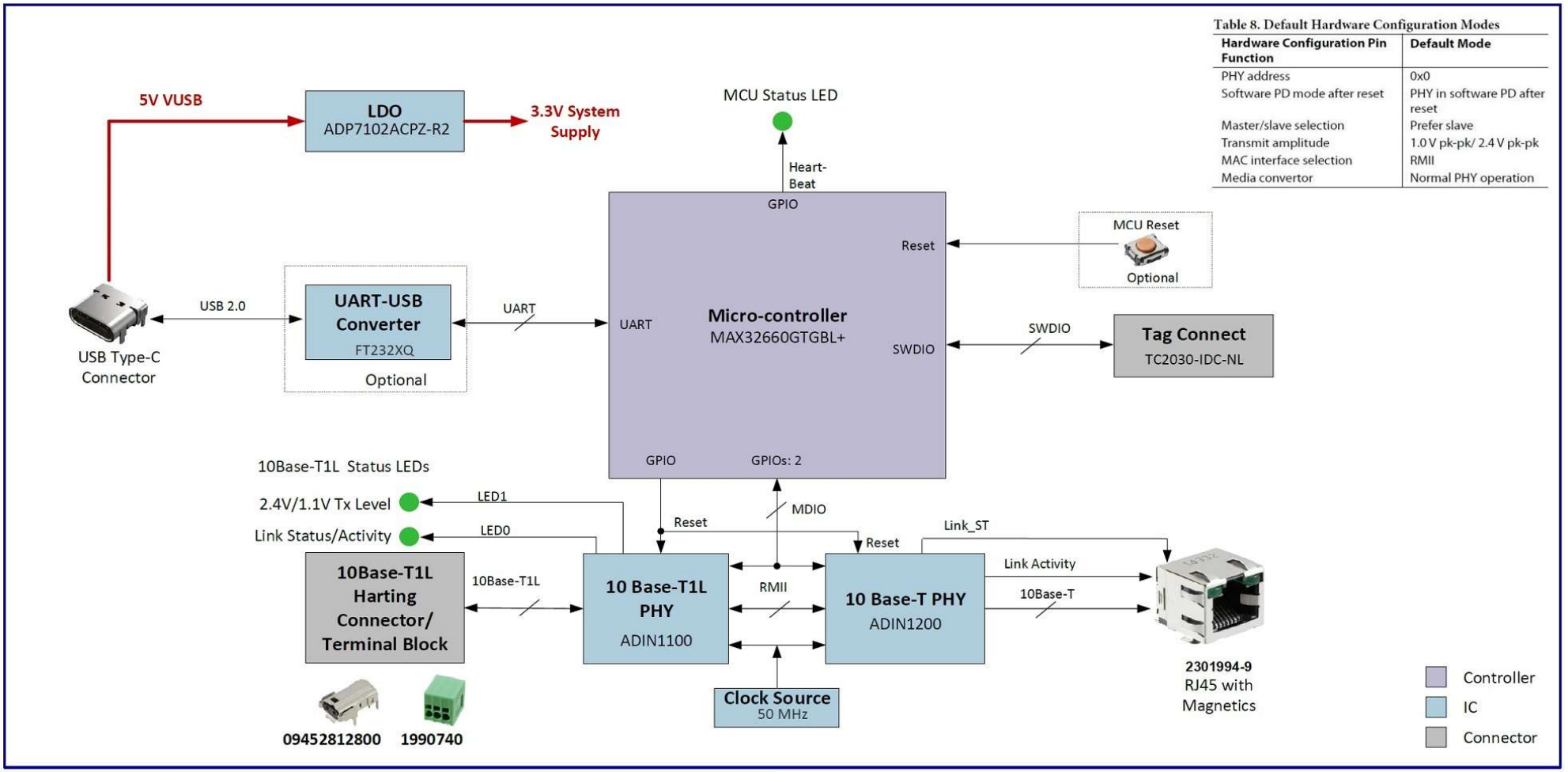

Table 8. Default Hardware Configuration Modes

Hardware Configuration Pin Function	Default Mode
PHY address	0x0
Software PD mode after reset	PHY in software PD after reset
Master/slave selection	Prefer slave
Transmit amplitude	1.0 V pk-pk/ 2.4 V pk-pk
MAC interface selection	RMII
Media convertor	Normal PHY operation

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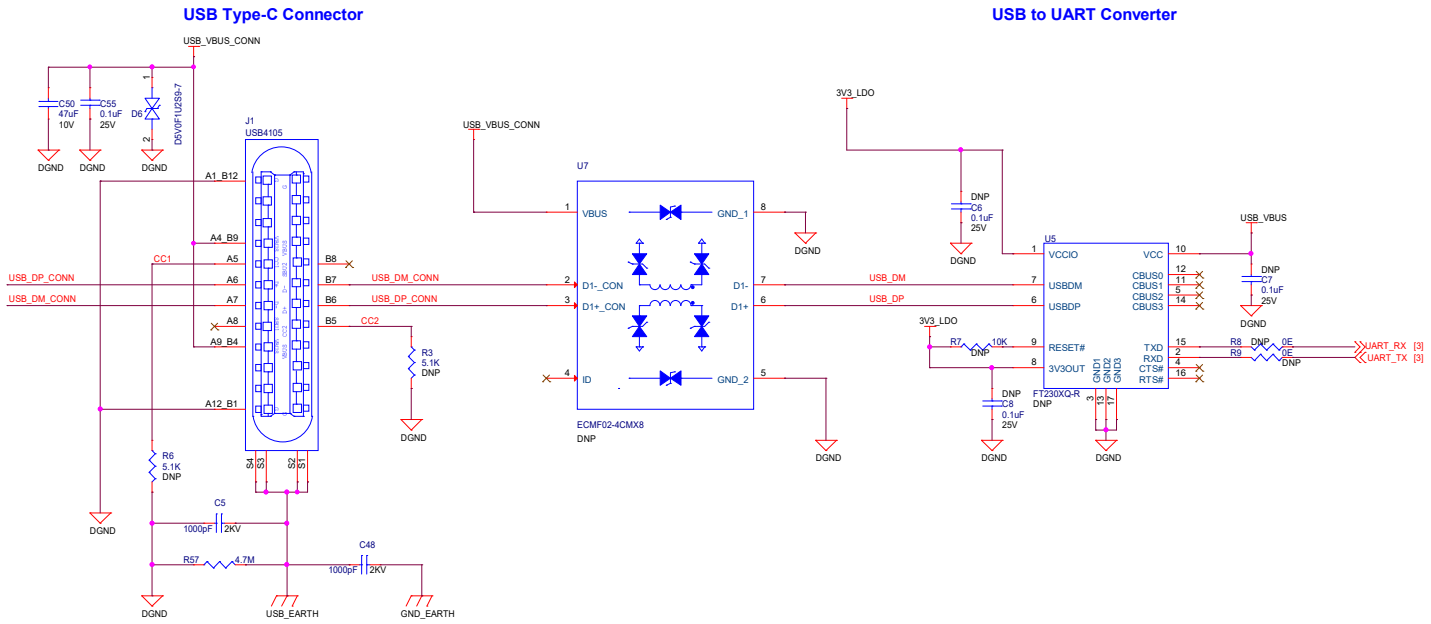
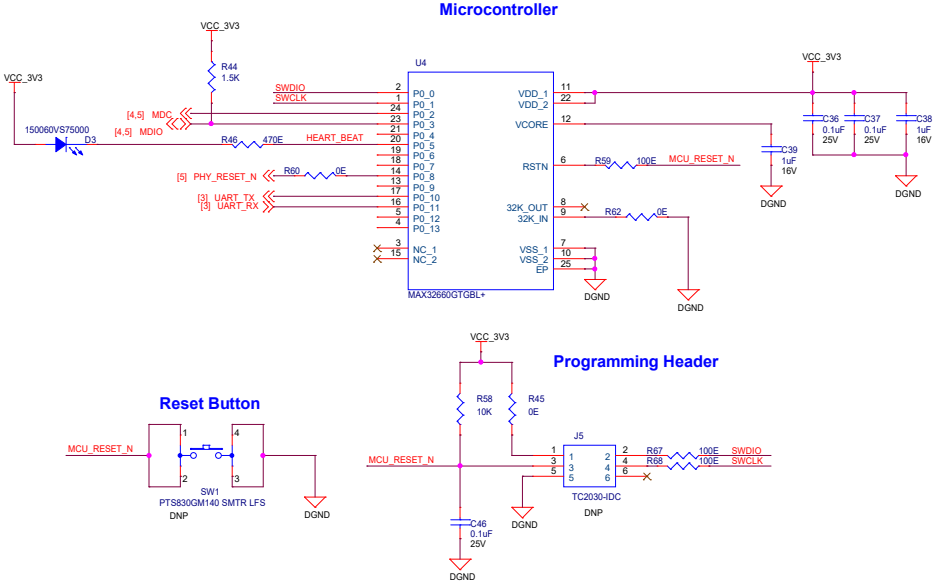
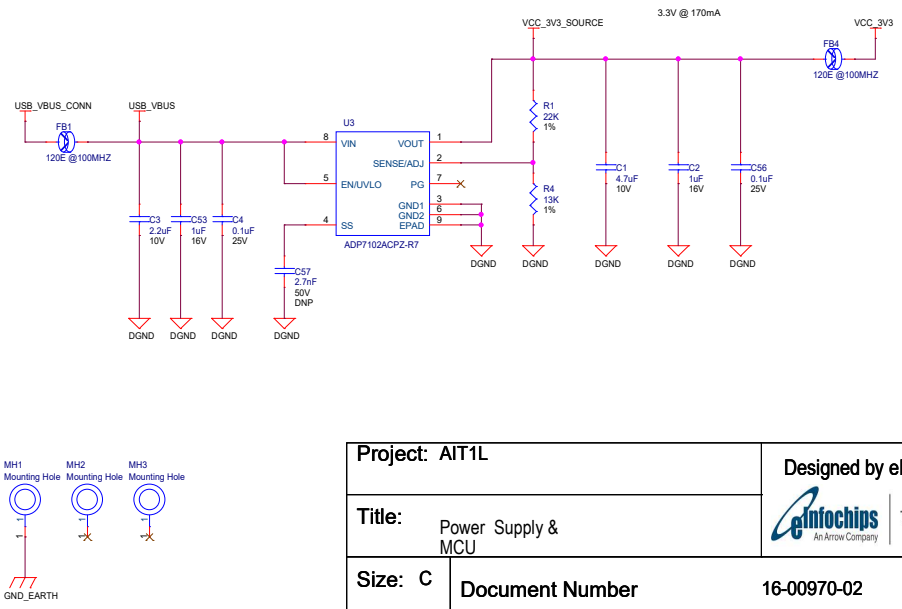
Power Supply & MCU Section







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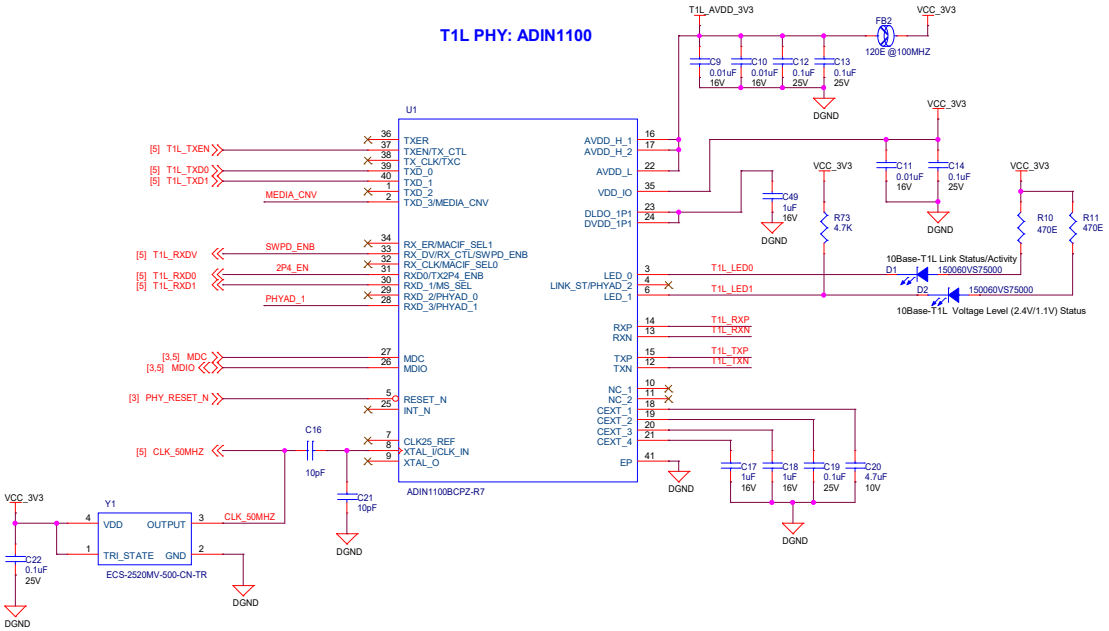
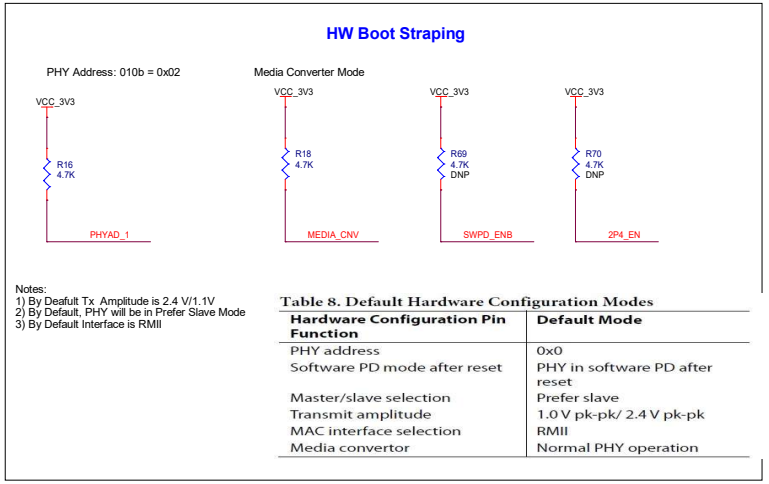
10Base-T1L Ethernet





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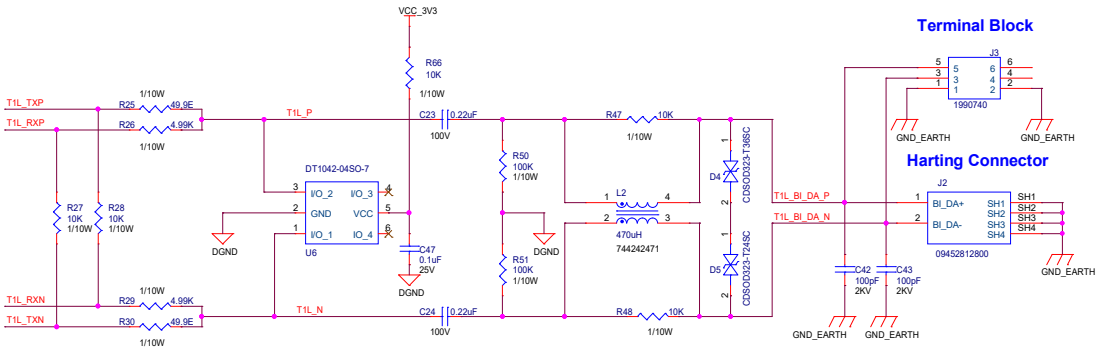

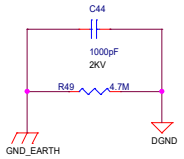

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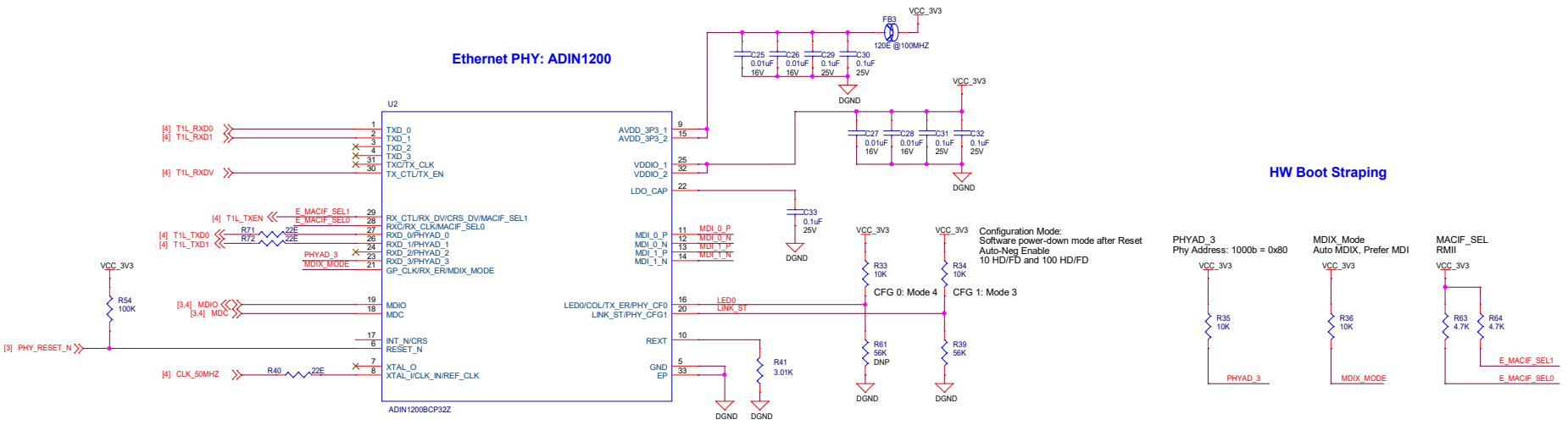
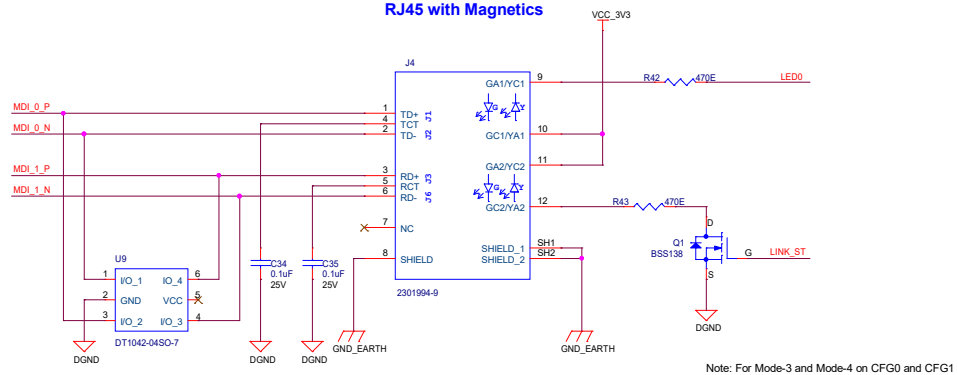
Ethernet



HW Boot Straping



Note: For Mode-3 and Mode-4 on CFG0 and CFG1 LEDs can be directly connected.

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Revision History

PCB Rev.	Sch. Rev.	Description	Date	Author
1.0	0.1	Initial Draft version created	26-May-2021	eInfochips
	0.2	MCU XTAL is removed; FBs are added on AVDD supplies	31-May-2021	eInfochips
	0.3	Series resistors on RMII removed. - Single Reset for ADIN1100 and ADIN1200. - ADIN1100 and ADIN1200 Link_Status signals are removed from MCU	07-Jun-2021	eInfochips
	0.4	- 100 ohm series resistors added on SWD lines - Separate Earth GND for USB	15-Jun-2021	eInfochips
	0.5	- Tag connect part changed to TC2030-IDC	18-Jun-2021	eInfochips
	0.6	- VCCIO of U3 is connected with 3V3_LDO. VCC_3V3 provision is removed.	22-Jun-2021	eInfochips
	0.7	Schematic update after customer review: - R17 deleted on SWPD_EN line; Q2 deleted on ADIN1200 LED0 line; - Two TVS diode in series in between 10Base-T1L signals.	24-Jun-2021	eInfochips
	0.8	Provision added on SWPD_EN and 2P4_ENB pins; R50 and R51 moved in between C23 and C24 and CMC	28-Jun-2021	eInfochips
	1.0	Schematics baslined; Gerber released for fabrication;	03-Jul-2021	eInfochips
2.0	1.1	Initial Beta draft: - U3 (FT232XQ) --> DNP; U2 (ECMF02-4CMX8) --> DNP - 47uF and TVS diode D5V0F1U2S9-7 cap added on VUSB_CONN - 0E series resistor added on T1L_TXD0 and T1L_TXD1 - RJ45 part changed to 2301994-9 - Snubber added on SW node of Buck-Regulator	31-Aug-2021	eInfochips
	1.2	- Buck Regulator is changed to LTC3103IMSE#PBF	02-Sep-2021	eInfochips
	1.3	Internal review comments implemented: - Discrete components of U3 are DNP - Series resistors on T1L_TXD0 and T1L_TXD1 are moved to source side. - 0.1uF cap added on VUSB_CONN near connector. - 10uF cap added on VIN of DC-DC regulator - Snubber components are populated. 2 Mounting hole added	03-Sep-2021	eInfochips
	1.4	- DC-DC regulator is changed with LDO ADP7102ACPZ-R7	07-Sep-2021	eInfochips
	1.5	- Term "SPE" is replaced with "T1L"	20-Sep-2021	eInfochips
	1.6	Customer's suggestion implemented: - Refdes change: U4-->U1; U7-->U2; U11-->U3; U10-->U4; U3-->U5; U2-->U7 - 4.7K added on ADIN1100 LED_1 pin	30-Sep-2021	eInfochips
	2.0	- Schematics is baselined; Gerber released for fabrication;	08-Oct-2021	eInfochips
	2.0	- C16 is changed to 10pF as per ADI suggestion.	25-Apr-2022	eInfochips

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