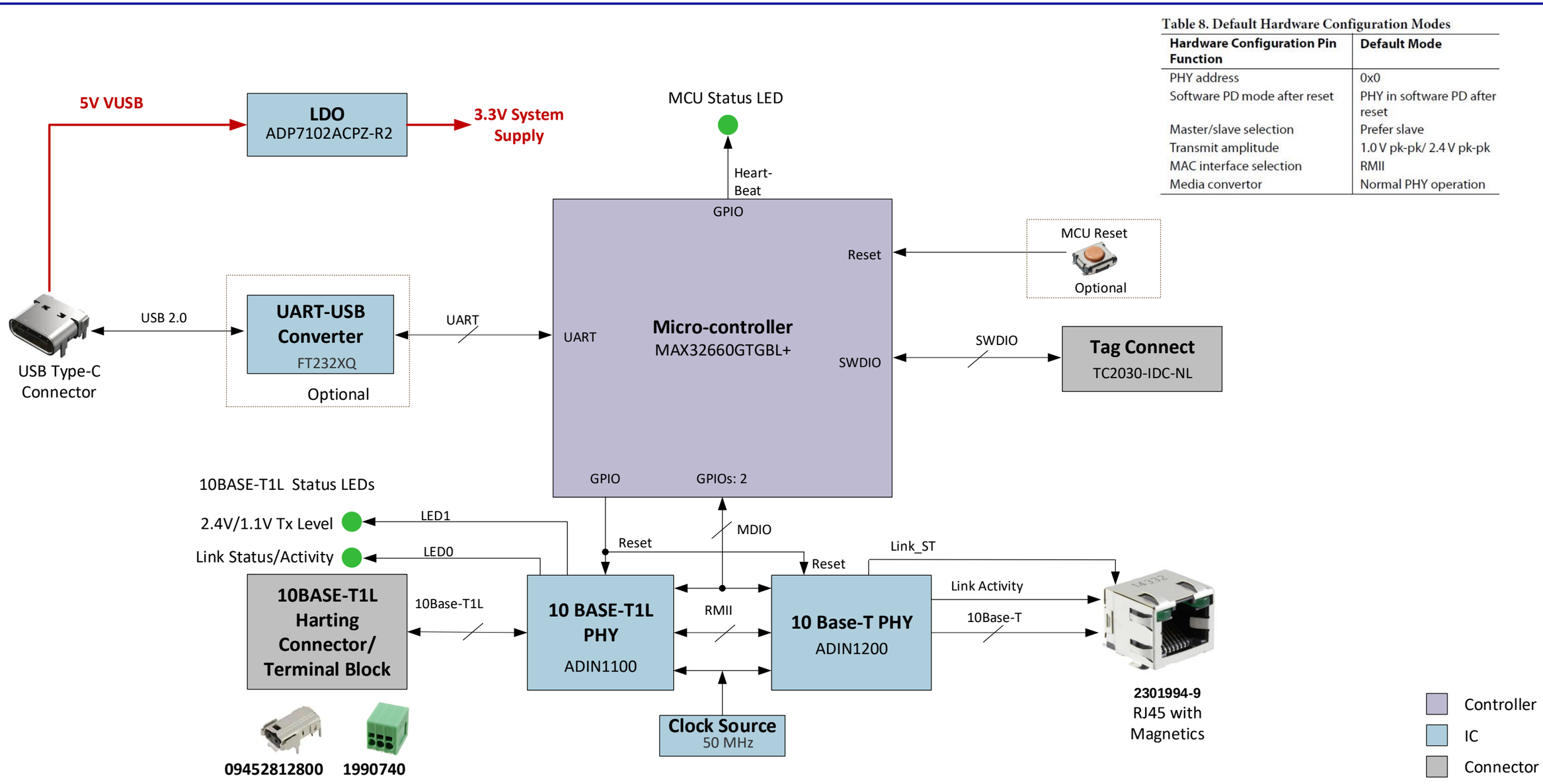
10BASE-T1L Media Converter Dongle Hardware Architecture

Rev-2.0

Table 8. Default Hardware Configuration Modes

Hardware Configuration Pin Function	Default Mode
PHY address	0x0
Software PD mode after reset	PHY in software PD after reset
Master/slave selection	Prefer slave
Transmit amplitude	1.0 V pk-pk/ 2.4 V pk-pk
MAC interface selection	RMII
Media convertor	Normal PHY operation



Revision History

Version	Date	Description
0.1	1-May-21	Initial Draft
0.2	3-May-21	Placement Feasibility added
0.3	7-May-21	DC Jack removed
0.4	13-May-21	EEPROM removed; INT and Reset are changed to optional
0.5	20-May-21	Power LED and T1L Link Status LED is removed
0.6	28-May-21	LED1 is added on ADIN1100
0.7	02-Jun-21	Link Status signals to MCU and INT are deleted.
1.0	02-Jul-21	Baselined
1.1	2-Sep-21	RJ45 part# changed to 2301994-9 Buck regulator part# changed to LDO ADP7102ACPZ-R2
2.0	07-Oct-21	Baselined