

System Generator

{Modeling to Hardware Synthesis}

Prepared by

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Step 1: Invoke System Generator.

On Windows systems select **Start > All Programs > Xilinx Design Tools > Vivado 2015.x > System Generator > System Generator 2015.x**.

Step 2: Design the following with the required blocksets from the Simulink Library.

In this lab, first we will make a design as shown in figure 1.

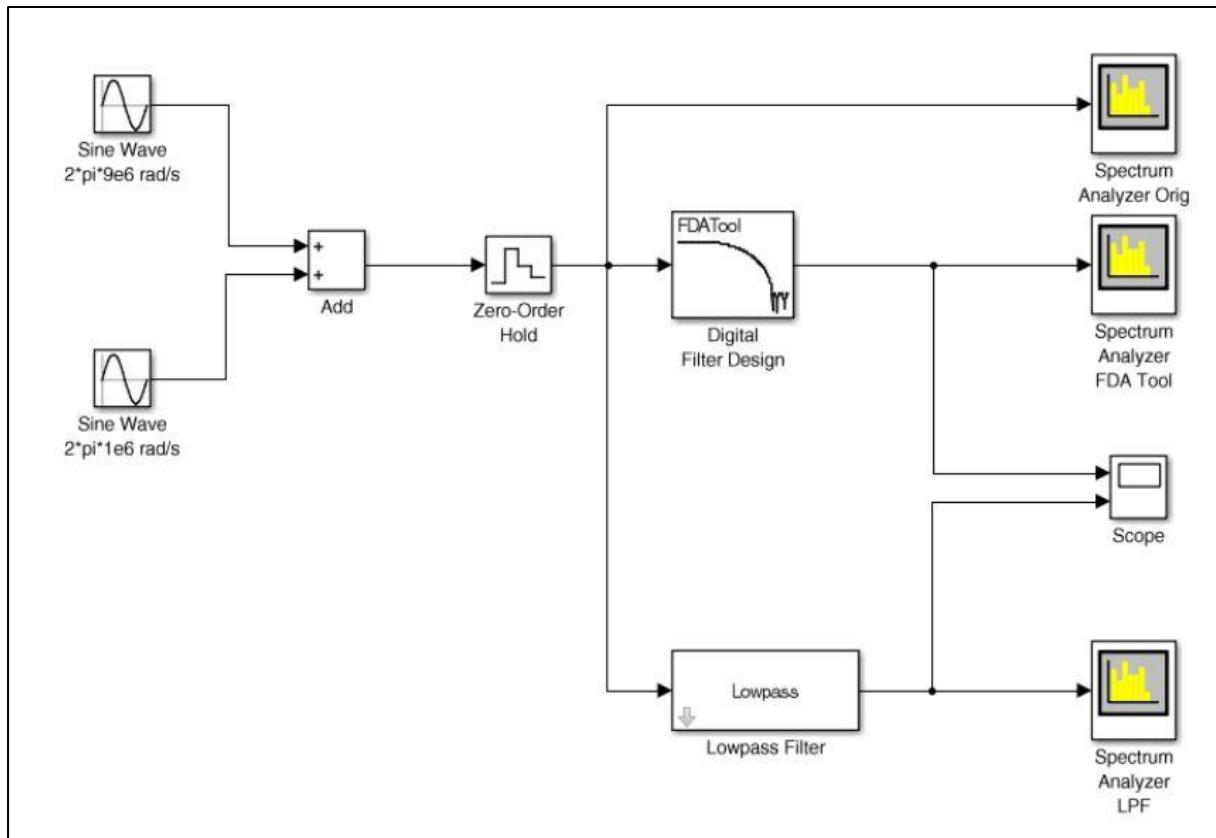


Figure 1: Lab1 Design

Step 3: Adding and Configuring different blocks from Simulink Library.

1. Click on **Simulink Library** in the MATLAB Window, and add the blocks as per the design requirements shown in the figure 1.

2. Make new file by pressing *Ctrl + N*.
3. Add two Sine Wave: *Simulink > Sources > Sine Wave* as shown in the figure 2.
Right Click on *Sine Wave* > *Add to Untitled*.
Rename them by clicking on the instance name as per the design.

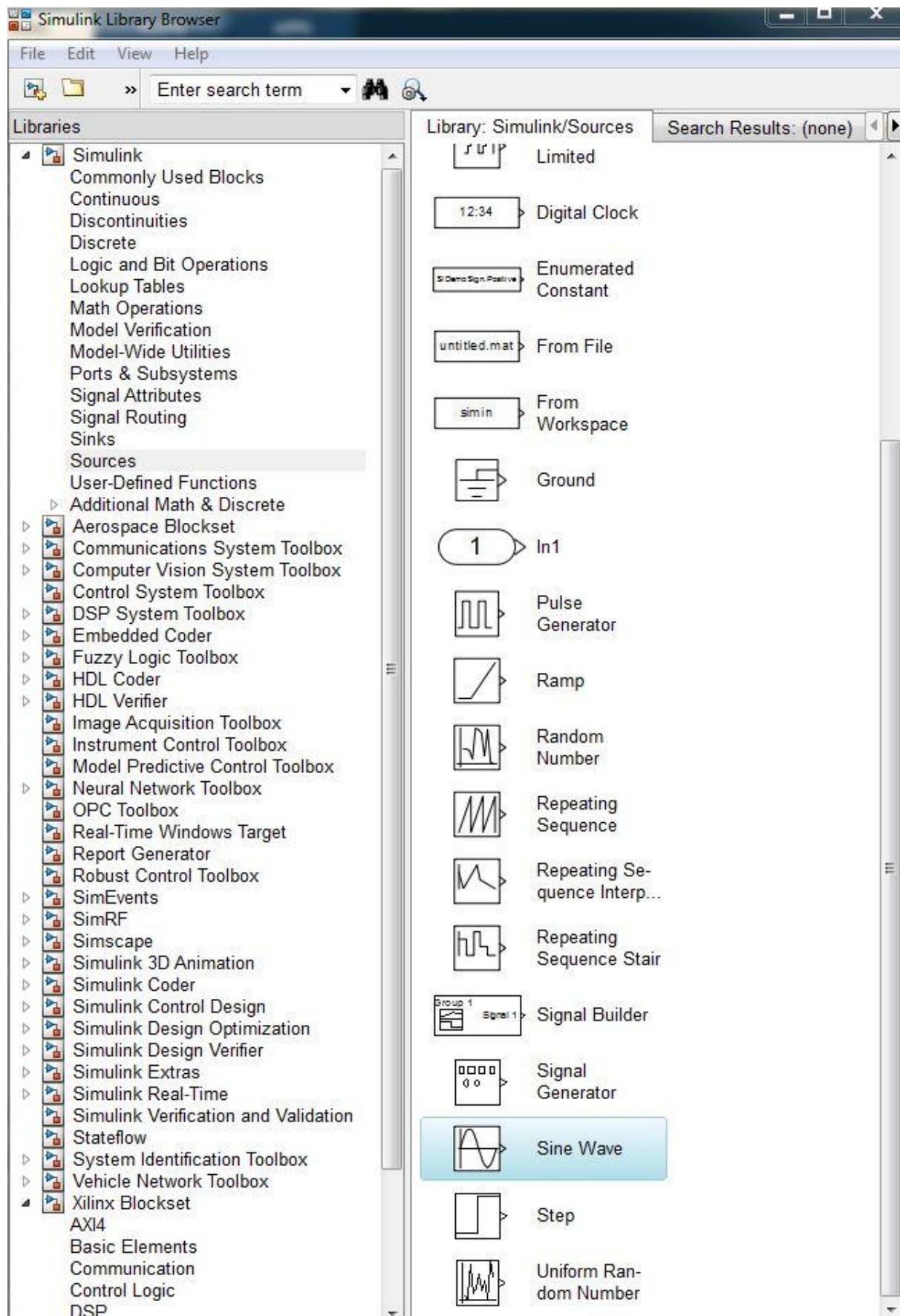


Figure 2 (a): Sine Wave block

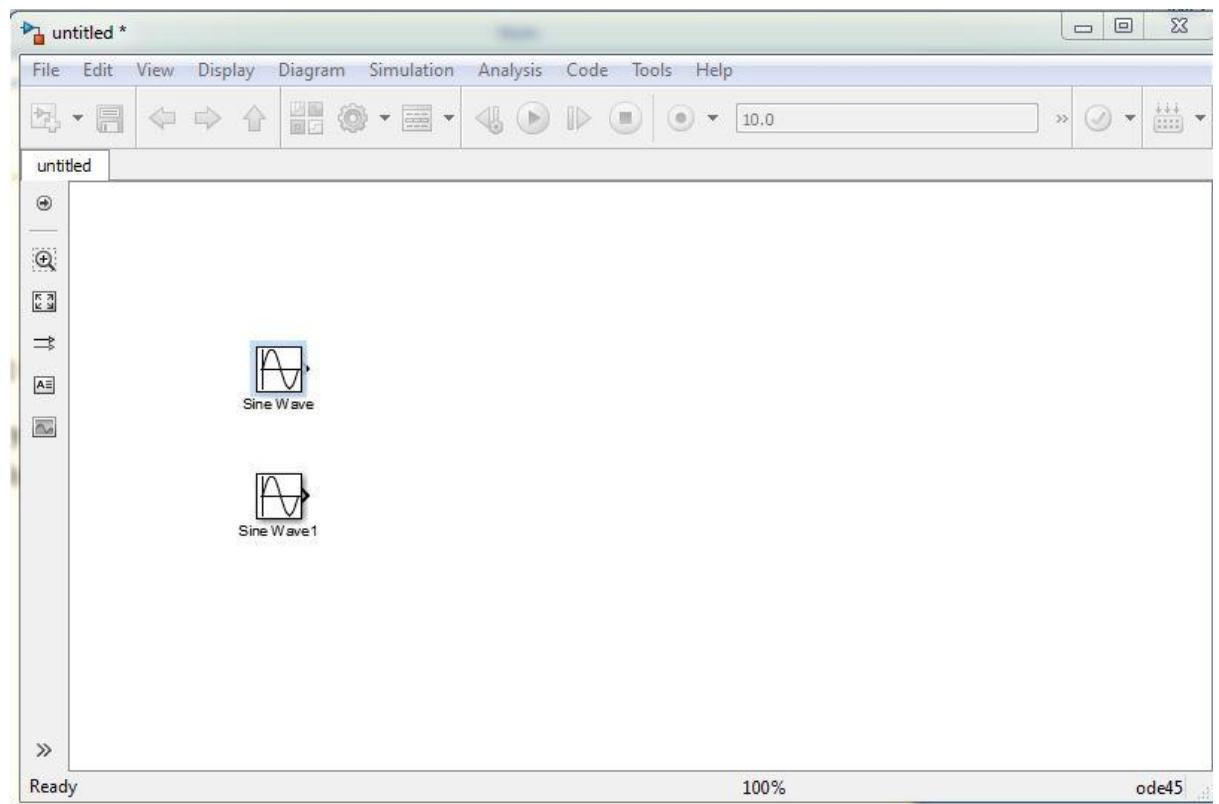


Figure 2 (b): Adding two Sine Wave.

4. Add *Add* block *Simulink > Math Operations > Add* as shown in figure 3.

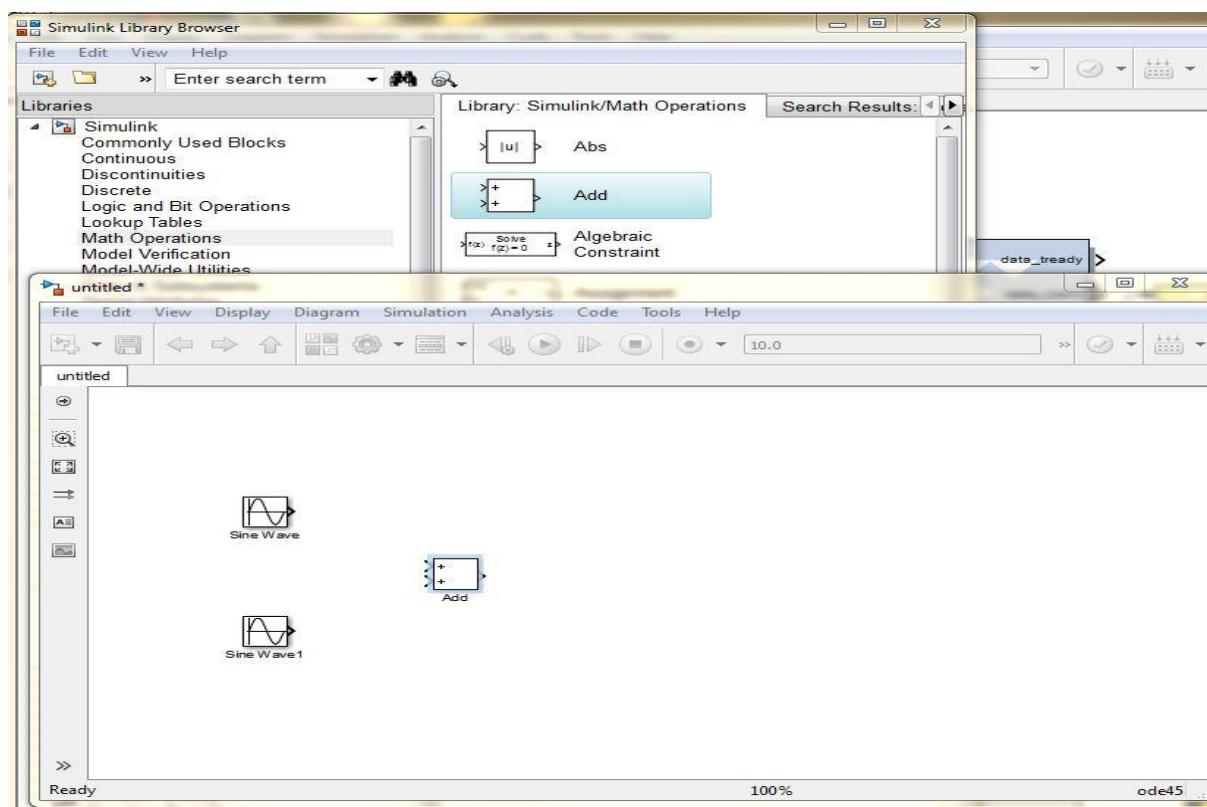


Figure 3: Add block addition.

5. Add Zero-Order Hold: *Simulink > Discrete > Zero-Order Hold* as shown in figure 4.

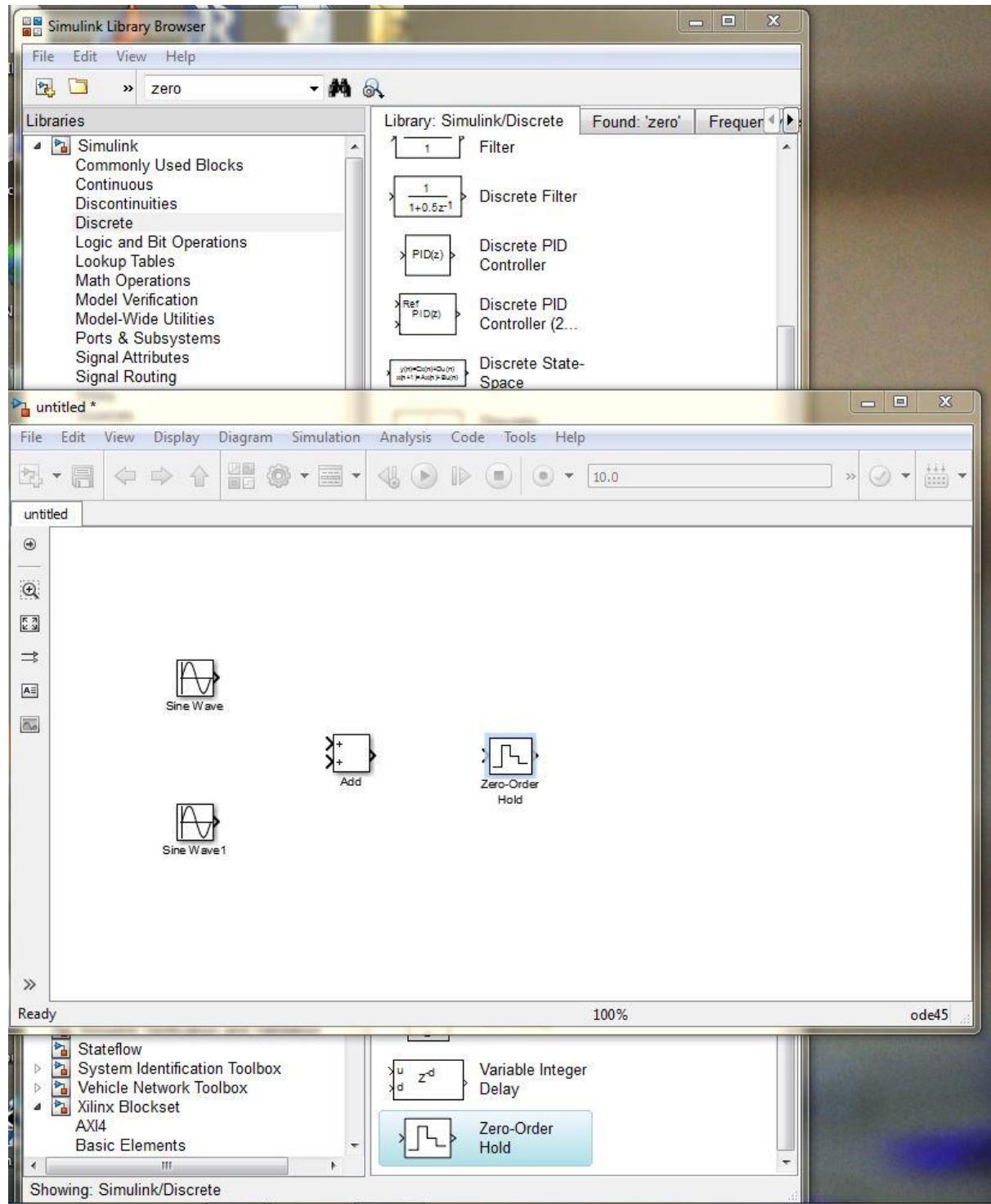


Figure 4: Addition of Zero-Order Hold.

6. Add FDATool block: *Xilinx Blockset > DSP > FDATool* as shown in the figure 5.
Rename the instance as per the design in figure 1.

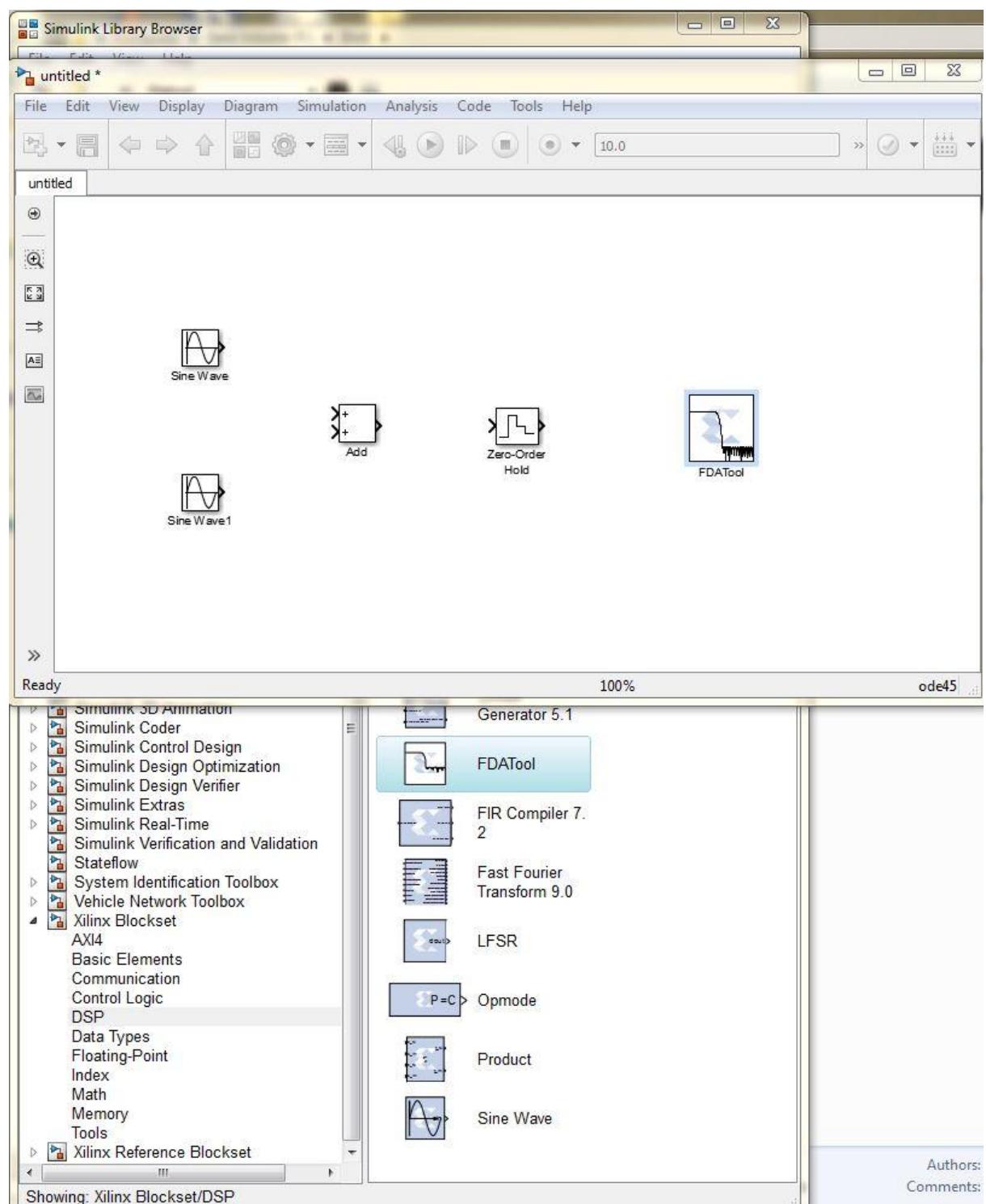


Figure 5: Addition of FDATool block.

7. Add Low Pass Filter: *DSP System Toolbox* > *Filtering* > *Filter Designs* > *Low Pass Filter* as shown in figure 6.

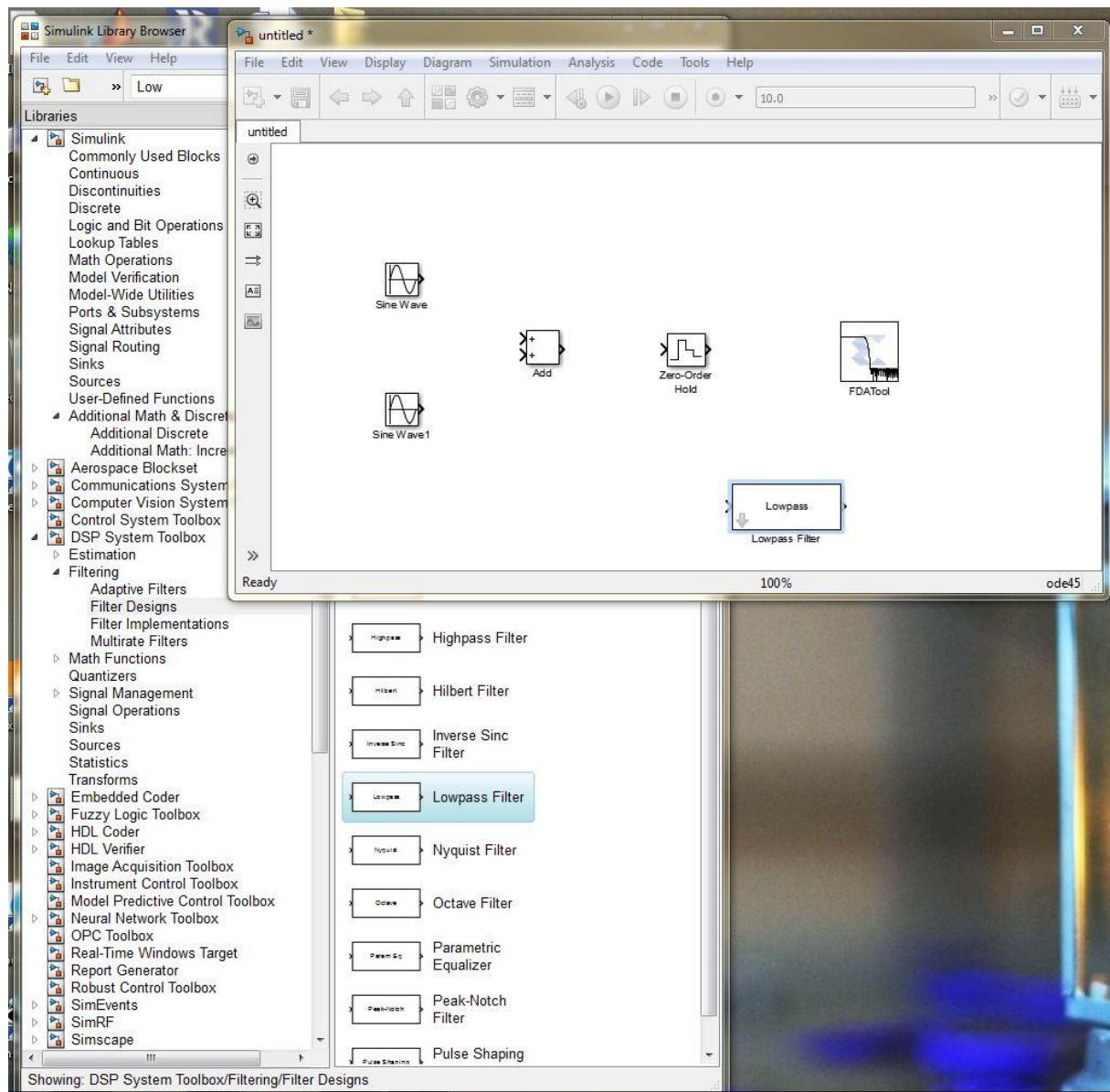


Figure 6: Addition of Low Pass Filter.

8. Add **three Spectrum Analyzer**: *DSP System Toolbox > Sinks > Spectrum Analyzer* as shown in figure 7.

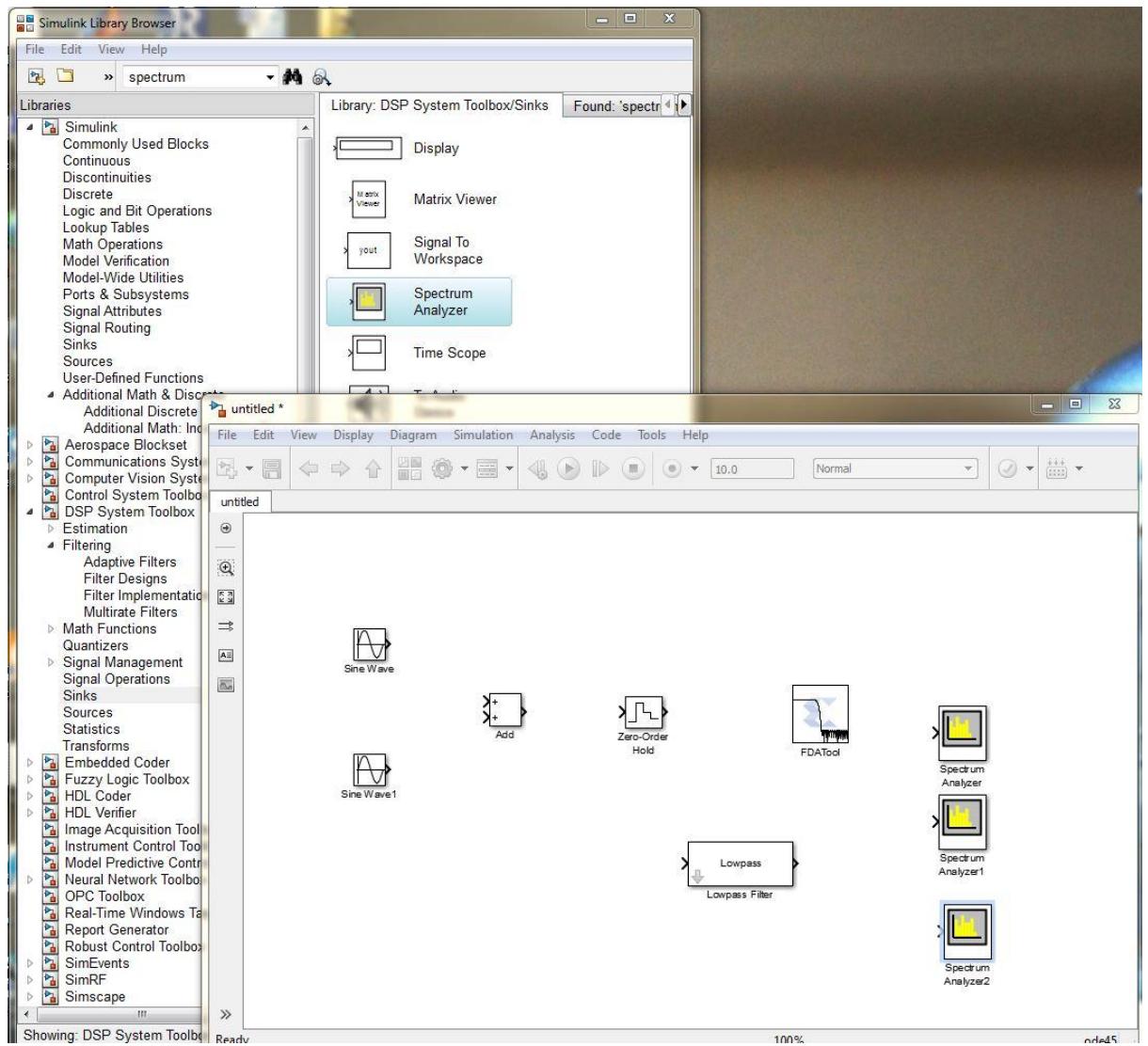


Figure 7: Addition of Spectrum Analyzer.

9. Add Scope: *Simulink > Sinks > Scope* as shown in figure 8.

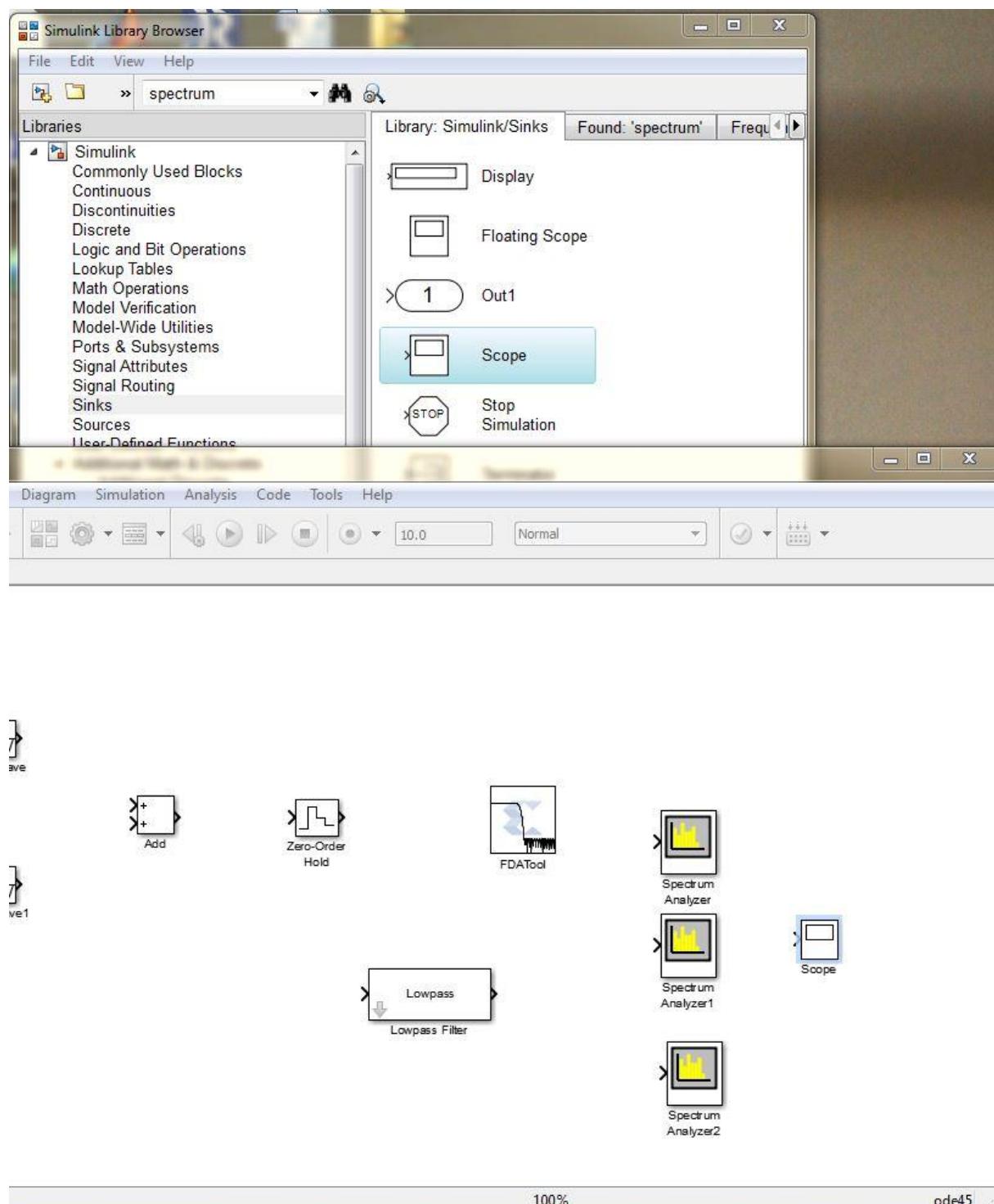


Figure 8: Addition of Scope.

Step 4: Configure each blocks

Now, after adding all the required blocks, we have to configure each blocks to obtain desired output as per the specifications.

1. For the block **Sine Wave 2*pi*9e6 rad/s**: We have changed **Frequency (rad/sec)** to **2*pi*9e6** as shown in the figure 9.

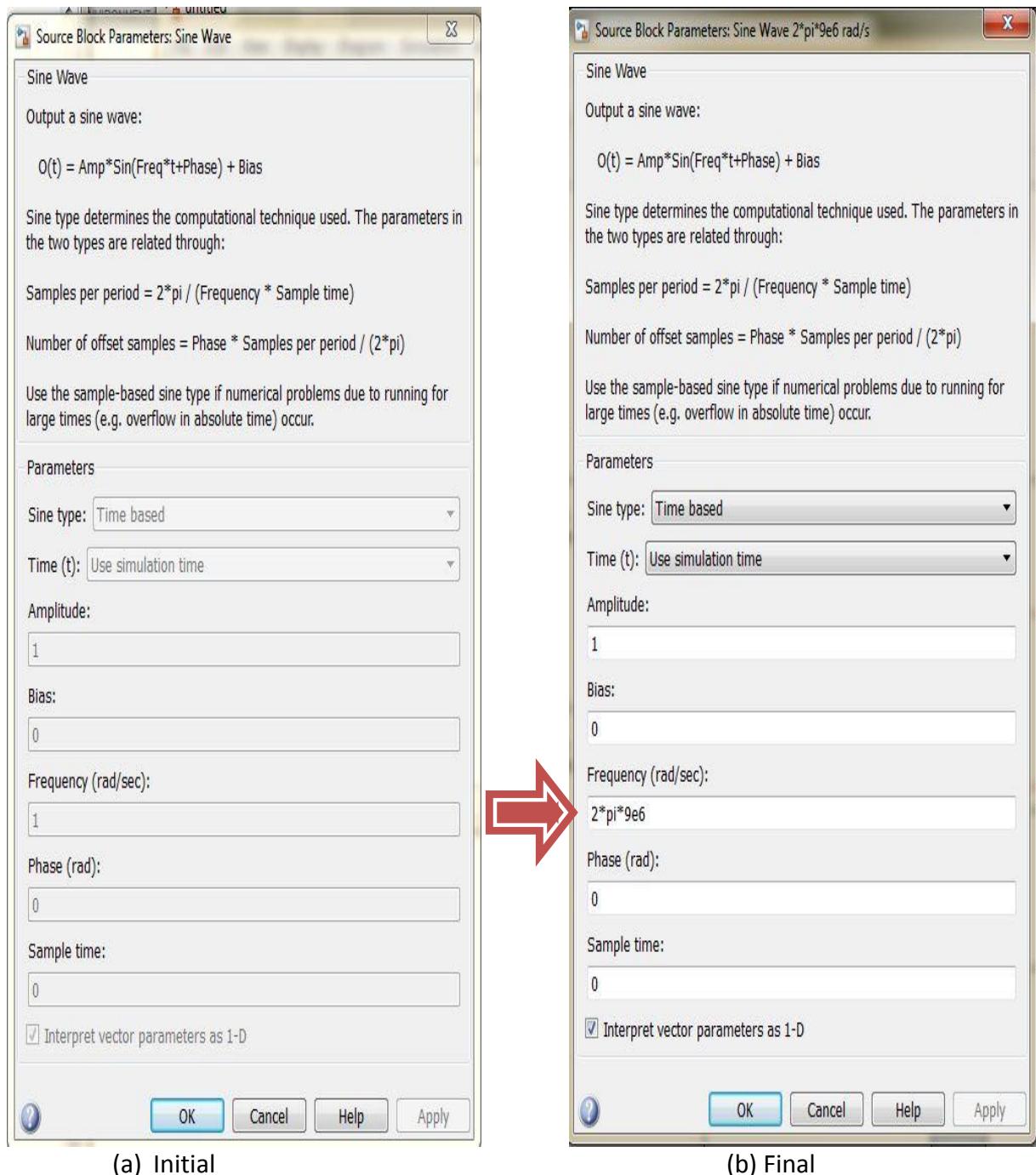


Figure 9: Sine Wave Source of frequency $2\pi \times 9 \times 10^6$ rad/s

2. For block **Sine Wave** $2\pi \cdot 10^6$ rad/s: We have changed **Frequency (rad/sec)** to $2\pi \cdot 10^6$ as shown in the figure 10.

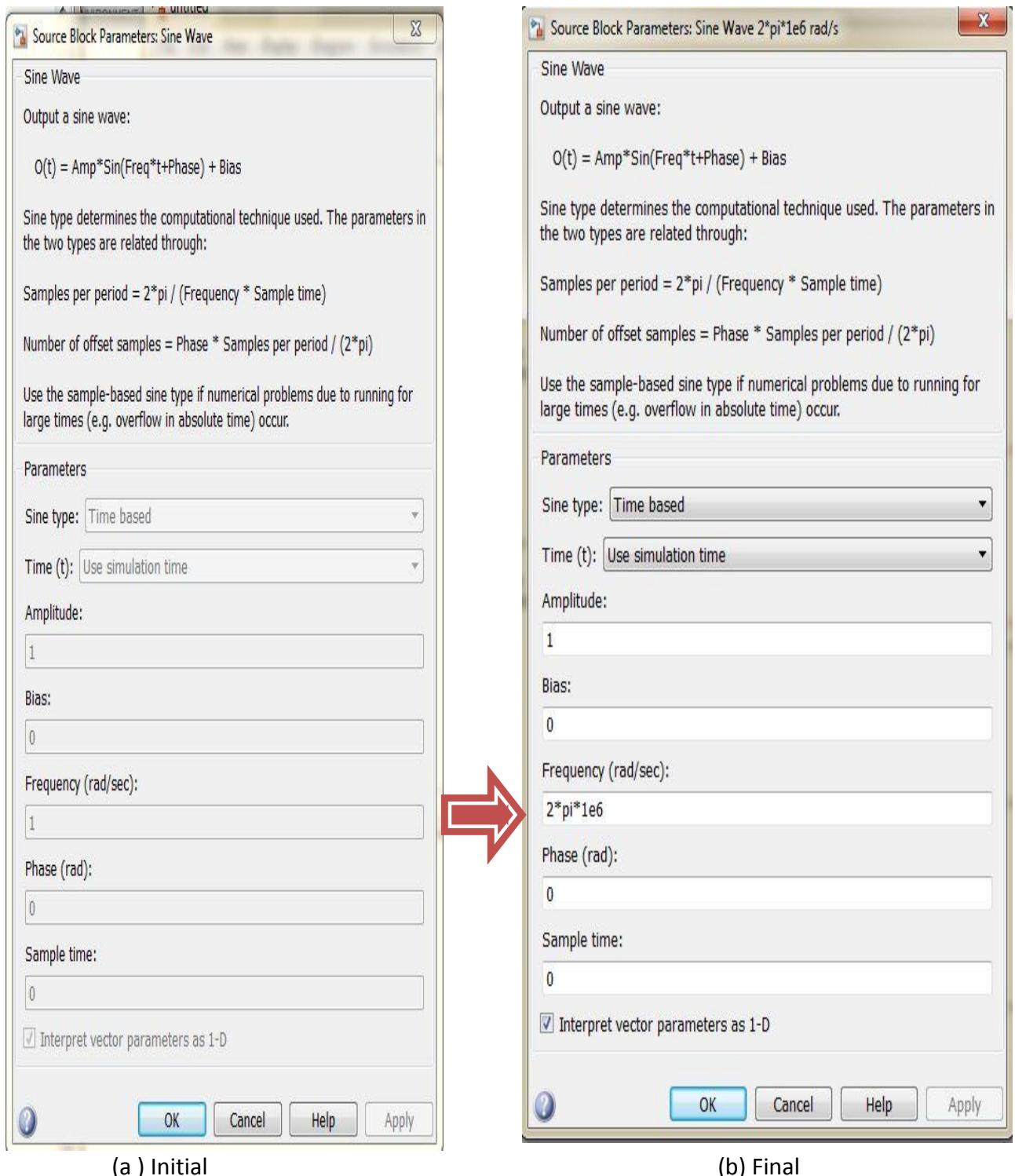


Figure 10: Sine Wave Source of frequency $2\pi \cdot 10^6$ rad/s.

3. For **Add** block: Figure 11 shows the default properties of the Add block as no change is required in the properties.

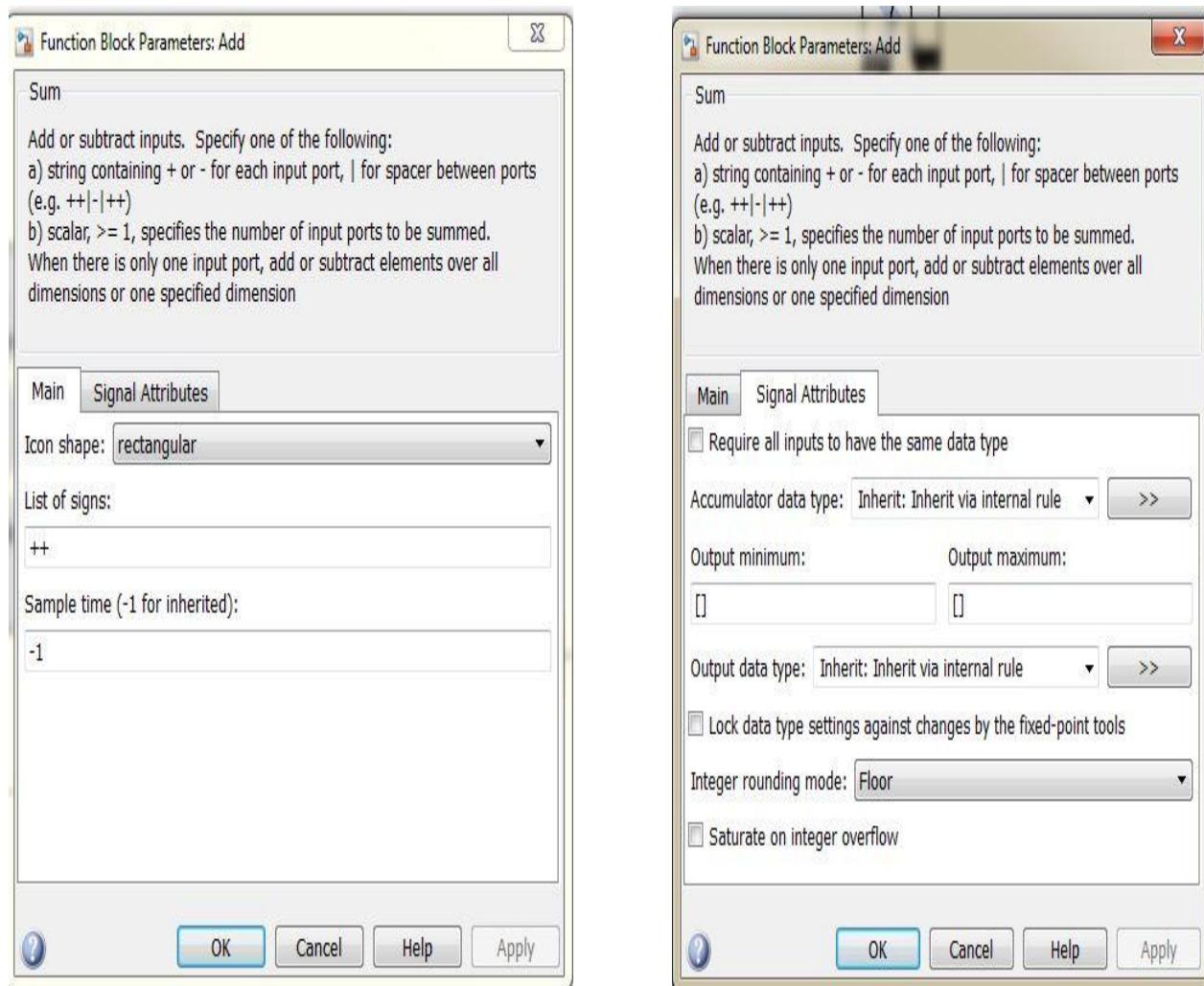
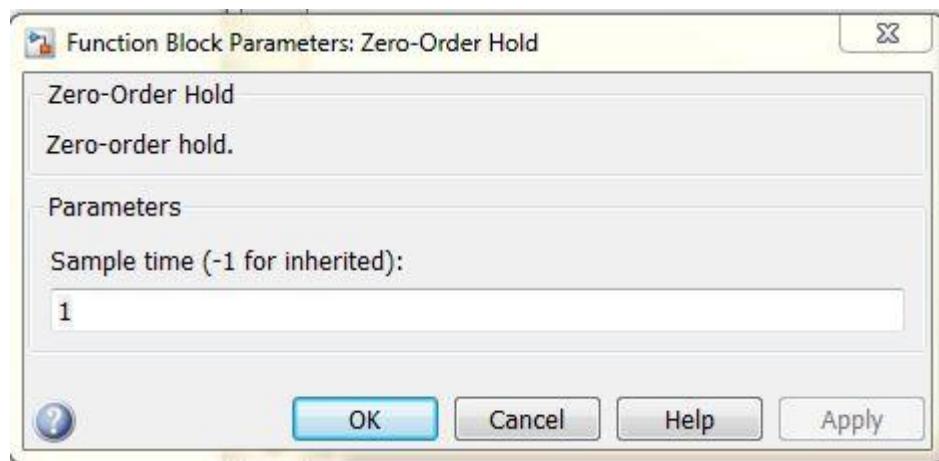
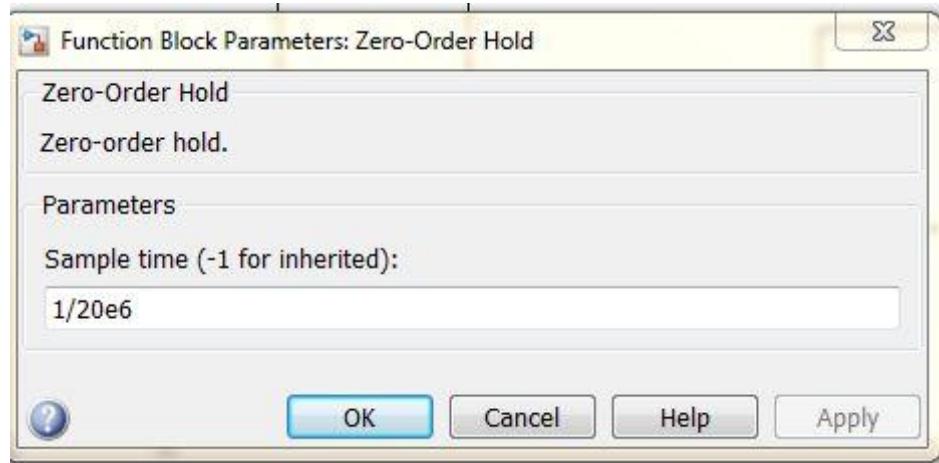


Figure 11: Add block properties.

4. For block **Zero-Order Hold**: We have changed the **Sample time to $1/20e6$** as per our design requirement as shown in figure 12.



(a) Initial



(b) Final

Figure 12: Zero-Order Hold properties.

5. For block **Digital Filter Design(From FDATool)**: Properties as shown in figure 13.

Make the following changes.

i. *Frequency Specifications*

Units = MHz

Fs = 20

Fpass = 1.5

Fstop = 8.5

ii. *Magnitude Specifications*

Units = dB

Apass = 0.01

Astop = 100

iii. *Response type: Low Pass*

After making above changes, click on *Design Filter*.

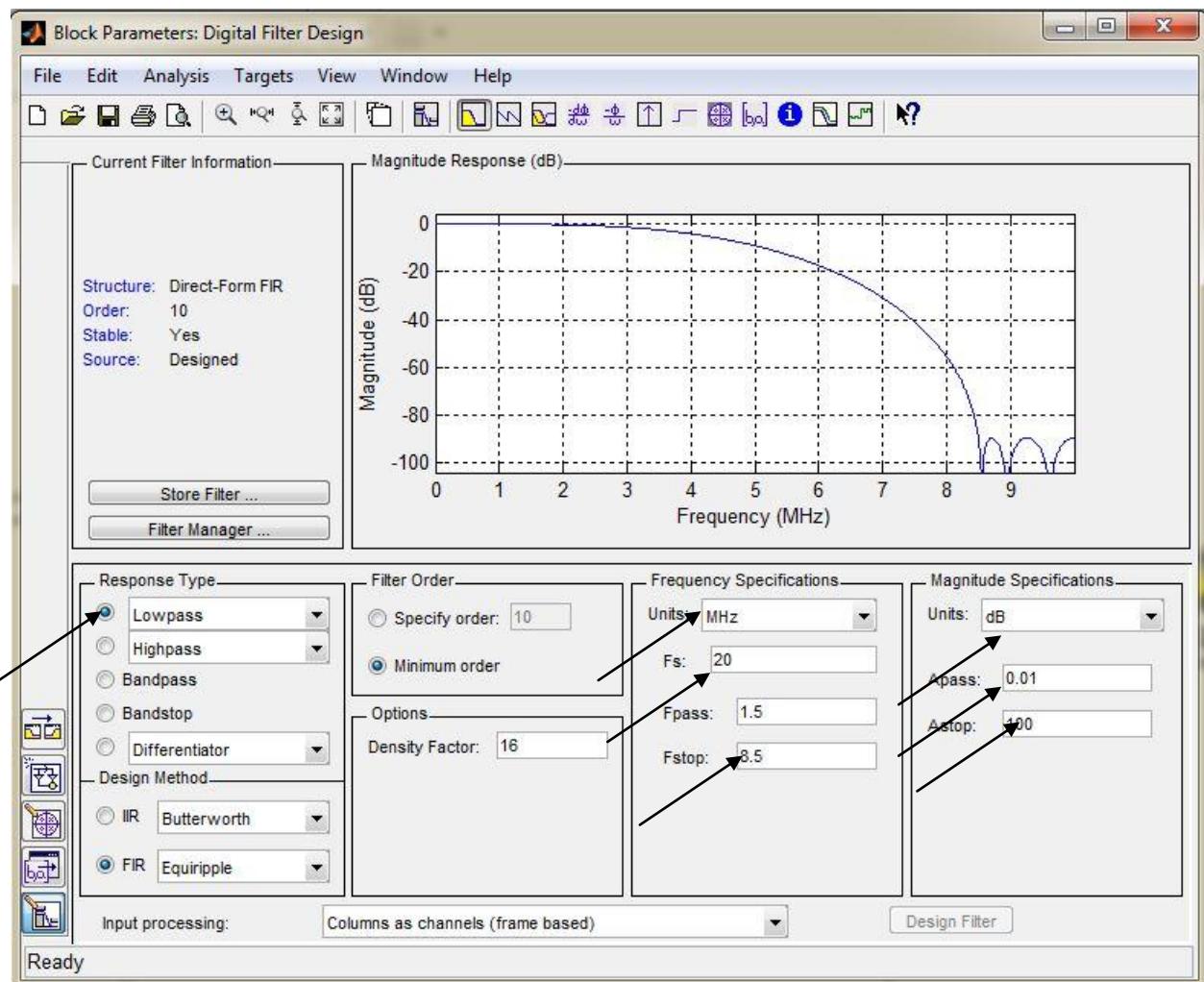


Figure 13: Digital Filter Design

6. For block **Low Pass Filter**: We have made following changes as shown in the figure 14:

In Frequency Specifications:

Frequency units: Mhz

Input sample rate: 20

Passband frequency: 1.5

Stopband frequency: 8.5

Passband Ripple: 0.01

Stopband Attenuation: 80

Click **OK** to save the properties.

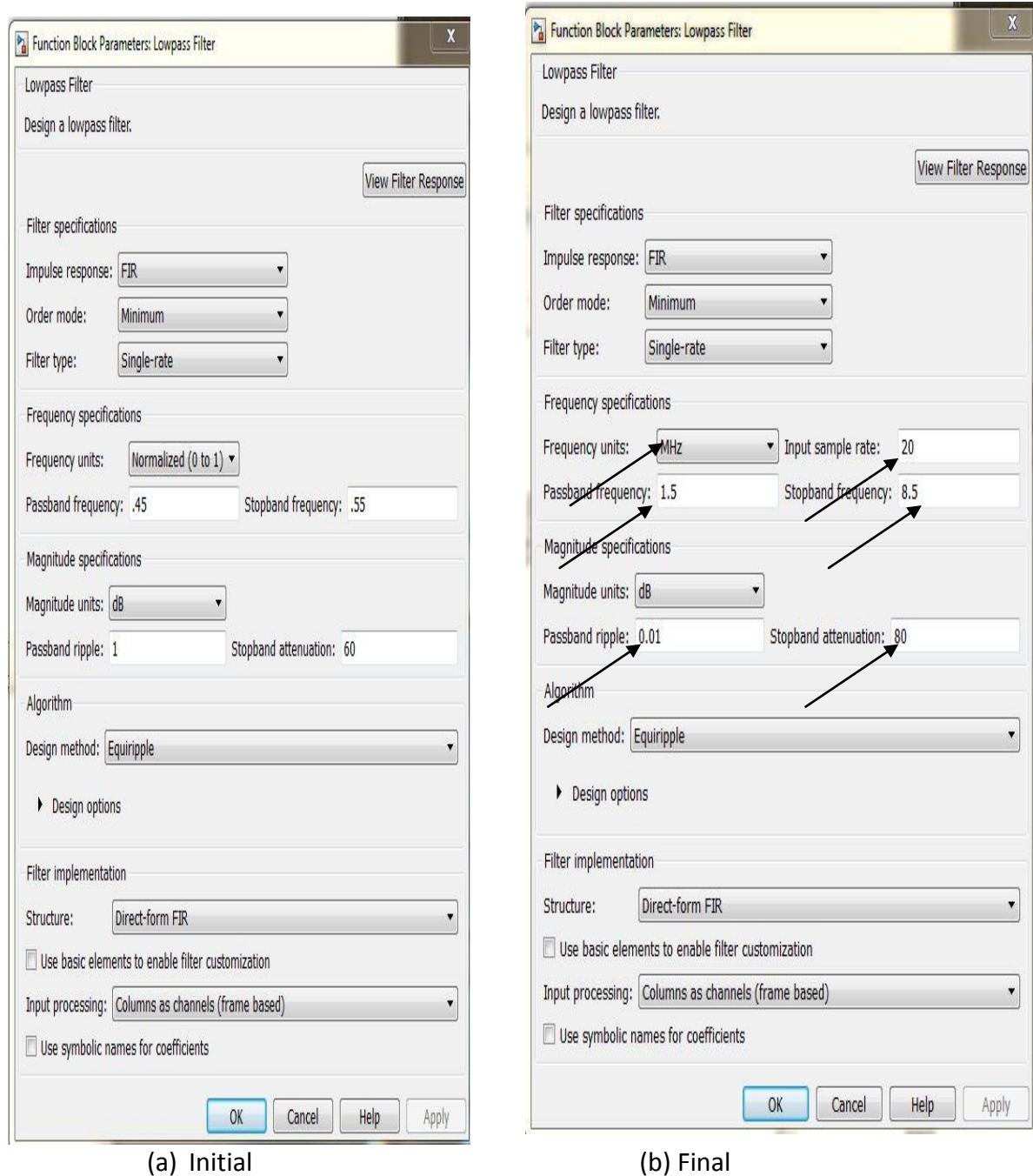


Figure 14: Low Pass Filter properties.

7. For **Spectrum Analyzer**: There will no specific changes required in the properties of the Spectrum Analyzer as shown in figure 15, changes to see different forms of output can easily be made while running the simulation itself dependent on what properties we want to see in the output.

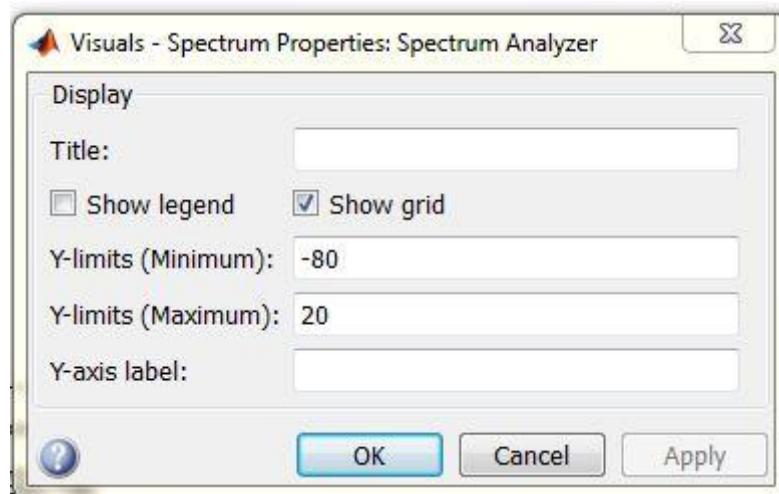


Figure 15: Spectrum Analyzer Properties.

8. For **Time Scope**: In Time Scope, we have to change *Number of Axes* = 2 as shown in the figure 16.

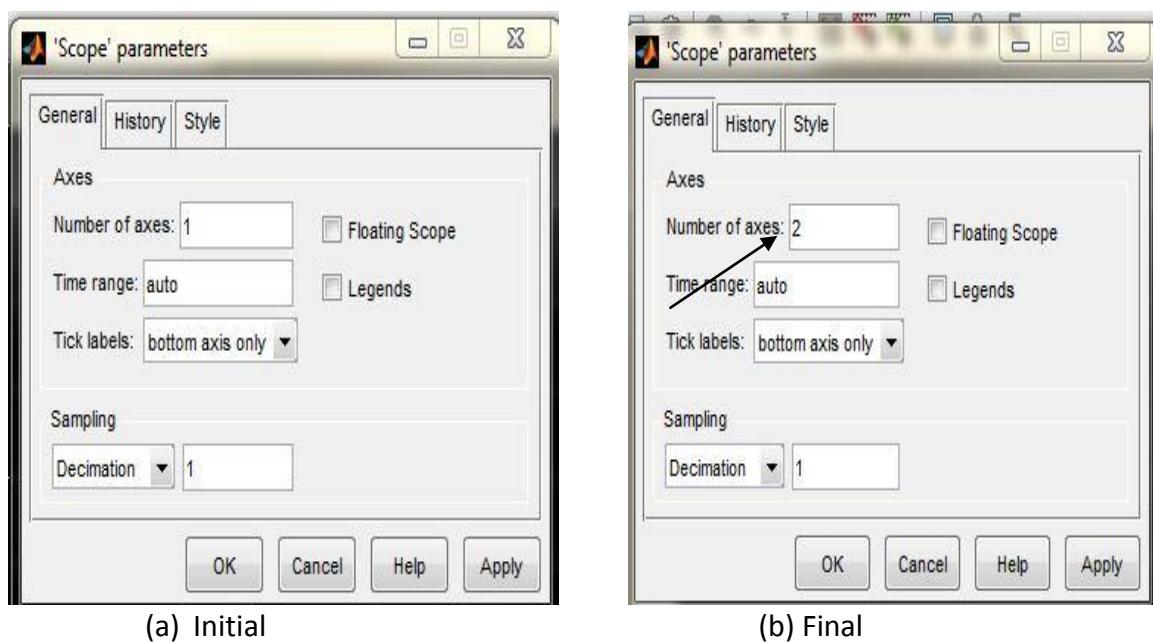


Figure 16: Scope block Properties.

Step 5: Connection and Saving of File.

After configuring each block, we will connect the blocks as per the design shown in figure 1. And Save the file as *File > Save As > Lab1*.

Step 6: Run Simulation.

Run the simulation by clicking *Run* as shown in figure 12.

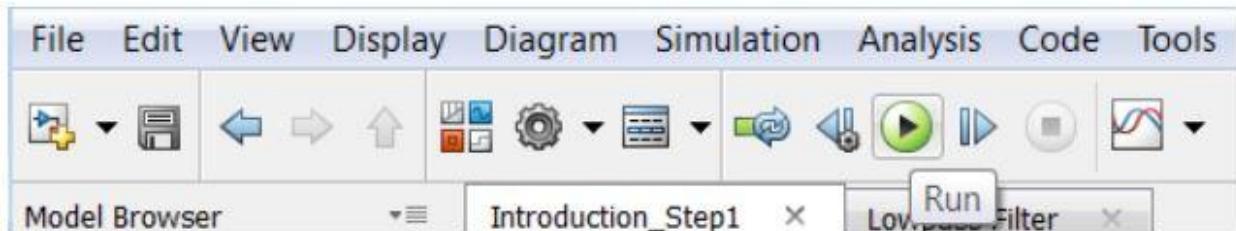


Figure 17: Running the simulation.

We will get the following output spectrums as shown in figures 18, 19 and 20.

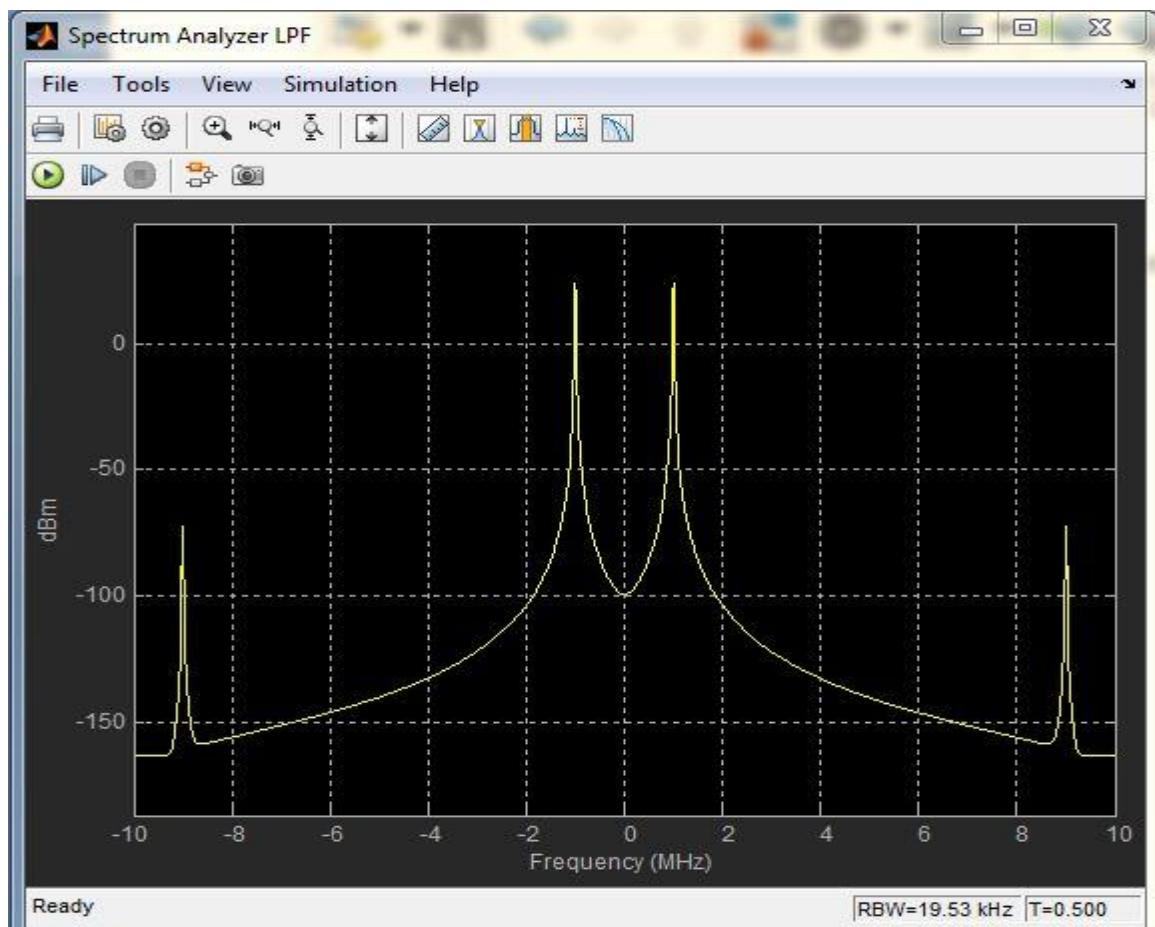


Figure 18: Spectrum of Spectrum Analyzer LPF

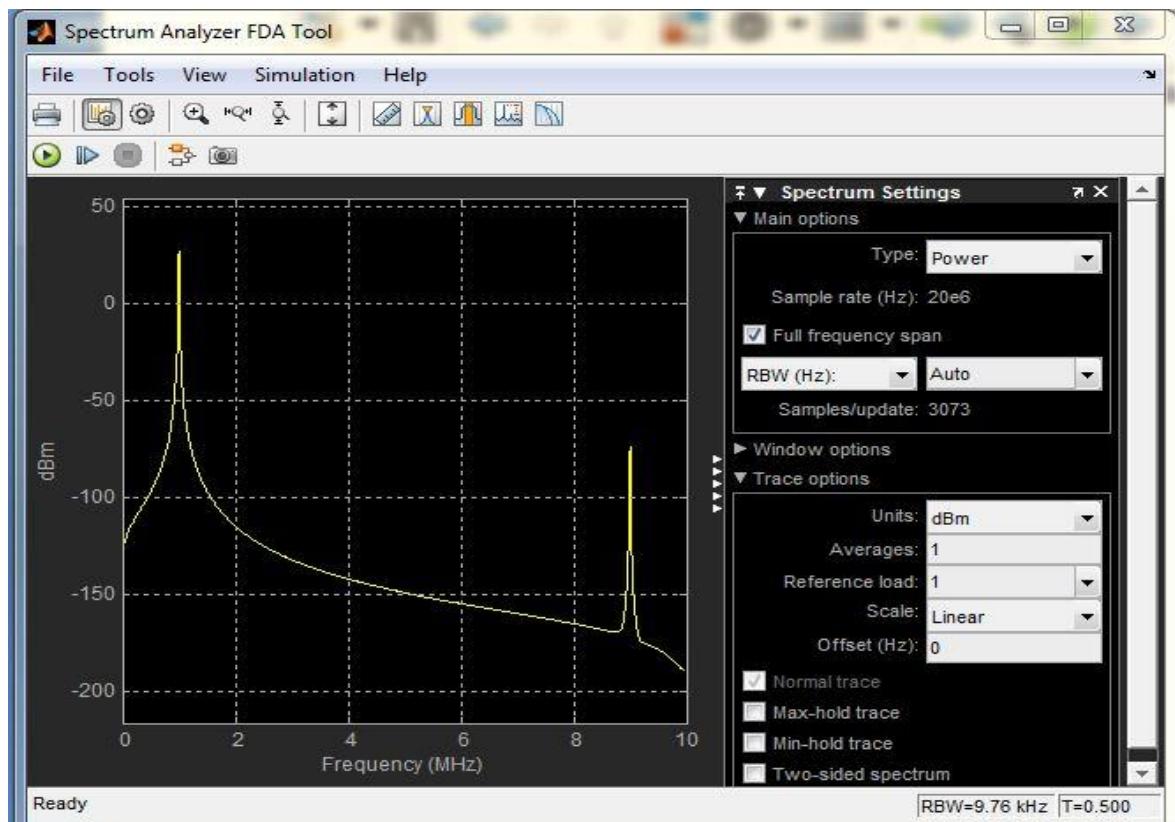


Figure 19: Spectrum of Spectrum Analyzer FDATool.

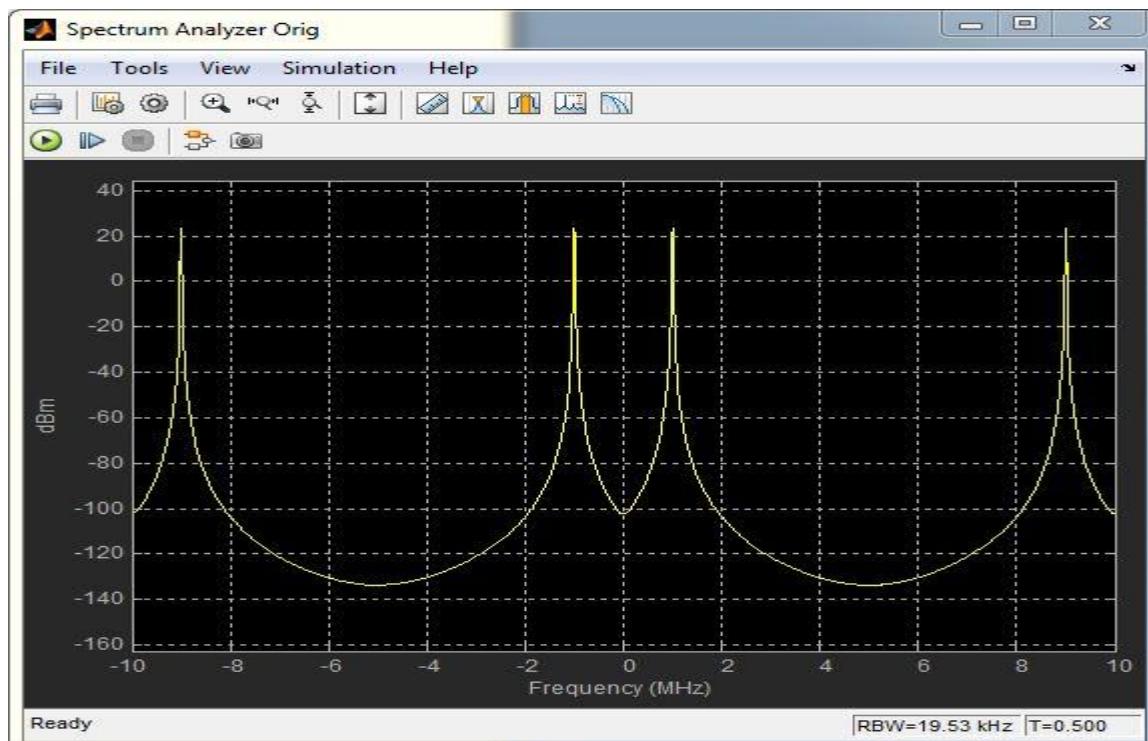


Figure 20: Spectrum of Spectrum Analyzer Orig.

Step 7: Creation and Configuration of System Generator blocks

Now, we will create a version of the same filter design using System Generator blocks for implementation in an FPGA and we will be configuring the blocks simultaneously.

1. Open **Simulink Library** from MATLAB Window and expand the **Xilinx Blockset** menu, select **DSP**, then select **FIR Compiler 7.2**.
2. Right-click the **FIR Compiler 7.2** block and select **Add block to model Lab1_1.(as shown in figure 21)**

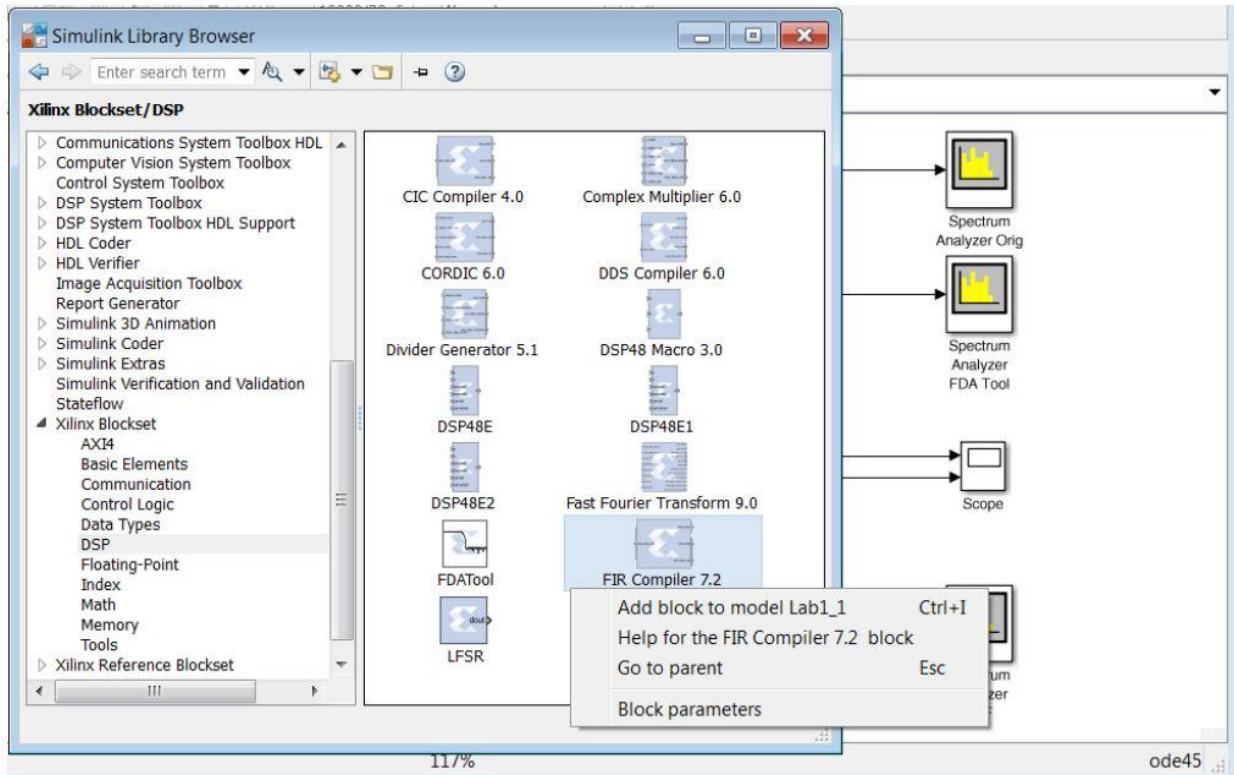


Figure 22: Adding of **FIR Compiler** Block from Simulink Library.

After adding the **FIR Compiler** block, double-click the **FIR Compiler** instance to open the Properties Editor.

3. In the **Basic Elements** menu, select **Gateway In** and add it to the design and edit the **Sample Period** to **1/20e6** as shown in the figure 23 (b).

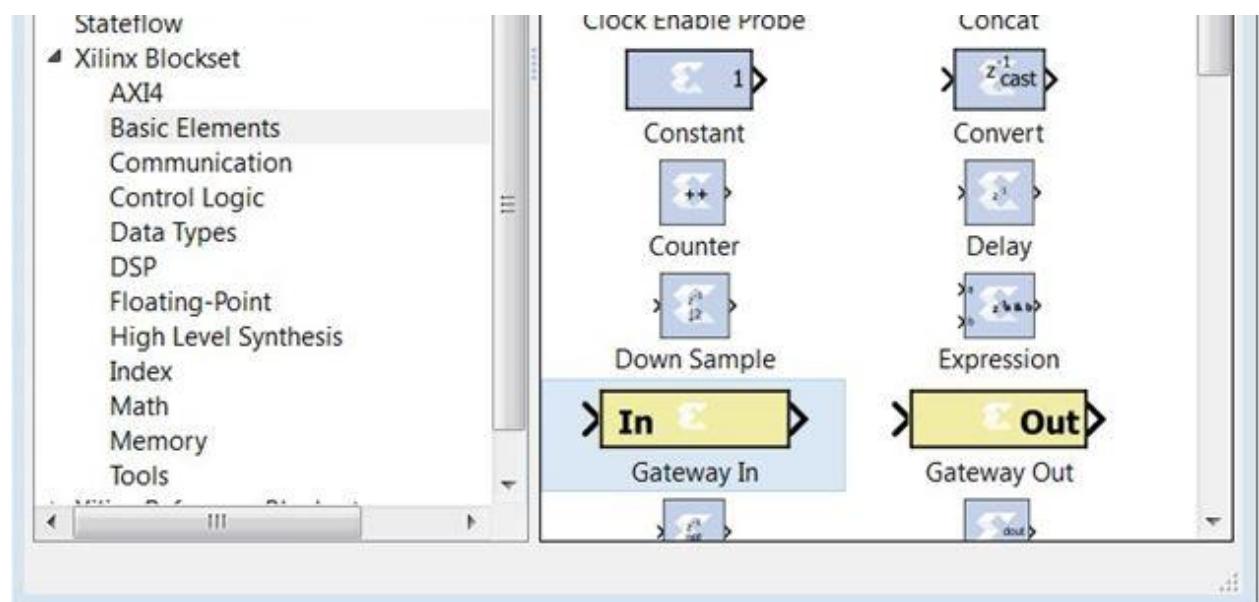


Figure 23 (a): Gateway In and Gateway Out blocks.

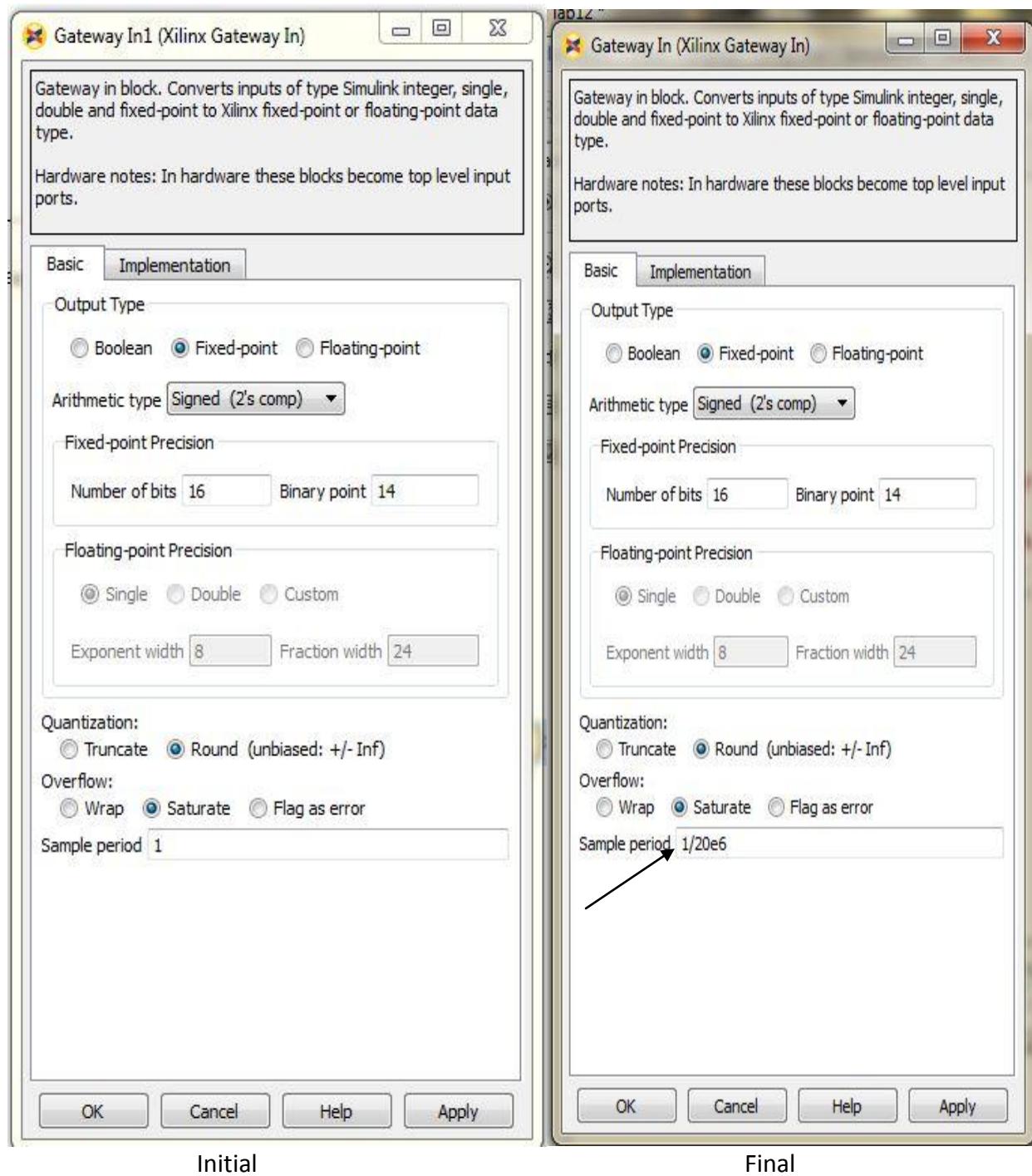


Figure 23 (b): Modifications in Gateway In block.

4. Similarly, from the same menu as shown in figure 23 (a), add a **Gateway Out** block to the design and edit its properties as shown in figure 24.

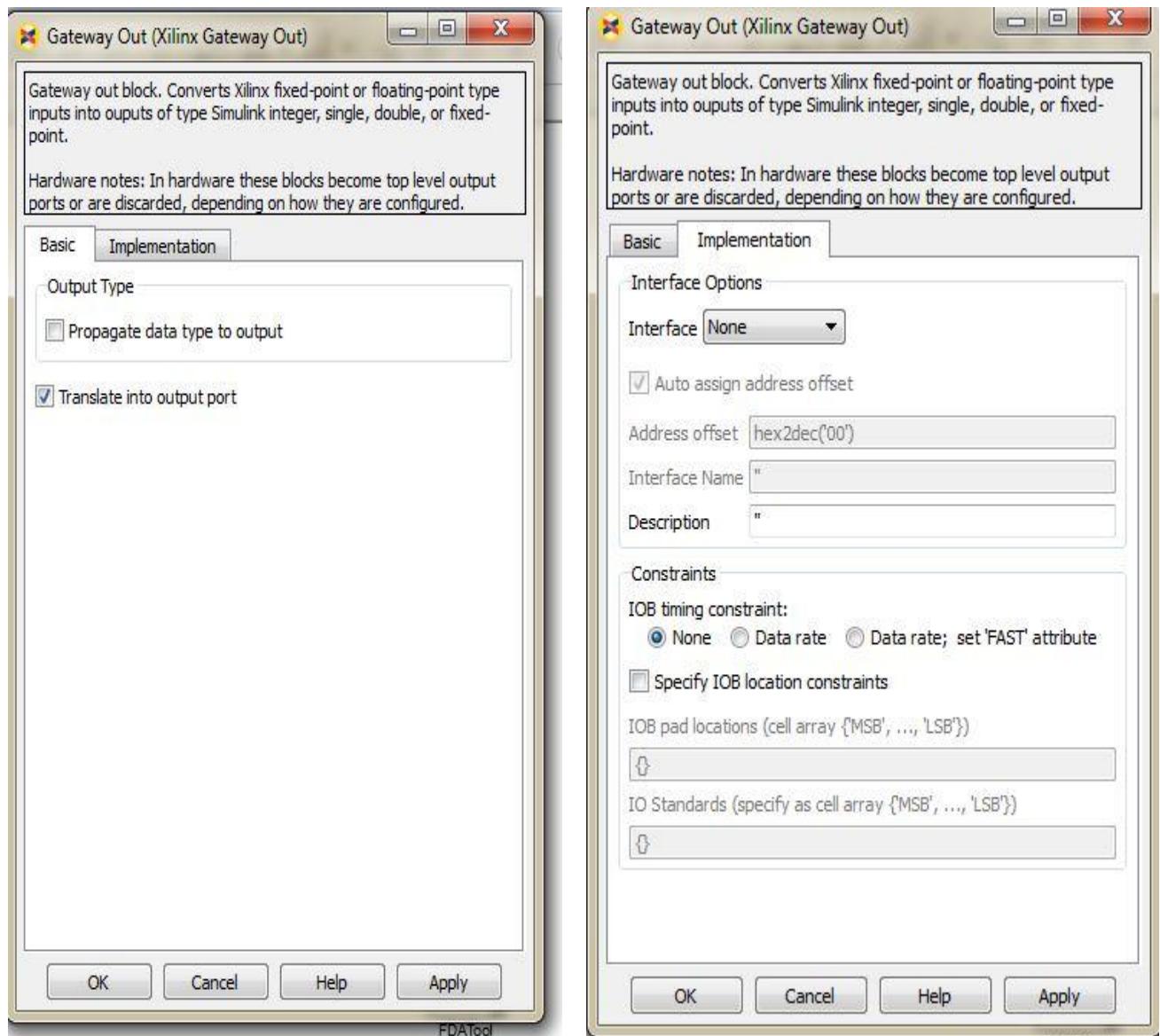


Figure 24: Gateway Out Block and its properties.

5. Add Constant: *Xilinx Blockset* > *Basic Elements* > *Constant* as shown in figure 25.

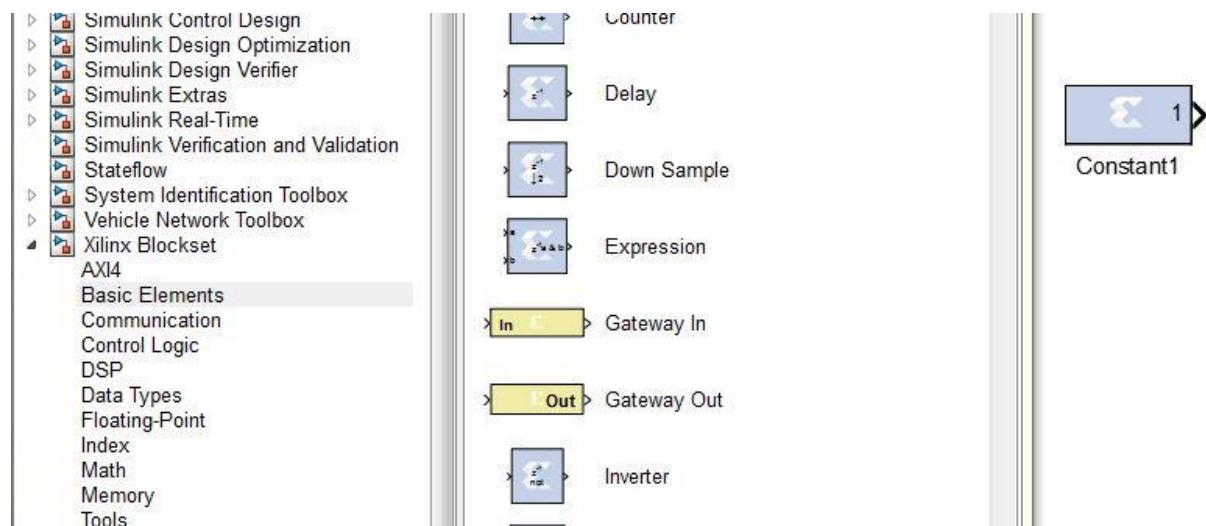


Figure 25: Constant Block Addition.

Change its **Output type** to **Boolean** as shown in figure 26.

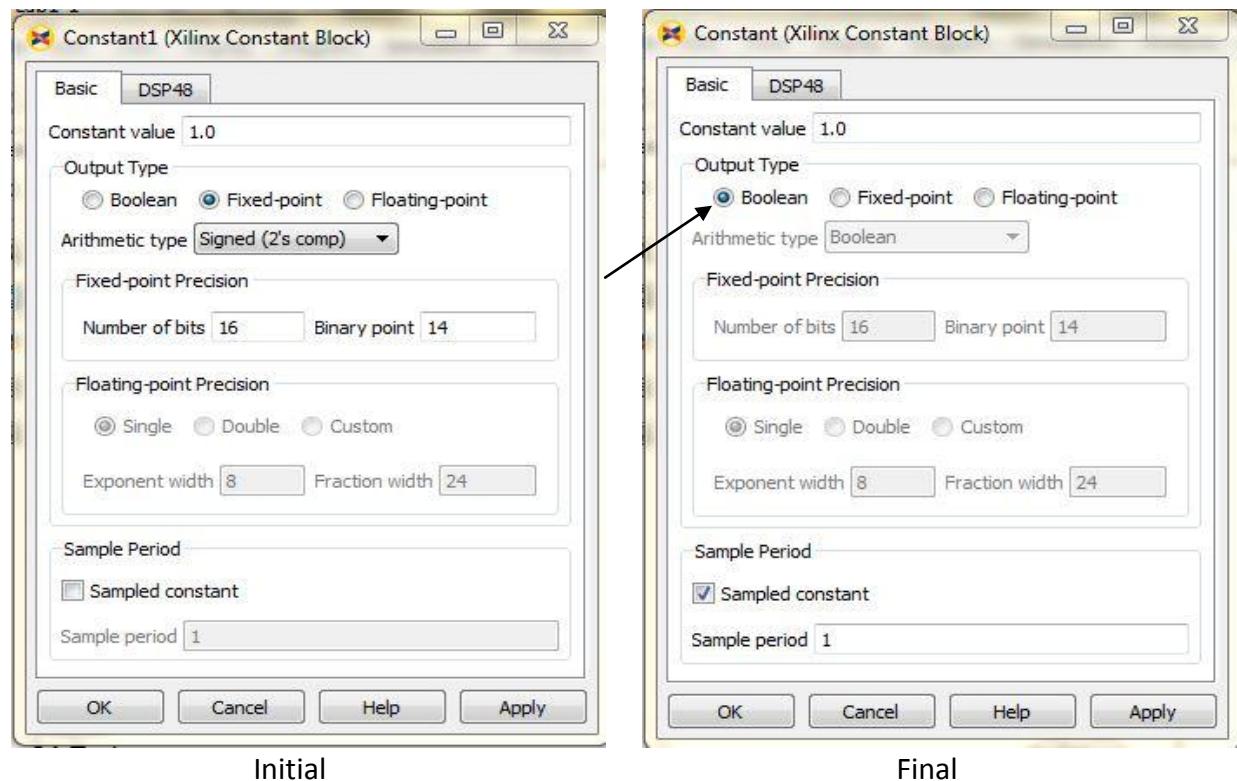


Figure 26: Constant Block Properties.

6. Similarly, from the same menu add the **System Generator** token used to define the FPGA technology.
7. Finally, make a copy of one of the existing Spectrum Analyzer blocks and rename the instance to **Spectrum Analyzer SysGen** by clicking the instance name label and editing the text.

Step 8: Configuring FDATool Block

Now, we have to configure the FDATool Block to have the properties as same as the **Digital Filter Design** that we have set earlier. Figure 27 shows the necessary changes made in the default properties.

Following changes are to be made:

- i. *Frequency Specifications*
Units = MHz
Fs = 20
Fpass = 1.5
Fstop = 8.5
- ii. *Magnitude Specifications*
Units = dB
Apass = 0.01
Astop = 100
- iii. *Response type: Low Pass*

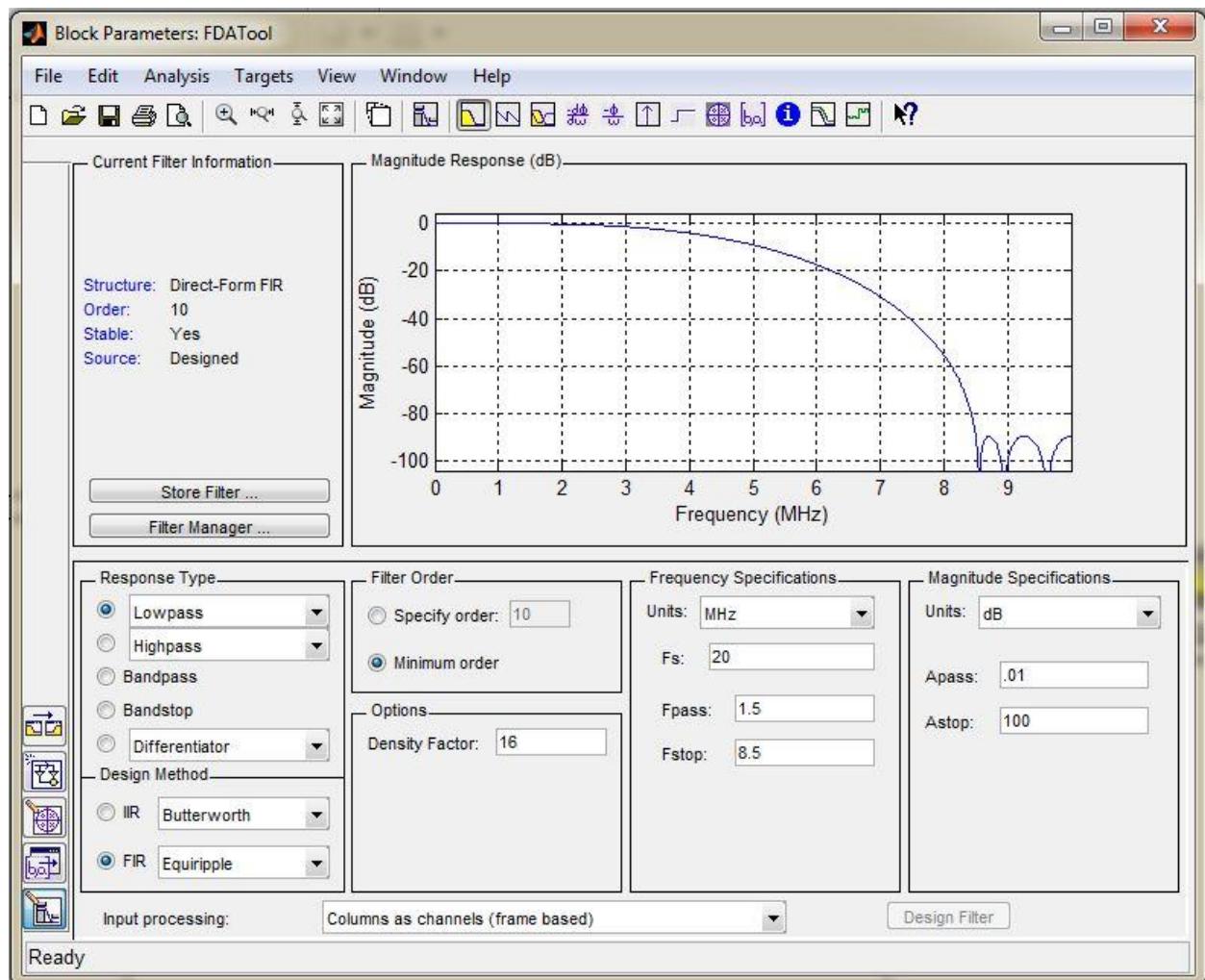


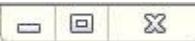
Figure 27: FDATool

Step 9: Configuring the FIR Compiler 7.2 block

Now, we will configure the FIR Compiler 7.2 as shown in figure 28.



FIR Compiler 7.2 (Xilinx FIR Compiler 7.2)

**Filter Specification** **Channel Specification** **Implementation** **Detailed Implementation** **Interface** **Advanced****Filter Coefficients****Coefficient Vector :**

xlfda_numerator('FDATool')

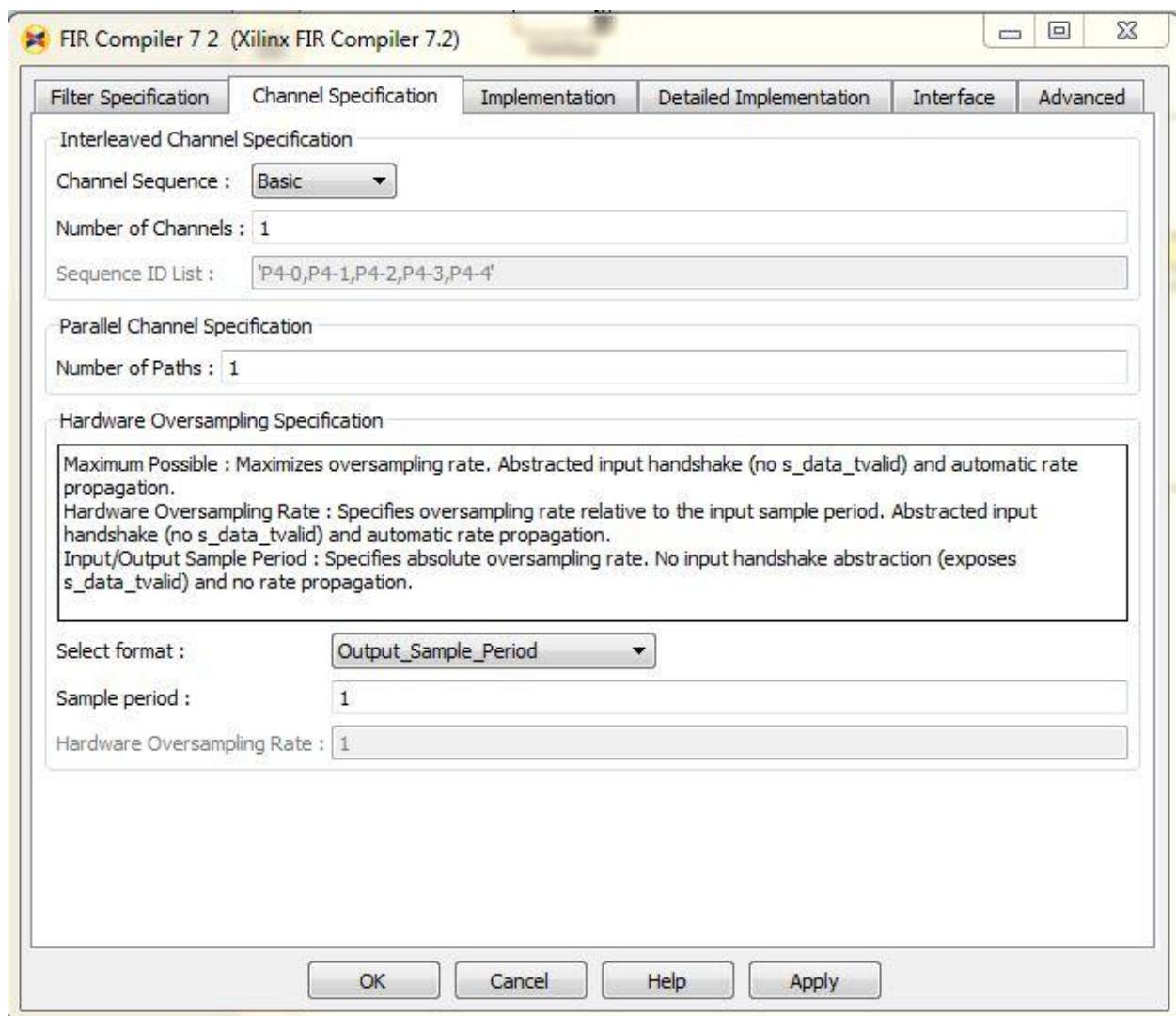
Number of Coefficient Sets : 1 **Use Reloadable Coefficients****Filter Specification****Filter Type :**

Single_Rate ▾

Rate Change Type :

Integer ▾

Interpolation Rate Value : 1**Decimation Rate Value :** 1**Zero Pack Factor :** 1**OK****Cancel****Help****Apply**



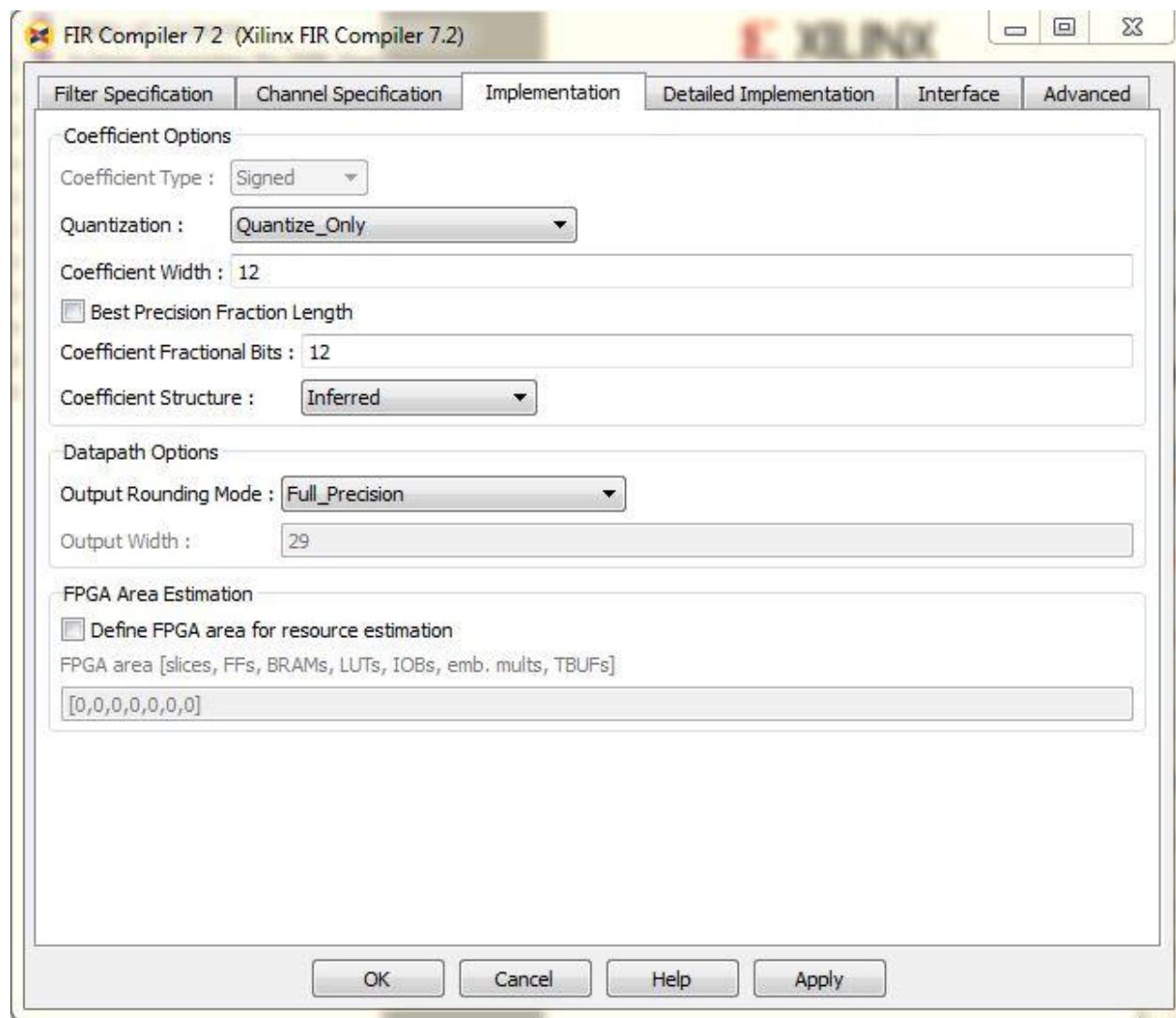


Figure 28: Configuring the FIR Compiler 7.2

Step 10: Final Design

Make the connections to have the final design as shown in figure 29.

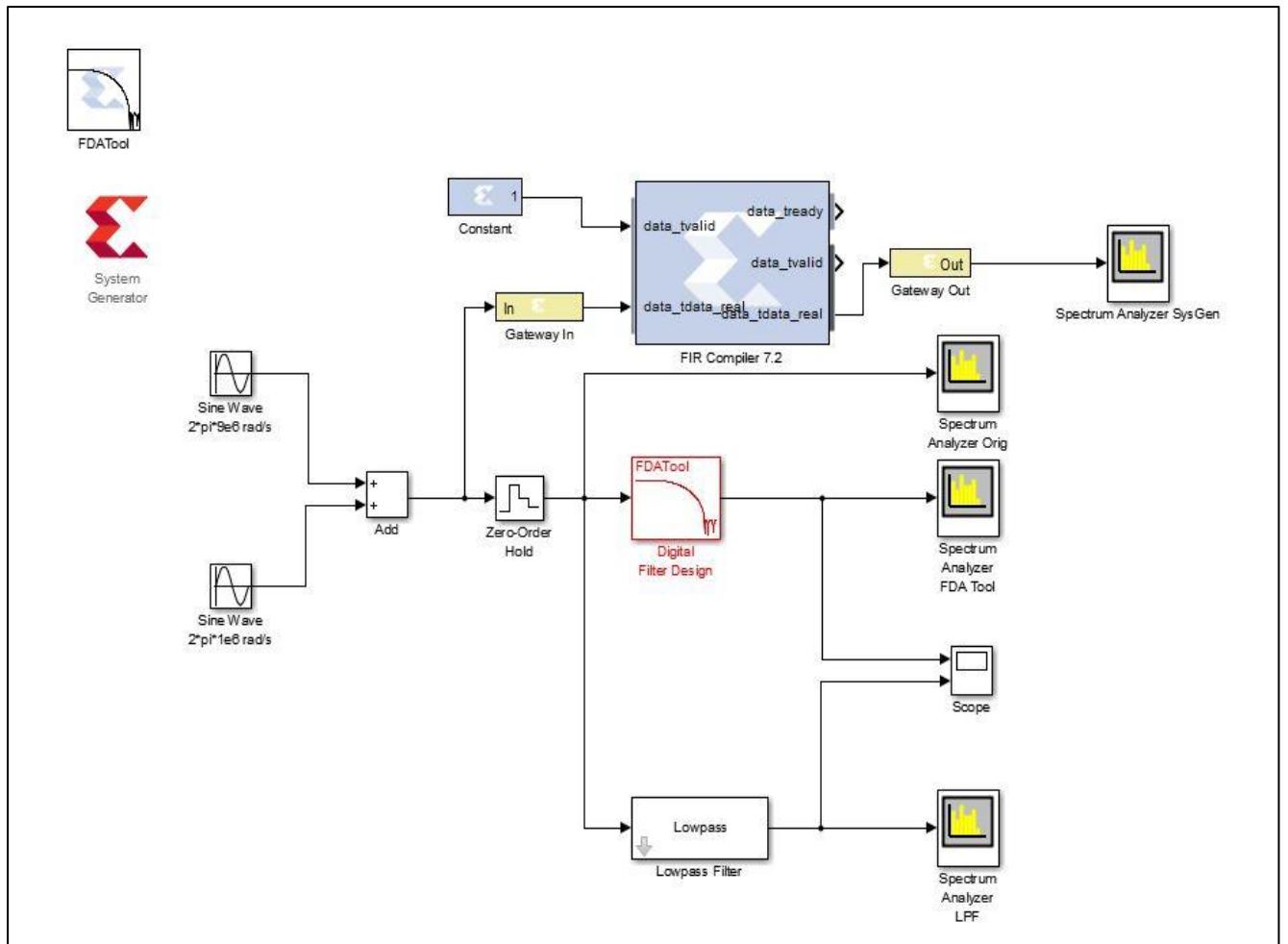


Figure 29: Final Design.

Step 11: Addition of Zedboard

After configuring all the blocks, now we will add the **ZedBoard** by writing following commands in the MATLAB Command Window as shown in figure 30.

Note: If it shows that the file is already present, then delete the file by going to the given path and again run the same command whch prompted the error.

```

Command Window

Warning: Executing startup failed in matlabrc.
This indicates a potentially serious problem in your MATLAB setup, which should be resolved as soon as possible. Error detected was:
MATLAB:noSuchMethodOrField
No appropriate method, property, or field setBoardFileRepos for class xilinx.environment.
> In matlabrc at 192
Type xlDoc to open the Xilinx System Generator help documentation.
Type demo blockset xilinx to view the demos available for Xilinx System Generator.
Tip of the day: Learn more about Adding a custom board for JTAG Co-Simulation.
>> xilinx.environment.addBoard('Zed','c:/Sys1','c://Xilinx/Vivado/2015.4/data/boards/board_parts/zynq/zed/1.2/')
>> xilinx.environment.addBoard('Zedboard','c:/Sys1','c://Xilinx/Vivado/2015.4/data/boards/board_parts/zynq/zed/1.2/')
>> xilinx.environment.rehashCompilationTarget
f >> |

```

Figure 30: Connecting Zed Board with the design.

Step 12: Hardware Generation.

Double-click the **System Generator** token to open the Properties Editor.

- Select **Compilation** tab and change Compilation to **Zed (JTAG)** and make **necessary changes** as shown in figure 31.



Figure 31: Compilation Tab modification.

- Select **Clocking** tab and make necessary changes as shown in the figure 32.

- > Specify an **FPGA clock Period of 50 ns (1/20 MHz)**.
- > Specify a **Simulink system period of 1/20e6 seconds**.



Figure 32: Clocking Tab Modification

c. **General** Tab modifications is shown in the figure 33.



Figure 33: General tab Modifications.

- d. Click OK to exit the System Generator token.
- e. Click **Generate** to compile the design into hardware. After Generation, **Compilation Status** will be prompted as shown in the figure 34.

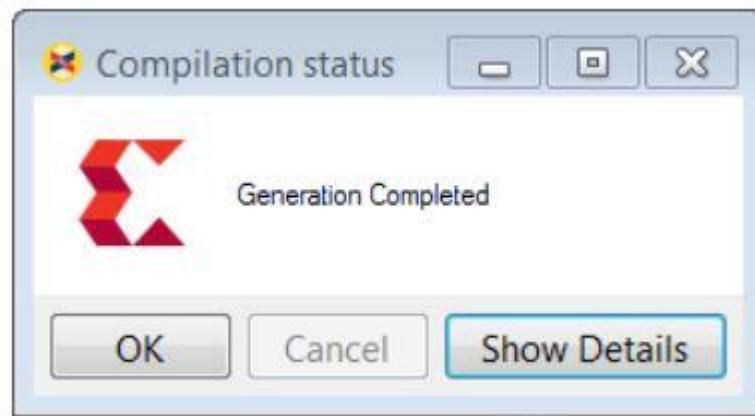


Figure 34: Generation Complete.

Step 13: Configuration of generated hardware

After the completion of generation, a hardware is generated as shown in figure 35.

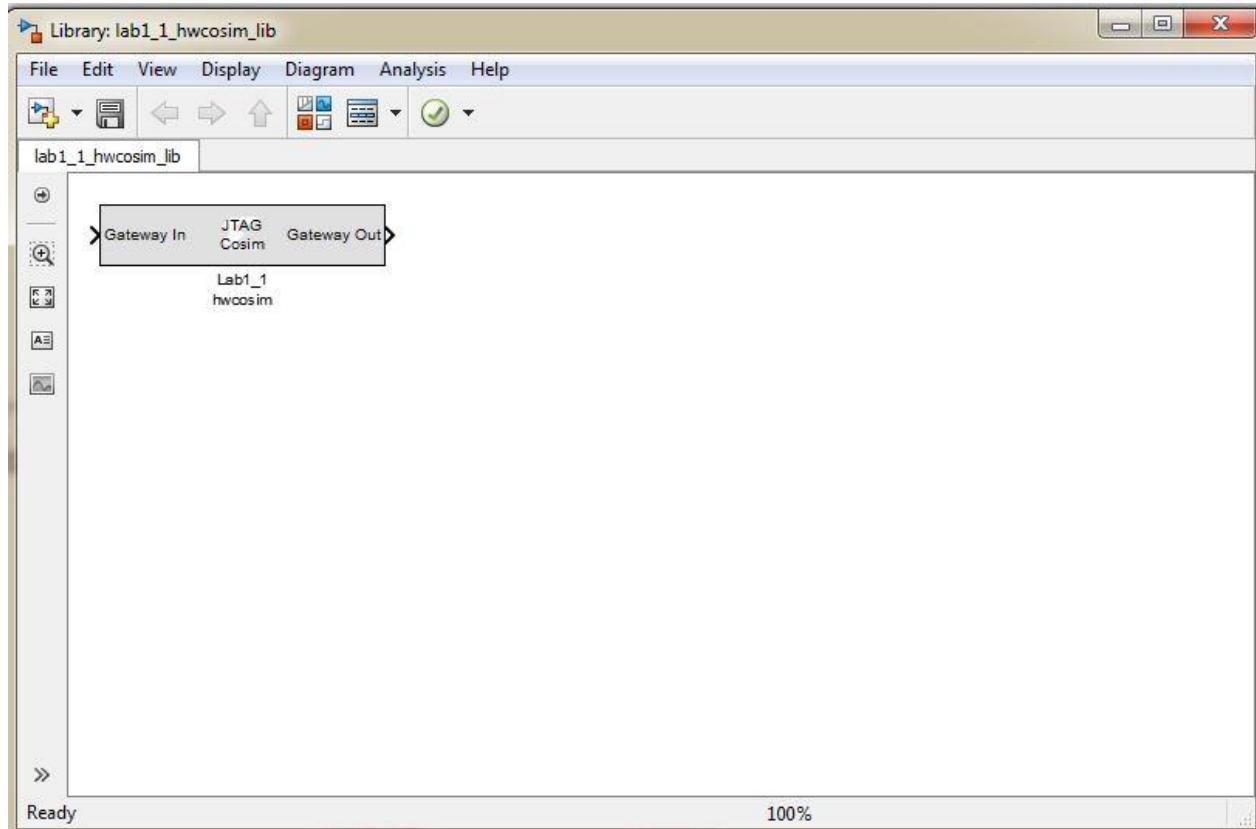


Figure 35: Generated Hardware.

Now we have to modify certain properties of the generated hardware as shown in the



Figure 36: Modification in the hardware generated block.

figure 36, we will uncheck the box associated with **Reset Zynq board before configuration** and rest remains the same.

Step 14: Adding generated hardware to the design

Now, we have to copy this generated hardware to the Lab1_1 and make connection as shown in figure 37.

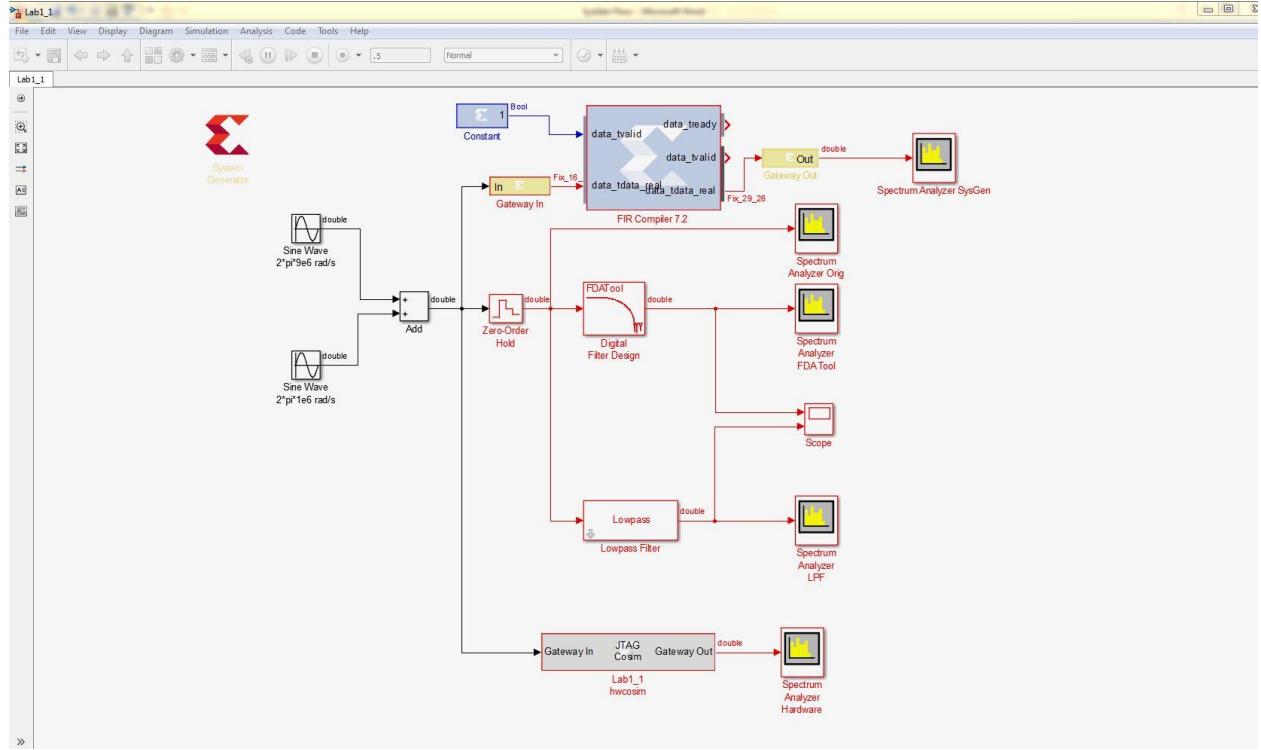


Figure 37: Final Model.

Step 15: Running simulation after addition of generated hardware.

Click the Run simulation button to simulate the design and observe the spectrum obtained at Spectrum Analyzer Hardware. A Blue Led will glow up on the board, which shows the generation of bit file and completion of simulation as shown in the figure 38.

And the Simulated Output is shown in the figure 39.

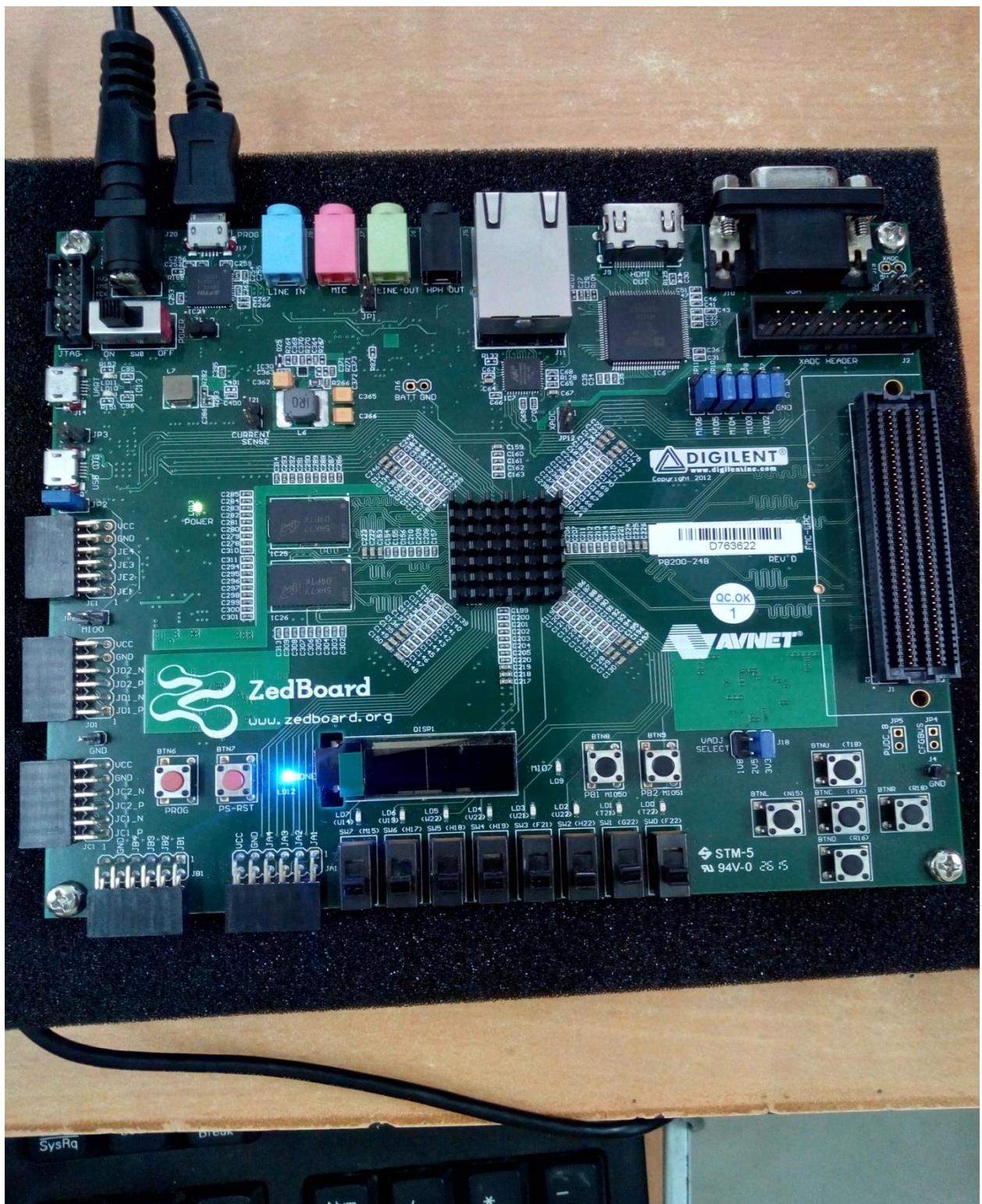


Figure 38: Indication of Bit File Generation and Completion of Simulation.

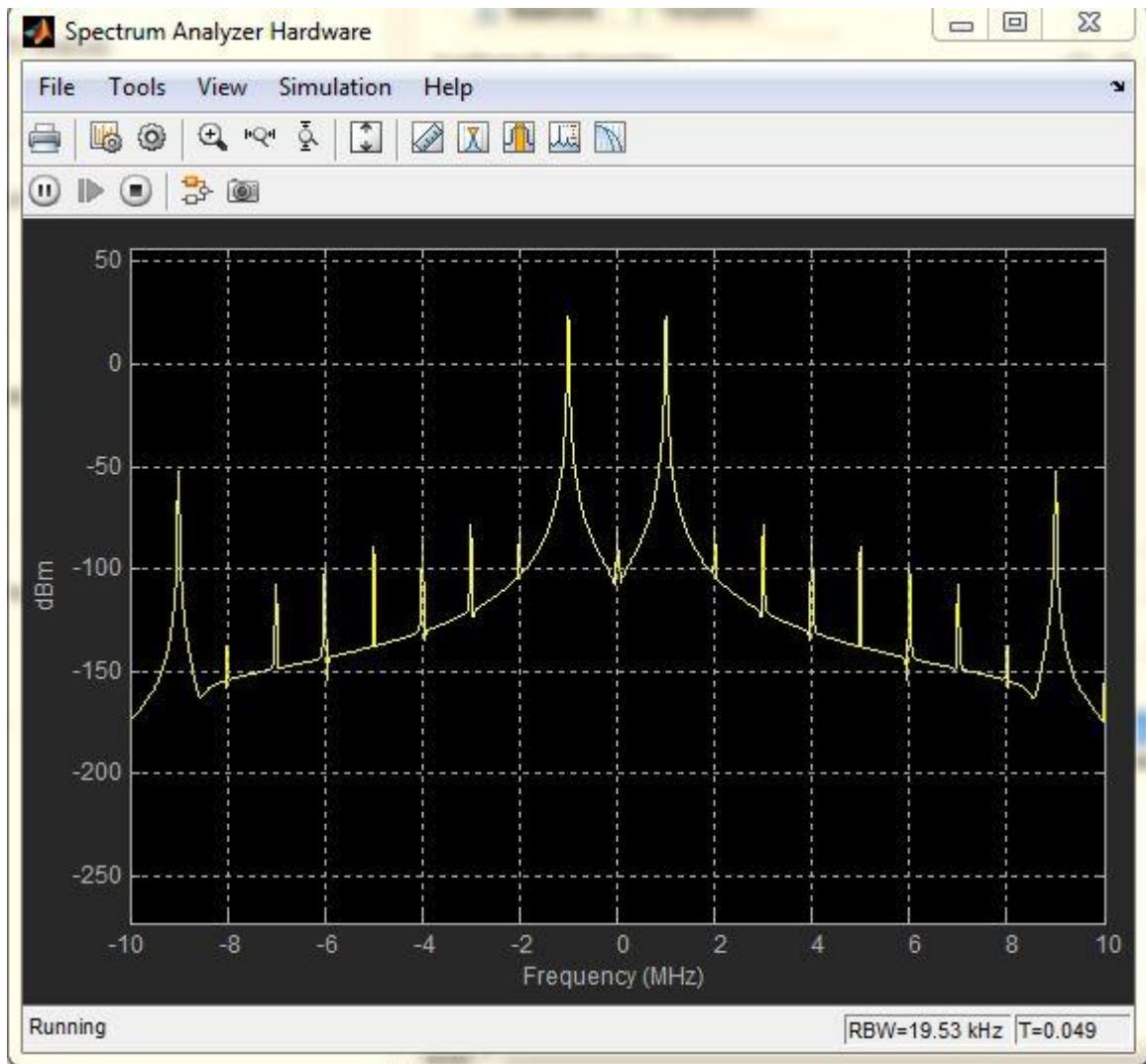


Figure 39: Simulated output shown in Spectrum Analyzer Hardware.

Step 16: Hardware Utilisation using Vivado

Now, we will see the hardware utilization with the help of Vivado.

- a. Open Vivado : Start > All Programs > Xilinx Design tools > Vivado 2015.4 > Vivado 2015.4
- b. Quick Strat > Open Project > Lab1_1 (File Type: Vivado Project File) as shown in figure 40.

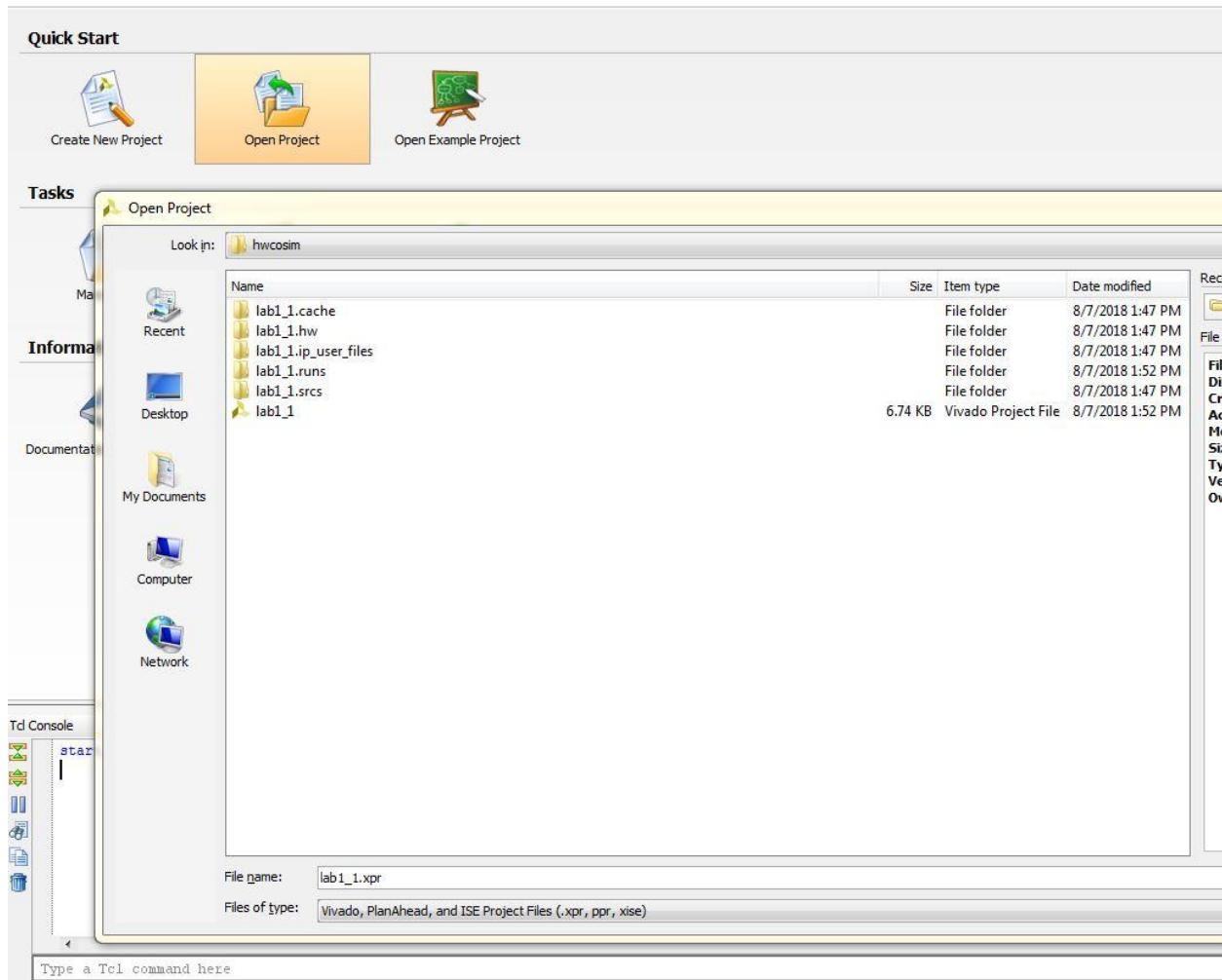


Figure 40: Open Project in Vivado.

c. Now, Run Synthesis as shown in figure 41, and wait till its completion.



Figure 41: Run Synthesis using Vivado

- d. After the Completion of synthesis a prompt will come where we have to select *Open Synthesized Design* as shown in the figure 42.

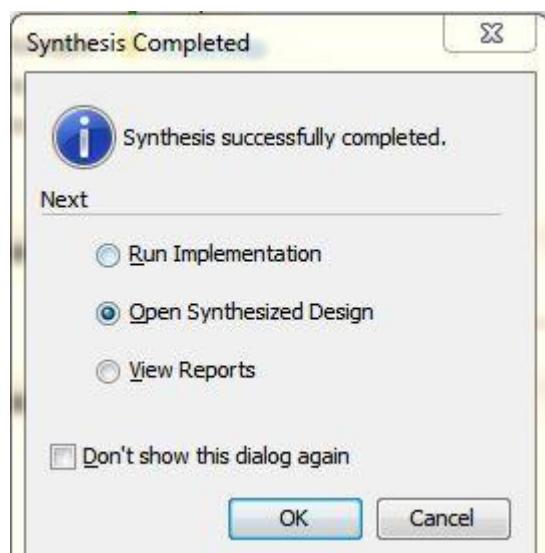


Figure 42: Synthesis Completed.

- e. We can see **Hardware Utilization** post synthesis in both Graphical and Tabular form as shown in figure 43 and 44 respectively.

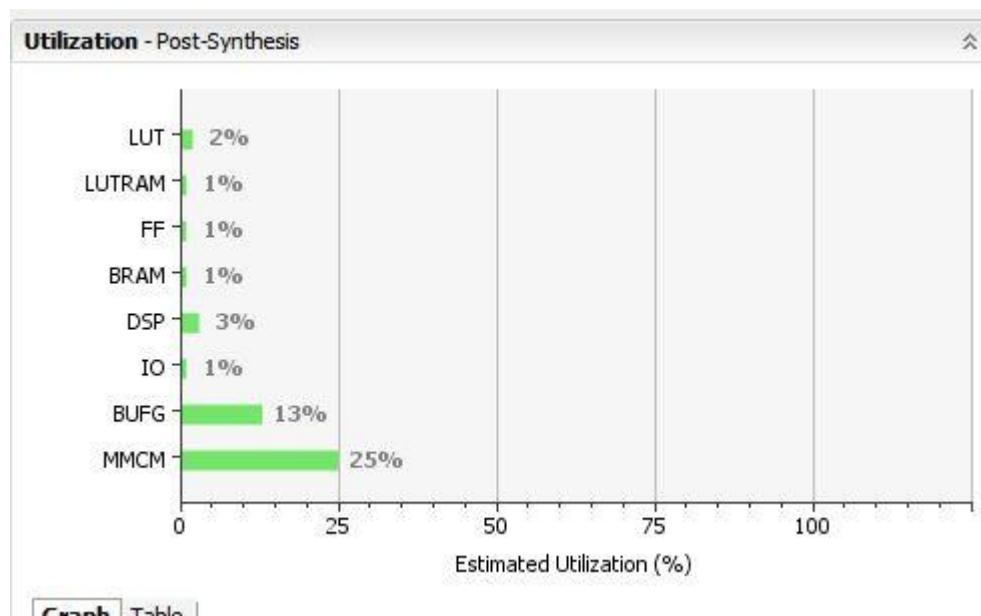


Figure 43: Hardware Utilization: Graphical Form

Utilization - Post-Synthesis				
Resource	Estimation	Available	Utilization %	
LUT	942	53200	1.77	
LUTRAM	162	17400	0.93	
FF	1283	106400	1.21	
BRAM	2	140	1.43	
DSP	6	220	2.73	
IO	1	200	0.50	
BUFG	4	32	12.50	
MMCM	1	4	25.00	

Figure 44: Hardware Utilization: Tabular Form.

The full flow of Lab1 is now completed. We can observe various other results as per our requirement.

In this lab, we have learned how to take different blocks from Simulink Library, Configuration of each block, connecting the blocks, SysGen Implementation, use of Zed board and also how to generate hardware utilization post synthesis.

Assignment Time!!!!!!

Assignment

Draw the following design as shown in the figure 45 from scratch and **compare the outputs** of **Spectrum Analyzer Digital Filter** and **Spectrum Analyzer SysGen**.

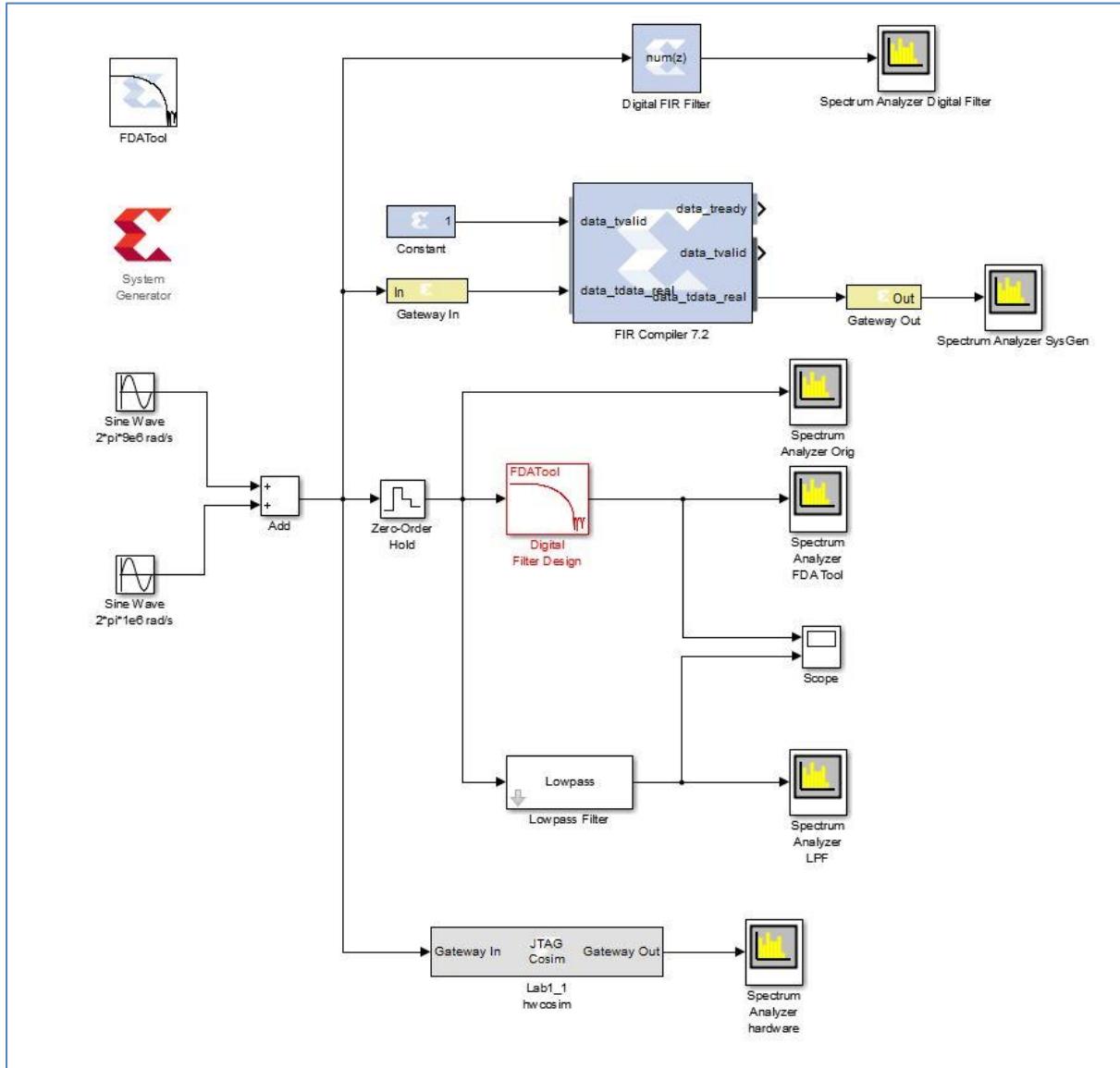


Figure 45: Assignment Model Design.

Hint: Export the coefficients of FDATool having variable name Num, and some modification in Digital FIR Filter may be needed.