Systolic Asymmetric Architecture

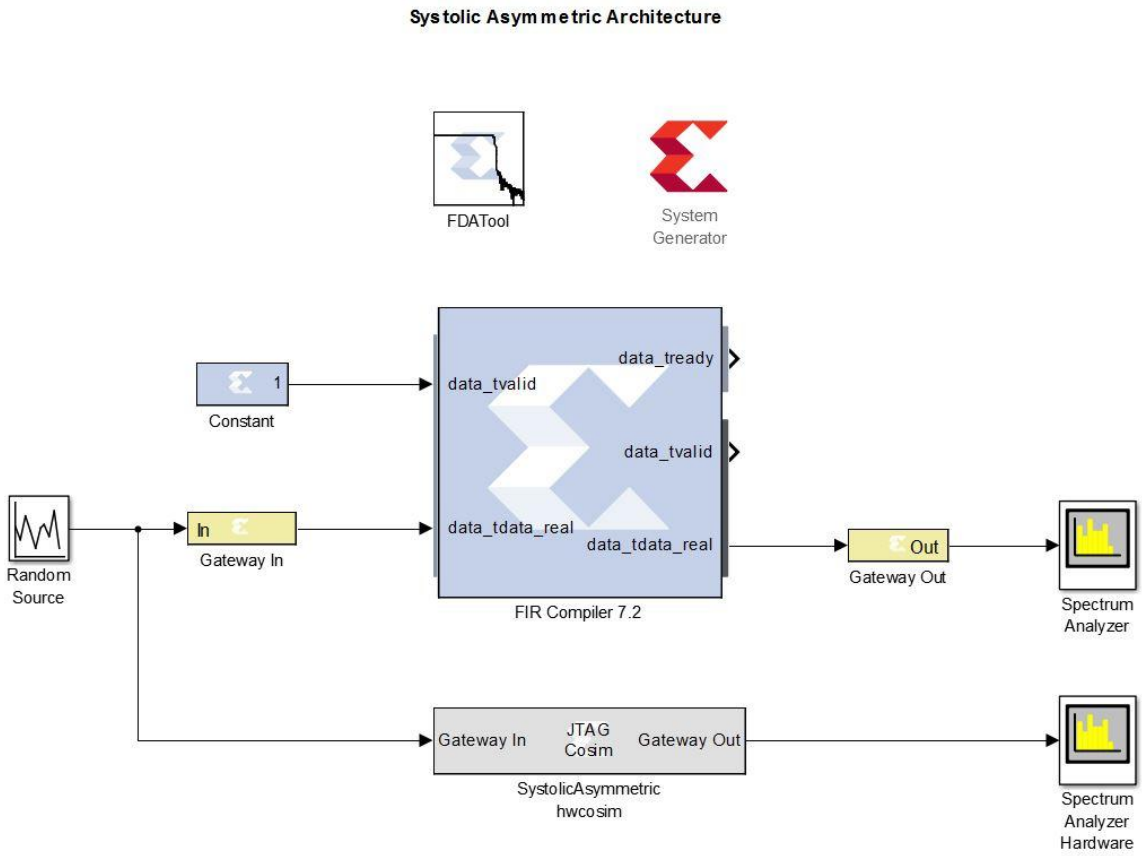


Figure 1: Systolic Asymmetric Architecture Design

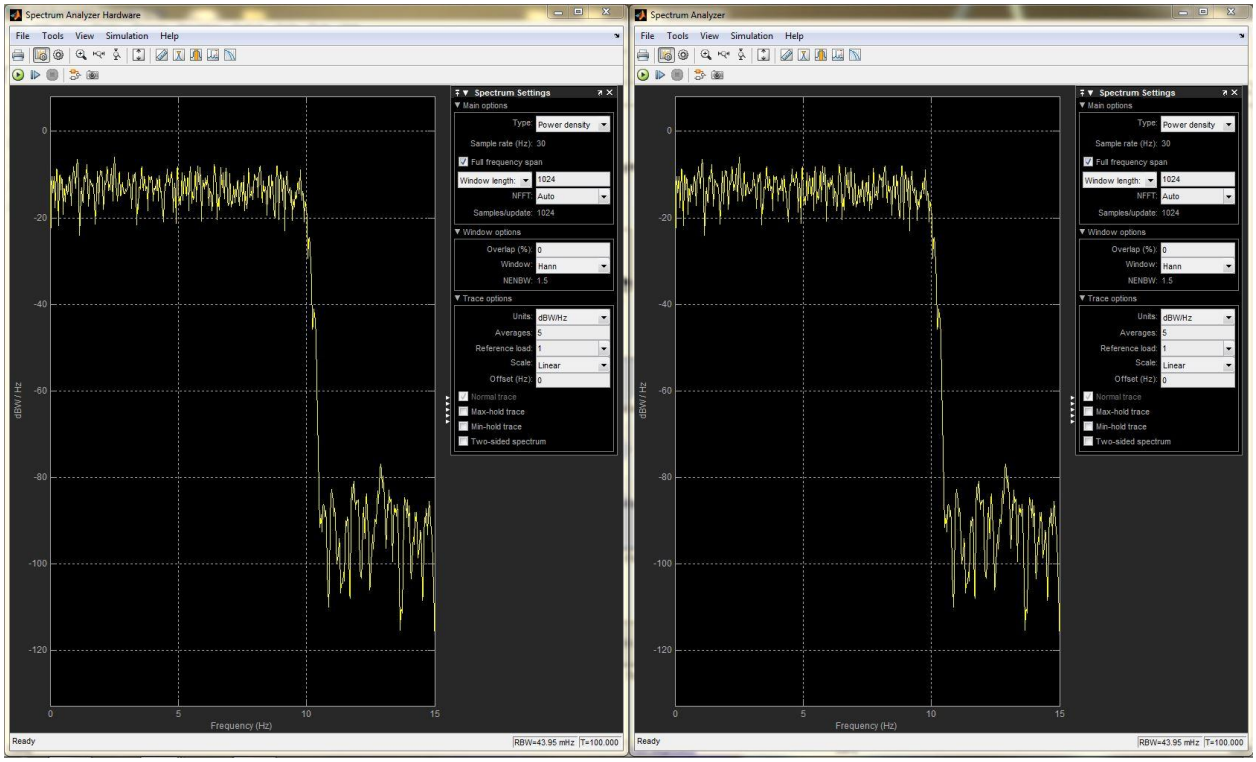


Figure 2: Frequency Response Comparison

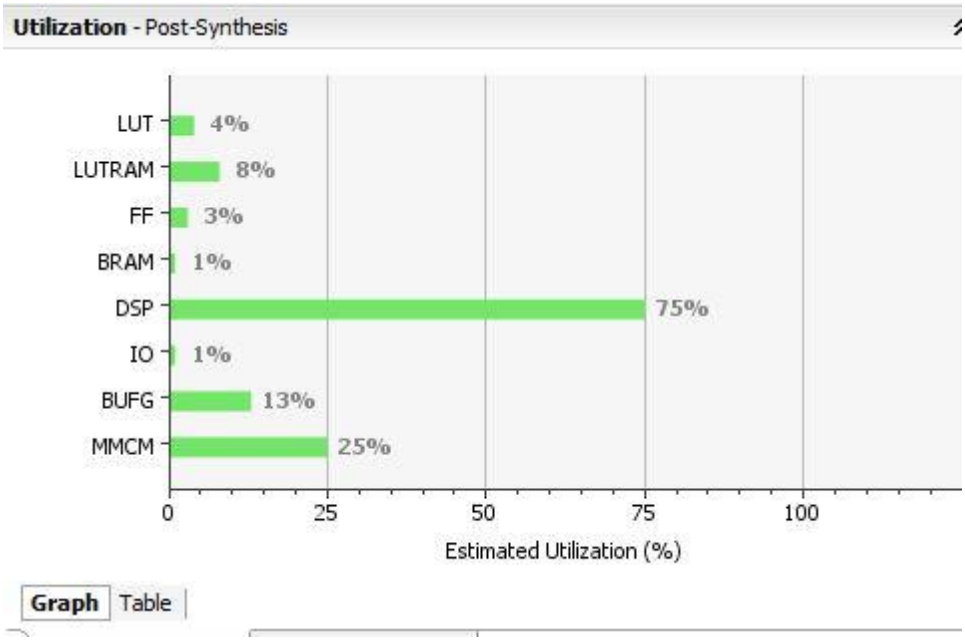
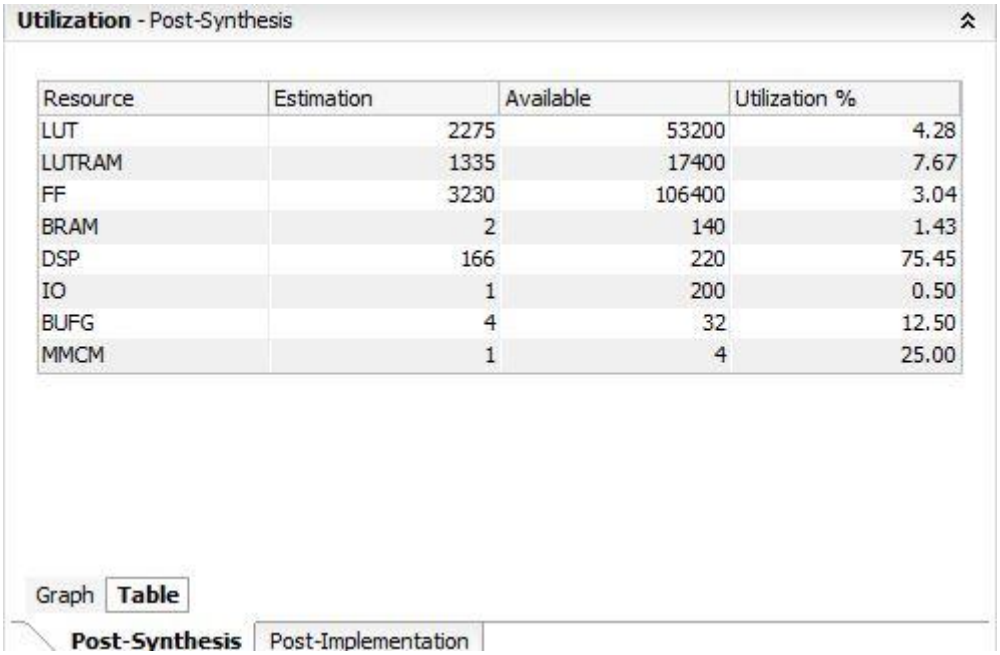
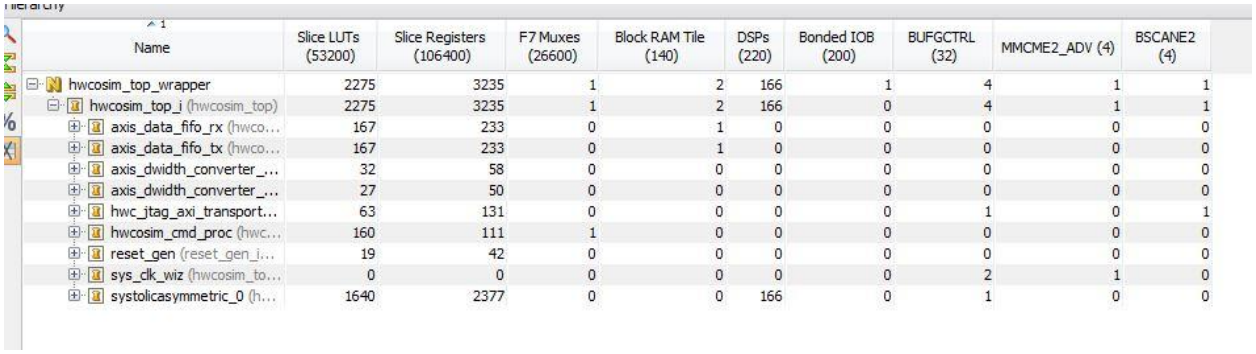


Figure 3: Post Synthesis Hardware Utilization Report(Graph)



Resource	Estimation	Available	Utilization %
LUT	2275	53200	4.28
LUTRAM	1335	17400	7.67
FF	3230	106400	3.04
BRAM	2	140	1.43
DSP	166	220	75.45
IO	1	200	0.50
BUFG	4	32	12.50
MMCM	1	4	25.00

Figure 4: Post Synthesis Hardware Utilization Report(Table)



Name	Slice LUTs (53200)	Slice Registers (106400)	F7 Muxes (26600)	Block RAM Tile (140)	DSPs (220)	Bonded IOB (200)	BUFGCTRL (32)	MMCME2_ADV (4)	BSCANE2 (4)
hwcosim_top_wrapper	2275	3235	1	2	166	1	4	1	1
hwcosim_top_i (hwcosim_top)	2275	3235	1	2	166	0	4	1	1
axis_data_fifo_rx (hwco…	167	233	0	1	0	0	0	0	0
axis_data_fifo_tx (hwco…	167	233	0	1	0	0	0	0	0
axis_dwidth_converter_…	32	58	0	0	0	0	0	0	0
axis_dwidth_converter_…	27	50	0	0	0	0	0	0	0
hwc_jtag_axi_transport…	63	131	0	0	0	0	1	0	1
hwcosim_cmd_proc (hwc…	160	111	1	0	0	0	0	0	0
reset_gen (reset_gen_i…	19	42	0	0	0	0	0	0	0
sys_clk_wiz (hwcosim_to…	0	0	0	0	0	0	2	1	0
systolicasymmetric_0 (h…	1640	2377	0	0	166	0	1	0	0

Figure 5: Hardware Utilization Report