

Instruction Set -inkorrekt

16 bit emulator

Gustaf Franzén och Adam Månsson

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Specifikationer

Generella

16-bitars little-endian cpu
32-bitars-address bus
4-Mb ram från address $0x00000000 - 0x003FFFFF$
4-Gb rom från $0x003FFFFF - 0xFFFFFFFF$
16-bit IO controller

Register

10 16-bitars register $r0 - r9$
10 8-bitars register $b0 - b9$ som motsvarar de minst signifikanta bitarna i motsvarande 16 bitars register
16-bitars Stack pointer register sp
16-bitars Status register sr
32-bitars program-counter register pc
r16 refererar till ett 16-bitars register ($r0-r9 - sp$), r8 ett 8-bitars

Addressing-modes

processorn stödjer 8 sätt att accessa minne från 32-bitars bussen. i Direkt adressering specificeras en address direkt medans i indirekt adressering specificeras en address där den direkta adressen ligger. Absolut adressering menas att hela 32-bitars adressen är specificerad medans med zeropage addressing specificeras endast en 16-bitars adress, därför kommer man endast åt de första 2^{16} adresserna

| type | description |
|------------|---|
| r16 | 16-bit register (r0-r9 — sp) |
| r8 | 8-bit register b0-b9 |
| im16 | 16-bit immediate value |
| im32 | 32-bit immediate value |
| [value]:8 | the 8-bit stored at value |
| [value]:16 | the 16-bit value stored at value |
| [value]:32 | the 32-bit value stored at value |

Table 1: H:r16, L:r16

Direct Absolute

| abs | direct | |
|------|---------------------------|---------------------------|
| args | $\langle H : r16 \rangle$ | $\langle L : r16 \rangle$ |

In Direct Absolute addressing the absolute address is formed by combining two registers to form a 32 bit address

syntax exaple to load r2 from address 0xABCD1234:

| | |
|---|-----------------|
| 1 | mov r0, #0xABCD |
| 2 | mov r1, #0x1234 |
| 3 | ldr r2, r0, r1 |

Direct Absolute Immediate

| abs | direct |
|------|----------------------------|
| args | $\langle V : im32 \rangle$ |

In Direct Absolute Immediate addressing the absolute address is supplied as a 32 bit immediate value

syntax exaple to load r2 from address 0xABCD1234:

| | |
|---|---------------------|
| 1 | ldr r2, #0xABCD1234 |
|---|---------------------|

Direct Zeropage

| abs | direct | |
|------|--------------------------|---------------------------|
| args | $\langle 0x0000 \rangle$ | $\langle Z : r16 \rangle$ |

Direct Zeropage addressing the absolute address is supplied as a 16-bit register and padded with 0s

syntax exaple to load r1 from address 0x1234:

```

1      mov r0, #1234
2      ldr r1, r0

```

Direct Zeropage Immidiate-offset

| abs | direct | |
|------|----------|---------------------------|
| args | <0x0000> | <R : r16> + <O : im16> |

Direct Zeropage Immidiate-offset addressing the absolute address is formed by a 16-bit register added with a immidiate offset, and padded with 0s

syntax exaple to load r1 from address 0x1235:

```

1      mov r0, #1234
2      ldr r1, r0, #1

```

Inderect Absolute Immidiate

| | |
|------|----------------------|
| abs | direct=[inderect]:32 |
| abs | inderect |
| args | <V : im32> |

Table 2: V:im32

Inderect Absolute Immidiate addressing the absolute address is read from the supplied address

syntax exaple to load r1 with 10 from address(0x00FF0000) stored at 0x1235

```

1      mov r0, #10
2      str r0, #0x00FF0000
3
4      mov r0, #0x0000
5      mov r1, #0x00FF
6
7      str r0, #0x00001235
8      str r1, #0x00001235 + #1 ; store in little
      endian

```

| | |
|----|-----------------------|
| 9 | |
| 10 | ldr r1, [#0x00001235] |