Characteristic description

TM1680 is a memory switching LED display control driver chip with multiple ROW/COM modes (32ROW/8COM 和 24ROW/16COM) that can be used to drive dot matrix LEDs. The chip provides software-set levels of pulse width modulation control output, 16
You can adjust the brightness of the LED loop display. By using serial interface (communication interface) serial input, you can easily access the command I2C
mode （MAND MDOE) and data modes DATA MODE require a simple command to set up the master chip and TM1680 of communication. Pass TM1680 Continuous output display can be performed, LED lamp display has wide application, 如 Industrial instrument control digital clock thermometer counter voltmeter display, meter data readout, LED display, smart bracelet and other applications. Ben Excellent performance and reliable quality.

Features of the function

- Working voltage 2.4～5.5V
- 32ROW*8COM 和 24ROW*16COM Two display schemes are available
- Integrated Display Memory —64*4 Display RAM （32ROW*8COM), which displays the RAM （24ROW*16COM ） 96*4
- 16 Level Pulse Width Modulation Controls Brightness
- Built-in 256kHz RC oscillator
- Interface (SDA、SCL) communication I2C
- Data mode and command mode instructions
- Optional NMOS output channels and PMOS output channels 编辑
- Package form: LQFP48 、LQFP52

Frame diagram of the internal structure

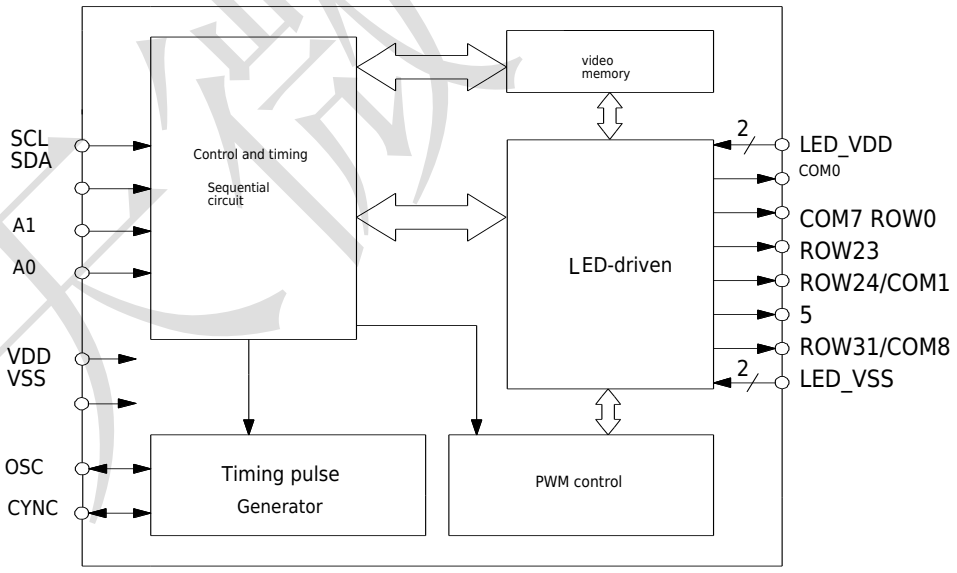


图1

Pipe arrangement

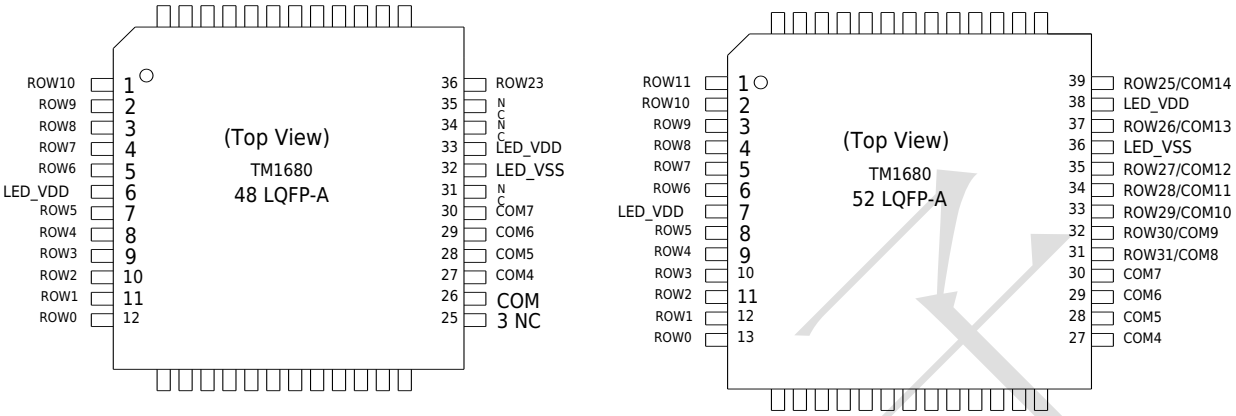


图2

Pin Function

Pin Name	Pin serial number	I/O	Description of the function
VDD	21	-	Chip Logic Power Supply Positive
VSS	14	-	Chip Logic Power Supply Negode
LED_VDD	7/38	-	LED Driver Power Supply Positive Recommendation VDD，接
LED_VSS	25/36	-	LED driver power supply negative, VSS is recommended
ROW0 ～ROW23	1～6/8～13/41～52	O	LED line drive output
ROW24/COM15 ～ROW31/COM8	31～35/37/39/40	O	LED line drive output or common input端
COM0 ～COM7	22～24/26～30	O	LED Common Input端
SYNC	20	I/O	If the main trigger mode or the external extended trigger mode is selected, the sync signal will be removed from the SYNC pin output; if passive mode is selected, the synchronization signal will be input from the SYNC pin.
OSC	15	I/O	When RC oscillation main trigger mode is selected, the system clock is generated by on-chip RC oscillation and is removed from the OSC pin output; if passive mode or external expansion trigger mode is selected, the system clock is controlled by the OSC foot input from outside.
A0	19	I	Slater address expansion bit, built-in pull-up resistor.
A1	18	I	Slater address expansion bit, built-in pull-up resistor.
SCL	17	I	I2C Communication clock input, data on the SDA line is written into the TM1680 ， Built-in pull-up resistor.
SDA	16	I/O	I2C Communication data input and output ports require an external pull-up resistor for application.

＊备 Note: The serial number of the pins in the table above, with LQFP52 Encapsulation as an example. Different packages, feet are different, please refer to the pin for details Arrange diagram. 48PIN Encapsulation is displayed only by 24*8。

Input Output Equivalents

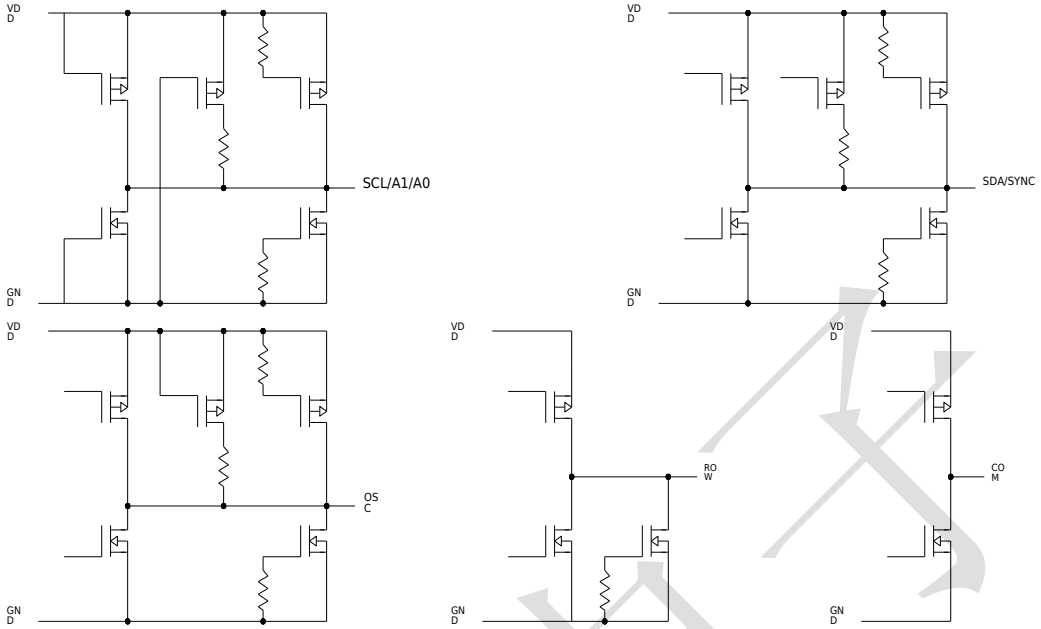


图3

Integrated circuit system electrostatic sensitive device, easy to use in the dry season or dry environment to generate a large amount of static electricity, electrostatic discharge can be

Can damage the integrated circuit, we recommend taking all appropriate IC preventive measures, improper operation Welding, may cause ESD damage or performance degradation, the chip does not work properly.

limit parameter)(1)(2)

Parameter Name		Parameter Symbols	Limit value	单位
Logic Supply Voltage		VDD	VSS -0.3V ～ VSS+6V	V
Voltage Range at Input	SDA, SCL, OSC, SYNC	Vin	VSS-0.3 ～ VDD+0.3	V
Working temperature range		Topt	-40～+85	°C
Storage temperature range		Tstg	-55～+125	°C

(1) chip operating for a long time under the above limit parameters, may cause loss of device reliability or permanent damage, day microelectronics

It is not recommended that any of these limits be reached or exceeded when used.

(2) all voltage values are systematically tested relative to.

Recommended working conditions

Parameter Name	Parameter Symbol	Minimum	Typical	Maximum	
Working voltage	VDD	2.4	5.0	5.5	V
Input Low Voltage	Vil	0	-	0.3 VDD	V
Input High Voltage	Vih	0.7VDD	-	5	V

DC electrical characteristics

在 VDD= 2.4 ~ 5.5V 及 TA=+25 °C test, unless otherwise stated				TM1680			units
Parameter Name	Parameter symbol	VDD	Test Condition	Minimum	Typical	Maximum	
Working Current	IDD	5.0V	On-chip RC, no load, open display		0.3	0.6	mA
Standby Current	ISTB	5.0V	Power saving mode, no load		0.1	10	μA
OSC, SYNC, SDA Sink Current	IOL1	5.0V	Vol=0.5V	18	25	-	mA
OSC, SYNC, SDA Pull Current	IOH1	5.0V	Voh = 4.5 V	- 10	- 13	-	mA
ROW Sink Current	IOL2	5.0V	Vol=0.5V	12	16	-	mA
ROW pull current	IOH2	5.0V	Voh = 4.5 V	- 50	- 70	-	mA
COM sink current	IOL3	5.0V	Vol=0.5V	250	350	-	mA
COM pull current	IOH3	5.0V	Voh = 4.5 V	- 45	- 60	-	mA
pull-up resistance	Rph	5.0V	SDA, SCL, OSC, SYNC	18	27	40	kΩ

Switches Features

Test at operating temperature at 25°C, unless otherwise stated			VDD=2.4 V ~5.5V		VDD=3.0V ~5.5V		units
Parameter Name	Parameter Symbols	Test Conditions	Minimum	maximum	maximum	maximum	
Clock Frequency	FSCL	Chip Internal Clock	-	100	-	400	kHz
Bus idle time	TBUF	Bus at the next time 钟到来之前的空闲时间	4.7	-	1.3	-	μs
Start Signal Hold Time	THD: STA	-	4	-	0.6	-	μs
SCL Low Time	TLOW	-	4.7	-	1.3	-	μs
SCL High Time	Thigh	-	4	-	0.6	-	μs
Start Signal Set Time	TSU: STA	-	4.7	-	0.6	-	μs
Data retention time	THD: DAT	-	0	-	0	-	μs
Data creation time	TSU: DAT	-	250	-	100	-	ns
SDA/SCL Rise Time	tr	-	-	1	-	0.3	μs
SDA/SCL Drop Time	tf	-	-	0.3	-	0.3	μs
Stop signal set up time	TSU: STO	-	4	-	0.6	-	μs
Denoising at SDA/SCL Input Time	TSP	Denoising Time	-	20	-	20	ns

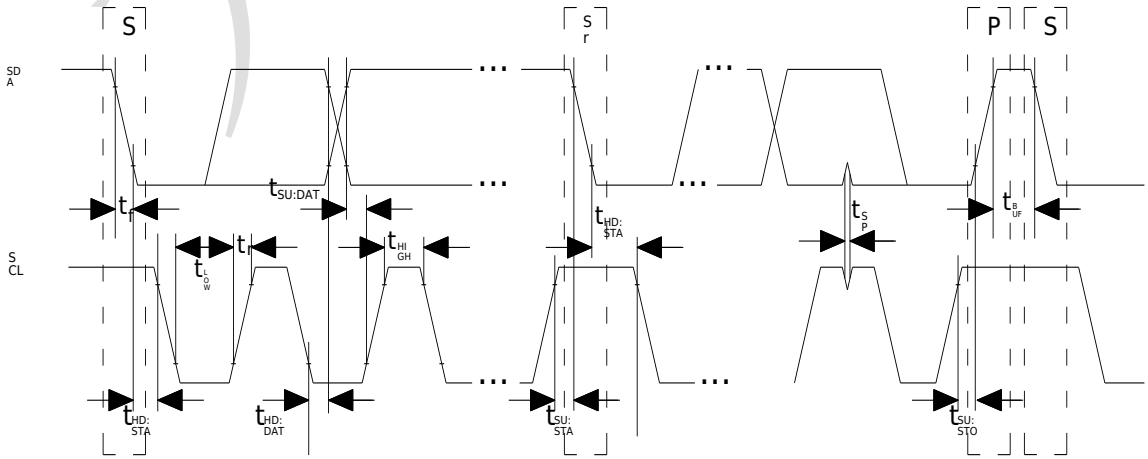


图 4

Description of the function

1 Display memory (RAM)

Static display memory contains 64*4Bit and 96*4 bit formats to store the data you need to display. If the pattern 32ROW/8COM mode is used by the , the storage space of RAM 64*4 bit; if the pattern 24ROW/16COM mode is selected, the RAM storage space is 96*4 bit. RAM directly to the LED display drive and the LED will be lit if the RAM data is set to "". The following figure Out is a map of the RAM LED:

	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0	
ROW0					01H					00h
ROW1					03H					02H
					3FH					3EH
	D3	D2	D1	D0	Addr / Data	D3	D2	D1	D0	Addr / Data

32 ROW & 8 COM for 64 × 4 Display RAM

图5

	COM15	COM14	COM13	COM12		…	COM3	COM2	COM1	COM0	
ROW0					03H	…					00h
ROW1					07H	…					04H
						…					
ROW24					5FH	…					5CH
	D3	D2	D1	D0	Addr / Data		D3	D2	D1	D0	Addr / Data

24 ROW & 16 COM for 96 × 4 Display RAM

图6

2 System clock

TM1680 is used to generate the clock frequency at which the system operates. LED driver clock, system clock can be taken from on-chip RC Oscillators (256kHz) or an external clock input using S/W settings. The system oscillator is constructed as shown when the SYS DIS command is

When executed, the system clock stops and the LED loop is closed (this instruction can only be used with the on-chip RC oscillator). Once the system is When the clock stops, the LED appears blank and the timebase loses its function. LED_OFF command is used to turn off the LED working cycle, LED working After the loop is closed, use the SYS DIS command to save power costs and act as a power-saving command; if an off-chip clock source is selected, It is not possible to turn off the oscillator and perform power-saving mode using the SYS DIS command. Crystal oscillator can provide clock frequency via OSC pin rate, in which case the system will not be able to enter power-saving mode. When the system is powered on, it is in the SYS DIS state by default.

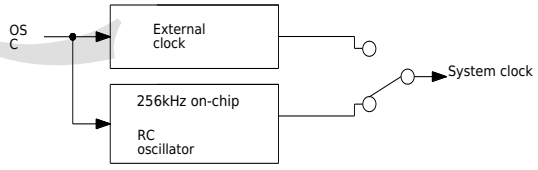


图7

3 LED driver

TM1680 Contains 256（32*8）and 384（24*16) two modes of LED drive, which can be set to or 32*8 24*16 显

The mode allows you to select MOS or MOS output channels via the COM port output. These features make it possible to adapt TM1680 different

的LED applications. The LED driver clock is derived from the system clock. The clock is usually driven by an on-chip RC oscillator or 256kHz

Extended external oscillator. See the command overview table for detailed setup commands.

4 Cascade operation

When cascading operations, the first chip in the cascade is set to host mode with the pin SYNC OSC used as output; the second chip in the cascade chip is set to slave mode, its pin SYNC OSC 都used as input and is connected to the SYNC OSC 脚 of the host chip. The device of the TM1680

Address contains bits external address selection bits 2 A1 、 A0 , so you can connect up to 4个TM1680 to the same bus. Please refer to Cascade for detailed settings

Application circuit diagram. A1 \ A0 Built-in pull-up resistor, when driving the chip separately, the A1 \ A0 可Hanging, at this point TM1680 address of the slave为0xe7。

5 LED drive mode output waveform

32×8 N MOS open-drain output drive mode output waveform is shown below (Tclk=1/Fsys):

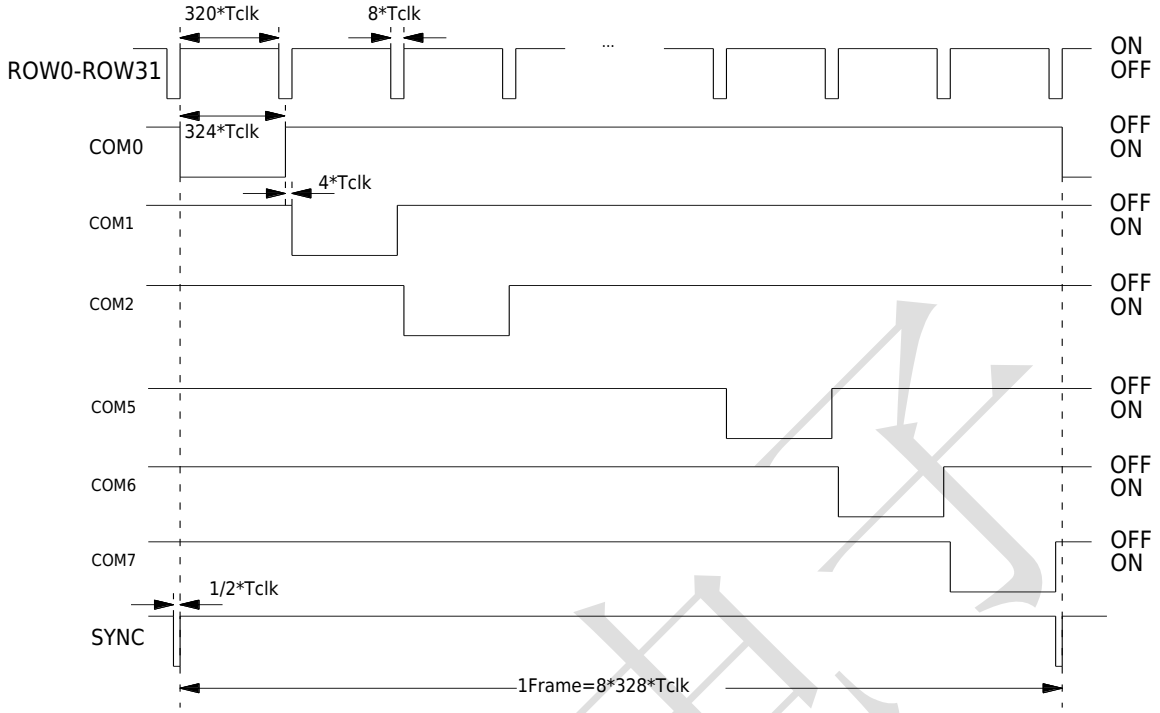


图9

24×16 P MOS open-drain output drive mode (Tclk=1/Fsys COM pin plus transistor)：

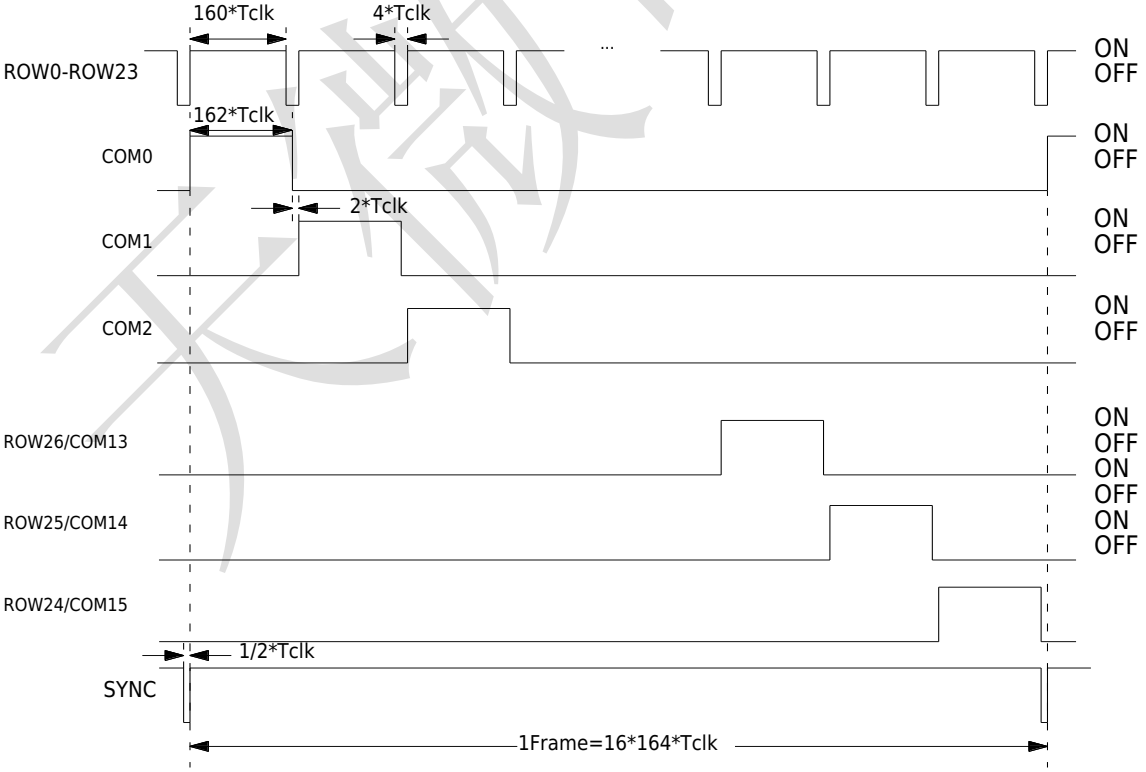


图 10

6 Flash

TM1680 Flicker function allows all LEDs to flicker at a certain frequency. The flicker rate can be set via the Blink command.

to be divided into 2 Hz/1 Hz/0.5 Hz ... The following is the output waveform for the flicker frequency: 2Hz

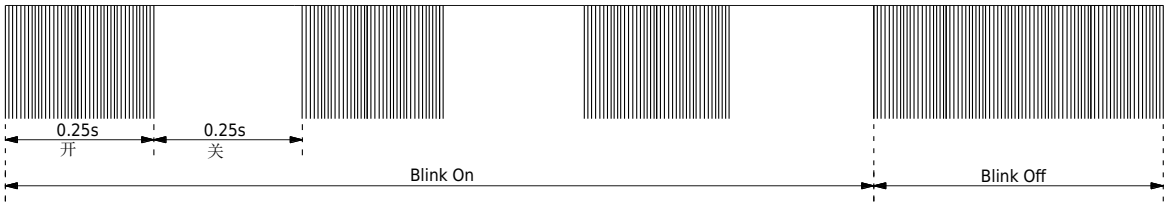


图8

7 Brightness adjustment settings

TM1680 Various brightness control can be performed by setting the PWM drive pulse width at the ROW end. The following figure shows COM under different duty cycle conditions

Output waveform at ROW: (1) T=20×Tclk (32 drive mode (2) T=10 Tclk (24 drive mode)) ; 11 和

(3) Tclk = 1/Fsys

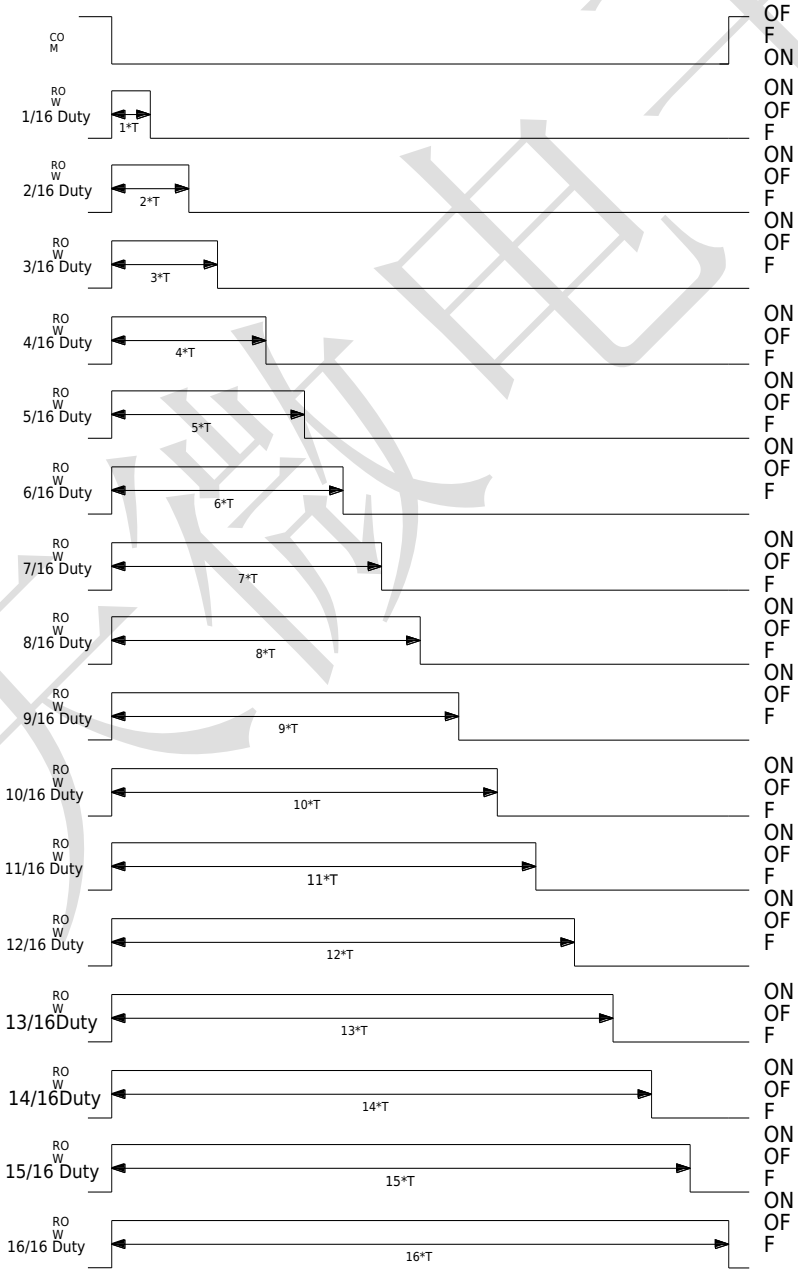


图11

8 Command Format

This chip must follow these steps when entering commands or displaying data:

（1) form the starting condition) to
（2send slave address (Slave Address))
（3command that displays the transfer
（4of data) to form a stop condition

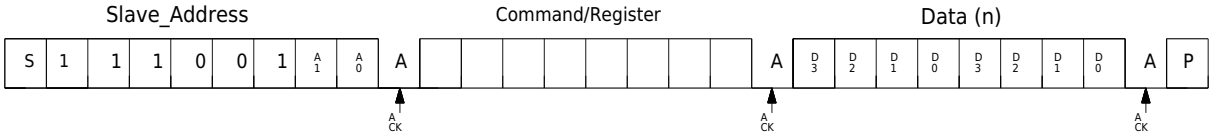


图12

9 I2C Serial interface

This chip is created by the I2C protocol 2 line serial interface for data transfer, contains a serial data line SDA and clock line SCL, within two lines The pull-up resistor is high when the bus is idle.

A starting signal is generated by the controller for each data transfer, data is transmitted in synchronous TM1680 with one byte per received After all responded to an ACK answer signal. Each byte sent to the SDA line must be bit and the number of bytes that can be sent per transfer 8

No restrictions. Each byte must be followed by an ACK response signal, from the first signal 8 descending edge of the 9 SCL signal when the ACK signal is not needed Low "" is required until the first signal descending edge. When data is transmitted from the highest bit, the controller generates a stop signal by to terminate the bus transfer, while the start signal is resent during data transmission without a stop signal.

当Data on the SDA remains stable when SCL is HIGH; SDA changes are allowed when SCL is LOW. If SCL is high, the

A descending edge is generated on the SDA, and a rising edge on the SDA is considered a stop signal if the SCL is high. As shown in the figure below:

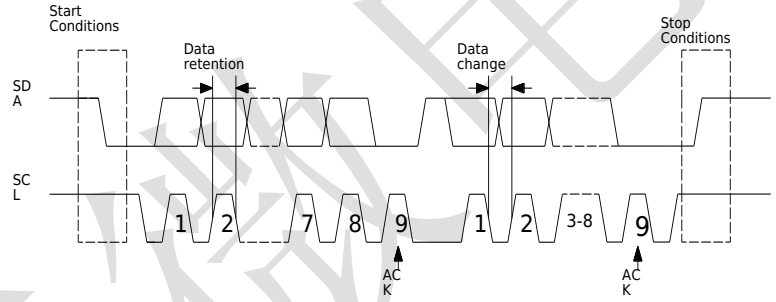


图13

Time sequence graph

1 写命令操作

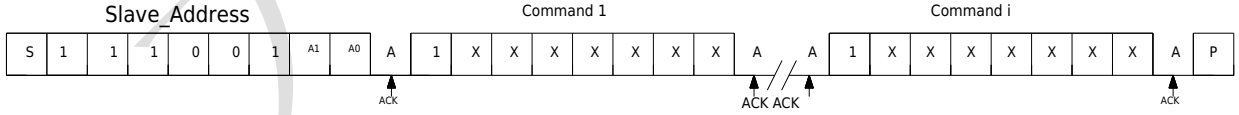


图14

As shown, the bit of the slave device is fixed from the high bit of the address byte, and the next 2 位 A1 、 A0 for the ground outside of the device Address.

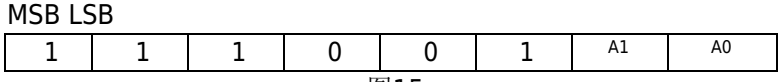


图15

2 Byte-write operations

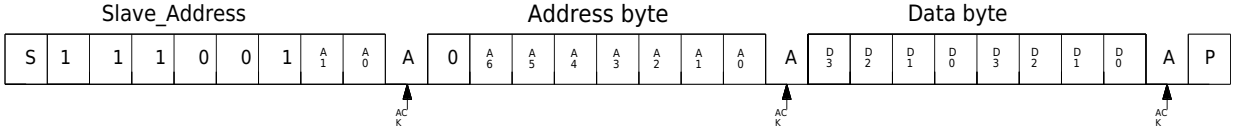


图16

3 Page writing operations

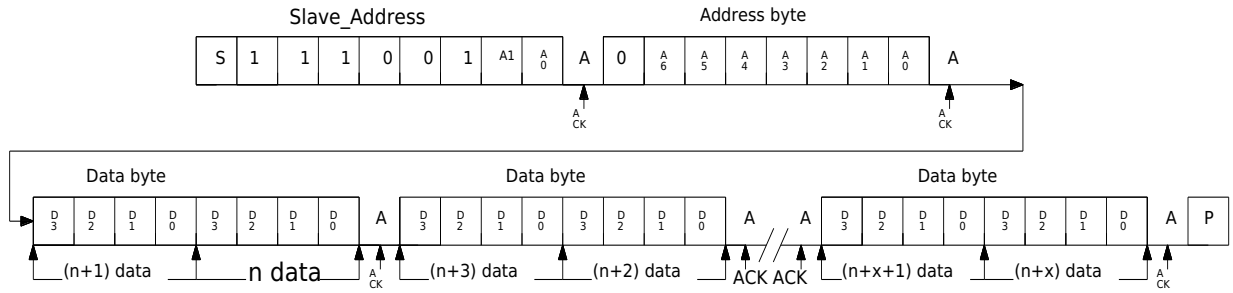


图17

4 Write command write data operations

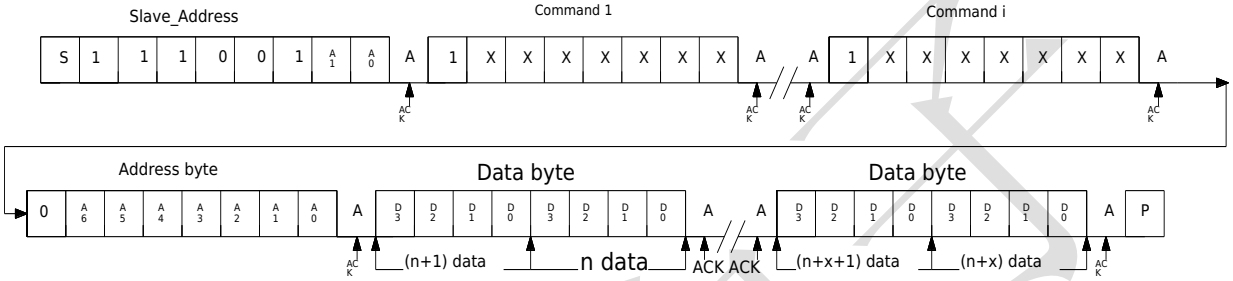


图18

Application circuit

Low power LED applications (direct drive mode): 32ROW*8COM Examples of patterns 图19

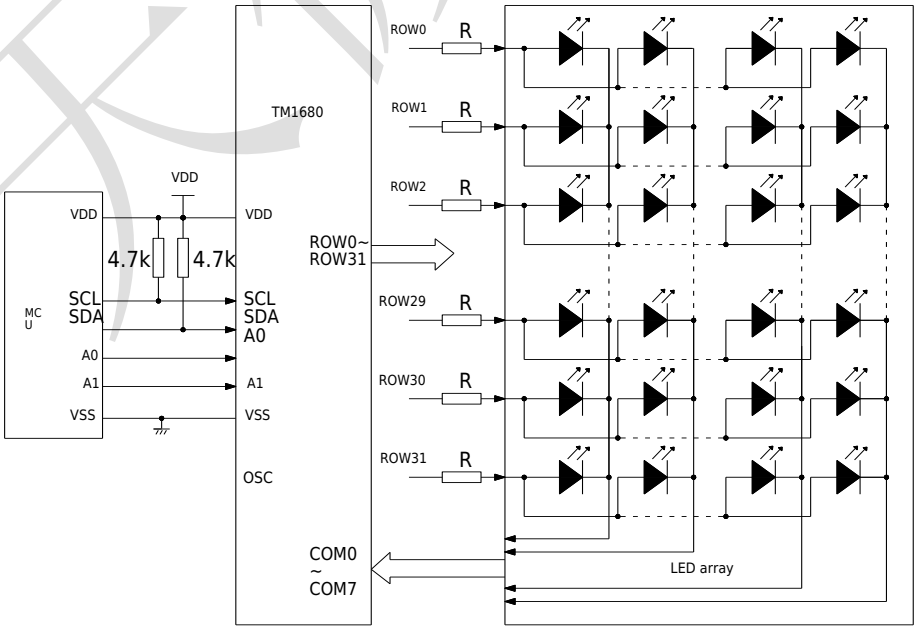


图19

Low power LED applications (direct drive mode):24ROW*16COM Examples of patterns 图20

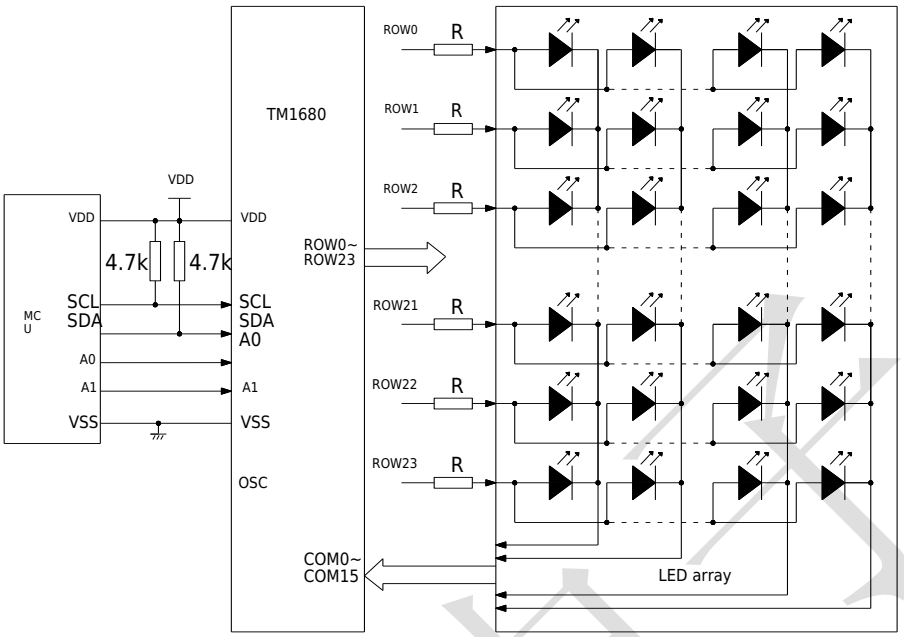


图20

Medium power LED applications (COM plus transistor drive mode): 32ROW*8COM Examples of patterns 图21

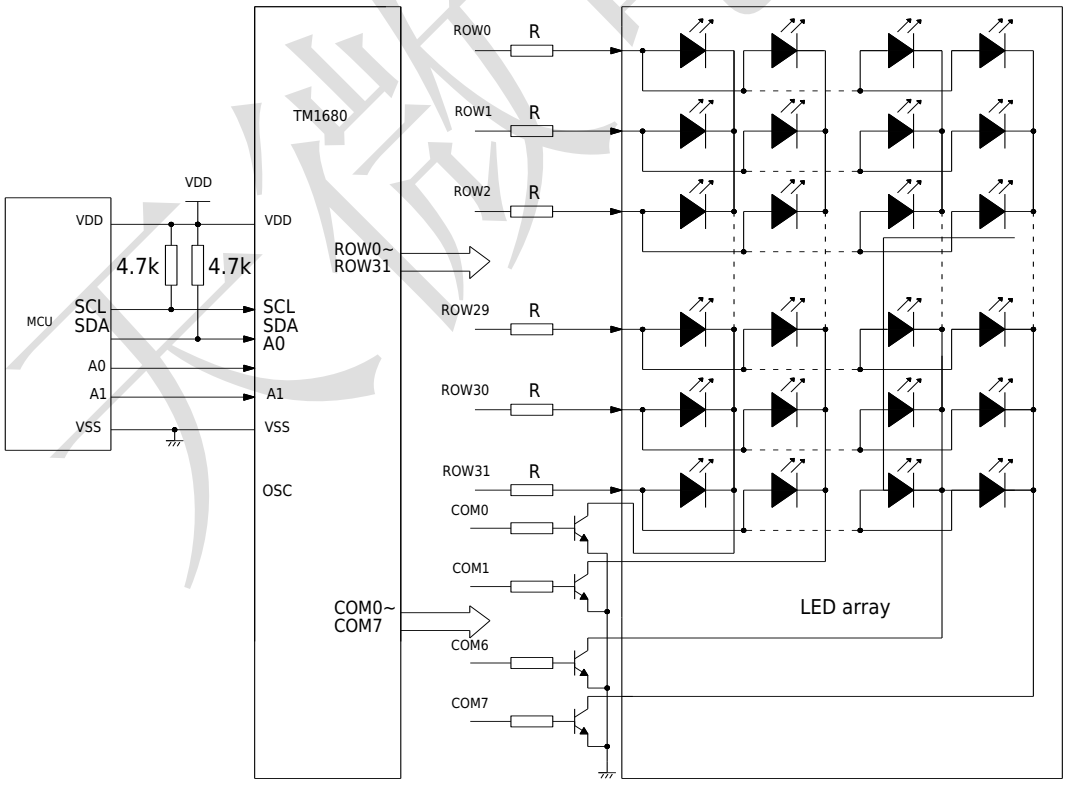


图21

Medium power LED applications (COM plus transistor drive mode): 24ROW*16COM Examples of patterns 图22

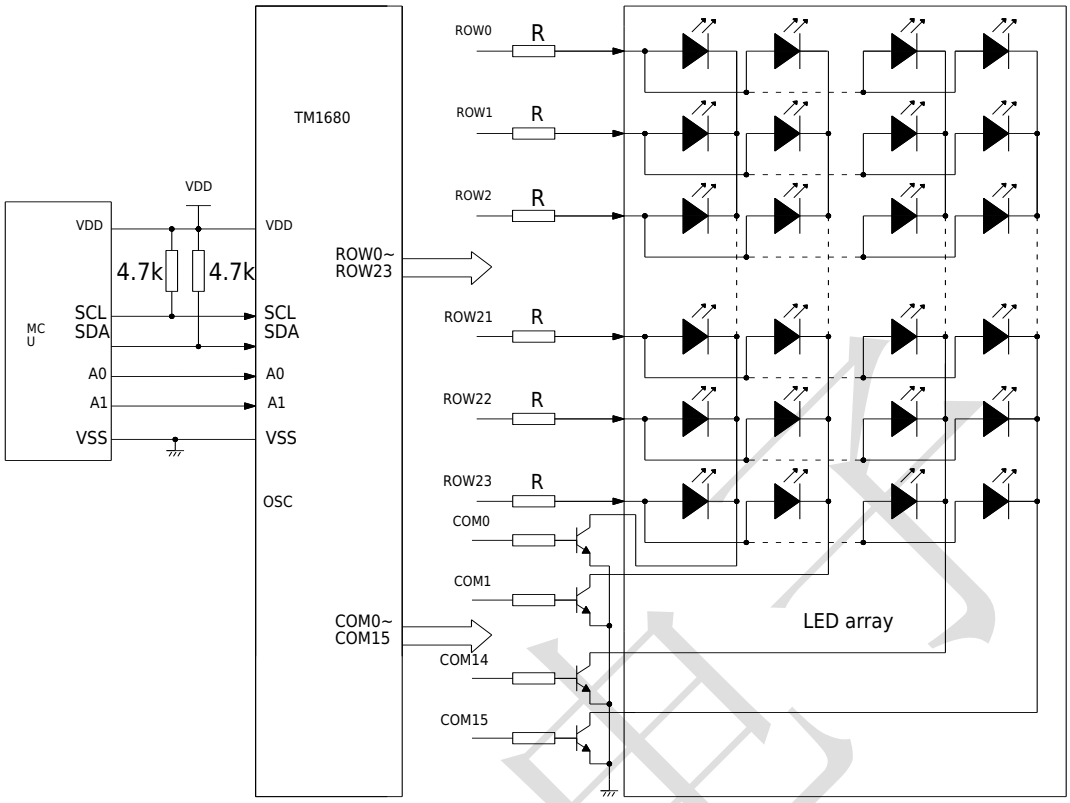


图22

High power LED applications (ROW COM plus transistor drive): 32ROW*8COM Examples of patterns 图23

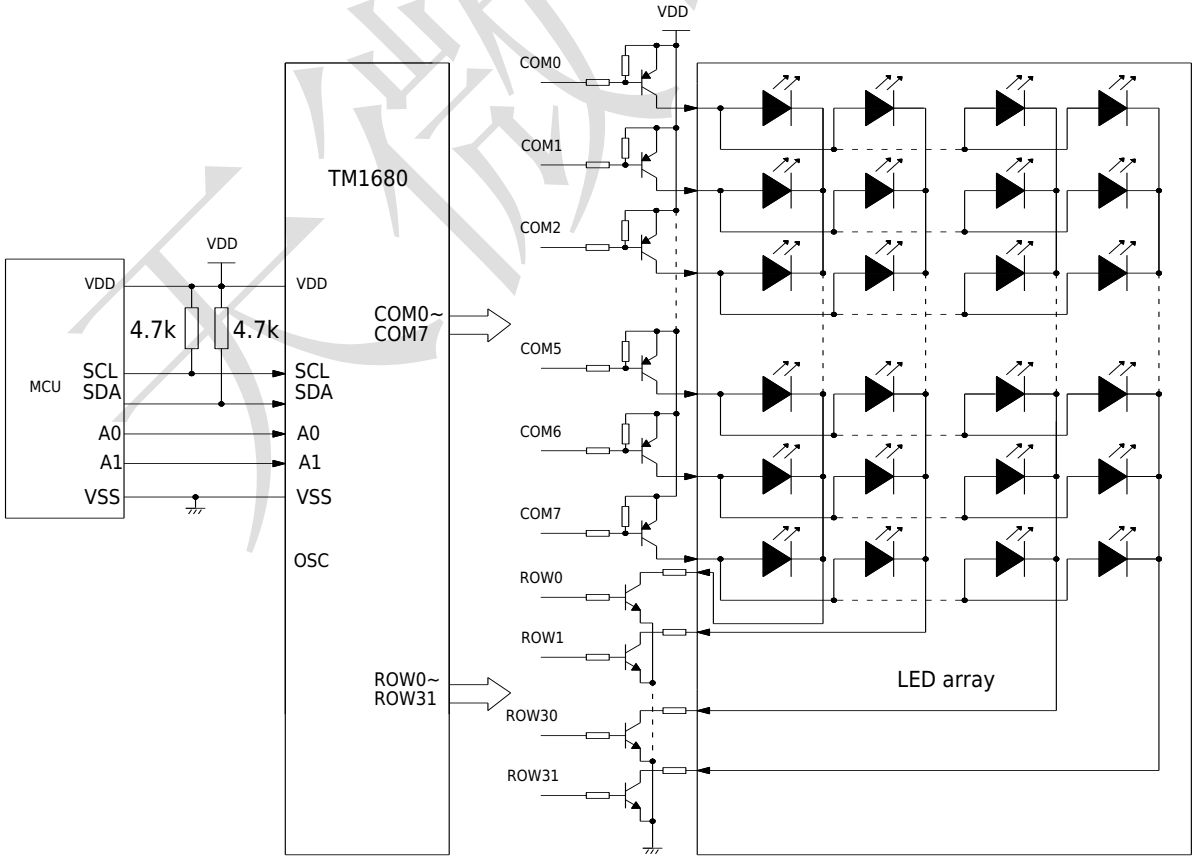


图23

High power LED applications(ROW COM plus transistor drive): 24ROW*16COM Examples of patterns 图24

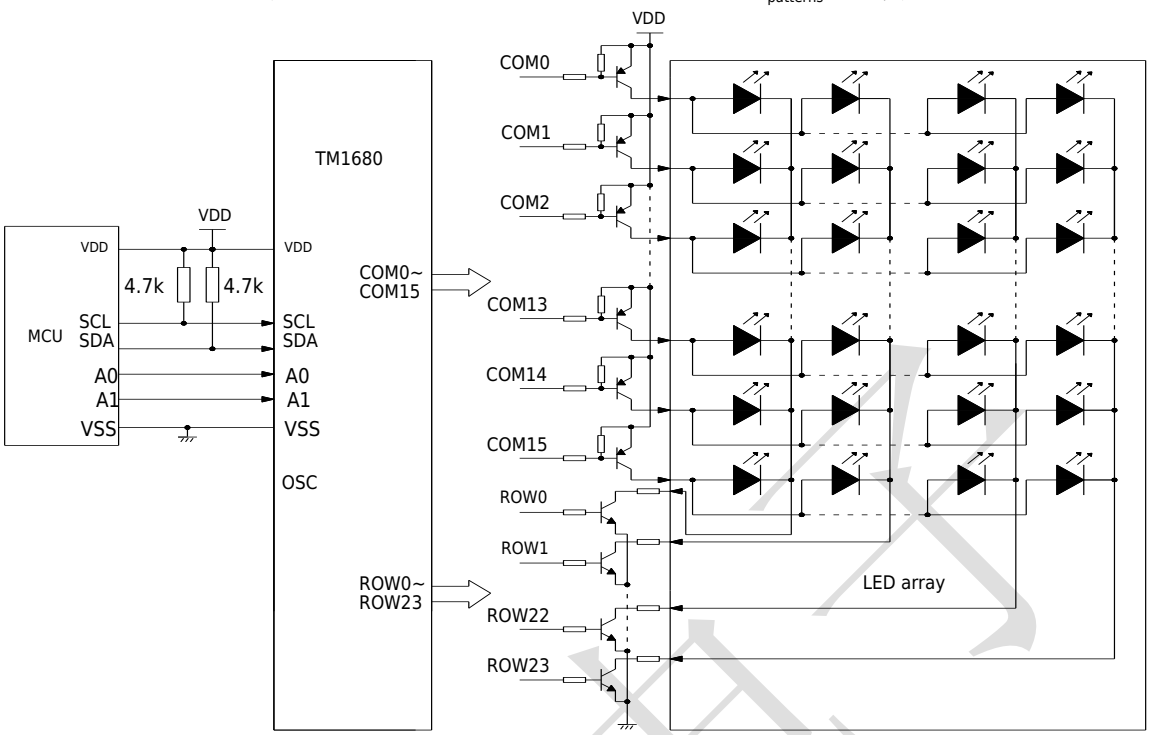


图24

Cascade application (direct drive mode): 32ROW*8COM Examples of patterns 图25

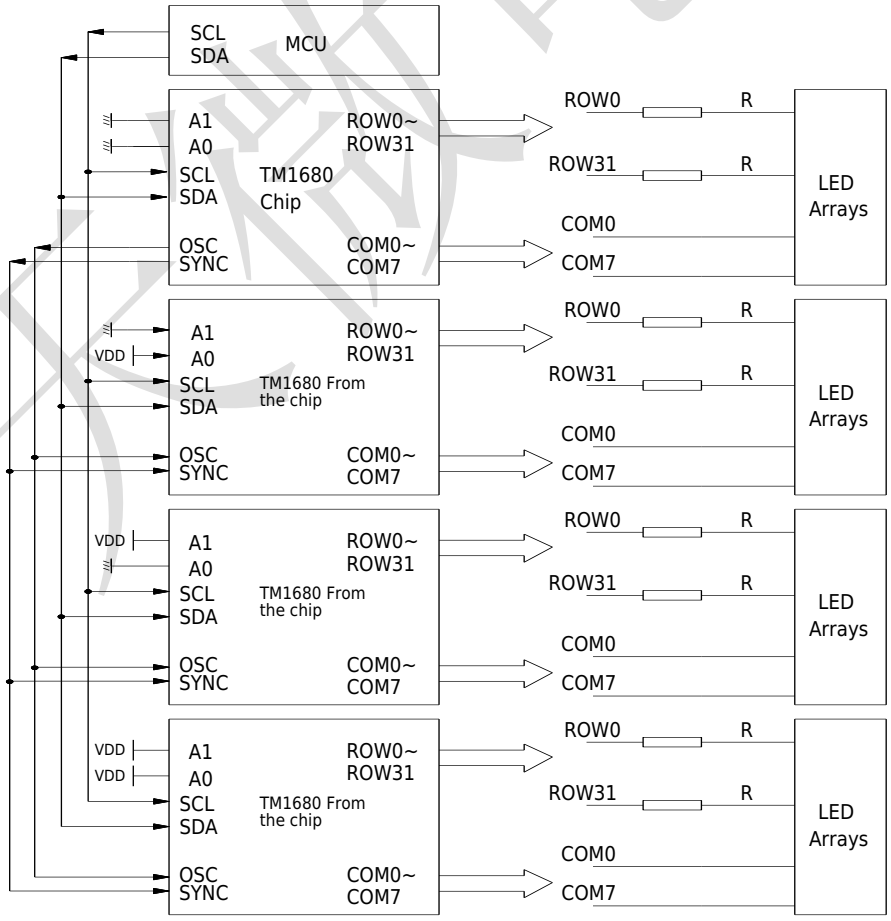


图25

Cascade applications (COM plus transistor drive): 32ROW*8COM Examples of patterns 图26

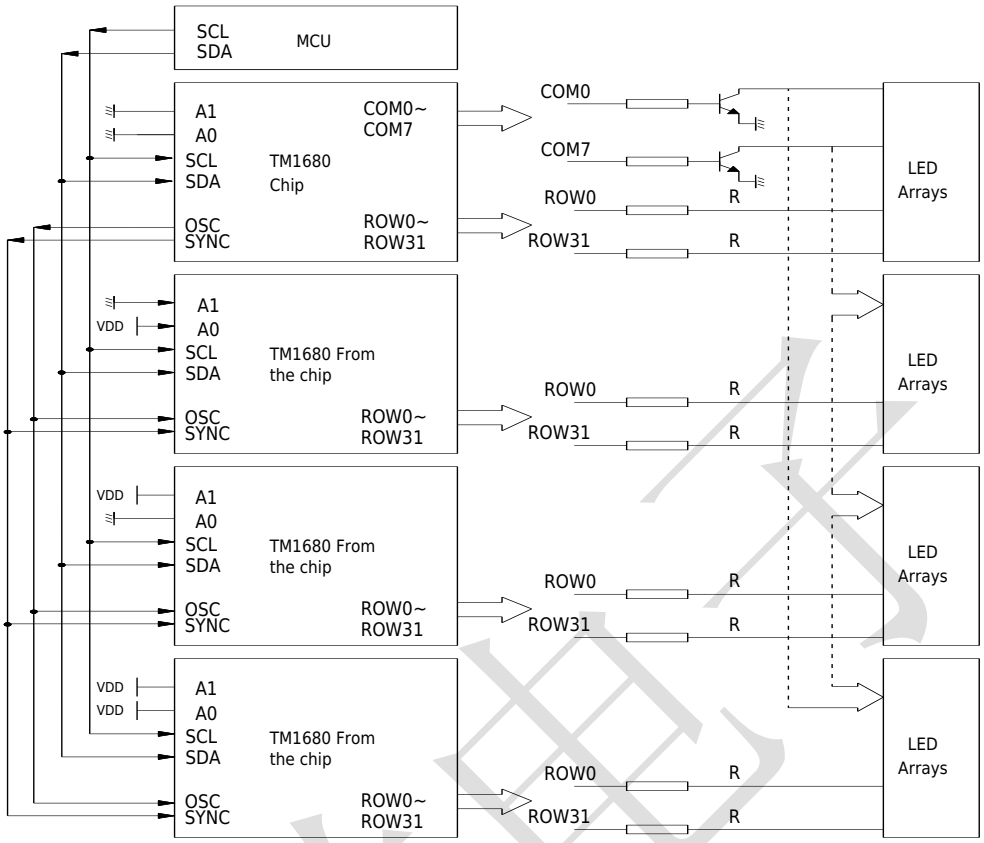


图26

Cascade application (direct drive mode): 24ROW*16COM Examples of patterns 图27

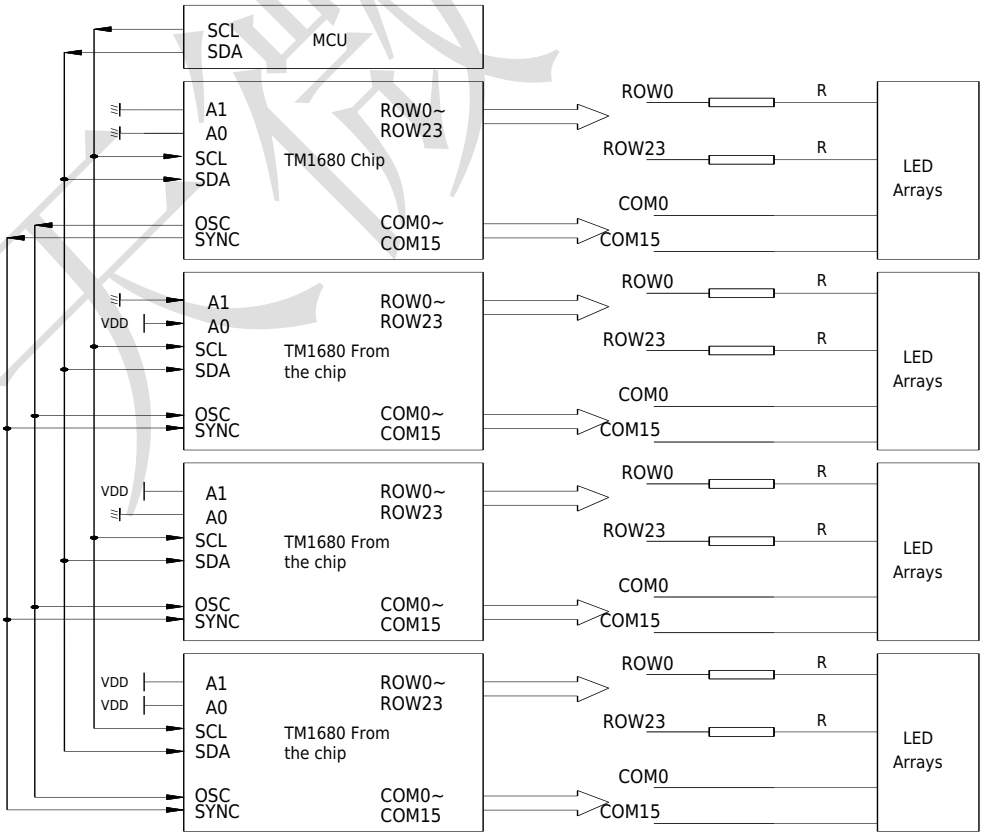


图27

Cascade applications (COM plus transistor drive): 24ROW*16COM Examples of patterns 图28

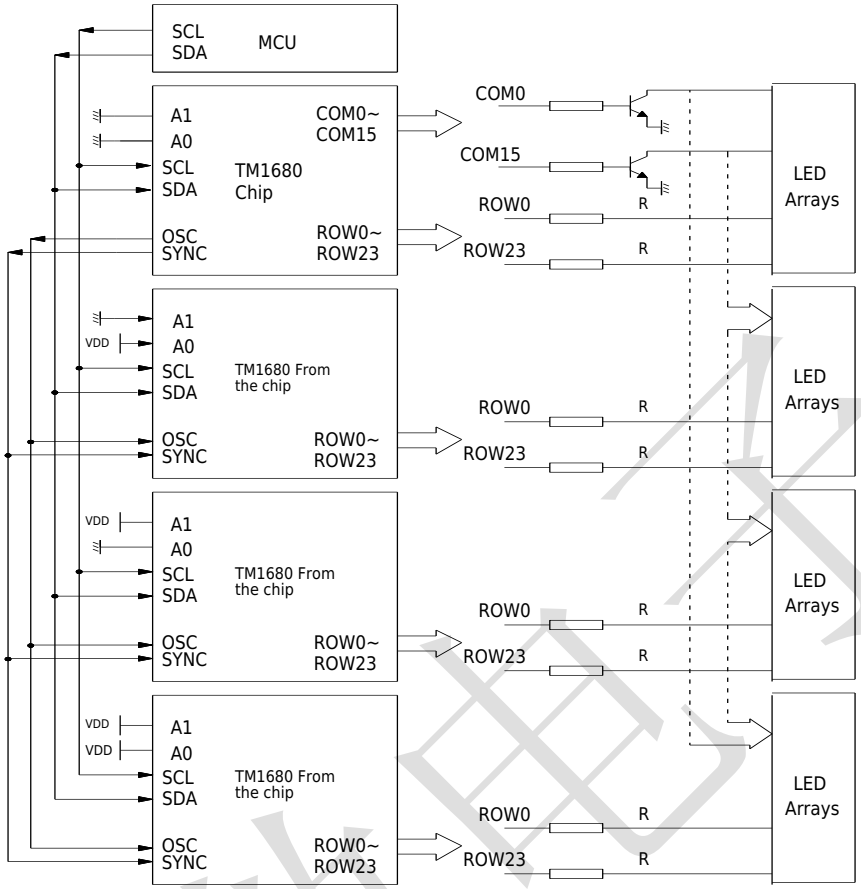
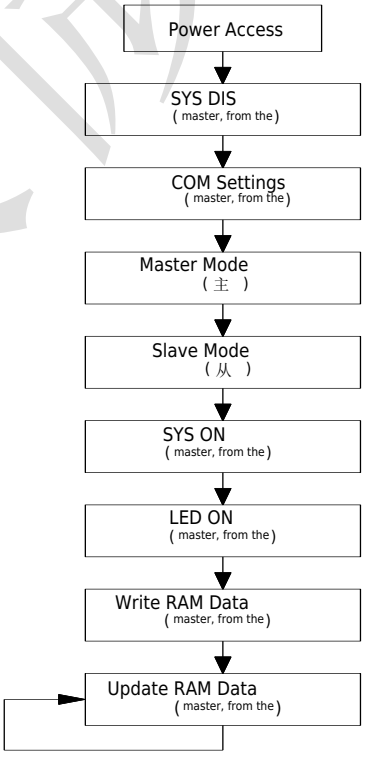


图28

General design flow chart



Command Overview Table :

Command Name	Command Code	D/C	Description of the function	Default
WRITE	1110- 01A1A0	D	Write the address of the slave machine	
Data address (I2C)	0 A6 A5 A4 A3 A2 A0	D	写 RAM Address	
The data format (I2C)	D0 D1 D2 D3 D4 D5 D6 D7	D	A3 - A0 Four down. Four down. R3 - R0 高	
SYS DIS	1000 - 0000	C	Turn off system clock and LED loop	√
SYS EN	1000 - 0001	C	Turn on the system oscillator	
LED OFF	1000 - 0010	C	Turn off LED loop	√
LED ON	1000 - 0011	C	Turn on the LED loop	
Blink O FF	1000 - 1000	C	Turn off the blinking function	√
Blink 2Hz	1000 - 1001	C	按 The frequency of the LED blinks 2Hz	
Blink_1Hz	1000 - 1010	C	按 The frequency of the LED blinks 1Hz	
Blink_0.5Hz	1000 - 1011	C	LED 按 0.5 Hz The frequency of flashing	
SLAVE MODE	1001 - 0Xxx	C	External oscillation, the clock is input from the OSC pin. Synchronous signal input by SYN pin	
RC Master Mode0	1001 - 100X	C	Built-in Oscillation, OSC Keep Low, Synchronized The signal remains high at the SYN pin and should only be For Single Chip	√
RC Master Mode1	1001 - 101X	C	Internal oscillation, internal frequency at OSC output, Synchronous signal output at SYN pin	
EXT CLK Master Mode0	1001 - 110X	C	External oscillation, the clock is input from the OSC pin. The synchronization signal is maintained high by the SYN pin. Only referenced to a single chip	√
EXT CLK Master Mode1	1001 - 111X	C	External oscillation, the clock is input from the OSC pin. Synchronous signal output from SYN pin	
COM Option	1010 - ABXX	C	当 ab=00, 8COM Nmos; 当 ab=01, 16COM Nmos; 当 ab=10, 8COM Pmos; 当 ab=11, 16COM Pmos;	00
PWM Duty	1011 - abcd	C	abcd 为 0-F abcd changes correspond separately 1/16—16/16 的 LED Driver 的 Brightness 节	F

Note:

1、X do not care, it is recommended to write "0".

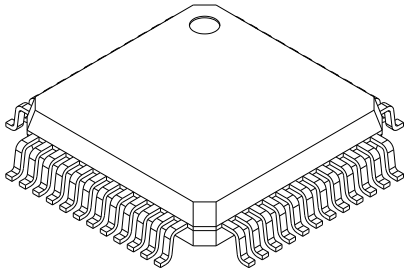
2、A6-A0 Memory address.

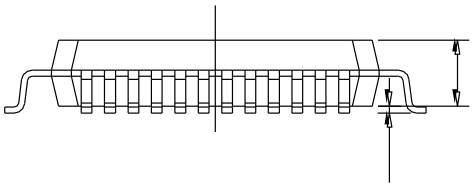
3、D0-D3 Memory data.

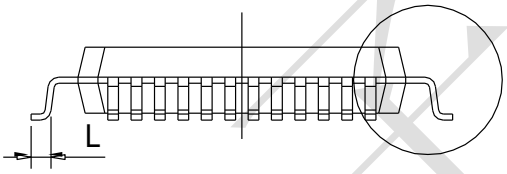
4、D/C data command mode.

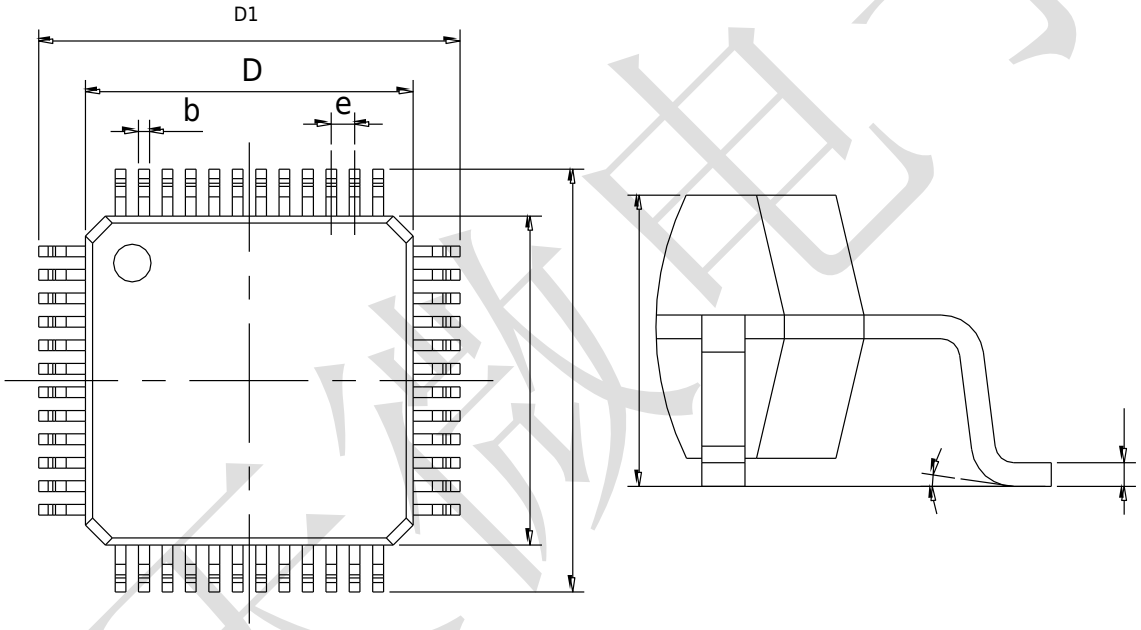
5、default: the state of the chip after power-up reset

Package Diagram (LQFP48 7m*7mm)



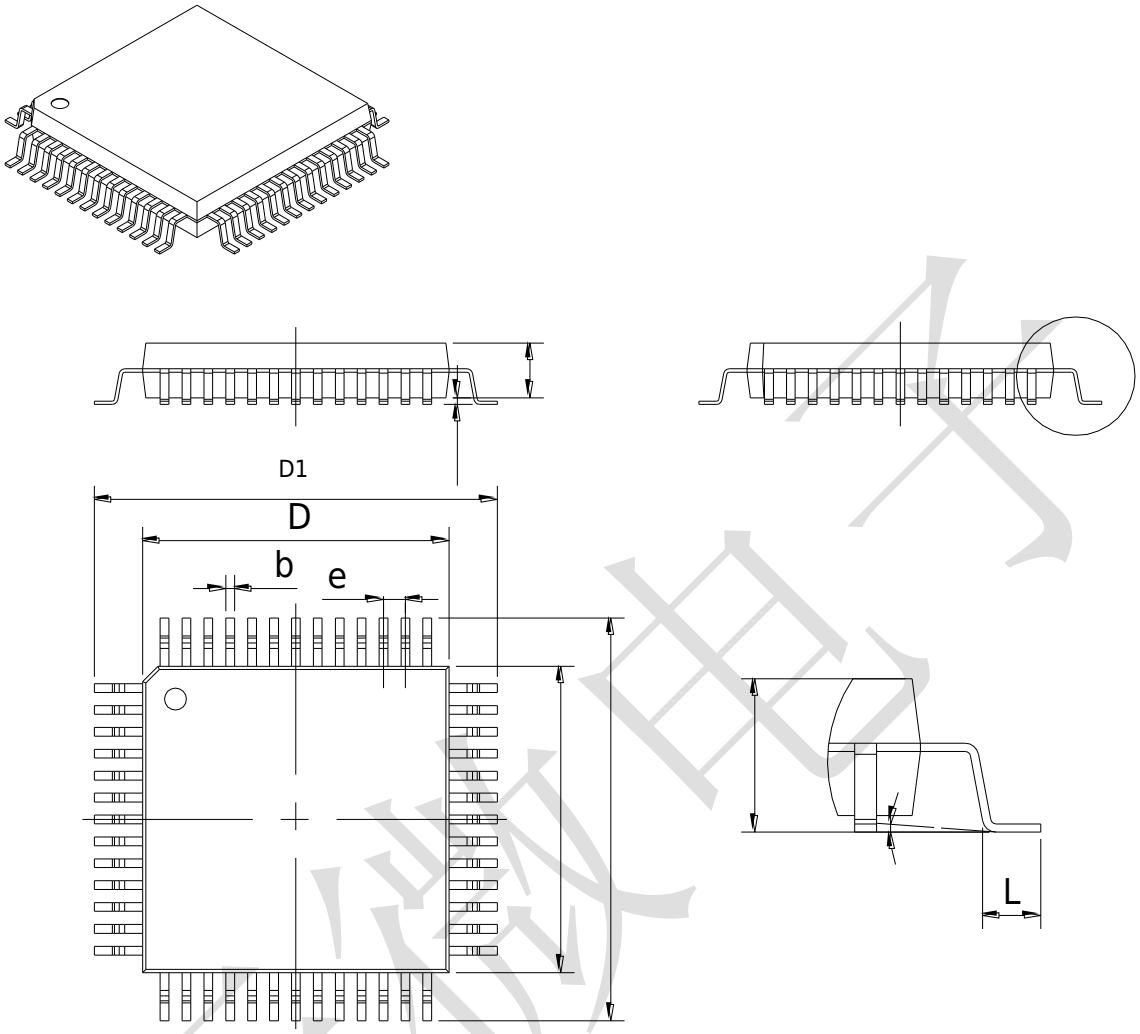






Symbol	Dimensions In Millimeters		Dimensions In Inchets	
	Min	Max	Min	Max
A		1.600		0.063
A1	0.050	0.150	0.002	0.006
A2	13.5	1.50 0	0.053	0.059
b	0.180	0.270	0.007	0.010
c	0.13 0	0.18 0	0.005	0.007
D	6.900	7VIII.100	0.272	0.280
D1	8.800	9.20 0	0.346	0.362
E	6.900	7.100	0.272	0.280
E1	8.800	9.20 0	0.346	0.362
e	0.500 (BSC)		0.020 (BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	7°	0°	7°

Package Diagram (QFP52 14m*14mm)



Symbol	Dimensions In Millimeters		Dimensions In Inchets	
	Min	Max	Min	Max
A	—	1.600	—	0.063
A1	0.100		0.004	
A2	1.350	1.500	0.053	0.059
b	0.400 (BSC)		0.016 (BSC)	
D	13.900	14.100	0.547	0.555
D1	15.800	16.200	0.622	0.638
E	13.900	14.100	0.547	0.555
E1	15.800	16.200	0.622	0.638
e	1.000 (BSC)		0.039(BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	7°	0°	7°

All specs and applications showing above subject to change without prior notice.

(The above circuit and specifications are for reference only, subject to correction by the Company without prior notice.)