Characteristic description

The TM1680 is a memory switching LED display control driver chip with multiple ROW/COM modes (32ROW/8COM and 24ROW/16COM) can be used to drive dot matrix LEDs. The chip provides 16 levels of pulse width modulation control output for software settings, You can adjust the brightness of the LED loop display. Using serial interface (I2C communication interface) serial input, you can easily access the command mode (COMMAND, MDOE) and data mode (DATA, MODE). Communication of TM1680. Through the TM1680, continuous output display can be performed, which has a wide range of applications in the display of LED light, Industrial instrument control, digital clock/thermometer, counter and voltmeter display, readout of meter data, LED display, smart bracelet and other applications. Ben Excellent performance and reliable quality.

Features of the function

- Operating voltage from 2.4 to 5.5 V Available in 32ROW*8COM and 24R OW*16COM
- Integrated display memory - 64*4 display RAM (32ROW*8COM), 96*4 display RAM
- (24ROW*16COM) 16 levels of pulse width modulation control brightness Built-in
- 256kHz RC oscillator I2C Interface (SDA, SCL) Communication Data mode and
- command mode instructions Optional NMOS output channels and PMOS output
- channels Package: LQFP48, LQFP52
-
-
-

Frame diagram of the internal structure

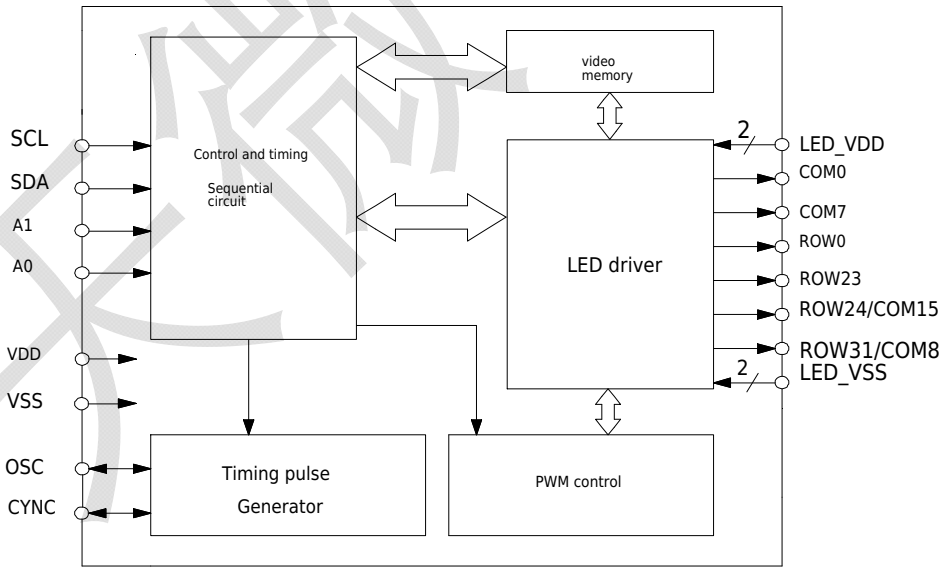


Figure 1

Pipe arrangement

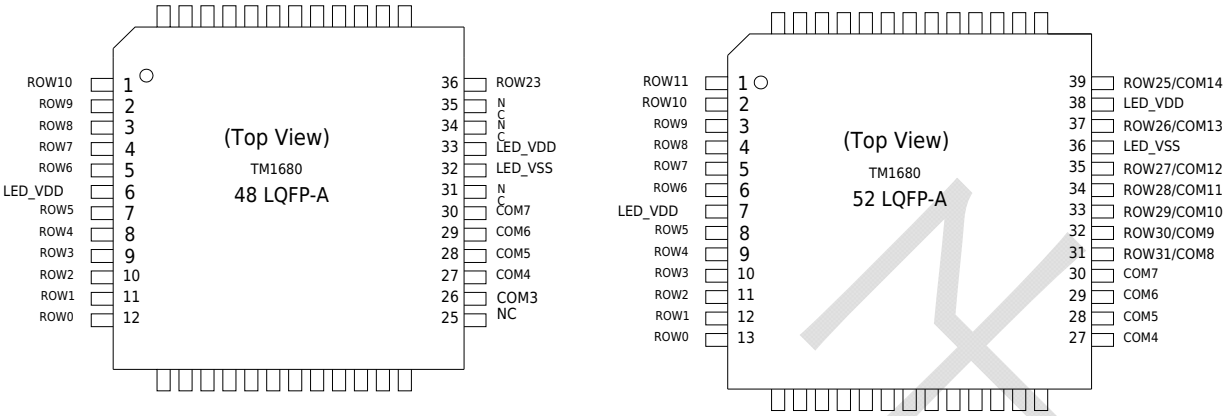


Figure 2

Pin Function

Pin Name	Pin serial number	I/O	Description of the function
VDD	21	-	Chip Logic Power Supply Positive
VSS	14	-	Chip Logic Power Supply Negode
LED_VDD	7/38	-	LED driver power supply positive, each LED_VDD is double key
LED_VSS	25/36	-	LED driver power supply negative, each LED_VSS is double key
ROW0~ROW23	1 ~ 6/8 ~ 13/41 ~ 52	O	LED line drive output
ROW24/COM15 ~ROW31/COM8	31 to 35/37/39/40	O	LED line drives output or common output, each COM pin is double button
COM0 ~ COM7	22 ~ 24/26 ~ 30	O	LED common output, each COM pin is double button
SYNC	20	I/O	If the main trigger mode or the external extended trigger mode is selected, the sync signal will be removed from the SYNC pin output; if passive mode is selected, the synchronization signal will be input from the SYNC pin.
OSC	15	I/O	When RC oscillation main trigger mode is selected, the system clock is generated by on-chip RC oscillation and is removed from the OSC pin output; if passive mode or external expansion trigger mode is selected, the system clock is controlled by the OSC foot input from outside.
A0	19	I	slave address expansion bit with built-in pull-up resistor.
A1	18	I	slave address expansion bit with built-in pull-up resistor.
SCL	17	I	I2C communication clock input, data on the SDA line is written to TM1680, Built-in pull-up resistor.
SDA	16	I/O	I2C communication data input/output ports require external pull-up resistors for applications.

*Note: The pin number in the table above, for example, the LQFP52 package. Different packages, feet are different, please refer to the pin for details Arrange diagram. The 48PIN package is displayed 24*8 and does not support 1/16 degree of brightness.

Input Output Equivalents

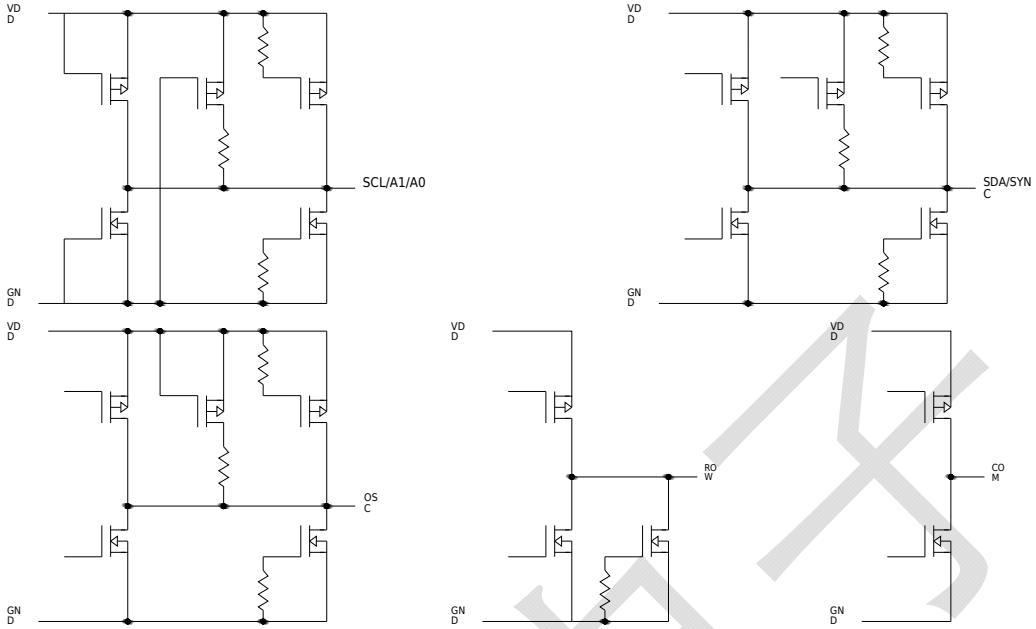


Figure 3

Integrated circuit system electrostatic sensitive device, easy to use in the dry season or dry environment to generate a large amount of static electricity, electrostatic discharge can be

Can damage the integrated circuit, we recommend taking all appropriate IC preventive measures, improper operation Welding, may cause ESD damage or performance degradation, the chip does not work properly.

Limit parameters (1) (2)

Parameter Name		Parameter Symbols	Limit value	Single Bit
Logic Supply Voltage		VDD	VSS-0.3V to VSS+6V	V
Voltage Range at Input	SDA, SCL, OSC, SYNC	Vin	VSS-0.3 to VDD+0.3	V
Working temperature range		Topt	-40 ~+85	°C
Storage temperature range		Tstg	-55 to +125	°C

(1) the chip work for a long time in the above limit parameters conditions, may cause device reliability reduction or permanent damage, day microelectronics

It is not recommended that any of these limits be reached or exceeded when used.

(2) All voltage values are tested in relation to the system.

Recommended working conditions

Parameter Name	Parameter Symbol	Minimum	Typical	Maximum	
Working voltage	VDD	2.4	5.0	5.5	V
Input Low Voltage	Vil	0	-	0.3 VDD	V
Input High Voltage	Vih	0.7VDD	-	5	V

DC electrical characteristics

Test at VDD=2.4~5.5V and Ta=+25°C, unless otherwise stated				TM1680			units
Parameter Name	Parameter symbol	VDD	Test Condition	Minimum	Typical	Maximum	
Working Current	IDD	5.0V	on-chip RC, no load, open display		0.3	0.6	mA
Standby Current	ISTB	5.0V	Power saving mode, no load		0.1	10	μA
OSC, SYNC, SDA Sink Current	IOL1	5.0V	Vol=0.5V	18	25	-	mA
OSC, SYNC, SDA Pull Current	IOH1	5.0V	Voh = 4.5 V	-10.	-13.	-	mA
ROW Sink Current	IOL2	5.0V	Vol=0.5V	12	16	-	mA
ROW pull current	IOH2	5.0V	Voh = 4.5 V	-50.	-70.	-	mA
COM sink current	IOL3	5.0V	Vol=0.5V	250	350	-	mA
COM pull current	IOH3	5.0V	Voh = 4.5 V	-45.	-60.	-	mA
pull-up resistance	Rph	5.0V	SDA, SCL, OSC, SYNC	18	27	40	KΩ

Switches Features

Test at operating temperature of 25°C, unless otherwise stated			VDD=2.4V~5.5V		VDD=3.0V~5.5V		units
Parameter Name	Parameter Symbols	Test Conditions	Minimum	maximum	maximum	maximum	
Clock Frequency	FSCL	Chip Internal Clock	-	100	-	400	kHz
Bus idle time	TBUF	Bus at the next time The clock before the arrival of the empty Free time	4.7	-	1.3	-	μs
Start Signal Hold Time	THD: STA	-	4	-	0.6	-	μs
SCL Low Time	TLOW	-	4.7	-	1.3	-	μs
SCL High Time	Thigh	-	4	-	0.6	-	μs
Start Signal Set up Time	TSU: STA	-	4.7	-	0.6	-	μs
Data retention time	THD: DAT	-	0	-	0	-	μs
Data creation time	TSU: DAT	-	250	-	100	-	ns
SDA/SCL Rise Time	tr	-	-	1	-	0.3	μs
SDA/SCL Drop Time	tf	-	-	0.3	-	0.3	μs
Stop signal set up time	TSU: STO	-	4	-	0.6	-	μs
Denoising at SDA/SCL Input Time	TSP	Denoising Time	-	20	-	20	ns

SSRP

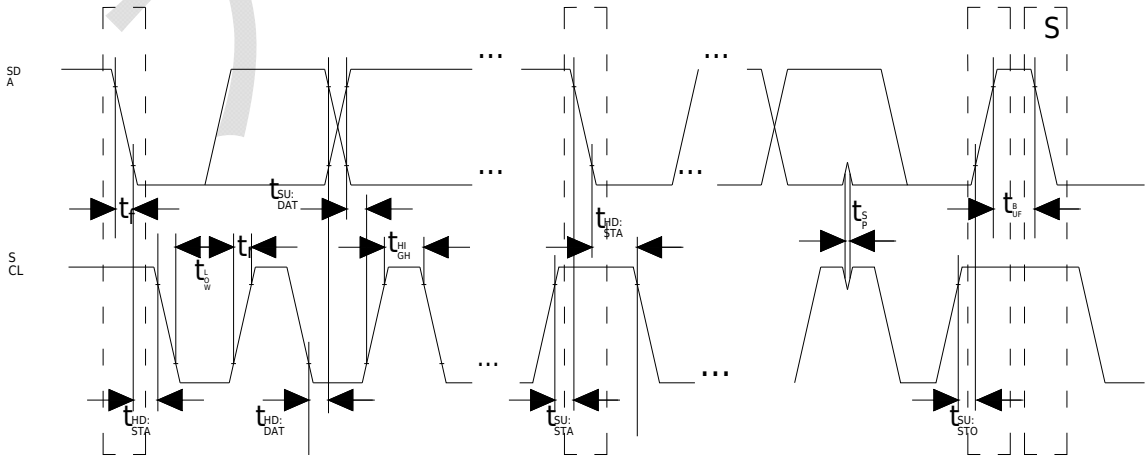


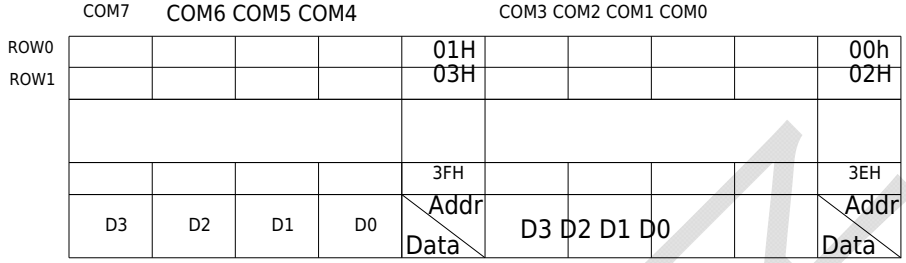
Figure 4

Description of the function

1 Display Memory (RAM)

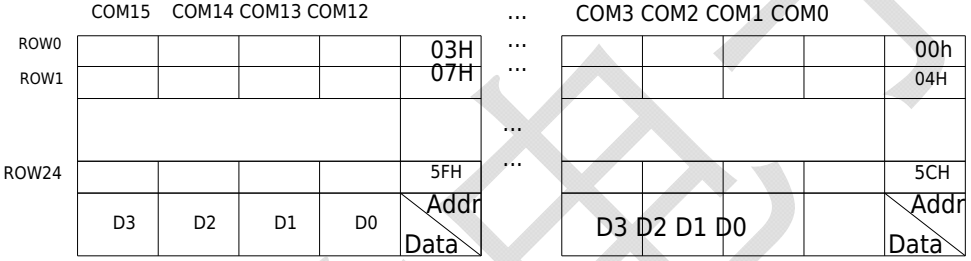
Static display memory consists of 64*4-bit and 96*4-bit formats to store the data you need to display. If the pattern 32ROW/8COM-mode is

, RAM has 64*4 bits of storage, and 96*4 bits of RAM if mode 24ROW/16COM mode is selected. RAM directly to the LED display drive, and if the RAM data is set to “1", the corresponding LED will be lit. Figures 5 and 6 below give Out is a map of RAM to LED:



32 ROW & 8 COM for 64 × 4 Display RAM

Figure 5



24 ROW & 16 COM for 96 × 4 Display RAM

Figure 6

2 System clock

The TM1680's system clock is used to generate the clock frequency at which the system operates. LED driver clock, system clock can be taken from on-chip RC

oscillator (256kHz) or an external clock input using S/W settings. The system oscillator is constructed as shown in Figure 7 when the SYS DIS command is When executed, the system clock stops and the LED operating cycle is closed (this instruction can only be applied with the on-chip RC oscillator). Once the system is When the clock stops, the LED appears blank and the timebase loses its function. LED_OFF command is used to turn off the LED working cycle, LED working After the loop is closed, use the SYS_DIS command to save power costs and act as a power-saving command; if an off-chip clock source is selected, It is not possible to turn off the oscillator and perform power-saving mode using the SYS DIS command. Crystal oscillator can provide clock frequency via OSC pin rate, in which case the system will not be able to enter power-saving mode. When the system is powered on, the TM1680 is in the SYS DIS state by default.

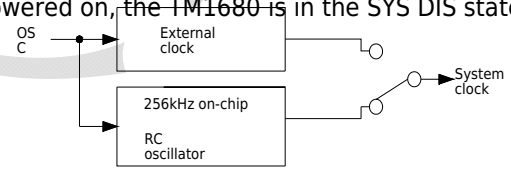


Figure 7

3 LED driver

The TM1680 contains 256 (32*8) and 384 (24*16) LED drivers, which can be set to 32*8 or 24*16 显

In the mode, N-MOS or P-MOS output channels can be selected via the COM port output. These features make the TM1680 adaptable to different for LED applications. The LED driver clock is derived from the system clock. The clock is usually driven by an on-chip RC oscillator 256kHz or Extended external oscillator. See the command overview table for detailed setup commands.

4 cascade operations

When cascading operations, the first chip in the cascade is set to host mode with pins SYNC and OSC used as outputs; the second chip in the cascade

The chip is set to slave mode, its pin SYNC and OSC are used as inputs and are connected to the SYNC and OSC feet of the host chip. Device Ground of TM1680 Address contains 2 bit external address selection bits A1, A0, so you can connect up to 4 TM1680 to the same bus. Please refer to Cascade for detailed settings Application circuit diagram.

5 LED drive mode output waveform

32 × 8 N-MOS open-drain output drive mode output waveform is shown below (Tclk=1/Fsys):

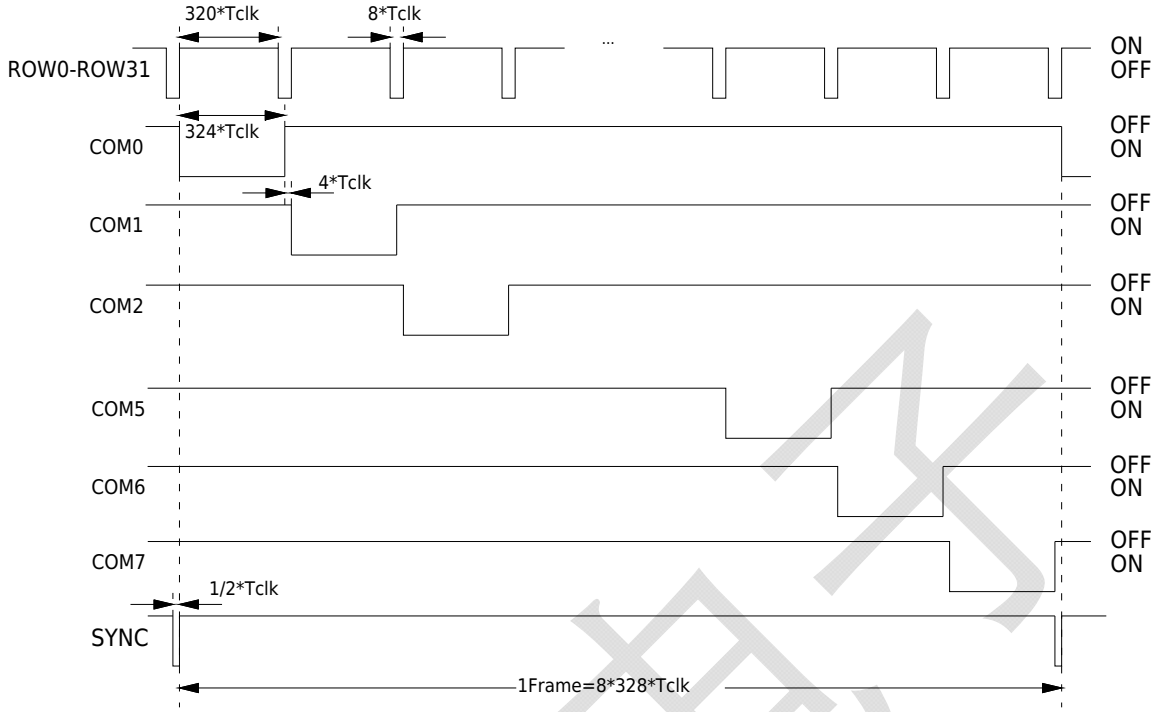


Figure 9

24 × 16 P-MOS open-drain output drive mode (Tclk= 1/Fsys, COM pin plus transistor):

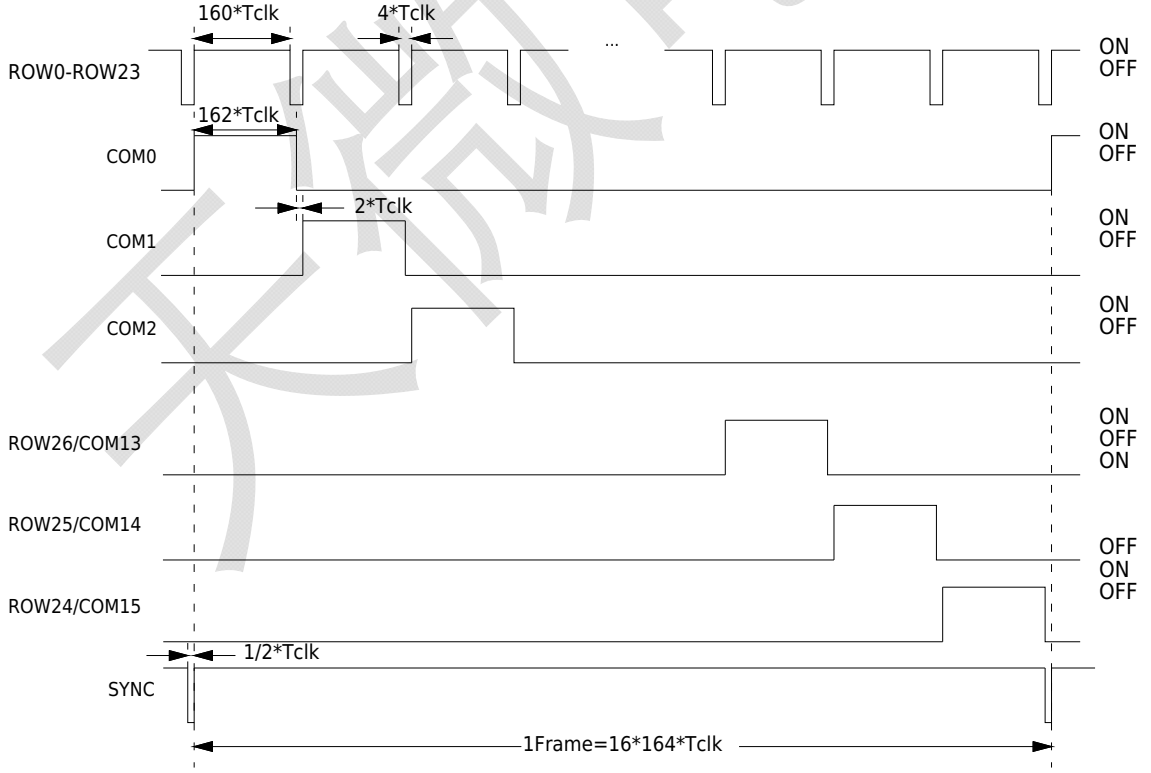


Figure 10

6 flash

The TM1680 has a flashing function that allows all LEDs to flicker at a certain frequency. The flicker rate can be set via the Blink command. to be divided into 2Hz/1Hz/0.5Hz. The following is the output waveform with a flashing frequency of 2Hz:

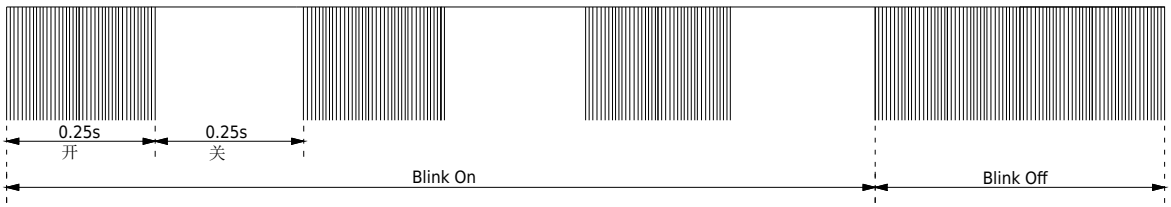


Figure 8

7 brightness adjustment settings

The TM1680 can be controlled by setting the PWM drive pulse width at the ROW end. Figure 11 below shows the COM and

Output waveform at ROW end: (1) T=20 × Tclk (32 × 8 drive mode); (2) T=10 × Tclk (24 × 16 drive mode); (3) Tclk = 1/Fsys

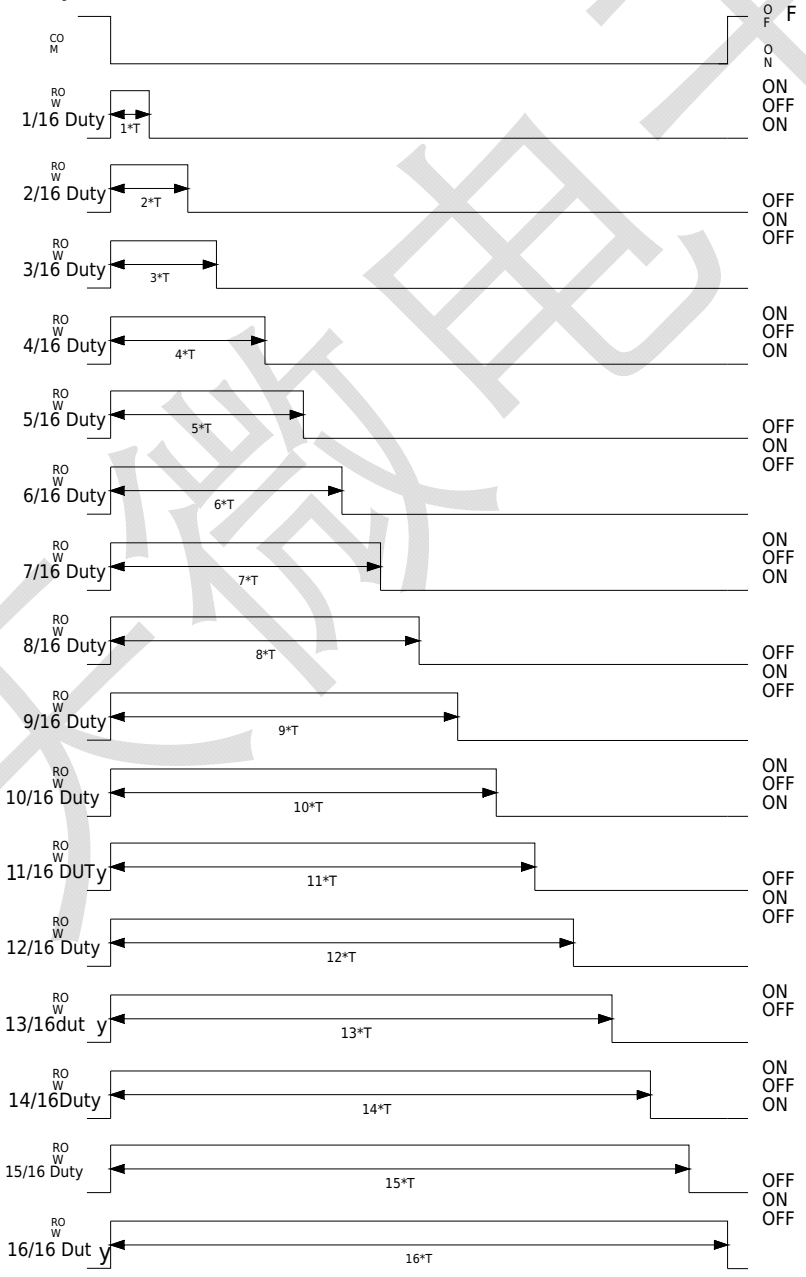


Figure 11

8 command format

This chip must follow these steps when entering commands or displaying data: (1) Formation of the starting conditions (2) Send slave address (3) Command, display the transmission of data (4) Formation of stop conditions

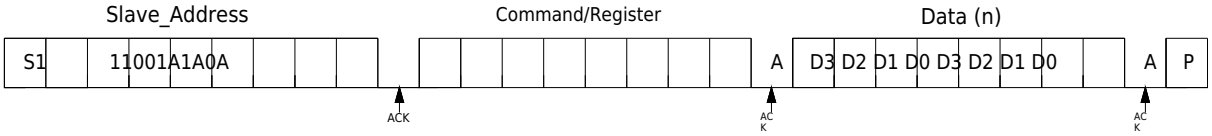


Figure 12

9 I2C Serial Interface

This chip is transmitted by the I2C protocol 2-wire serial interface, containing a serial data line SDA and clock line SCL, within two lines

The pull-up resistor is high when the bus is idle.

A starting signal is generated by the controller for each data transfer, using synchronous serial transmission, TM1680 per byte received

After all responded to an ACK answer signal. Each byte sent to the SDA line must be 8 bits and the number of bytes that can be sent per transfer No restrictions. Each byte must be followed by an ACK response signal, which falls from the 8th edge of the SCL signal when the ACK signal is not needed A low “L” is required until the ninth signal descending edge. When data is transmitted from the highest bit, the controller generates a stop signal by to terminate the bus transfer, while the start signal is resent during data transmission without a stop signal.

Data on the SDA remains stable when SCL is HIGH; SDA changes are allowed when SCL is LOW. If SCL is high, the

A descending edge is generated on the SDA, and a rising edge on the SDA is considered a stop signal if the SCL is high. As shown in the figure below:

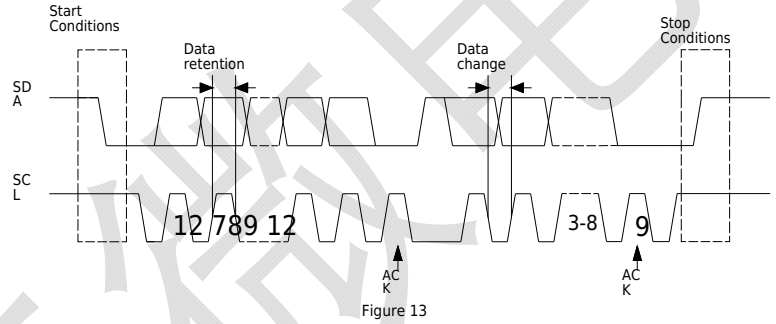


Figure 13

Time sequence graph

1 Write command operation

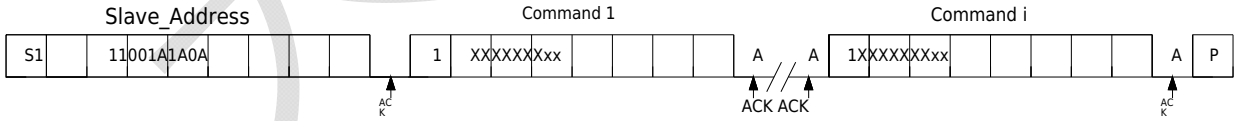


Figure 14

As shown in Figure 15, the 8-bit slave device is fixed to 111001 from the high 6-bit address byte, and the next 2-bit A1 and A0 are ground outside the device

Address.

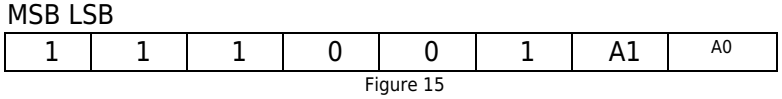


Figure 15

2-byte write operation

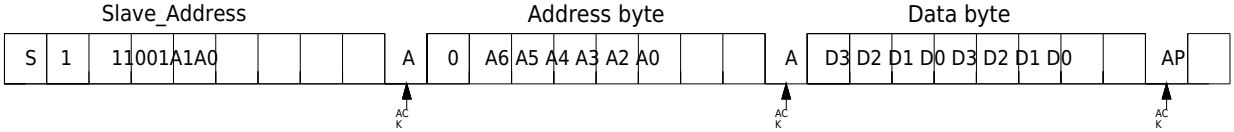


Figure 16

3 page write operations

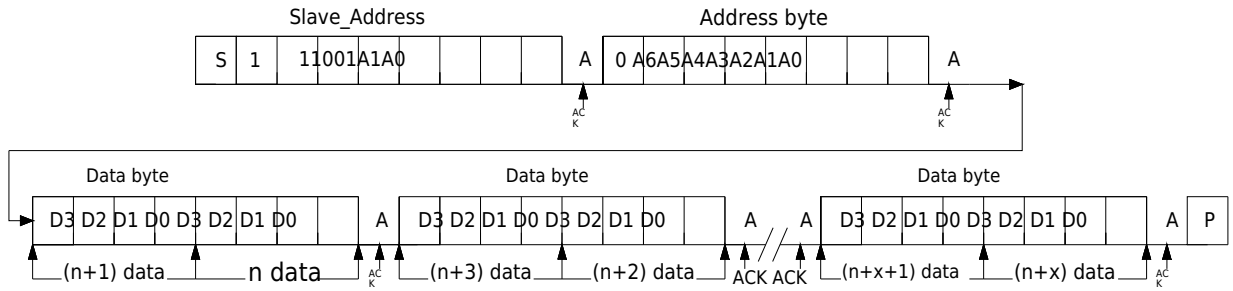


Figure 17

4 write commands+write data operations

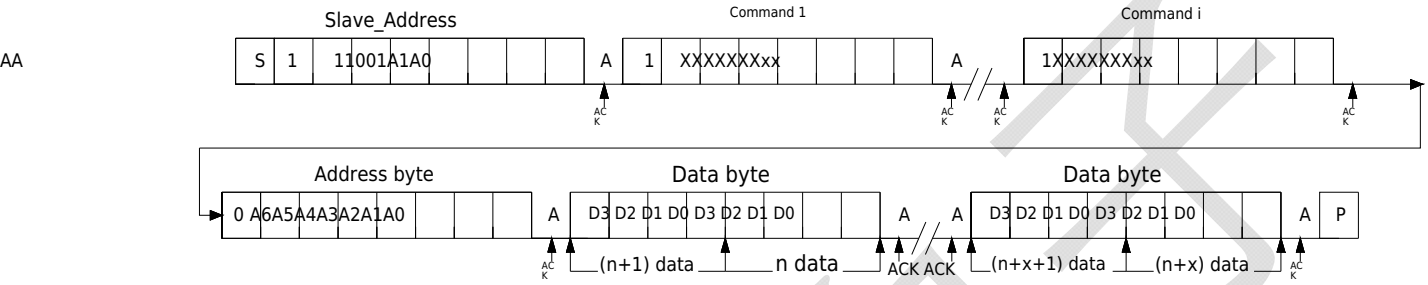


Figure 18

Application circuit

Low power LED application (direct drive mode): Example diagram of 32ROW*8COM mode 19

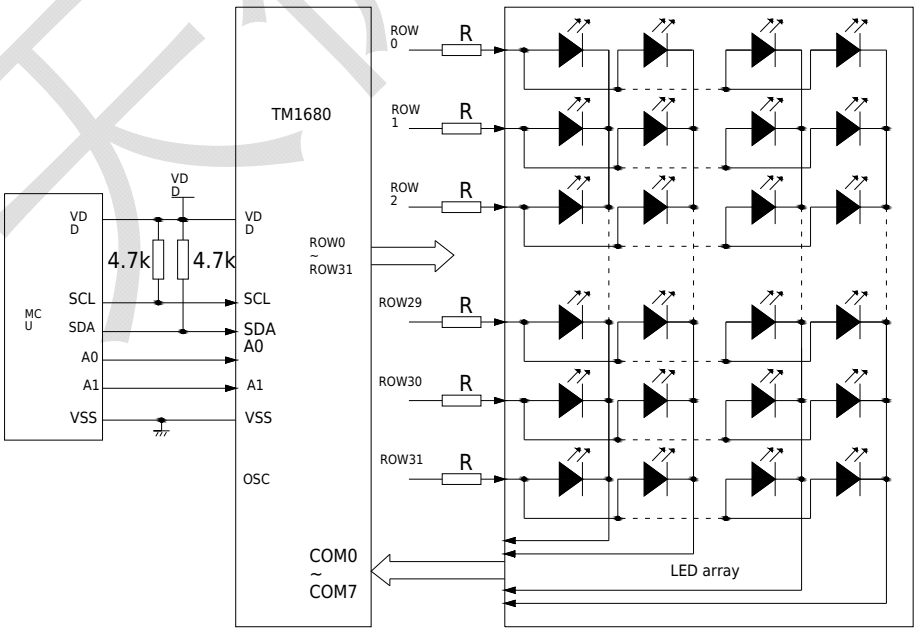


Figure 19

Low Power LED Application (Direct Drive Mode): Example of 24ROW*16COM Mode 20

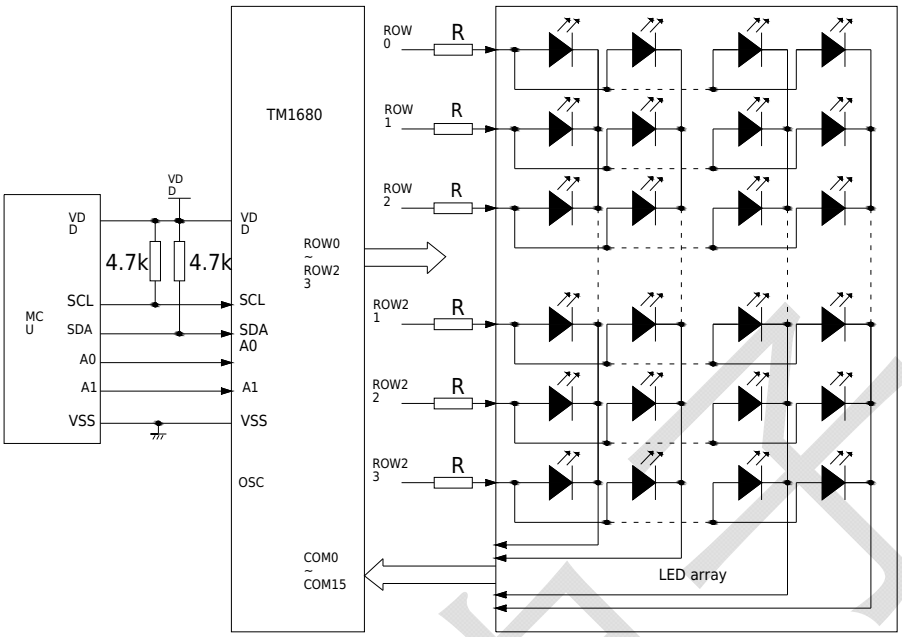


Figure 20

Medium power LED application (COM plus transistor drive mode): 3 2ROW*8COM mode example diagram 21

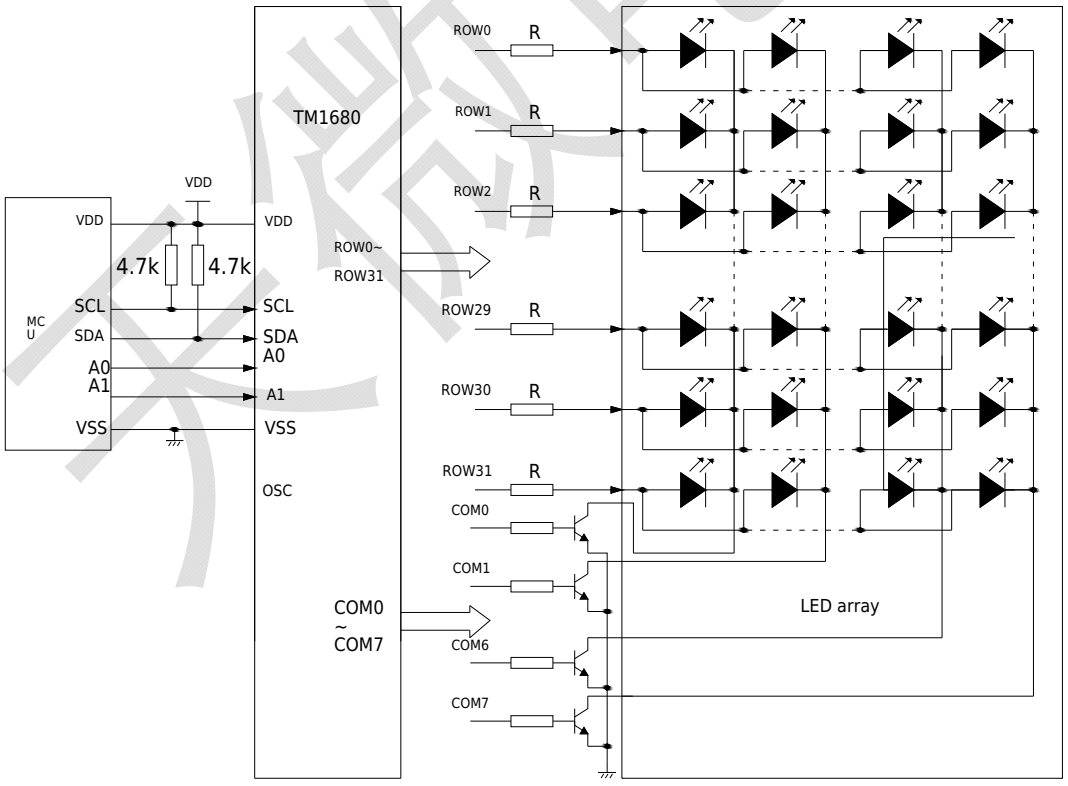


Figure 21

Medium power LED application (COM plus transistor drive mode): 2 4ROW*16COM mode example diagram 22

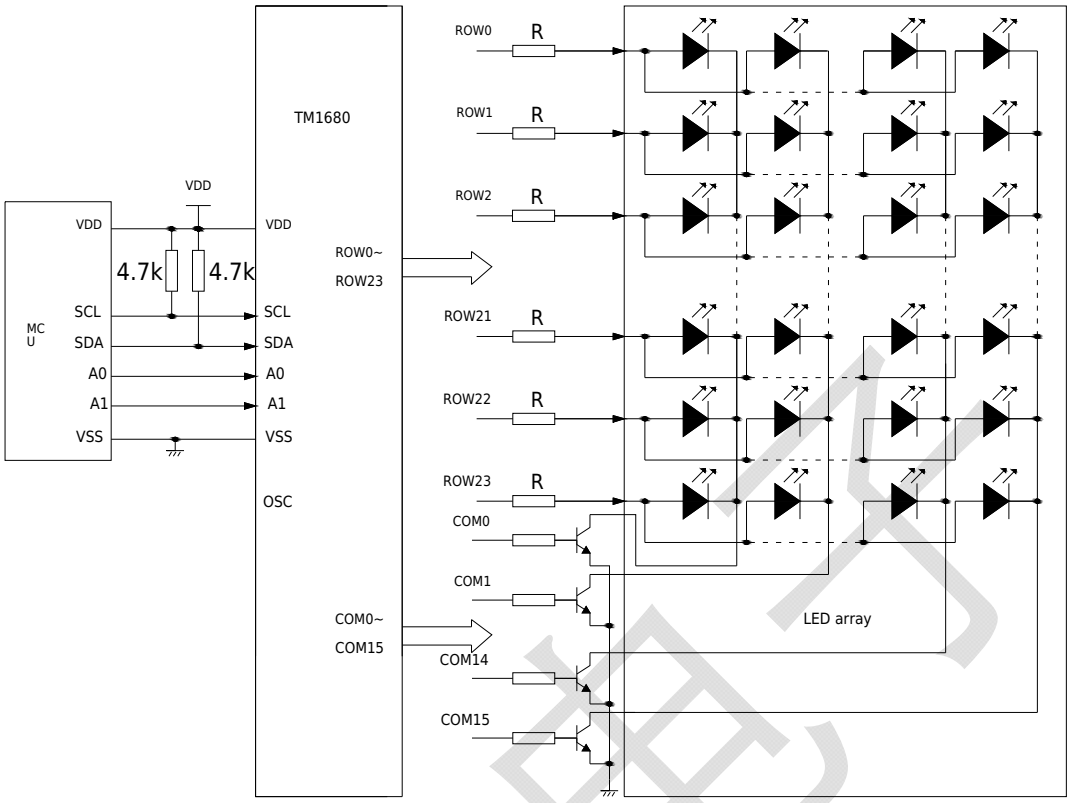


Figure 22

High power LED applications (ROW and COM plus transistor drive mode): Example diagram of 32ROW*8COM mode 23

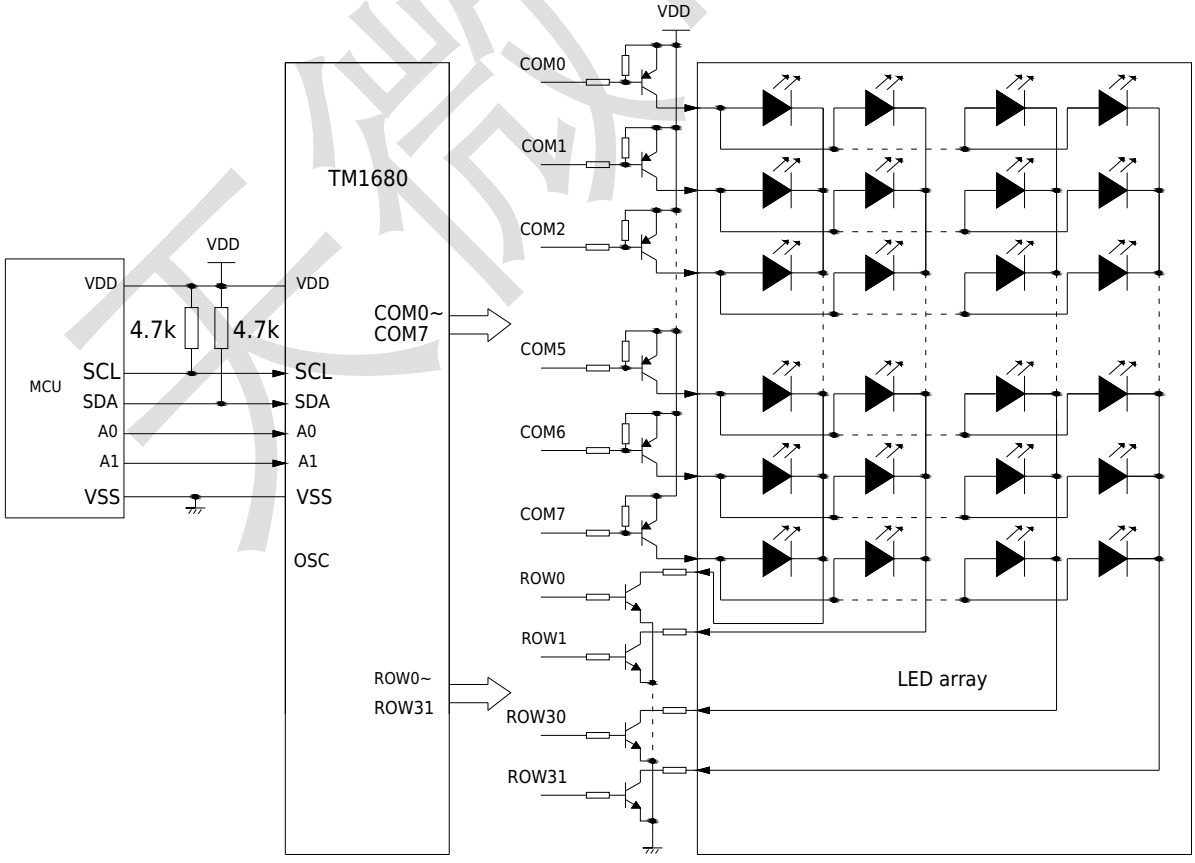


Figure 23

High power LED applications (ROW and COM plus transistor drive mode): examples of 24ROW*16COM mode 24

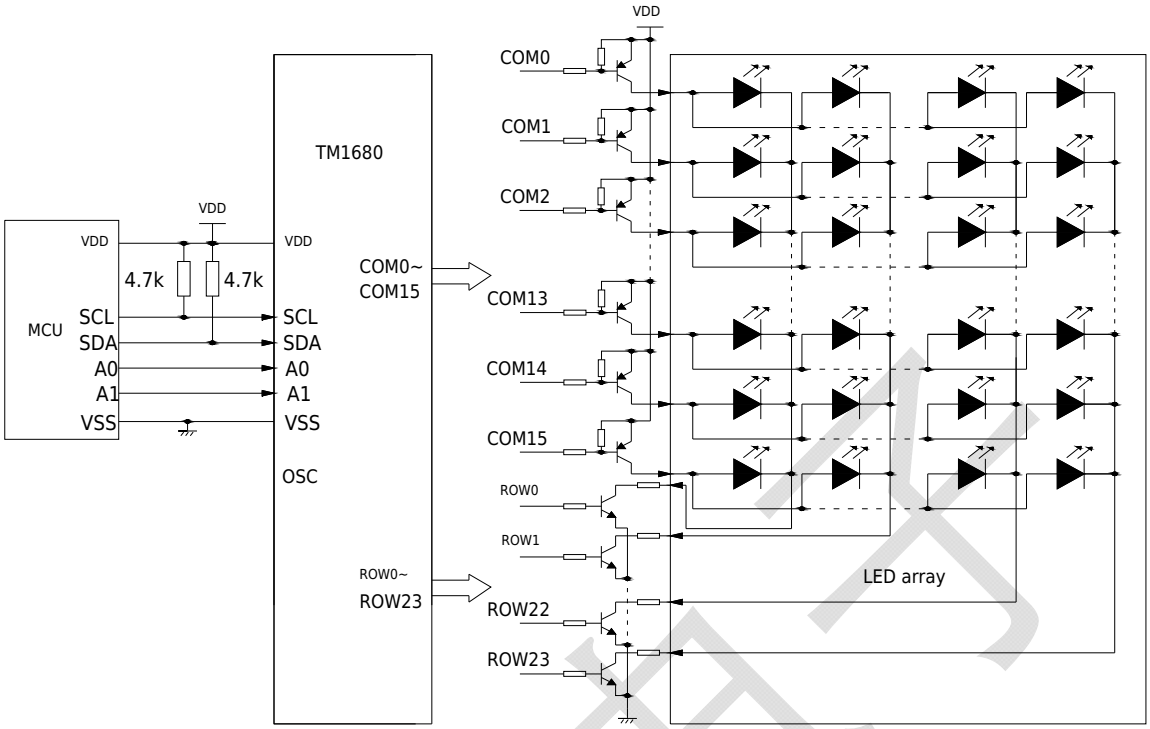


Figure 24

Cascade application (direct drive mode): 32ROW*8COM mode example diagram 25

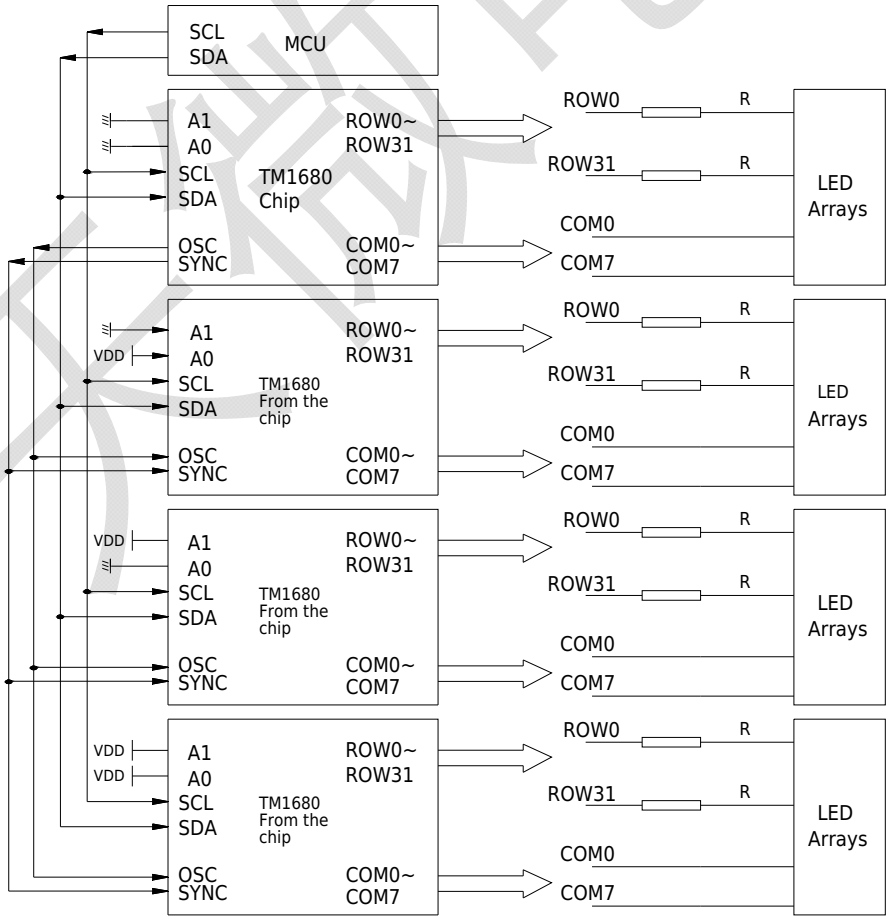


Figure 25

Cascade application (COM plus transistor drive mode): Example diagram of 32ROW*8COM mode 26

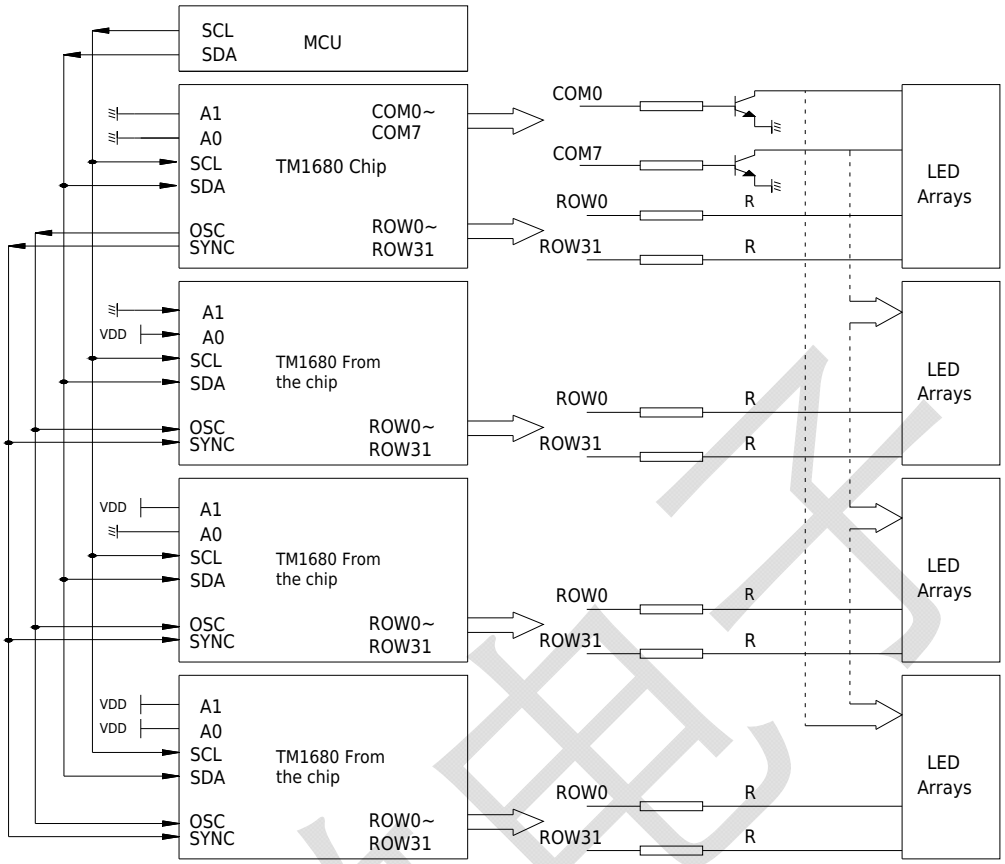


Figure 26

Cascade application (direct drive mode): examples of 24ROW*16COM mode 27

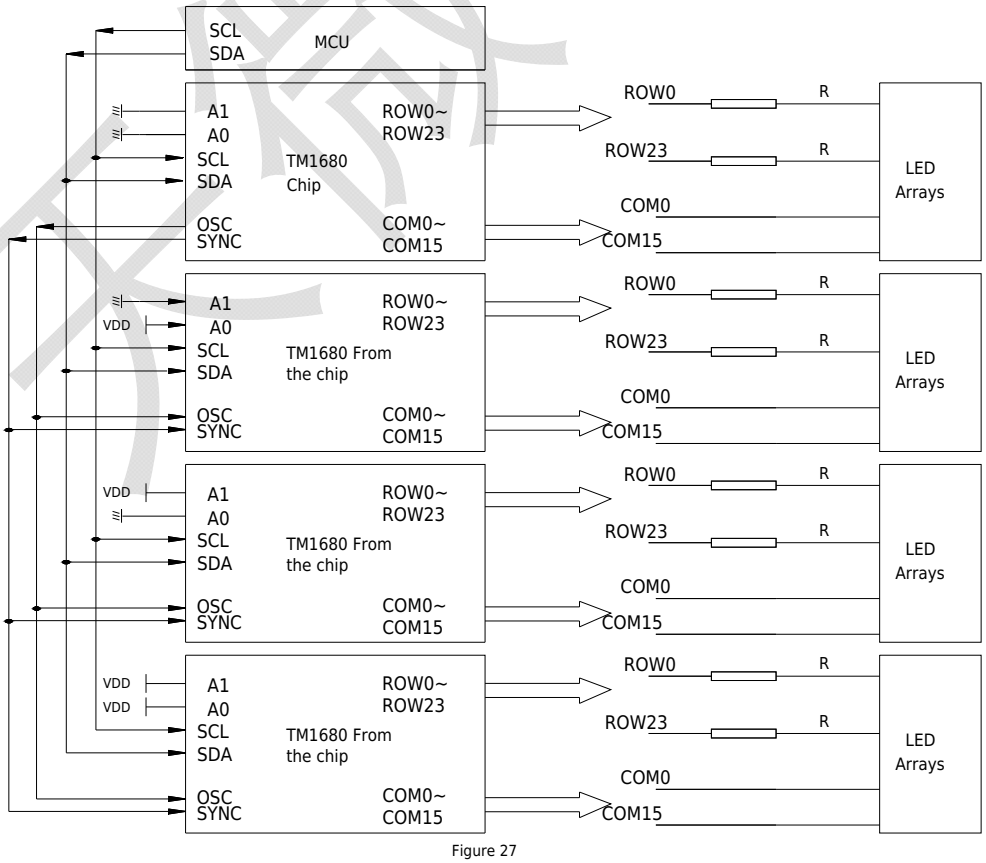


Figure 27

Cascade application (COM plus transistor drive mode): examples of 24ROW*16COM mode 28

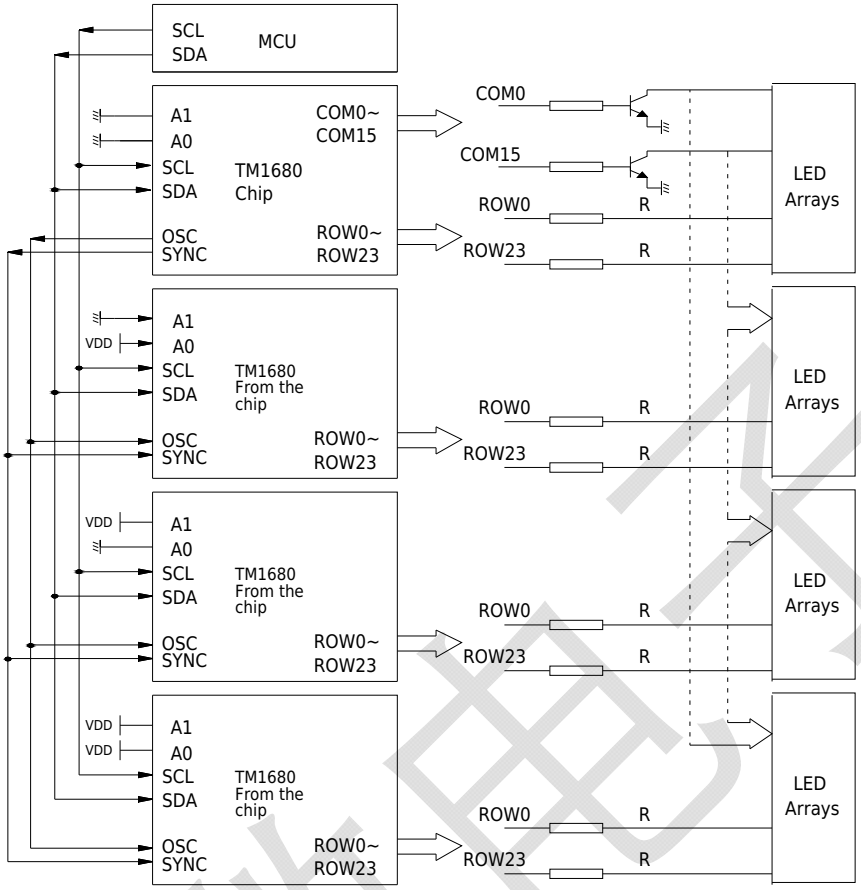
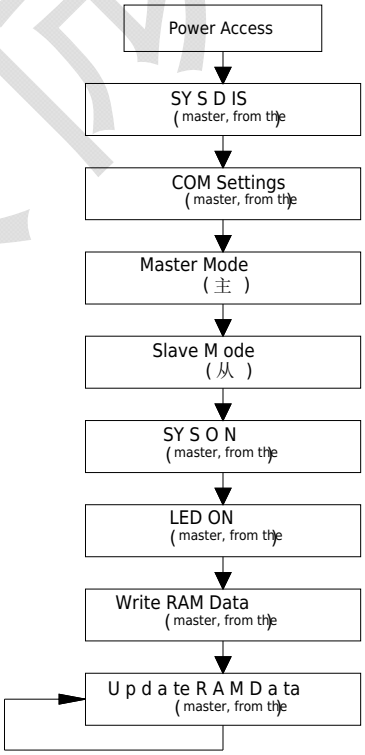


Figure 28

General design flow chart

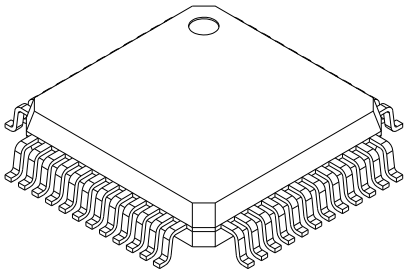


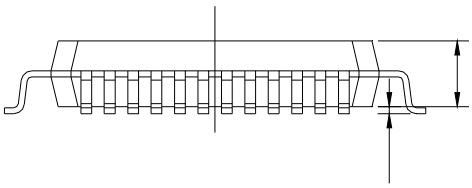
Command overview table:

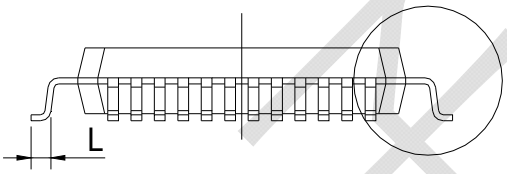
Command Name	Command Code	D/C	Description of the function	Default
WRITE	1110-01A1A0	D	Write the address of the slave machine	
Data Address (I2C)	0 A6 A5 A4 A3 A2 A0	D	Write RAM Address	
The data format (I2C)	D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	D A3-A0 high 4 bits, B3-B0 low 4 bits		
SYS DIS	1000-0000	C shuts off system clock and LED loop √		
SYS EN	1000-0001	C	Turn on the system oscillator	
LED OFF	1000-0010	C	Turn off LED loop	√
LED ON	1000-0011	C	Turn on the LED loop	
BLINK OFF	1000-1000	C	Turn off the blinking function	√
Blink 2Hz	1000-1001	C	LED blinks at a frequency of 2Hz	
Blink_1Hz	1000-1010	C	LED blinks at a frequency of 1Hz	
Blink_0.5Hz	1000-1011	C	LED blinks at a frequency of 0.5Hz	
SLAVE MODE	1001-0Xxx	C external oscillation, the clock is input from the OSC pin. Synchronous signal input by SYN pin		
RC Master Mode0	1001-100X	C built-in oscillation, OSC stays low, synchronized The signal remains high at the SYN pin and should only be For Single Chip		√
RC Master Mode1	1001-101X	C internal oscillation, internal frequency at the OSC output, Synchronous signal output at SYN pin		
EXT CLK Master Mode0	1001-110X	C external oscillation, the clock is input from the OSC pin. The synchronization signal is maintained high by the SYN pin. Only referenced to a single chip		√
EXT CLK Master Mode1	1001-111X	C external oscillation, the clock is input from the OSC pin. Synchronous signal output from SYN pin		
COM Option	1010-ABXX	C when ab=00, 8COM Nmos; when ab=01, 16COM Nmos; 8COM Pmos when ab=10; 16COM Pmos when ab=11;		00
PWM Duty	1011-abcd	C abcd changes from 0-F respectively correspond 16-order luminance of 1/16—16/16 LED section		F

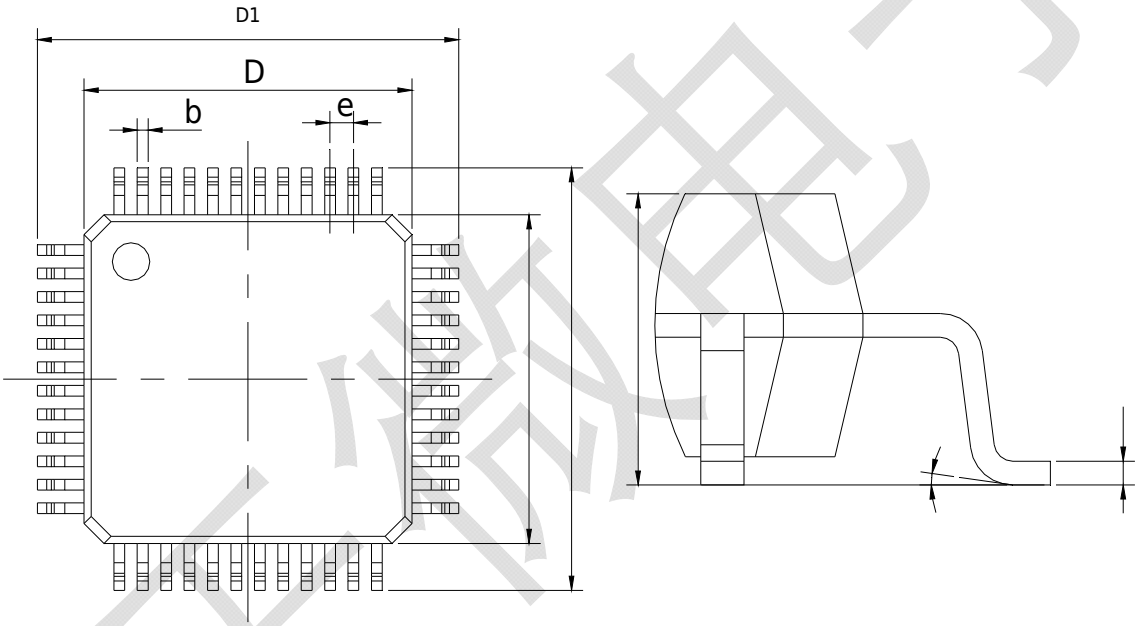
Note: 1, X does not care, it is recommended to write “0". 2, A6 ~ A0 memory address. 3, D0~D3 memory data. 4, D/C data/command mode. 5, default: the state of the chip after power-up reset

Package diagram (LQFP48 7m*7mm)



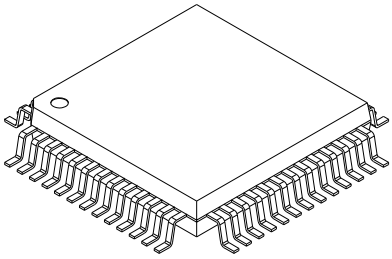


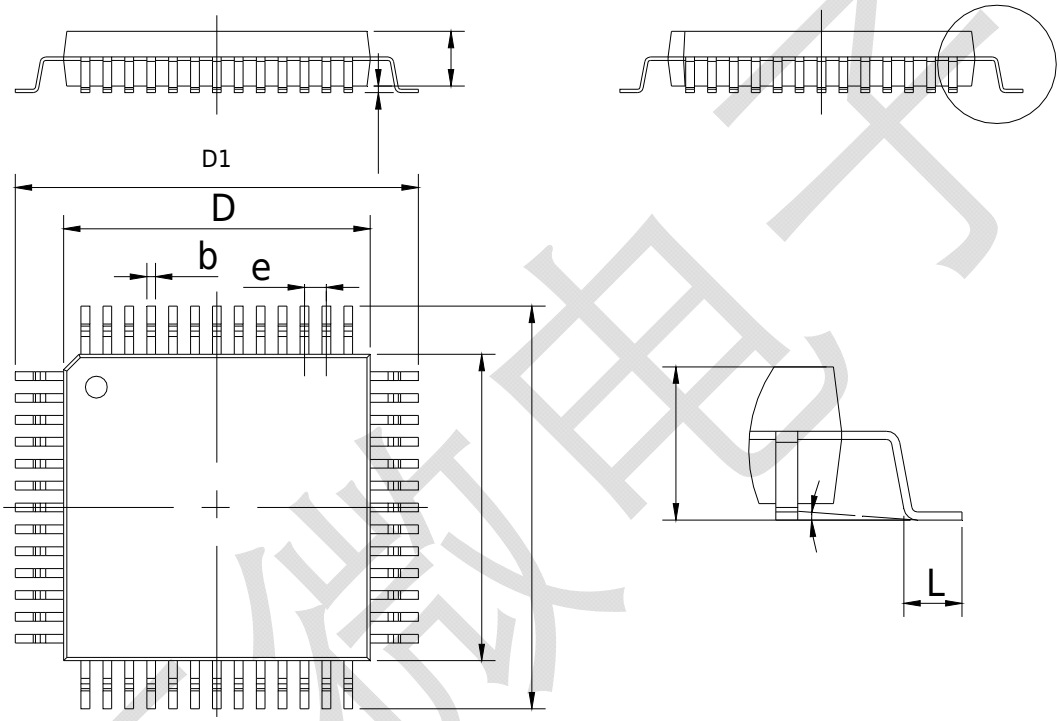




Symbol	Dimensions In Millimeters		Dimensions In Inchets	
	Min	Max	Min	Max
A		1.600		0.063
A1	0.050	0.150	0.002	0.006
A2	13.5	1.500	0.053	0.059
b	0.180	0.270	0.007	0.010
c	0.130	0.180	0.005	0.007
D	6.900	7.100	0.272	0.280
D1	8.800	9.200	0.346	0.362
E	6.900	7.100	0.272	0.280
E1	8.800	9.200	0.346	0.362
e	0.500 (BSC)		0.020 (BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	7°	0°	7°

Package diagram (QFP52 14m*14mm)





Symbol	Dimensions In Millimeters		Dimensions In Inchets	
	Min	Max	Min	Max
A	—	1.600	—	0.063
A1	0.100		0.004	
A2	133500	1.500	0.053	0.059
b	0.400 (BSC)		0.016 (BSC)	
D	13.900	14.100	0.547	0.555
D1	15.800	16.200	0.622	0.638
E	13.900	14.100	0.547	0.555
E1	15.800	16.200	0.622	0.638
e	1.000 (BSC)		0.039 (BSC)	
L	0.450	0.750	0.018	0.030
θ	0°	7°	0°	7°

All specs and applications are above subject to change withou t prior notice. (The above circuit and specifications are for reference only, if amended by the Company without prior notice)