Bryan **Orabutt**

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SKILLS

PROGRAMMING
C • Python • MATLAB • C++
OTPL • Verilog • VerilogA
Assembly • JSL

TOOLS
Cadence IC Tools • KiCAD
Calibre DRC/LVS/PEX • Git

EMBEDDED PLATFORMS
Arduino • PSoC • Raspberry Pi
Beaglebone • ESP32

EDUCATION

WASHINGTON UNIVERSITY IN ST. LOUIS
MS in Computer Engineering
May 2022| St. Louis, MO

SOUTHERN ILLINOIS UNIVERSITY EDWARDSVILLE
MS in Electrical Engineering
August 2018 | Edwardsville, IL

BS in Computer Engineering
December 2015 | Edwardsville, IL

INTERESTS

I am an engineer at heart and love to make things. I enjoy embedded programming, circuit design, and 3D printing.

You can also often find me playing board games and table top RPGs with friends, or out foraging for wild mushrooms.

EXPERIENCE

INTEL | Product Development Engineer
Jan 2022 - Present | Hillsboro, OR

- Developed OTPL test programs for sorting singulated die. Collected and analyzed data for performing failure analysis and feeding back into the foundry for process improvements.
- Developed a python script for automating OTPL test plan generation to reduce test time across multiple products.

SOUTHERN ILLINOIS UNIVERSITY EDWARDSVILLE | Lecturer
August 2018 – December 2018 | Edwardsville, IL

- Prepared and delivered lecture material to over 80 students across two courses: *Intro to Electronics* and *Intro to VLSI Design* courses.

RESEARCH

WUSTL RADIOCHEMISTRY LAB | Doctoral Research
Jan 2019 – Jan 2022 | St. Louis, MO

- Worked with **Dr. Roger Chamberlain** and **Dr. Lee Sobotka** to develope Verilog-A models to simulate new mixed-mode pulse processing electronics.
- Supported the development of new iterations on existing pulse processing electronics for particle identification and heavy ion energy measurements.

SIUE VLSI DESIGN LAB | Master's Research
Jan 2016 – August 2018 | Edwardsville, IL

- Worked with **Dr. George Engel** to devlop a new analog ASIC for detecting the onset of radiation at a scintillator detector.
- Engaged in all aspects of the development: from design, schematic entry, simulation, layout, and final testing of the packaged silicon.

ACADEMIC PROJECTS

ML ACCELERATOR | Cadence Encounter, Verilog, C
Washington University in St. Louis

- Designed a machine learning accelerator for the MNIST data set comprised of multiple pipelined multiply accumulator units with an input/output RAM.
- Wrote a C program to model and train the neural network, obtaining the weight matrices for testing the accelerator design.

REAL-TIME GPIO INTERRUPT | Raspberry Pi, C, Linux, PSoC
Southern Illinois University Edwardsville

- Developed a project to reduce IRQ latency on the Raspberry Pi GPIO using a kernel driver and user space library.
- The user space library uses a character device to cause blocking reads until a GPIO interrupt is detected.
- The kernel driver uses a FIFO with real time scheduling to schedule IRQ handlers for each GPIO request, alerting user space via the character device.

PUBLICATIONS

[1] B. Orabutt, R. D. Chamberlain, J. Elson, G. Engel, F. Delaunay, and L. G. Sobotka. Design of mixed-mode systems for pulse-shape discrimination. In *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 990–994, 2021.