Scheduling - Part I (MIEIC - Compilers - 2021)

* This form will record your name, please fill your name.

1. The scheduling phase must be done after the register allocation

   - ◯ Yes
   - ◯ No

2. The selection of instruction does not influence the scheduling

   - ◯ Yes
   - ◯ No

3. Consider the low-level IR of statement A[i] = A[i]*c;
   t1=4*i; //i1 (//i1)
   t2=A+t1; //i2 (//i2)
   t3=MEM[t2]; //i3 (//i3)
   t4=t3*c; //i4 (//i4)
   MEM[t2]=t4; //i5 (//i5)
   (where A represents the base address of the array A, i and c represent local variables, and t's represent auxiliary/temporary variables)
   Consider a target CPU with two units, one ALU (*, +, etc.) and one LOAD/STORE (LD/ST) unit. All ALU operations and ST require 1 clock cycle, and LD requires 2 clock cycles (after 1 cycle another LD operations can be scheduled to the LD/ST unit).
   Using List scheduling assign the operations of the IR to the respective cycle and unit (don't forget that first you should draw a DDG):

	ALU	LD/ST
Cycle 1		
Cycle 2		
Cycle 3		
Cycle 4		
Cycle 5		
Cycle 6		
Cycle 7		

4. If the target CPU can only execute a maximum of one operation per cycle (i.e., ALU cannot execute operations in parallel with the LD/ST unit), how many clock cycles would be needed to execute the code of the IR of the previous question?

   ◯ 6

   ◯ 5