



# Design of an open source AED in the framework of the UBORA project

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The objective of this thesis is the development of an open source Automated External Defibrillator (AED), in the framework of UBORA project.

UBORA is a EU founded project that aims at creating an European Union-Africa e-Infrastructure, for open source co-design of new solutions to face the current and future healthcare challenges of both continents.

In this context the open source approach grants various advantages, among which: safer devices, less development costs, needs based devices, improved design, and the use of the projects as a teaching instrument.

Sudden Cardiac Arrest (SCA) is a condition in which the heart suddenly and unexpectedly stops beating in an ordered fashion way, and instead start exhibiting a chaotic behaviour. When this happens, blood stops flowing to the brain and other vital organs. In these conditions the patient may be considered to all effects dead, and will remain so unless someone help him/her immediately. SCA is a very dangerous condition, responsible every year for over 300'000 deaths in United States [1].

The most effective way to treat a SCA is with defibrillation, namely a therapeutic dose of electrical energy. The necessity of performing defibrillation as soon as possible -in order to significantly raise the chance of resuscitation- has led to the development of AEDs.

AEDs are portable devices capable of automatically diagnose whether a patient is experiencing SCA or not, and treat him/her through defibrillation when needed. The critical aspect of AEDs is the easiness of use that allows the operation with a very basic training. This, coupled with a capillary diffusion, could drastically reduce the number of deaths for SCA.

The goal of this thesis therefore, was the development of an Open-source Automated External Defibrillator, named OAED. The device was designed keeping in mind: compliance with the regulatory standards required to obtain the CE marking; the necessity of using it as a teaching instrument; the low costs required for a greater diffusion; and competitiveness with the existing devices, in terms of efficiency, reliability, and safety.

Defibrillation is usually schematized as a RC circuit, in which the capacitor is the element that stores the defibrillation energy, and the patient is modelled with a resistor. As shown in Equation 1, the amount of energy released into the patient depends on its resistance, and the capacitor.

$$\begin{aligned} U &= \int_0^T (i(t) \cdot v(t)) \partial t = \frac{V_0^2}{Z} \cdot \left[ -\frac{Z \cdot C}{2} \cdot e^{\frac{-2t}{ZC}} \right]_0^T \\ &= \frac{V_0^2 \cdot C}{2} \cdot \left( 1 - e^{\frac{-2T}{ZC}} \right) \end{aligned} \quad (1)$$

However the only parameter we can actively modify to modulate defibrillation is the discharge time  $T$ , given by Equation 2.

$$\begin{aligned} U &= \frac{V_0^2 \cdot C}{2} \cdot \left( 1 - e^{\frac{-2T}{ZC}} \right) \Rightarrow \frac{2U}{V_0^2 \cdot C} = 1 - e^{\frac{-2T}{ZC}} \Rightarrow \\ \Rightarrow T &= -\frac{ZC}{2} \cdot \ln \left[ 1 - \frac{2U}{V_0^2 \cdot C} \right] \end{aligned} \quad (2)$$

The basic RC model can be improved in different ways. In particular, many researches evinced that inverting the defibrillation polarities during the release lead to a considerable

improvement of the resuscitation chances, with the side effect of also requiring less energy [2, 3, 4].

According to EEC medical devices directive 93/42 (MDD 93/42), AEDs belongs in class *I Ib*. This means that they need a notified body to verify them during the design and production phase for obtaining the CE marking for commercialization in European Union.

The AEDs related standards are mainly in the family of IEC 60601. Amongst these, the most important are the: 60601-1, which is about the *general requirements for basic safety and Essential Performance of medical electrical equipments and systems*; and the 60601-2-4, that contains the *particular requirements for the safety of cardiac defibrillators and cardiac defibrillators monitors*. The rules resulting from the analysis of these norms represents the Essential Requirements from which OAED design process started.

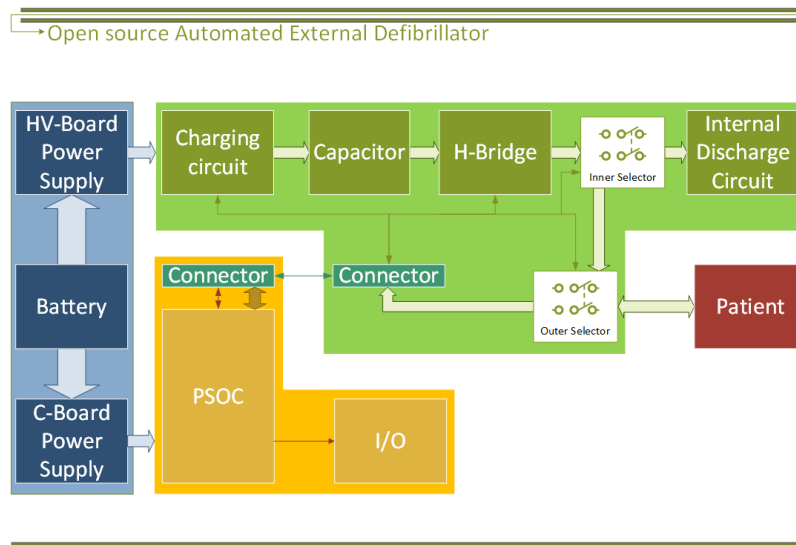


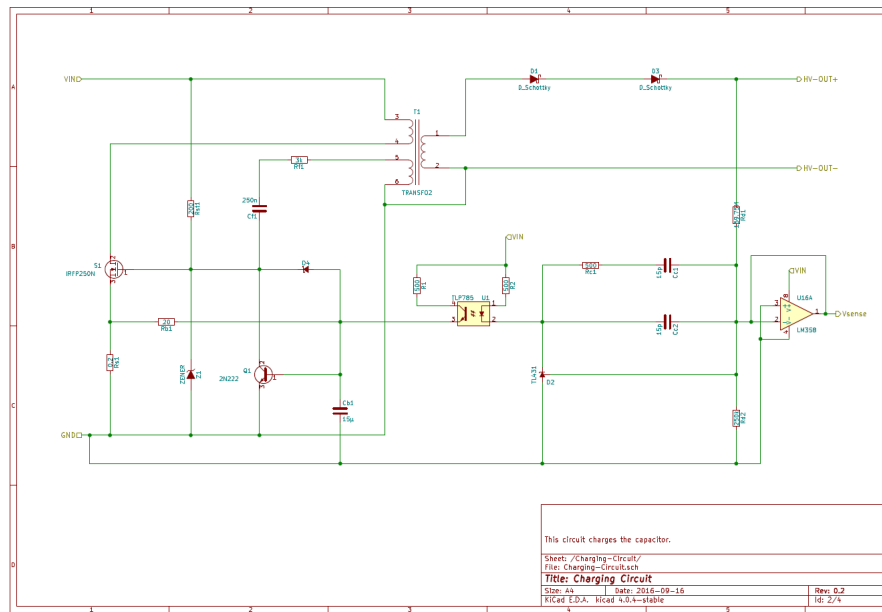
Figure 1: OAED block diagram

I started outlining a conceptual scheme (shown in Figure 1). There are two separate boards powered by a battery: the High-Voltage Board (HV-B) -highlighted in green, and the Control Board (C-B) -which is the yellow one.

The first contains all the circuitry necessary to perform defibrillation. This includes: a capacitor, used to store the energy to release; a charging circuit, that rapidly charges the capacitor; an H-Bridge circuit, used to perform biphasic -or polyphasic- defibrillation; an internal discharge circuit, used to dump the unused residual energy; and two selectors, used to isolate the patient from the capacitor, and to route the ECG signal to the C-B.

In the High-Voltage Board design, particular attention was dedicated to the charging circuit. I modified a flyback converter circuit, to obtain a custom Ringing Choke Converter (RCC) (Figure 2). The numerical simulations made with LTspice shown that the RCC I designed is capable of efficiently charging the  $150\mu F$  capacitor to a voltage of  $1700V$  in under 6 seconds.

The second critical circuit in the HV-B is the H-Bridge, used to obtain the biphasic defibrillation waveform. Although this is a well-known circuit, it required some special attention to handle rapid current changes at high voltages. Every switch of the classic H-Bridge design has been implemented with two IGBTs in order to improve safety and performances, and at the same time keep the costs low. Furthermore, because of the high-voltage across every IGBT, each of them required a driving circuit composed by an optical coupler and an

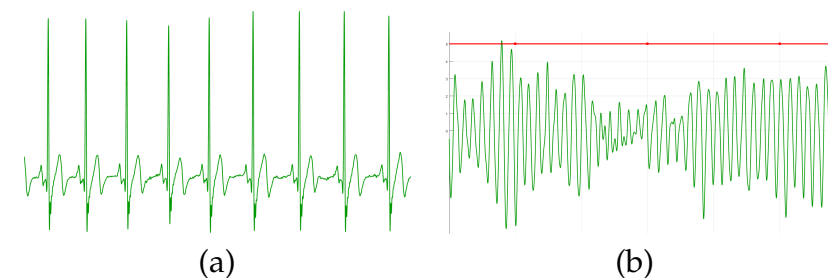


isolated power supply.

The Control Board instead, can be seen as the device *brain*. It contains a Programmable System on Chip (PSoC), which -amongst other functions- integrates the whole analogical front-end used to obtain the Electrocardiogram (ECG) and impedance acquisitions. The PSoC also contains an ARM Cortex-M3 CPU which is used to analyse the signals and assert the defibrillation needs.

Since the main focus of AEDs is the ease of use, only one couple of electrodes can be applied on the patient. Therefore ECG and impedance acquisitions share the same electrodes. Impedance measurement is a very critical aspect in AEDs, because it is used to assert if a patient is connected to the device, and to calculate the discharge time required to release a precise amount of energy into the patient.

The acquisition chain includes a buffered  $\Delta\Sigma$ -ADC that samples the patient signal at a sampling frequency of  $4000\text{sp/s}$ , with a  $16\text{bit}$  resolution. The signal is collected by three different DMAs (Direct Memory Access): one for the ECG, one for impedance, and one for the raw signal -which is mostly used for debug purpose. The ECG and impedance signals are digitally filtered in the PSoC Digital Filter Block before being sent into the SRAM. Once there, the ECG is decimated to match a sampling frequency of  $500\text{sp/s}$ , and stored in 4 seconds arrays. An example of ECG signal obtained using the development board of OAED is showed on Figure 3 (a).



The PSoC, has been programmed with a specific firmware. This acts as a finite-state machine in which each state depends on the occurrence of specific events. When entering a state, the firmware enable or disable certain circuits, depending on the state itself. The firmware also integrates five different algorithms used for SCA diagnosis: Threshold Crossing Intervals [5], VF filter [6], Threshold Crossing Sample Count [7], Phase Space Reconstruction [8], and Hilbert Transform algorithm [9]. These have been evaluated and tested using a special dataset of pathological ECG (Figure 3 (b)) obtained from the PhysioNet database [10].

The whole designing phase has been done following the ERs defined in the regulatory analysis. The design is mostly compliant with the standards defined by the 60601. However tests are needed for the experimental validation of HV-B; and for the SCA recognition algorithms, due to the fact that the norm requires a huge amount of data that was not readily available.

Finally, OAED will be used as a template for the development of UBORA e-infrastructure, and to design new open devices compliant with MDD 93/42 and ISO standards.

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