Tutorial sheet - 10 IEC103

(Q1) Determine the Q point of the transistor circuit shown in Fig. Q1 below. Also draw the DC load line.

Given that $\beta (h_{FE}) = 200$ and $V_{BE} = 0.7V$

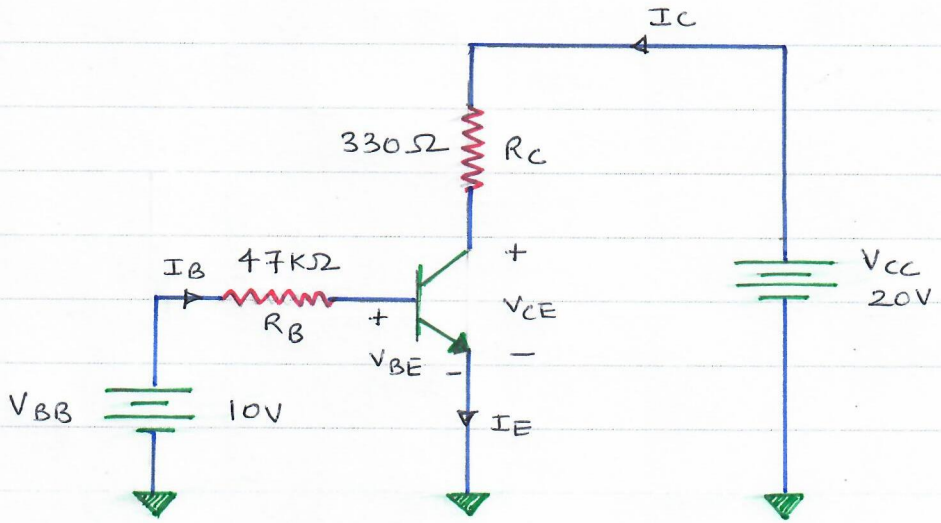

Fig. Q1

(Q2) Find the Q-point of the base-bias transistor circuit shown in Fig. Q2. Also, construct the DC load line and plot the Q-point from the values obtained. Determine, whether the circuit is mid-point biased.

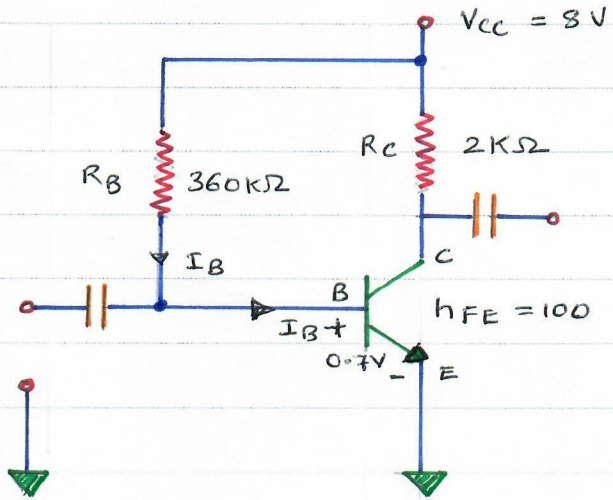

Fig. Q2

Q3 Determine the values of I_{CQ} and V_{CEQ} of the circuit shown in Fig. Q3 using voltage divider bias. Calculate the exact value of the Q point.

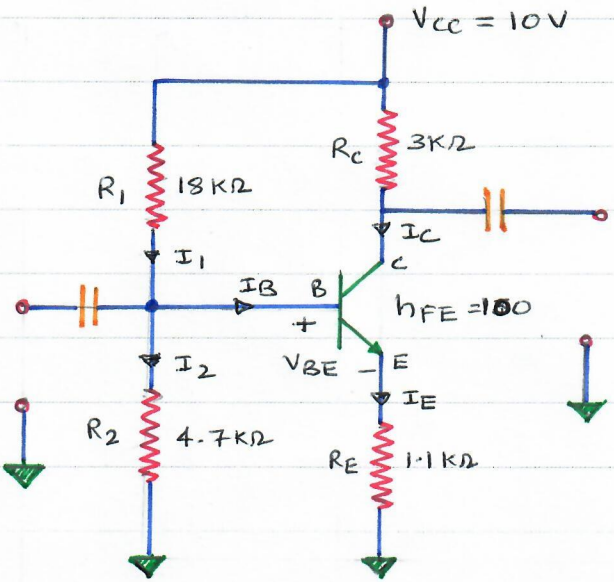

Fig. Q3

Q4 For the same circuit shown in Fig. Q3 (from previous question), calculate the approximate value of Q-point using the assumption $I_2 > 10 I_B$.

(Q5) Figures Fig Q5a), Q5b) and Q5c) show CE, CB, and CC amplifiers respectively with typical biasing schemes used, Establish the quiscent point for each circuit.

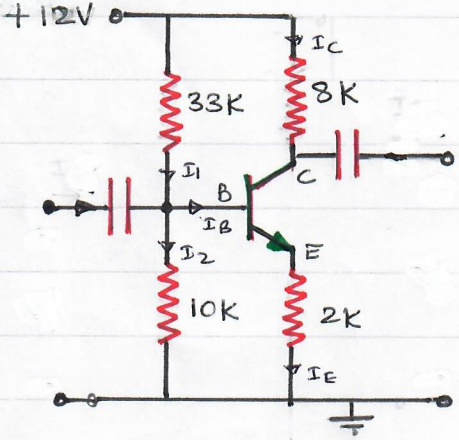

Fig Q5a)

(CE)

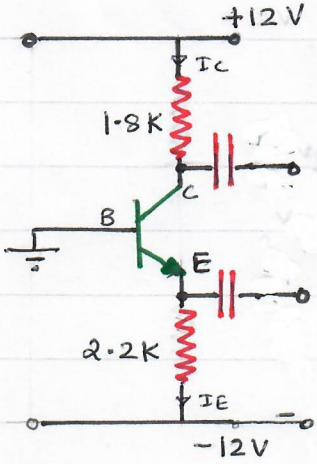

Fig Q5b)

(CB)

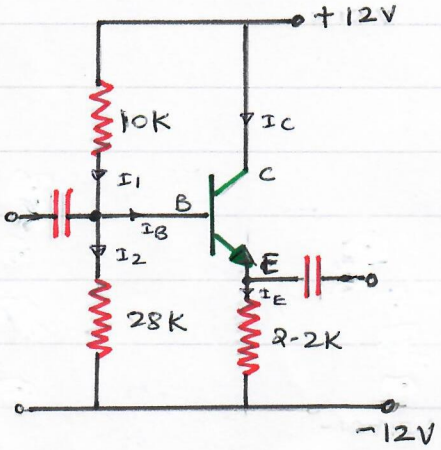

Fig Q5c)

(CC)

Take $V_{BE} = 0.7V$. Use the assumption that $I_2 > 10I_B$ in case of voltage divider bias