Solutions to Tutorial sheet-10 IEC103

Q1 Determine the Q point of the transistor circuit shown in Fig. Q1 below. Also draw the DC load line.

Given that $\beta$ ($h_{FE}$) = 200 and $V_{BE}$ = 0.7V

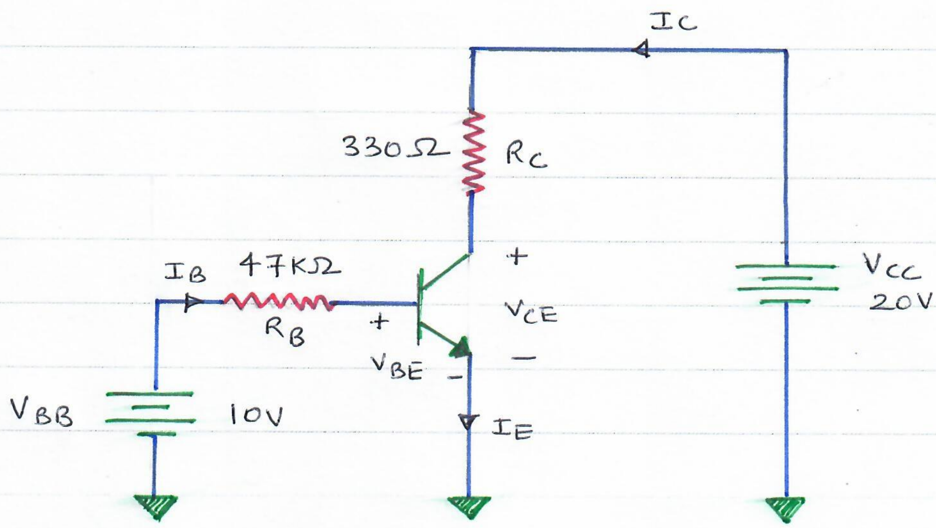



Fig. Q1

Sol. Q point is $(V_{CE}, I_C)$

Applying KVL around the input circuit (loop), we have

$$-V_{BB} + I_B R_B + V_{BE} = 0$$

$$\Rightarrow \quad I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$$= \frac{10 - 0.7}{47K} = \frac{9.3}{47K} = 197.9\ \mu A$$

$$I_C = \beta I_B = 200 \times 197.9\ \mu A = 39.58\ mA$$

Applying KVL around output circuit (loop), we have

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

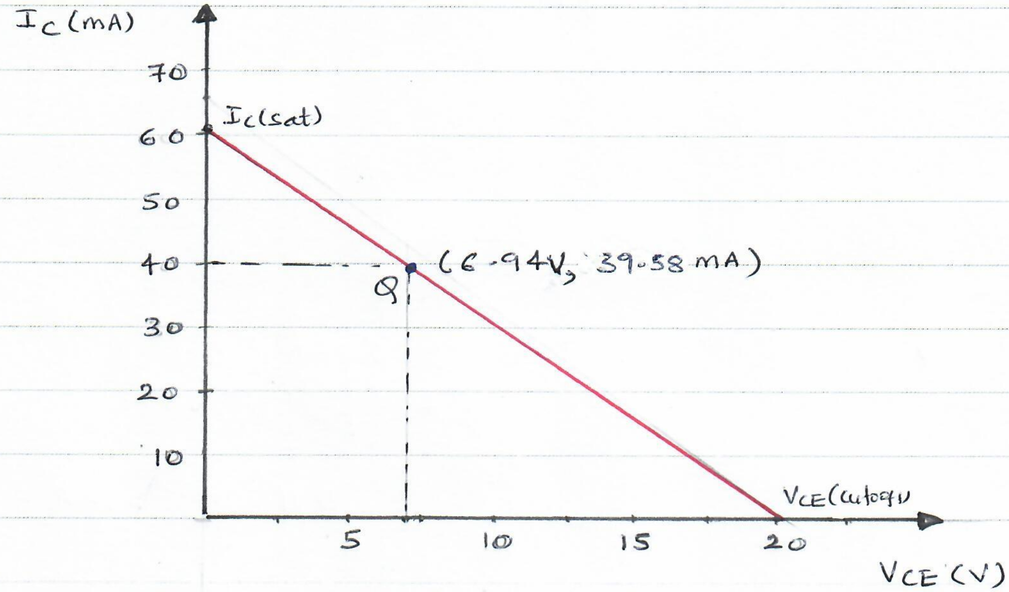
$$\Rightarrow \quad V_{CE} = V_{CC} - I_C R_C = 20 - 39.58 \times 10^{-3} \times 330 = 6.94\ V$$

∴ Q point is $(6.98V, 39.58\ mA)$.

For DC load line we need to calculate $V_{CE}$ (cut-off) and $I_C$(sat)

$$V_{CE}(\text{cutoff}) = V_{CC} = 20V, \qquad I_C(\text{sat}) = \frac{V_{CC}}{R_C} = \frac{20}{330} = 60.6\ mA$$

The DC load line along with the location of operating point is as shown below.



(Q2) Find the Q-point of the base-bias transistor circuit shown in Fig. Q2. Also, construct the DC load line and plot the Q-point from the values obtained. Determine, whether the circuit is mid-point biased.

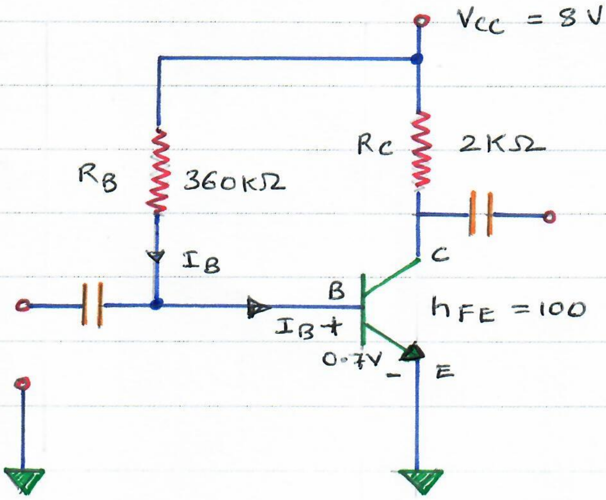



Fig. Q2

Sol:

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow \quad I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{8 - 0.7}{360K} = 20.28 \mu A$$

$$I_C = h_{FE} I_B = 100 \times 20.28 \ \mu A = 2.028 \ mA$$

$$V_{CE} = V_{CC} - I_C R_C = 8 - 2.028 \times 10^{-3} \times 2 \times 10^{3}$$

$$= 8 - 2.028 \times 2 = 3.94 \ V$$

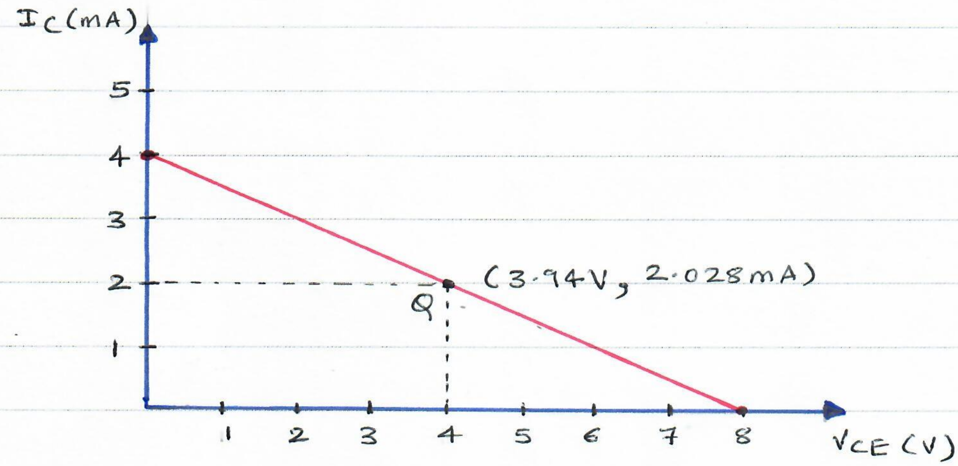
For DC load line we need to calculated $I_C(sat)$ and $V_{CE}(cutoff)$

$$I_C(sat) = \frac{V_{CC}}{R_C} = \frac{8}{2K} = 4 mA$$

$$V_{CE}(off) = V_{CC} = 8V$$

The DC load line along with Q-point is as shown - in next page

Q-point is (3.94V, 2.028 mA)




The Q-point is almost the midpoint of the DC load line.

∴ The circuit is midpoint biased.

(Q3) Determine the values of $I_{CQ}$ and $V_{CEQ}$ of the circuit shown in Fig. Q3 using voltage divider bias.
Calculate the exact value of the Q point.

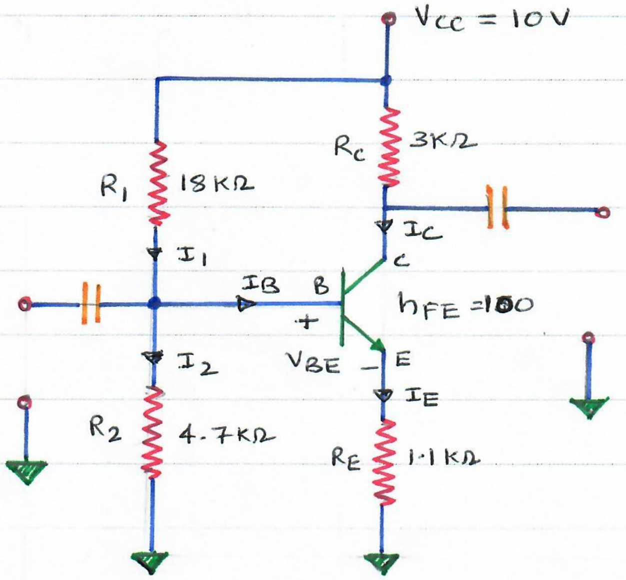


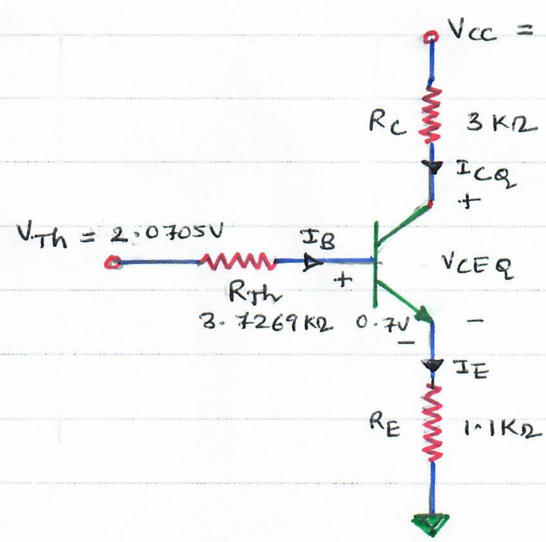

Fig. Q3

Sol. Thevenize the voltage-divider biase circuit.

$$V_{Th} = \frac{V_{CC} \times R_2}{R_1 + R_2} = 10 \times \frac{4.7K}{18K + 4.7K} = 2.0705\ V$$

$$R_{Th} = R_1 \| R_2 = \frac{4.7K \times 18K}{4.7K + 18K} = 3.7269\ K\Omega$$

The Transistor circuit with Thevenized voltage-divider circuit is as shown below




$h_{FE} = \beta = 100$

$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$

$\Rightarrow V_{Th} - I_B R_{Th} - V_{BE} - (\beta+1) I_B R_E = 0$

$\Rightarrow I_B (R_{Th} + (\beta+1) R_E) = V_{Th} - V_{BE}$

$$\Rightarrow I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1) R_E}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta+1)R_E} = \frac{2.0705 - 0.7}{3.7269K + (100+1)*1.1K}$$

$$= \frac{1.3705}{114.83K}$$

$$= 11.935 \mu A$$

$$I_C = h_{FE} I_B = 100 \times 11.935 \mu A = 1.1935 \text{ mA}$$

$$V_{CEQ} = V_{CC} - I_C R_C - I_E R_E$$

$$= 10 - 1.1935m \times 3K - \frac{(100+1)}{100} I_C R_E$$

$$= 10 - 1.1935m \times 3K - \frac{101}{100} \times 1.1935m \times 1.1K$$

$$= 10 - 1.1935 \times 3 - \frac{101}{100} \times 1.1935 \times 1.1$$

$$= 10 - 3.5805 - 1.326 = 5.0935V$$

The Q point is $(5.0935V, 1.1935mA)$

Q4 For the same circuit shown in Fig. Q3 (from previous question), calculate the approximate value of Q-point using the assumption $I_2 > 10 I_B$.

Sol.

$$V_B = \frac{V_{CC} \times R_2}{(R_1 + R_2)} = \frac{10 \times 4.7K}{18K + 4.7K}$$

$$= \frac{10 \times 4.7}{22.7} = 2.0705V$$

$$V_E = V_B - V_{BE} = 2.0705 - 0.7 = 1.3705V$$

$$I_E = \frac{V_E}{R_E} = \frac{1.3705}{1.1K} = 1.2459 \text{ mA}$$

$$I_C = \frac{h_{FE}}{(1+h_{FE})} \times I_E = 1.2336 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 10 - 1.2336 \times 10^{-3} \times 3 \times 10^{3} - 1.2459 \times 10^{-3} \times 1.1 \times 10^{3}$$

$$= 10 - 1.2336 \times 3 - 1.2459 \times 1.1$$

$$= 4.9287 \text{ V}$$

$\therefore$ Q-point is (4.9287 V, 1.2336 mA)

(Q5) Figures Fig Q5a), Q5b) and Q5c) show CE, CB, and CC amplifiers respectively with typical biasing schemes used. Establish the quiscent point for each circuit.

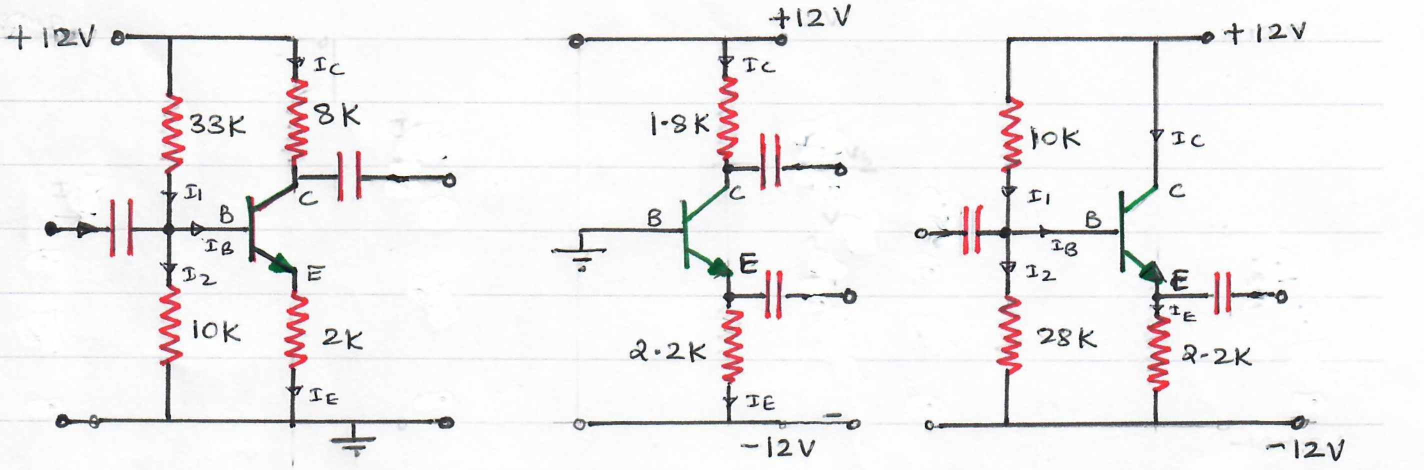



Fig Q5a) (CE) | Fig Q5b) (CB) | Fig Q5c) (CC)

Take $V_{BE} = 0.7V$. Use the assumption that $I_2 > 10 I_B$ in case of voltage divider bias

Sol. i) CE configuration (Fig Q5a)

$$V_B = \frac{12 \times 10K}{10K + 33K} = \frac{12 \times 10}{43} = 2.79\,V$$

$$V_E = V_B - V_{BE} = 2.79 - 0.7 = 2.09\,V$$

$$I_E = \frac{V_E}{2K} = \frac{2.09}{2K} \simeq 1mA$$

$$I_C \simeq I_E = 1mA$$

$$V_C = 12 - I_C \times 8K = 12 - 1m \times 8K = 12 - 8 = 4V$$

$$V_{CE} = V_C - V_E = 2.09 - 4 = 2.09 \simeq 2V;$$

$$I_C = 1mA$$

∴ Quiscent point is $V_{CE} \simeq 2V$ and $I_C \simeq 1mA$

ii) CB configuration ( Fig Q5 b)

$V_B = 0$ since base is grounded

$V_{BE} = 0.7 \Rightarrow V_B - V_E = 0.7$

$\Rightarrow V_E = -0.7\,V$

$$I_E = \frac{V_E - (-12)}{2.2K} = \frac{-0.7+12}{2.2K} = \frac{11.3}{2.2K} = 5.13\,mA$$

$$I_C \simeq I_E$$

$$V_C = 12 - I_C \times 1.8K$$

$$= 12 - 5.13m \times 1.8K$$

$$= 12 - 5.13 \times 1.8$$

$$= 2.8\,V$$

$$V_{CE} = V_C - V_E = 2.8 - (-0.7) = 3.5\,V$$

Quiscent point $V_{CE} = 3.5\,V$ ; $I_C = 5.13\,mA$

iii) CC configuration ( Fig 5 c)

Please note that there two DC sources $V_{CC} = 12V$ and $V_{EE} = -12V$

$$V_B = \frac{12 \times 28K}{28K+10K} - \frac{12 \times 10K}{28K+10K}$$

$$= 8.84 - 3.158 = 5.68\,V$$

$$V_E = V_B - V_E = 5.68 - 0.7 \simeq 5\,V$$

$$I_E = \frac{V_E - (-12)}{2.2K} = 7.7\,mA \simeq I_C$$

$$V_{CE} = 12 - V_E = 12 - 5 = 7\,V$$

Quiscent point $V_{CE} = 7V$; $I_C = 7.7\,mA$