

NEW YORK INSTITUTE OF TECHNOLOGY

SPRING 2019

**Introduction to VLSI Design**

CSCI 660 SECTION M01

Meeting Day: Friday

**INSTRUCTOR:** Prof. Hakan Pekcan

**STUDENT:** Daniel M. Wong (1249022), Christopher De Leon (0668599)

**Final Design Project:** **Sequence Generator Written In VHDL**

**Submission Date:** 5/3/2019

Table of Contents

[Objective 1](#_Toc7789924)

[VHDL Implementation 2](#_Toc7789925)

[FiniteStateMachine 2](#_Toc7789926)

[Library 2](#_Toc7789927)

[Entity 2](#_Toc7789928)

[Architecture 2](#_Toc7789929)

[SYNC 7](#_Toc7789930)

[Library 7](#_Toc7789931)

[Entity 8](#_Toc7789932)

[Architecture 8](#_Toc7789933)

[PLL 11](#_Toc7789934)

[Library 11](#_Toc7789935)

[Entity 11](#_Toc7789936)

[Architecture 12](#_Toc7789937)

[Vector Waveform Synthesis 14](#_Toc7789938)

[RTL Viewer 14](#_Toc7789939)

[State Machine Viewer 14](#_Toc7789940)

[Altera DE1 Pin Assignments 15](#_Toc7789941)

# Objective

The objective of this design project is to create a simple project using any/all knowledge of VHDL learned in class. The project chosen will be a 4-bit finite state machine (FSM) composed of 16 states (0 to 15). Each state will be shown on a computer monitor over VGA as well as on LEDs. Each state has a unique output that will be displayed on 4 8-segment displays that will be transitioned to after every second if an enable switch is on. A display switch is used to switch between the unique output or the current time and state number. This should be tested on an FPGA board (ex. Altera DE1 board) after appropriate pin assignments.

# VHDL Implementation

The following are screenshots of the three VHDL files used to accomplish the tasks in Objective.

## FiniteStateMachine

### Library



Figure – The libraries used to run FiniteStateMachine.

### Entity

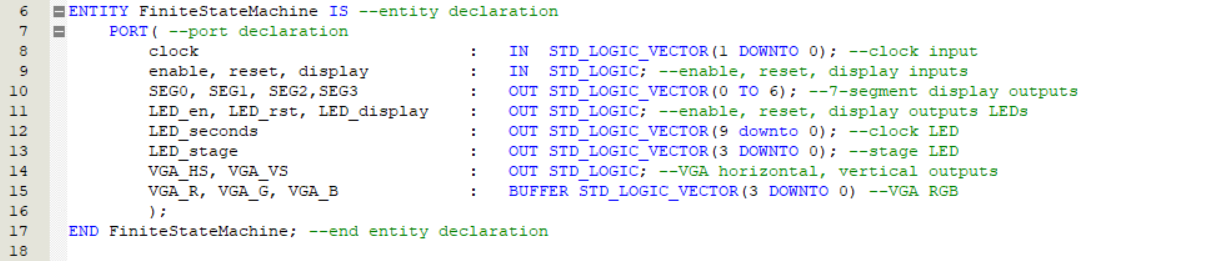


Figure – The entities used to run FiniteStateMachine.

### Architecture

#### Signals / Variables



Figure – The signal and/or variables used to run FiniteStateMachine.

#### Components

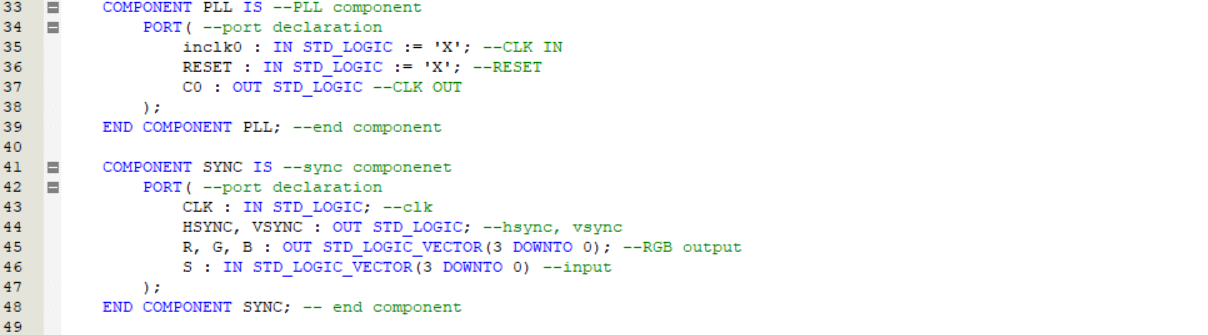


Figure – The components used to run FiniteStateMachine.

#### Function

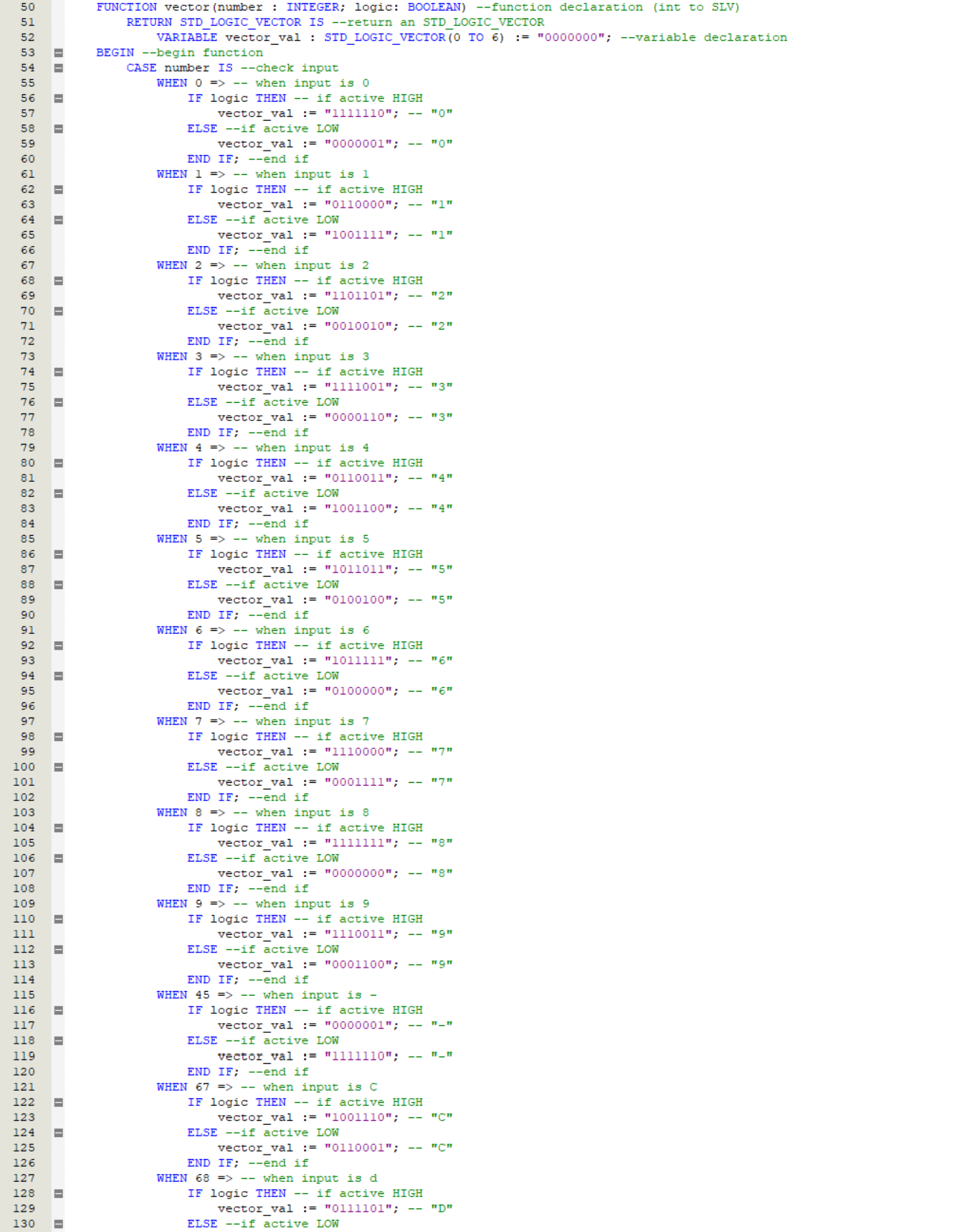


Figure – The components used to run FiniteStateMachine (1/2).

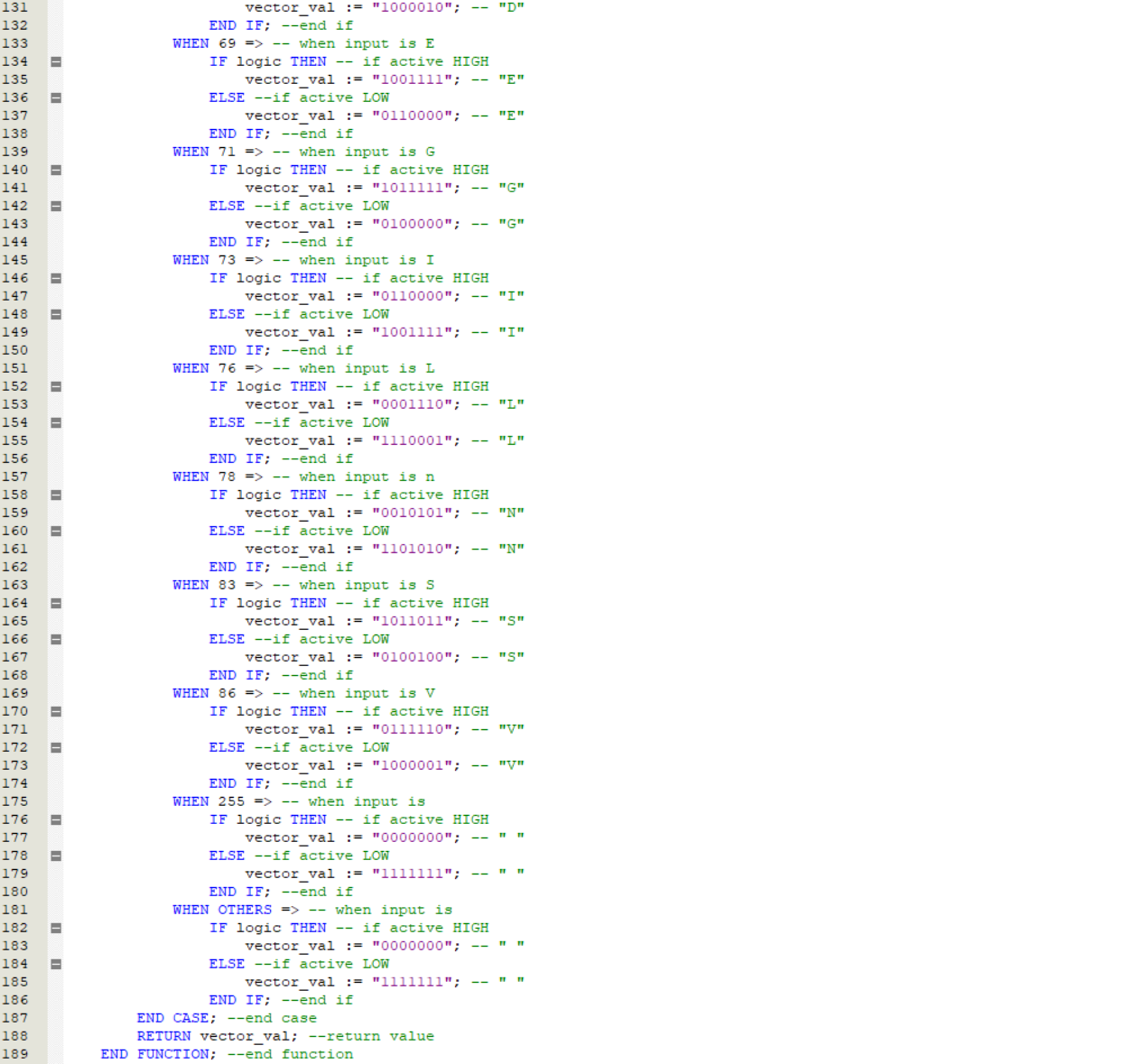


Figure – The components used to run FiniteStateMachine (2/2).

#### Process 1: State

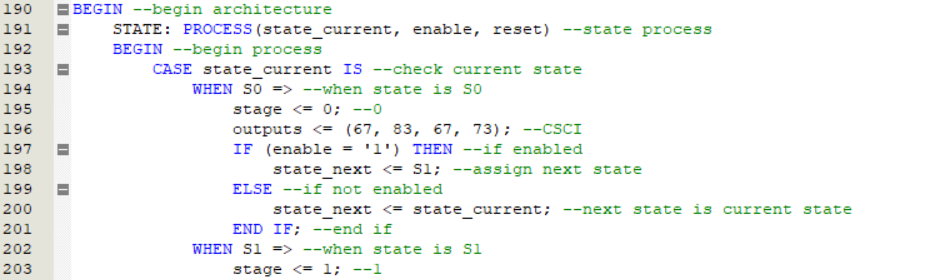


Figure – The first process used to run FiniteStateMachine (1/3).

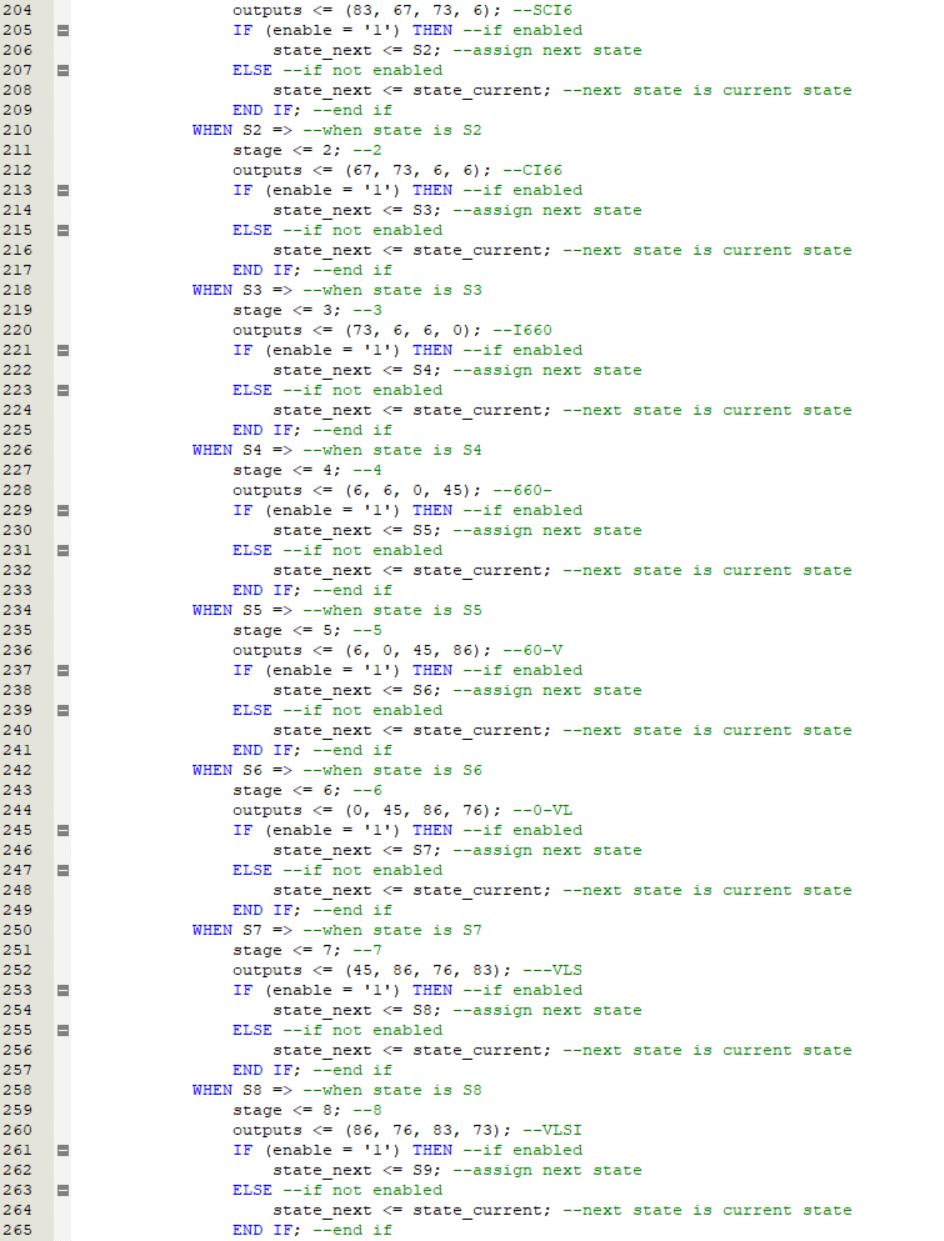


Figure – The first process used to run FiniteStateMachine (2/3).

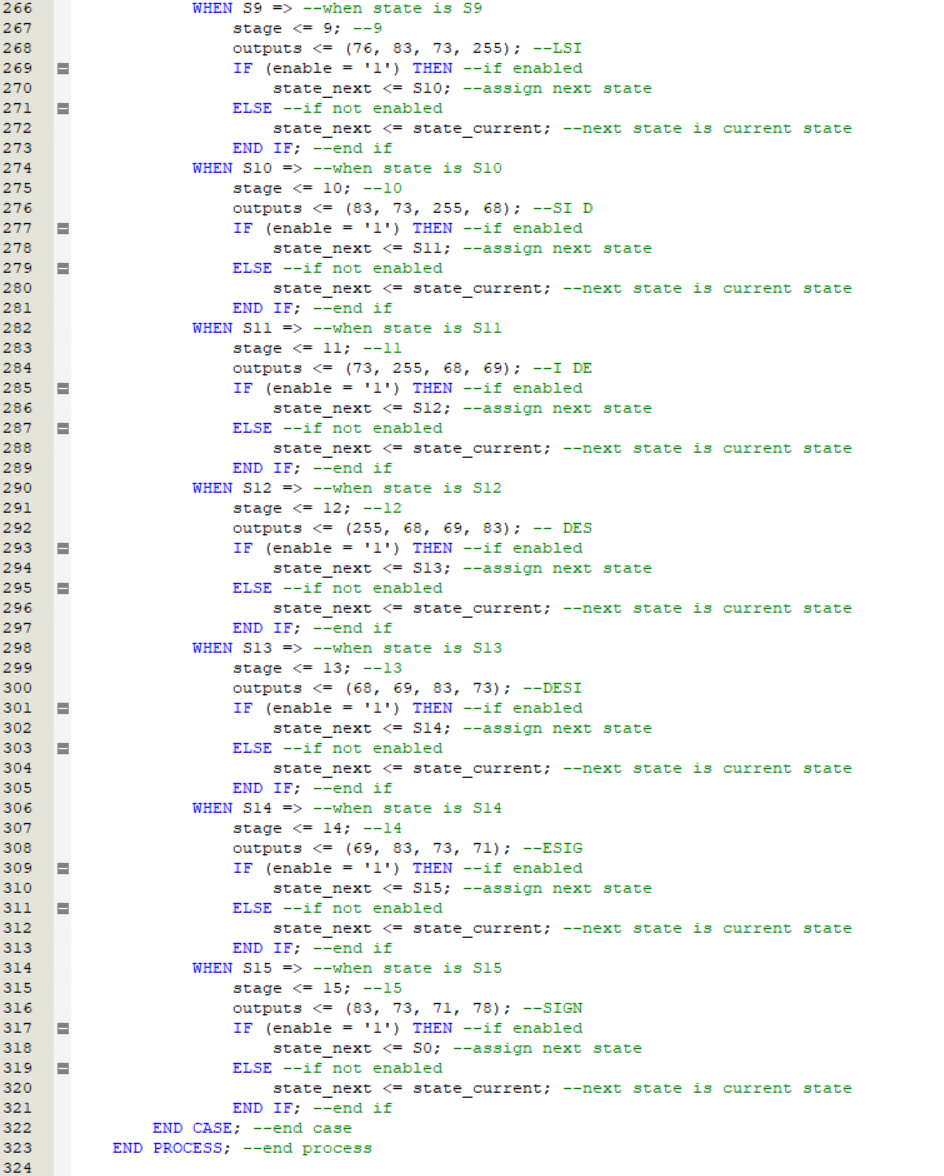


Figure – The first process used to run FiniteStateMachine (3/3).

#### Process 2: SYNCH

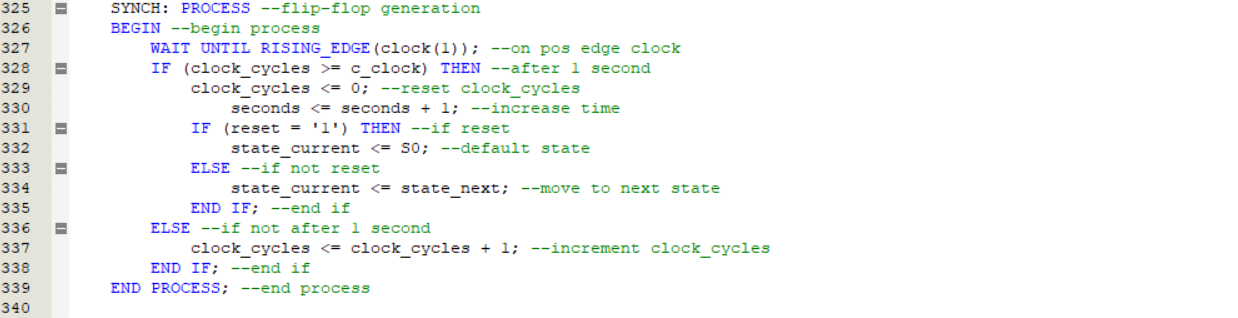


Figure – The second process used to run FiniteStateMachine.

#### Process 3:

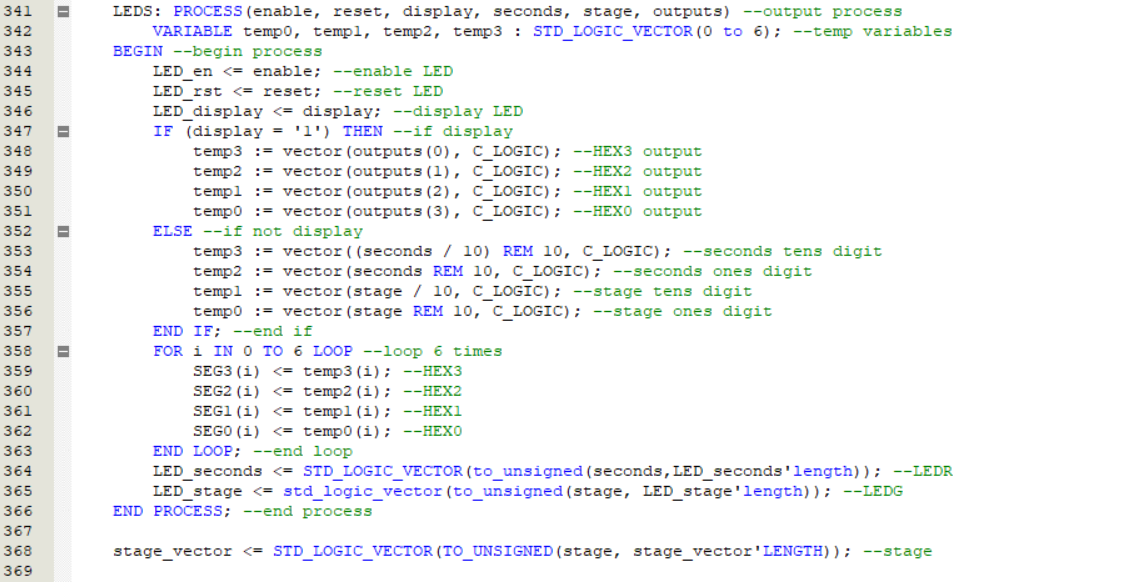


Figure – The third process used to run FiniteStateMachine.

#### Port Map

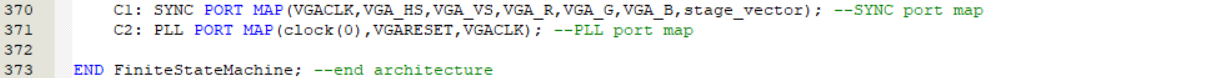


Figure – The port map used to run FiniteStateMachine.

## SYNC

### Library

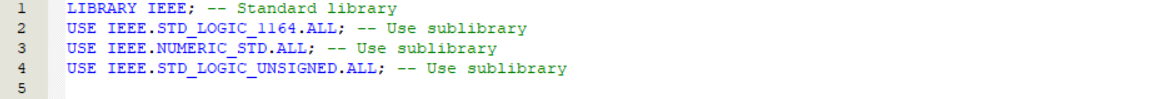


Figure 13 – The libraries used to run SYNC.

### Entity

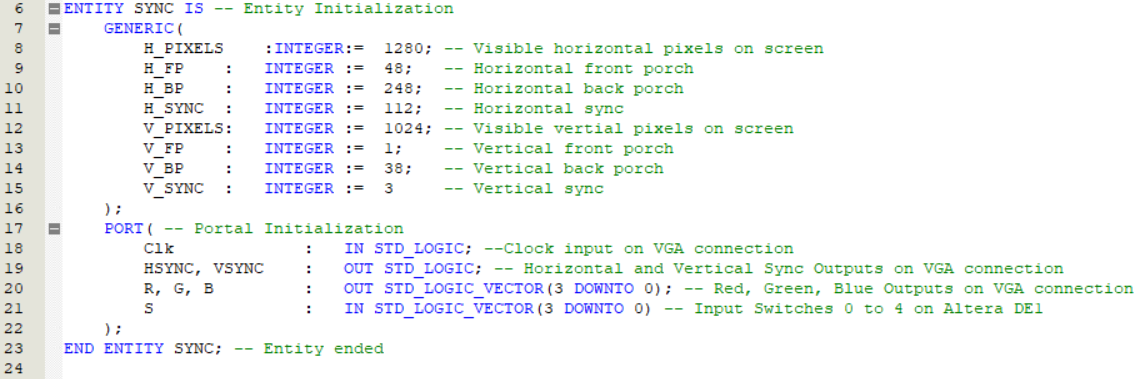


Figure 14 – The entities used to run SYNC.

### Architecture

#### Signals / Variables

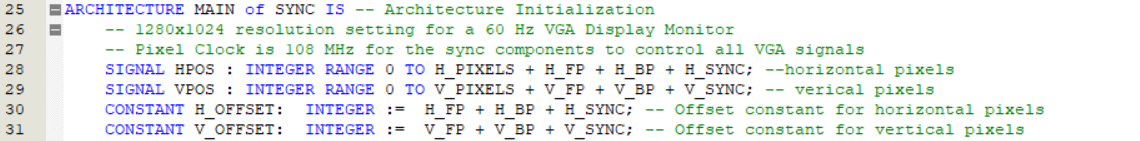


Figure 15 – The signal and/or variables used to run SYNC.

#### Process

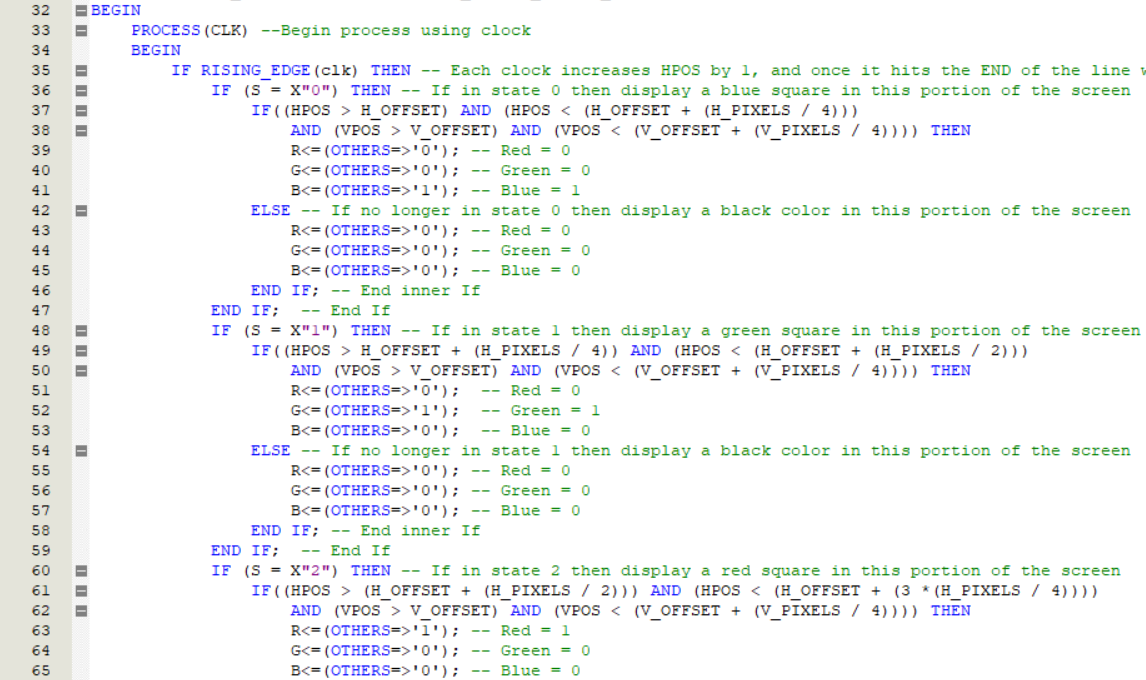


Figure 16 – The process used to run SYNC (1/4).

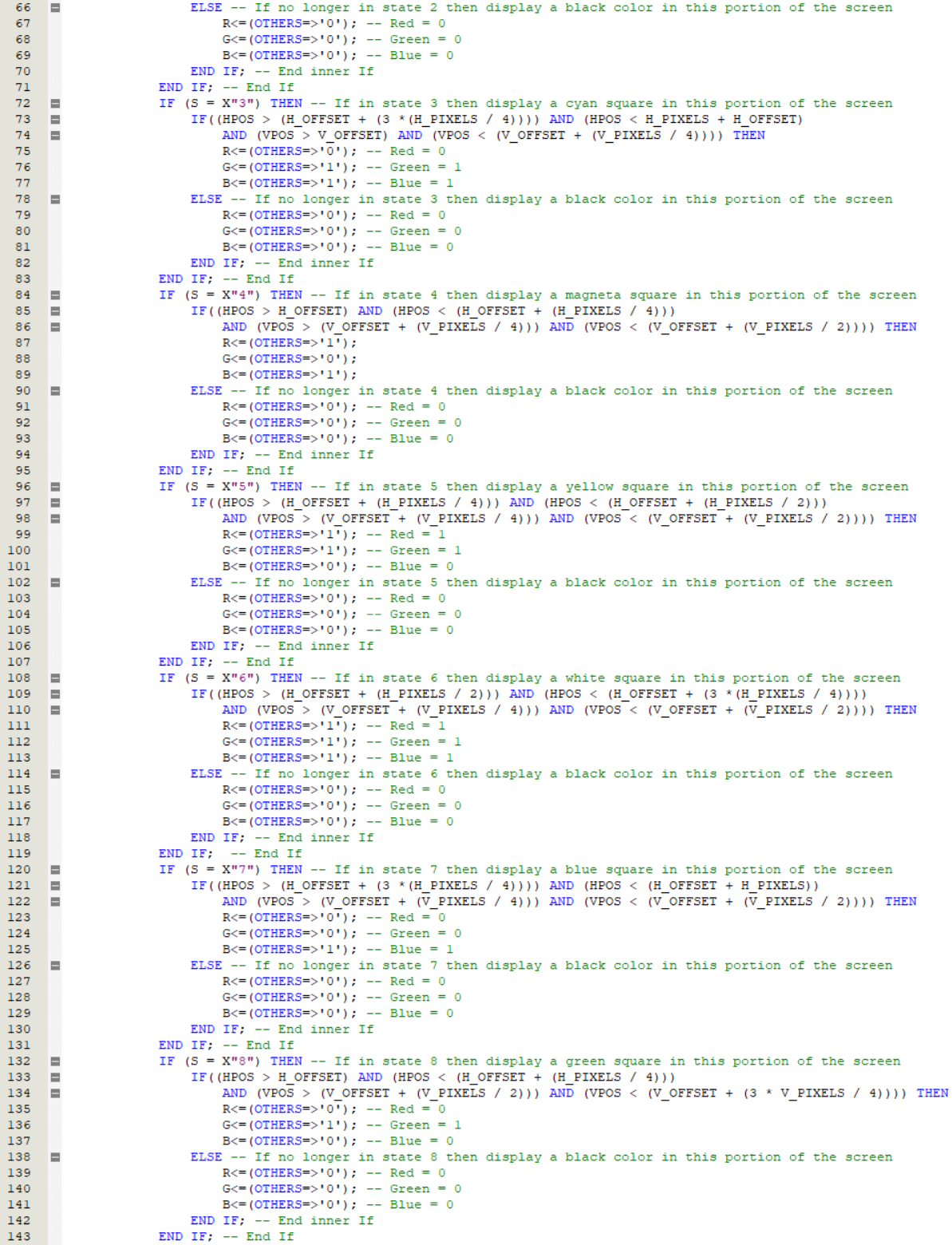


Figure 17 – The process used to run SYNC (2/4).



Figure 18 – The process used to run SYNC (3/4).

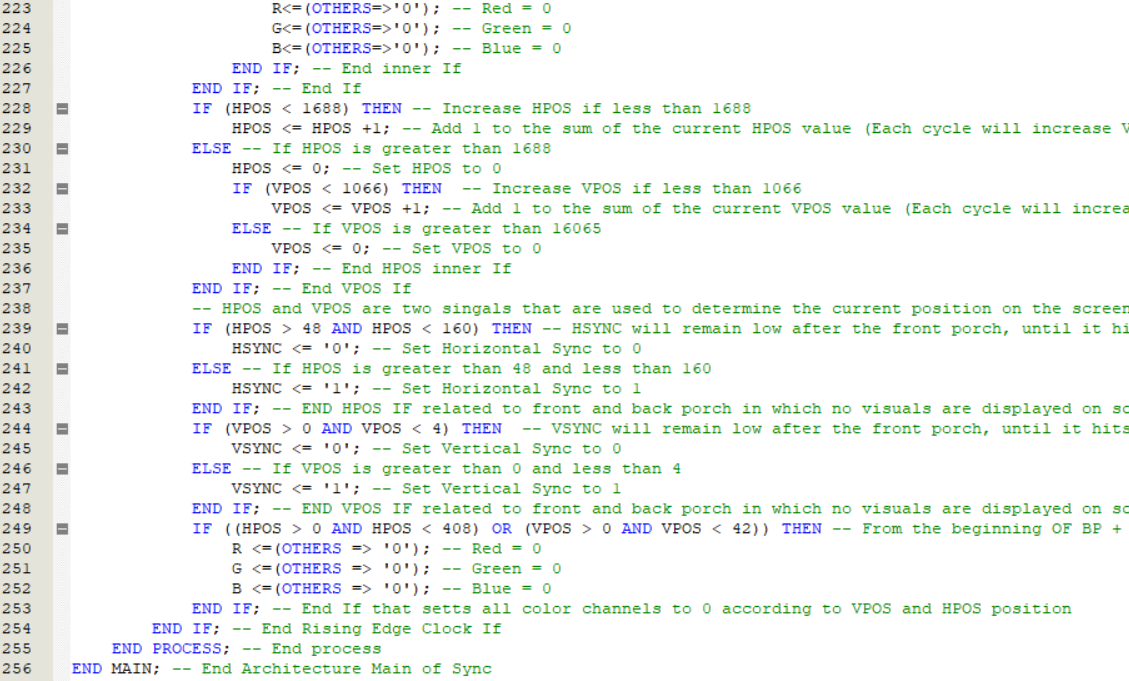


Figure 19 – The process used to run SYNC (4/4).

## PLL

### Library



Figure 20 – The libraries used to run PLL.

### Entity



Figure 21 – The entities used to run PLL.

### Architecture

#### Signals / Variables

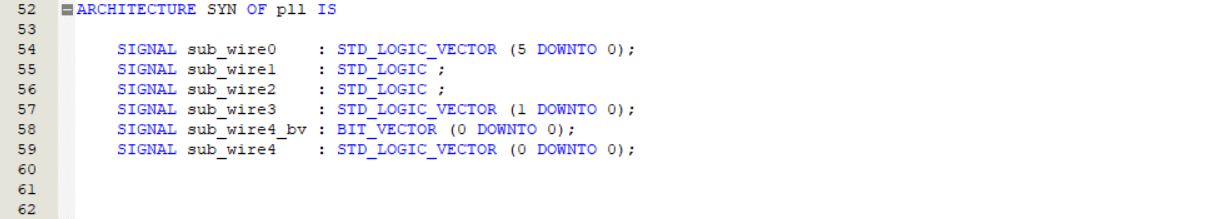


Figure 22 – The signal and/or variables used to run PLL.

#### Component

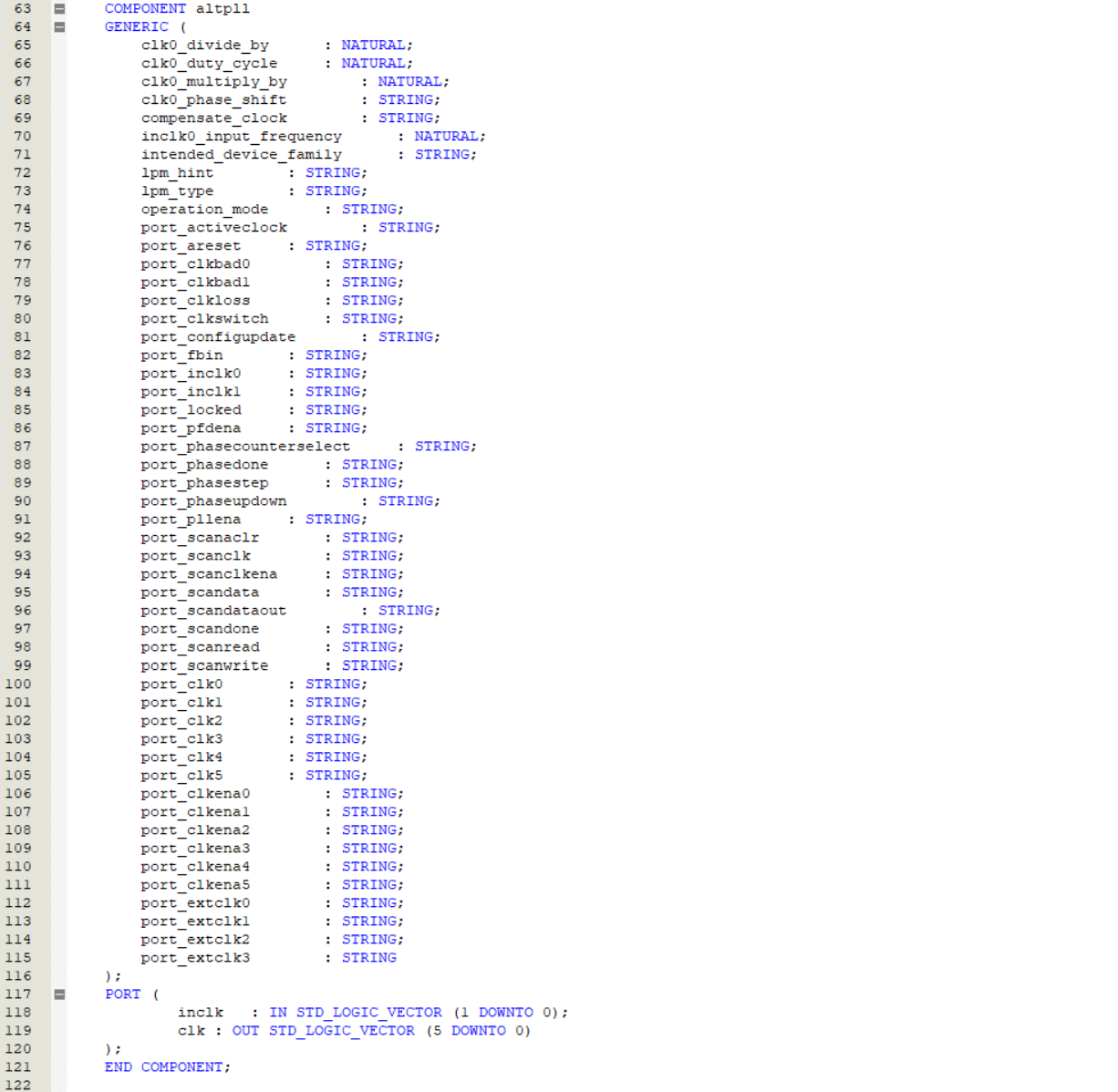


Figure 23 – The component used to run PLL.

#### Process

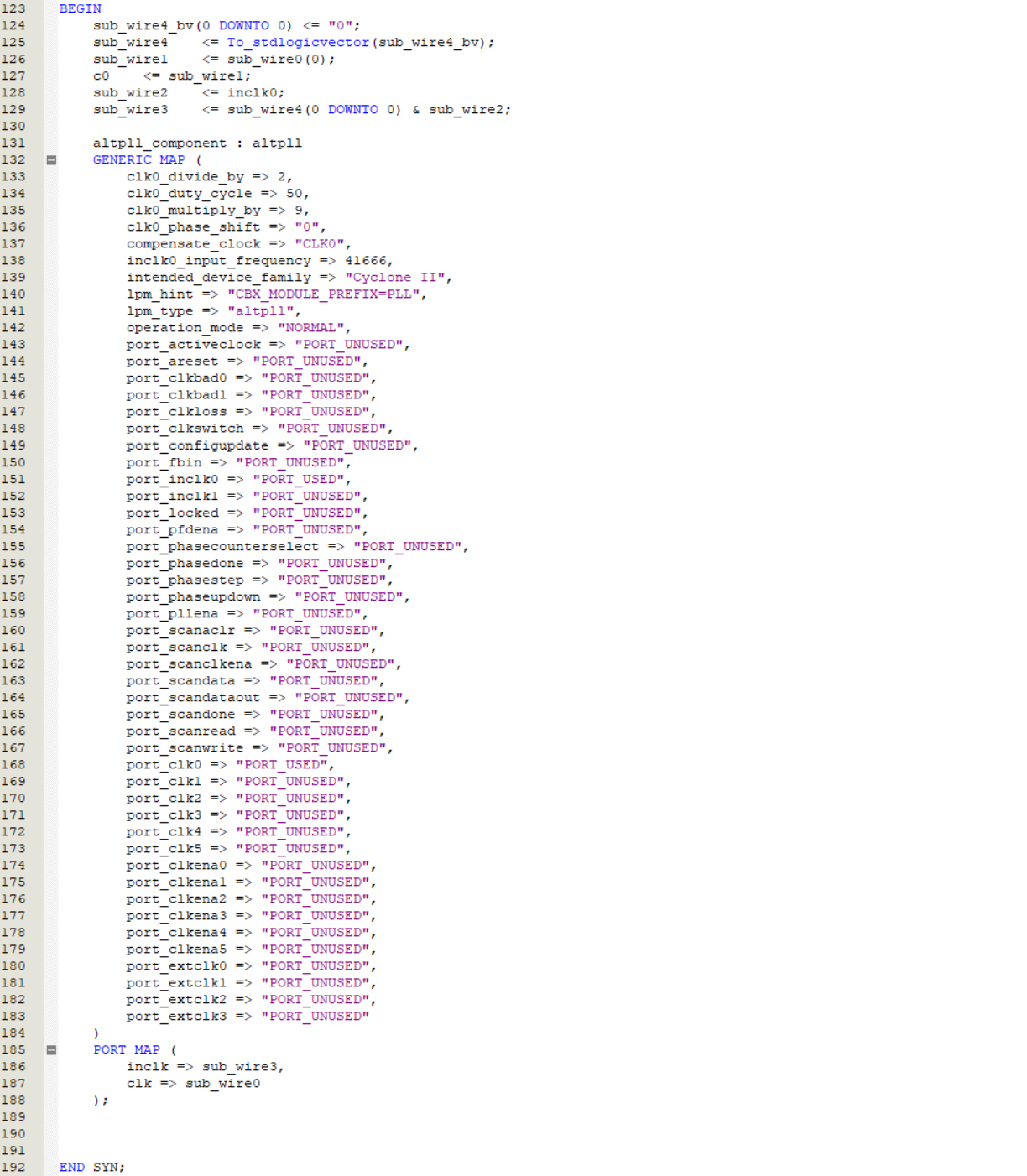


Figure 24 – The process used to run PLL.

# Vector Waveform Synthesis

Due to the large processing time needed to generate the 24 MHz clock frequency input, no computer in our possession can generate the output. The following screenshot is what the waveform file should look (without the output generated).

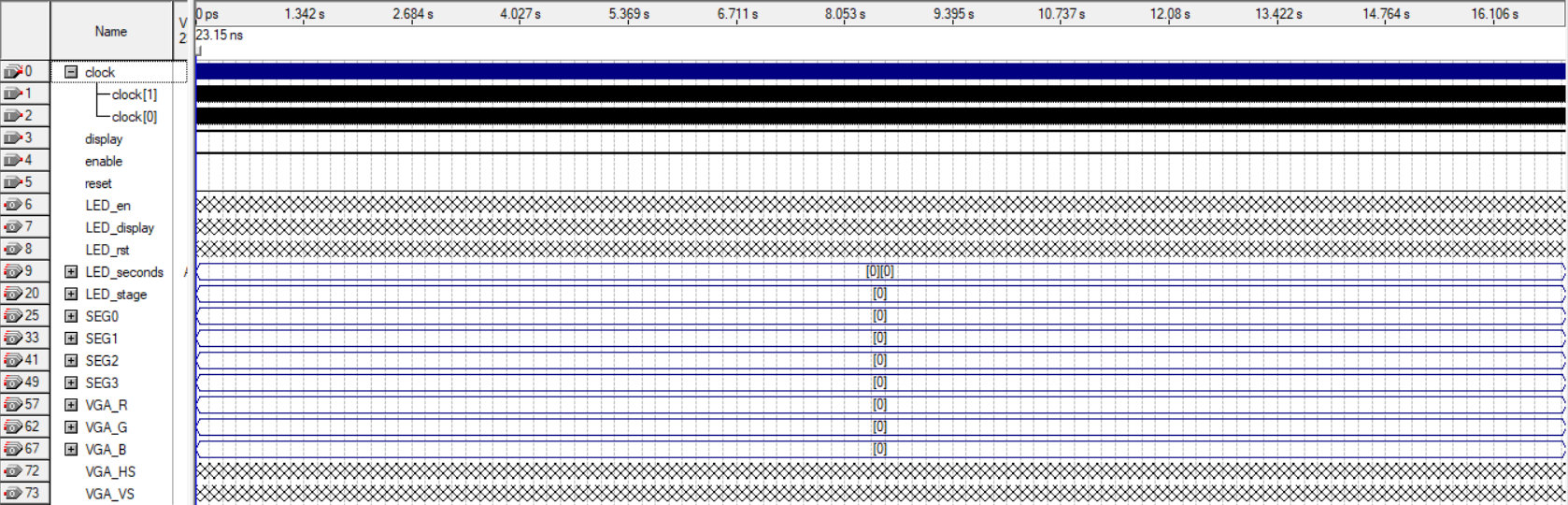


Figure 25 – The vector waveform file used to test this project.

# RTL Viewer

Due to the large number of components in this project, the RTL cannot be shown in this report. The screenshots of the RTL Viewer are provided within the project .zip file.

# State Machine Viewer

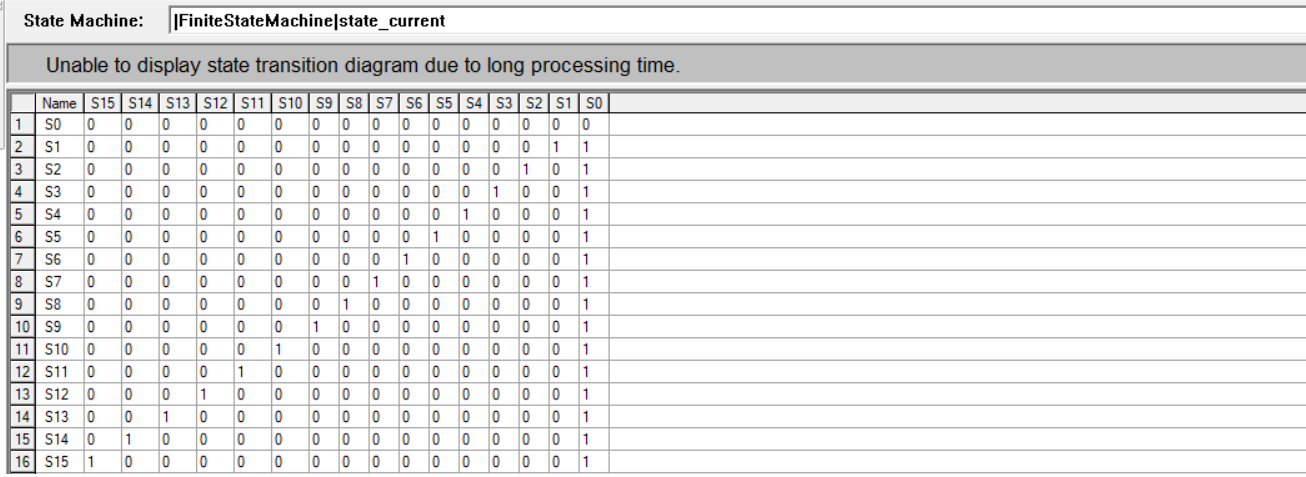


Figure 26 – The state machine viewer of this project.

# Altera DE1 Pin Assignments

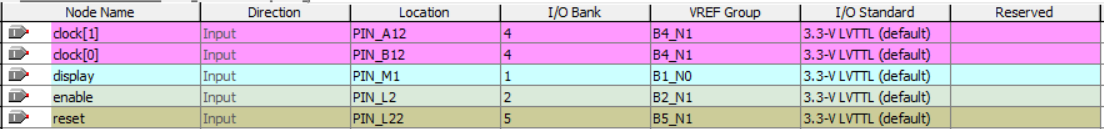


Figure 27 – The input pin assignments used to run this project.

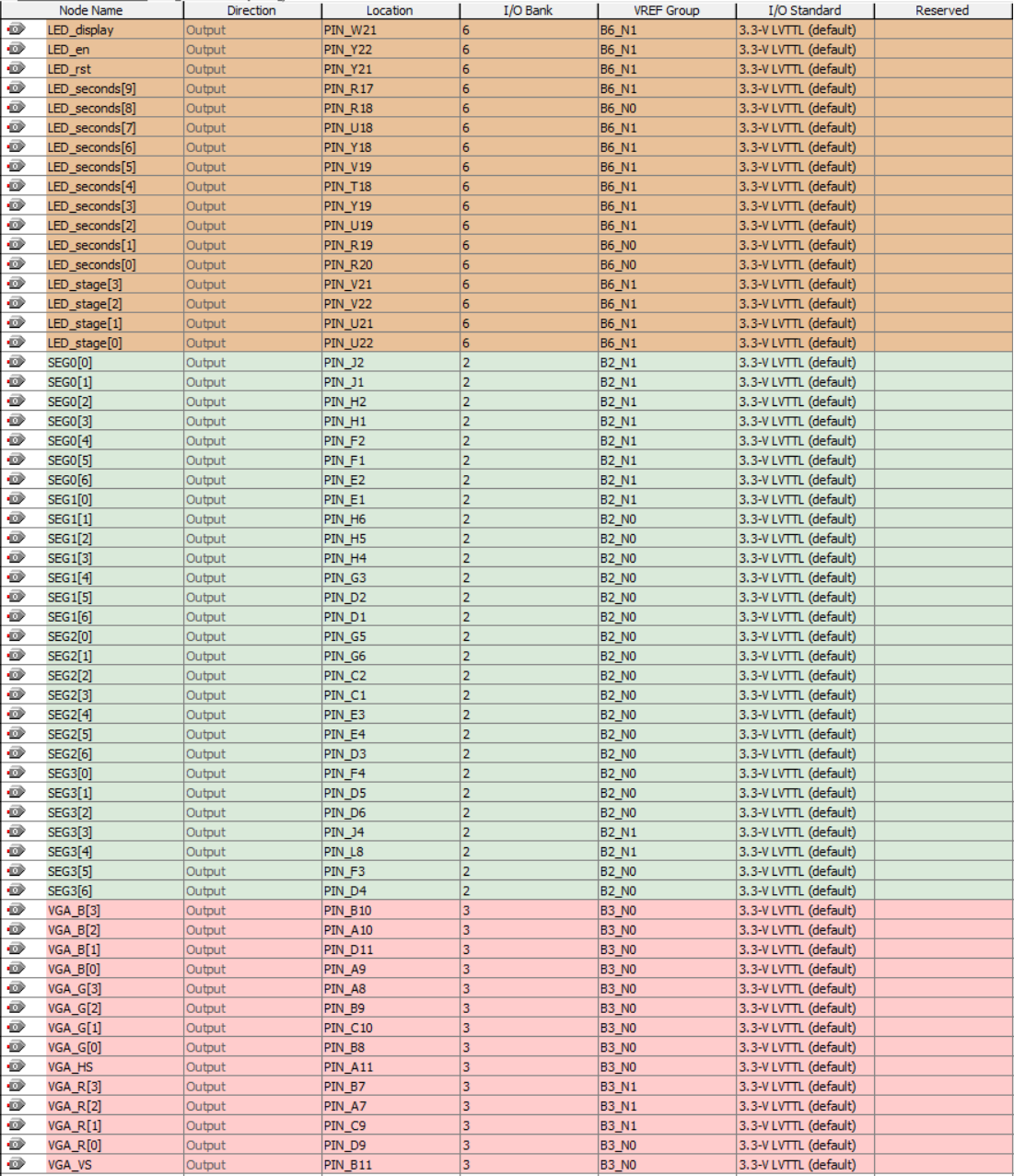


Figure 28 – The output pin assignments used to run this project.