Achieving High Bandwidth with Intel Parallel Studio XE

Stanford University, ME344 — Summer 2018

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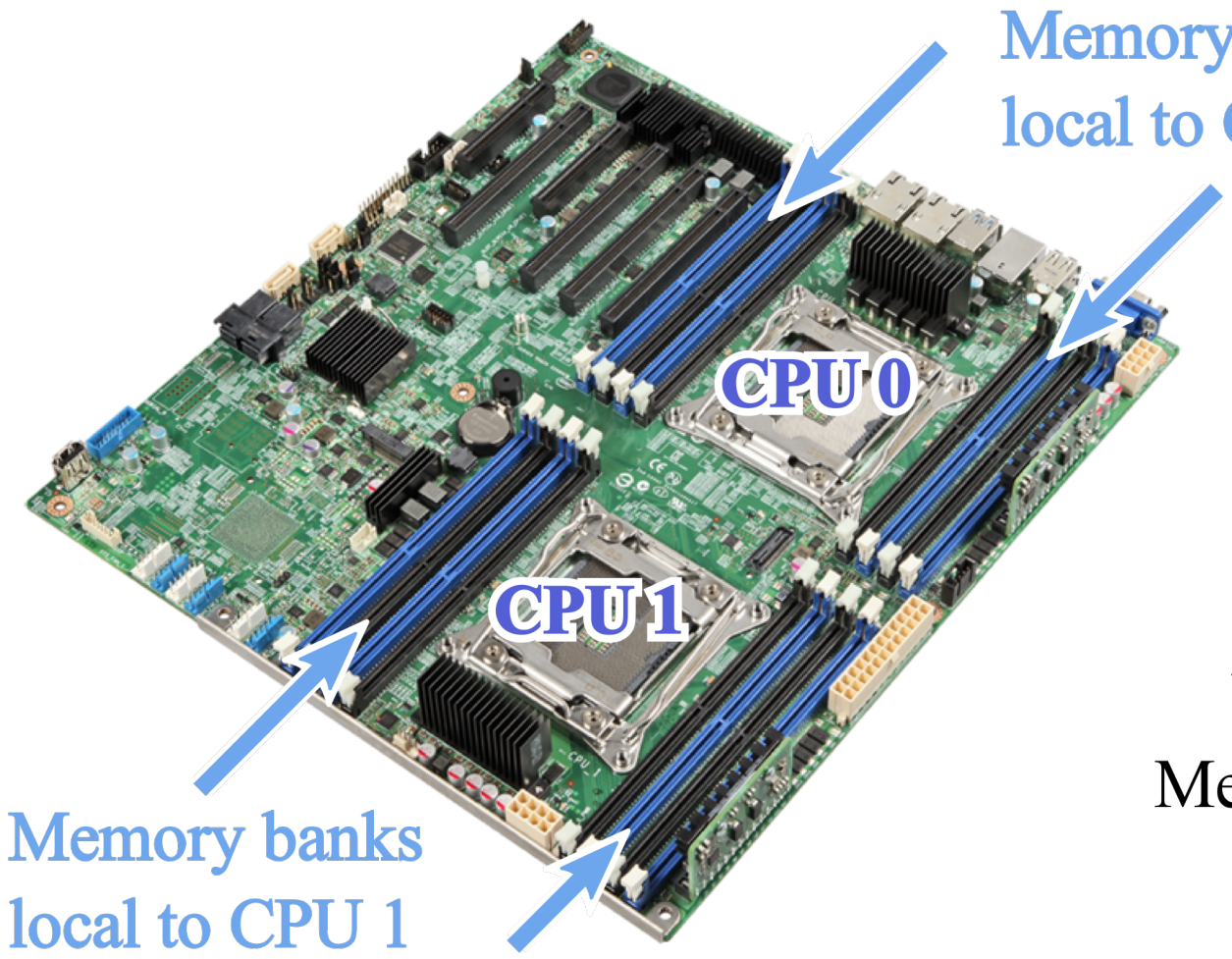
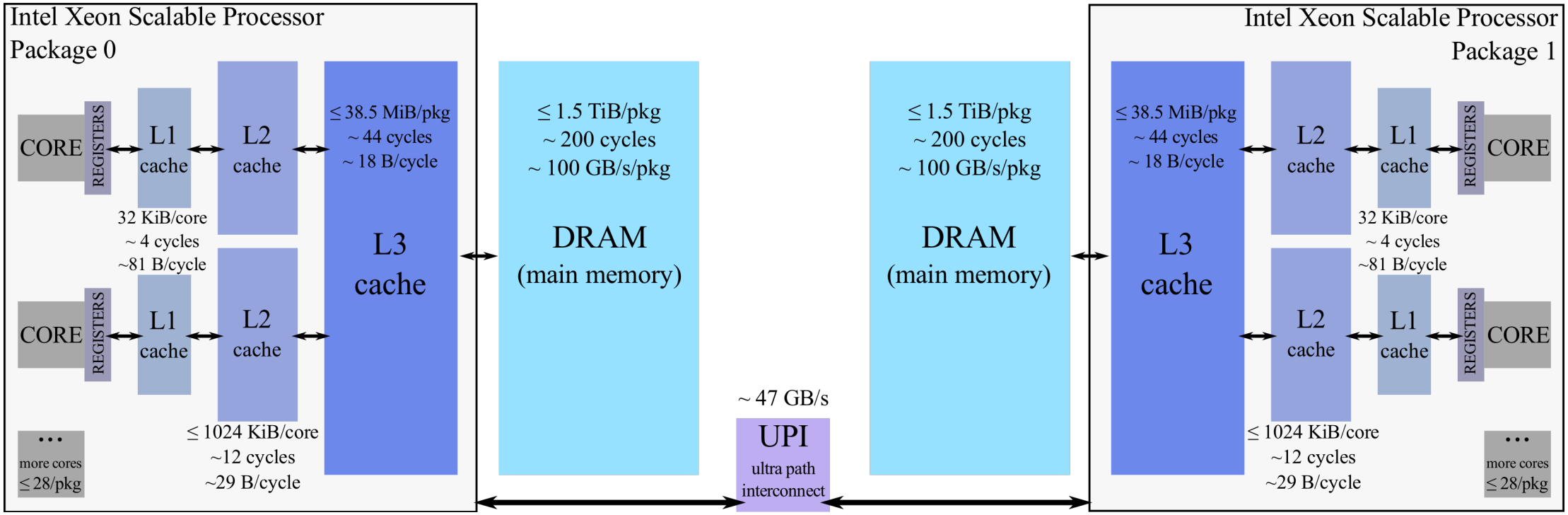
NUMA and Data Access Locality

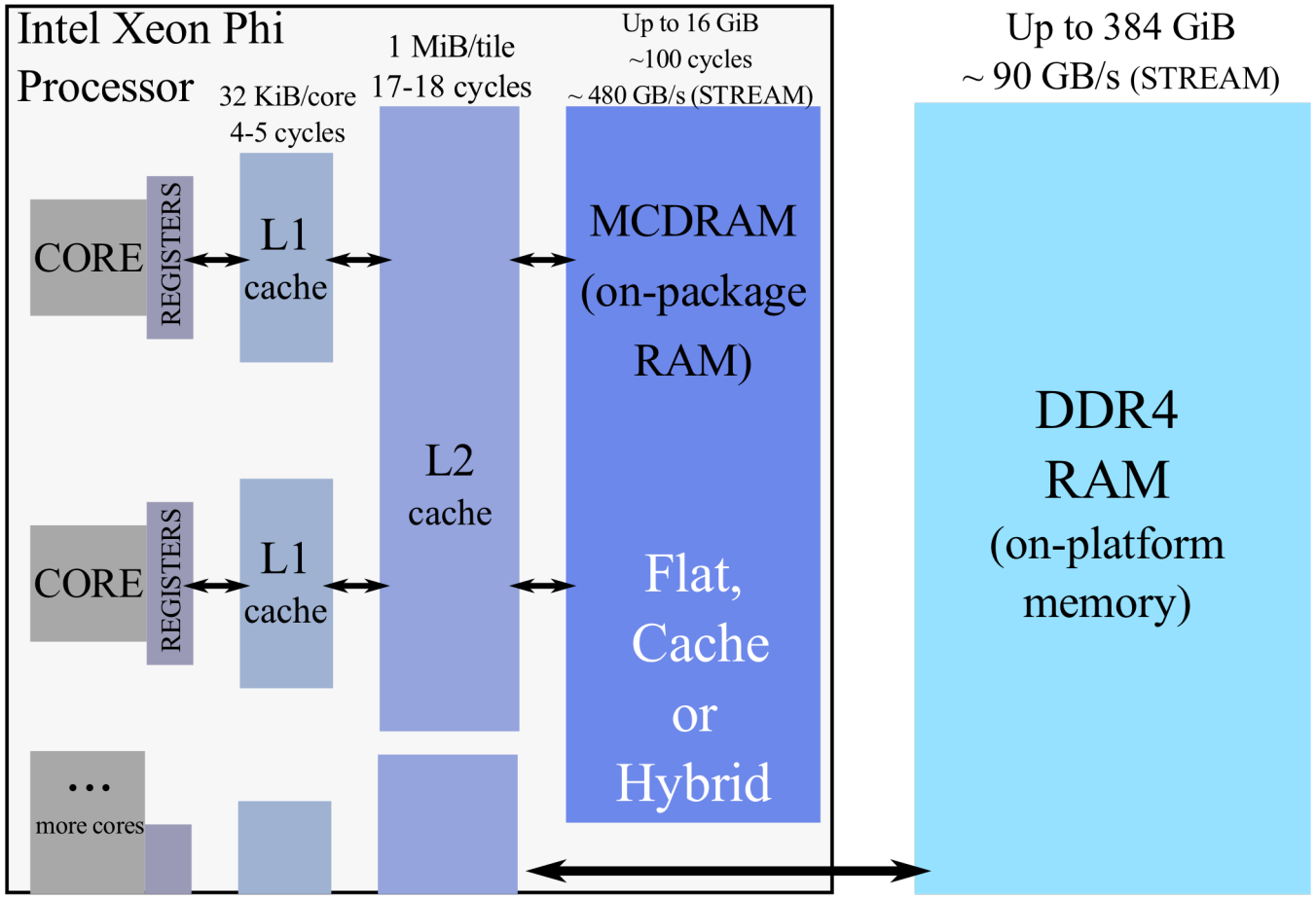


Non-Uniform
Memory Access
(NUMA)

Memory Hierarchy, Intel Xeon CPU



Memory Hierarchy, Intel Xeon Phi CPU

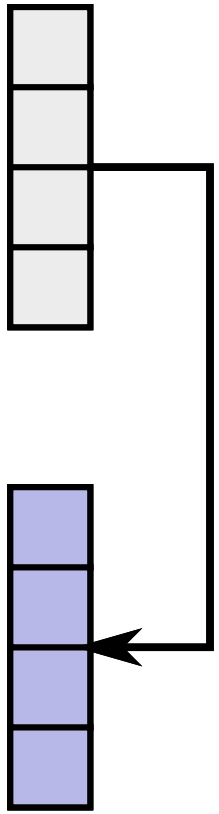


Access Online Materials

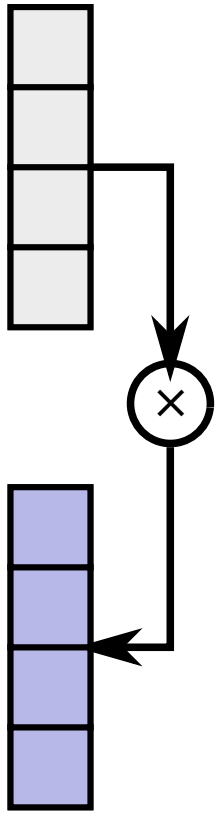
mc2learning.com/course/parallelism-and-memory-bandwidth-in-a-stencil-code-c-lin/

STREAM Benchmark

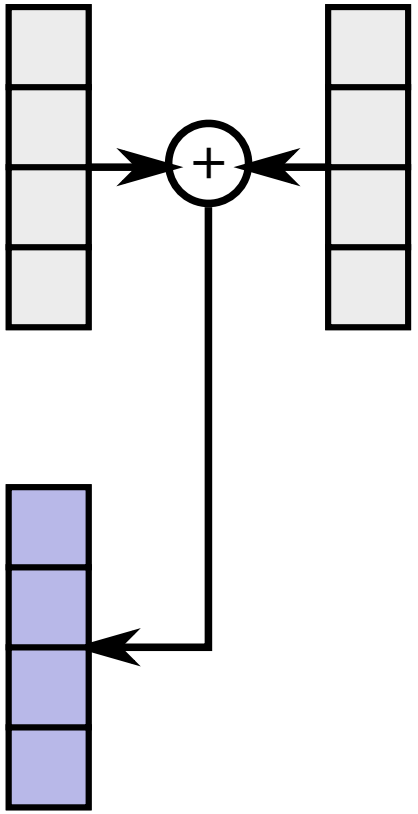
Copy:
`c[j] = a[j]`



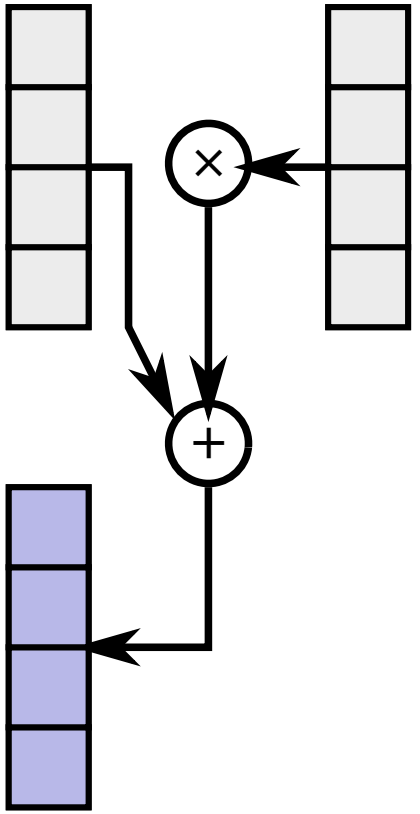
Scale:
`b[j] = S*a[j]`



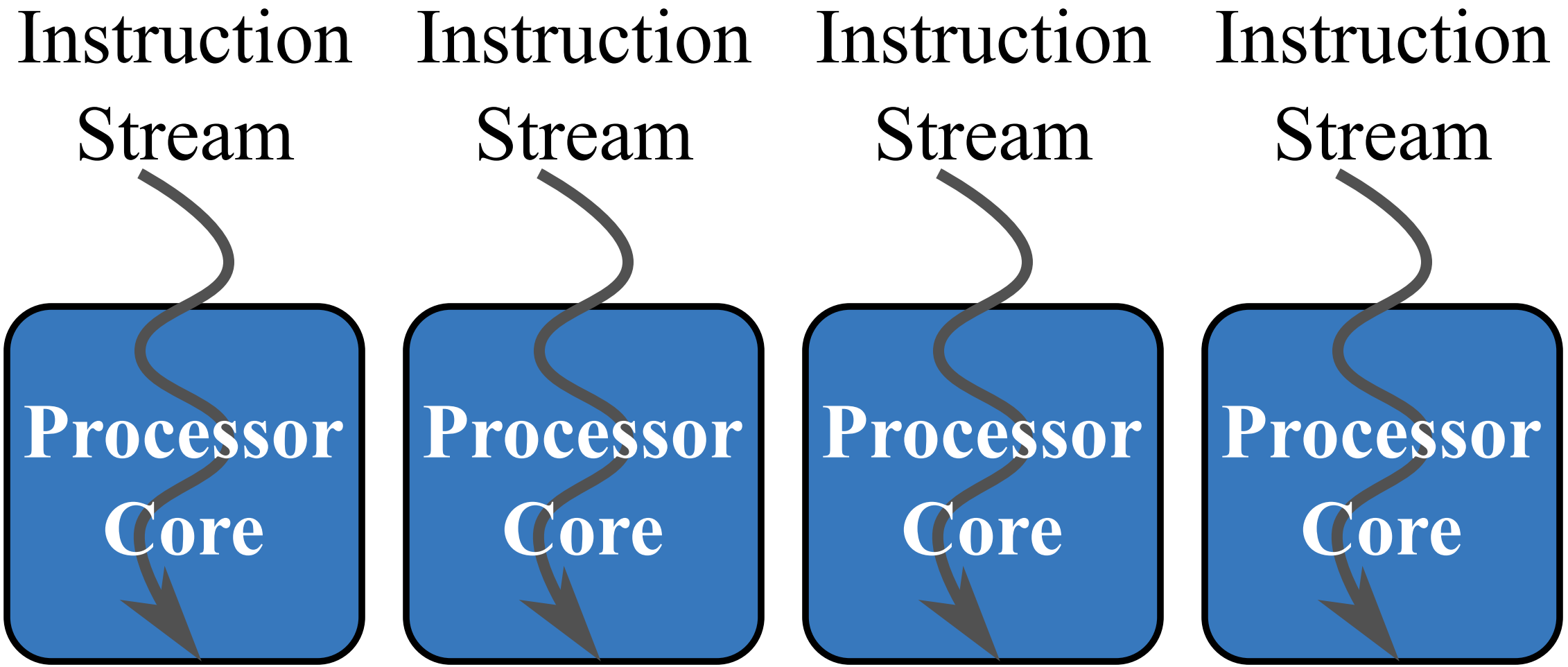
Add:
`c[j] = a[j]+b[j]`



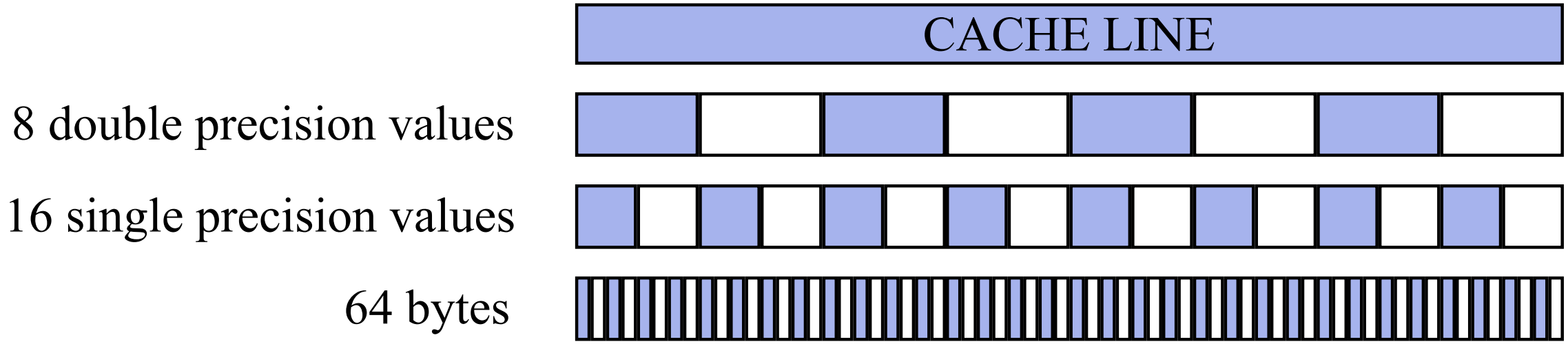
Triad:
`a[j] = b[j]+S*c[j]`



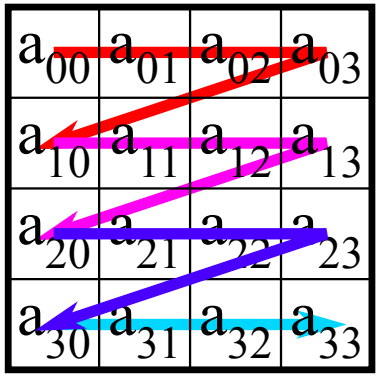
Memory Controllers and Threads

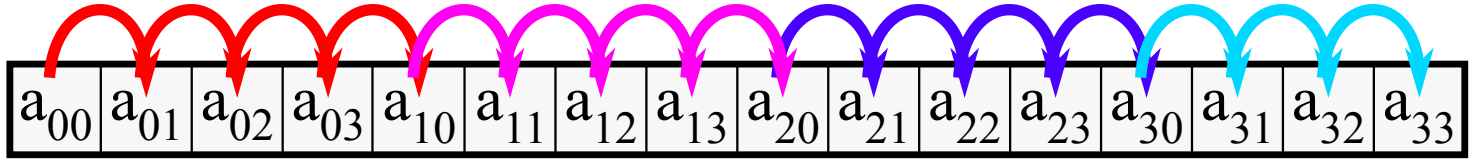


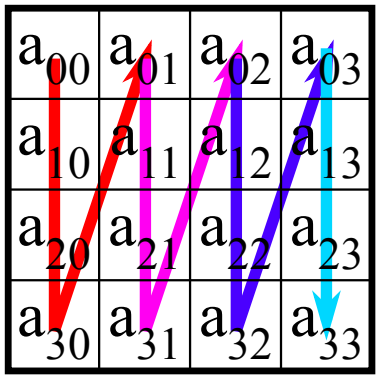
Cache Lines and Vectorization

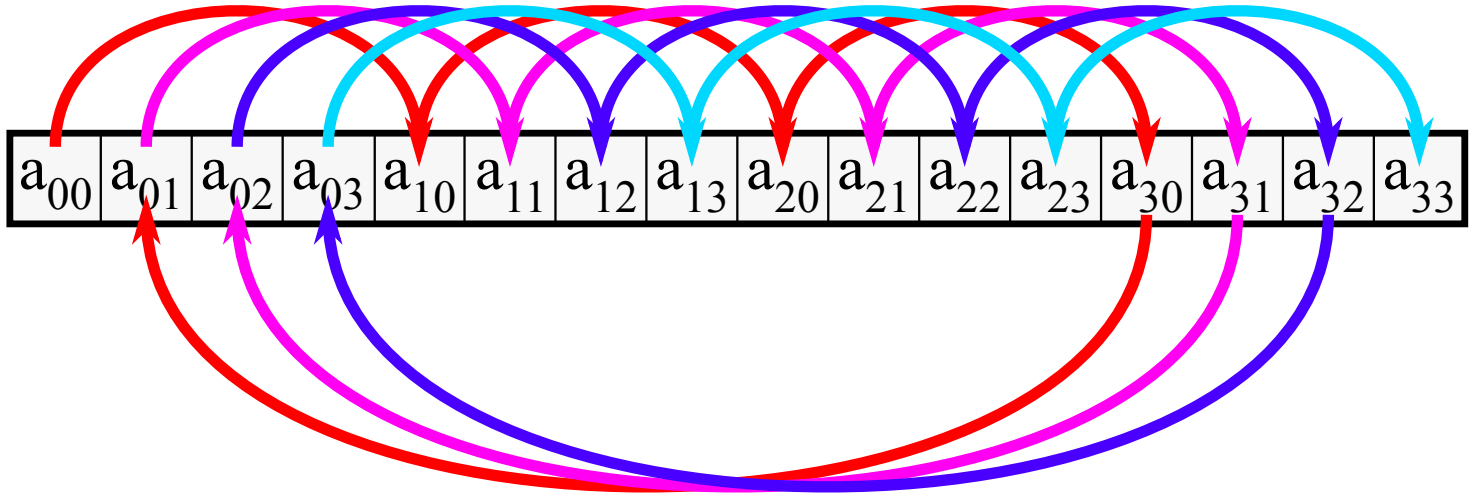


Sequential Access

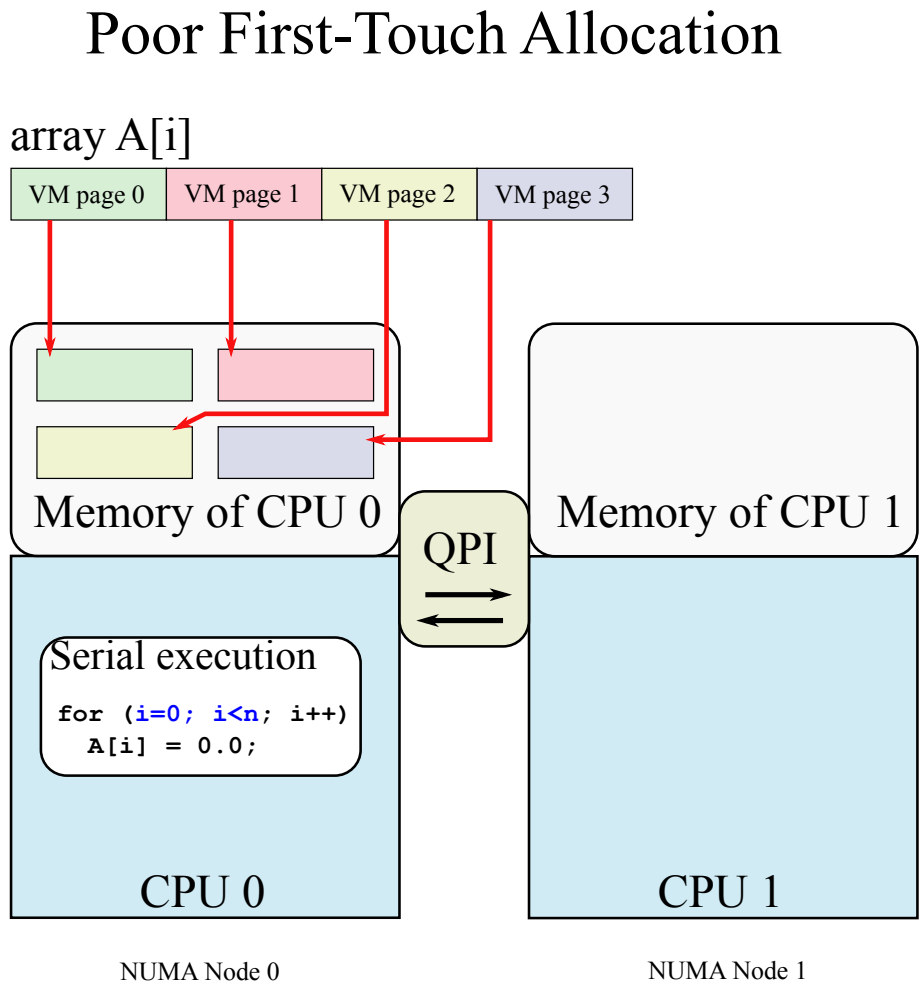


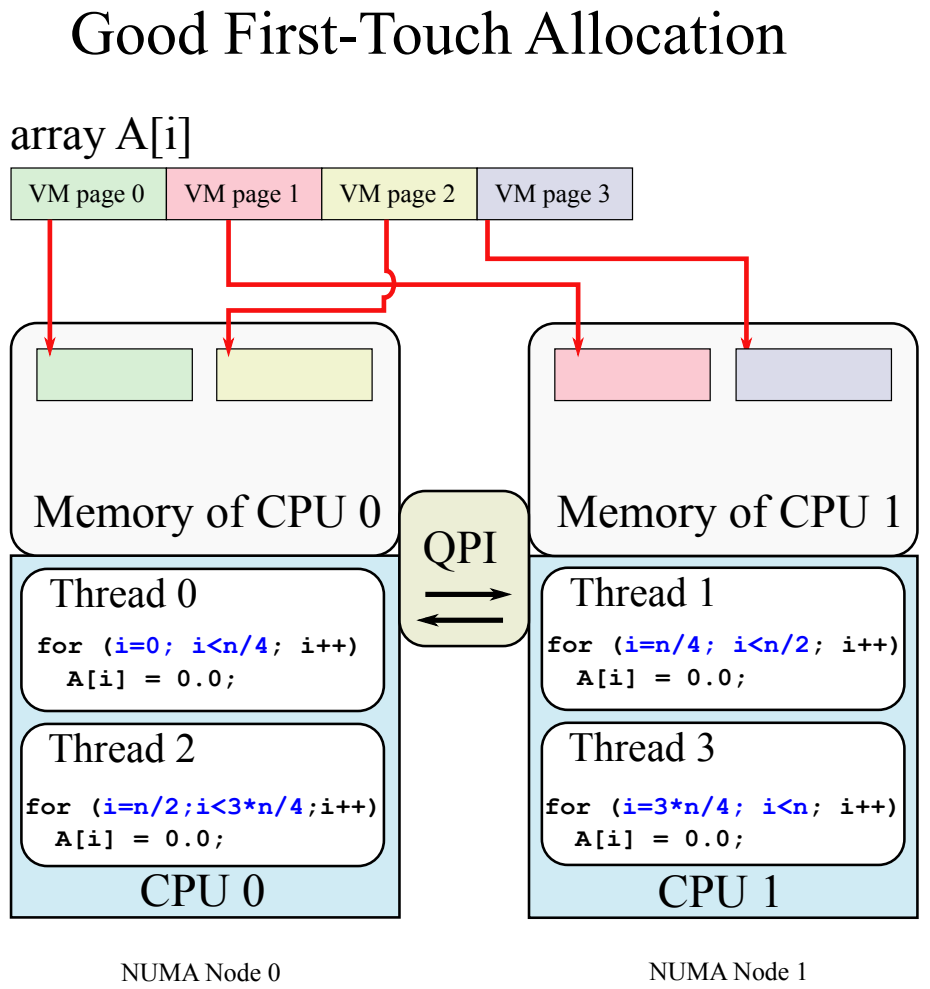




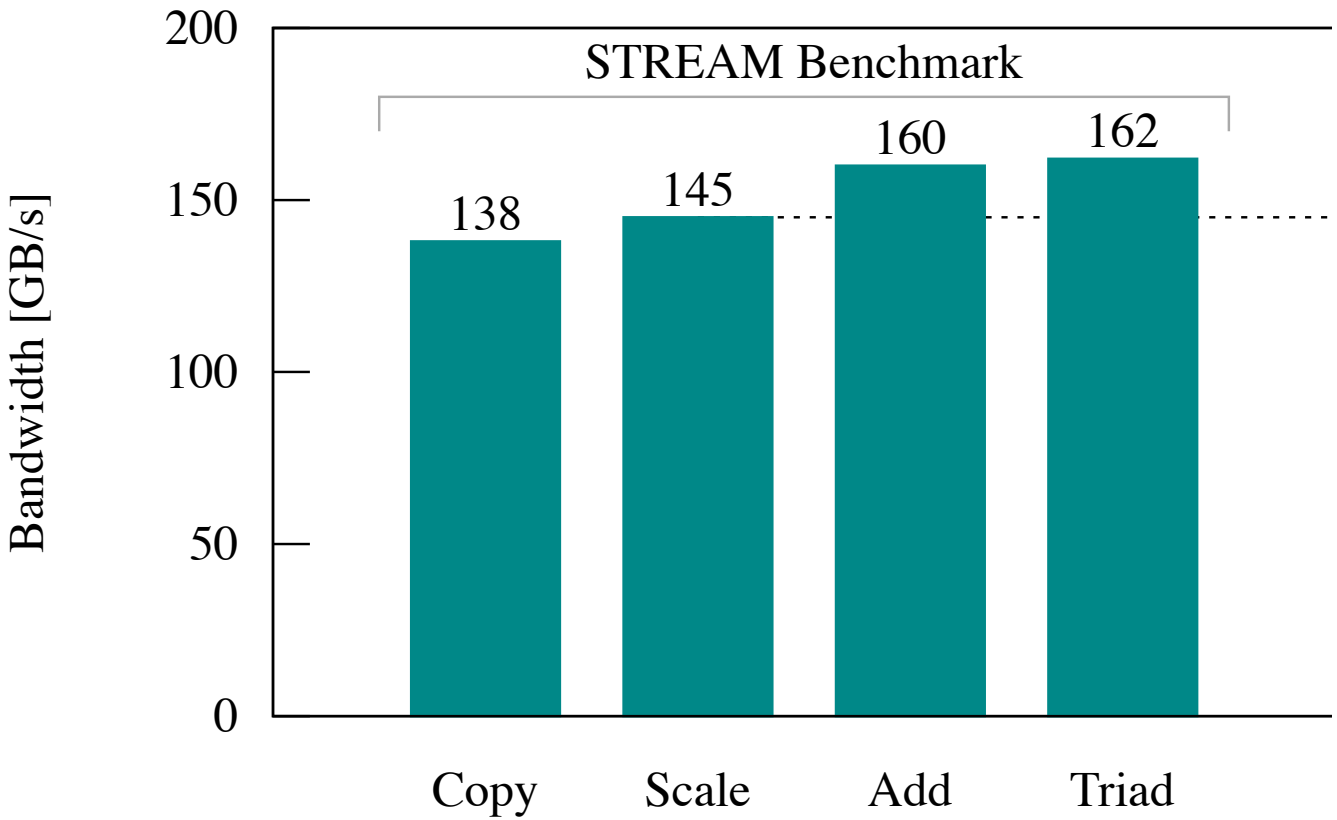


First Touch Policy and Array Initialization



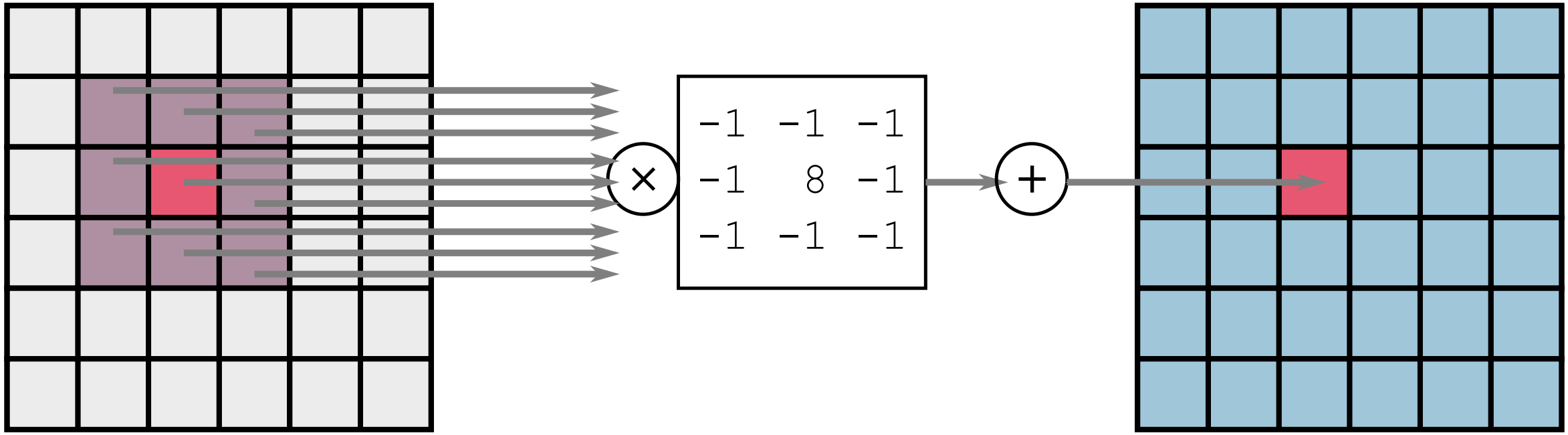


STREAM Optimization

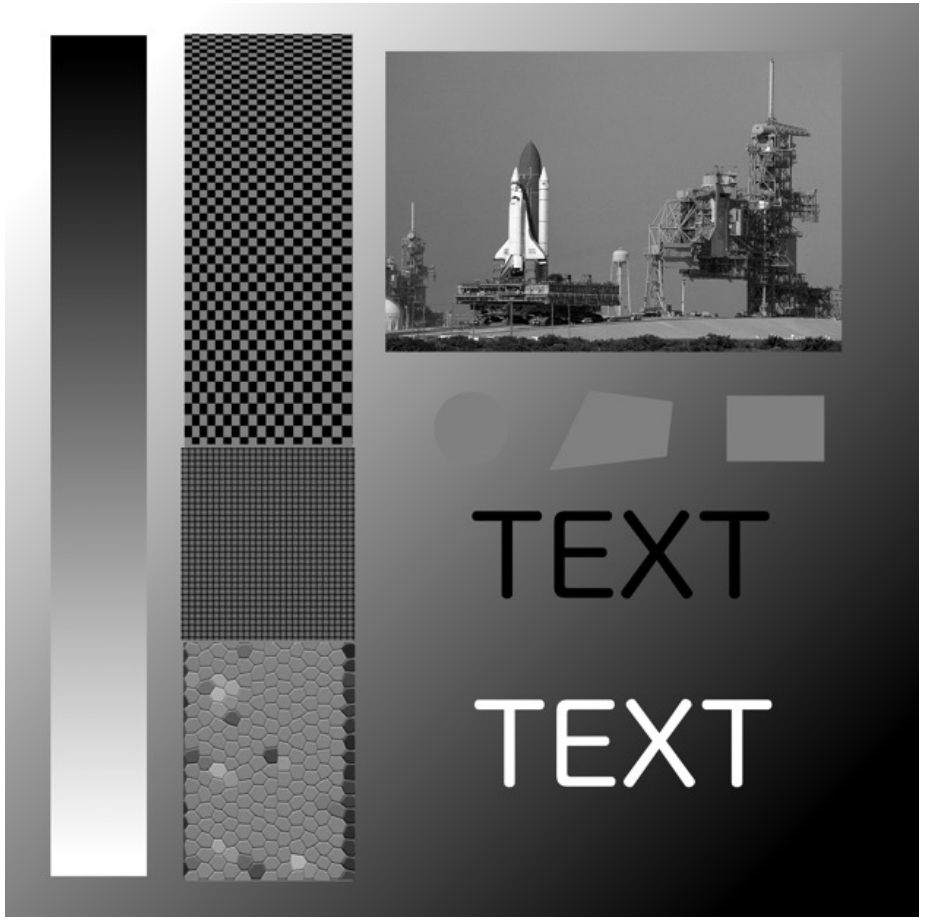


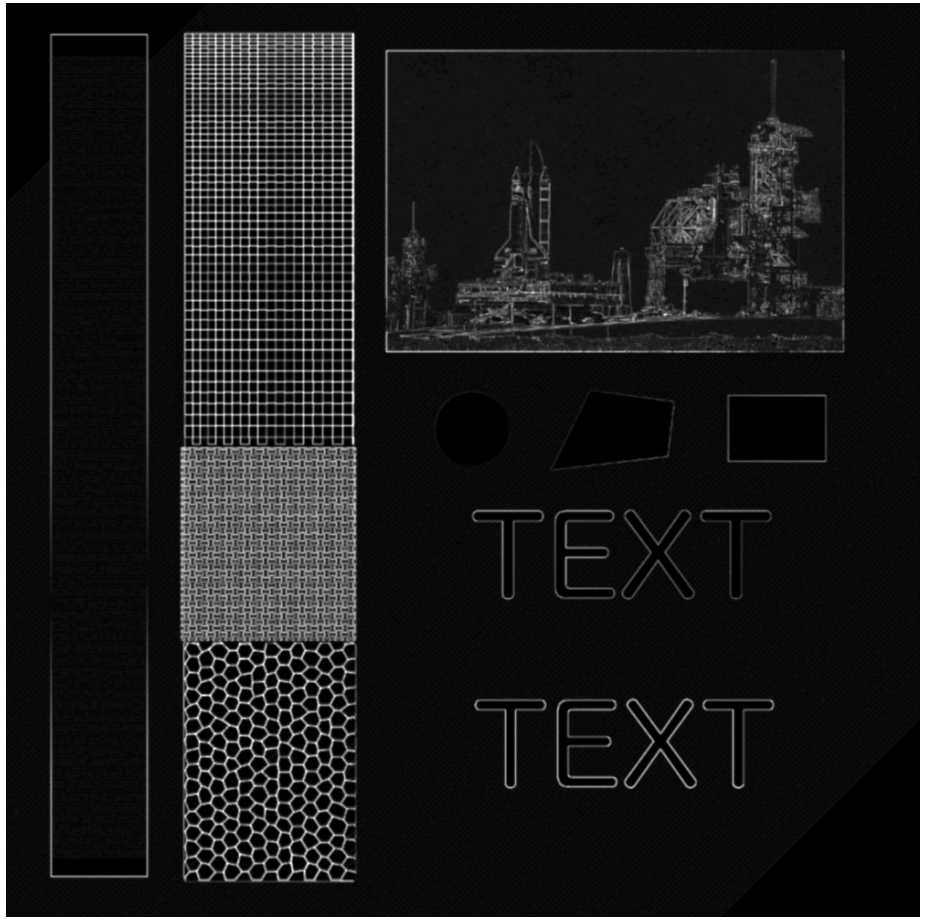
- Multithreading
- Vector ISA
- Thread affinity
- Streaming Stores

9-Point Stencil

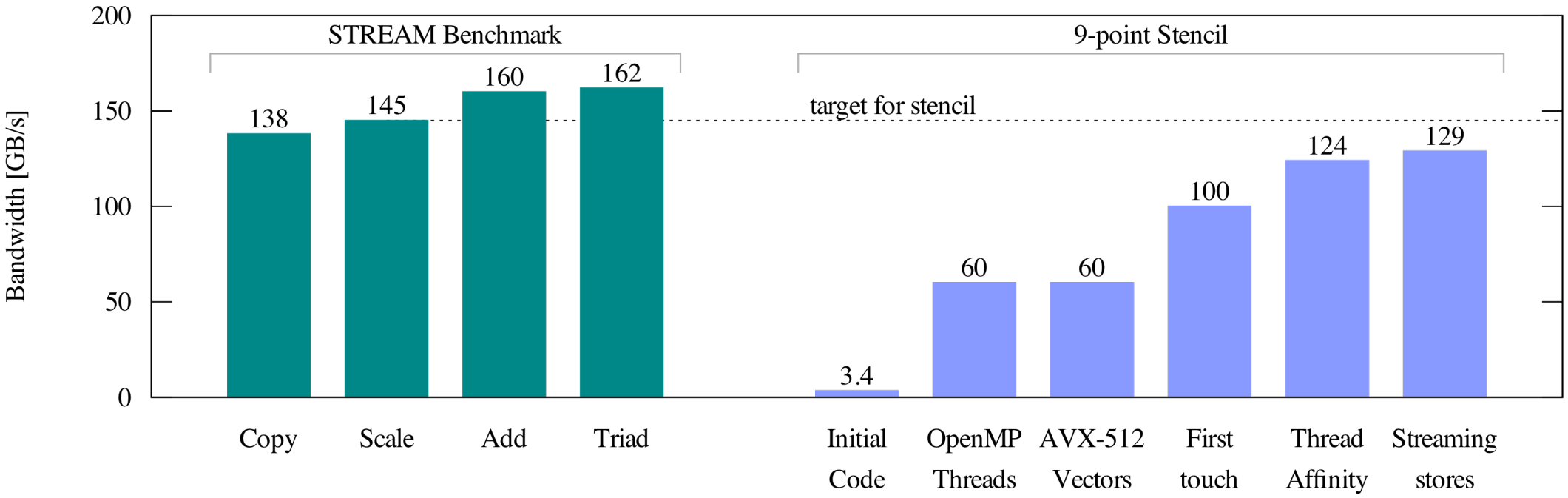


Edge Detection

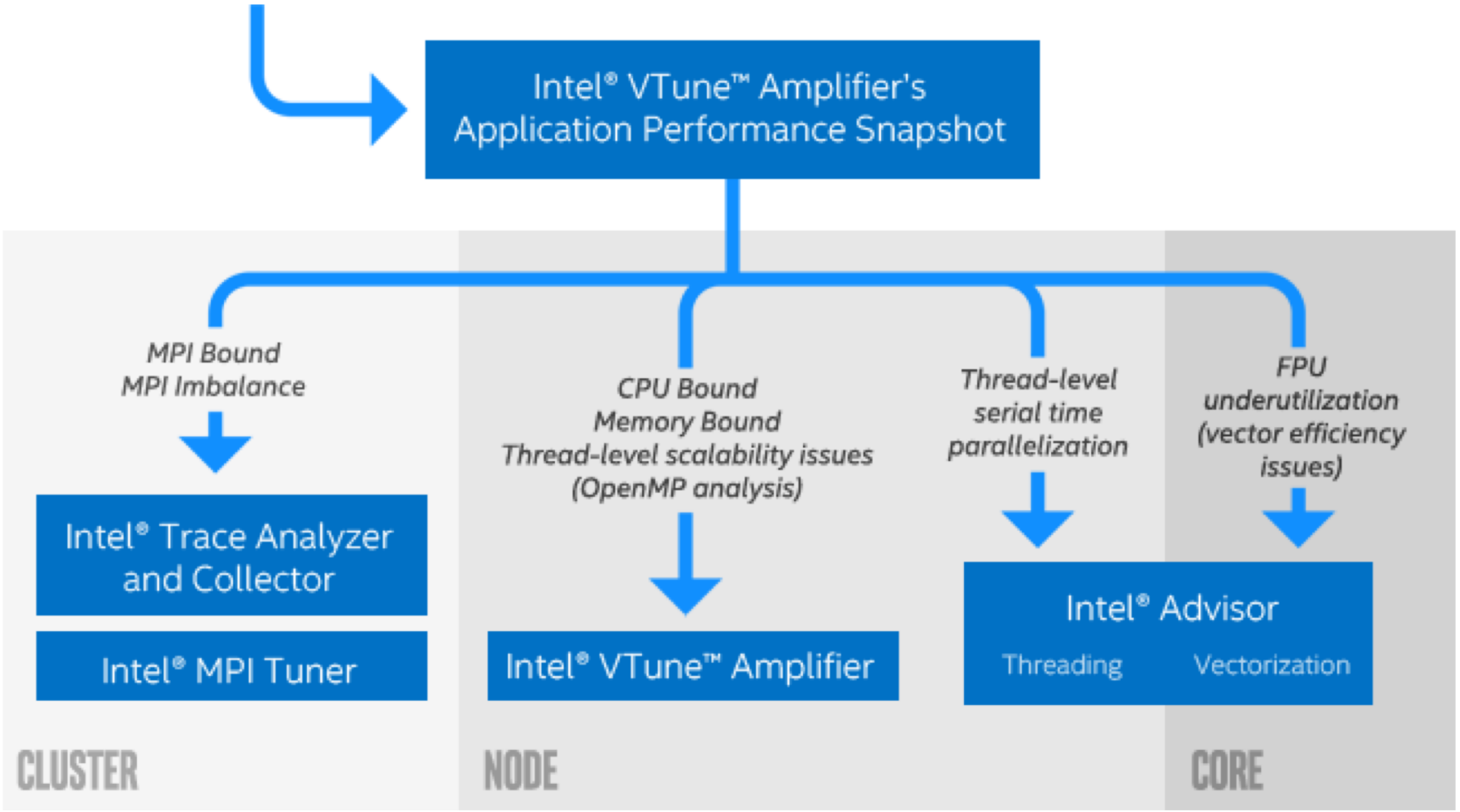




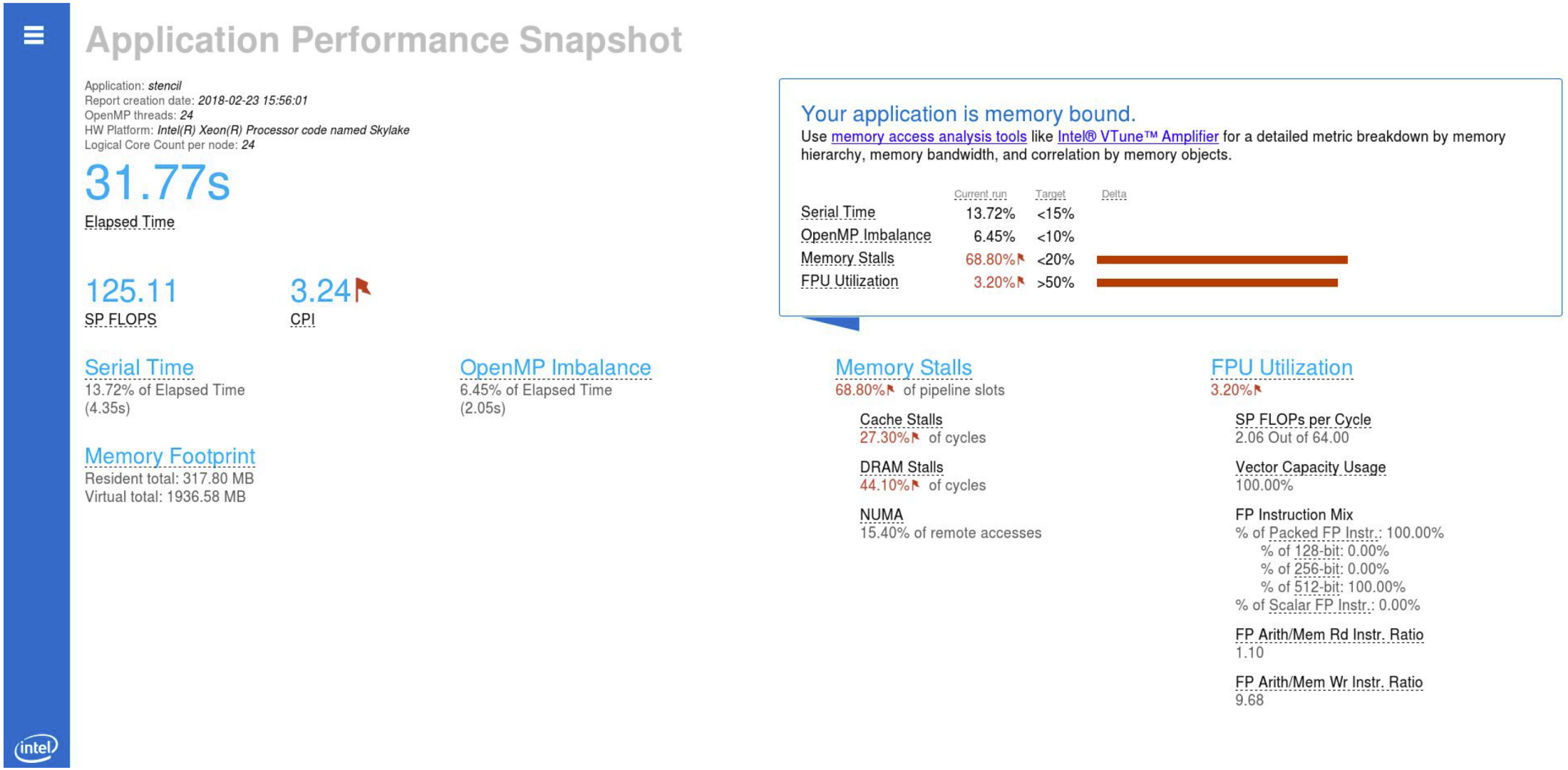
Stencil Code Optimization



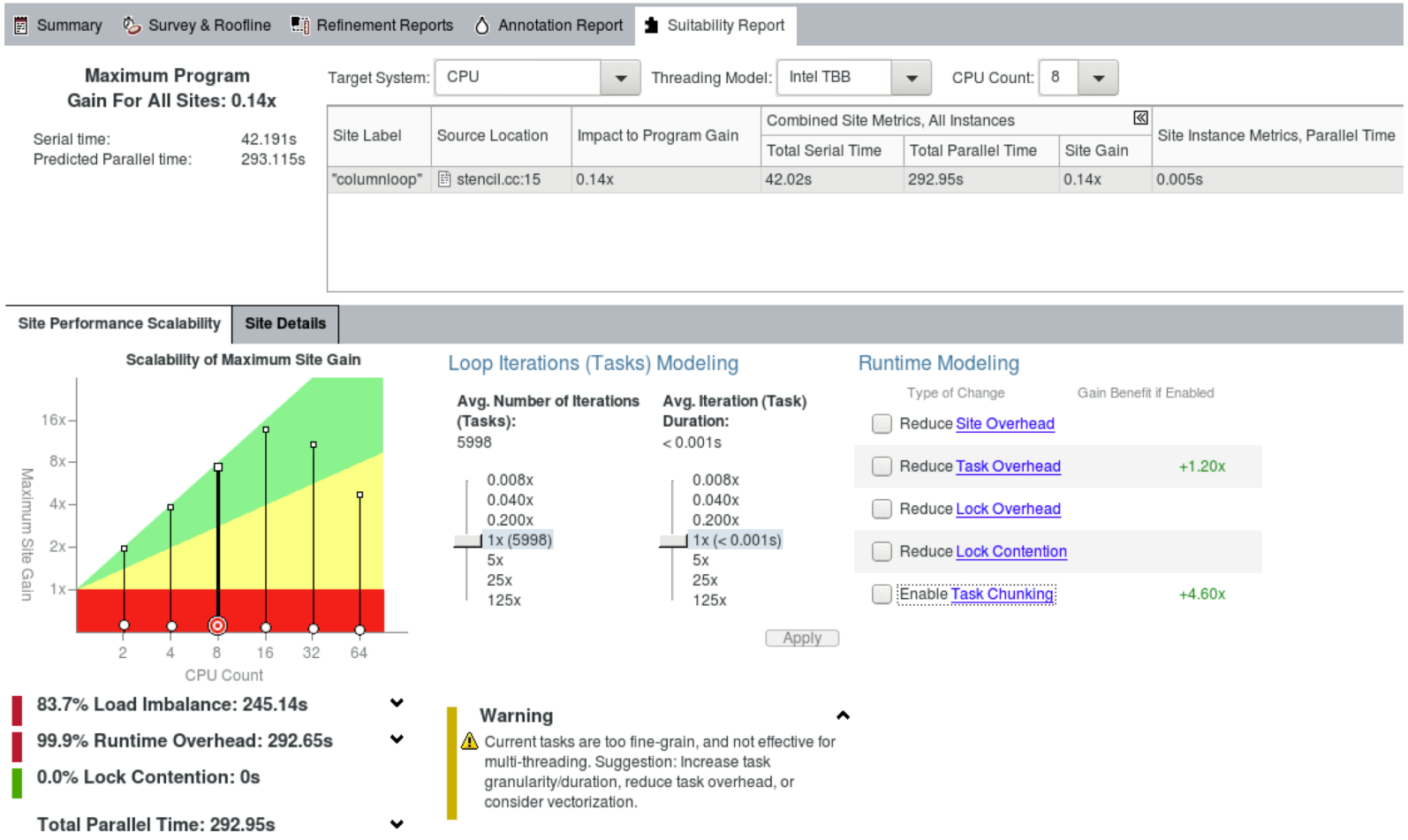
Intel Parallel Studio XE Tools



Intel VTune Amplifier — Application Performance Snapshot



Intel Advisor



Intel VTune Amplifier