ENGR 3410 Computer Architecture
Lab 3: CPU

Workplan

Anna, Apurva, Jee

Processor design: Single-cycle CPU

Schematic	2 hours
Integration of modules	2 hours

Modules

Data Memory (Lab 2)	30 min
Data memory test bench and timing	1 hour
ALU (Lab 1)	30 min
ALU test bench and timing	1 hour
Register file (HW4)	30 min
Register file test bench (HW4)	1 hour
Control Table	2 hours
Finite State Machine (FSM)	3 hours
Fsm test bench and timing	5 hours
Instruction Register and Decoder	3 hours
IR test bench	5 hours
Total (modules):	9.5 hours
Total (test benches):	13 hours

Midpoint check-in (9 Nov)

Control Table
Schematics
All the modules
Working test benches for modules

Due 14 Nov

Integrate Modules	1 hour
Assembly Coding/ MARS testing	4 hours

Due 18 Nov

Synthesis	5 hours
synthesize design with Vivado to collect performance/area data	
Final Debugging	24 hours
Report	4 hours