AISHWARYA UPHAD

PROFILE

M-Tech fresher with specialization in ICT domain. Familiar with Verilog, System Verilog, UVM and ARM Assembly language, ADS, MATLAB tools used in current VLSI industry, research and academics. My interest includes VLSI Verification and digital systems. I am not bounded by this domain but would like to work in the field of VLSI. I am passionate and eager to learn new technologies and enhance my skill sets.

CONTACT

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KNOWLEDGE

- RTL Coding
- FSM based design
- Simulation
- Code Coverage
- Synthesis
- Static Timing Analysis

VLSI DOMAIN SKILLS

- Understanding of ASIC and FPGA design flow
- Writing RTL models using Verilog HDL
- Writing Test Benches using System Verilog and UVM
- Coverage Driven Verification
- Assertion Based Verification

EDUCATION

Dhirubhai Ambani Institute of Information and Communication Technology
2017 - 2019
Master of Technology (M-Tech) in Information and Communication Technology with CGPA of 6.5.

Mumbai University
2012 - 2016
Bachelors of Engineering with specialization in Electrical engineering with CGPA of 7.53.

St. Joseph High School, CBSE
2010 - 2012
Higher Senior Secondary with CGPA of 7.23.

Carmel School, CBSE
Senior Secondary with CGPA of 9.4.

SKILLS

[Programming Language(s)]

- UVM
- System Verilog (HVL)
- Verilog (HDL)
- Assembly language (ARM)
- LT Spice
- MATLAB
- C (Basic)

[Tool and Technologies]

- Xilinx ISE
- Questa Sim – Mentor Graphics (EDA tool)
- Riviera Pro- Aldec (EDA tool)
- MATLAB
- HFSS (High Frequency Structured Simulator)
- ADS (Advanced Design Software)
- Diptrace (PCB fabrication software)
- LINUX and Windows (Operating Systems)

[Technical Elective(s)]

Digital logic design, VLSI Subsystem design, Wireless Communication, Microwave Engineering, Antenna Theory and Propagation.

EXPERIENCE AND TRAINING

MAVEN Silicon Softech Pvt Ltd
[Sept,2019-Present]
Undergoing Advanced VLSI training for Design and Verification using Verilog, System Verilog and UVM Methodologies.

VLSI PROJECTS

[UART-IP core-Verification]
[Feb,2020]-[March,2020]
HVL : System Verilog
TB Methodology: UVM
EDA Tools: Questa Sim

Description: The UART IP core provides serial communication capabilities, which allow communication with modem or other external devices. UART will operate in three different modes – Simplex mode, Full Duplex mode and loopback mode.

Responsibilities:

- Architected the class based verification environment in UVM
- Defined Verification Plan
- Verified the RTL module using System Verilog
- Generated functional and code coverage for the RTL verification sign-off

[Design and Verification of Router 1*3]
[Oct, 2019]-[Nov, 2019]
HDL: Verilog
HVL: SystemVerilog
TB Methodology: UVM
EDA Tools: Questasim and ISE

Description: The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2.

Responsibilities:

- Architected the block level structure for the design
- Implemented RTL using Verilog HDL.
- Architected the class based verification environment using System Verilog.
- Verified the RTL model using System Verilog.
- Generated functional and code coverage for the RTL verification sign-off.

[Design of Low Noise Amplifier]
[Mar, 2018]-[Nov, 2018]
Design simulation of low noise amplifier using Advance design software (ADS). The design methodology required the design of proper DC biasing network, the analysis of the resistor stability, input and output matching network selection. The design is for the specification of single layer NE3210S01 at 2.4 GHz.

[CMOS Analog Design]
[Feb, 2018]–[April, 2018]
Designing of analog circuits for Cascoded telescopic amplifier for the required specification using LTSpice and Verilog.

OTHER PROJECTS

[Antenna Design and Forward Problem Solution for Brain Stroke Detection using Microwave Imaging] [M-Tech Thesis]
[June, 2018]-[June, 2019]
To test the capability of the system to detect brain injuries and stroke in the frequency range of 1 GHz to 4 GHz to accurately detect the presence and location of the stroke. Along with Antenna Fabrication and Measurement.

[Machine Learning and Pattern Recognition]
[Jan, 2018]–[April, 2018]
Slideshow Presentation Control Through Hand Pattern Recognition Using Web Camera using MATLAB.

[Control of Inverter via a Virtual Capacitor to achieve capacitive output impedance] [Bachelors Project]
[Dec, 2015]–[Mar, 2016]
Control Strategy involving feedback of the inductor current through an integrator which is actually the impedance of a virtual capacitor using MATLAB Simulink blocks.

ACHIEVEMENTS

Qualified GATE Exam in 2017.
Won best paper award for the topic "Control of Inverter via a Virtual Capacitor to achieve output impedance" in inter-college competition.
Teaching Assistant for Digital Communication.
Teaching Assistant for Digital Logic Design.
Teaching Assistant for Probability and Statistics.