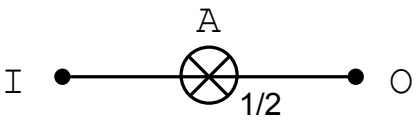
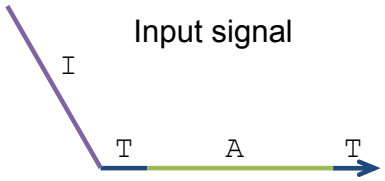
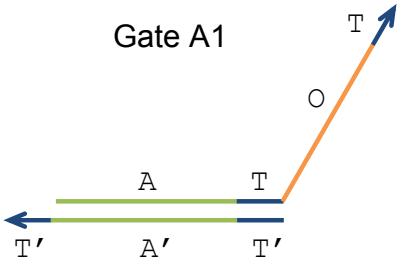
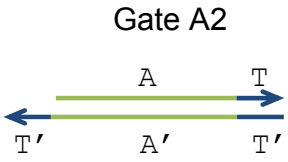
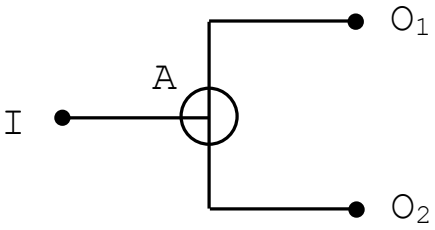

A
I
O
1/2

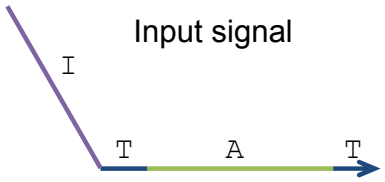

Input signal
I
T
A
T

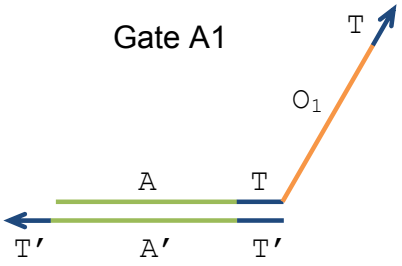

Gate A1
T
O
A
T
T′
A′
T′

[A1] = [A2]

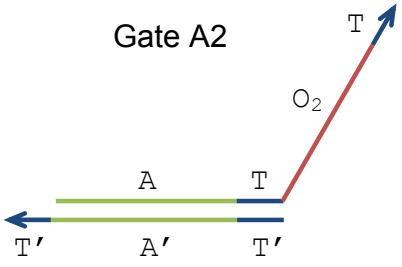

Gate A2
A
T
T′
A′
T′


O1
A
I
O2


Input signal
I
T
A
T


Gate A1
T
O1
A
T
T′
A′
T′

[A1] = [A2]


Gate A2
T
O2
A
T
T′
A′
T′