1. Description

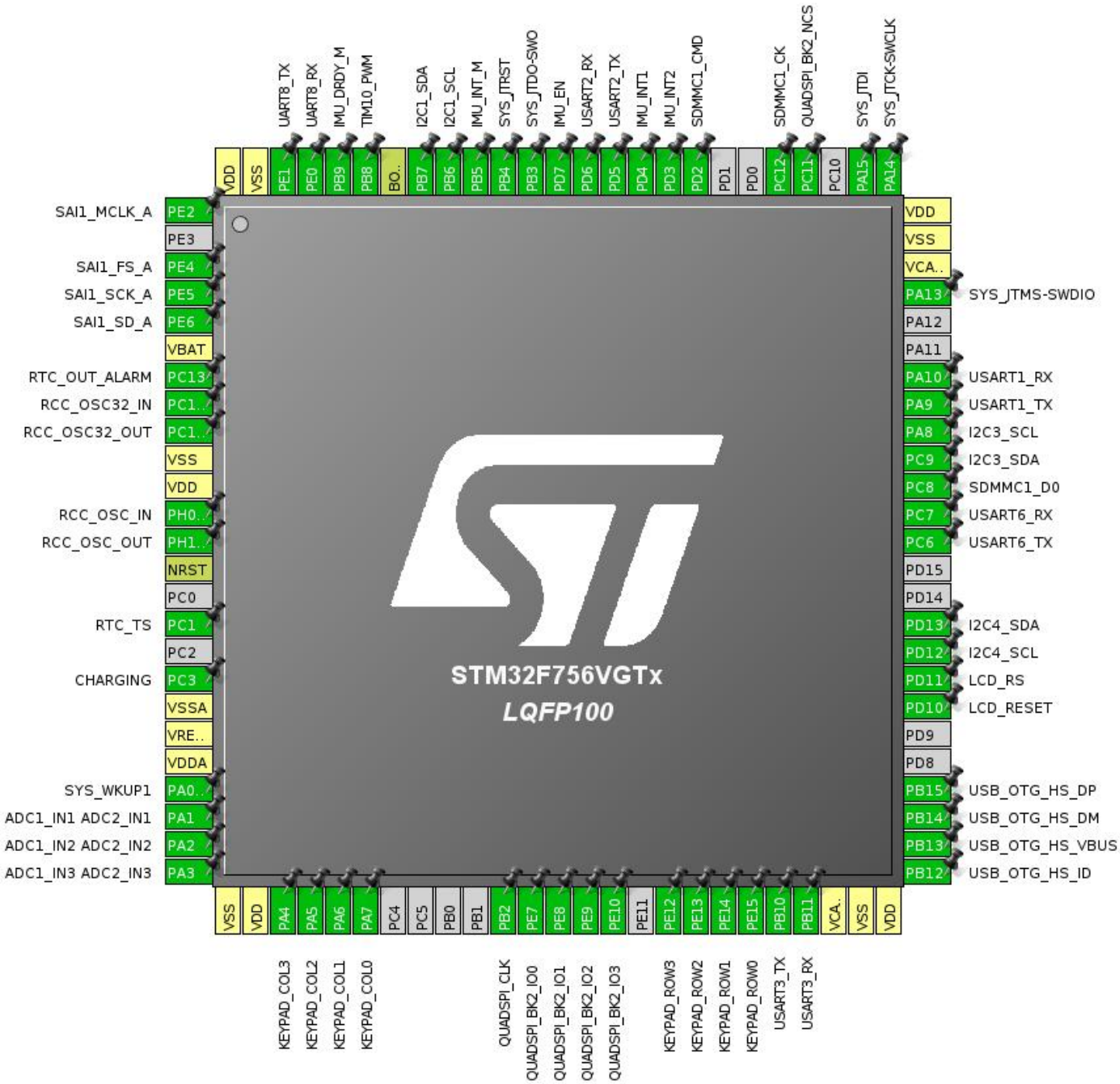
1.1. Project

Project Name	BIOS
Board Name	BIOS
Generated with:	STM32CubeMX 4.22.0
Date	09/06/2017

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x6
MCU name	STM32F756VGTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

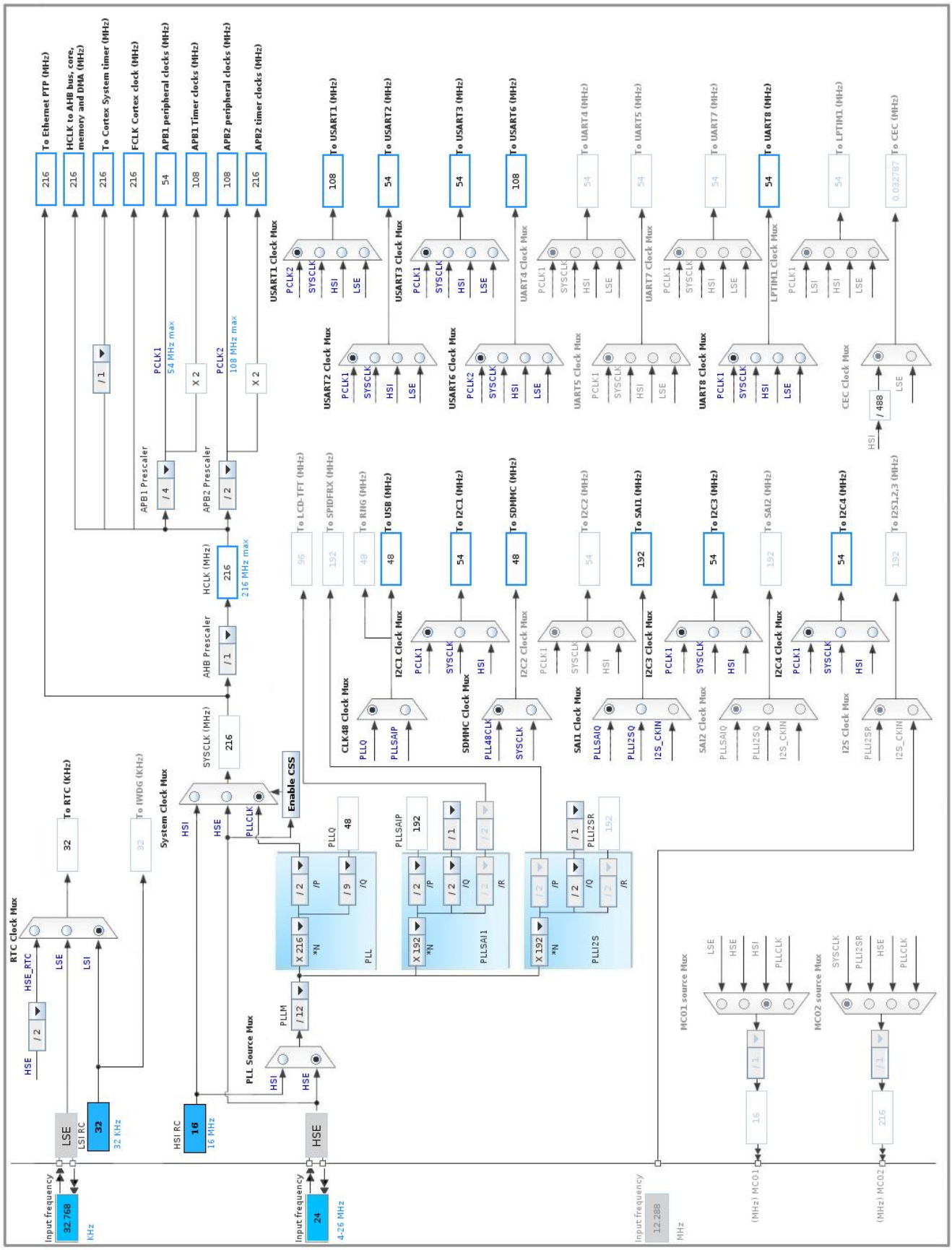
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SAI1_MCLK_A	
3	PE4	I/O	SAI1_FS_A	
4	PE5	I/O	SAI1_SCK_A	
5	PE6	I/O	SAI1_SD_A	
6	VBAT	Power		
7	PC13	I/O	RTC_OUT_ALARM	
8	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0/OSC_IN	I/O	RCC_OSC_IN	
13	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
16	PC1	I/O	RTC_TS	
18	PC3 *	I/O	GPIO_Input	CHARGING
19	VSSA	Power		
20	VREF+	Power		
21	VDDA	Power		
22	PA0/WKUP	I/O	SYS_WKUP1	
23	PA1	I/O	ADC1_IN1, ADC2_IN1	
24	PA2	I/O	ADC1_IN2, ADC2_IN2	
25	PA3	I/O	ADC1_IN3, ADC2_IN3	
26	VSS	Power		
27	VDD	Power		
28	PA4 *	I/O	GPIO_Output	KEYPAD_COL3
29	PA5 *	I/O	GPIO_Output	KEYPAD_COL2
30	PA6 *	I/O	GPIO_Output	KEYPAD_COL1
31	PA7 *	I/O	GPIO_Output	KEYPAD_COL0
36	PB2	I/O	QUADSPI_CLK	
37	PE7	I/O	QUADSPI_BK2_IO0	
38	PE8	I/O	QUADSPI_BK2_IO1	
39	PE9	I/O	QUADSPI_BK2_IO2	
40	PE10	I/O	QUADSPI_BK2_IO3	
42	PE12 *	I/O	GPIO_Input	KEYPAD_ROW3
43	PE13 *	I/O	GPIO_Input	KEYPAD_ROW2
44	PE14 *	I/O	GPIO_Input	KEYPAD_ROW1

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
45	PE15 *	I/O	GPIO_Input	KEYPAD_ROW0
46	PB10	I/O	USART3_TX	
47	PB11	I/O	USART3_RX	
48	VCAP_1	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	USB_OTG_HS_ID	
52	PB13	I/O	USB_OTG_HS_VBUS	
53	PB14	I/O	USB_OTG_HS_DM	
54	PB15	I/O	USB_OTG_HS_DP	
57	PD10 *	I/O	GPIO_Output	LCD_RESET
58	PD11 *	I/O	GPIO_Output	LCD_RS
59	PD12	I/O	I2C4_SCL	
60	PD13	I/O	I2C4_SDA	
63	PC6	I/O	USART6_TX	
64	PC7	I/O	USART6_RX	
65	PC8	I/O	SDMMC1_D0	
66	PC9	I/O	I2C3_SDA	
67	PA8	I/O	I2C3_SCL	
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15	I/O	SYS_JTDI	
79	PC11	I/O	QUADSPI_BK2_NCS	
80	PC12	I/O	SDMMC1_CK	
83	PD2	I/O	SDMMC1_CMD	
84	PD3 *	I/O	GPIO_Input	IMU_INT2
85	PD4 *	I/O	GPIO_Input	IMU_INT1
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
88	PD7 *	I/O	GPIO_Output	IMU_EN
89	PB3	I/O	SYS_JTDO-SWO	
90	PB4	I/O	SYS_JTRST	
91	PB5 *	I/O	GPIO_Input	IMU_INT_M
92	PB6	I/O	I2C1_SCL	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
95	PB8	I/O	TIM10_CH1	TIM10_PWM
96	PB9 *	I/O	GPIO_Input	IMU_DRDY_M
97	PE0	I/O	UART8_RX	
98	PE1	I/O	UART8_TX	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN1

mode: IN2

mode: IN3

mode: Vbat Channel

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 6 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. ADC2

mode: IN1

mode: IN2
mode: IN3

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 6 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.3. I2C1

I2C: I2C

5.3.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0

Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.4. I2C3

I2C: I2C

5.4.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.5. I2C4

I2C: I2C

5.5.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode

I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x20404768 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

5.6. QUADSPI

QuadSPI Mode: Bank2 with Quad SPI Lines

5.6.1. Parameter Settings:

General Parameters:

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low
Flash ID	Flash ID 2
Dual Flash	Disabled

5.7. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

5.7.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Enabled
Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

5.8. RTC

mode: Activate Clock Source
mode: Activate Calendar
Alarm A: Internal Alarm A
Alarm B: Routed to OUT
WakeUp: Internal WakeUp
mode: Timestamp

5.8.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255
Output Polarity	Output Polarity High
Output Type	Output Type Opendrain

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

Alarm A:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

Alarm B:

Hours	0
Minutes	0
Seconds	0
Sub Seconds	0
Alarm Mask Date Week day	Disable
Alarm Mask Hours	Disable
Alarm Mask Minutes	Disable
Alarm Mask Seconds	Disable
Alarm Sub Second Mask	All Alarm SS fields are masked.
Alarm Date Week Day Sel	Date
Alarm Date	1

Wake UP:

Wake Up Clock	RTCCLK / 16
Wake Up Counter	0

Time Stamp:

Time Stamp Pin Edge	Time Stamp occurs on the Rising edge

5.9. SAI1

Mode: Master with Master Clock Out

5.9.1. Parameter Settings:

SAI A:

Basic Parameters

Protocol	Free
Audio Mode	Master Transmit
Frame Length	8 bits
Data Size	24 Bits

Slot Size	DataSize
Output Mode	Stereo
Companding Mode	No companding mode
SAI SD Line Output Mode	Driven
Frame Parameters	
First Bit	MSB First
Frame Synchro Active Level Length	1
Frame Synchro Definition	Start Frame
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
Slot Parameters	
First Bit Offset	0
Number of Slots	1
Slot Active Final Value	0x00000000
Slot Active	Neither
Clock Parameters	
Master Clock Divider	Enabled
Audio Frequency	192 KHz
Real Audio Frequency	0
Error between Selected	0
Clock Strobing	Falling Edge
Advanced Parameters	
Fifo Threshold	Empty
Output Drive	Disabled
Synchronization External	Disabled

5.10. SDMMC1

Mode: SD 1 bit

5.10.1. Parameter Settings:

SDMMC parameters:

SDMMCCLK clock divide factor	0

5.11. SYS

Debug: JTAG (5 pins)

mode: System Wake-Up 1

Timebase Source: SysTick

5.12. TIM10

mode: Activated

Channel1: PWM Generation CH1

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.13. UART8

Mode: Asynchronous

5.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable

Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.14. USART1

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.15. USART2

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200

Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.16. USART3

Mode: Asynchronous

5.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable

MSB First	Disable

5.17. USART6

Mode: Asynchronous

5.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	7 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

5.18. USB_OTG_HS

Internal FS Phy: OTG/Dual_Role_Device

mode: Activate_VBUS

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC1_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC1_IN3	Analog mode	No pull-up and no pull-down	n/a	
ADC2	PA1	ADC2_IN1	Analog mode	No pull-up and no pull-down	n/a	
	PA2	ADC2_IN2	Analog mode	No pull-up and no pull-down	n/a	
	PA3	ADC2_IN3	Analog mode	No pull-up and no pull-down	n/a	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
	PA8	I2C3_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
I2C4	PD12	I2C4_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PD13	I2C4_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
QUADSPI	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE7	QUADSPI_BK2_IO0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE8	QUADSPI_BK2_IO1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE9	QUADSPI_BK2_IO2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE10	QUADSPI_BK2_IO3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC11	QUADSPI_BK2_NCS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
RTC	PC13	RTC_OUT_ALARM	n/a	n/a	n/a	
	PC1	RTC_TS	n/a	n/a	n/a	
SAI1	PE2	SAI1_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE4	SAI1_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE5	SAI1_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE6	SAI1_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA0/WKUP	SYS_WKUP1	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA15	SYS_JTDI	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
	PB4	SYS_JTRST	n/a	n/a	n/a	
TIM10	PB8	TIM10_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM10_PWM
UART8	PE0	UART8_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PE1	UART8_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART2	PD5	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PD6	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART3	PB10	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB11	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART6	PC6	USART6_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PC7	USART6_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USB_OTG_HS	PB12	USB_OTG_HS_ID	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	USB_OTG_HS_VBUS	Input mode	No pull-up and no pull-down	**n/a**	
	PB14	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB15	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PC3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CHARGING
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KEYPAD_COL3
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KEYPAD_COL2
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KEYPAD_COL1
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	KEYPAD_COL0
	PE12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KEYPAD_ROW3
	PE13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KEYPAD_ROW2
	PE14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KEYPAD_ROW1
	PE15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	KEYPAD_ROW0
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RESET
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LCD_RS
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IMU_INT2
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IMU_INT1
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IMU_EN
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IMU_INT_M
	PB9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IMU_DRDY_M

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD interrupt through EXTI line 16	unused		
RTC tamper and timestamp interrupts through EXTI line 21	unused		
RTC wake-up interrupt through EXTI line 22	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
RTC alarms (A and B) interrupt through EXTI line 17	unused		
SDMMC1 global interrupt	unused		
USART6 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
UART8 global interrupt	unused		
SAI1 global interrupt	unused		
QUADSPI global interrupt	unused		
I2C4 event interrupt	unused		
I2C4 error interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x6
MCU	STM32F756VGTx
Datasheet	027589_Rev4

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	BIOS
Project Folder	/home/bastian/Dokumente/NokiaRetroFit/firmware/bios/BIOS
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.7.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes