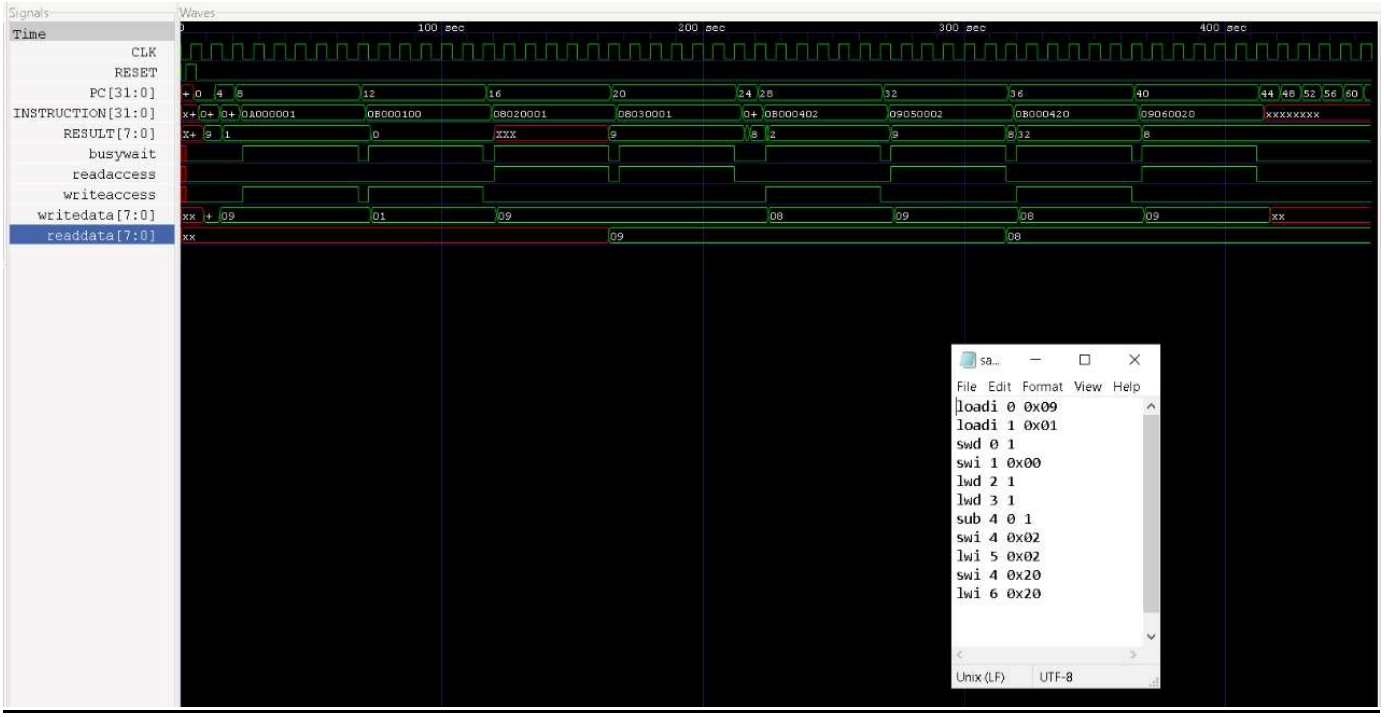
LAB 06: BUILDING A MEMORY HIERARCHY

PART II: DATA CACHE

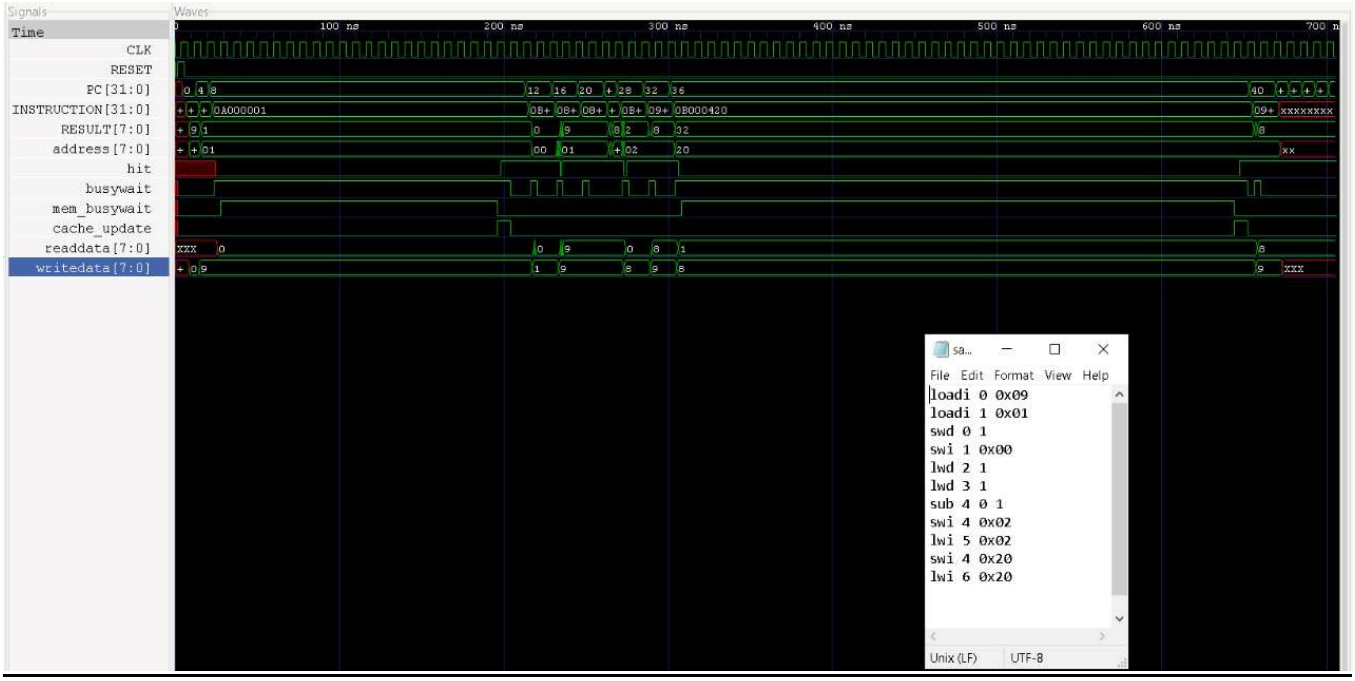
GROUP 30

In the part I of this lab we have added a memory sub-system to our single-cycle CPU. In part II we have to implement data cache in our CPU. when we implemented data cache, we can see that the timings have become less than the timings of the part II. we have added timing diagrams of both of those parts running them with the same sample program below.

Timing diagram of part 1



Timing diagram of part 2



When comparing to timing diagram of part II with part I we can see that the 1st swd instructions takes more time in part II. that because we have no data memory in the cache at the beginning. after that the cache get the data so it directly passes the data to the CPU. because of that it reduces the timings of next instructions compare to part 1.