An Exercise in Optimizing Matrix-Matrix Multiplication

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Abstract

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1 Introduction

In this exercise, we are going to optimize GEMM (General Matrix-Matrix Multiplication) on modern computer architectures. Specifically, we consider the simple case:

$$C := C + A * B$$

where A, B, and C are $m \times k$, $k \times n$, $m \times n$ matrices, respectively. GEMM can be performed using $2mkn$ floating point operations, as illustrated in the following pseudocode:

```
for j=0 : n-1 steps of 1
  for p=0 : k-1 steps of 1
    for i=0 : m-1 steps of 1
      C(i,j) += A(i,p) B(p,j)
    endfor
  endfor
endfor
```

2 The Goto Approach to Implementing GEMM

[1] [5] [4] [2] [3]

3 Step-by-step approach to the peak performance

Architecture: Ivy Bridge and Haswell.

3.1 Naive Approach: Three loops

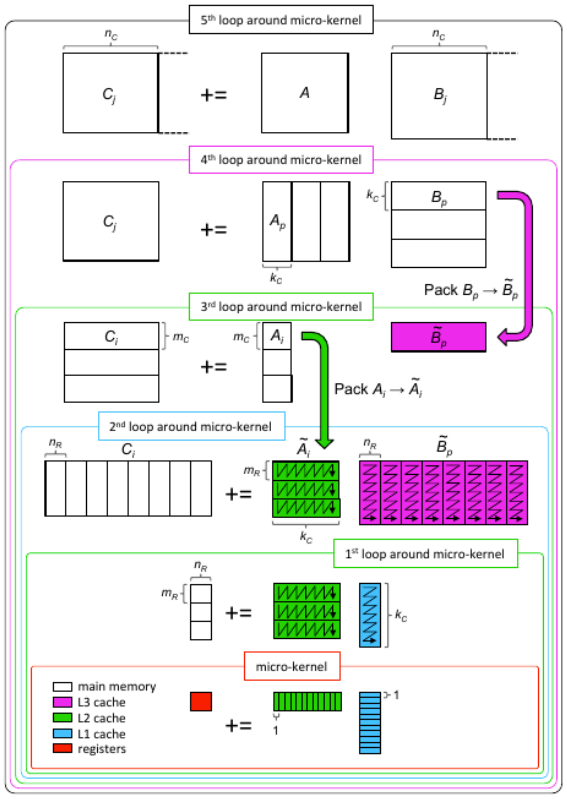
3.2 Cache Blocking: 6 loops

refer to GOTO paper: How to permuate to get the best loop order var2, var1, var3
Performance Graph

3.3 Add Packing

3.4 Micro-kernel Tricks

1. Butterfly or Broadcasting?
2. Double buffering



Loop 5 **for** $j_c = 0 : n-1$ **steps of** n_c
  $\mathcal{J}_c = j_c : j_c + n_c - 1$
Loop 4 **for** $p_c = 0 : k-1$ **steps of** k_c
    $\mathcal{P}_c = p_c : p_c + k_c - 1$
    $B(\mathcal{P}_c, \mathcal{J}_c) \rightarrow B_c$ // Pack into B_c
Loop 3 **for** $i_c = 0 : m-1$ **steps of** m_c
      $\mathcal{I}_c = i_c : i_c + m_c - 1$
      $A(\mathcal{I}_c, \mathcal{P}_c) \rightarrow A_c$ // Pack into A_c
      // Macro-kernel
Loop 2 **for** $j_r = 0 : n_c - 1$ **steps of** n_r
        $\mathcal{J}_r = j_r : j_r + n_r - 1$
Loop 1 **for** $i_r = 0 : m_c - 1$ **steps of** m_r
          $\mathcal{I}_r = i_r : i_r + m_r - 1$
          // Micro-kernel
Loop 0 **for** $k_r = 0 : k_c - 1$
            $C_c(\mathcal{I}_r, \mathcal{J}_r)$
              $+= A_c(\mathcal{I}_r, k_r)\ \ B_c(k_r, \mathcal{J}_r)$
          endfor
        endfor
      endfor
    endfor
  endfor
endfor

Figure 1: Left: The Goto algorithm for matrix-matrix multiplication as refactored in BLIS. Right: the same algorithm, but expressed as loops.

3.5 Parameter Tuning

3.6 Parallelization

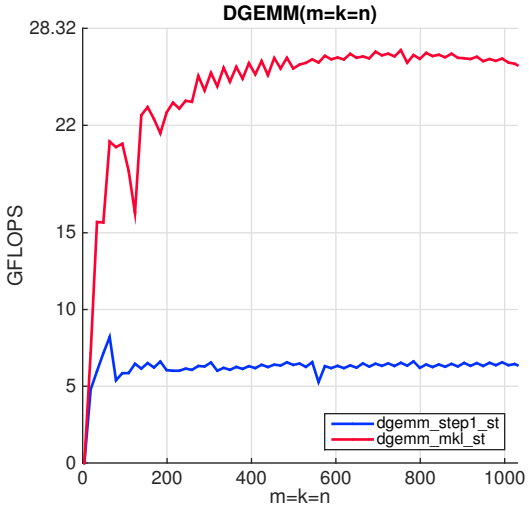


Figure 2: Step1 performance

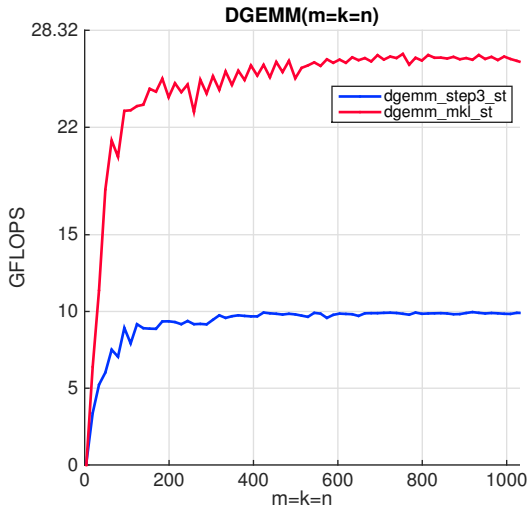


Figure 3: Step3 performance

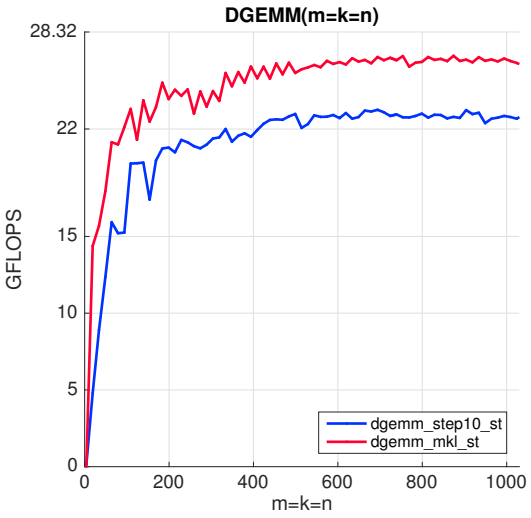


Figure 4: Step10 performance

4 Conclusion

Conclusion.

Additional information

For additional information on FLAME visit
`http://www.cs.utexas.edu/users/flame/`.

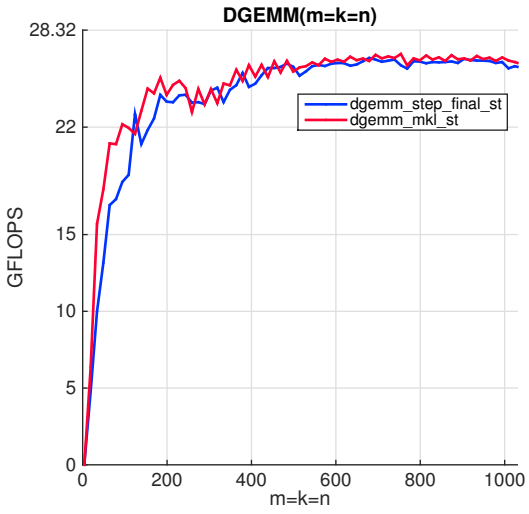


Figure 5: Step Final performance

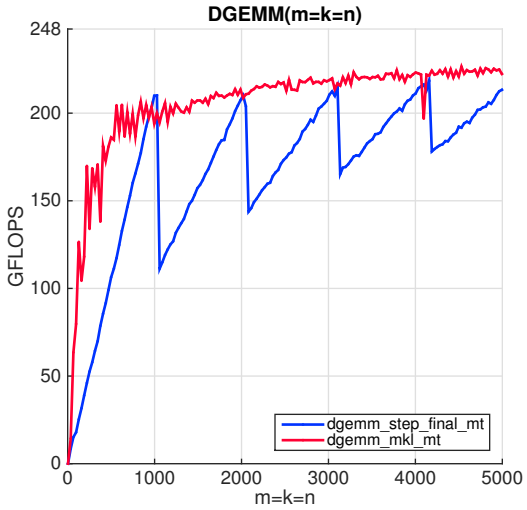


Figure 6: Step Final performance (multi-thread)

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References

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