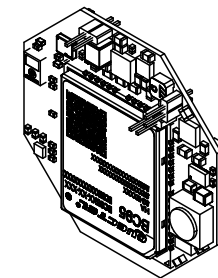


### Layer Stack Legend

	Material	Layer	Thickness	Dielectric Material	Type	Gerber
		Top Overlay			Legend	GTO
	Surface Material	Top Solder	0.03mm	SM-001	Solder Mask	GTS
	PbSn	Top Surface Finish	0.02mm		Surface Finish	
	CF-004	Top Layer	0.04mm		Signal	GTL
	Prepreg		0.07mm	PP-006	Dielectric	
	CF-004	Int1 (GND)	0.04mm		Signal	G1
	Core		0.12mm	Core-035	Dielectric	
	CF-004	Int2 (Sign)	0.04mm		Signal	G2
	Prepreg		0.07mm	PP-006	Dielectric	
	Prepreg		0.07mm	PP-006	Dielectric	
	CF-004	Int3 (GND)	0.04mm		Signal	G3
	Core		0.12mm	Core-035	Dielectric	
	CF-004	Int4 (PWR)	0.04mm		Signal	G4
	Prepreg		0.07mm	PP-006	Dielectric	
	CF-004	Bottom Layer	0.04mm		Signal	GBL
	PbSn	Bottom Surface Finish	0.02mm		Surface Finish	
	Surface Material	Bottom Solder	0.03mm	SM-001	Solder Mask	GBS
		Bottom Overlay			Legend	GBO

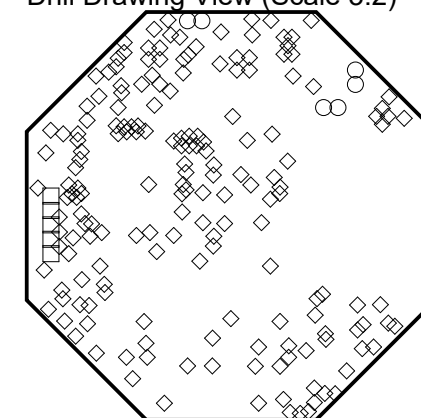
Total thickness: 0.83mm



## Drill Table

Symbol	Count	Hole Size	Plated	Via / Pad
◇	180	0.20mm	Plated	Via
○	6	0.60mm	Plated	Pad
□	5	0.90mm	Plated	Pad
191 Total				

### Drill Drawing View (Scale 3:2)



Eidgenössische Technische Hochschule Zürich  
Swiss Federal Institute of Technology Zurich

Project:

## H-Watch Manufacturing

Drawing number: MANV0.2

Rev: V0.2

Format:	Laboratory: <a href="#">ETH-PBL</a>
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A4 Q

Drawn by: schuluka, polonelli

Sheet: H-Watch manufacturing.F

Page 1 of 1

File: C:\Users\schuluka\Git\Github\H-Watch\Hardware\H-Watch V0.2\H-Watch manufacturing.PCBDwf