ETHZurich

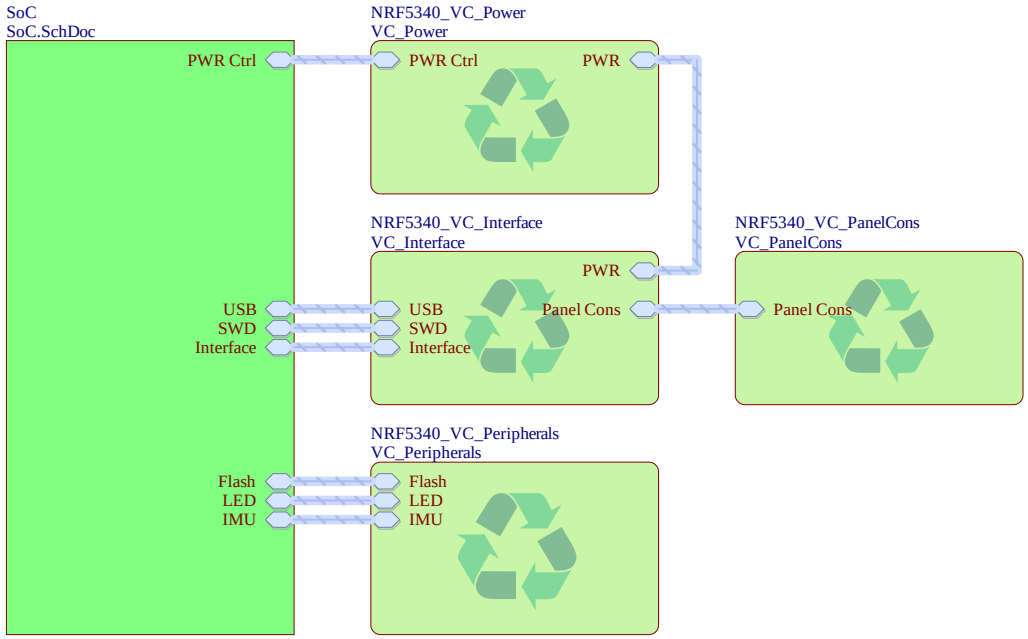
Logo ETH Zurich

VitalCore

Logo VitalCore

Vitalcore ETH

Logo Vitalcore ETH



ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: VitalCore: NRF5340

Overview

Laboratory: D-ITET PBL

Date: 3/4/2024 2:21:37 PM

Rev: 1.3 License: GNU GPL v3

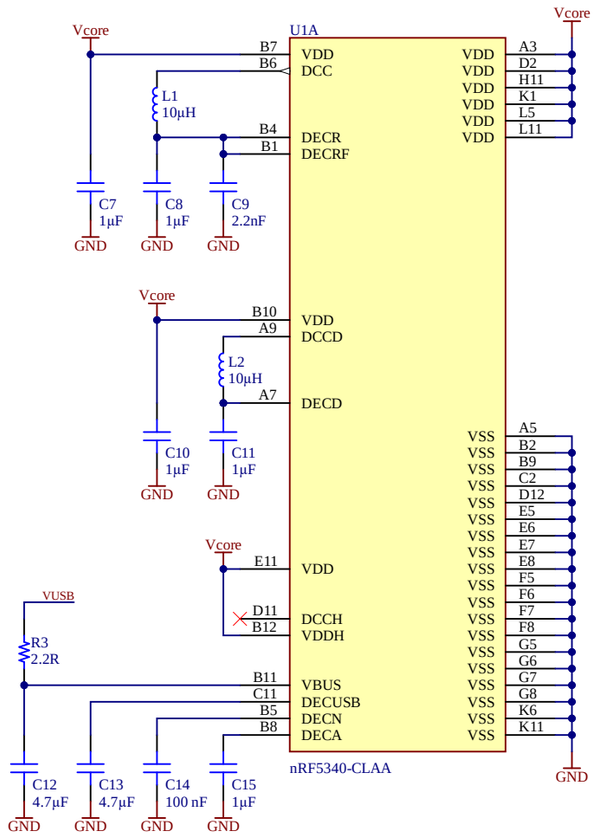
Variant: Complete

Drawn By: Philipp Schilk, Alfonso Blanco Fontao

Checked By: Federico Villani, Lukas Schulthess

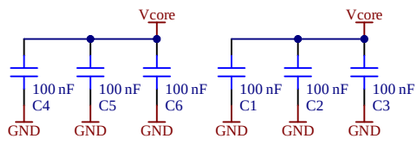
File: VC_NRF5340.SchDoc

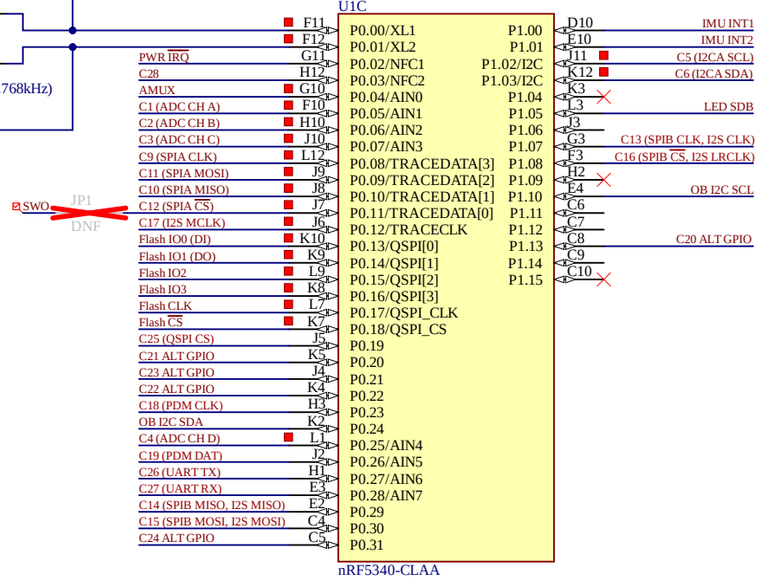
Sheet: 1 / 6



Based on CLAA sample configuration 2 (DS v1.3 pg. 812)

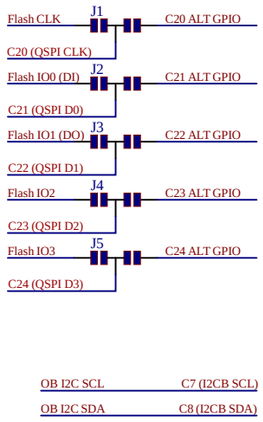
DCCH left NC if VREGH is not used (DS v1.3 pg 52)

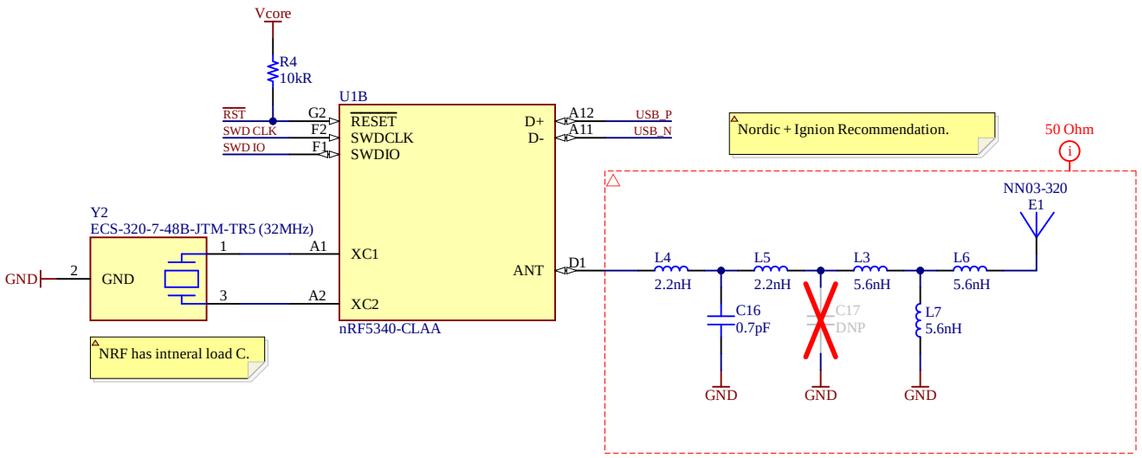




Red box indicates that signal cannot be freely re-assigned to another pin.

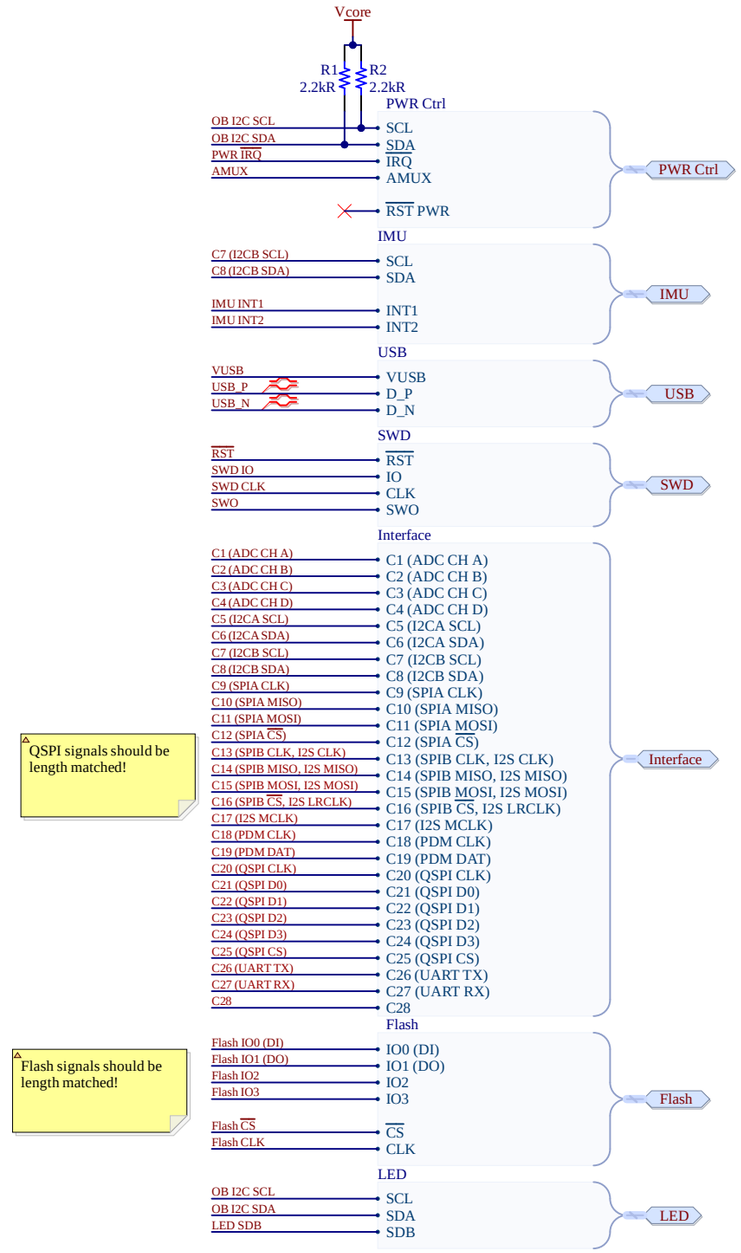
Jumper on SWO line enables SWO to be disconnected if SPI is used in high-speed mode, to reduce trace capacitance.





NRF has intneral load C.

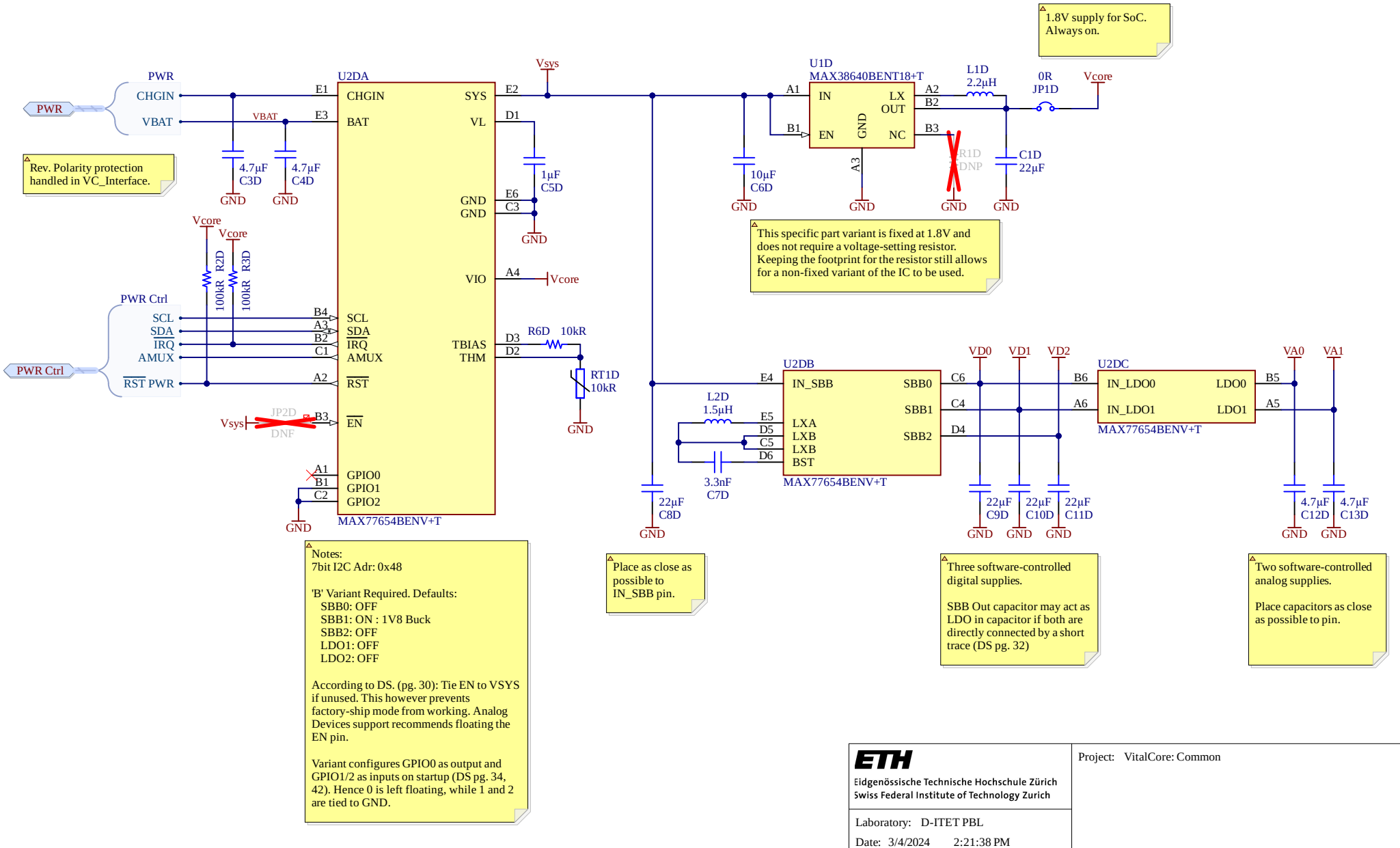
Nordic + Ignion Recommendation.

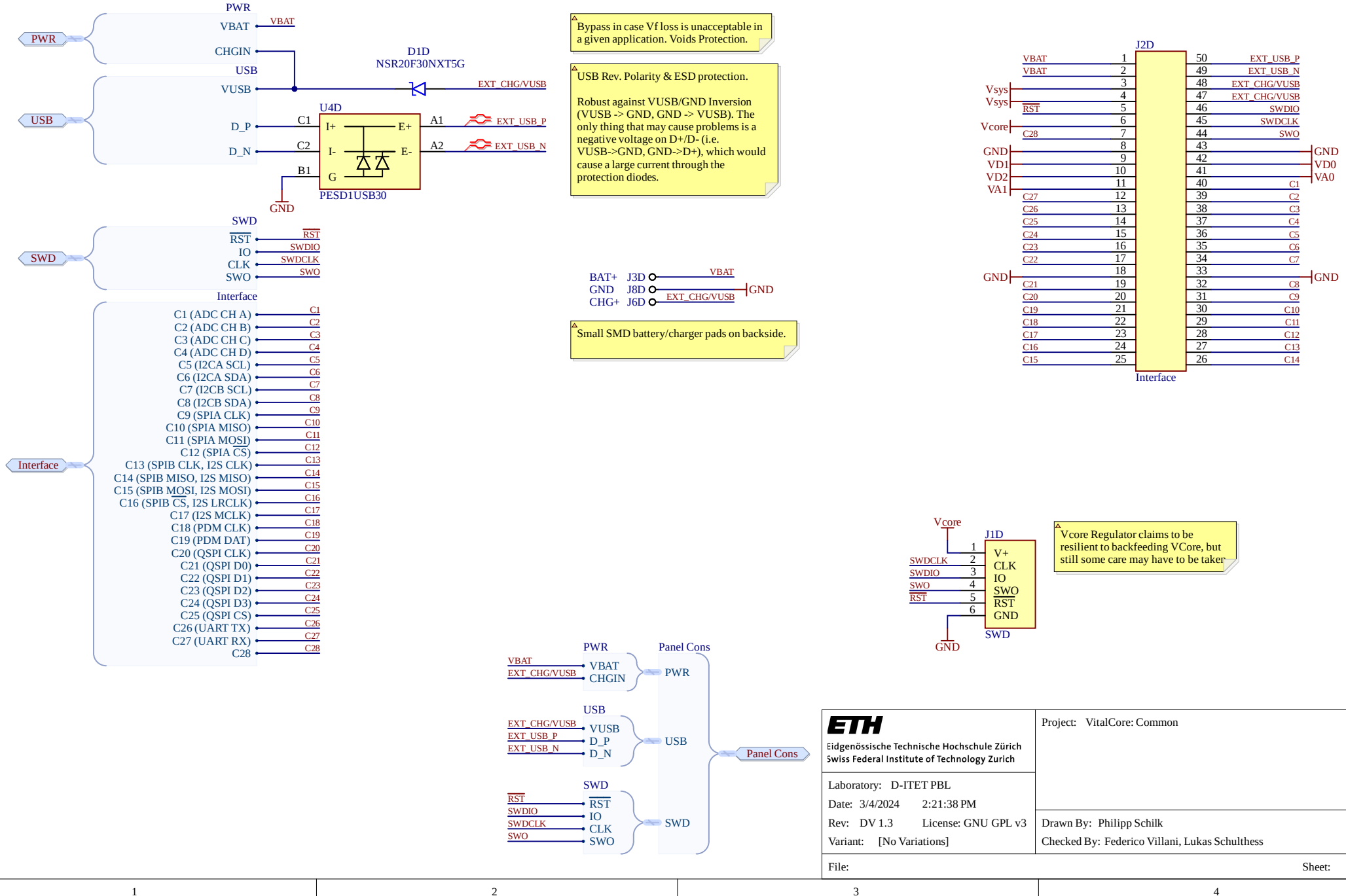


QSPI signals should be length matched!

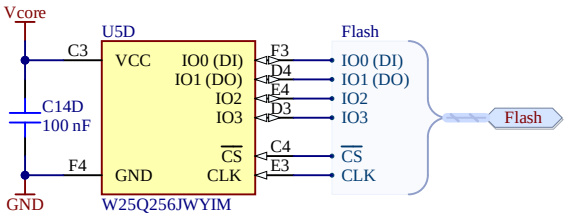
Flash signals should be length matched!

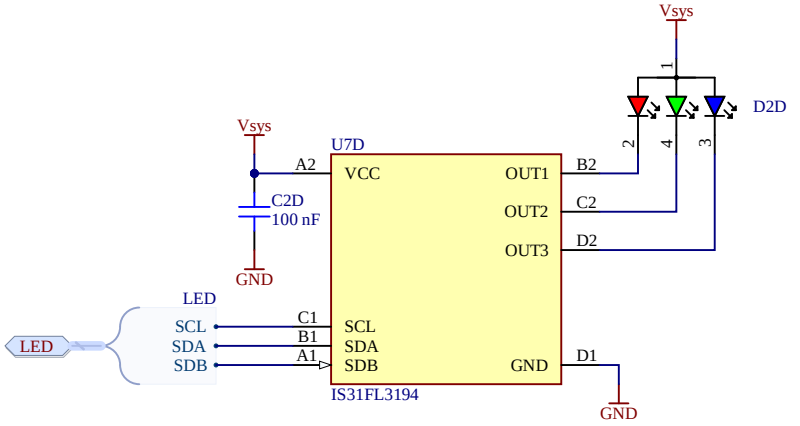
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	NRF5340 SoC, BLE Antenna
Laboratory: D-ITET PBL	
Date: 3/4/2024 2:21:37 PM	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Rev: 1.3 License: GNU GPL v3	Checked By: Federico Villani, Lukas Schulthess
Variation: Complete	
File: SoC.SchDoc	Sheet: 2 / 6

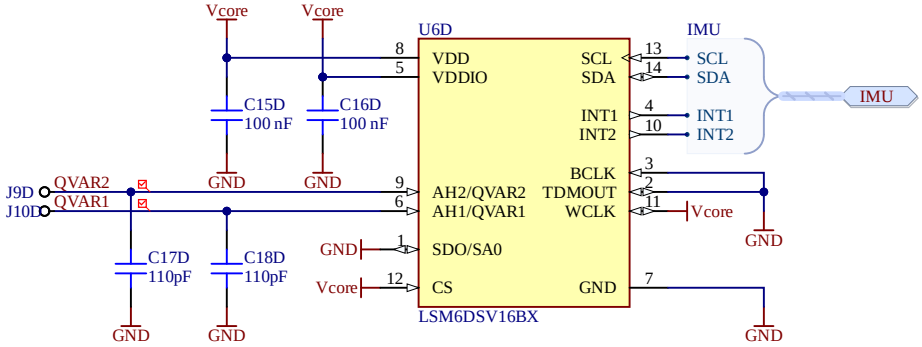

PWR
CHGIN
VBAT
Rev. Polarity protection handled in VC_Interface.
U2DA
CHGIN
BAT
SYS
VL
GND
GND
VIO
TBIAS
THM
SCL
SDA
IRQ
AMUX
RST
EN
GPIO0
GPIO1
GPIO2
MAX77654BENV+T
4.7µF C3D
4.7µF C4D
1µF C5D
R2D 100kR
R3D 100kR
PWR Ctrl
R6D 10kR
RT1D 10kR
JP2D DNF
Notes:
7bit I2C Adr: 0x48
'B' Variant Required. Defaults:
SBB0: OFF
SBB1: ON : 1V8 Buck
SBB2: OFF
LDO1: OFF
LDO2: OFF
According to DS. (pg. 30): Tie EN to VSYS if unused. This however prevents factory-ship mode from working. Analog Devices support recommends floating the EN pin.
Variant configures GPIO0 as output and GPIO1/2 as inputs on startup (DS pg. 34, 42). Hence 0 is left floating, while 1 and 2 are tied to GND.
1.8V supply for SoC. Always on.
U1D
MAX38640BENT18+T
IN
LX
OUT
EN
GND
NC
L1D 2.2µH
0R JP1D
Vcore
10µF C6D
R1D DNP
C1D 22µF
This specific part variant is fixed at 1.8V and does not require a voltage-setting resistor. Keeping the footprint for the resistor still allows for a non-fixed variant of the IC to be used.
U2DB
IN_SBB
SBB0
SBB1
SBB2
LXA
LXB
LXB
BST
MAX77654BENV+T
L2D 1.5µH
3.3nF C7D
22µF C8D
Place as close as possible to IN_SBB pin.
VD0
VD1
VD2
22µF C9D
22µF C10D
22µF C11D
Three software-controlled digital supplies.
SBB Out capacitor may act as LDO in capacitor if both are directly connected by a short trace (DS pg. 32)
U2DC
IN_LDO0
IN_LDO1
LDO0
LDO1
MAX77654BENV+T
VA0
VA1
4.7µF C12D
4.7µF C13D
Two software-controlled analog supplies.
Place capacitors as close as possible to pin.
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich
Project: VitalCore: Common
Laboratory: D-ITET PBL
Date: 3/4/2024 2:21:38 PM
Rev: DV 1.3 License: GNU GPL v3
Variant: [No Variations]
Drawn By: Philipp Schilk
Checked By: Federico Villani, Lukas Schulthess
File:
Sheet: /



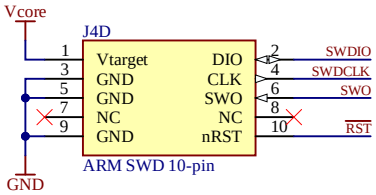
Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: Common
Laboratory: D-ITET PBL Date: 3/4/2024 2:21:38 PM Rev: DV 1.3 License: GNU GPL v3 Variant: [No Variations]	Drawn By: Philipp Schilk Checked By: Federico Villani, Lukas Schulthess
File:	Sheet: /

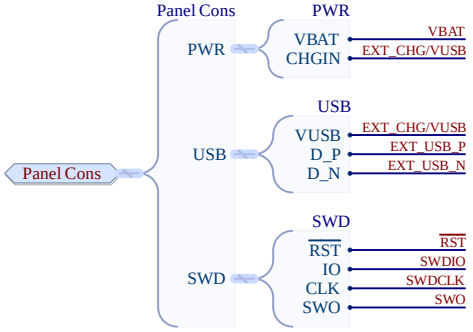


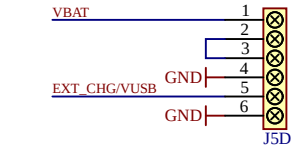


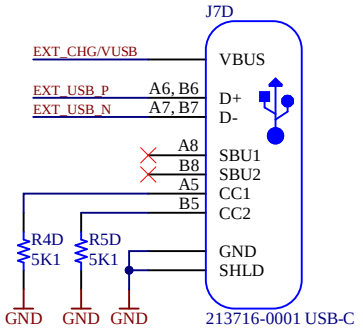


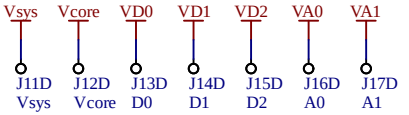
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: Common
Laboratory: D-ITET PBL Date: 3/4/2024 2:21:38 PM Rev: DV 1.3 License: GNU GPL v3 Variant: [No Variations]	Drawn By: Philipp Schilk Checked By: Federico Villani, Lukas Schulthess
File:	Sheet: /





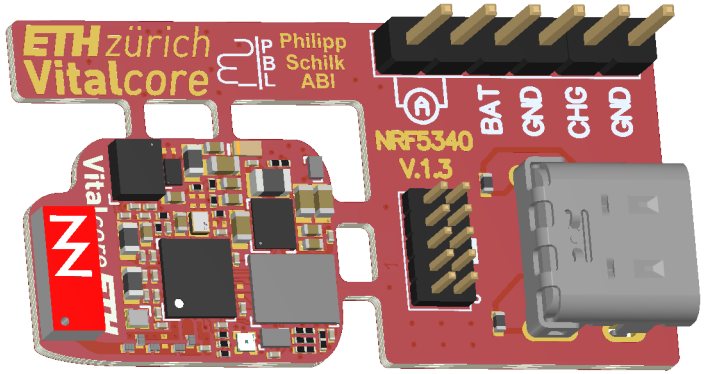




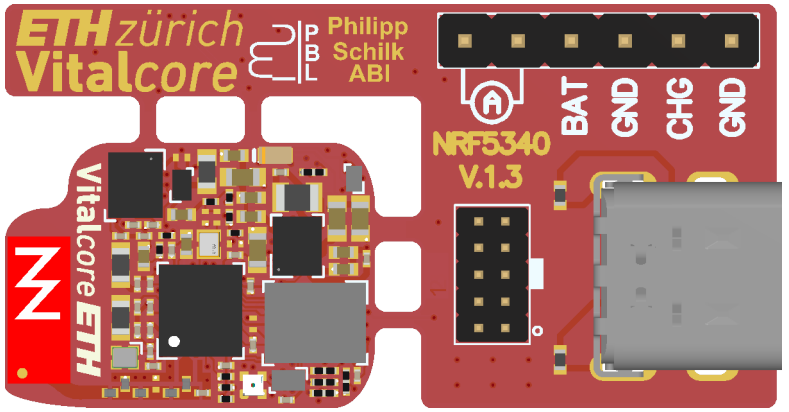


ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: Common
Laboratory: D-ITET PBL Date: 3/4/2024 2:21:38 PM Rev: DV 1.3 License: GNU GPL v3 Variant: [No Variations]	Drawn By: Philipp Schilk Checked By: Federico Villani, Lukas Schulthess
File:	Sheet: /

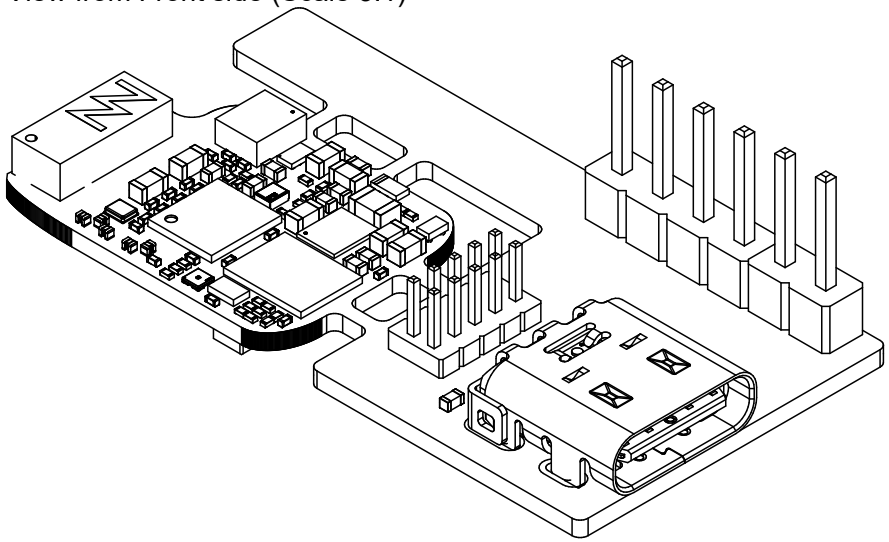
Realistic View



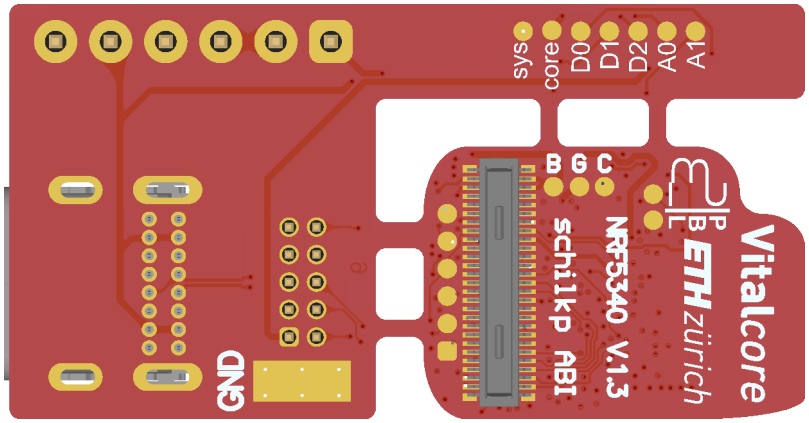
Realistic View



View from Front side (Scale 3:1)

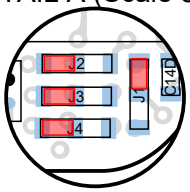


Realistic View



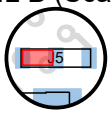
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	3D Render
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:21 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: Complete	Checked By: Federico Villani, Lukas Schulthess
File: DOC_3D.PCBDwf	Sheet: 1/1

DETAIL A (Scale 8:1)



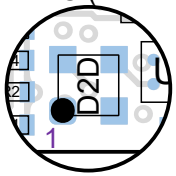
J2, J3, J4: Mount resistor from central pad to left pad
J1: Mount resistor from central pad to upper pad.

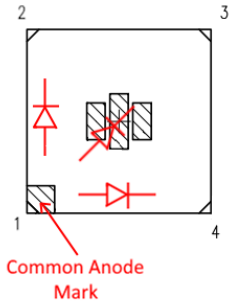
DETAIL B (Scale 8:1)



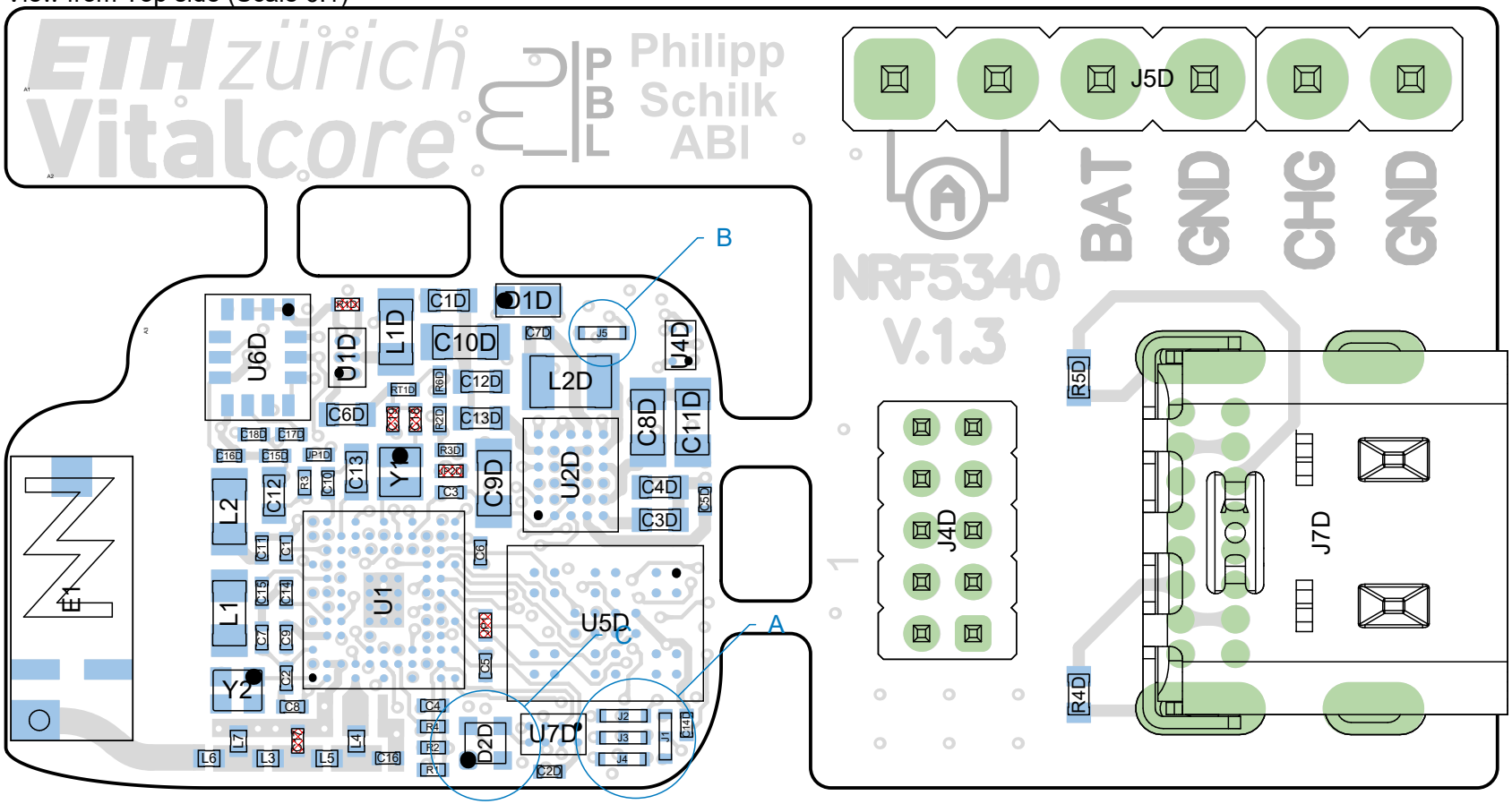
J5: mount resistor from central pad to left pad

DETAIL C (Scale 8:1)

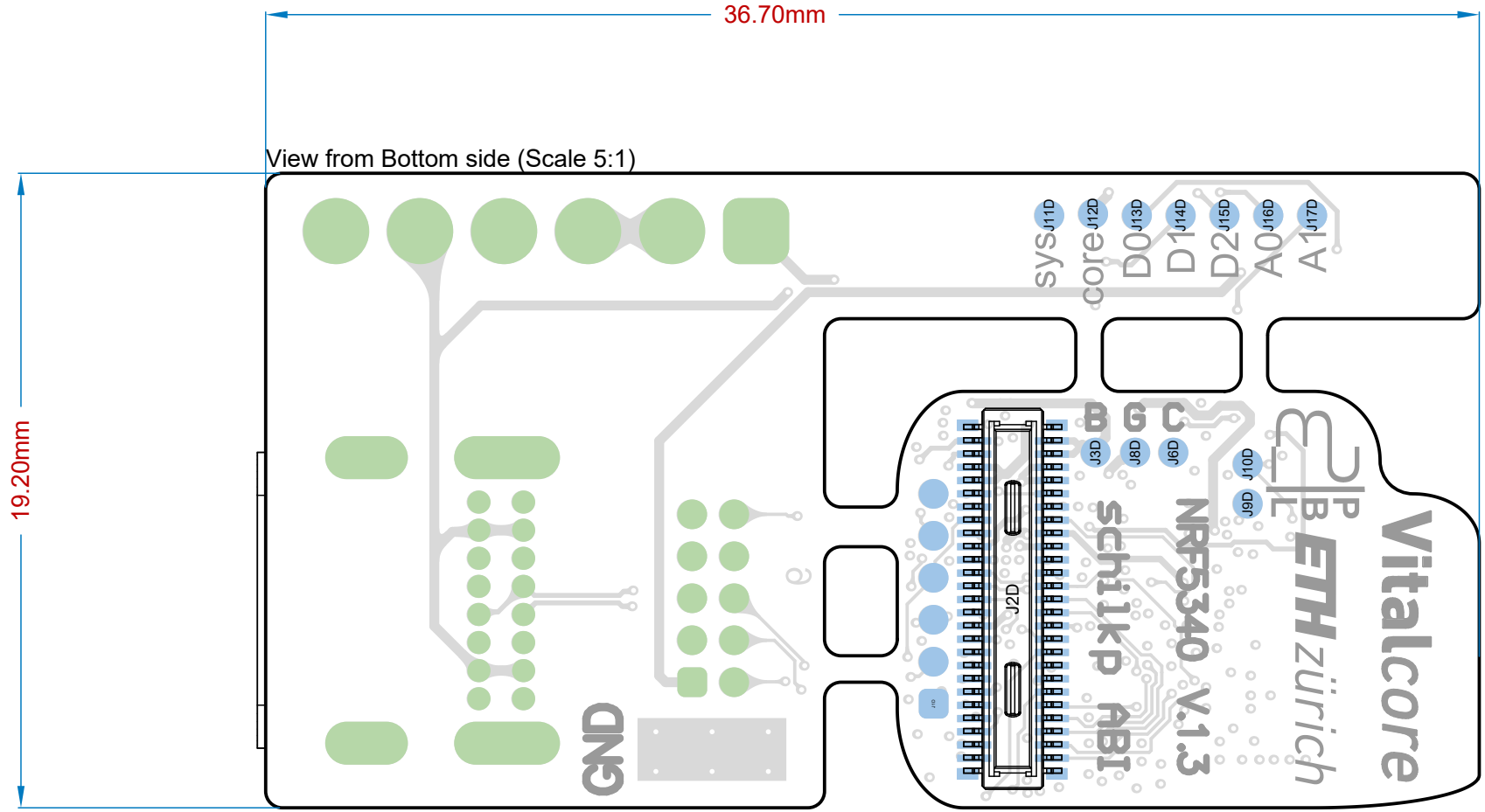




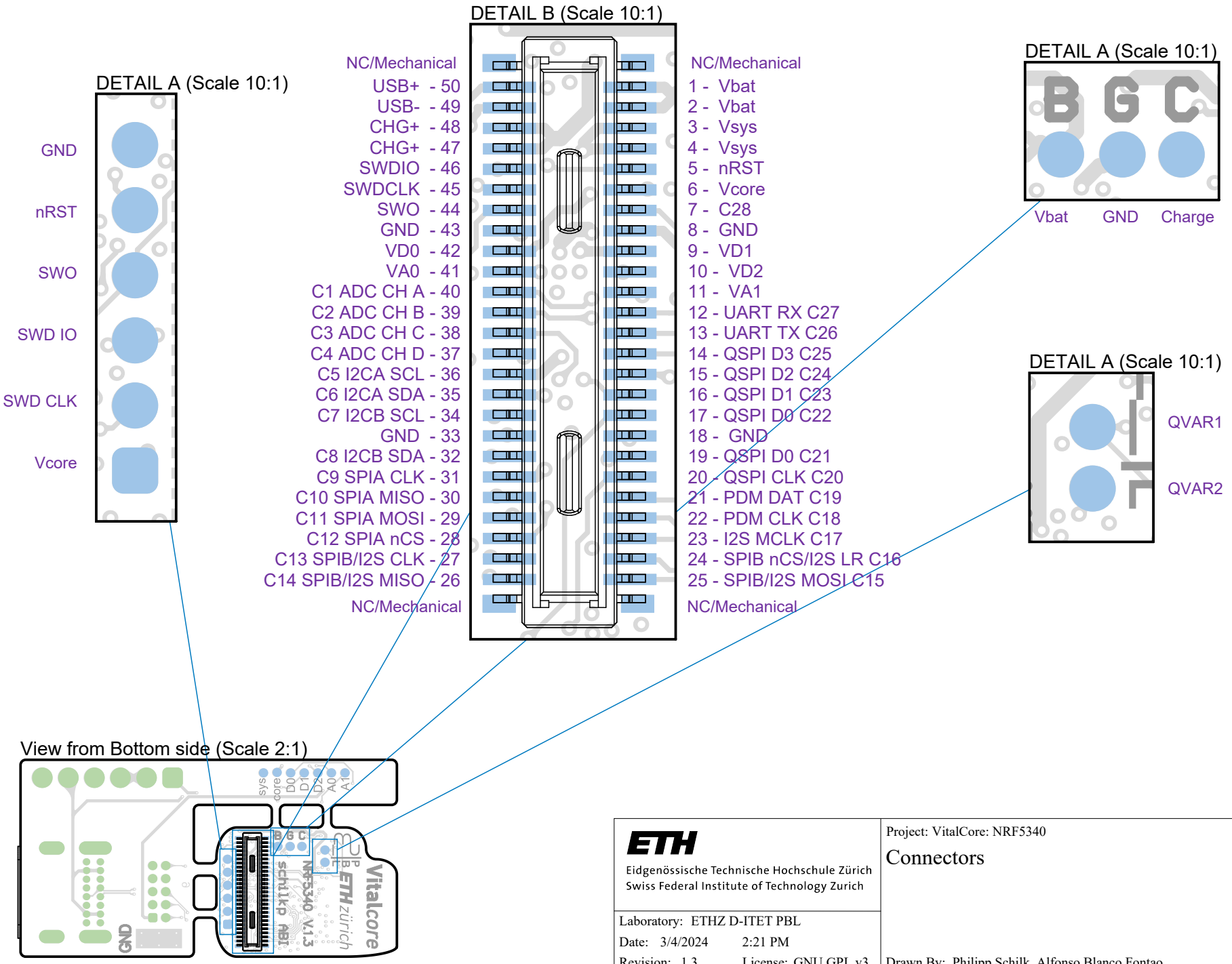
View from Top side (Scale 6:1)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Assembly
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:21 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: Complete	Checked By: Federico Villani, Lukas Schulthess
File: DOC_ASSEMBLY.PCBDwf	Sheet: 1/2



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340 Assembly
Laboratory: ETHZ D-ITET PBL Date: 3/4/2024 2:21 PM Revision: 1.3 License: GNU GPL v3 Variant: Complete	Drawn By: Philipp Schilk, Alfonso Blanco Fontao Checked By: Federico Villani, Lukas Schulthess
File: DOC_ASSEMBLY.PCBDwf	Sheet: 2/2



ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: VitalCore: NRF5340

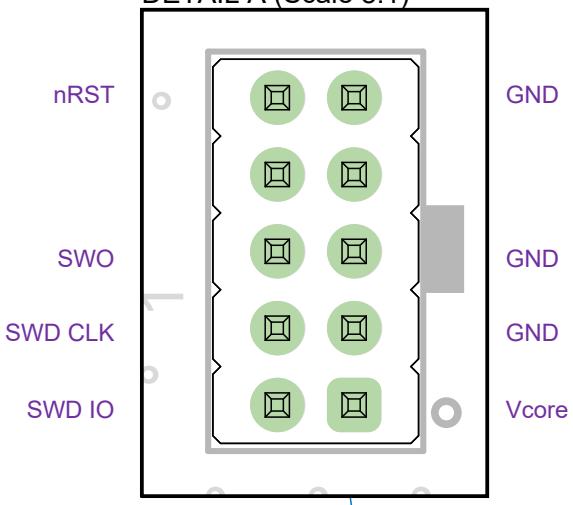
Connectors

Laboratory: ETHZ D-ITET PBL
Date: 3/4/2024 2:21 PM
Revision: 1.3 License: GNU GPL v3
Variant: Complete

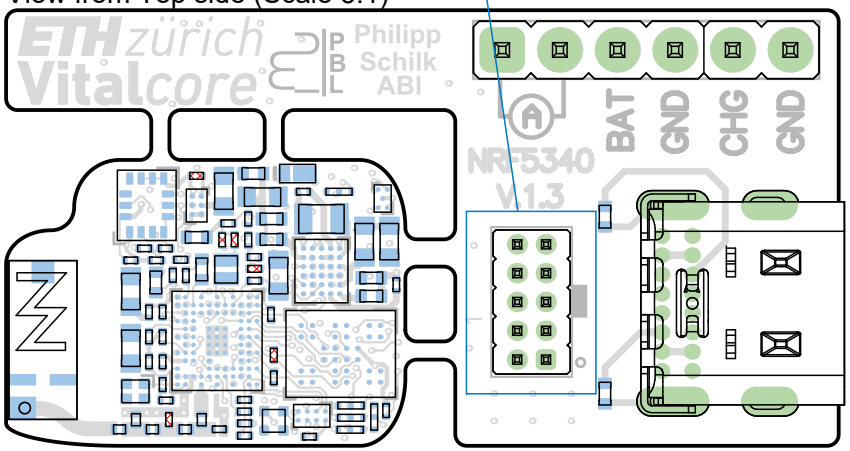
Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Checked By: Federico Villani, Lukas Schulthess

File: DOC_CONN.PCBDwf

DETAIL A (Scale 8:1)

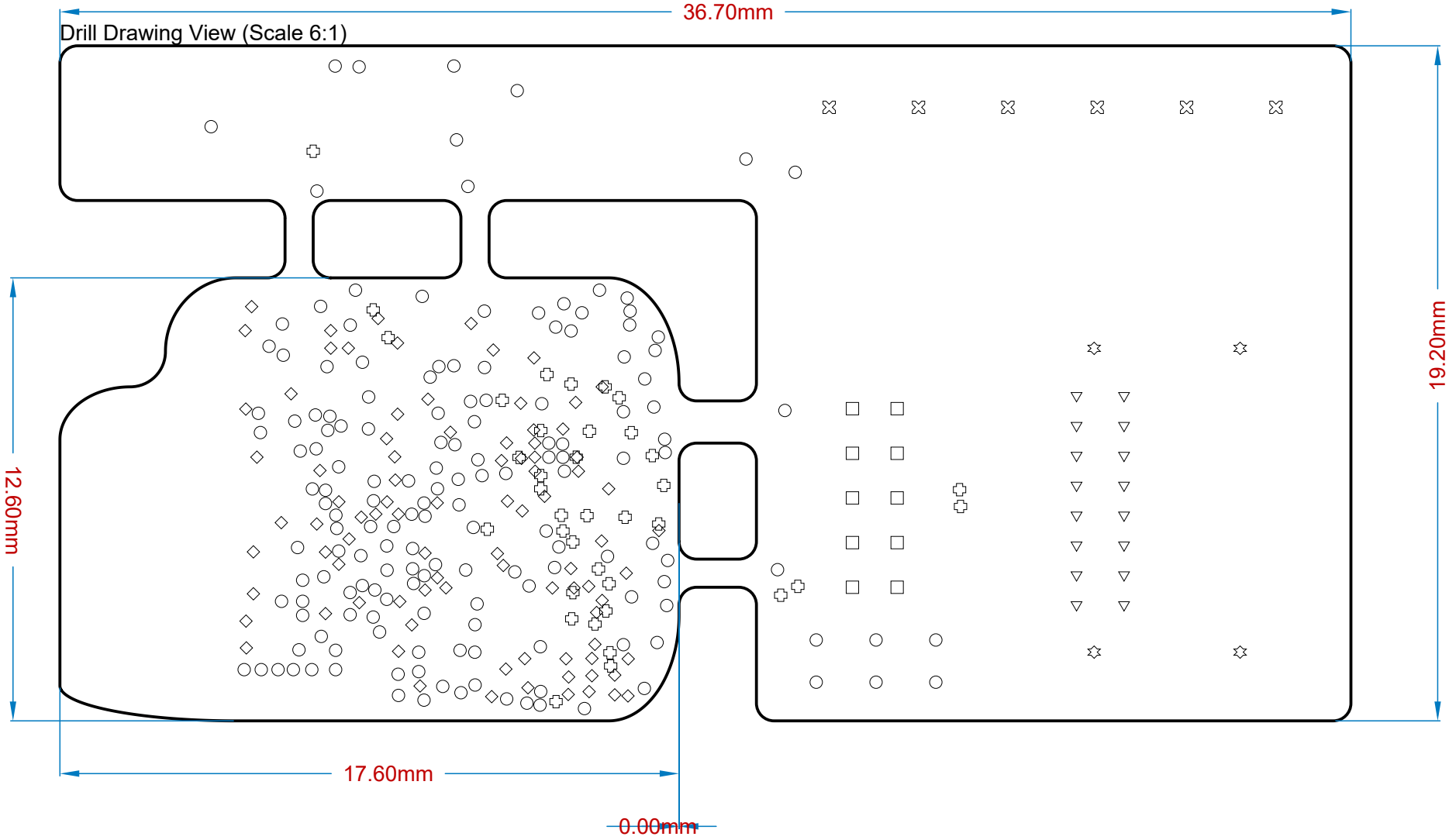


View from Top side (Scale 3:1)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Connectors
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:21 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: Complete	Checked By: Federico Villani, Lukas Schulthess
File: DOC_CONN.PCBDwf	Sheet: 2/2

Drill Drawing View (Scale 6:1)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair
○	160	0.15mm	Plated	Top Layer - Bottom Layer
◇	88	0.15mm	Plated	[UVIA] Top Layer - Int1 (Sign)
⌖	37	0.15mm	Plated	[UVIA] Int4 (Sign) - Bottom Layer
▽	16	0.40mm	Plated	Top Layer - Bottom Layer
□	10	0.65mm	Plated	Top Layer - Bottom Layer
✡	4	0.70mm	Plated	Top Layer - Bottom Layer
☒	6	1.00mm	Plated	Top Layer - Bottom Layer
	321 Total			

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Laboratory: ETHZ D-ITET PBL
Date: 3/4/2024 2:21 PM
Revision: 1.3 License: GNU GPL v3
Variant: Complete

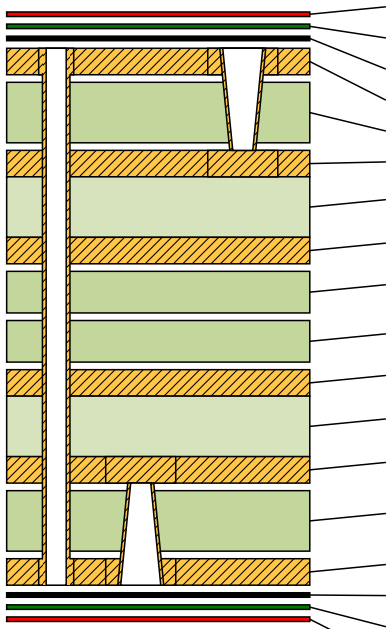
Project: VitalCore: NRF5340

Manufacturing

Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Checked By: Federico Villani, Lukas Schulthess

File: DOC_MANUFACTURE.PCBDwf

Layer Stack Legend



Layer	Type	Gerber
Top Overlay	Legend	GTO
Top Solder	Solder Mask	GTS
Top Surface Finish	Surface Finish	
Top Layer	**Signal**	**GTL**
	Dielectric	
Int1 (Sign)	**Signal**	**G1**
	Dielectric	
Int2 (GND)	**Signal**	**G2**
	Dielectric	
	Dielectric	
Int3 (PWR)	**Signal**	**G3**
	Dielectric	
Int4 (Sign)	**Signal**	**G4**
	Dielectric	
Bottom Layer	**Signal**	**GBL**
Bottom Surface Finish	Surface Finish	
Board Layer Stack Bottom Solder	Solder Mask	GBS
Board Layer Stack Bottom Overlay	Legend	GBO

NOTES:

- HDI/Buried Via.
- Via in pad.
- 0.8mm Board: Use PCBWAY standard stackup (see left).
- ENIG finish.
- Red solder mask.

Use standard PCBWAY 6layer/0.8mm stackup:

Thickness	Copper thick (outer/inner)	Layer No.	StackUp	Laminated chart Thickness
0.8mm±0.1mm	1/1oz	L1		Copper 18 um--plating to 35um
				PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L2		
		L3		Core 0.2mm with 1/1 oz Cu
				PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L4		
		L5		Core 0.2mm with 1/1 oz Cu
				PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L6		Copper 18 um--plating to 35um

ETH
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Swiss Federal Institute of Technology Zurich

Project: VitalCore: NRF5340

Manufacturing

Laboratory: ETHZ D-ITET PBL
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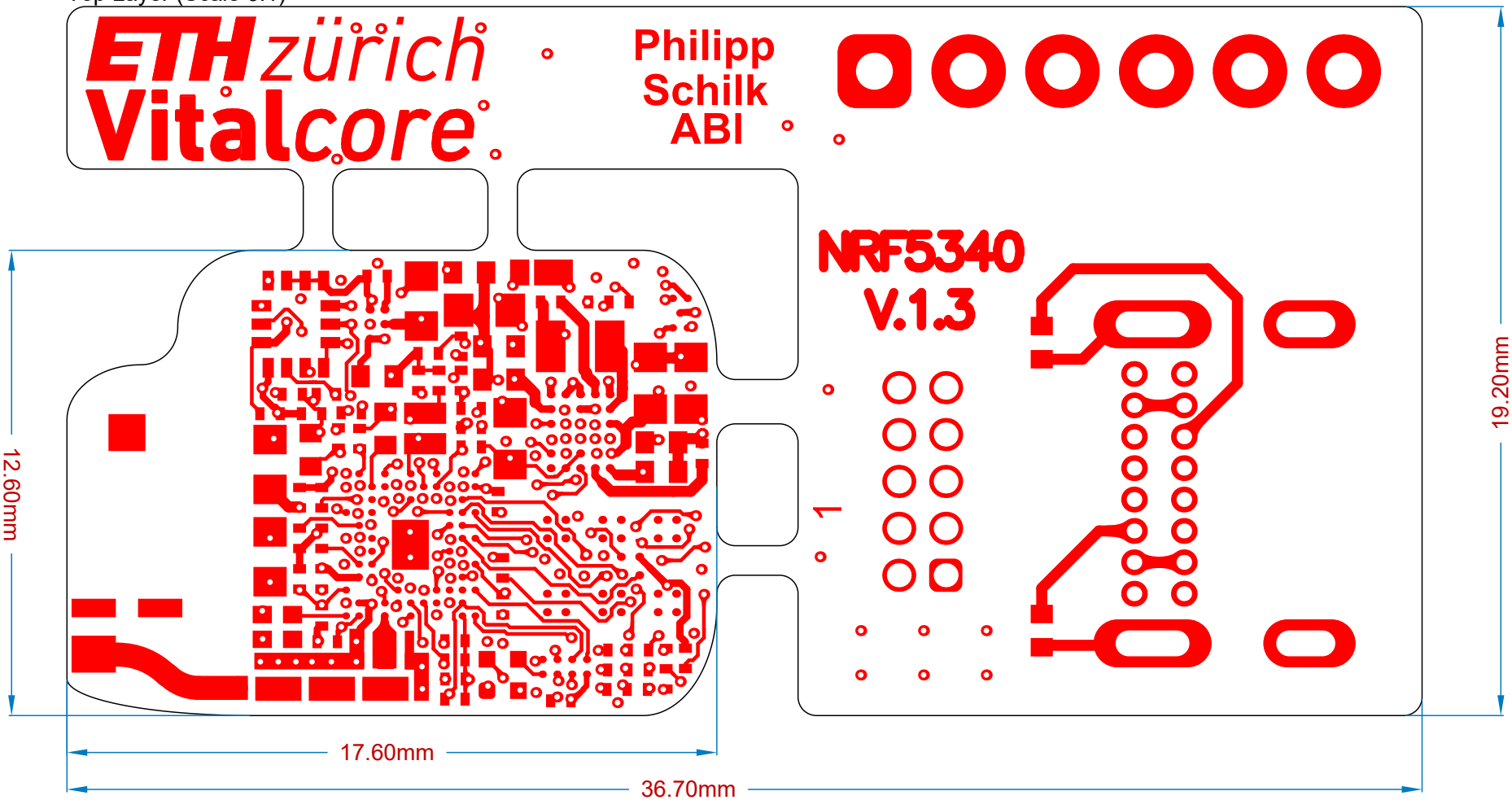
Revision: 1.3 License: GNU GPL v3
Variant: Complete

Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Checked By: Federico Villani, Lukas Schulthess

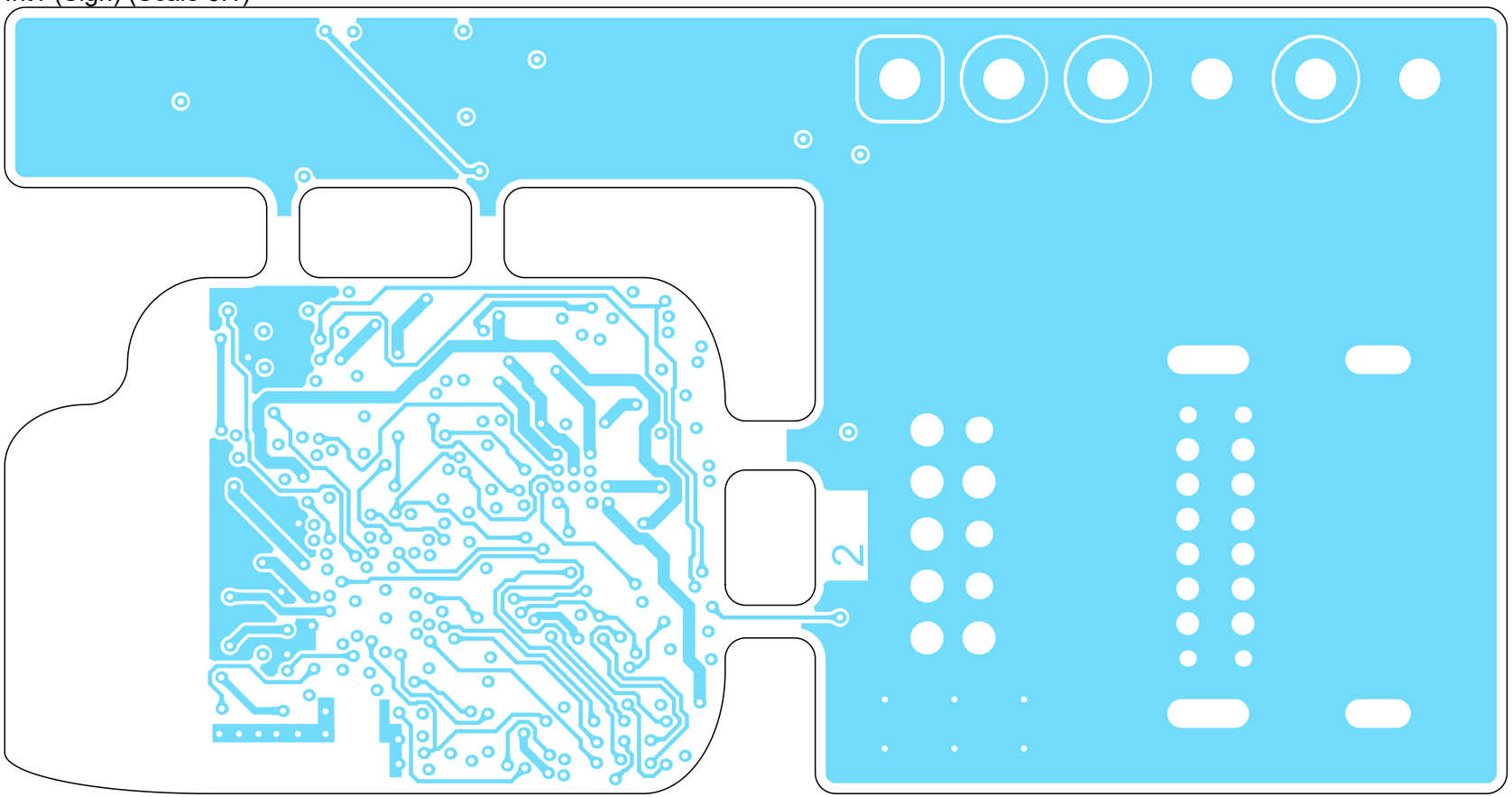
File: DOC_MANUFACTURE.PCBDwf

Top Layer (Scale 6:1)



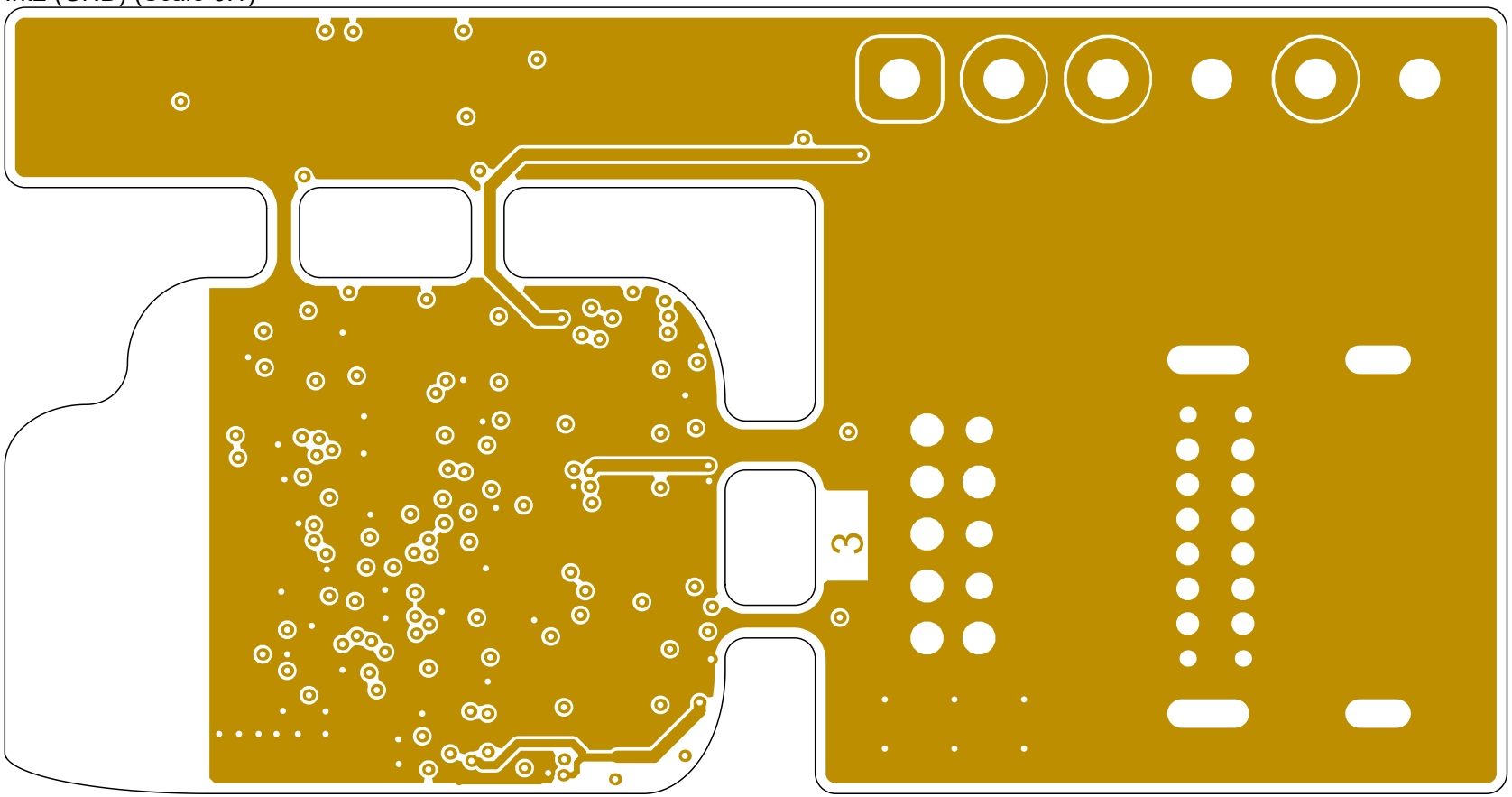
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Art
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:21 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: Complete	Checked By: Federico Villani, Lukas Schulthess
File: DOC_ART.PCBDwf	Sheet: 1/6

Int1 (Sign) (Scale 6:1)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Art
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:21 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: Complete	Checked By: Federico Villani, Lukas Schulthess
File: DOC_ART.PCBDwf	Sheet: 2/6

Int2 (GND) (Scale 6:1)



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	Art
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:21 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: Complete	Checked By: Federico Villani, Lukas Schulthess
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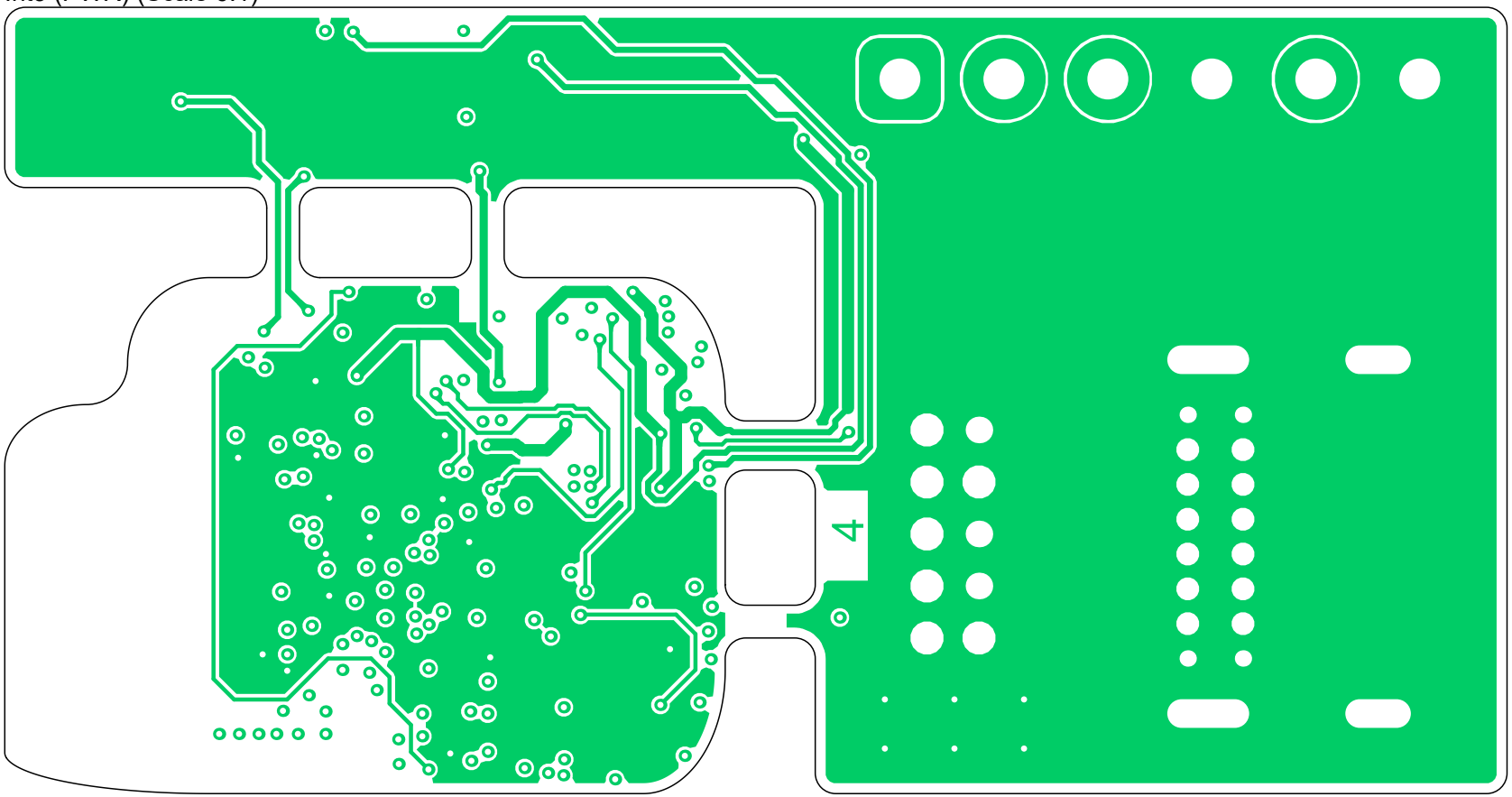
Int3 (PWR) (Scale 6:1)



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	Art
Laboratory: ETHZ D-ITET PBL	
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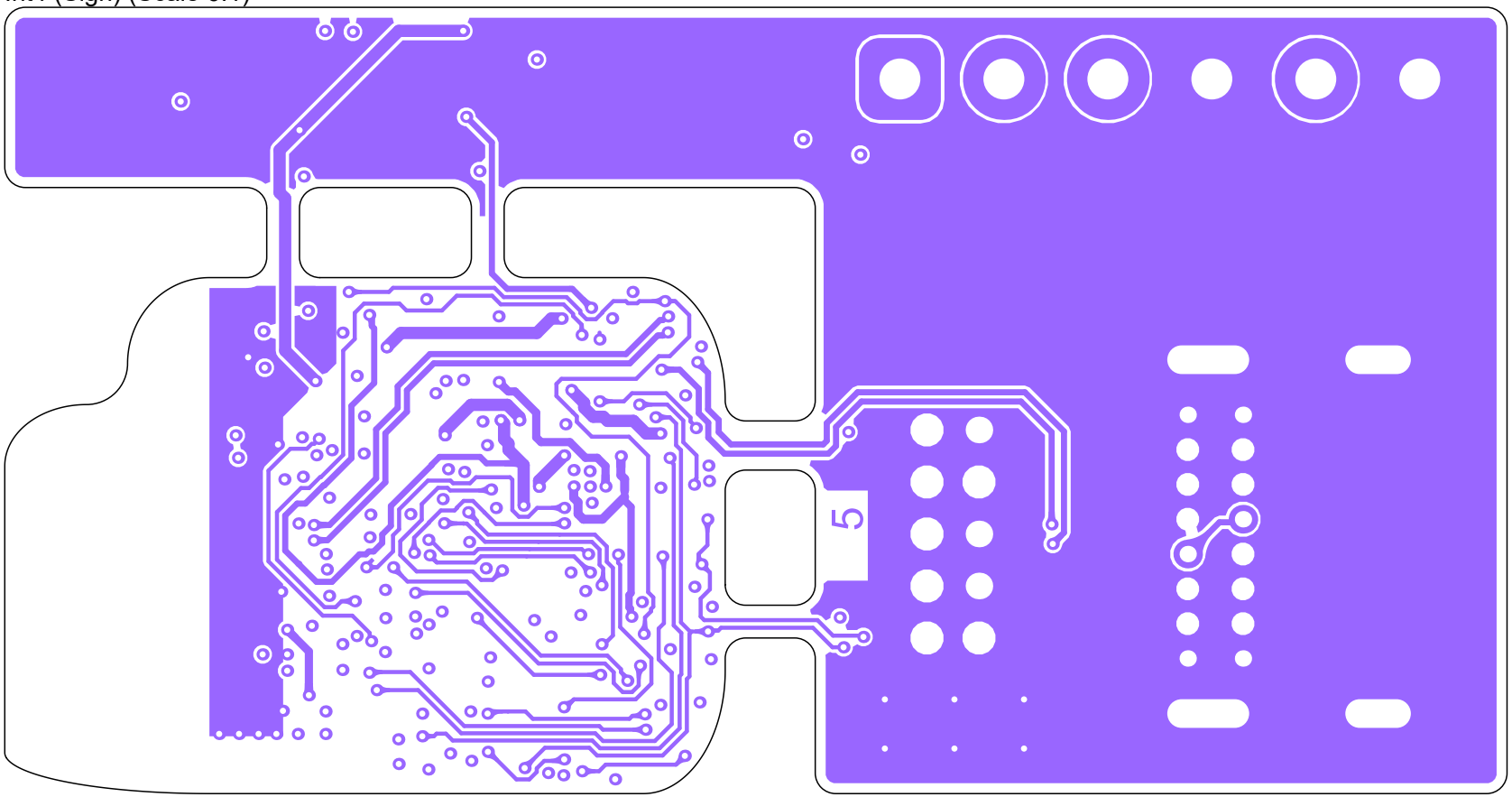
Int4 (Sign) (Scale 6:1)



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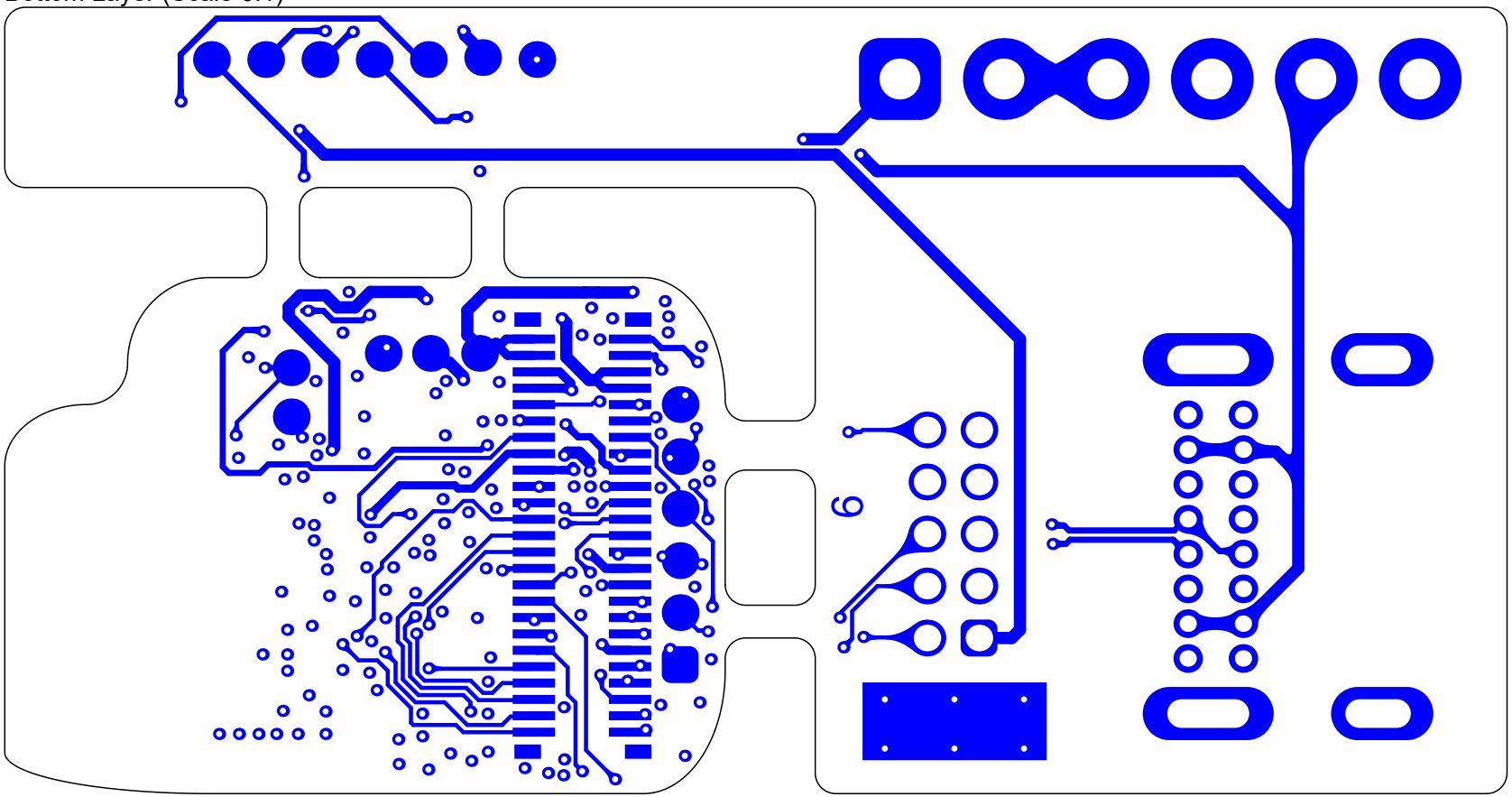
Bottom Layer (Scale 6:1)



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Laboratory: ETHZ D-ITET PBL Date: 3/4/2024 2:21 PM Revision: 1.3 License: GNU GPL v3 Variant: Complete	Drawn By: Philipp Schilk, Alfonso Blanco Fontao Checked By: Federico Villani, Lukas Schulthess
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Bill Of Materials

Line #	Designator	Comment	Quantity	Design Item Id	Manufacturer	Manufacturer Part Number
1	C1, C2, C2D, C3, C4, C5, C6, C14, C14D, C15D, C16D	100 nF	11	CAP_0201_100n_10V	Murata	GRM033Z71A104KE14D
2	C1D	22µF	1	CAP_0402_22u_6V3	Kyocera AVX	CM05X5R226M06AH080
3	C3D, C4D, C12, C12D, C13, C13D	4.7µF	6	CAP_0402_4.7u_16V	Kyocera AVX	0402YD475MAT2A
4	C5D, C7, C8, C10, C11, C15	1µF	6	CAP_0201_1u_10V	Murata	GRM033C81A105ME05D
5	C6D	10µF	1	CAP_0402_10u_10V	Samsung	CL05A106MP5NUNC
6	C7D	3.3nF	1	CAP_0201_3.3n_16V	Murata	GRM033R71C332KA88D
7	C8D, C9D, C10D, C11D	22µF	4	CAP_0603_22u_10V	Murata	GRM187R61A226ME15D
8	C9	2.2nF	1	CAP_0201_2.2n_16V	Murata	GRM033R71C222KA88D
9	C16	0.7pF	1	CAP_RF_0201_0.7pF	Murata	GJM0335C1ER70BB01D
10	C17D, C18D	110pF	2	CAP_0201_110p_50V	Murata	GRM0335C1H111JA01D
11	D1D	NSR20F30NXT5G	1	D_NSR20F30NXT5G	ON Semiconductor	NSR20F30NXT5G
12	D2D	SML-LX0404SIUPGUSB	1	D_RGB_LED	Lumex	SML-LX0404SIUPGUSB
13	E1	NN03-320	1	NN03-320	Fractus Antennas	NN03-320
14	J1, J2, J3, J4, J5	Solder Jumper	5	JMP_0201_3WAY	Panasonic	ERJ-1GN0R00C
15	J2D	Interface	1	CONN_50P_M_COMBI_INTERFACE		
16	J4D	ARM SWD 10-pin	1	CONN_SWD		
17	J5D	6Pin	1	CONN_PINHEADER_6PIN		
18	J7D	213716-0001 USB-C	1	CONN_USB_C	Molex	213716-0001
19	JP1D	0R	1	JMP_0201	Panasonic	ERJ-1GN0R00C
20	L1, L2	10µH	2	L_0603_10uH_300mA	Murata	LQM18DN100M70L
21	L1D	2.2µH	1	L_0603_2.2uH_520mA	Taiyo Yuden	MBKK1608T2R2M
22	L2D	1.5µH	1	L_0805_1.5uH_2A	Murata	DFE201210S-1R5M=P2
23	L3, L6, L7	5.6nH	3	L_RF_0201_5.6nH	Murata	LQW03AW5N6J00D
24	L4, L5	2.2nH	2	L_RF_0201_2.2nH	Murata	LQP03HQ2N2B02D
25	R1, R2	2.2kR	2	R_0201_2.2K	Panasonic	ERJ-1GNF2201C
26	R2D, R3D	100kR	2	R_0201_100K	Panasonic	ERJ-1GNF1003C
27	R3	2.2R	1	R_0201_2.2R	Yageo	RC0201FR-072R2L
28	R4, R6D	10kR	2	R_0201_10K	Panasonic	ERJ-1GNF1002C
29	R4D, R5D	5K1	2	R_0402_5K1	Panasonic	ERJ-2RKF5101X
30	RT1D	10kR	1	NTC_0201_10k	Panasonic	ERTJZEG103FA
31	U1	nRF5340-CLAA	1	nRF5340-CLAA	Nordic	NRF5340-CLAA-R7
32	U1D	MAX38640BENT18+T	1	MAX38640BENT18+T	Maxim	MAX38640BENT18+T
33	U2D	MAX77654BENV+T	1	MAX77654BENV+T	Maxim	MAX77654BENV+T
34	U4D	PESD1USB30	1	PESD1USB30	NXP Semiconductors	PESD1USB30
35	U5D	W25Q256JWYIM	1	W25Q256JWYIM	Winbond	W25Q256JWYIM TR
36	U6D	LSM6DSV16BX	1	LSM6DSV16BX	STMicroelectronics	LSM6DSV16BX
37	U7D	IS31FL3194	1	IS31FL3194	ISSI	IS31FL3194-CLS2-TR
38	Y1	ECS-.327-9-1210 (32.768kHz)	1	Y_ECS-327-9-1210	ECS International	ECS-.327-9-1210-TR
39	Y2	ECS-320-7-48B-JTM-TR5 (32MHz)	1	Y_ECS-320-7-48B-JTM-TR5	ECS International	ECS-320-7-48B-JTM-TR5

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

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