ETHZurich

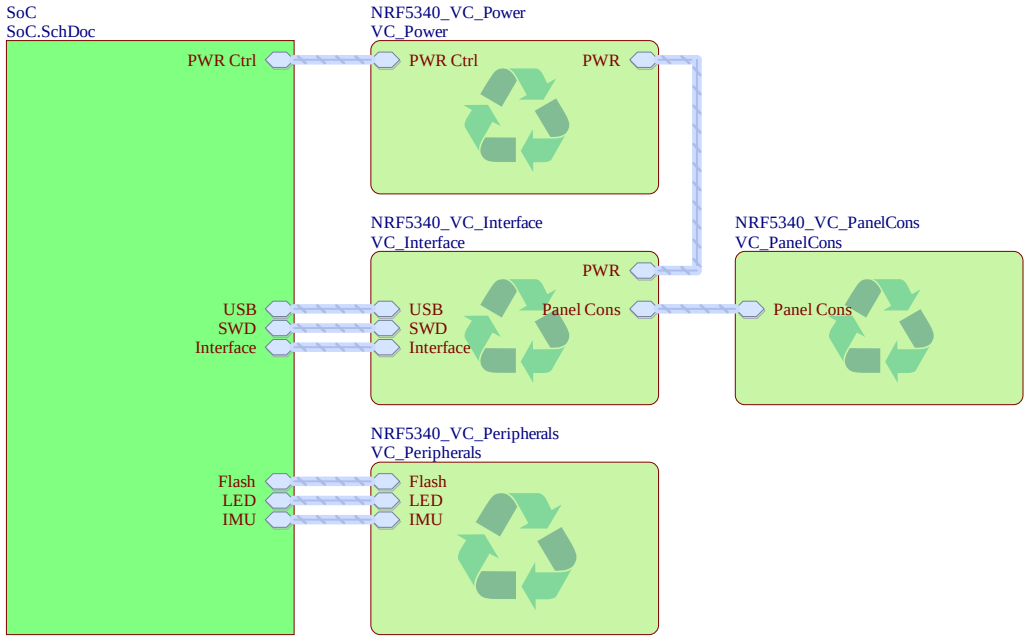
Logo ETH Zurich

VitalCore

Logo VitalCore

Vitalcore ETH

Logo Vitalcore ETH



Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

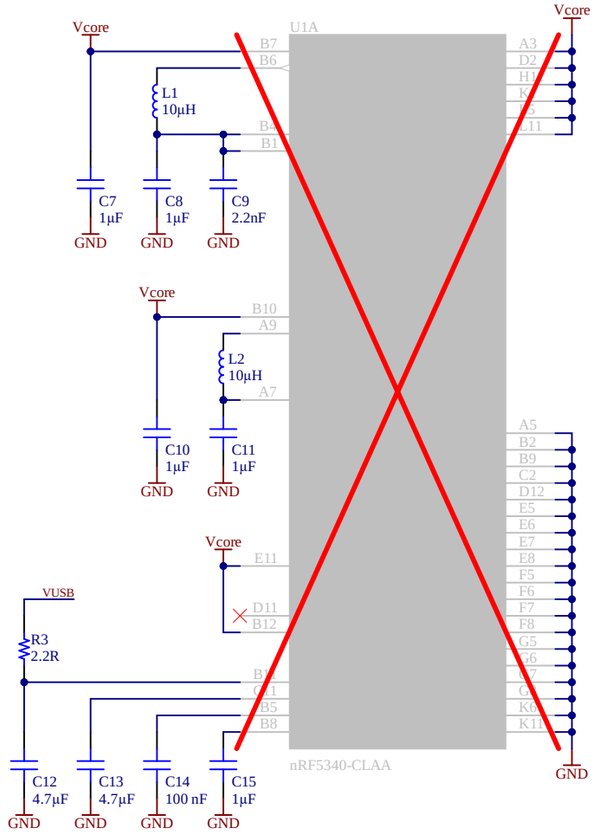
Laboratory: D-ITET PBL
Date: 3/4/2024 2:24:04 PM
Rev: 1.3 License: GNU GPL v3
Variant: PassivesOnlyAssembly

Project: VitalCore: NRF5340

Overview

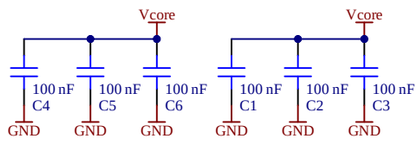
Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Checked By: Federico Villani, Lukas Schulthess

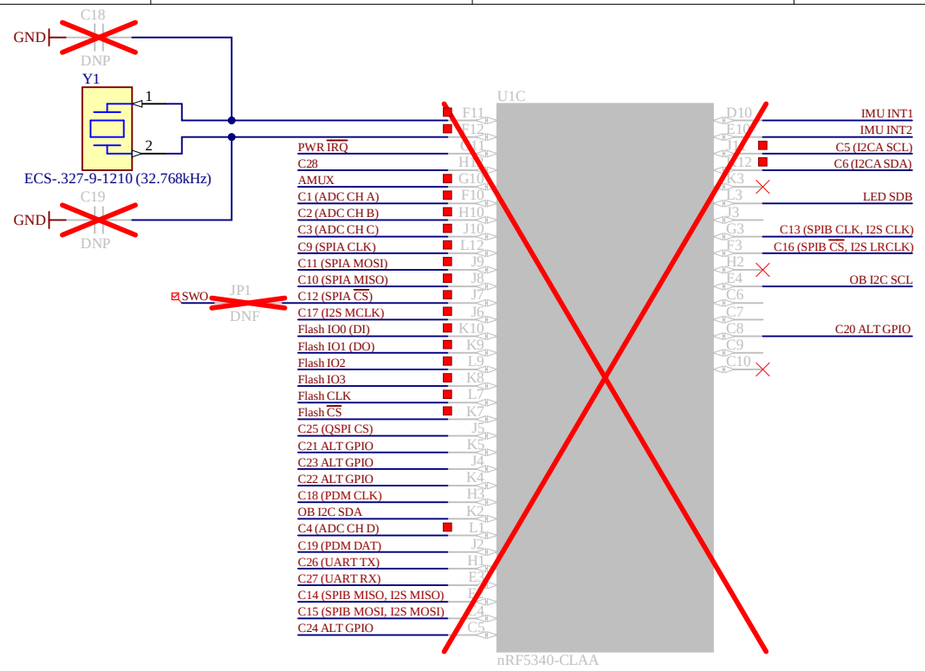
File: VC_NRF5340.SchDoc Sheet: 1 / 6



Based on CLAA sample configuration 2 (DS v1.3 pg. 812)

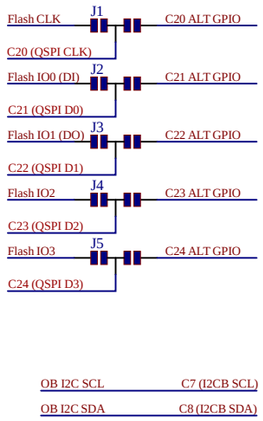
DCCH left NC if VREGH is not used (DS v1.3 pg 52)

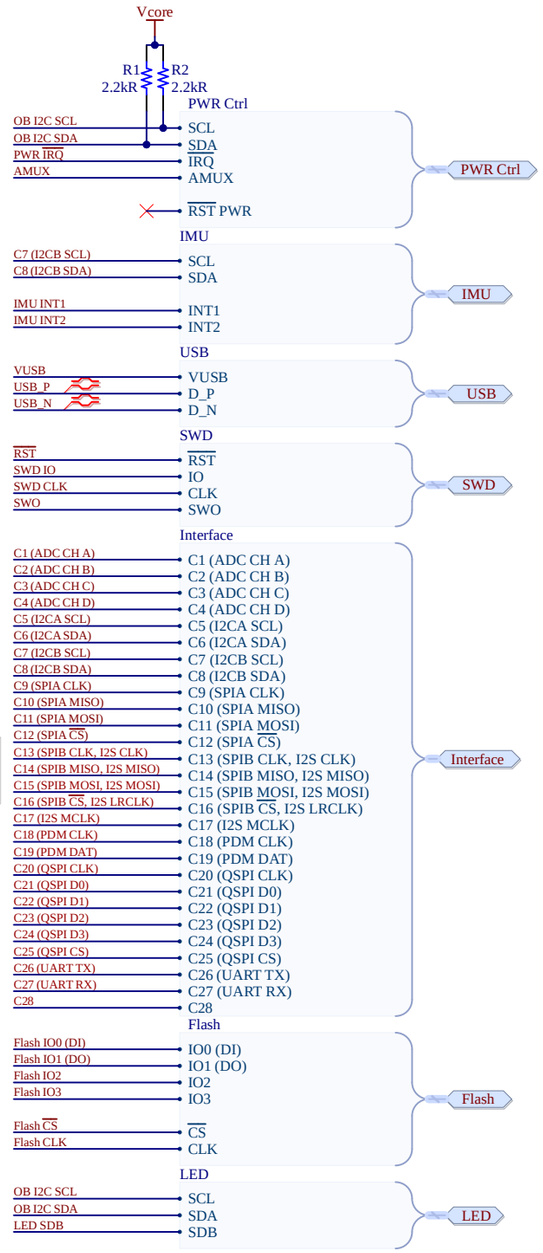




Red box indicates that signal cannot be freely re-assigned to another pin.

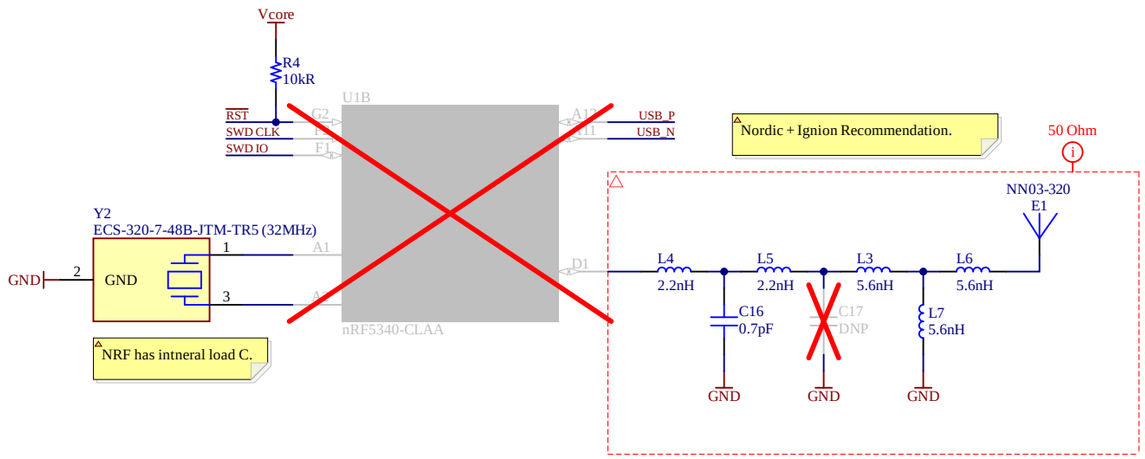
Jumper on SWO line enables SWO to be disconnected if SPI is used in high-speed mode, to reduce trace capacitance.





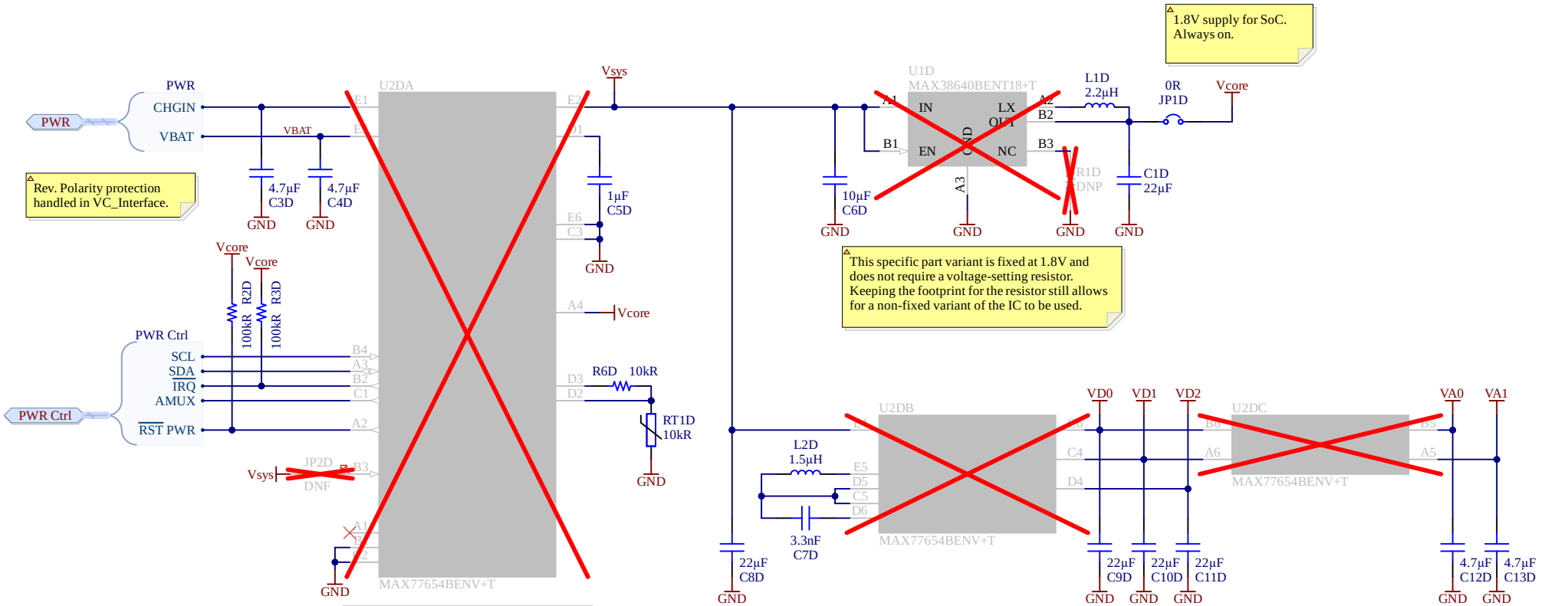
QSPI signals should be length matched!

Flash signals should be length matched!



NRF has intneral load C.

ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	NRF5340 SoC, BLE Antenna
Laboratory: D-ITET PBL	
Date: 3/4/2024 2:24:04 PM	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Rev: 1.3 License: GNU GPL v3	Checked By: Federico Villani, Lukas Schulthess
Variation: PassivesOnlyAssembly	
File: SoC.SchDoc	Sheet: 2 / 6



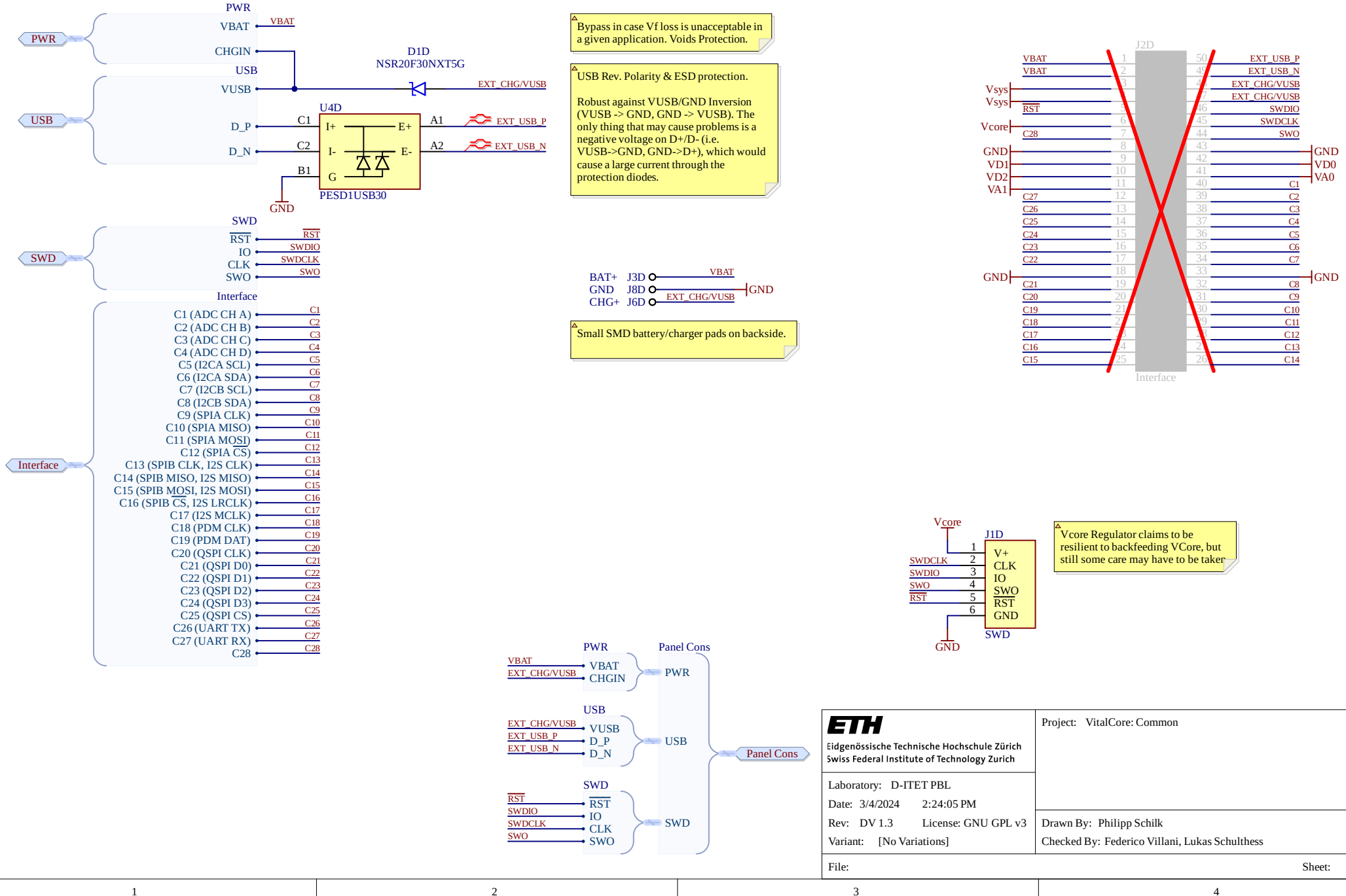
ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: VitalCore: Common

Laboratory: D-ITET PBL
Date: 3/4/2024 2:24:04 PM
Rev: DV 1.3 License: GNU GPL v3
Variant: [No Variations]

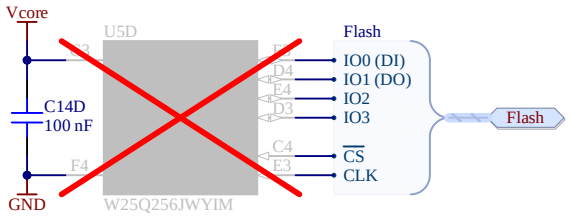
Drawn By: Philipp Schilk
Checked By: Federico Villani, Lukas Schulthess

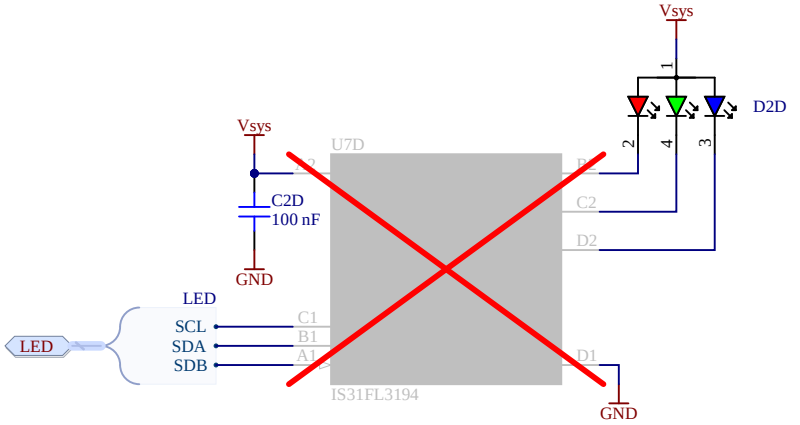
File: Sheet: /

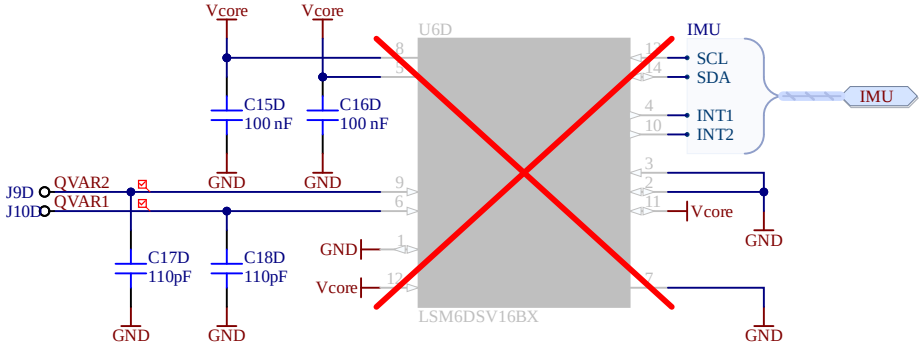


ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich

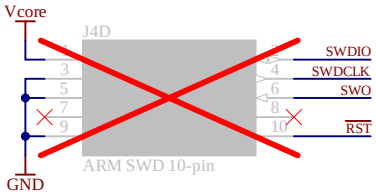
Project: VitalCore: Common	
Laboratory: D-ITET PBL	Drawn By: Philipp Schilk
Date: 3/4/2024 2:24:05 PM	Checked By: Federico Villani, Lukas Schulthess
Rev: DV 1.3 License: GNU GPL v3	
Variant: [No Variations]	
File:	Sheet: /

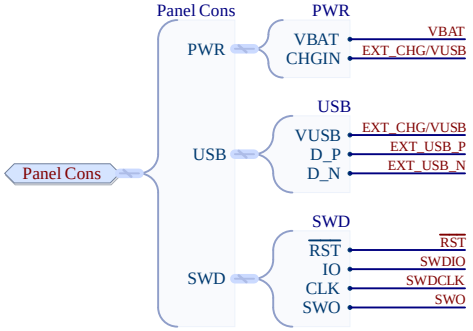


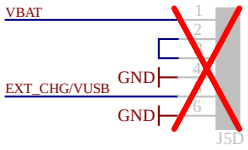


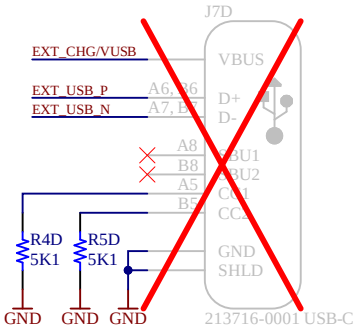


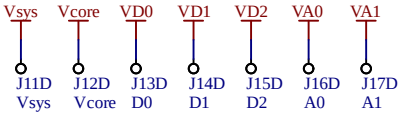
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: Common
Laboratory: D-ITET PBL Date: 3/4/2024 2:24:05 PM Rev: DV 1.3 License: GNU GPL v3 Variant: [No Variations]	Drawn By: Philipp Schilk Checked By: Federico Villani, Lukas Schulthess
File:	Sheet: /





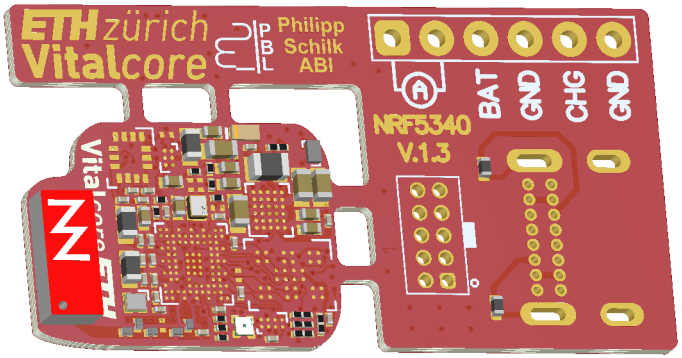




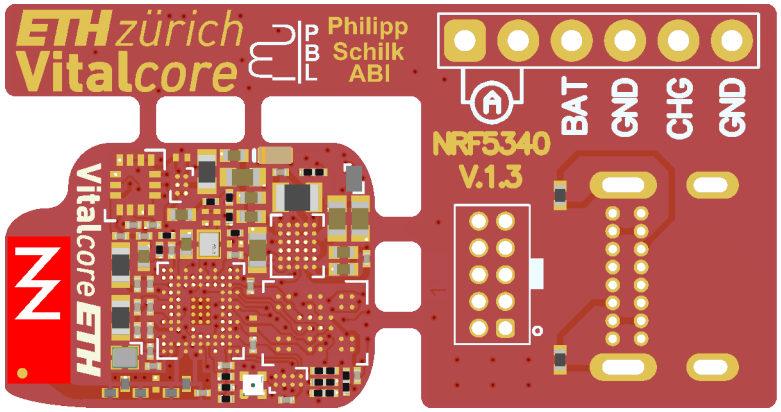


ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: Common
Laboratory: D-ITET PBL Date: 3/4/2024 2:24:05 PM Rev: DV 1.3 License: GNU GPL v3 Variant: [No Variations]	Drawn By: Philipp Schilk Checked By: Federico Villani, Lukas Schulthess
File:	Sheet: /

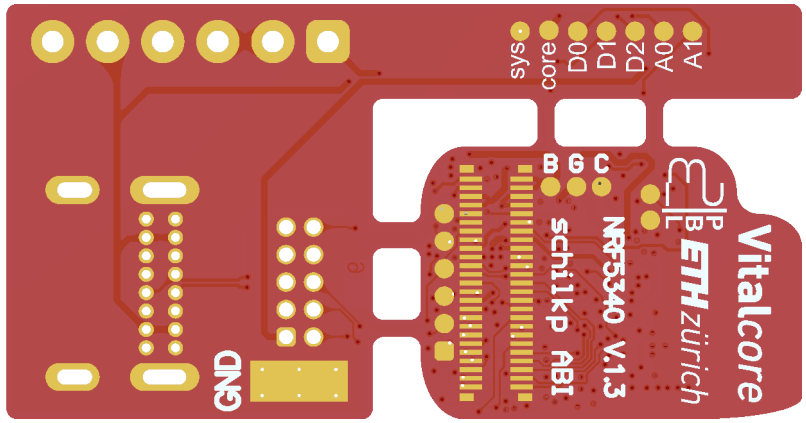
Realistic View



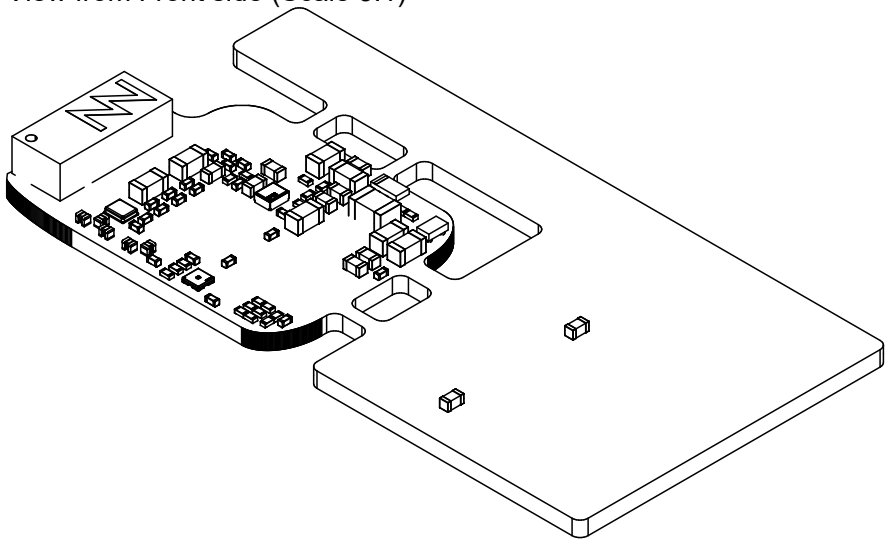
Realistic View



Realistic View

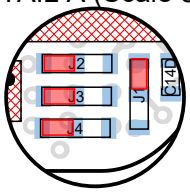


View from Front side (Scale 3:1)



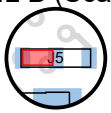
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	3D Render
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:24 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: PassivesOnlyAssembly	Checked By: Federico Villani, Lukas Schulthess
File: DOC_3D.PCBDwf	Sheet: 1/1

DETAIL A (Scale 8:1)



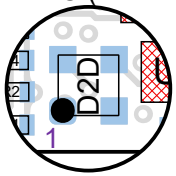
J2, J3, J4: Mount resistor from central pad to left pad
J1: Mount resistor from central pad to upper pad.

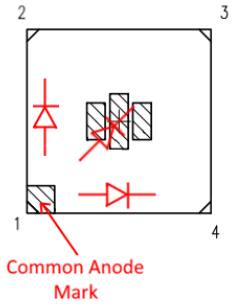
DETAIL B (Scale 8:1)



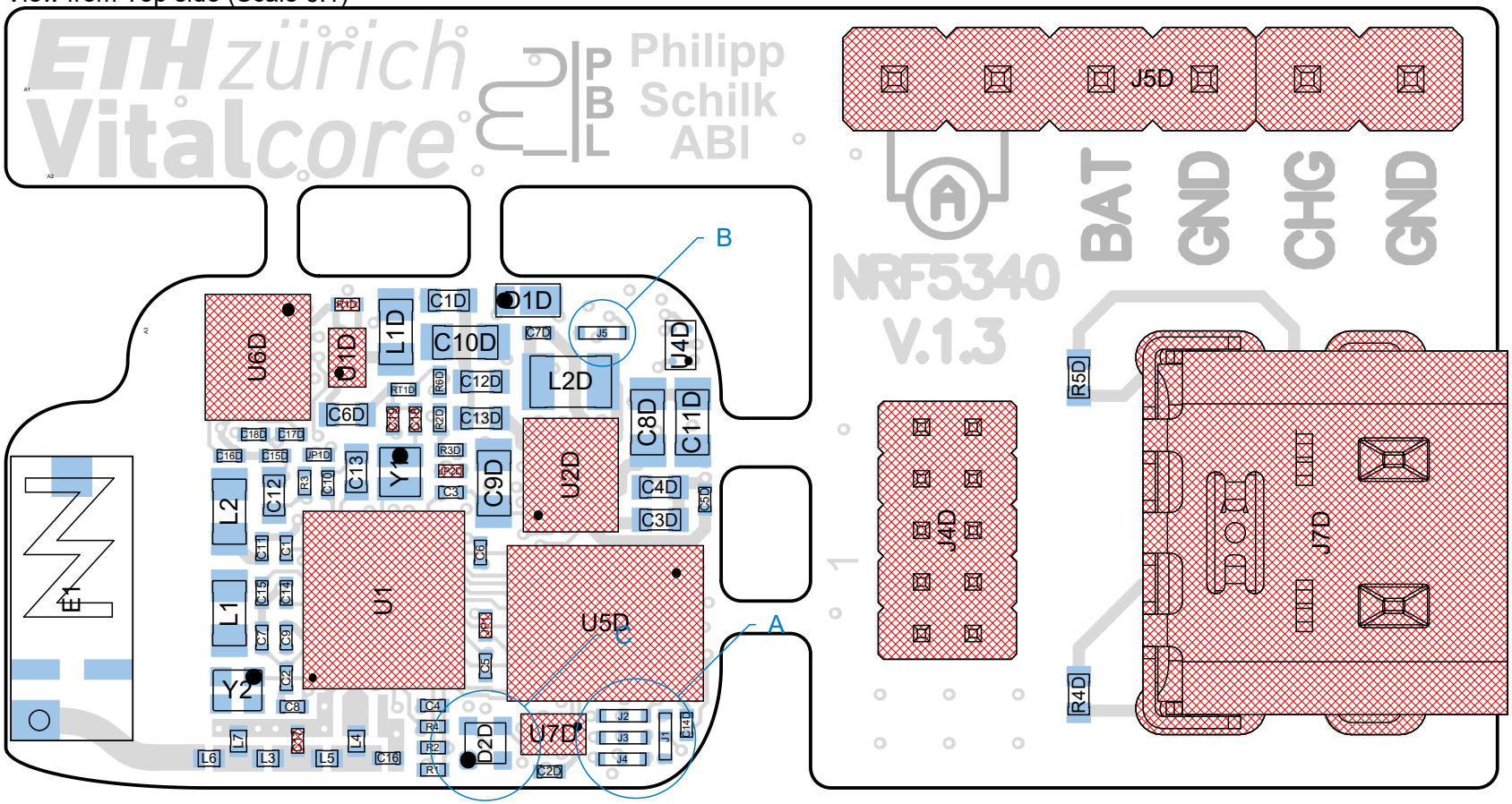
J5: mount resistor from central pad to left pad

DETAIL C (Scale 8:1)

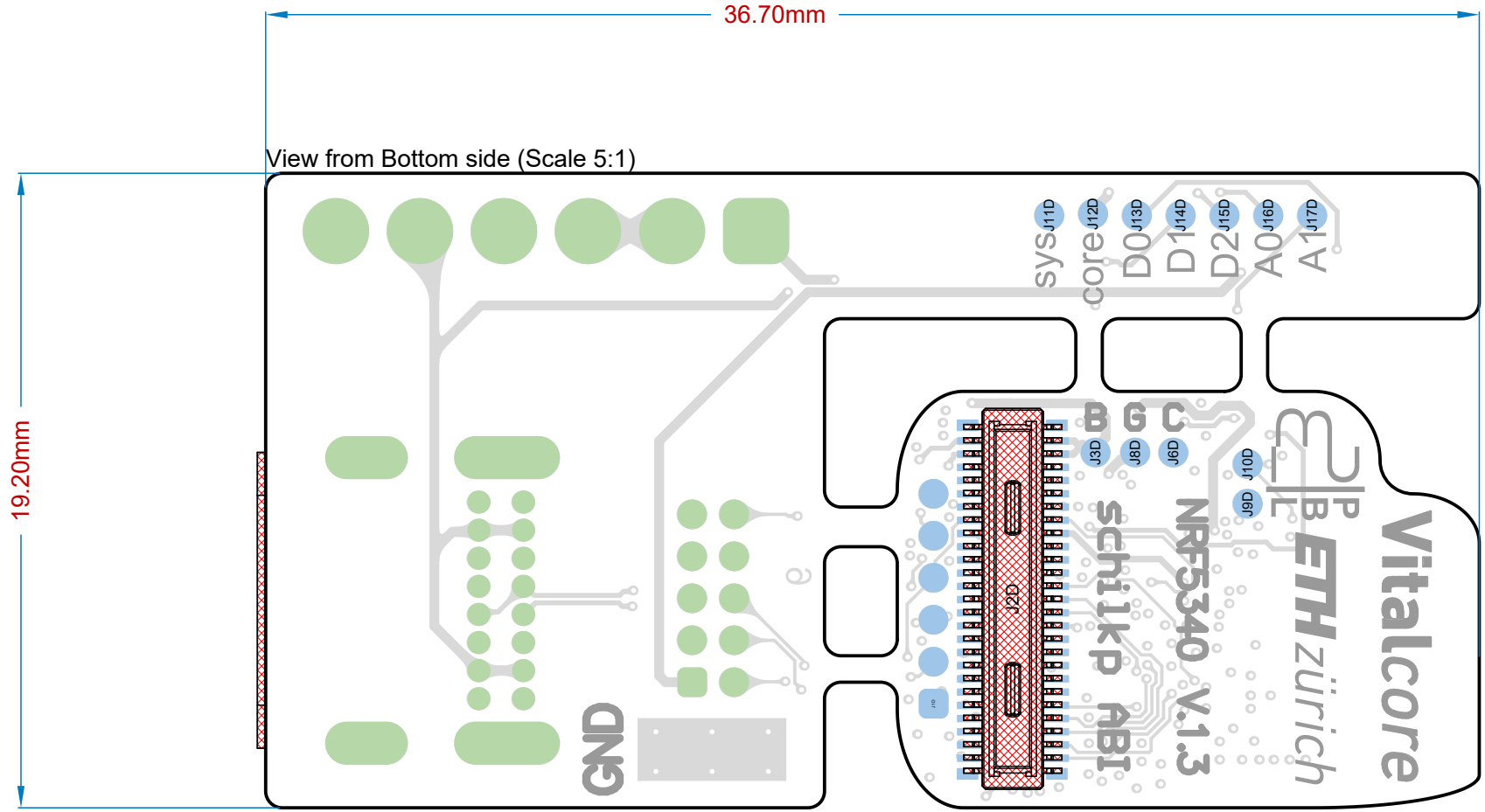




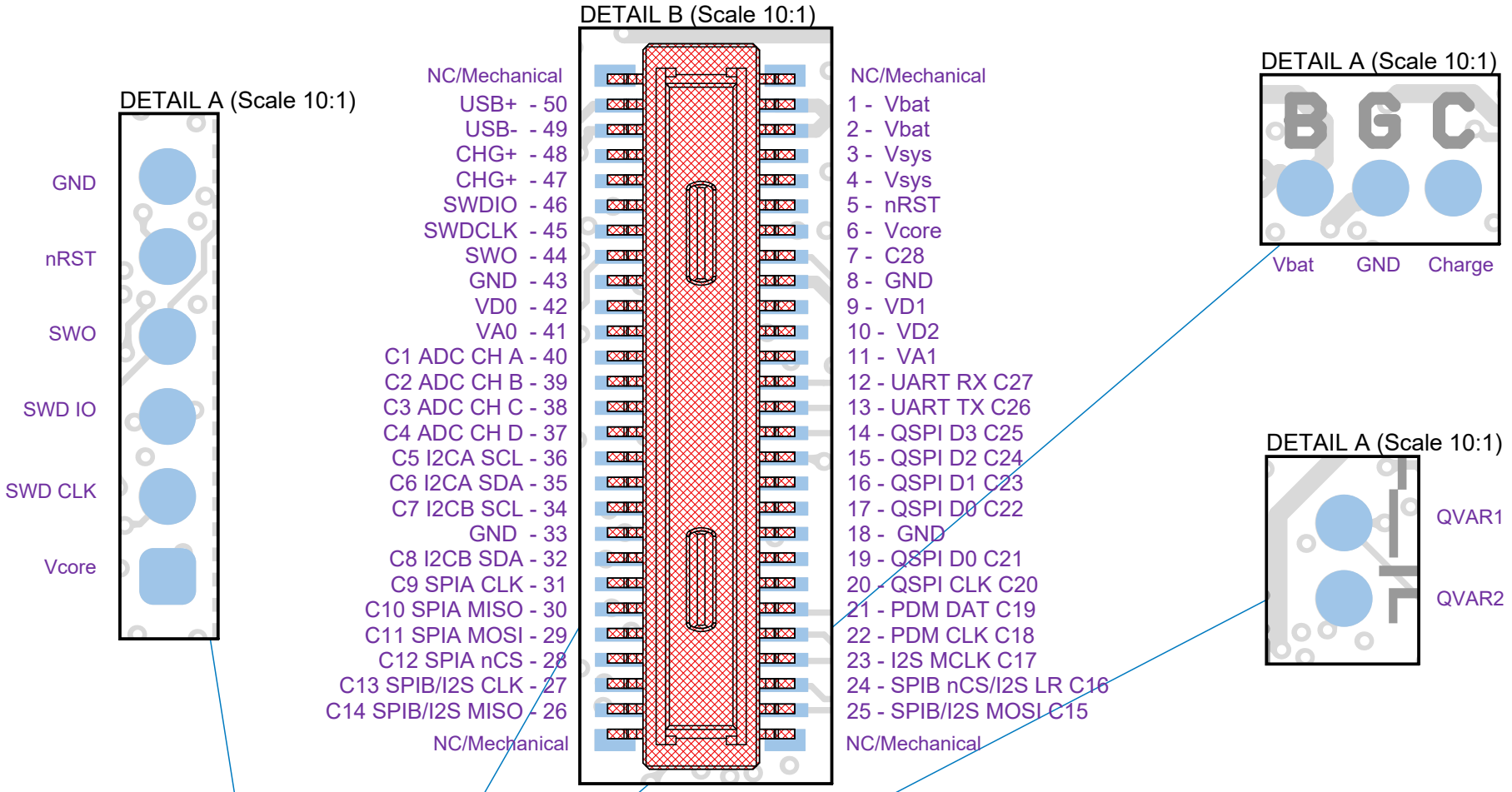
View from Top side (Scale 6:1)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Assembly
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:24 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: PassivesOnlyAssembly	Checked By: Federico Villani, Lukas Schulthess
File: DOC_ASSEMBLY.PCBDwf	Sheet: 1/2



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340 Assembly
Laboratory: ETHZ D-ITET PBL Date: 3/4/2024 2:24 PM Revision: 1.3 License: GNU GPL v3 Variant: PassivesOnlyAssembly	Drawn By: Philipp Schilk, Alfonso Blanco Fontao Checked By: Federico Villani, Lukas Schulthess
File: DOC_ASSEMBLY.PCBDwf	Sheet: 2/2



ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: VitalCore: NRF5340

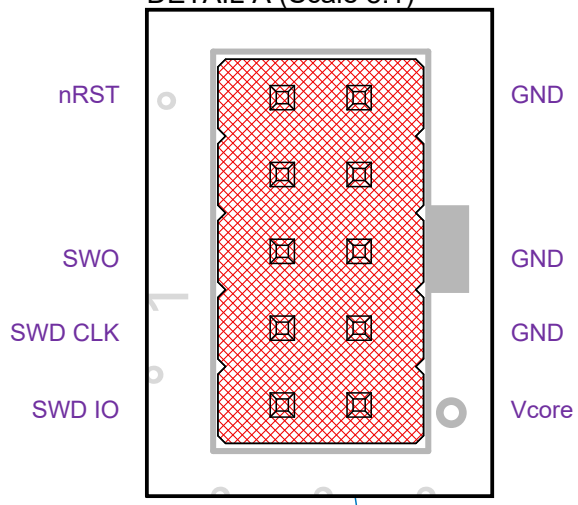
Connectors

Laboratory: ETHZ D-ITET PBL
Date: 3/4/2024 2:24 PM
Revision: 1.3 License: GNU GPL v3
Variant: PassivesOnlyAssembly

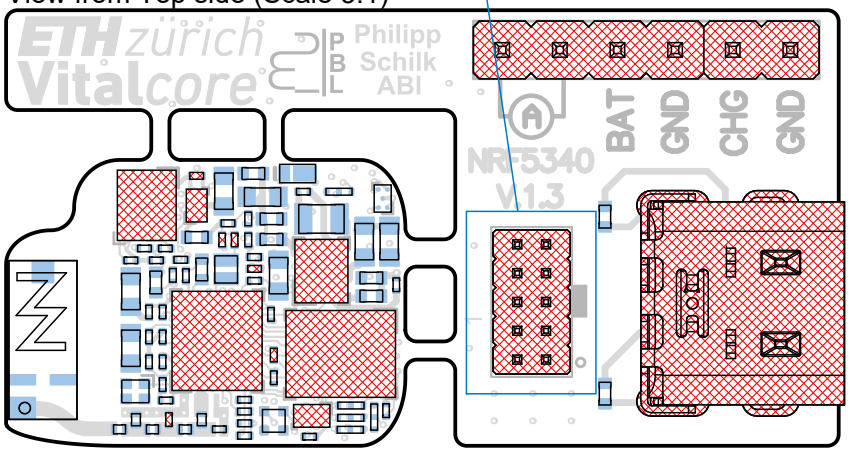
Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Checked By: Federico Villani, Lukas Schulthess

File: DOC_CONN.PCBDwf Sheet: 1/2

DETAIL A (Scale 8:1)

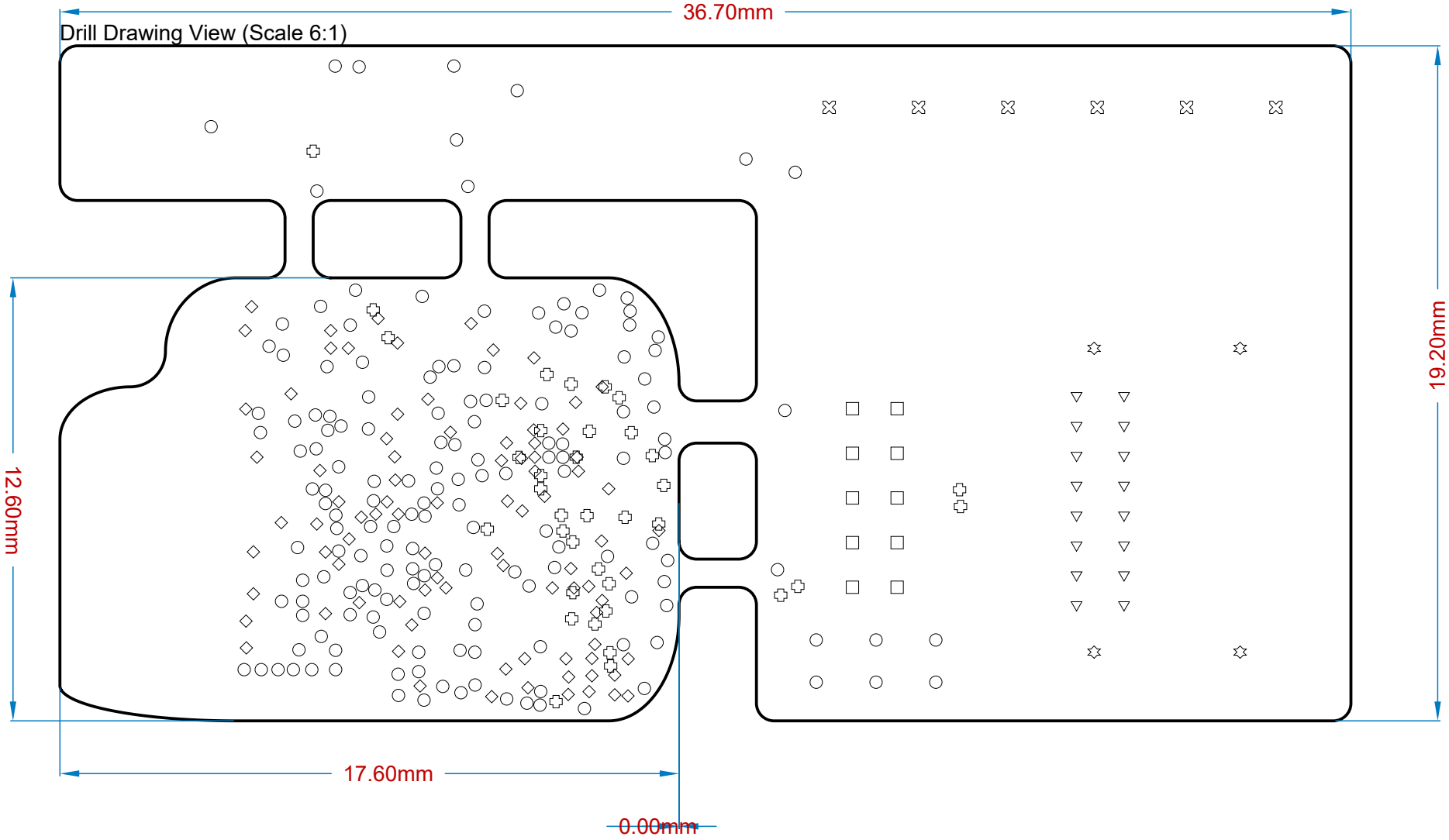


View from Top side (Scale 3:1)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Connectors
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:24 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: PassivesOnlyAssembly	Checked By: Federico Villani, Lukas Schulthess
File: DOC_CONN.PCBDwf	Sheet: 2/2

Drill Drawing View (Scale 6:1)



Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair
○	160	0.15mm	Plated	Top Layer - Bottom Layer
◇	88	0.15mm	Plated	[UVIA] Top Layer - Int1 (Sign)
⌑	37	0.15mm	Plated	[UVIA] Int4 (Sign) - Bottom Layer
▽	16	0.40mm	Plated	Top Layer - Bottom Layer
□	10	0.65mm	Plated	Top Layer - Bottom Layer
✡	4	0.70mm	Plated	Top Layer - Bottom Layer
⊠	6	1.00mm	Plated	Top Layer - Bottom Layer
	321 Total			

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: VitalCore: NRF5340

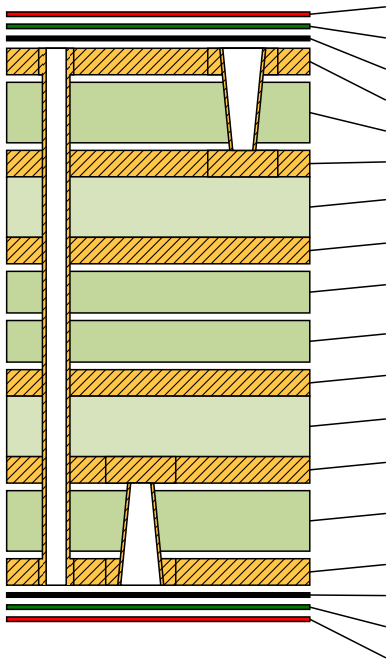
Manufacturing

Laboratory: ETHZ D-ITET PBL
Date: 3/4/2024 2:24 PM
Revision: 1.3 License: GNU GPL v3
Variant: PassivesOnlyAssembly

Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Checked By: Federico Villani, Lukas Schulthess

File: DOC_MANUFACTURE.PCBDwf

Layer Stack Legend



Layer	Type	Gerber
Top Overlay	Legend	GTO
Top Solder	Solder Mask	GTS
Top Surface Finish	Surface Finish	
Top Layer	**Signal**	**GTL**
	Dielectric	
Int1 (Sign)	**Signal**	**G1**
	Dielectric	
Int2 (GND)	**Signal**	**G2**
	Dielectric	
	Dielectric	
Int3 (PWR)	**Signal**	**G3**
	Dielectric	
Int4 (Sign)	**Signal**	**G4**
	Dielectric	
Bottom Layer	**Signal**	**GBL**
Bottom Surface Finish	Surface Finish	
Board Layer Stack Bottom Solder	Solder Mask	GBS
Board Layer Stack Bottom Overlay	Legend	GBO

NOTES:

- HDI/Buried Via.
- Via in pad.
- 0.8mm Board: Use PCBWAY standard stackup (see left).
- ENIG finish.
- Red solder mask.

Use standard PCBWAY 6layer/0.8mm stackup:

Thickness	Copper thick (outer/inner)	Layer No.	StackUp	Laminated chart Thickness
0.8mm±0.1mm	1/1oz	L1		Copper 18 um--plating to 35um
				PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L2		
		L3		Core 0.2mm with 1/1 oz Cu
				PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L4		
		L5		Core 0.2mm with 1/1 oz Cu
				PP 0.11 mm(2116) dielectric constant 4.29 ± (The DK value is not absolute and will vary depending on the base material's models and thickness.)
		L6		Copper 18 um--plating to 35um

ETH
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Manufacturing

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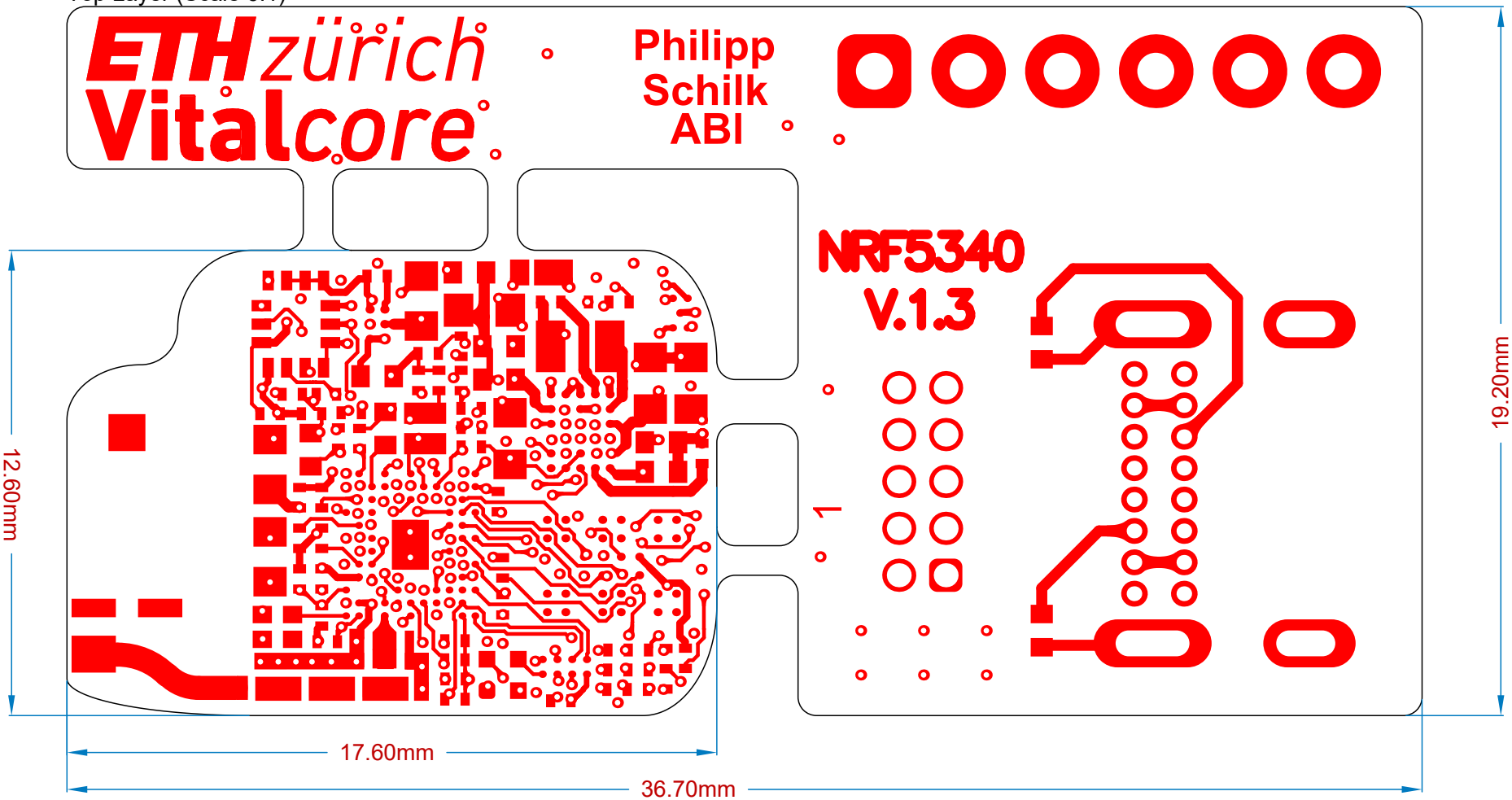
Date: 3/4/2024 2:24 PM
Revision: 1.3 License: GNU GPL v3
Variant: PassivesOnlyAssembly

Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Checked By: Federico Villani, Lukas Schulthess

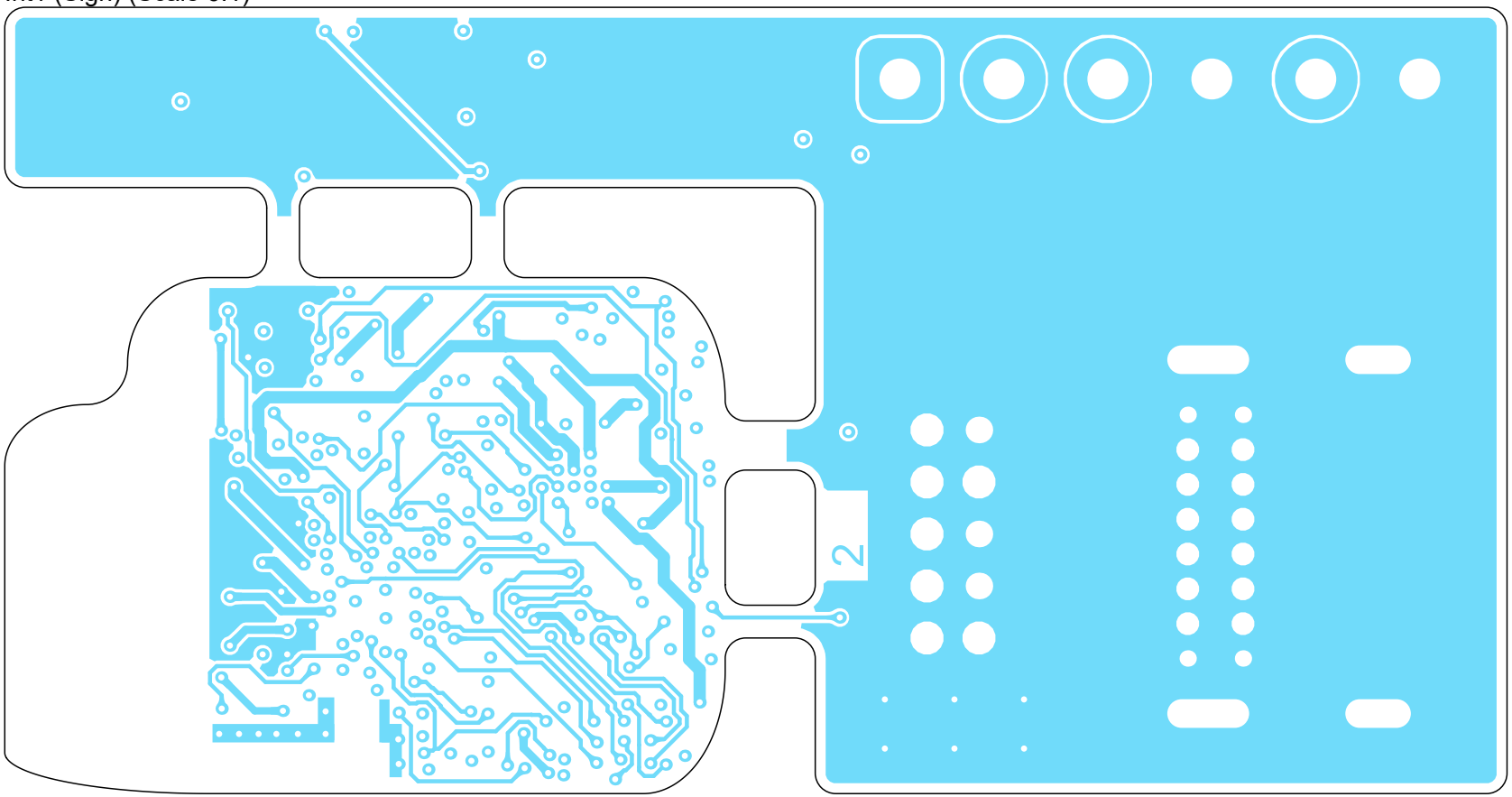
File: DOC_MANUFACTURE.PCBDwf

Top Layer (Scale 6:1)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Art
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:24 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: PassivesOnlyAssembly	Checked By: Federico Villani, Lukas Schulthess
File: DOC_ART.PCBDwf	Sheet: 1/6

Int1 (Sign) (Scale 6:1)



ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Project: VitalCore: NRF5340

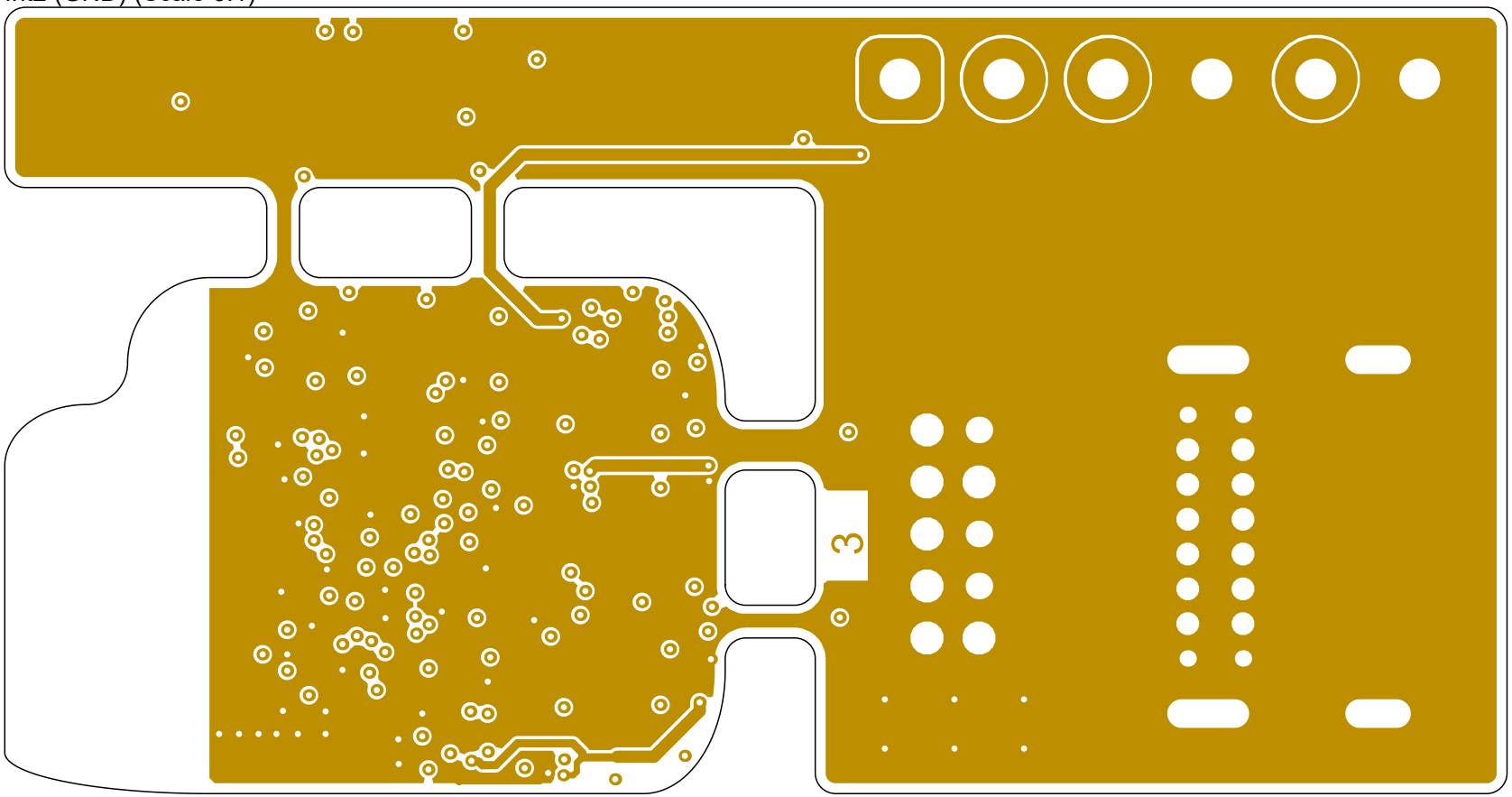
Art

Laboratory: ETHZ D-ITET PBL
Date: 3/4/2024 2:24 PM
Revision: 1.3 License: GNU GPL v3
Variant: PassivesOnlyAssembly

Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Checked By: Federico Villani, Lukas Schulthess

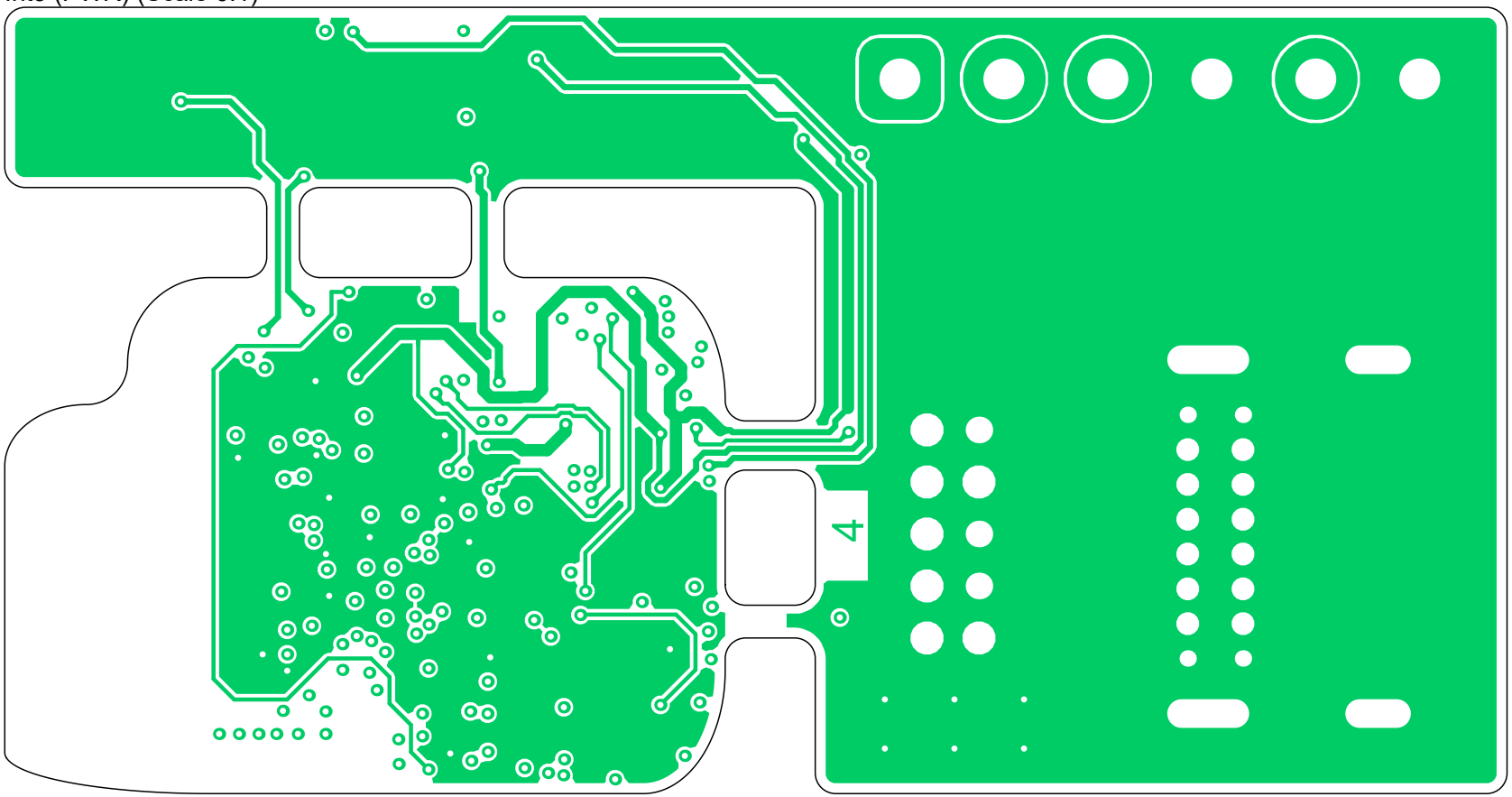
File: DOC_ART.PCBDwf

Int2 (GND) (Scale 6:1)



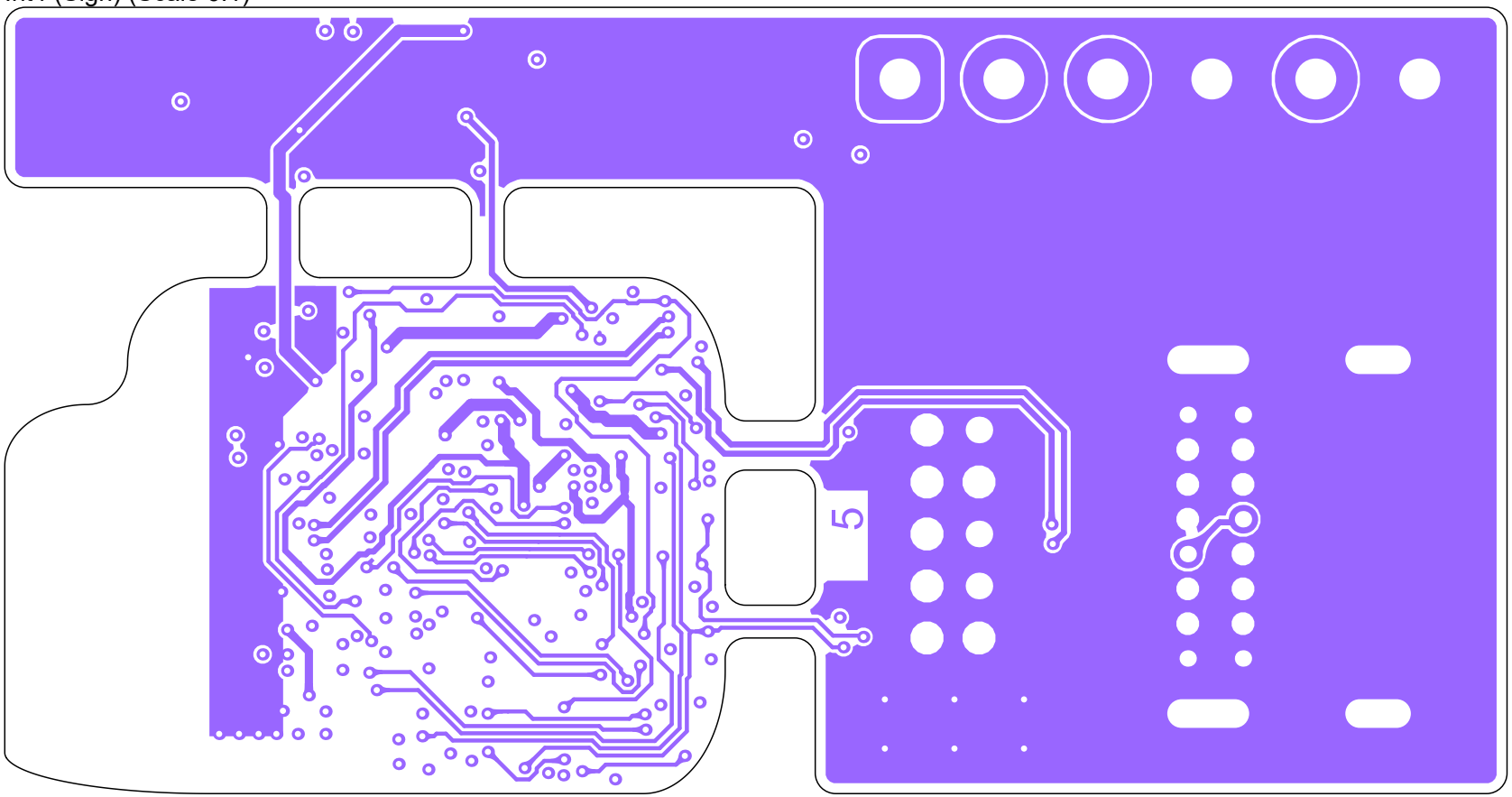
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Art
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:24 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: PassivesOnlyAssembly	Checked By: Federico Villani, Lukas Schulthess
File: DOC_ART.PCBDwf	Sheet: 3/6

Int3 (PWR) (Scale 6:1)



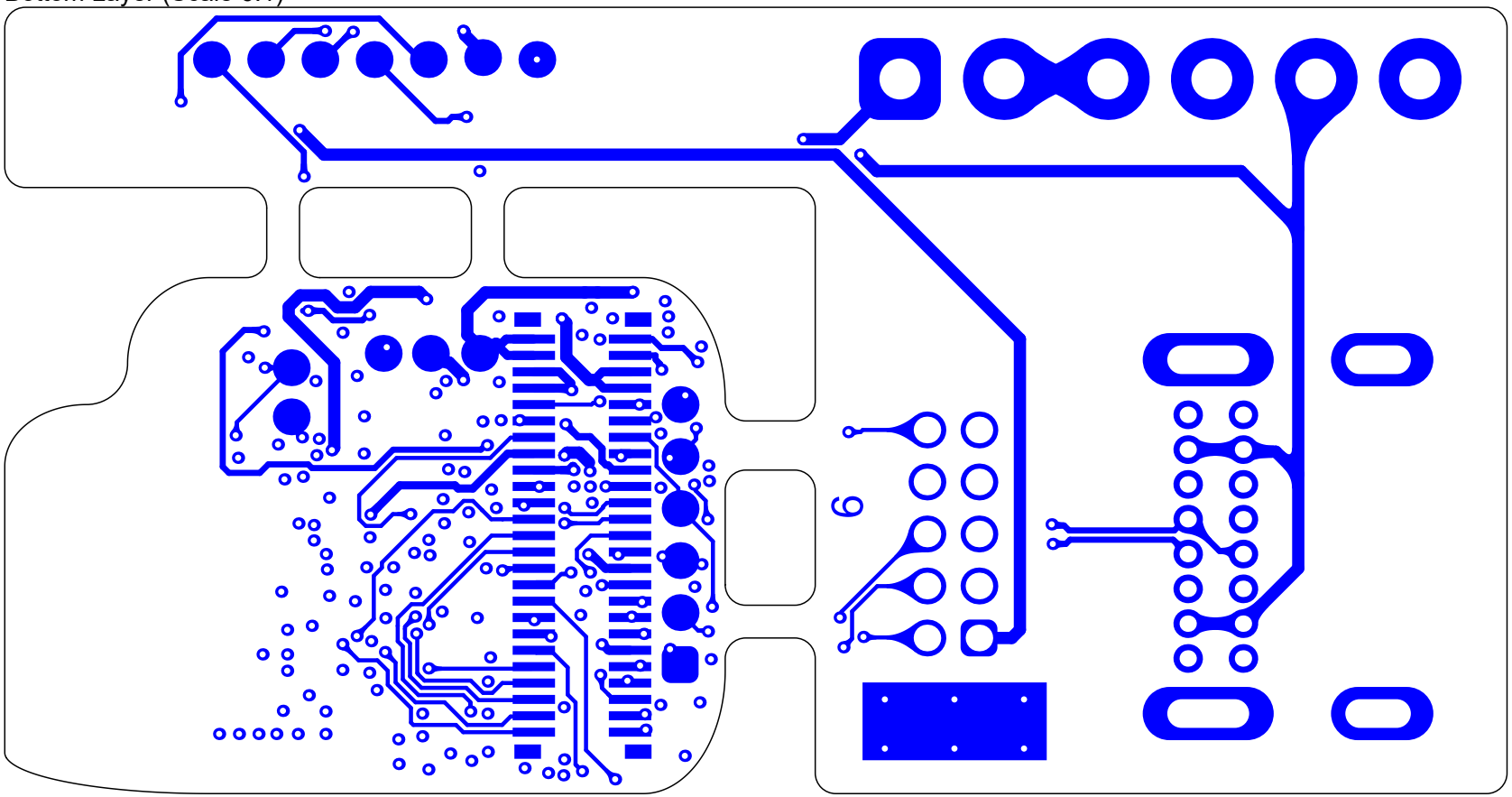
ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Art
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:24 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: PassivesOnlyAssembly	Checked By: Federico Villani, Lukas Schulthess
File: DOC_ART.PCBDwf	Sheet: 4/6

Int4 (Sign) (Scale 6:1)



ETH Eidgenössische Technische Hochschule Zürich Swiss Federal Institute of Technology Zurich	Project: VitalCore: NRF5340
	Art
Laboratory: ETHZ D-ITET PBL	
Date: 3/4/2024 2:24 PM	
Revision: 1.3 License: GNU GPL v3	Drawn By: Philipp Schilk, Alfonso Blanco Fontao
Variant: PassivesOnlyAssembly	Checked By: Federico Villani, Lukas Schulthess
File: DOC_ART.PCBDwf	Sheet: 5/6

Bottom Layer (Scale 6:1)



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Bill Of Materials

Line #	Designator	Comment	Quantity	Design Item Id	Manufacturer	Manufacturer Part Number
1	C1, C2, C2D, C3, C4, C5, C6, C14, C14D, C15D, C16D	100 nF	11	CAP_0201_100n_10V	Murata	GRM033Z71A104KE14D
2	C1D	22µF	1	CAP_0402_22u_6V3	Kyocera AVX	CM05X5R226M06AH080
3	C3D, C4D, C12, C12D, C13, C13D	4.7µF	6	CAP_0402_4.7u_16V	Kyocera AVX	0402YD475MAT2A
4	C5D, C7, C8, C10, C11, C15	1µF	6	CAP_0201_1u_10V	Murata	GRM033C81A105ME05D
5	C6D	10µF	1	CAP_0402_10u_10V	Samsung	CL05A106MP5NUNC
6	C7D	3.3nF	1	CAP_0201_3.3n_16V	Murata	GRM033R71C332KA88D
7	C8D, C9D, C10D, C11D	22µF	4	CAP_0603_22u_10V	Murata	GRM187R61A226ME15D
8	C9	2.2nF	1	CAP_0201_2.2n_16V	Murata	GRM033R71C222KA88D
9	C16	0.7pF	1	CAP_RF_0201_0.7pF	Murata	GJM0335C1ER70BB01D
10	C17D, C18D	110pF	2	CAP_0201_110p_50V	Murata	GRM0335C1H111JA01D
11	D1D	NSR20F30NXT5G	1	D_NSR20F30NXT5G	ON Semiconductor	NSR20F30NXT5G
12	D2D	SML-LX0404SIUPGUSB	1	D_RGB_LED	Lumex	SML-LX0404SIUPGUSB
13	E1	NN03-320	1	NN03-320	Fractus Antennas	NN03-320
14	J1, J2, J3, J4, J5	Solder Jumper	5	JMP_0201_3WAY	Panasonic	ERJ-1GN0R00C
15	JP1D	0R	1	JMP_0201	Panasonic	ERJ-1GN0R00C
16	L1, L2	10µH	2	L_0603_10uH_300mA	Murata	LQM18DN100M70L
17	L1D	2.2µH	1	L_0603_2.2uH_520mA	Taiyo Yuden	MBKK1608T2R2M
18	L2D	1.5µH	1	L_0805_1.5uH_2A	Murata	DFE201210S-1R5M=P2
19	L3, L6, L7	5.6nH	3	L_RF_0201_5.6nH	Murata	LQW03AW5N6J00D
20	L4, L5	2.2nH	2	L_RF_0201_2.2nH	Murata	LQP03HQ2N2B02D
21	R1, R2	2.2kR	2	R_0201_2.2K	Panasonic	ERJ-1GNF2201C
22	R2D, R3D	100kR	2	R_0201_100K	Panasonic	ERJ-1GNF1003C
23	R3	2.2R	1	R_0201_2.2R	Yageo	RC0201FR-072R2L
24	R4, R6D	10kR	2	R_0201_10K	Panasonic	ERJ-1GNF1002C
25	R4D, R5D	5K1	2	R_0402_5K1	Panasonic	ERJ-2RKF5101X
26	RT1D	10kR	1	NTC_0201_10k	Panasonic	ERTJZEG103FA
27	U4D	PESD1USB30	1	PESD1USB30	NXP Semiconductors	PESD1USB30
28	Y1	ECS-.327-9-1210 (32.768kHz)	1	Y_ECS-327-9-1210	ECS International	ECS-.327-9-1210-TR
29	Y2	ECS-320-7-48B-JTM-TR5 (32MHz)	1	Y_ECS-320-7-48B-JTM-TR5	ECS International	ECS-320-7-48B-JTM-TR5

ETH
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