OMTI.5510
IBM PC

5510 CONTROLLER SCHEMATIC
Part # 8606837
Drawn: JC 12/06/84
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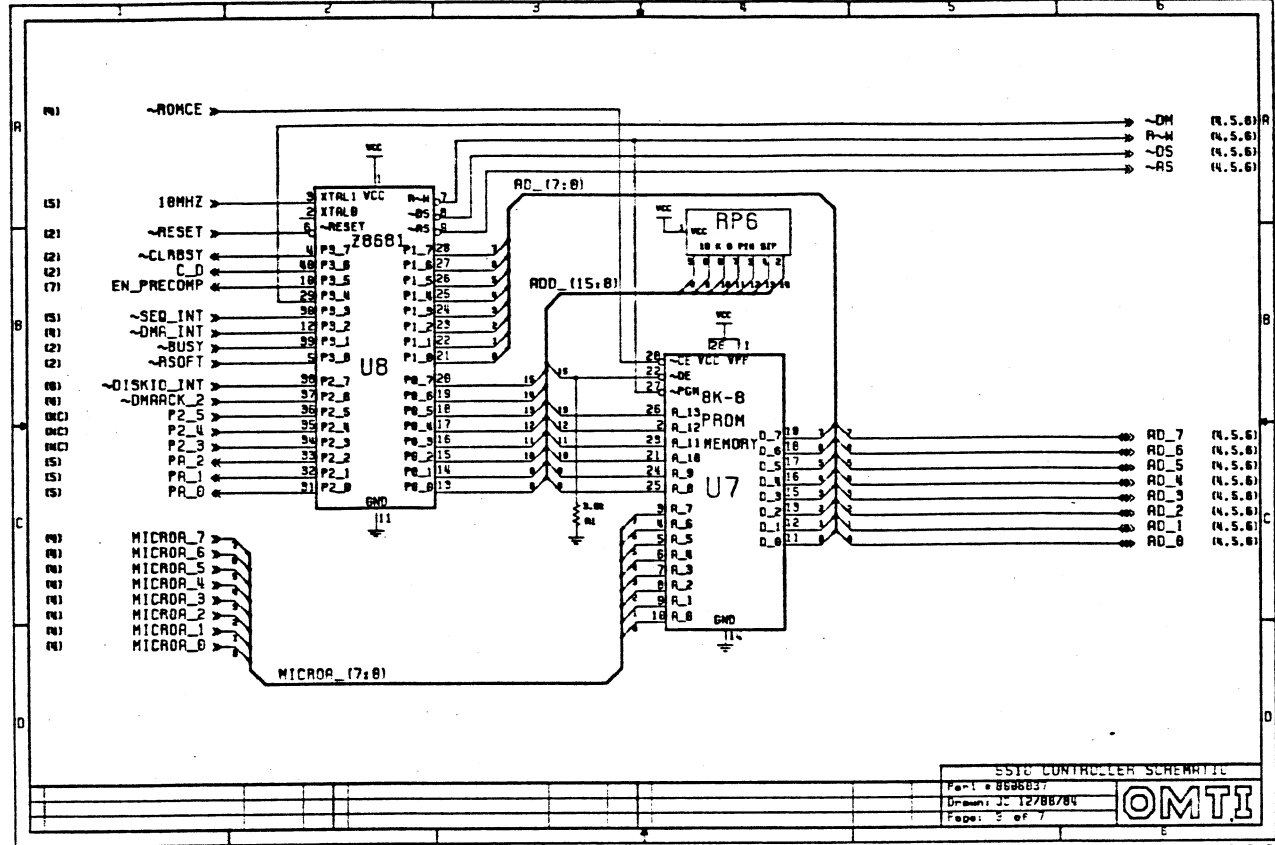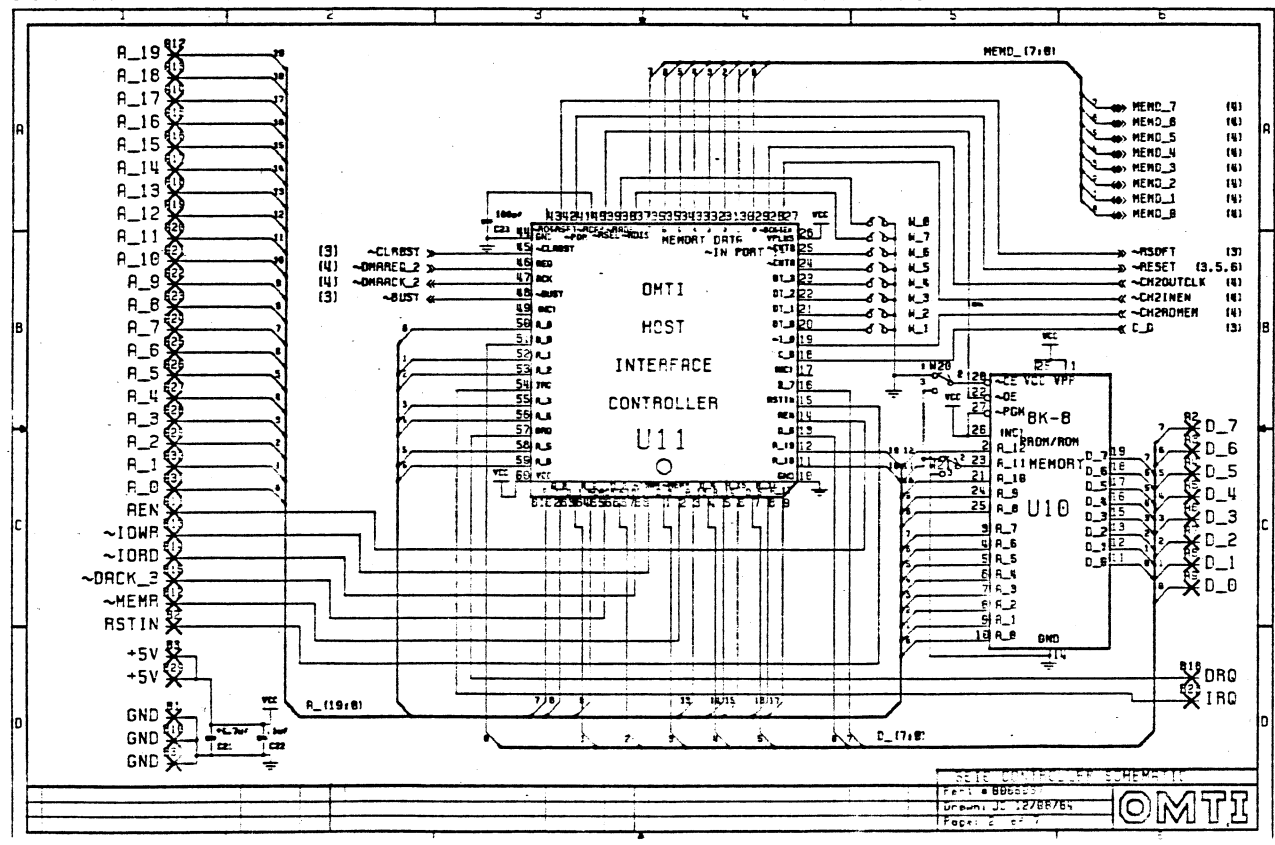
OMTI

Job: V85.Z85.JEFFC.85515.SHEET5

Enqueued: 1/24/1985 3:11 pm (pdt)
Printed: 1/24/1985 3:16 pm (pdt)
Magnification: 8.617879 (auto-scaled)

Sheet 5 — 5515 CONTROLLER SCHEMATIC

VCC
24
VCC   ~CE   18
                       ~OE   20
2K-8   ~WAT 21
RAM
17 D_7   A_10 19
16 D_6   A_9   22
15 D_5   A_8   23
14 D_4 MEMORY
13 D_3   A_7   1   → PA_2   (3)
11 D_2   A_6   2   ← PA_1   (3)
10 D_1   A_5   3   ← PA_0   (3)
9   D_0   A_4   4
               A_3   5
               A_2   6
          U2   A_1   7
               A_0   8
         GND
         12

(4) MEMD_0
(4) MEMD_1
(4) MEMD_2
(4) MEMD_3
(4) MEMD_4
(4) MEMD_5
(4) MEMD_6
(4) MEMD_7

OMTI
PROGRAMMABLE
DATA
SEQUENCER
U3

(4) REQ_0   SEL_A1
(4) ACK_0   SEL_A2
(4) REQ_3   SEL_A3
(4) ACK_3   SEL_A4
(NC) ~INSTB2   ~SEMRT
(NC) ~INSTB3   AM_FOUND → AM_FOUND   (7)
(NC) ~WRTL2   READ/REF_CLK → RD_REF_CLK (7)
(NC) ~WRTL3
(NC) ~GAPRD1   NRZ_IN   → NRZ_IN   (7)
(NC) ~GAPWRT1   NRZ_OUT   → NRZ_OUT   (7)
(3,4,7) 10MHZ   WRT_CLK   → WRT_CLK   (NC)
(2) ~RESET   AM_ENABLE → AM_ENABLE (7)
(NC) 20MHZ   RD_GATE   → RD_GATE   (7)
                   WRT_GATE → WRT_GATE (6,7)
Y1   INDEX   ← INDEX   (6)
20 MHZ   SECTOR   ← SECTOR   (6)
(3) ~SEQ_INT

RD_7 (3)
RD_6 (3)
RD_5 (3)
RD_4 (3)
RD_3 (3)
RD_2 (3)
RD_1 (3)
RD_0 (3)

(3) ~DM
(3) ~DS
(3) R~W
(3) ~AS

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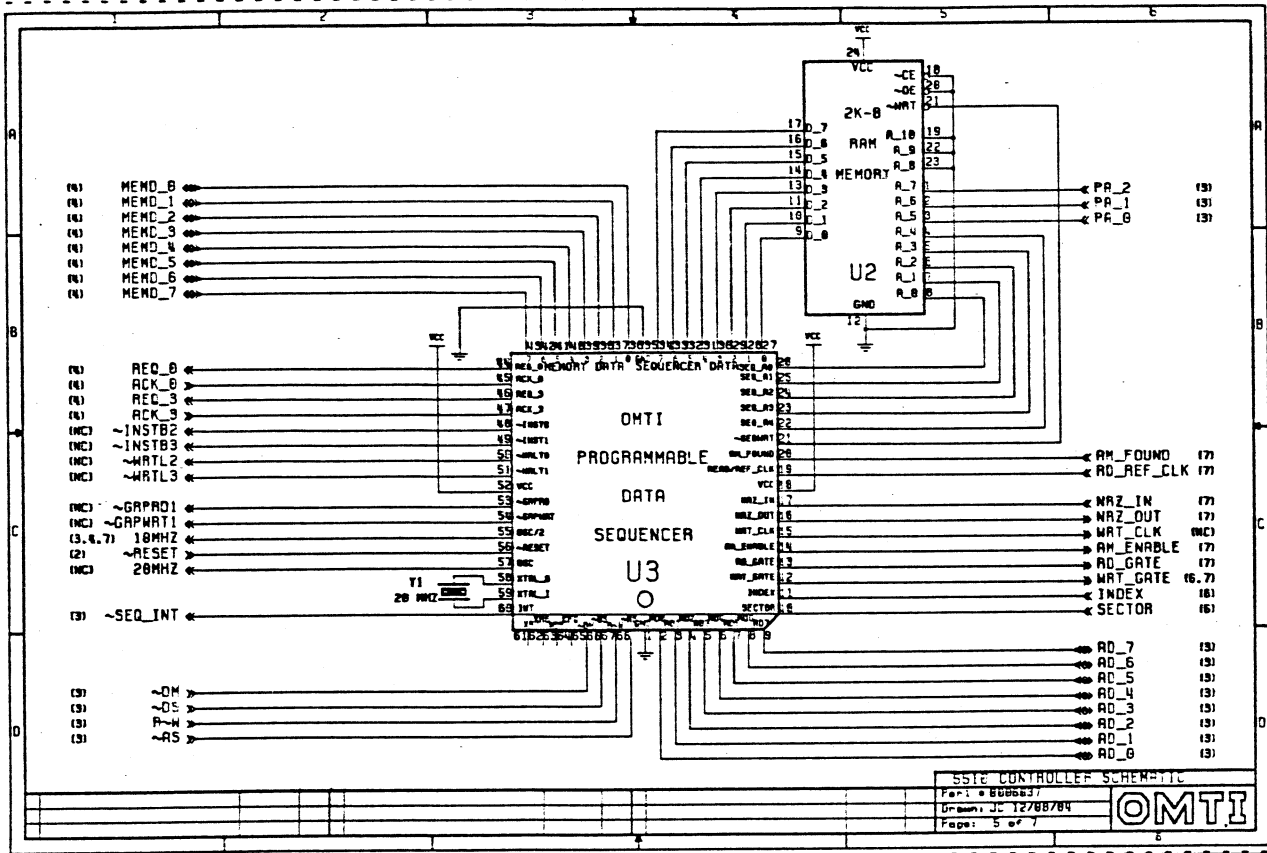OMTI

Job: V85.Z85.JEFFC.85515.SHEET4

Enqueued: 1/24/1985 3:11 pm (pdt)
Printed: 1/24/1985 3:15 pm (pdt)
Magnification: 8.617879 (auto-scaled)

VCC
24
VCC   ~CE   18
               ~OE   20
               ~WAT 21
2K-8
RAM   A_10 19   D_7 17 → MEMD_7 (2,5)
      A_9   22   D_6 16 → MEMD_6 (2,5)
      A_8   23   D_5 15 → MEMD_5 (2,5)
MEMORY A_7 1   D_4 14 → MEMD_4 (2,5)
      A_6   2   D_3 13 → MEMD_3 (2,5)
      A_5   3   D_2 11 → MEMD_2 (2,5)
      A_4   4   D_1 10 → MEMD_1 (2,5)
      A_3   5   D_0 9   → MEMD_0 (2,5)
      A_2   6
      A_1   7   U4
      A_0   8
           GND
           12

OMTI
FOUR_CHANNEL
DMA
CONTROLLER
U5

(2) ~CH2OUTCLK   REQ_0   ← REQ_0   (5)
(2) ~CH2INEN   ACK_0   → ACK_0   (5)
(2) ~CH2RDMEM   REQ_1   ← REQ_1   (NC)
(NC) ~GAPRD0   ACK_1   → ACK_1   (NC)
(NC) ~GAPWRT0   ~DMAREQ_2 ← ~DMAREQ_2 (2)
(5) 10MHZ   ~DMAACK_2 → ~DMAACK_2 (2,3)
                     REQ_3   ← REQ_3   (5)
(NC) ~INSTB0   ACK_3   → ACK_3   (5)
(NC) ~INSTB1
(NC) ~WRTL0   MICRO_A_0 → MICROA_0 (3)
(NC) ~WRTL1   MICRO_A_1 → MICROA_1 (3)
(NC) ~CH1OUTCLK   MICRO_A_2 → MICROA_2 (3)
(NC) ~CH1INEN   MICRO_A_3 → MICROA_3 (3)
(3) ~ROMCE   MICRO_A_4 → MICROA_4 (3)
(3) ~DMA_INT   MICRO_A_5 → MICROA_5 (3)
                     MICRO_A_6 → MICROA_6 (3)
                     MICRO_A_7 → MICROA_7 (3)

RD_7 (3)
RD_6 (3)
RD_5 (3)
RD_4 (3)
RD_3 (3)
RD_2 (3)
RD_1 (3)
RD_0 (3)

(3) ~DM
(3) ~DS
(3) R~W
(3) ~AS

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Job: V85.Z858.JEFFC.S5518.SHEET7

Enqueued: 1/24/1985 3:11 pm (pdt)
Printed: 1/24/1985 3:18 pm (pdt)
Magnification: 8.617879 (auto-scaled)
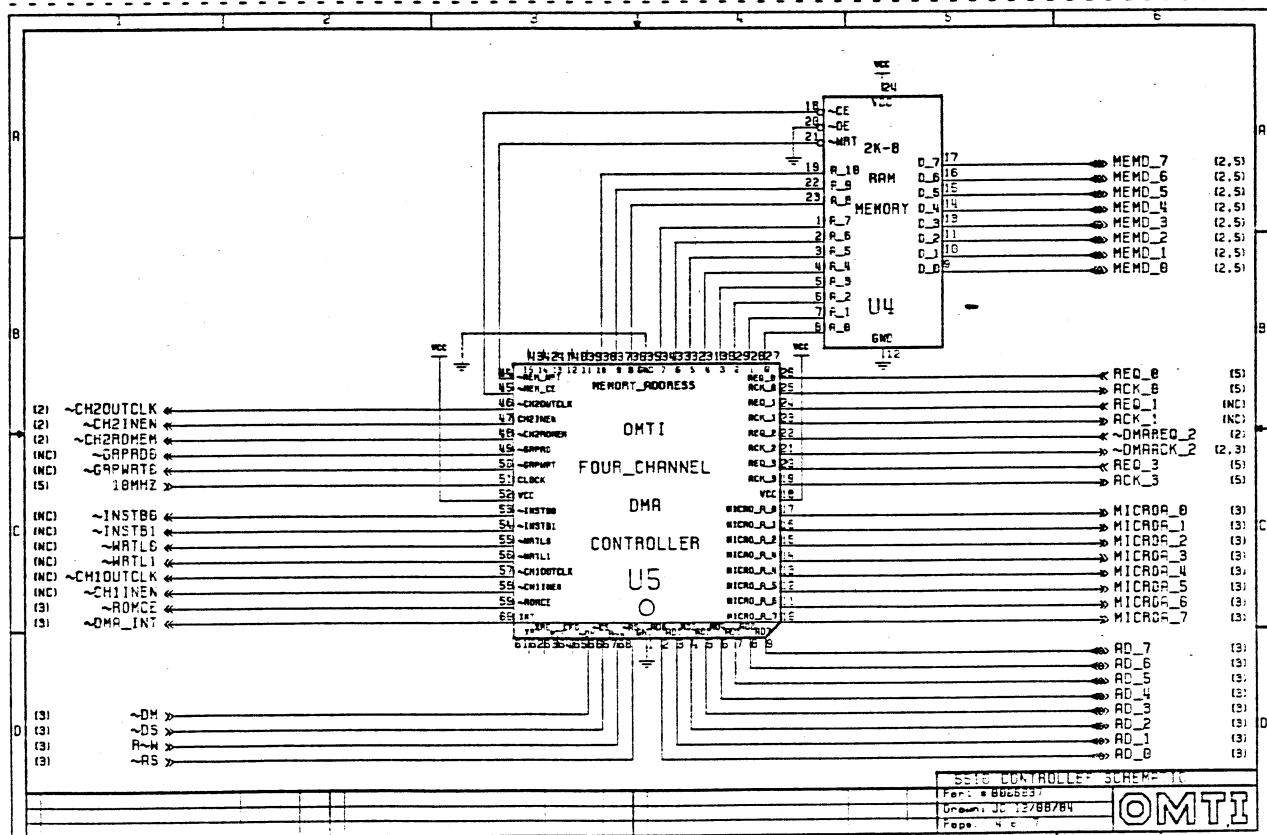
(S) NRZ_OUT

(S) RD_GATE
(S) WRT_GATE
(S) 18MHZ
(S) AM_ENABLE

(3) EN_PRECOMP

DELAY_8UT.TEST
RETRIG_1_SHOT.TEST

OMTI
MFM
ENCOD
DECODE
U6

AM_FOUND   (S)
RD_REF_CLK   (S)
NRZ_IN   (S)

PHASE_COMPARE.TEST

VCC

J-3
RD_0
~RD_0
(S) ~SEL_D-1

J-4
RD_1
~RD_1
(8) ~SEL_D-2

OMTI
Driver
RECEIVER
U9

VCC

J-3
WD_0
~WD_0
(NOTE 3)

J-4
WD_1
~WD_1
(NOTE 4)

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Job: V85.Z858.JEFFC.S5518.SHEET6

Enqueued: 1/24/1985 3:11 pm (pdt)
Printed: 1/24/1985 3:17 pm (pdt)
Magnification: 8.617879 (auto-scaled)

VCC RP4   VCC RP5

J-3
~SEL_D-1
~WRT_PROT-1
~CART_CHG-1

~SEL_D-1   (7)
INDEX   (S)
SECTOR   (S)
WRT_GATE   (S)

J-4
~SEL_D-2
~WRT_PROT-2
~CART_CHG-2

~SEL_D-2   (7)

J-2
~SEK_COMPLT
~TRACK_C
~WRT_FAULT
~SECTOR
~INDEX
~READY
(NOTE 2)

OMTI
DISK I/O
BUS
CONTROLLER
U1

J-2
~HEAD_2-3
~HEAD_2-2
~WRT_GATE
~HEAD_2-0
~HEAD_2-1
~STEP
~DRV_SEL_1
~DRV_SEL_2
~DRV_SEL_3
~DRV_SEL_4
~DIRECTION

AD_0   (3)
AD_1   (3)
AD_2   (3)
AD_3   (3)
AD_4   (3)
AD_5   (3)
AD_6   (3)
AD_7   (3)

(3) ~RESET
(3) ~DM
(3) ~DS
(3) R~W
(3) ~AS

AD_17:8]

~DISKIO_INT (3)

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