

LPC55S69 MCU Powering and USB

The schematic illustrates the power and USB interface for the LPC55S69 microcontroller unit (MCU). Key components include:

- Power Supply:** A +5V input is regulated by U2 (XC6227C331PR-G) to provide a stable +3V3 supply to the MCU's VDDIO pins.
- Voltage Divider:** Resistors R1 (10k) and R2 (20k) divide the +5V input to provide a lower voltage level to the MCU's VDDIO pins.
- Decoupling and Filtering:** Numerous capacitors (C1-C26) and inductors (L1-L4) are used to filter noise and ensure stable power delivery across different voltage domains (VDD, VDDA, VBAT).
- Crystal Oscillator:** Q1 (N32258-16M-STD-CRA) provides the clock signal for the MCU.
- USB Interface:** J9 (USB4110-GF-A_REV B) connects the MCU to a host. Signals include VBUS, D-, D+, SBU1, SBU2, CC1, CC2, GND, and SHIELD.
- SWDIO/SWCLK:** These signals are connected to the MCU's debug pins (LPC_SWIDIO, LPC_SWIDCLK).

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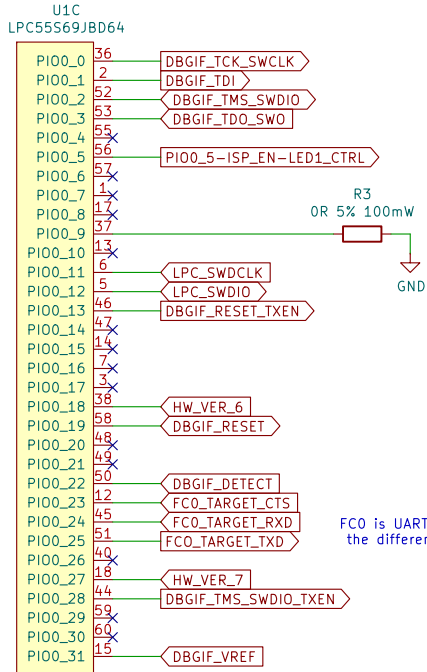
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File: mcmlink_kicad_power_usb.kicad_sch

Title: MCU-Link MR

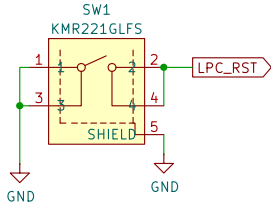
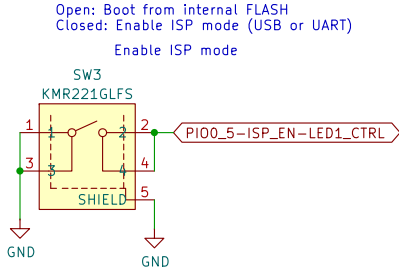
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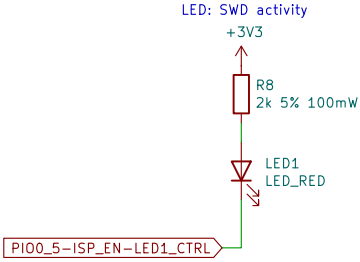
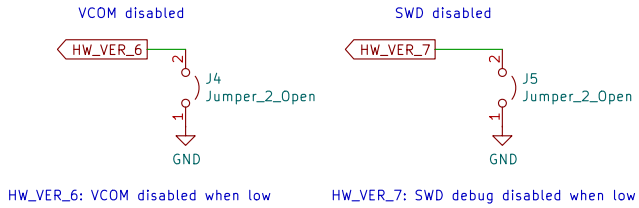
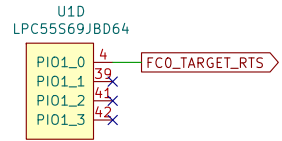
LPC55S69 IO Ports



FCO is UART connection to the different target ports.

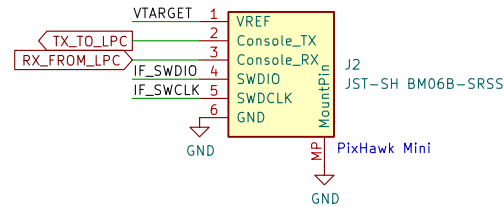
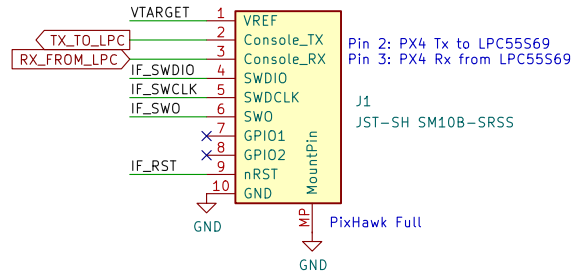


Feature set supported

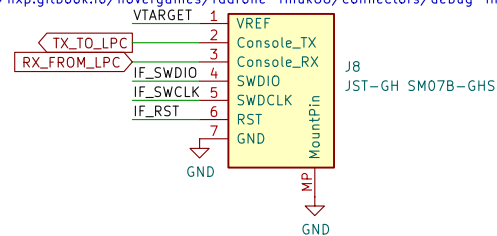


Debug & UART Interface

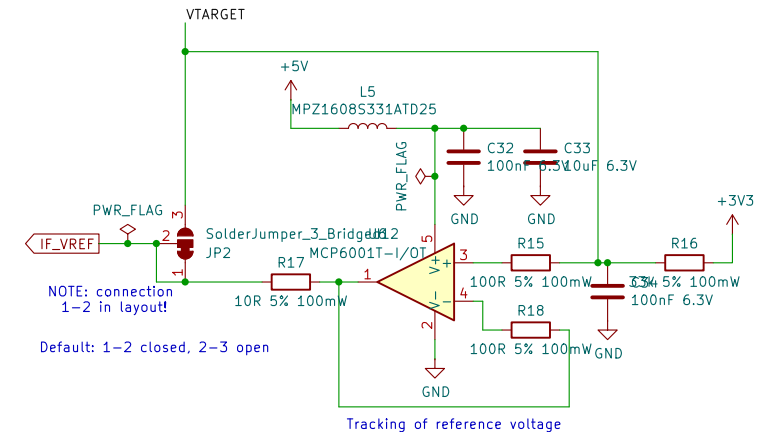
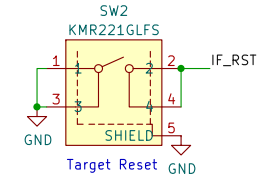
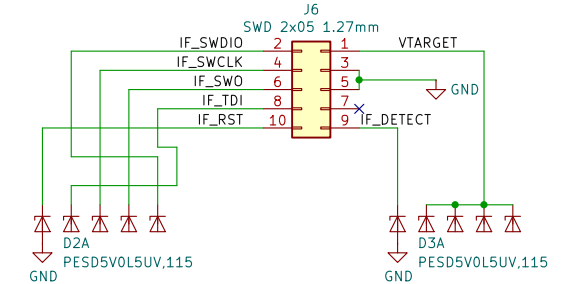
Debug Console: TX/RX is from PX4 point of view
HobbyBro Pixhawk 6X RT: 115200 baud
FTDI Yellow: -> to PC
FTDI Orange: <- from PC



<https://nxp.gitbook.io/hovergames/rddrone-fmuk66/connectors/debug-interface-dcd-lz>



Target Cortex Debug (SWD/JTAG)



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UART Interface to Target (NavQPlus)

UART to NXP NavQPlus:
<https://nxp.gitbook.io/navqplus/hardware/hardware-interfaces/uart/uart2-a53-debug>
1: 5V: not connected
2: TXD: TX from target to debug probe
3: RXD: RX from debug probe to target
4: CTS: CTS from target to debug probe
5: RTS: RTS from debug probe to target
6: GND

The schematic shows four 74LVC1T45GW buffers (U9, U10, U8, U11) used as level shifters. Each buffer has two input/output pairs (A/B and DIR/GND) and two power pins (VCCA/VCCB). The inputs are labeled FCO_TARGET_RXD, FCO_TARGET_TXD, FCO_TARGET_CTS, and FCO_TARGET_RTS. The outputs are connected to a JST-GH BM06B-GHS connector (J11) pins 1 through 6. Power supply connections include +3V3, GND, and IF_VREF. Capacitors C40-C47 (100nF 6.3V) are placed near the power pins. Resistors R25-R28 (10k 5% 100mW) are connected between the output pins and ground.

UART to NXP NavQPlus:
<https://nxp.gitbook.io/navqplus/hardware/hardware-interfaces/uart/uart2-a53-debug>
 1: 5V: not connected
 2: TXD: TX from target to debug probe
 3: RXD: RX from debug probe to target
 4: CTS: CTS from target to debug probe
 5: RTS: RTS from debug probe to target
 6: GND

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