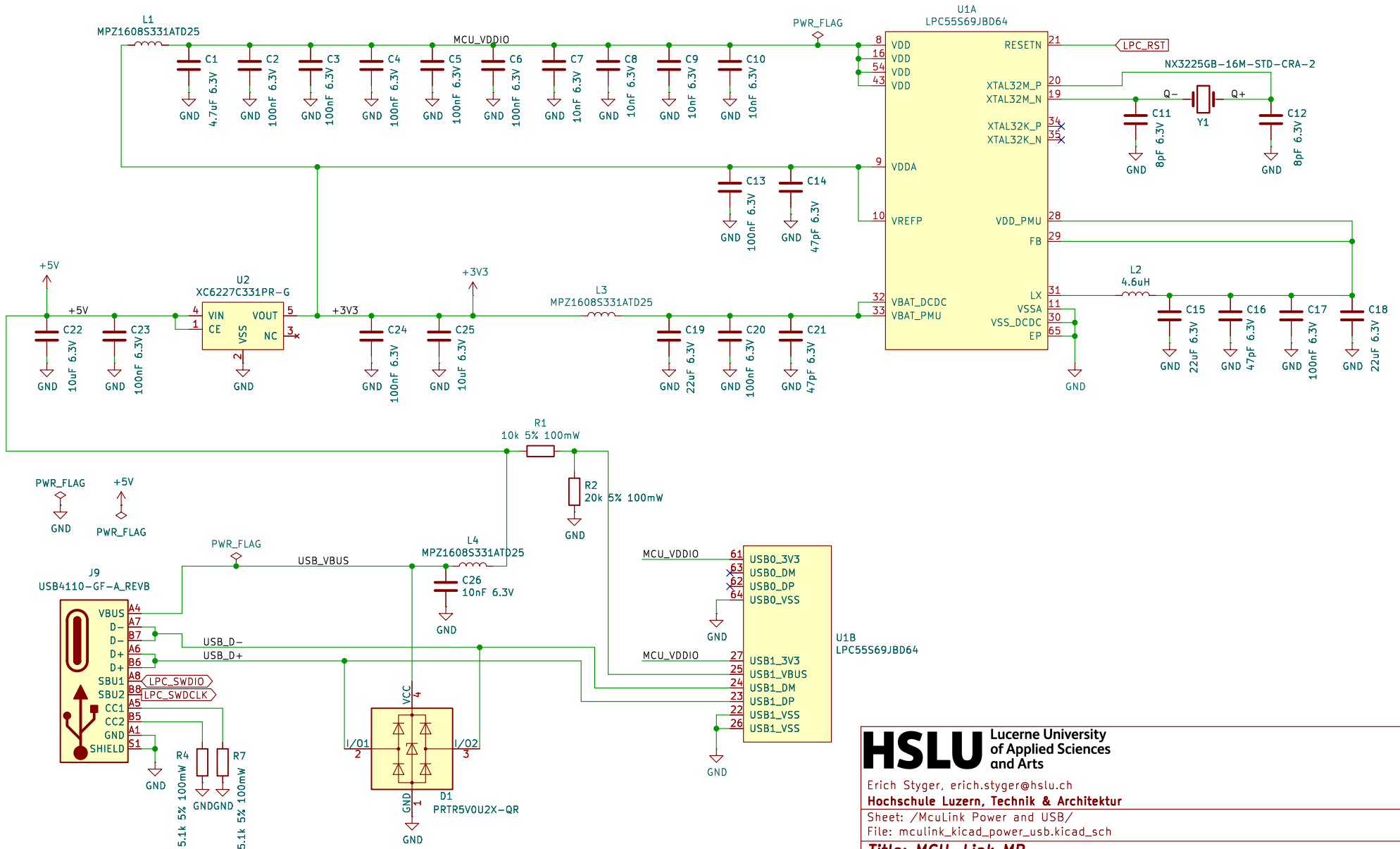


LPC55S69 MCU Powering and USB



HSLU Lucerne University
of Applied Sciences
and Arts

Erich Styger, erich.styger@hslu.ch

Hochschule Luzern, Technik & Architektur

Sheet: /McuLink Power and USB/

File: mcmlink_kicad_power_usb.kicad_sch

Title: MCU-Link MR

Size: A4

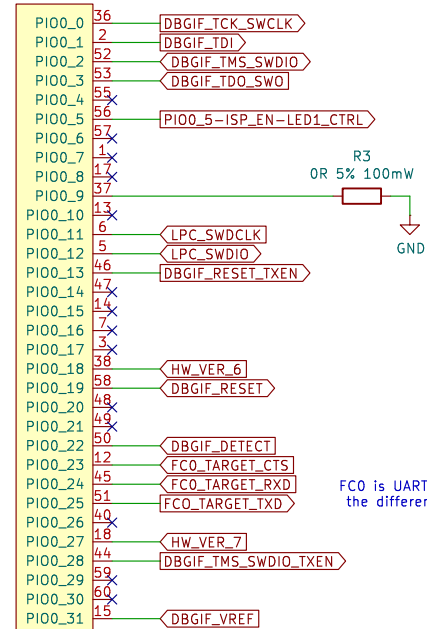
Date: 2024-04-28

Rev: v0.2

KiCad E.D.A. 9.0.5

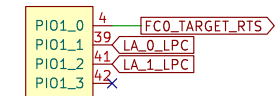
Id: 2/5

U1C
LPC55569JBD64



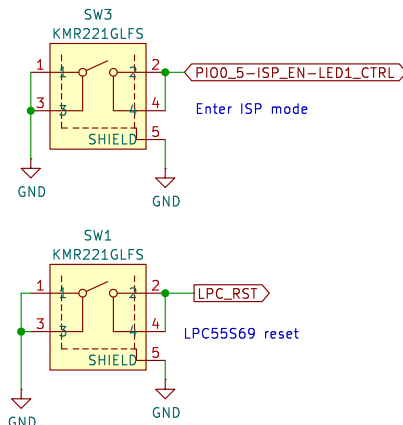
FCO is UART connection to the different target ports.

U1D
LPC55569JBD64

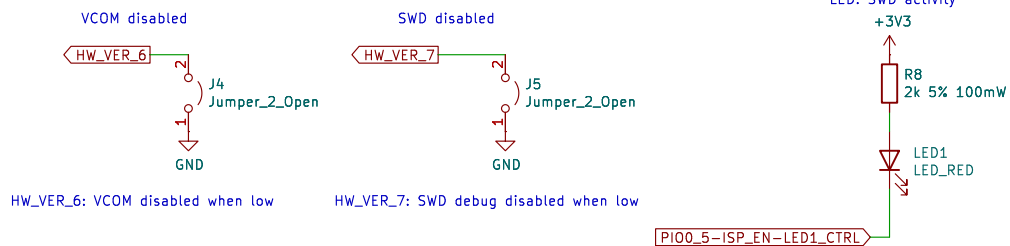


LPC55569 IO Ports

Open: Boot from internal FLASH
Closed: Enable ISP mode (USB or UART)
Enable ISP mode



Feature set supported



HSLU Lucerne University
of Applied Sciences
and Arts

Erich Styger, erich.styger@hslu.ch

Hochschule Luzern, Technik & Architektur

Sheet: /LPC55569 IO Ports/

File: mculink_kicad_ioports.kicad_sch

Title: MCU-Link MR

Size: A4 Date: 2025-10-29

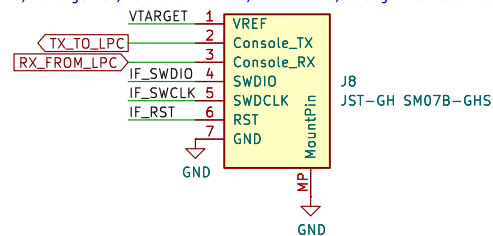
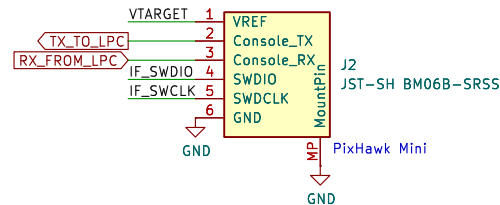
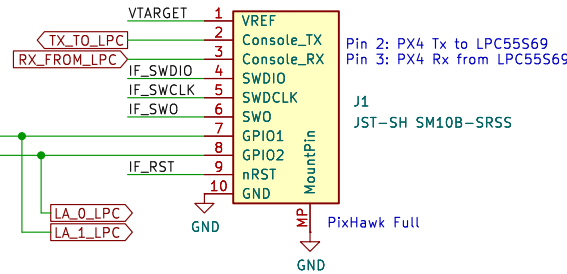
KiCad E.D.A. 9.0.5

Rev: v0.5

Id: 3/5

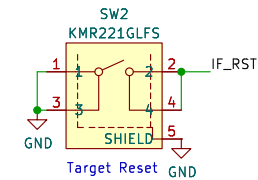
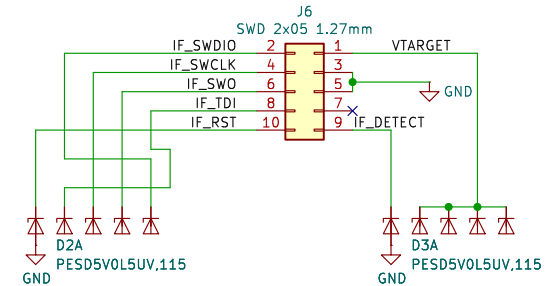
Debug & UART Interface

Debug Console: TX/RX is from PX4 point of view
 Holybro Pixhawk 6X RT: 115200 baud
 FTDI Yellow: -> to PC
 FTDI Orange: <- from PC

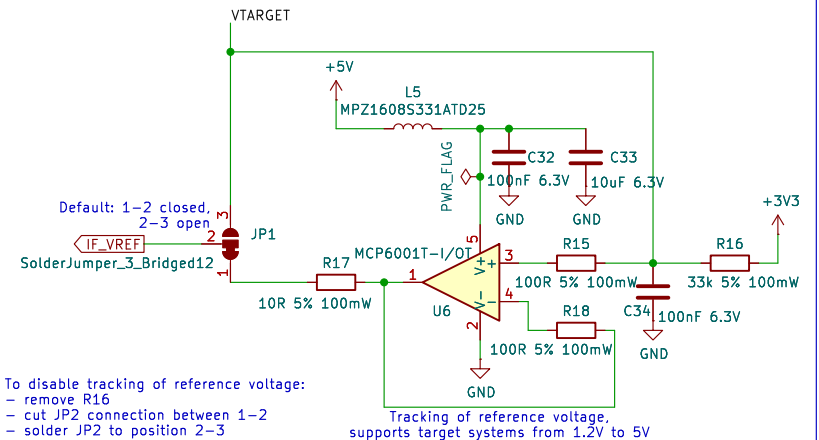


<https://nxp.gitbook.io/hovergames/rddrone-fmuk66/connectors/debug-interface-dcd-lz>

Target Cortex Debug (SWD/JTAG)



Circuit tracks target reference voltage (VTARGET) and generates IF_VREF output voltage.



HSLU Lucerne University of Applied Sciences and Arts

Erich Styger, erich.styger@hslu.ch

Hochschule Luzern, Technik & Architektur

Sheet: /Debug interface/

File: mcmlink_kicad_debug.kicad_sch

Title: MCU-Link MR

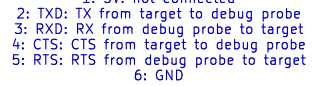
Size: A4 Date: 2024-11-24

KiCad E.D.A. 9.0.5

Rev: v0.5

Id: 4/5

UART to NXP NavQPlus:
<https://nxp.gitbook.io/navqplus/hardware/hardware-interfaces/uart/uart2-a53-debug>



Rev: v0.3
Id: 5/5