MM54C922,MM54C923,MM74C922,MM74C923

MM54C922 MM74C922 16-Key Encoder MM54C923 MM74C923 20-Key Encoder

TEXAS INSTRUMENTS

Literature Number: SNOS345A

National Semiconductor

July 1993

MM54C922/MM74C922 16-Key Encoder
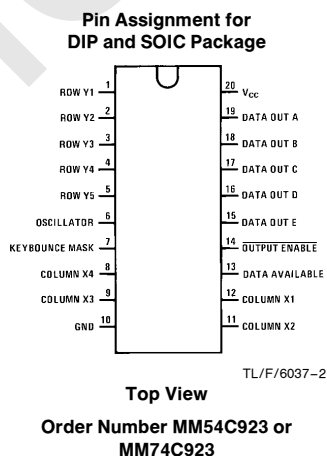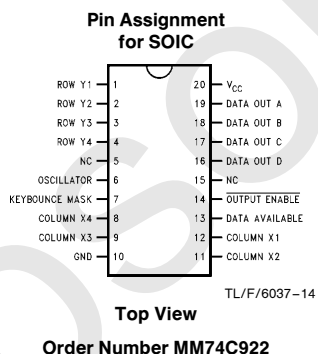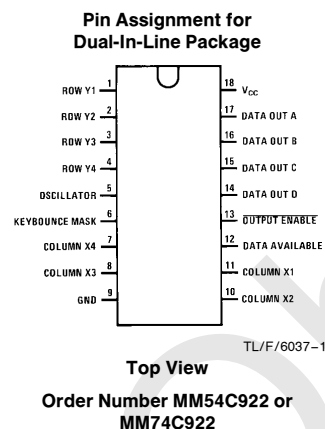# MM54C923/MM74C923 20-Key Encoder

General Description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outsput LPTTL compatible
- Wide supply range   3V to 15V
- Low power consumption

Connection Diagrams

Pin Assignment for Dual-In-Line Package

ROW Y1 — 1	18 — V_CC
ROW Y2 — 2	17 — DATA OUT A
ROW Y3 — 3	16 — DATA OUT B
ROW Y4 — 4	15 — DATA OUT C
OSCILLATOR — 5	14 — DATA OUT D
KEYBOUNCE MASK — 6	13 — OUTPUT ENABLE
COLUMN X4 — 7	12 — DATA AVAILABLE
COLUMN X3 — 8	11 — COLUMN X1
GND — 9	10 — COLUMN X2

TL/F/6037–1

Top View

Order Number MM54C922 or MM74C922

Pin Assignment for SOIC

ROW Y1 — 1	20 — V_CC
ROW Y2 — 2	19 — DATA OUT A
ROW Y3 — 3	18 — DATA OUT B
ROW Y4 — 4	17 — DATA OUT C
NC — 5	16 — DATA OUT D
OSCILLATOR — 6	15 — NC
KEYBOUNCE MASK — 7	14 — OUTPUT ENABLE
COLUMN X4 — 8	13 — DATA AVAILABLE
COLUMN X3 — 9	12 — COLUMN X1
GND — 10	11 — COLUMN X2

TL/F/6037–14

Top View

Order Number MM74C922

Pin Assignment for DIP and SOIC Package

ROW Y1 — 1	20 — V_CC
ROW Y2 — 2	19 — DATA OUT A
ROW Y3 — 3	18 — DATA OUT B
ROW Y4 — 4	17 — DATA OUT C
ROW Y5 — 5	16 — DATA OUT D
OSCILLATOR — 6	15 — DATA OUT E
KEYBOUNCE MASK — 7	14 — OUTPUT ENABLE
COLUMN X4 — 8	13 — DATA AVAILABLE
COLUMN X3 — 9	12 — COLUMN X1
GND — 10	11 — COLUMN X2

TL/F/6037–2

Top View

Order Number MM54C923 or MM74C923

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin $V_{CC} - 0.3V$ to $V_{CC} + 0.3V$

Operating Temperature Range
  MM54C922, MM54C923 $-55°C$ to $+125°C$
  MM74C922, MM74C923 $-40°C$ to $+85°C$

Storage Temperature Range $-65°C$ to $+150°C$

Power Dissipation (P_D)
  Dual-In-Line 700 mW
  Small Outline 500 mW

Operating V_{CC} Range 3V to 15V

V_{CC} 18V

Lead Temperature
  (Soldering, 10 seconds) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	$V_{CC} = 5V$, $I_{IN} \geq 0.7$ mA	3.0	3.6	4.3	V
		$V_{CC} = 10V$, $I_{IN} \geq 1.4$ mA	6.0	6.8	8.6	V
		$V_{CC} = 15V$, $I_{IN} \geq 2.1$ mA	9.0	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	$V_{CC} = 5V$, $I_{IN} \geq 0.7$ mA	0.7	1.4	2.0	V
		$V_{CC} = 10V$, $I_{IN} \geq 1.4$ mA	1.4	3.2	4.0	V
		$V_{CC} = 15V$, $I_{IN} \geq 2.1$ mA	2.1	5	6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	$V_{CC} = 5V$	3.5	4.5		V
		$V_{CC} = 10V$	8.0	9		V
		$V_{CC} = 15V$	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	$V_{CC} = 5V$		0.5	1.5	V
		$V_{CC} = 10V$		1	2	V
		$V_{CC} = 15V$		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	$V_{CC} = 5V$, $V_{IN} = 0.1 V_{CC}$		-2	-5	μA
		$V_{CC} = 10V$		-10	-20	μA
		$V_{CC} = 15V$		-22	-45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10$ μA	4.5			V
		$V_{CC} = 10V$, $I_O = -10$ μA	9			V
		$V_{CC} = 15V$, $I_O = -10$ μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = 10$ μA			0.5	V
		$V_{CC} = 10V$, $I_O = 10$ μA			1	V
		$V_{CC} = 15V$, $I_O = 10$ μA			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	$V_{CC} = 5V$, $V_O = 0.5V$		500	1400	Ω
		$V_{CC} = 10V$, $V_O = 1V$		300	700	Ω
		$V_{CC} = 15V$, $V_O = 1.5V$		200	500	Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	$V_{CC} = 5V$		0.55	1.1	mA
		$V_{CC} = 10V$		1.1	1.9	mA
		$V_{CC} = 15V$		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$ $I_O = -360$ μA	2.4			V
		74C, $V_{CC} = 4.75V$ $I_O = -360$ μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$ $I_O = -360$ μA			0.4	V
		74C, $V_{CC} = 4.75V$ $I_O = -360$ μA			0.4	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

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DC Electrical Characteristics
Min/Max limits apply across temperature range unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$, $T_A = 25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25°C$	-8	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	8	16		mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	$C_L = 50$ pF *(Figure 1)* $V_{CC} = 5V$ $V_{CC} = 10V$ $V_{CC} = 15V$		60 35 25	150 80 60	ns ns ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	$R_L = 10k$, $C_L = 10$ pF *(Figure 2)* $V_{CC} = 5V$, $R_L = 10k$ $V_{CC} = 10V$, $C_L = 10$ pF $V_{CC} = 15V$		80 65 50	200 150 110	ns ns ns
t_{H0}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	$R_L = 10k$, $C_L = 50$ pF *(Figure 2)* $V_{CC} = 5V$, $R_L = 10k$ $V_{CC} = 10V$, $C_L = 50$ pF $V_{CC} = 15V$		100 55 40	250 125 90	ns ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output (Note 2)		10		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms
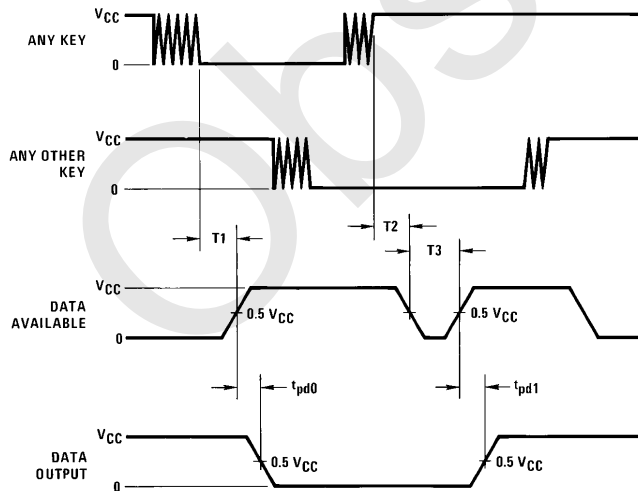
T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC, where R ≈ 10k and C is external capacitor at KBM input.
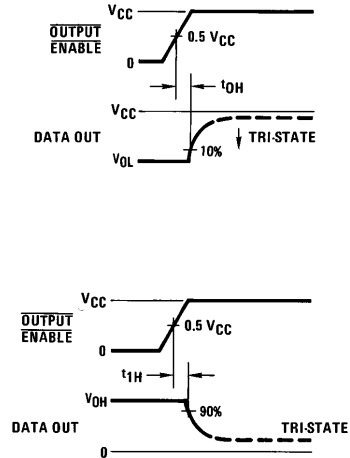
TL/F/6037–3

FIGURE 1

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FIGURE 2

Block Diagram
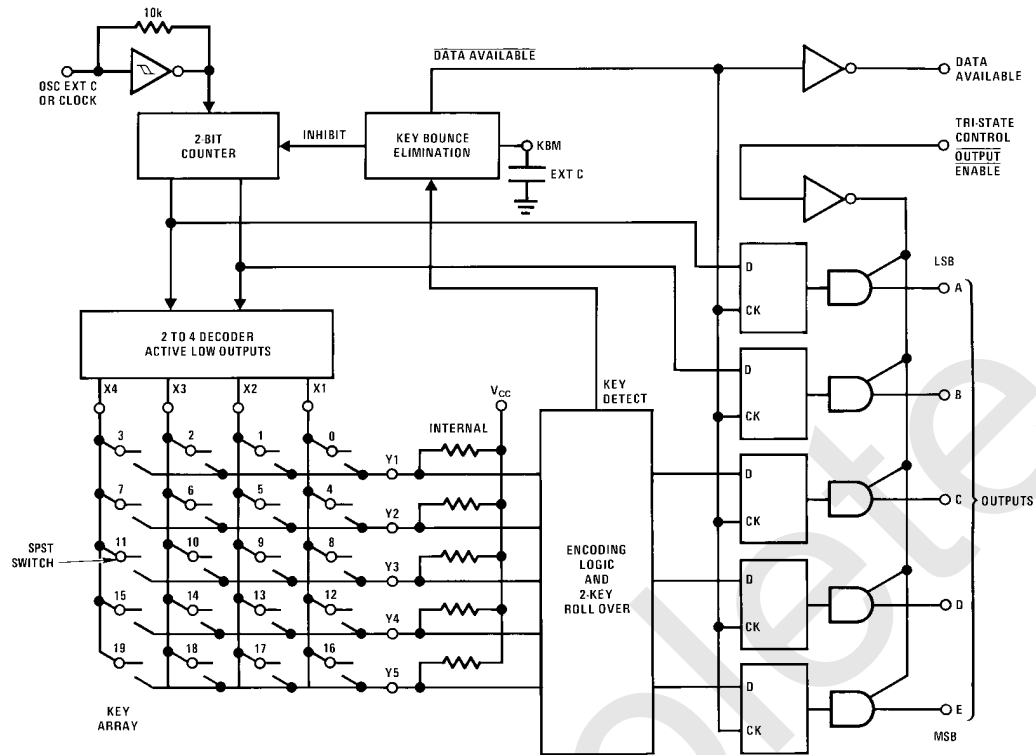
TL/F/6037–5

Truth Table

Switch Position	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5*,X1	17 Y5*,X2	18 Y5*,X3	19 Y5*,X4
D A T A A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
O C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
U D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
T E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

*Omit for MM54C922/MM74C922

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Typical Performance Characteristics

Typical I_{rp} vs V_{IN} at Any Y Input

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Typical R_{on} vs V_{OUT} at Any X Output

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Typical F_{SCAN} vs C_{OSC}

TL/F/6037–8

Typical Debounce Period vs C_{KBM}
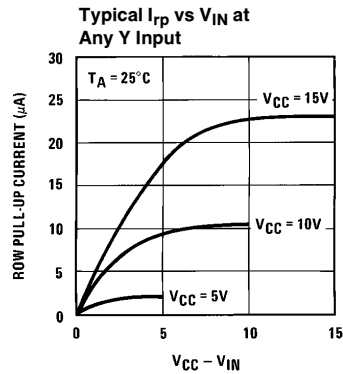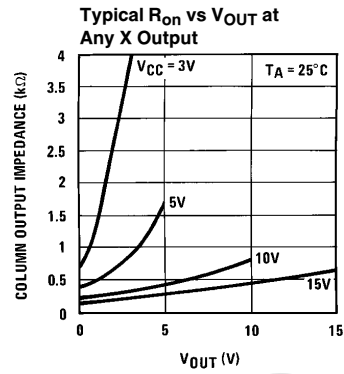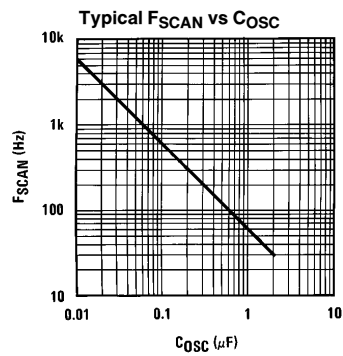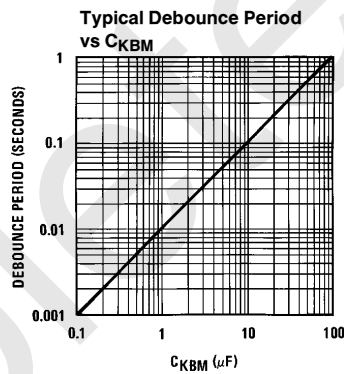
TL/F/6037–9

Typical Applications

Synchronous Handshake (MM74C922)
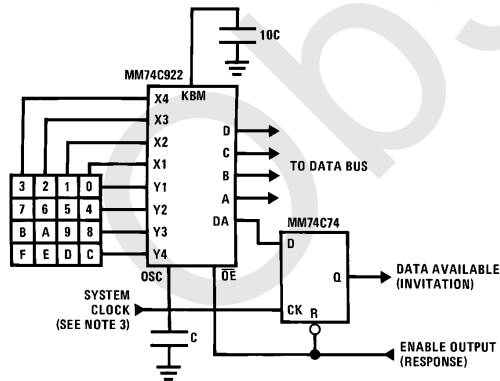
TL/F/6037–10

Synchronous Data Entry Onto Bus (MM74C922)
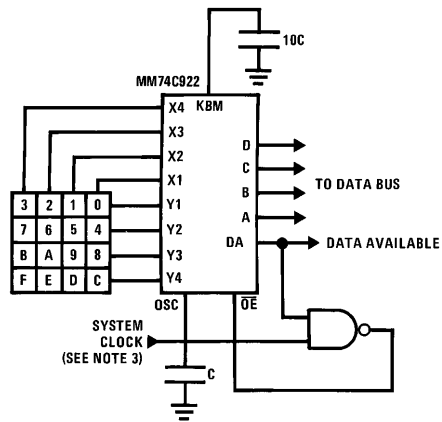
TL/F/6037–11

Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

5

Typical Applications (Continued)

Asynchronous Data Entry Onto Bus (MM74C922)
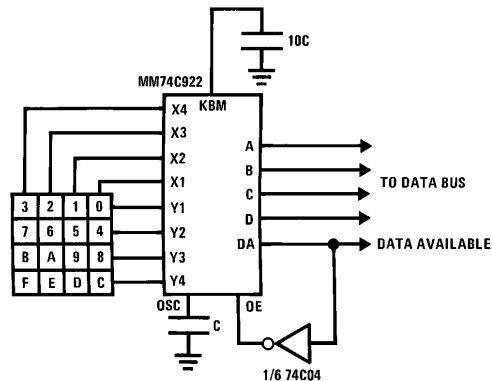
Outputs are in TRI-STATE until key is pressed, then data is placed on bus.
When key is released, outputs return to TRI-STATE.

TL/F/6037–12

Expansion to 32 Key Encoder (MM74C922)
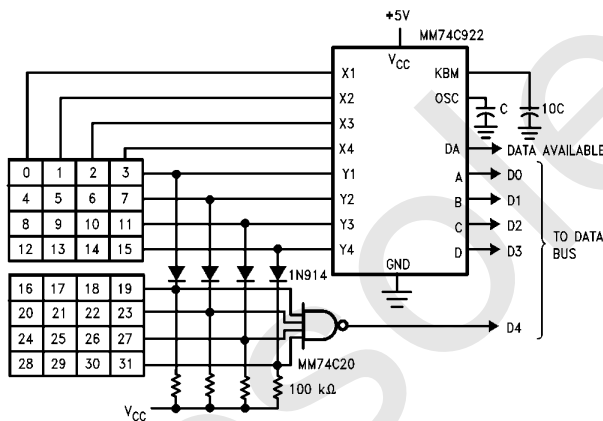
TL/F/6037–13

Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going

low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed TRI-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

6

Physical Dimensions inches (millimeters)

0.020
(0.508) RAD MAX

0.025
(0.635) RAD

0.915
(23.24) MAX

18 17 16 15 14 13 12 11 10

1 2 3 4 5 6 7 8 9

0.310
(7.874) MAX

0.005
(0.127) MIN

0.200
(5.080) MAX

0.037 ± 0.005
(0.940 ± 0.127)

0.020 − 0.060
(0.508 − 1.524)

0.125 − 0.200
(3.175 − 5.080)

0.290 − 0.320
(7.366 − 8.128)

0.055 ± 0.005
(1.397 ± 0.127)

GLASS SEALANT

0.180
(4.572) MAX

0.008 − 0.012
(0.203 − 0.305)

95° ± 5°

86° 94°
TYP

0.310 − 0.410
(7.874 − 10.41)

0.100 ± 0.010
(2.540 ± 0.254) TYP

0.018 ± 0.003
(0.457 ± 0.076) TYP

0.098
(2.489) MAX
BOTH ENDS

0.150
(3.810) MIN

J18A (REV L)
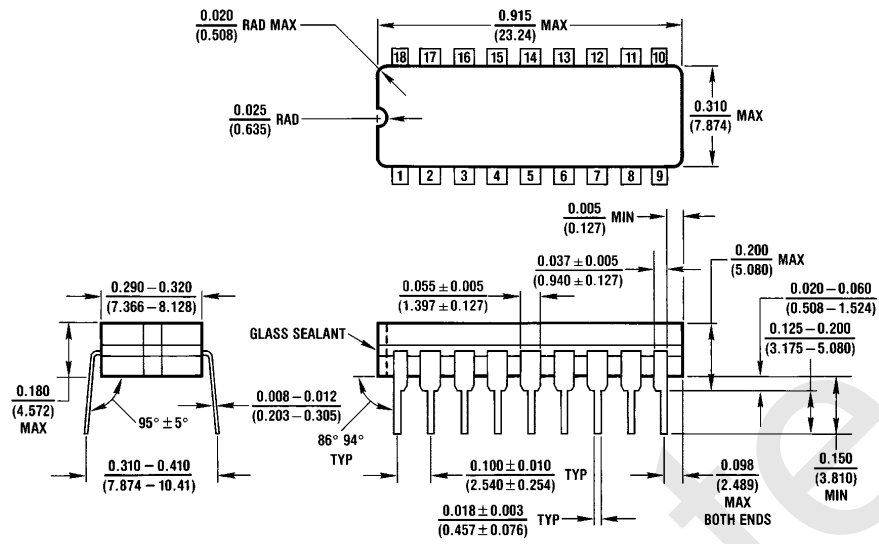
Ceramic Dual-In-Line Package (J)
Order Number MM54C922J or MM74C922J
NS Package Number J18A

0.025
(0.635) RAD

0.985
(25.019) MAX

20 19 18 17 16 15 14 13 12 11

1 2 3 4 5 6 7 8 9 10

0.220 − 0.310
(5.588 − 7.874)

0.005 − 0.020
(0.127 − 0.508) RAD TYP

0.037 ± 0.005
(0.940 ± 0.127)

0.180
(4.572) MAX

0.290 − 0.320
(7.366 − 8.128)

GLASS SEALANT

0.005
(0.127) MIN

0.055 ± 0.005
(1.397 ± 0.127)

0.020 − 0.060
(0.508 − 1.524)

0.200
(5.080) MAX

0.150
(3.810) MIN

0.125 − 0.200
(3.175 − 5.080)

95° ± 5°

0.008 − 0.012
(0.203 − 0.305)

86° 94°

0.310 − 0.410
(7.874 − 10.41)

0.060
(1.524) MAX
BOTH ENDS

0.100 ± 0.010
(2.540 ± 0.254)

0.018 ± 0.003
(0.457 ± 0.076)

J20A (REV M)
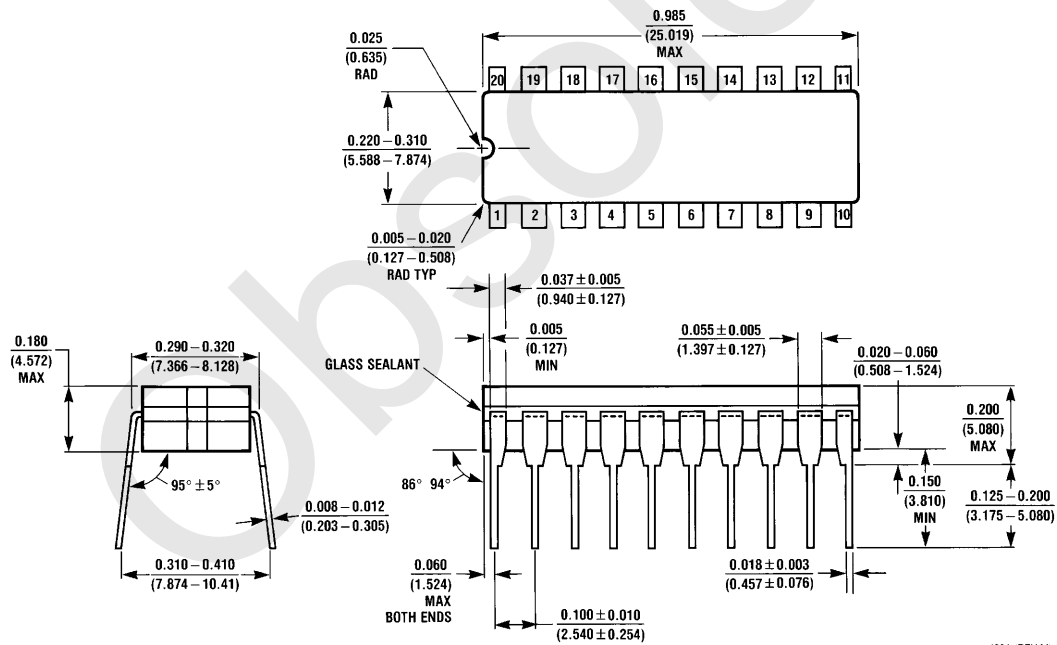
Ceramic Dual-In-Line Package (J)
Order Number MM54C923J or MM74C923J
NS Package Number J20A

7

Physical Dimensions inches (millimeters) (Continued)

0.496 − 0.512
(12.598 − 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 − 0.419
(10.008 − 10.643)

LEAD NO. 1
IDENT

1 2 3 4 5 6 7 8 9 10

30° TYP

0.010
(0.254) MAX

0.291 − 0.299
(7.391 − 7.595)

0.010 − 0.029
(0.254 − 0.737) × 45°

8° MAX TYP
ALL LEADS

0.009 − 0.013
(0.229 − 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.093 − 0.104
(2.362 − 2.642)

0.004 − 0.012
(0.102 − 0.305)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020
(0.356 − 0.508) TYP

M20B (REV F)
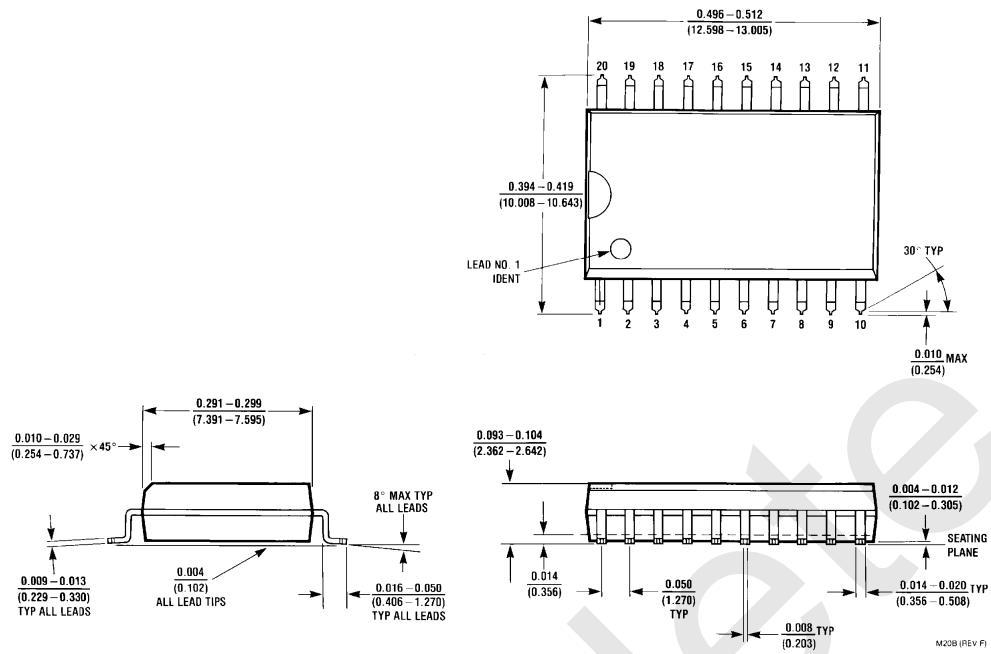
Plastic Small Outline I.C. Package (M)
Order Number MM74C922M or MM74C923M
NS Package Number M20B
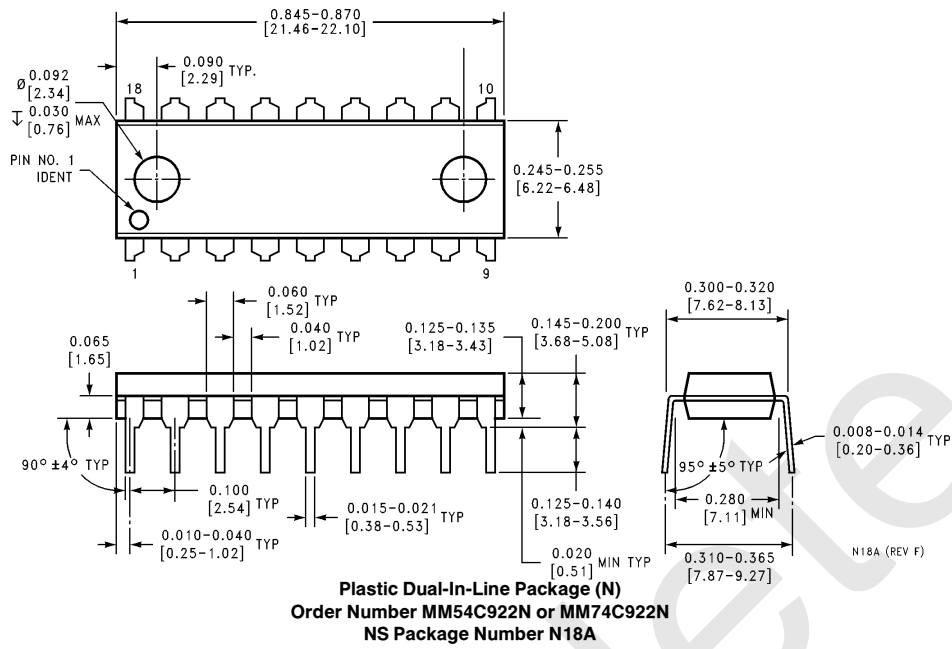
Physical Dimensions inches (millimeters) (Continued)

Plastic Dual-In-Line Package (N)
Order Number MM54C922N or MM74C922N
NS Package Number N18A

N18A (REV F)

Physical Dimensions inches (millimeters) (Continued)

1.013–1.040
(25.73–26.42)

0.092 × 0.030
(2.337 × 0.762)
MAX DP

PIN NO. 1 IDENT

OPTION 1

0.260 ±0.005
(6.604 ±0.127)

0.032 ±0.005
(0.813 ±0.127)
RAD

PIN NO. 1 IDENT

OPTION 2

0.280
(7.112)
MIN

0.300–0.320
(7.620–8.128)

0.065
(1.651)

0.090
(2.286)

0.060
(1.524)
NOM
TYP

0.040
(1.016)
TYP

OPTION 2
4° (4X)

0.130 0.005
(3.302 0.127)

0.145–0.200
(3.683–5.080)

95°± 5°

0.009–0.015
(0.229–0.381)
TYP

0.060 ±0.005
(1.524 ± 0.127)

0.100 ±0.010
(2.540 ±0.254)

0.018 ±0.003
(0.457 ±0.076)

90°± 0.004°

0.020
(0.508)
MIN

0.125–0.140
(3.175–3.556)

0.325 +0.040
       −0.015

(8.255 +1.016
         −0.381)

N20A (REV G)

Plastic Dual-In-Line Package (N)
Order Number MM54C923N or MM74C923N
NS Package Number N20A

Obsolete

IMPORTANT NOTICE