Answers to Self-Test Questions

Tutorial 9: Using the General Purpose Timers

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1.	Using time delays for controlling the time between events is inefficient. While the delay loop is executing, no other processing can be done.
2.	The *Event Manager* of the TMS320F24x is a hardware block of timers and counters, which can be used to control events and generate outputs. The TMS320F243 has a single *Event Manager* (EV), and the TMS320LF2407 has two (EVA and EVB).
3.	The term GP T1 means General Purpose Timer 1.
4.	The term "continuous up-counting mode" means that the counter counts 0, then counts 1, 2, 3 etc until a maximum value is reached. Counting then starts over again automatically at zero.
5.	At power up, the PWM outputs of the TMS320F24x controlled by GPT1 and GPT2 are turned off. To turn them on, we must set the appropriate bits of Output Control Register (OCRA) of the TMS320F243. The TMS320LF2407 uses the name Mode Control Register (MCRA) instead.
6.	A *pre-scaler* is a frequency divider, which is used to slow down the clock applied to General Purpose Timer 1 (GPT1) and General Purpose Timer 2 (GPT2). This extends the period of the timer.
7.	The maximum value we can use for T1PR is FFFFh. This causes the timer to run slowly.
8.	The minimum value we can use for T1PR is 1.
9.	The term *period* when applied to a timer means the amount of time between repeated sequences.
10.	The *duty cycle* is the percentage of the time per repeated sequence where the output is active. For example, full on would be 100%, while full off would be 0%.
11.	It is important to set up T1CNT to –1 or –2 when setting up GP T1 because a timer can have any value. Setting T1CNT to –1 or –2 guarantees that the timer is near roll-over, and will therefore always contain a value less than T1PR. This is more important for slow clock speeds.
12.	If we make T1CMP greater than T1PR, there will be no waveform generated on T1PWM.
13.	To use the instruction `LACC` to perform a shift to the right, we in fact shift to the left, then ignore the low 16 bits of the accumulator. This works because ignoring the low 16 bits of the accumulator is equivalent to a shift of 16 to the right. Hence a shift of 15 to the right is implemented as a shift of 1 to the left and ignoring the low word of the accumulator. This makes the total shift to the right of +1 – 15 = +1.
14.	The term *polling* means to ask. This means reading the value in a register at regular intervals. An alternative to *polling* is to use *interrupts*.