

- **High-Performance Static CMOS Technology**
 - 33-ns Instruction Cycle Time (30 MHz)
 - 30-MIPS Performance
 - Low-Power 3.3-V Design
- **Based on TMS320C2xx DSP CPU Core**
 - Code-Compatible With F243/F241/C242
 - Instruction Set and Module Compatible With F240/C240
- **On-Chip Memory**
 - Up to 32K Words x 16 Bits of Flash EEPROM (4 Sectors)
 - Up to 2.5K Words x 16 Bits of Data/Program RAM
 - 544 Words of Dual-Access RAM
 - Up to 2K Words of Single-Access RAM
- **Boot ROM**
 - SCI/SPI Bootloader
- **Two Event-Manager (EV) Modules (EVA and EVB), Each Include:**
 - Two 16-Bit General-Purpose Timers
 - Eight 16-Bit Pulse-Width Modulation (PWM) Channels Which Enable:
 - Three-Phase Inverter Control
 - Center- or Edge-Alignment of PWM Channels
 - Emergency PWM Channel Shutdown With External PDPINTx Pin
 - Programmable Deadband (Deadtime) Prevents Shoot-Through Faults
 - Three Capture Units For Time-Stamping of External Events
 - On-Chip Position Encoder Interface Circuitry
 - Synchronized Analog-to-Digital Conversion
 - Designed for AC Induction, BLDC, Switched Reluctance, and Stepper Motor Control
 - Applicable for Multiple Motor and/or Converter Control
- **External Memory Interface (LF2407)**
 - 192K Words x 16 Bits of Total Memory: 64K Program, 64K Data, 64K I/O
- **Watchdog (WD) Timer Module**
- **10-Bit Analog-to-Digital Converter (ADC)**
 - 8 or 16 Multiplexed Input Channels
 - 500 ns Minimum Conversion Time
 - Selectable Twin 8-Input Sequencers Triggered by Two Event Managers
- **Controller Area Network (CAN) 2.0B Module**
- **Serial Communications Interface (SCI)**
- **16-Bit Serial Peripheral Interface (SPI) Module**
- **Phase-Locked-Loop (PLL)-Based Clock Generation**
- **Up to 40 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins**
- **Up to Five External Interrupts (Power Drive Protection, Reset, and Two Maskable Interrupts)**
- **Power Management:**
 - Three Power-Down Modes
 - Ability to Power Down Each Peripheral Independently
- **Real-Time JTAG-Compliant Scan-Based Emulation, IEEE Standard 1149.1† (JTAG)**
- **Development Tools Include:**
 - Texas Instruments (TI) ANSI C Compiler, Assembler/Linker, and Code Composer Studio™ Debugger
 - Evaluation Modules
 - Scan-Based Self-Emulation (XDS510™)
 - Broad Third-Party Digital Motor Control Support
- **Package Options**
 - 144-Pin Low-Profile Quad Flatpack (LQFP) PGE (LF2407)
 - 100-Pin LQFP PZ (LF2406)
 - 64-Pin Quad Flatpack (QFP) PG (LF2402)
- **Extended Temperature Options (A and S)**
 - A: – 40°C to 85°C
 - S: – 40°C to 125°C



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Code Composer Studio and XDS510 are trademarks of Texas Instruments.

Other trademarks are the property of their respective owners.

† IEEE Standard 1149.1–1990, IEEE Standard Test-Access Port

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TMS320LF2407, TMS320LF2406, TMS320LF2402

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REVISION HISTORY

| REVISION | DATE | PRODUCT STATUS | HIGHLIGHTS |
|----------|--------------|-----------------|---|
| F | January 2001 | Production Data | <p>The description for the V_{CCP} pin has been modified. This information can be found in Table 2, LF240x Pin List and Package Options.</p> <p>The conditions for high-impedance state for the strobe signals have been changed. This information can be found in Table 2, LF240x Pin List and Package Options.</p> <p>The t_{h(A)COLW} parameter is now referenced from the next falling CLKOUT edge than what was shown in the previous data sheets. The specification for this parameter is –5 ns (MIN).</p> <p>Ready-on-Read and Ready-on-Write timings for one software wait state and one external wait state have been added.</p> <p>Bits 15 and 8 of the SCSR1 register are now reserved (see Table 19, LF240x DSP Peripheral Register Description).</p> |
| G | August 2001 | Production Data | <p>Updated description of TMS2 in Table 2.</p> <p>Updated Figure 6, Event Manager A Block Diagram. TCLKINx is now routed through the prescaler.</p> <p>Updated the ADC module list of functions in the Enhanced Analog-to-Digital Converter (ADC) Module section (p.38).</p> <p>The I/O buffers used in 240x/240xA are not 5-V compatible.</p> <p>Updated the f_{CLKOUT} parameter in the Recommended Operating Conditions table (p.61).</p> <p>Updated the t_{c(AD)} and t_{w(SHC)} parameters in the Internal ADC Module Timings table of the 10-Bit Analog-to-Digital Converter (ADC) section (p.96).</p> <p>Updated PDDATDIR register (0x0709E) in Table 19, LF240x DSP Peripheral Register Description.</p> |



description

The TMS320LF240x devices, new members of the TMS320C24x™ generation of digital signal processor (DSP) controllers, are part of the TMS320C2000™ platform of fixed-point DSPs. The 240x† devices offer the enhanced TMS320™ DSP architectural design of the C2xx core CPU for low-cost, low-power, and high-performance processing capabilities. Several advanced peripherals, optimized for digital motor and motion control applications, have been integrated to provide a true single-chip DSP controller. While code-compatible with the existing C24x™ DSP controller devices, the 240x offers increased processing performance (30 MIPS) and a higher level of peripheral integration. See the TMS320x240x Device Summary section for device-specific features.

The 240x generation offers an array of memory sizes and different peripherals tailored to meet the specific price/performance points required by various applications. Flash devices of up to 32K words offer a cost-effective reprogrammable solution for volume production. Note that Flash-based devices contain a 256-word boot ROM to facilitate in-circuit programming. The 240x family also includes ROM devices that are fully pin-to-pin compatible with their Flash counterparts. (The ROM devices are described in the SPRS145 data sheet.)

All 240x devices offer at least one event manager module which has been optimized for digital motor control and power conversion applications. Capabilities of this module include center- and/or edge-aligned PWM generation, programmable deadband to prevent shoot-through faults, and synchronized analog-to-digital conversion. Devices with dual event managers enable multiple motor and/or converter control with a single 240x DSP controller.

The high-performance, 10-bit analog-to-digital converter (ADC) has a minimum conversion time of 500 ns and offers up to 16 channels of analog input. The autosequencing capability of the ADC allows a maximum of 16 conversions to take place in a single conversion session without any CPU overhead.

A serial communications interface (SCI) is integrated on all devices to provide asynchronous communication to other devices in the system. For systems requiring additional communication interfaces, the 2407 and 2406 offer a 16-bit synchronous serial peripheral interface (SPI). The 2407 and 2406 also offer a controller area network (CAN) communications module that meets 2.0B specifications. To maximize device flexibility, functional pins are also configurable as general-purpose inputs/outputs (GPIOs).

To streamline development time, JTAG-compliant scan-based emulation has been integrated into all devices. This provides non-intrusive real-time capabilities required to debug digital control systems. A complete suite of code-generation tools from C compilers to the industry-standard Code Composer Studio™ debugger supports this family. Numerous third-party developers not only offer device-level development tools, but also system-level design and development support.

TMS320C24x, TMS320C2000, TMS320, and C24x are trademarks of Texas Instruments.

† Throughout this data sheet, 240x is used as a generic name for LF240x devices.

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TMS320x240x device summary

Note that throughout this data sheet, 240x is used as a generic name for the LF240x devices.

Table 1. Hardware Features of 240x Devices

| FEATURE | | LF2402 | LF2406 | LF2407 |
|---|---------------------------|-----------|------------|-------------|
| C2xx DSP Core | | Yes | Yes | Yes |
| Instruction Cycle | | 33 ns | 33 ns | 33 ns |
| MIPS (30 MHz) | | 30 MIPS | 30 MIPS | 30 MIPS |
| RAM (16-bit word) | Dual-Access RAM (DARAM) | 544 | 544 | 544 |
| | Single-Access RAM (SARAM) | 512 | 2K | 2K |
| On-chip Flash (16-bit word) (4 sectors: 4K, 12K, 12K, 4K) | | 8K | 32K | 32K |
| Boot ROM (16-bit word) | | Yes | Yes | Yes |
| External Memory Interface | | — | — | Yes |
| Event Managers A and B (EVA and EVB) | | EVA | EVA, EVB | EVA, EVB |
| • General-Purpose (GP) Timers | | 2 | 4 | 4 |
| • Compare (CMP)/PWM | | 6/8 | 12/16 | 12/16 |
| • Capture (CAP)/QEP | | 3/2 | 6/4 | 6/4 |
| Watchdog Timer | | Yes | Yes | Yes |
| 10-Bit ADC | | Yes | Yes | Yes |
| • Channels | | 8 | 16 | 16 |
| • Conversion Time (minimum) | | 500 ns | 500 ns | 500 ns |
| SPI | | — | Yes | Yes |
| SCI | | Yes | Yes | Yes |
| CAN | | — | Yes | Yes |
| Digital I/O Pins (Shared) | | 21 | 41 | 41 |
| External Interrupts | | 3 | 5 | 5 |
| Supply Voltage | | 3.3 V | 3.3 V | 3.3 V |
| Packaging | | 64-pin PG | 100-pin PZ | 144-pin PGE |

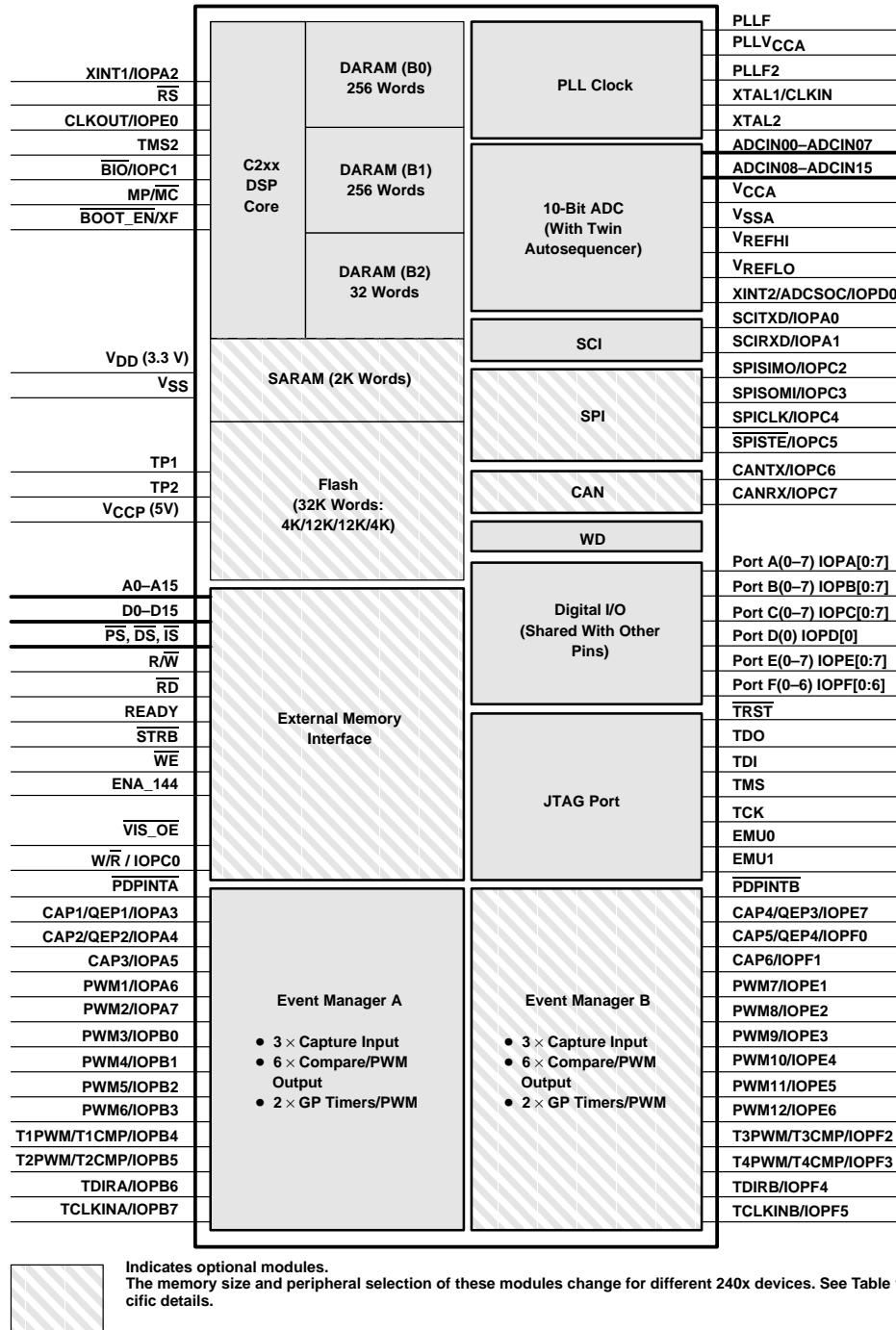
NOTE: ROM-equivalent LC240xA devices are described in SPRS145.



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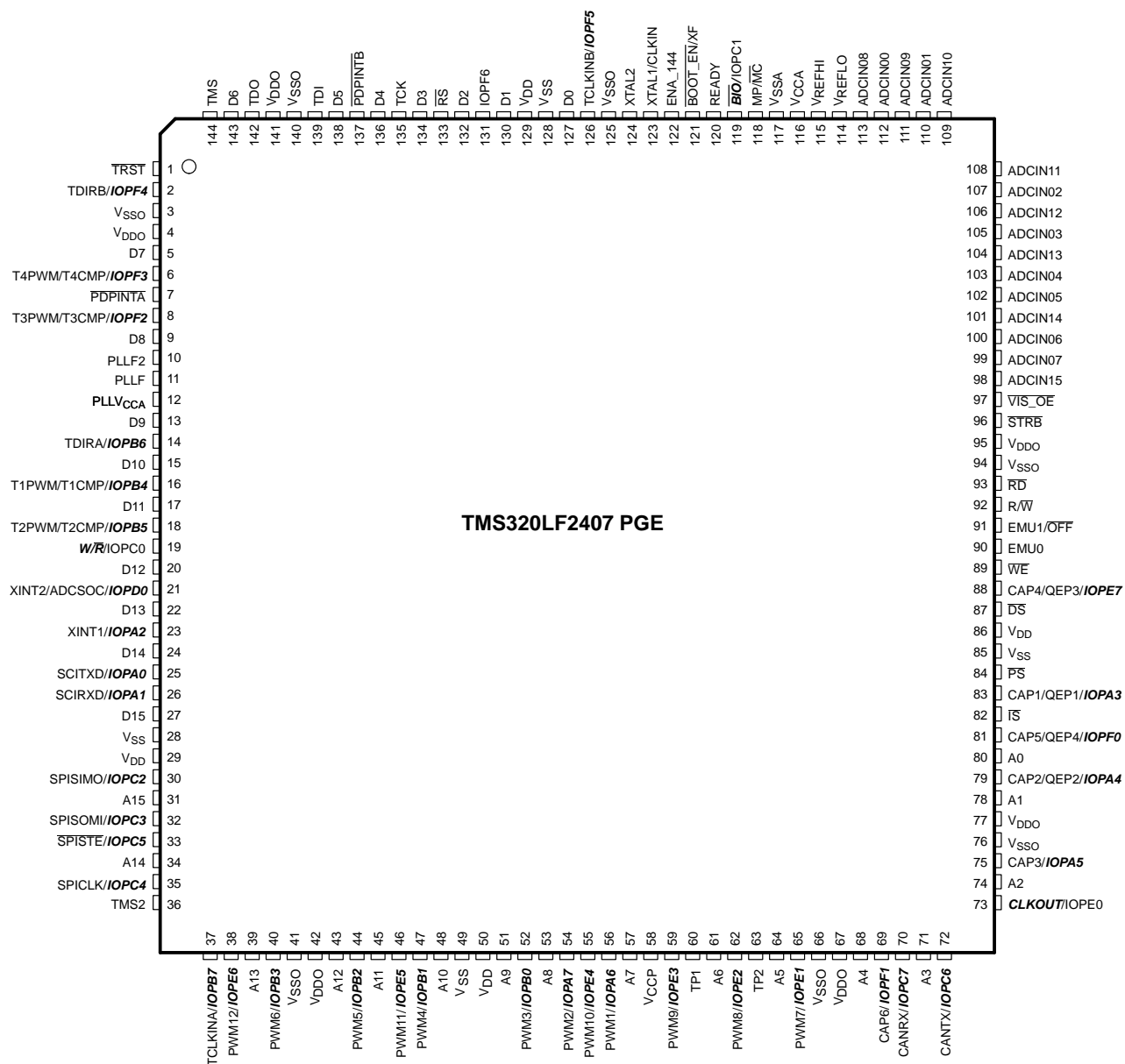
functional block diagram of the 2407 DSP controller



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PGE PACKAGE† (TOP VIEW)

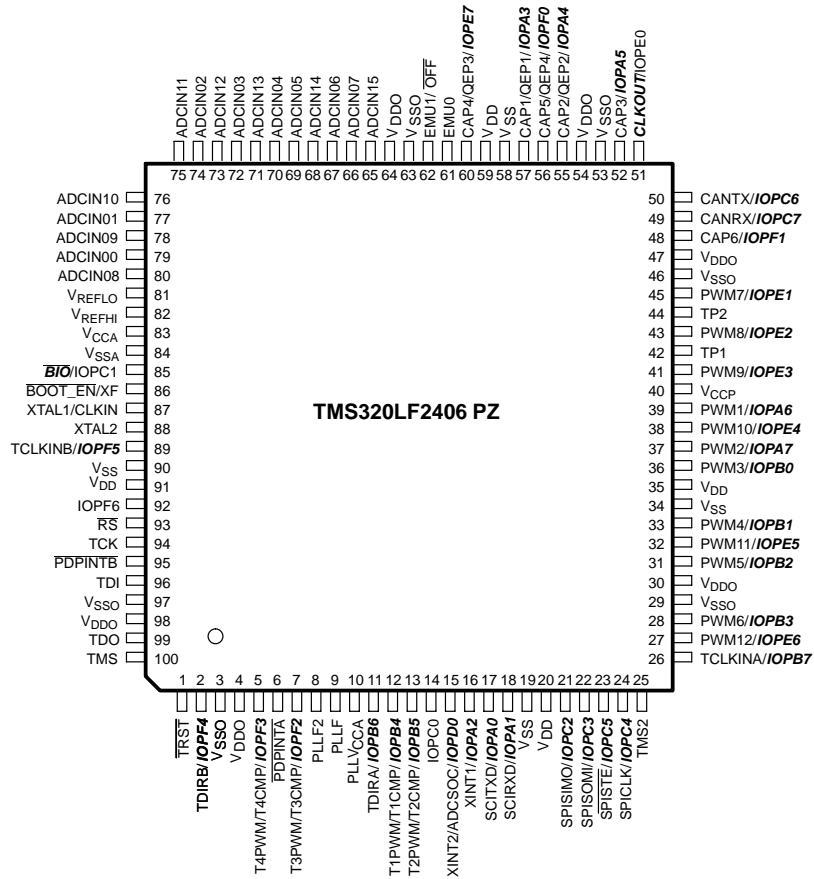


† **Bold, italicized pin names** indicate pin function after reset.

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PZ PACKAGE† (TOP VIEW)

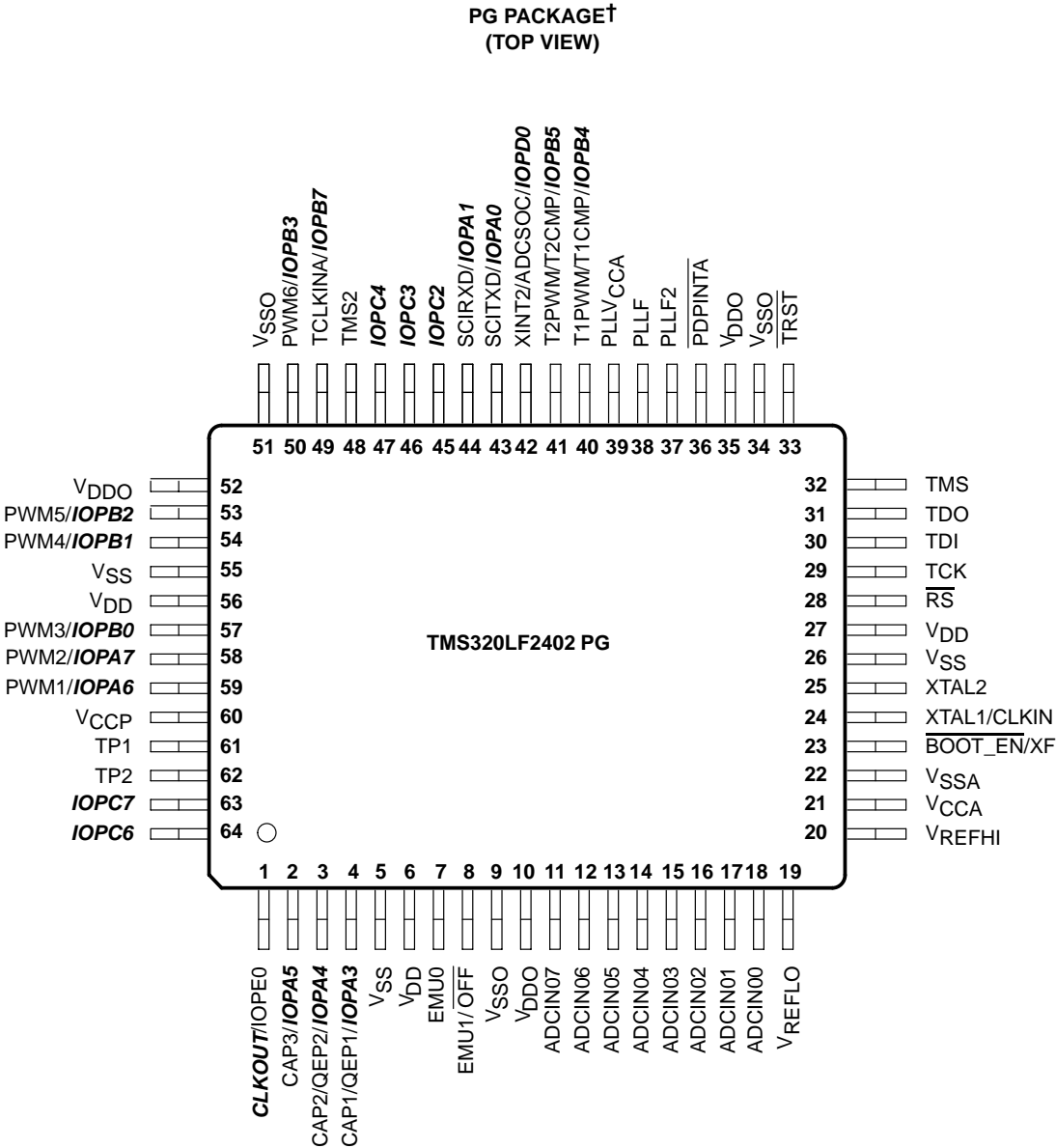


† **Bold, italicized pin names** indicate pin function after reset.



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† **Bold, italicized pin names** indicate pin function after reset.

pin functions

The TMS320LF2407 device is the superset of all the 240x devices. All signals are available on the 2407 device. Table 2 lists the signals available in the 240x generation of devices.

Table 2. LF240x Pin List and Package Options†‡

| PIN NAME | LF2407 | LF2406 | LF2402 | DESCRIPTION |
|----------------------------------|--------|--------|--------|--|
| EVENT MANAGER A (EVA) | | | | |
| CAP1/QEP1/ <i>IOPA3</i> | 83 | 57 | 4 | Capture input #1/quadrature encoder pulse input #1 (EVA) or GPIO (↑) |
| CAP2/QEP2/ <i>IOPA4</i> | 79 | 55 | 3 | Capture input #2/quadrature encoder pulse input #2 (EVA) or GPIO (↑) |
| CAP3/ <i>IOPA5</i> | 75 | 52 | 2 | Capture input #3 (EVA) or GPIO (↑) |
| PWM1/ <i>IOPA6</i> | 56 | 39 | 59 | Compare/PWM output pin #1 (EVA) or GPIO (↑) |
| PWM2/ <i>IOPA7</i> | 54 | 37 | 58 | Compare/PWM output pin #2 (EVA) or GPIO (↑) |
| PWM3/ <i>IOPB0</i> | 52 | 36 | 57 | Compare/PWM output pin #3 (EVA) or GPIO (↑) |
| PWM4/ <i>IOPB1</i> | 47 | 33 | 54 | Compare/PWM output pin #4 (EVA) or GPIO (↑) |
| PWM5/ <i>IOPB2</i> | 44 | 31 | 53 | Compare/PWM output pin #5 (EVA) or GPIO (↑) |
| PWM6/ <i>IOPB3</i> | 40 | 28 | 50 | Compare/PWM output pin #6 (EVA) or GPIO (↑) |
| T1PWM/T1CMP/ <i>IOPB4</i> | 16 | 12 | 40 | Timer 1 compare output (EVA) or GPIO (↑) |
| T2PWM/T2CMP/ <i>IOPB5</i> | 18 | 13 | 41 | Timer 2 compare output (EVA) or GPIO (↑) |
| TDIRA/ <i>IOPB6</i> | 14 | 11 | | Counting direction for general-purpose (GP) timer (EVA) or GPIO. If TDIRA = 1, upward counting is selected. If TDIRA = 0, downward counting is selected. (↑) |
| TCLKINA/ <i>IOPB7</i> | 37 | 26 | 49 | External clock input for GP timer (EVA) or GPIO. Note that the timer can also use the internal device clock. (↑) |
| EVENT MANAGER B (EVB) | | | | |
| CAP4/QEP3/ <i>IOPE7</i> | 88 | 60 | | Capture input #4/quadrature encoder pulse input #3 (EVB) or GPIO (↑) |
| CAP5/QEP4/ <i>IOPE0</i> | 81 | 56 | | Capture input #5/quadrature encoder pulse input #4 (EVB) or GPIO (↑) |
| CAP6/ <i>IOPE1</i> | 69 | 48 | | Capture input #6 (EVB) or GPIO (↑) |
| PWM7/ <i>IOPE1</i> | 65 | 45 | | Compare/PWM output pin #7 (EVB) or GPIO (↑) |
| PWM8/ <i>IOPE2</i> | 62 | 43 | | Compare/PWM output pin #8 (EVB) or GPIO (↑) |
| PWM9/ <i>IOPE3</i> | 59 | 41 | | Compare/PWM output pin #9 (EVB) or GPIO (↑) |
| PWM10/ <i>IOPE4</i> | 55 | 38 | | Compare/PWM output pin #10 (EVB) or GPIO (↑) |
| PWM11/ <i>IOPE5</i> | 46 | 32 | | Compare/PWM output pin #11 (EVB) or GPIO (↑) |
| PWM12/ <i>IOPE6</i> | 38 | 27 | | Compare/PWM output pin #12 (EVB) or GPIO (↑) |
| T3PWM/T3CMP/ <i>IOPE2</i> | 8 | 7 | | Timer 3 compare output (EVB) or GPIO (↑) |
| T4PWM/T4CMP/ <i>IOPE3</i> | 6 | 5 | | Timer 4 compare output (EVB) or GPIO (↑) |
| TDIRB/ <i>IOPE4</i> | 2 | 2 | | Counting direction for general-purpose (GP) timer (EVB) or GPIO. If TDIRB = 1, upward counting is selected. If TDIRB = 0, downward counting is selected. (↑) |
| TCLKINB/ <i>IOPE5</i> | 126 | 89 | | External clock input for GP timer (EVB) or GPIO. Note that the timer can also use the internal device clock. (↑) |

† **Bold, italicized pin names** indicate pin function after reset.

‡ GPIO – General-purpose input/output pin. All GPIOs come up as input after reset.

§ It is highly recommended that V_{CCA} be isolated from the digital supply voltage (and V_{SSA} from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.

¶ Only when all of the following conditions are met: EMU1/̄OFF is low, ̄TRST is low, and EMU0 is high

No power supply pin (V_{DD}, V_{DDO}, V_{SS}, or V_{SSO}) should be left unconnected. All power supply pins must be connected appropriately for proper device operation.

LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is ±16 μA.)

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pin functions (continued)

Table 2. LF240x Pin List and Package Options^{†‡} (Continued)

| PIN NAME | | LF2407 | LF2406 | LF2402 | DESCRIPTION |
|---|---------|--------|--------|--------|--|
| ANALOG-TO-DIGITAL CONVERTER (ADC) | | | | | |
| ADCIN00 | | 112 | 79 | 18 | Analog input #0 to the ADC |
| ADCIN01 | | 110 | 77 | 17 | Analog input #1 to the ADC |
| ADCIN02 | | 107 | 74 | 16 | Analog input #2 to the ADC |
| ADCIN03 | | 105 | 72 | 15 | Analog input #3 to the ADC |
| ADCIN04 | | 103 | 70 | 14 | Analog input #4 to the ADC |
| ADCIN05 | | 102 | 69 | 13 | Analog input #5 to the ADC |
| ADCIN06 | | 100 | 67 | 12 | Analog input #6 to the ADC |
| ADCIN07 | | 99 | 66 | 11 | Analog input #7 to the ADC |
| ADCIN08 | | 113 | 80 | | Analog input #8 to the ADC |
| ADCIN09 | | 111 | 78 | | Analog input #9 to the ADC |
| ADCIN10 | | 109 | 76 | | Analog input #10 to the ADC |
| ADCIN11 | | 108 | 75 | | Analog input #11 to the ADC |
| ADCIN12 | | 106 | 73 | | Analog input #12 to the ADC |
| ADCIN13 | | 104 | 71 | | Analog input #13 to the ADC |
| ADCIN14 | | 101 | 68 | | Analog input #14 to the ADC |
| ADCIN15 | | 98 | 65 | | Analog input #15 to the ADC |
| VREFHI | | 115 | 82 | 20 | ADC analog high-voltage reference input |
| VREFLO | | 114 | 81 | 19 | ADC analog low-voltage reference input |
| VCCA | | 116 | 83 | 21 | Analog supply voltage for ADC (3.3 V)§ |
| VSSA | | 117 | 84 | 22 | Analog ground reference for ADC |
| CONTROLLER AREA NETWORK (CAN), SERIAL COMMUNICATIONS INTERFACE (SCI), SERIAL PERIPHERAL INTERFACE (SPI) | | | | | |
| CANRX/ <i>IOPC7</i> | CANRX | 70 | 49 | – | CAN receive data or GPIO (↑) |
| | IOPC7 | 70 | 49 | 63 | |
| CANTX/ <i>IOPC6</i> | CANTX | 72 | 50 | – | CAN transmit data or GPIO (↑) |
| | IOPC6 | 72 | 50 | 64 | |
| SCITXD/ <i>IOPA0</i> | | 25 | 17 | 43 | SCI asynchronous serial port transmit data or GPIO (↑) |
| SCIRXD/ <i>IOPA1</i> | | 26 | 18 | 44 | SCI asynchronous serial port receive data or or GPIO (↑) |
| SPICLK/ <i>IOPC4</i> | SPICLK | 35 | 24 | – | SPI clock or GPIO (↑) |
| | IOPC4 | 35 | 24 | 47 | |
| SPISIMO/ <i>IOPC2</i> | SPISIMO | 30 | 21 | – | SPI slave in, master out or GPIO (↑) |
| | IOPC2 | 30 | 21 | 45 | |
| SPISOMI/ <i>IOPC3</i> | SPISOMI | 32 | 22 | – | SPI slave out, master in or GPIO (↑) |
| | IOPC3 | 32 | 22 | 46 | |
| SPISTE/ <i>IOPC5</i> | SPISTE | 33 | 23 | – | SPI slave transmit-enable (optional) or GPIO (↑) |
| | IOPC5 | 33 | 23 | – | |

[†] **Bold, italicized pin names** indicate pin function after reset.

[‡] GPIO – General-purpose input/output pin. All GPIOs come up as input after reset.

[§] It is highly recommended that VCCA be isolated from the digital supply voltage (and VSSA from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.

[¶] Only when all of the following conditions are met: EMU1/OFF is low, TRST is low, and EMU0 is high

[#] No power supply pin (VDD, VDDO, VSS, or VSSO) should be left unconnected. All power supply pins must be connected appropriately for proper device operation.

LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is ±16 μA.)



pin functions (continued)

Table 2. LF240x Pin List and Package Options^{†‡} (Continued)

| PIN NAME | LF2407 | LF2406 | LF2402 | DESCRIPTION |
|--|-----------------------|--------|--------|---|
| EXTERNAL INTERRUPTS, CLOCK | | | | |
| <u>RS</u> | 133 | 93 | 28 | Device reset. <u>RS</u> causes the 240x to terminate execution and sets PC = 0. When <u>RS</u> is brought to a high level, execution begins at location zero of program memory. <u>RS</u> affects (or sets to zero) various registers and status bits. When the watchdog timer overflows, it initiates a system reset pulse that is reflected on the <u>RS</u> pin. (↑) |
| <u>PDPINTA</u> | 7 | 6 | 36 | Power drive protection interrupt input. This interrupt, when activated, puts the PWM output pins (EVA) in the high-impedance state should motor drive/power converter abnormalities, such as overvoltage or overcurrent, etc., arise. <u>PDPINTA</u> is a falling-edge-sensitive interrupt. (↑) |
| XINT1/<i>IOPA2</i> | 23 | 16 | | External user interrupt 1 or GPIO. Both XINT1 and XINT2 are edge-sensitive. The edge polarity is programmable. (↑) |
| XINT2/ADCSOC/<i>IOPD0</i> | 21 | 15 | 42 | External user interrupt 2 and ADC start of conversion or GPIO. External "start-of-conversion" input for ADC/GPIO. Both XINT1 and XINT2 are edge-sensitive. The edge polarity is programmable. (↑) |
| <i>CLKOUT</i>/IOPE0 | 73 | 51 | 1 | Clock output or GPIO. This pin outputs either the CPU clock (CLKOUT) or the watchdog clock (WDCLK). The selection is made by the CLKSRC bit (bit 14) of the System Control and Status Register (SCSR). This pin can be used as a GPIO if not used as a clock output pin. (↑) |
| <u>PDPINTB</u> | 137 | 95 | | Power drive protection interrupt input. This interrupt, when activated, puts the PWM output pins (EVB) in the high-impedance state should motor drive/power converter abnormalities, such as overvoltage or overcurrent, etc., arise. <u>PDPINTB</u> is a falling-edge-sensitive interrupt. (↑) |
| OSCILLATOR, PLL, FLASH, BOOT, AND MISCELLANEOUS | | | | |
| XTAL1/CLKIN | 123 | 87 | 24 | PLL oscillator input pin. Crystal input to PLL/clock source input to PLL. XTAL1/CLKIN is tied to one side of a reference crystal. |
| XTAL2 | 124 | 88 | 25 | Crystal output. PLL oscillator output pin. XTAL2 is tied to one side of a reference crystal. This pin goes in the high-impedance state when EMU1/ <u>OFF</u> is active low. |
| PLLVCCA | 12 | 10 | 39 | PLL supply (3.3 V) |
| IOPF6 | 131 | 92 | | General-purpose I/O (↑) |
| <u>BOOT_EN</u> / XF | <u>BOOT_EN</u> | 121 | 86 | Boot ROM enable, GPO, XF. This pin will be sampled as input (<u>BOOT_EN</u>) to update SCSR2.3 (<u>BOOT_EN</u> bit) during reset and then driven as an output signal for XF. After reset, XF is driven high. The <u>BOOT_EN</u> pin must be driven with a passive circuit only. (↑) |
| | XF | 121 | 86 | |

[†] **Bold, italicized pin names** indicate pin function after reset.

[‡] GPIO – General-purpose input/output pin. All GPIOs come up as input after reset.

[§] It is highly recommended that VCCA be isolated from the digital supply voltage (and VSSA from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.

[¶] Only when all of the following conditions are met: EMU1/OFF is low, TRST is low, and EMU0 is high

[#] No power supply pin (VDD, VDDO, VSS, or VSSO) should be left unconnected. All power supply pins must be connected appropriately for proper device operation.

LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is ±16 µA.)

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pin functions (continued)

Table 2. LF240x Pin List and Package Options†‡ (Continued)

| PIN NAME | LF2407 | LF2406 | LF2402 | DESCRIPTION |
|--|--------|--------|--------|--|
| OSCILLATOR, PLL, FLASH, BOOT, AND MISCELLANEOUS (CONTINUED) | | | | |
| PLL1F | 11 | 9 | 38 | Filter input 1 |
| PLL1F2 | 10 | 8 | 37 | Filter input 2 |
| V _{CCP} (5V) | 58 | 40 | 60 | Flash programming voltage pin. This pin must be connected to a 5-V supply for Flash programming. The Flash cannot be programmed if this pin is connected to GND. When not programming the Flash (i.e., during normal device operation), this pin can either be left connected to the 5-V supply or it can be tied to GND. This pin must not be left floating at any time. Do not use any current-limiting resistor in series with the 5-V supply on this pin. This pin is a “no connect” (NC) on ROM parts and can be left open. |
| TP1 (Flash) | 60 | 42 | 61 | Flash array test pin. <i>Do not connect.</i> |
| TP2 (Flash) | 63 | 44 | 62 | Flash array test pin. <i>Do not connect.</i> |
| BIO /IOPC1 | 119 | 85 | | Branch control input. BIO is polled by the BCND pma, BIO instruction. If BIO is low, a branch is executed. If BIO is not used, it should be pulled high. This pin is configured as a branch control input by all device resets. It can be used as a GPIO, if not used as a branch control input. (↑) |
| EMULATION AND TEST | | | | |
| EMU0 | 90 | 61 | 7 | Emulator I/O #0 with internal pullup. When TRST is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. (↑) |
| EMU1/ OFF | 91 | 62 | 8 | Emulator pin 1. Emulator pin 1 disables all outputs. When TRST is driven high, EMU1/ OFF is used as an interrupt to or from the emulator system and is defined as an input/output through the JTAG scan. When TRST is driven low, this pin is configured as OFF . EMU1/ OFF , when active low, puts all output drivers in the high-impedance state. Note that OFF is used exclusively for testing and emulation purposes (not for multiprocessing applications). Therefore, for the OFF condition, the following apply: TRST = 0 EMU0 = 1 EMU1/OFF = 0 (↑) |
| TCK | 135 | 94 | 29 | JTAG test clock with internal pullup (↑) |
| TDI | 139 | 96 | 30 | JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (↑) |
| TDO | 142 | 99 | 31 | JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. (↓) |
| TMS | 144 | 100 | 32 | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (↑) |
| TMS2 | 36 | 25 | 48 | JTAG test-mode select 2 (TMS2) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. Used for test and emulation only. This pin can be left unconnected in user applications. If the PLL bypass mode is desired, TMS2, TMS, and TRST should be held low during reset. (↑) |

† **Bold, italicized pin names** indicate pin function after reset.

‡ GPIO – General-purpose input/output pin. All GPIOs come up as input after reset.

§ It is highly recommended that V_{CCA} be isolated from the digital supply voltage (and V_{SSA} from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.

¶ Only when all of the following conditions are met: EMU1/**OFF** is low, **TRST** is low, and EMU0 is high

No power supply pin (V_{DD}, V_{DDO}, V_{SS}, or V_{SSO}) should be left unconnected. All power supply pins must be connected appropriately for proper device operation.

LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is ±16 µA.)



pin functions (continued)

Table 2. LF240x Pin List and Package Options^{†‡} (Continued)

| PIN NAME | LF2407 | LF2406 | LF2402 | DESCRIPTION |
|--|--------------------------------|--------|--------|---|
| EMULATION AND TEST (CONTINUED) | | | | |
| $\overline{\text{TRST}}$ | 1 | 1 | 33 | JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. (↓) |
| ADDRESS, DATA, AND MEMORY CONTROL SIGNALS | | | | |
| $\overline{\text{DS}}$ | 87 | | | Data space strobe. $\overline{\text{IS}}$, $\overline{\text{DS}}$, and $\overline{\text{PS}}$ are always high unless low-level asserted for access to the relevant external memory space or I/O. They are placed in the high-impedance state. [¶] |
| $\overline{\text{IS}}$ | 82 | | | I/O space strobe. $\overline{\text{IS}}$, $\overline{\text{DS}}$, and $\overline{\text{PS}}$ are always high unless low-level asserted for access to the relevant external memory space or I/O. They are placed in the high-impedance state. [¶] |
| $\overline{\text{PS}}$ | 84 | | | Program space strobe. $\overline{\text{IS}}$, $\overline{\text{DS}}$, and $\overline{\text{PS}}$ are always high unless low-level asserted for access to the relevant external memory space or I/O. They are placed in the high-impedance state. [¶] |
| $\text{R}/\overline{\text{W}}$ | 92 | | | Read/write qualifier signal. $\text{R}/\overline{\text{W}}$ indicates transfer direction during communication to an external device. It is normally in read mode (high), unless low level is asserted for performing a write operation. It is placed in the high-impedance state. [¶] |
| $\text{W}/\overline{\text{R}}$ / IOPC0 | $\text{W}/\overline{\text{R}}$ | 19 | | Write/Read qualifier or GPIO. This is an inverted $\text{R}/\overline{\text{W}}$ signal useful for zero-wait-state memory interface. It is normally low, unless a memory write operation is performed. See Table 12, Port C section, for reset note regarding LF2406 and LF2402. (↑) |
| | IOPC0 | 19 | 14 | |
| $\overline{\text{RD}}$ | 93 | | | Read-enable strobe. Read-select indicates an active, external read cycle. $\overline{\text{RD}}$ is active on all external program, data, and I/O reads. $\overline{\text{RD}}$ goes into the high-impedance state. [¶] |
| $\overline{\text{WE}}$ | 89 | | | Write-enable strobe. The falling edge of $\overline{\text{WE}}$ indicates that the device is driving the external data bus (D15–D0). $\overline{\text{WE}}$ is active on all external program, data, and I/O writes. $\overline{\text{WE}}$ goes in the high-impedance state. [¶] |
| $\overline{\text{STRB}}$ | 96 | | | External memory access strobe. $\overline{\text{STRB}}$ is always high unless asserted low to indicate an external bus cycle. $\overline{\text{STRB}}$ is active for all off-chip accesses. It is placed in the high-impedance state. [¶] |
| READY | 120 | | | READY is pulled low to add wait states for external accesses. READY indicates that an external device is prepared for a bus transaction to be completed. If the device is not ready, it pulls the READY pin low. The processor waits one cycle and checks READY again. Note that the processor performs READY-detection if at least one software wait state is programmed. To meet the external READY timings, the wait-state generator control register (WSGR) should be programmed for at least one wait state. (↑) |

[†] **Bold, italicized pin names** indicate pin function after reset.

[‡] GPIO – General-purpose input/output pin. All GPIOs come up as input after reset.

[§] It is highly recommended that V_{CCA} be isolated from the digital supply voltage (and V_{SSA} from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.

[¶] Only when all of the following conditions are met: EMU1/ $\overline{\text{OFF}}$ is low, $\overline{\text{TRST}}$ is low, and EMU0 is high

[#] No power supply pin (V_{DD} , V_{DDO} , V_{SS} , or V_{SSO}) should be left unconnected. All power supply pins must be connected appropriately for proper device operation.

LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is $\pm 16 \mu\text{A}$.)

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DSP CONTROLLERS

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pin functions (continued)

Table 2. LF240x Pin List and Package Options†‡ (Continued)

| PIN NAME | LF2407 | LF2406 | LF2402 | DESCRIPTION |
|--|--------|--------|--------|--|
| ADDRESS, DATA, AND MEMORY CONTROL SIGNALS (CONTINUED) | | | | |
| MP/MC | 118 | | | Microprocessor/Microcomputer mode select. If this pin is low during reset, the device is put in microcomputer mode and program execution begins at 0000h of internal program memory (Flash EEPROM). A high value during reset puts the device in microprocessor mode and program execution begins at 0000h of external program memory. This line sets the MP/MC bit (bit 2 in the SCSR2 register). (↓) |
| ENA_144 | 122 | | | Active high to enable external interface signals. If pulled low, the 2407 behaves like the 2406/2402—i.e., it has no external memory and generates an illegal address if DS is asserted. This pin has an internal pulldown. (↓) |
| VIS_OE | 97 | | | Visibility output enable (active when data bus is output). This pin is active (low) whenever the external data bus is driving as an output during visibility mode. Can be used by external decode logic to prevent data bus contention while running in visibility mode. |
| A0 | 80 | | | Bit 0 of the 16-bit address bus |
| A1 | 78 | | | Bit 1 of the 16-bit address bus |
| A2 | 74 | | | Bit 2 of the 16-bit address bus |
| A3 | 71 | | | Bit 3 of the 16-bit address bus |
| A4 | 68 | | | Bit 4 of the 16-bit address bus |
| A5 | 64 | | | Bit 5 of the 16-bit address bus |
| A6 | 61 | | | Bit 6 of the 16-bit address bus |
| A7 | 57 | | | Bit 7 of the 16-bit address bus |
| A8 | 53 | | | Bit 8 of the 16-bit address bus |
| A9 | 51 | | | Bit 9 of the 16-bit address bus |
| A10 | 48 | | | Bit 10 of the 16-bit address bus |
| A11 | 45 | | | Bit 11 of the 16-bit address bus |
| A12 | 43 | | | Bit 12 of the 16-bit address bus |
| A13 | 39 | | | Bit 13 of the 16-bit address bus |
| A14 | 34 | | | Bit 14 of the 16-bit address bus |
| A15 | 31 | | | Bit 15 of the 16-bit address bus |
| D0 | 127 | | | Bit 0 of 16-bit data bus (↑) |
| D1 | 130 | | | Bit 1 of 16-bit data bus (↑) |
| D2 | 132 | | | Bit 2 of 16-bit data bus (↑) |
| D3 | 134 | | | Bit 3 of 16-bit data bus (↑) |
| D4 | 136 | | | Bit 4 of 16-bit data bus (↑) |
| D5 | 138 | | | Bit 5 of 16-bit data bus (↑) |
| D6 | 143 | | | Bit 6 of 16-bit data bus (↑) |
| D7 | 5 | | | Bit 7 of 16-bit data bus (↑) |
| D8 | 9 | | | Bit 8 of 16-bit data bus (↑) |

† **Bold, italicized pin names** indicate pin function after reset.

‡ GPIO – General-purpose input/output pin. All GPIOs come up as input after reset.

§ It is highly recommended that VCCA be isolated from the digital supply voltage (and VSSA from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.

¶ Only when all of the following conditions are met: EMU1/OFF is low, TRST is low, and EMU0 is high

No power supply pin (VDD, VDDO, VSS, or VSSO) should be left unconnected. All power supply pins must be connected appropriately for proper device operation.

LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is ±16 µA.)



pin functions (continued)

Table 2. LF240x Pin List and Package Options^{†‡} (Continued)

| PIN NAME | LF2407 | LF2406 | LF2402 | DESCRIPTION |
|--|--------|--------|--------|--|
| ADDRESS, DATA, AND MEMORY CONTROL SIGNALS (CONTINUED) | | | | |
| D9 | 13 | | | Bit 9 of 16-bit data bus (↑) |
| D10 | 15 | | | Bit 10 of 16-bit data bus (↑) |
| D11 | 17 | | | Bit 11 of 16-bit data bus (↑) |
| D12 | 20 | | | Bit 12 of 16-bit data bus (↑) |
| D13 | 22 | | | Bit 13 of 16-bit data bus (↑) |
| D14 | 24 | | | Bit 14 of 16-bit data bus (↑) |
| D15 | 27 | | | Bit 15 of 16-bit data bus (↑) |
| POWER SUPPLY | | | | |
| V _{DD} [#] | 29 | 20 | 6 | Core supply +3.3 V. Digital logic supply voltage. |
| | 50 | 35 | 27 | |
| | 86 | 59 | 56 | |
| | 129 | 91 | | |
| V _{DDO} [#] | 4 | 4 | 10 | I/O buffer supply +3.3 V. Digital logic and buffer supply voltage. |
| | 42 | 30 | 35 | |
| | 67 | 47 | 52 | |
| | 77 | 54 | | |
| | 95 | 64 | | |
| V _{SS} [#] | 141 | 98 | | Core ground. Digital logic ground reference. |
| | 28 | 19 | 5 | |
| | 49 | 34 | 26 | |
| | 85 | 58 | 55 | |
| V _{SSO} [#] | 128 | 90 | | I/O buffer ground. Digital logic and buffer ground reference. |
| | 3 | 3 | 9 | |
| | 41 | 29 | 34 | |
| | 66 | 46 | 51 | |
| | 76 | 53 | | |
| | 94 | 63 | | |
| | 125 | 97 | | |
| | 140 | | | |

[†] **Bold, italicized pin names** indicate pin function after reset.

[‡] GPIO – General-purpose input/output pin. All GPIOs come up as input after reset.

[§] It is highly recommended that V_{CCA} be isolated from the digital supply voltage (and V_{SSA} from digital ground) to maintain the specified accuracy and improve the noise immunity of the ADC.

[¶] Only when all of the following conditions are met: EMU1/ $\overline{\text{OFF}}$ is low, $\overline{\text{TRST}}$ is low, and EMU0 is high

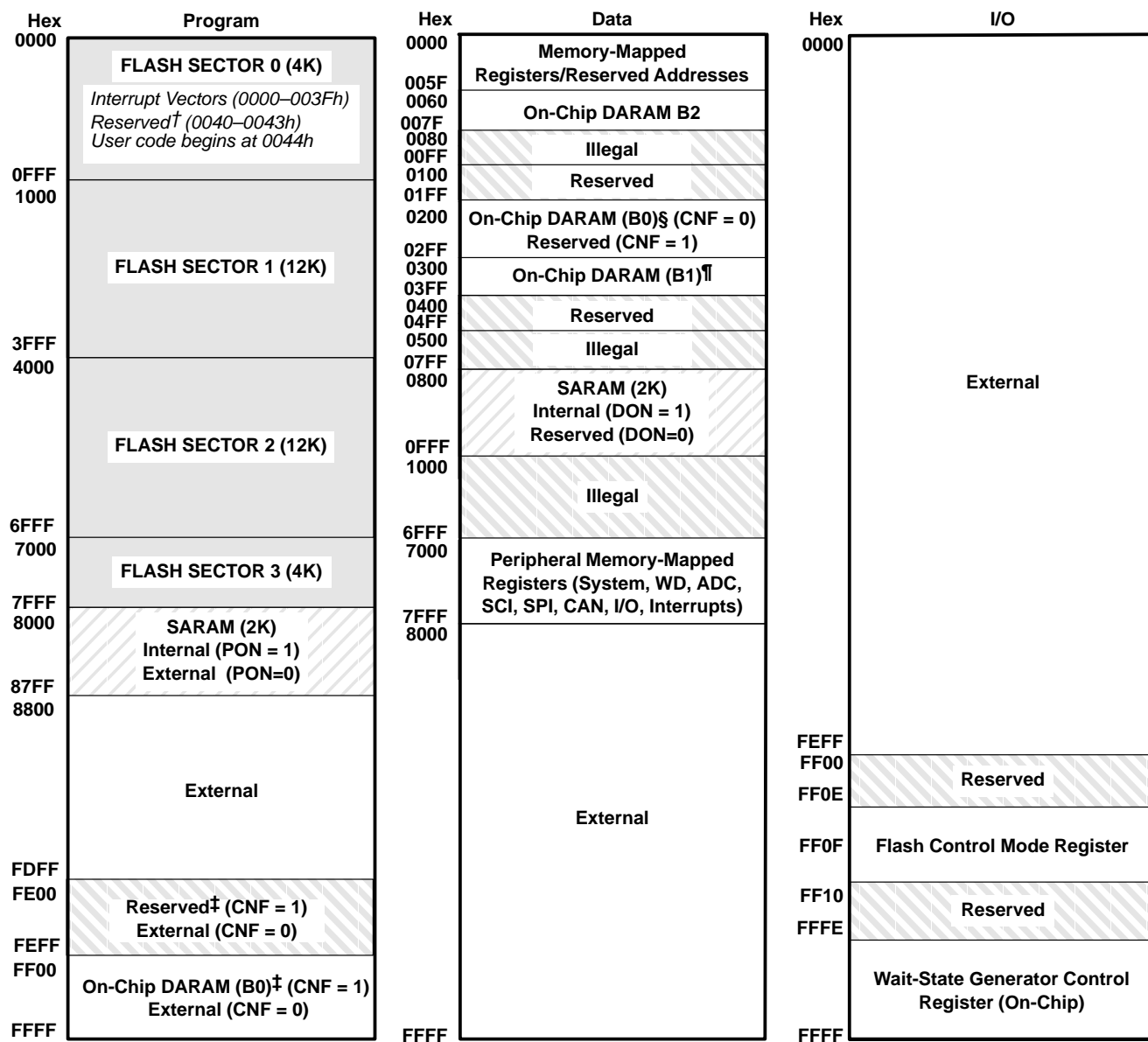
[#] No power supply pin (V_{DD}, V_{DDO}, V_{SS}, or V_{SSO}) should be left unconnected. All power supply pins must be connected appropriately for proper device operation.

LEGEND: ↑ – Internal pullup ↓ – Internal pulldown (Typical active pullup/pulldown value is ±16 μA.)

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memory maps – LF2407



On-Chip Flash Memory (Sectored) – if $\overline{\text{MP}}/\overline{\text{MC}} = 0$
 External Program Memory – if $\overline{\text{MP}}/\overline{\text{MC}} = 1$

SARAM (See Table 1 for details.)

Reserved or Illegal

NOTE A: Boot ROM: If the boot ROM is enabled, then addresses 0000–00FF in the program space will be occupied by boot ROM.

† Addresses 0040h–0043h in on-chip program memory are reserved for future device enhancements.

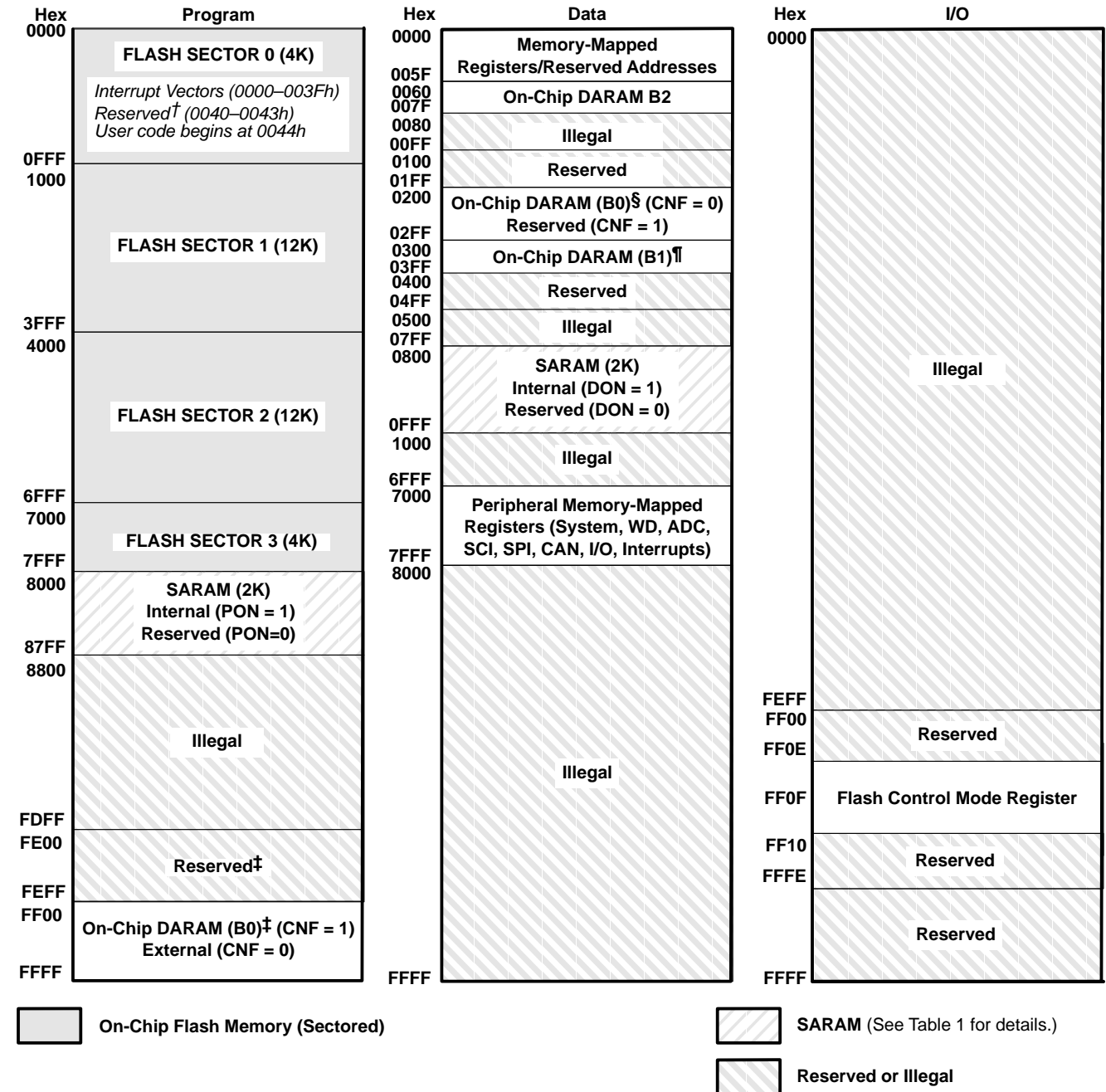
‡ When CNF = 1, addresses FE00h–FEFFh and FF00h–FFFFh are mapped to the same physical block (B0) in program-memory space. For example, a write to FE00h has the same effect as a write to FF00h. For simplicity, addresses FE00h–FEFFh are referred to as reserved when CNF = 1.

§ When CNF = 0, addresses 0100h–01FFh and 0200h–02FFh are mapped to the same physical block (B0) in data-memory space. For example, a write to 0100h has the same effect as a write to 0200h. For simplicity, addresses 0100h–01FFh are referred to as reserved.

† Addresses 0300h–03FFh and 0400h–04FFh are mapped to the same physical block (B1) in data-memory space. For example, a write to 0400h has the same effect as a write to 0300h. For simplicity, addresses 0400h–04FFh are referred to as reserved.

Figure 1. TMS320LF2407 Memory Map

memory maps (continued) – LF2406



NOTE A: Boot ROM: If the boot ROM is enabled, then addresses 0000–00FF in the program space will be occupied by boot ROM.

† Addresses 0040h–0043h in program memory are reserved for future device enhancements.

‡ When CNF = 1, addresses FE00h–FEFFh and FF00h–FFFFh are mapped to the same physical block (B0) in program-memory space. For example, a write to FE00h has the same effect as a write to FF00h. For simplicity, addresses FE00h–FEFFh are referred to as reserved.

§ When CNF = 0, addresses 0100h–01FFh and 0200h–02FFh are mapped to the same physical block (B0) in data-memory space. For example, a write to 0100h has the same effect as a write to 0200h. For simplicity, addresses 0100h–01FFh are referred to as reserved.

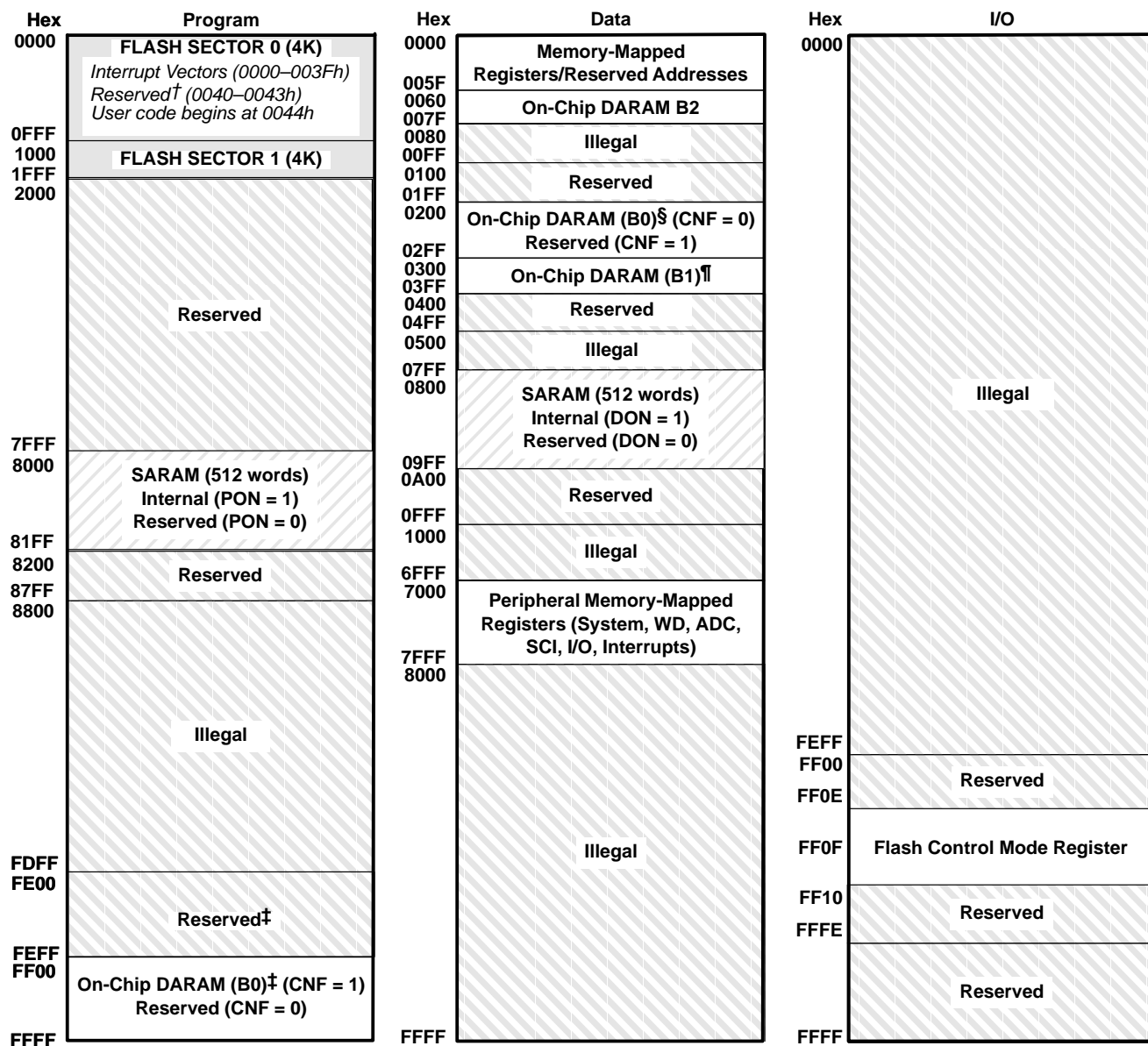
¶ Addresses 0300h–03FFh and 0400h–04FFh are mapped to the same physical block (B1) in data-memory space. For example, a write to 0400h has the same effect as a write to 0300h. For simplicity, addresses 0400h–04FFh are referred to as reserved.

Figure 2. TMS320LF2406 Memory Map

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memory maps (continued) – LF2402



On-Chip Flash Memory (Sectored)

SARAM (See Table 1 for details.)

Reserved or Illegal

NOTE A: Boot ROM: If the boot ROM is enabled, then addresses 0000–00FF in the program space will be occupied by boot ROM.

† Addresses 0040h–0043h in program memory are reserved for future device enhancements.

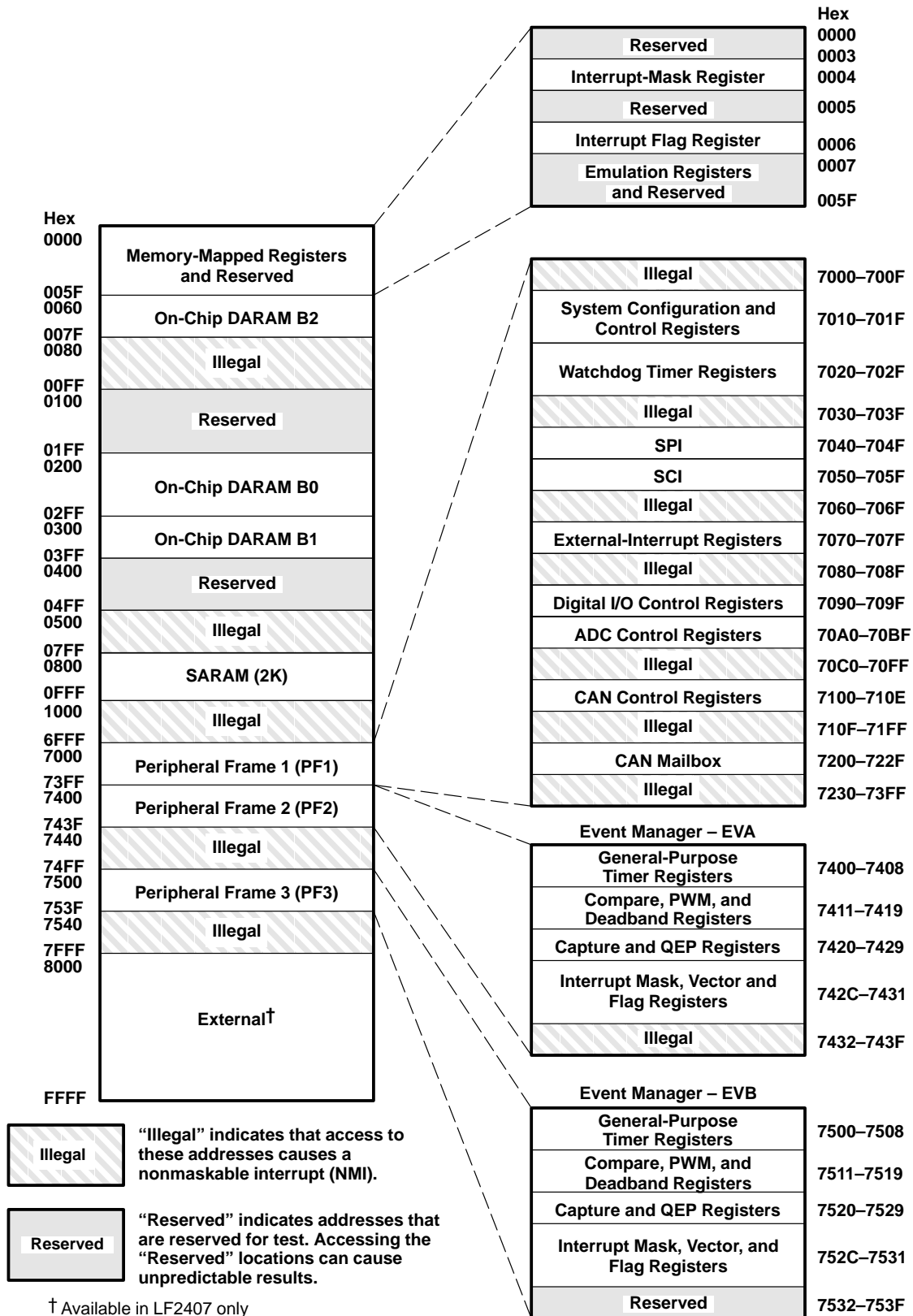
‡ When CNF = 1, addresses FE00h–FEFFh and FF00h–FFFFh are mapped to the same physical block (B0) in program-memory space. For example, a write to FE00h has the same effect as a write to FF00h. For simplicity, addresses FE00h–FEFFh are referred to as reserved.

§ When CNF = 0, addresses 0100h–01FFh and 0200h–02FFh are mapped to the same physical block (B0) in data-memory space. For example, a write to 0100h has the same effect as a write to 0200h. For simplicity, addresses 0100h–01FFh are referred to as reserved.

¶ Addresses 0300h–03FFh and 0400h–04FFh are mapped to the same physical block (B1) in data-memory space. For example, a write to 0400h has the same effect as a write to 0300h. For simplicity, addresses 0400h–04FFh are referred to as reserved.

Figure 3. TMS320LF2402 Memory Map

peripheral memory map of the LF240x



device reset and interrupts

The TMS320x240x software-programmable interrupt structure supports flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The LF240x recognizes three types of interrupt sources.

- **Reset** (hardware- or software-initiated) is unarbitrated by the CPU and takes immediate priority over any other executing functions. All maskable interrupts are disabled until the reset service routine enables them.
The LF240x devices have two sources of reset: an external reset pin and a watchdog timer time-out (reset).
- **Hardware-generated interrupts** are requested by external pins or by on-chip peripherals. There are two types:
 - *External interrupts* are generated by one of four external pins corresponding to the interrupts XINT1, XINT2, PDPINTA, and PDPINTB. These four can be masked both by dedicated enable bits and by the CPU's interrupt mask register (IMR), which can mask each maskable interrupt line at the DSP core.
 - *Peripheral interrupts* are initiated internally by these on-chip peripheral modules: event manager A, event manager B, SPI, SCI, CAN, and ADC. They can be masked both by enable bits for each event in each peripheral and by the CPU's IMR, which can mask each maskable interrupt line at the DSP core.
- **Software-generated interrupts** for the LF240x devices include:
 - *The INTR instruction.* This instruction allows initialization of any LF240x interrupt with software. Its operand indicates the interrupt vector location to which the CPU branches. This instruction globally disables maskable interrupts (sets the INTM bit to 1).
 - *The NMI instruction.* This instruction forces a branch to interrupt vector location 24h. This instruction globally disables maskable interrupts. 240x devices do not have the NMI hardware signal, only software activation is provided.
 - *The TRAP instruction.* This instruction forces the CPU to branch to interrupt vector location 22h. The TRAP instruction does *not* disable maskable interrupts (INTM is not set to 1); therefore, when the CPU branches to the interrupt service routine, that routine can be interrupted by the maskable hardware interrupts.
 - *An emulator trap.* This interrupt can be generated with either an INTR instruction or a TRAP instruction.

Six core interrupts (INT1–INT6) are expanded using a peripheral interrupt expansion (PIE) module identical to the F24x devices. The PIE manages all the peripheral interrupts from the 240x peripherals and are grouped to share the six core level interrupts. Figure 4 shows the PIE block diagram for hardware-generated interrupts.

The PIE block diagram (Figure 4) and the interrupt table (Table 3) explain the grouping and interrupt vector maps. LF240x devices have interrupts identical to those of the F24x devices and should be completely code-compatible. 240x devices also have peripheral interrupts identical to those of the F24x – plus additional interrupts for new peripherals such as event manager B. Though the new interrupts share the 24x interrupt grouping, they all have a unique vector to differentiate among the interrupts. See Table 3 for details.

device reset and interrupts (continued)

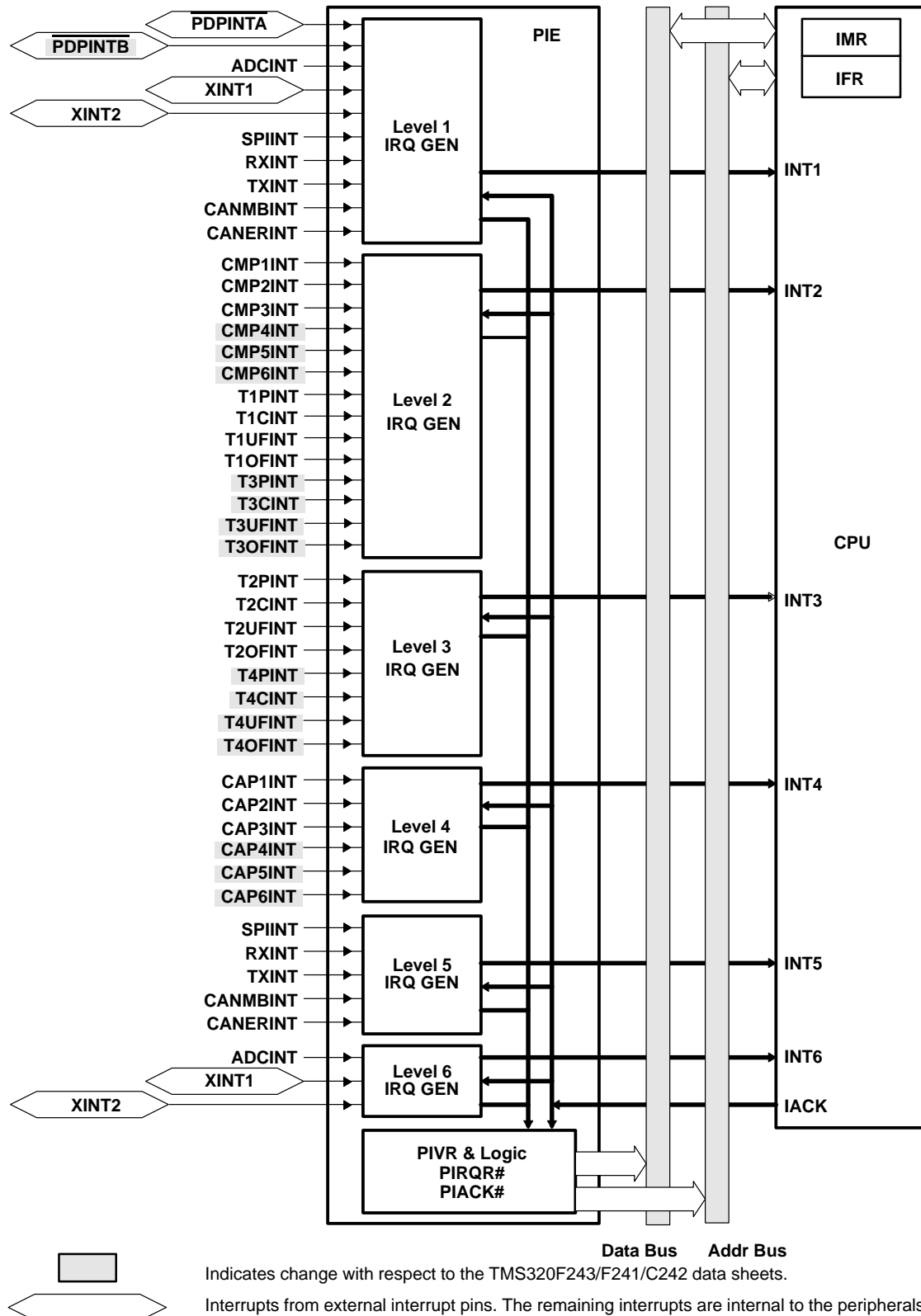


Figure 4. Peripheral Interrupt Expansion (PIE) Module Block Diagram for Hardware-Generated Interrupts

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interrupt request structure

Table 3. LF240x Interrupt Source Priority and Vectors

| INTERRUPT NAME | OVERALL PRIORITY | CPU INTERRUPT AND VECTOR ADDRESS | BIT POSITION IN PIRQRx AND PIACKRx | PERIPHERAL INTERRUPT VECTOR (PIV) | MASK-ABLE? | SOURCE PERIPHERAL MODULE | DESCRIPTION |
|----------------|------------------|----------------------------------|------------------------------------|-----------------------------------|------------|--------------------------------------|---|
| Reset | 1 | RSN 0000h | | N/A | N | $\overline{\text{RS}}$ pin, Watchdog | Reset from pin, watchdog timeout |
| Reserved | 2 | — 0026h | | N/A | N | CPU | Emulator trap |
| NMI | 3 | NMI 0024h | | N/A | N | Nonmaskable Interrupt | Nonmaskable interrupt, software interrupt only |
| PDPINTA | 4 | INT1 0002h | 0.0 | 0020h | Y | EVA | Power device protection interrupt pins |
| PDPINTB | 5 | | 2.0 | 0019h | Y | EVB | |
| ADCINT | 6 | | 0.1 | 0004h | Y | ADC | ADC interrupt in high-priority mode |
| XINT1 | 7 | | 0.2 | 0001h | Y | External Interrupt Logic | External interrupt pins in high priority |
| XINT2 | 8 | | 0.3 | 0011h | Y | External Interrupt Logic | |
| SPIINT | 9 | | 0.4 | 0005h | Y | SPI | SPI interrupt pins in high priority |
| RXINT | 10 | | 0.5 | 0006h | Y | SCI | SCI receiver interrupt in high-priority mode |
| TXINT | 11 | | 0.6 | 0007h | Y | SCI | SCI transmitter interrupt in high-priority mode |
| CANMBINT | 12 | | 0.7 | 0040 | Y | CAN | CAN mailbox in high-priority mode |
| CANERINT | 13 | | 0.8 | 0041 | Y | CAN | CAN error interrupt in high-priority mode |
| CMP1INT | 14 | INT2 0004h | 0.9 | 0021h | Y | EVA | Compare 1 interrupt |
| CMP2INT | 15 | | 0.10 | 0022h | Y | EVA | Compare 2 interrupt |
| CMP3INT | 16 | | 0.11 | 0023h | Y | EVA | Compare 3 interrupt |
| T1PINT | 17 | | 0.12 | 0027h | Y | EVA | Timer 1 period interrupt |
| T1CINT | 18 | | 0.13 | 0028h | Y | EVA | Timer 1 compare interrupt |
| T1UFINT | 19 | | 0.14 | 0029h | Y | EVA | Timer 1 underflow interrupt |
| T1OFINT | 20 | | 0.15 | 002Ah | Y | EVA | Timer 1 overflow interrupt |
| CMP4INT | 21 | | 2.1 | 0024h | Y | EVB | Compare 4 interrupt |
| CMP5INT | 22 | | 2.2 | 0025h | Y | EVB | Compare 5 interrupt |
| CMP6INT | 23 | | 2.3 | 0026h | Y | EVB | Compare 6 interrupt |
| T3PINT | 24 | | 2.4 | 002Fh | Y | EVB | Timer 3 period interrupt |
| T3CINT | 25 | | 2.5 | 0030h | Y | EVB | Timer 3 compare interrupt |
| T3UFINT | 26 | | 2.6 | 0031h | Y | EVB | Timer 3 underflow interrupt |
| T3OFINT | 27 | | 2.7 | 0032h | Y | EVB | Timer 3 overflow interrupt |

† Refer to the *TMS320LF/LC240x DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357) for more information.
NOTE: Some interrupts may not be available in a particular device due to the absence of a peripheral. See Table 1 for more details.

New peripheral interrupts and vectors with respect to the F243/F241 devices.



interrupt request structure (continued)

Table 3. LF240x Interrupt Source Priority and Vectors (Continued)

| INTERRUPT NAME | OVERALL PRIORITY | CPU INTERRUPT AND VECTOR ADDRESS | BIT POSITION IN PIRQRx AND PIACKRx | PERIPHERAL INTERRUPT VECTOR (PIV) | MASK-ABLE? | SOURCE PERIPHERAL MODULE | DESCRIPTION |
|--------------------------|------------------|----------------------------------|------------------------------------|-----------------------------------|------------|--------------------------|---|
| T2PINT | 28 | INT3 0006h | 1.0 | 002Bh | Y | EVA | Timer 2 period interrupt |
| T2CINT | 29 | | 1.1 | 002Ch | Y | EVA | Timer 2 compare interrupt |
| T2UFINT | 30 | | 1.2 | 002Dh | Y | EVA | Timer 2 underflow interrupt |
| T2OFINT | 31 | | 1.3 | 002Eh | Y | EVA | Timer 2 overflow interrupt |
| T4PINT | 32 | | 2.8 | 0039h | Y | EVB | Timer 4 period interrupt |
| T4CINT | 33 | | 2.9 | 003Ah | Y | EVB | Timer 4 compare interrupt |
| T4UFINT | 34 | | 2.10 | 003Bh | Y | EVB | Timer 4 underflow interrupt |
| T4OFINT | 35 | | 2.11 | 003Ch | Y | EVB | Timer 4 overflow interrupt |
| CAP1INT | 36 | INT4 0008h | 1.4 | 0033h | Y | EVA | Capture 1 interrupt |
| CAP2INT | 37 | | 1.5 | 0034h | Y | EVA | Capture 2 interrupt |
| CAP3INT | 38 | | 1.6 | 0035h | Y | EVA | Capture 3 interrupt |
| CAP4INT | 39 | | 2.12 | 0036h | Y | EVB | Capture 4 interrupt |
| CAP5INT | 40 | | 2.13 | 0037h | Y | EVB | Capture 5 interrupt |
| CAP6INT | 41 | | 2.14 | 0038h | Y | EVB | Capture 6 interrupt |
| SPIINT | 42 | INT5 000Ah | 1.7 | 0005h | Y | SPI | SPI interrupt (low priority) |
| RXINT | 43 | | 1.8 | 0006h | Y | SCI | SCI receiver interrupt (low-priority mode) |
| TXINT | 44 | | 1.9 | 0007h | Y | SCI | SCI transmitter interrupt (low-priority mode) |
| CANMBINT | 45 | | 1.10 | 0040h | Y | CAN | CAN mailbox interrupt (low-priority mode) |
| CANERINT | 46 | | 1.11 | 0041h | Y | CAN | CAN error interrupt (low-priority mode) |
| ADCINT | 47 | INT6 000Ch | 1.12 | 0004h | Y | ADC | ADC interrupt (low priority) |
| XINT1 | 48 | | 1.13 | 0001h | Y | External Interrupt Logic | External interrupt pins (low-priority mode) |
| XINT2 | 49 | | 1.14 | 0011h | Y | External Interrupt Logic | |
| Reserved | | 000Eh | | N/A | Y | CPU | Analysis interrupt |
| TRAP | N/A | 0022h | | N/A | N/A | CPU | TRAP instruction |
| Phantom Interrupt Vector | N/A | N/A | | 0000h | N/A | CPU | Phantom interrupt vector |
| INT8–INT16 | N/A | 0010h–0020h | | N/A | N/A | CPU | Software interrupt vectors† |
| INT20–INT31 | N/A | 00028h–0003Fh | | N/A | N/A | CPU | |

† Refer to the *TMS320LF/LC240x DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357) for more information.
NOTE: Some interrupts may not be available in a particular device due to the absence of a peripheral. See Table 1 for more details.

New peripheral interrupts and vectors with respect to the F243/F241 devices.

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DSP CPU core

The TMS320x240x devices use an advanced Harvard-type architecture that maximizes processing power by maintaining two separate memory bus structures — program and data — for full-speed execution. This multiple bus structure allows data and instructions to be read simultaneously. Instructions support data transfers between program memory and data memory. This architecture permits coefficients that are stored in program memory to be read in RAM, thereby eliminating the need for a separate coefficient ROM. This, coupled with a four-deep pipeline, allows the LF240x devices to execute most instructions in a single cycle. See the functional block diagram of the 240x DSP CPU for more information.

TMS320x240x instruction set

The x240x microprocessor implements a comprehensive instruction set that supports both numeric-intensive signal-processing operations and general-purpose applications, such as multiprocessing and high-speed control.

For maximum throughput, the next instruction is prefetched while the current one is being executed. Because the same data lines are used to communicate to external data, program, or I/O space, the number of cycles an instruction requires to execute varies, depending upon whether the next data operand fetch is from internal or external memory. Highest throughput is achieved by maintaining data memory on chip and using either internal or fast external program memory.

addressing modes

The TMS320x240x instruction set provides four basic memory-addressing modes: direct, indirect, immediate, and register.

In direct addressing, the instruction word contains the lower seven bits of the data memory address. This field is concatenated with the nine bits of the data memory page pointer (DP) to form the 16-bit data memory address. Therefore, in the direct-addressing mode, data memory is paged effectively with a total of 512 pages, with each page containing 128 words.

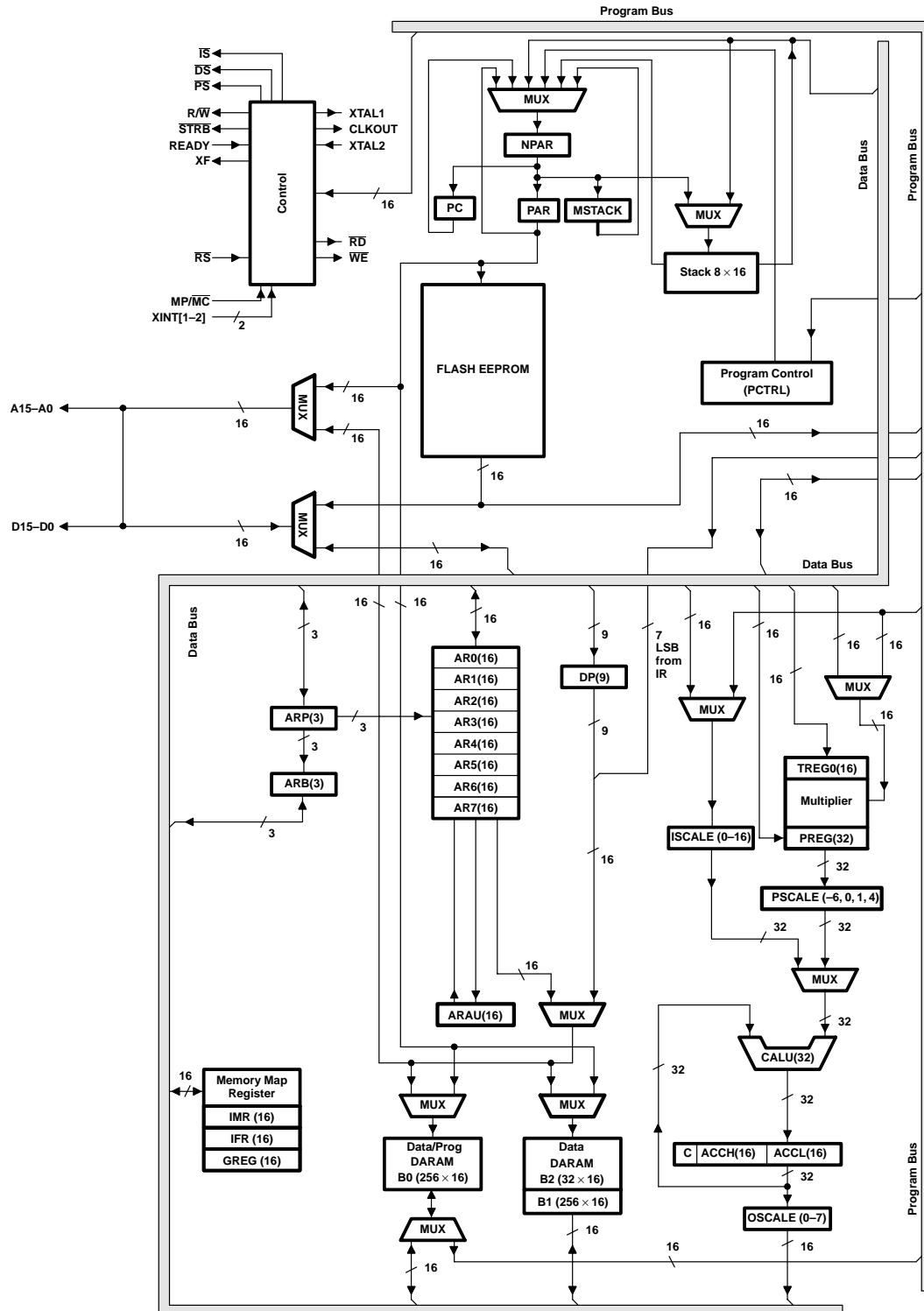
Indirect addressing accesses data memory through the auxiliary registers. In this addressing mode, the address of the instruction operand is contained in the currently selected auxiliary register. Eight auxiliary registers (AR0–AR7) provide flexible and powerful indirect addressing. To select a specific auxiliary register, the auxiliary register pointer (ARP) is loaded with a value from 0 to 7 for AR0 through AR7, respectively.

scan-based emulation

TMS320x2xx devices incorporate scan-based emulation logic for code-development and hardware-development support. Scan-based emulation allows the emulator to control the processor in the system without the use of intrusive cables to the full pinout of the device. The scan-based emulator communicates with the x2xx by way of the IEEE 1149.1-compatible (JTAG) interface. The x240x DSPs do not include boundary scan. The scan chain of these devices is useful for emulation function only.



functional block diagram of the 240x DSP CPU



- NOTES:
- See Table 4 for symbol descriptions.
 - For clarity, the data and program buses are shown as single buses although they include address and data bits.
 - Refer to the *TMS320C240 DSP Controllers CPU, System, and Instruction Set Reference Guide* (literature number SPRU160) for CPU instruction set information.

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240x legend for the internal hardware

Table 4. Legend for the 240x DSP CPU Internal Hardware

| SYMBOL | NAME | DESCRIPTION |
|----------|------------------------------------|---|
| ACC | Accumulator | 32-bit register that stores the results and provides input for subsequent CALU operations. Also includes shift and rotate capabilities |
| ARAU | Auxiliary Register Arithmetic Unit | An unsigned, 16-bit arithmetic unit used to calculate indirect addresses using the auxiliary registers as inputs and outputs |
| AUX REGS | Auxiliary Registers 0–7 | These 16-bit registers are used as pointers to anywhere within the data space address range. They are operated upon by the ARAU and are selected by the auxiliary register pointer (ARP). AR0 can also be used as an index value for AR updates of more than one and as a compare value to AR. |
| C | Carry | Register carry output from CALU. C is fed back into the CALU for extended arithmetic operation. The C bit resides in status register 1 (ST1), and can be tested in conditional instructions. C is also used in accumulator shifts and rotates. |
| CALU | Central Arithmetic Logic Unit | 32-bit-wide main arithmetic logic unit for the TMS320C2xx core. The CALU executes 32-bit operations in a single machine cycle. CALU operates on data coming from ISCALE or PSCALE with data from ACC, and provides status results to PCTRL. |
| DARAM | Dual-Access RAM | If the on-chip RAM configuration control bit (CNF) is set to 0, the reconfigurable data dual-access RAM (DARAM) block B0 is mapped to data space; otherwise, B0 is mapped to program space. Blocks B1 and B2 are mapped to data memory space only, at addresses 0300–03FF and 0060–007F, respectively. Blocks 0 and 1 contain 256 words, while block 2 contains 32 words. |
| DP | Data Memory Page Pointer | The 9-bit DP register is concatenated with the seven least significant bits (LSBs) of an instruction word to form a direct memory address of 16 bits. DP can be modified by the LST and LDP instructions. |
| GREG | Global Memory Allocation Register | GREG specifies the size of the global data memory space. Since the global memory space is not used in the 240x devices, this register is reserved. |
| IMR | Interrupt Mask Register | IMR individually masks or enables the seven interrupts. |
| IFR | Interrupt Flag Register | The 7-bit IFR indicates that the TMS320C2xx has latched an interrupt from one of the seven maskable interrupts. |
| INT# | Interrupt Traps | A total of 32 interrupts by way of hardware and/or software are available. |
| ISCALE | Input Data-Scaling Shifter | 16- to 32-bit barrel left-shifter. ISCALE shifts incoming 16-bit data 0 to 16 positions left, relative to the 32-bit output within the fetch cycle; therefore, no cycle overhead is required for input scaling operations. |
| MPY | Multiplier | 16 × 16-bit multiplier to a 32-bit product. MPY executes multiplication in a single cycle. MPY operates either signed or unsigned 2s-complement arithmetic multiply. |
| MSTACK | Micro Stack | MSTACK provides temporary storage for the address of the next instruction to be fetched when program address-generation logic is used to generate sequential addresses in data space. |
| MUX | Multiplexer | Multiplexes buses to a common input |
| NPAR | Next Program Address Register | NPAR holds the program address to be driven out on the PAB in the next cycle. |
| OSCALE | Output Data-Scaling Shifter | 16- to 32-bit barrel left-shifter. OSCALE shifts the 32-bit accumulator output 0 to 7 bits left for quantization management and outputs either the 16-bit high- or low-half of the shifted 32-bit data to the data-write data bus (DWEB). |
| PAR | Program Address Register | PAR holds the address currently being driven on PAB for as many cycles as it takes to complete all memory operations scheduled for the current bus cycle. |
| PC | Program Counter | PC increments the value from NPAR to provide sequential addresses for instruction-fetching and sequential data-transfer operations. |
| PCTRL | Program Controller | PCTRL decodes instruction, manages the pipeline, stores status, and decodes conditional operations. |

240x legend for the internal hardware (continued)

Table 4. Legend for the 240x DSP CPU Internal Hardware (Continued)

| SYMBOL | NAME | DESCRIPTION |
|--------|-------------------------|---|
| PREG | Product Register | 32-bit register holds results of 16×16 multiply |
| PSCALE | Product-Scaling Shifter | 0-, 1-, or 4-bit left shift, or 6-bit right shift of multiplier product. The left-shift options are used to manage the additional sign bits resulting from the 2s-complement multiply. The right-shift option is used to scale down the number to manage overflow of product accumulation in the CALU. PSCALE resides in the path from the 32-bit product shifter and from either the CALU or the data-write data bus (DWEB), and requires no cycle overhead. |
| STACK | Stack | STACK is a block of memory used for storing return addresses for subroutines and interrupt-service routines, or for storing data. The C2xx stack is 16 bits wide and 8 levels deep. |
| TREG | Temporary Register | 16-bit register holds one of the operands for the multiply operations. TREG holds the dynamic shift count for the LACT, ADDT, and SUBT instructions. TREG holds the dynamic bit position for the BITT instruction. |

status and control registers

Two status registers, ST0 and ST1, contain the status of various conditions and modes. These registers can be stored into data memory and loaded from data memory, thus allowing the status of the machine to be saved and restored for subroutines.

The load status register (LST) instruction is used to write to ST0 and ST1. The store status register (SST) instruction is used to read from ST0 and ST1 — except for the INTM bit, which is not affected by the LST instruction. The individual bits of these registers can be set or cleared when using the SETC and CLRC instructions. Figure 5 shows the organization of status registers ST0 and ST1, indicating all status bits contained in each. Several bits in the status registers are reserved and are read as logic 1s. Table 5 lists status register field definitions.

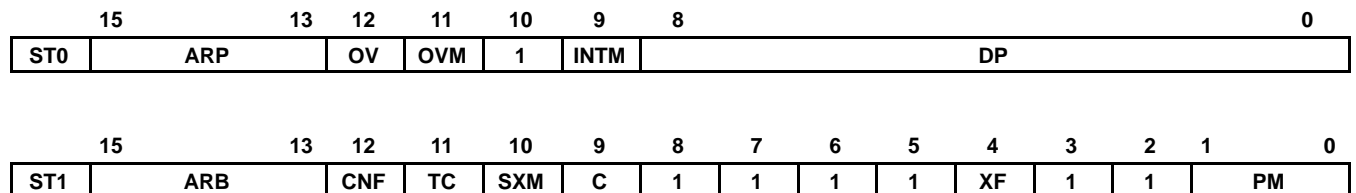


Figure 5. Organization of Status Registers ST0 and ST1

Table 5. Status Register Field Definitions

| FIELD | FUNCTION |
|-------|--|
| ARB | Auxiliary register pointer buffer. When the ARP is loaded into ST0, the old ARP value is copied to the ARB except during an LST instruction. When the ARB is loaded by way of an LST #1 instruction, the same value is also copied to the ARP. |
| ARP | Auxiliary register (AR) pointer. ARP selects the AR to be used in indirect addressing. When the ARP is loaded, the old ARP value is copied to the ARB register. ARP can be modified by memory-reference instructions when using indirect addressing, and by the LARP, MAR, and LST instructions. The ARP is also loaded with the same value as ARB when an LST #1 instruction is executed. |
| C | Carry bit. C is set to 1 if the result of an addition generates a carry, or reset to 0 if the result of a subtraction generates a borrow. Otherwise, C is reset after an addition or set after a subtraction, except if the instruction is ADD or SUB with a 16-bit shift. In these cases, ADD can only set and SUB can only reset the carry bit, but cannot affect it otherwise. The single-bit shift and rotate instructions also affect C, as well as the SETC, CLRC, and LST #1 instructions. Branch instructions have been provided to branch on the status of C. C is set to 1 on a reset. |
| CNF | On-chip RAM configuration control bit. If CNF is set to 0, the reconfigurable data dual-access RAM blocks are mapped to data space; otherwise, they are mapped to program space. The CNF can be modified by the SETC CNF, CLRC CNF, and LST #1 instructions. \overline{RS} sets the CNF to 0. |

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status and control registers (continued)

Table 5. Status Register Field Definitions (Continued)

| FIELD | FUNCTION |
|-------|--|
| DP | Data memory page pointer. The 9-bit DP register is concatenated with the 7 LSBs of an instruction word to form a direct memory address of 16 bits. DP can be modified by the LST and LDP instructions. |
| INTM | Interrupt mode bit. When INTM is set to 0, all unmasked interrupts are enabled. When set to 1, all maskable interrupts are disabled. INTM is set and reset by the SETC INTM and CLRC INTM instructions. RS also sets INTM. INTM has no effect on the unmaskable RS and NMI interrupts. Note that INTM is unaffected by the LST instruction. This bit is set to 1 by reset. It is also set to 1 when a maskable interrupt trap is taken. |
| OV | Overflow flag bit. As a latched overflow signal, OV is set to 1 when overflow occurs in the arithmetic logic unit (ALU). Once an overflow occurs, the OV remains set until a reset, BCND/D on OV/NOV, or LST instruction clears OV. |
| OVM | Overflow mode bit. When OVM is set to 0, overflowed results overflow normally in the accumulator. When set to 1, the accumulator is set to either its most positive or negative value upon encountering an overflow. The SETC and CLRC instructions set and reset this bit, respectively. LST can also be used to modify the OVM. |
| PM | Product shift mode. If these two bits are 00, the multiplier's 32-bit product is loaded into the ALU with no shift. If PM = 01, the PREG output is left-shifted one place and loaded into the ALU, with the LSB zero-filled. If PM = 10, the PREG output is left-shifted by 4 bits and loaded into the ALU, with the LSBs zero-filled. PM = 11 produces a right shift of 6 bits, sign-extended. Note that the PREG contents remain unchanged. The shift takes place when transferring the contents of the PREG to the ALU. PM is loaded by the SPM and LST #1 instructions. PM is cleared by RS. |
| SXM | Sign-extension mode bit. SXM = 1 produces sign extension on data as it is passed into the accumulator through the scaling shifter. SXM = 0 suppresses sign extension. SXM does not affect the definitions of certain instructions; for example, the ADDS instruction suppresses sign extension regardless of SXM. SXM is set by the SETC SXM instruction and reset by the CLRC SXM instruction and can be loaded by the LST #1 instruction. SXM is set to 1 by reset. |
| TC | Test/control flag bit. TC is affected by the BIT, BITT, CMPR, LST #1, and NORM instructions. TC is set to a 1 if a bit tested by BIT or BITT is a 1, if a compare condition tested by CMPR exists between AR (ARP) and AR0, if the exclusive-OR function of the 2 most significant bits (MSBs) of the accumulator is true when tested by a NORM instruction. The conditional branch, call, and return instructions can execute based on the condition of TC. |
| XF | XF pin status bit. XF indicates the state of the XF pin, a general-purpose output pin. XF is set by the SETC XF instruction and reset by the CLRC XF instruction. XF is set to 1 by reset. |

central processing unit

The TMS320x240x central processing unit (CPU) contains a 16-bit scaling shifter, a 16 x 16-bit parallel multiplier, a 32-bit central arithmetic logic unit (CALU), a 32-bit accumulator, and additional shifters at the outputs of both the accumulator and the multiplier. This section describes the CPU components and their functions. The functional block diagram shows the components of the CPU.

input scaling shifter

The TMS320x240x provides a scaling shifter with a 16-bit input connected to the data bus and a 32-bit output connected to the CALU. This shifter operates as part of the path of data coming from program or data space to the CALU and requires no cycle overhead. It is used to align the 16-bit data coming from memory to the 32-bit CALU. This is necessary for scaling arithmetic as well as aligning masks for logical operations.

The scaling shifter produces a left shift of 0 to 16 on the input data. The LSBs of the output are filled with zeros; the MSBs can either be filled with zeros or sign-extended, depending upon the value of the SXM bit (sign-extension mode) of status register ST1. The shift count is specified by a constant embedded in the instruction word or by a value in TREG. The shift count in the instruction allows for specific scaling or alignment operations specific to that point in the code. The TREG base shift allows the scaling factor to be adaptable to the system's performance.



multiplier

The TMS320x240x devices use a 16 x 16-bit hardware multiplier that is capable of computing a signed or an unsigned 32-bit product in a single machine cycle. All multiply instructions, except the MPYU (multiply unsigned) instruction, perform a signed multiply operation. That is, two numbers being multiplied are treated as 2s-complement numbers, and the result is a 32-bit 2s-complement number. There are two registers associated with the multiplier, as follow:

- 16-bit temporary register (TREG) that holds one of the operands for the multiplier
- 32-bit product register (PREG) that holds the product

Four product-shift modes (PM) are available at the PREG output (PSCALE). These shift modes are useful for performing multiply/accumulate operations, performing fractional arithmetic, or justifying fractional products. The PM field of status register ST1 specifies the PM shift mode, as shown in Table 6.

Table 6. PSCALE Product-Shift Modes

| PM | SHIFT | DESCRIPTION |
|----|----------|---|
| 00 | No shift | Product feed to CALU or data bus with no shift |
| 01 | Left 1 | Removes the extra sign bit generated in a 2s-complement multiply to produce a Q31 product |
| 10 | Left 4 | Removes the extra 4 sign bits generated in a 16x13 2s-complement multiply to produce a Q31 product when using the multiply-by-a-13-bit constant |
| 11 | Right 6 | Scales the product to allow up to 128 product accumulation without the possibility of accumulator overflow |

The product can be shifted one bit to compensate for the extra sign bit gained in multiplying two 16-bit 2s-complement numbers (MPY instruction). A four-bit shift is used in conjunction with the MPY instruction with a short immediate value (13 bits or less) to eliminate the four extra sign bits gained in multiplying a 16-bit number by a 13-bit number. Finally, the output of PREG can be right-shifted 6 bits to enable the execution of up to 128 consecutive multiply/accumulates without the possibility of overflow.

The LT (load TREG) instruction normally loads TREG to provide one operand (from the data bus), and the MPY (multiply) instruction provides the second operand (also from the data bus). A multiplication also can be performed with a 13-bit immediate operand when using the MPY instruction. Then, a product is obtained every two cycles. When the code is executing multiple multiplies and product sums, the CPU supports the pipelining of the TREG load operations with CALU operations using the previous product. The pipeline operations that run in parallel with loading the TREG include: load ACC with PREG (LTP); add PREG to ACC (LTA); add PREG to ACC and shift TREG input data (DMOV) to next address in data memory (LTD); and subtract PREG from ACC (LTS).

Two multiply/accumulate instructions (MAC and MACD) fully utilize the computational bandwidth of the multiplier, allowing both operands to be processed simultaneously. The data for these operations can be transferred to the multiplier each cycle by way of the program and data buses. This facilitates single-cycle multiply/accumulates when used with the repeat (RPT) instruction. In these instructions, the coefficient addresses are generated by program address generation (PAGEN) logic, while the data addresses are generated by data address generation (DAGEN) logic. This allows the repeated instruction to access the values from the coefficient table sequentially and step through the data in any of the indirect addressing modes.

The MACD instruction, when repeated, supports filter constructs (weighted running averages) so that as the sum-of-products is executed, the sample data is shifted in memory to make room for the next sample and to throw away the oldest sample.

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multiplier (continued)

The MPYU instruction performs an unsigned multiplication, which greatly facilitates extended-precision arithmetic operations. The unsigned contents of TREG are multiplied by the unsigned contents of the addressed data memory location, with the result placed in PREG. This process allows the operands of greater than 16 bits to be broken down into 16-bit words and processed separately to generate products of greater than 32 bits. The SQRA (square/add) and SQRS (square/subtract) instructions pass the same value to both inputs of the multiplier for squaring a data memory value.

After the multiplication of two 16-bit numbers, the 32-bit product is loaded into the 32-bit product register (PREG). The product from PREG can be transferred to the CALU or to data memory by way of the SPH (store product high) and SPL (store product low) instructions. Note: the transfer of PREG to either the CALU or data bus passes through the PSCALE shifter, and therefore is affected by the product shift mode defined by PM. This is important when saving PREG in an interrupt-service-routine context save as the PSCALE shift effects cannot be modeled in the restore operation. PREG can be cleared by executing the MPY #0 instruction. The product register can be restored by loading the saved low half into TREG and executing a MPY #1 instruction. The high half, then, is loaded using the LPH instruction.

central arithmetic logic unit

The TMS320x240x central arithmetic logic unit (CALU) implements a wide range of arithmetic and logical functions, the majority of which execute in a single clock cycle. This ALU is referred to as central to differentiate it from a second ALU used for indirect-address generation called the auxiliary register arithmetic unit (ARAU). Once an operation is performed in the CALU, the result is transferred to the accumulator (ACC) where additional operations, such as shifting, can occur. Data that is input to the CALU can be scaled by ISCALE when coming from one of the data buses (DRDB or PRDB) or scaled by PSCALE when coming from the multiplier.

The CALU is a general-purpose ALU that operates on 16-bit words taken from data memory or derived from immediate instructions. In addition to the usual arithmetic instructions, the CALU can perform Boolean operations, facilitating the bit-manipulation ability required for a high-speed controller. One input to the CALU is always provided from the accumulator, and the other input can be provided from the product register (PREG) of the multiplier or the output of the scaling shifter (that has been read from data memory or from the ACC). After the CALU has performed the arithmetic or logical operation, the result is stored in the accumulator.

The TMS320x240x devices support floating-point operations for applications requiring a large dynamic range. The NORM (normalization) instruction is used to normalize fixed-point numbers contained in the accumulator by performing left shifts. The four bits of the TREG define a variable shift through the scaling shifter for the LACT/ADDT/SUBT (load/add to/subtract from accumulator with shift specified by TREG) instructions. These instructions are useful in floating-point arithmetic where a number needs to be denormalized — that is, floating-point to fixed-point conversion. They are also useful in the execution of an automatic gain control (AGC) going into a filter. The BITT (bit test) instruction provides testing of a single bit of a word in data memory based on the value contained in the four LSBs of TREG.

The CALU overflow saturation mode can be enabled/disabled by setting/resetting the OVM bit of ST0. When the CALU is in the overflow saturation mode and an overflow occurs, the overflow flag is set and the accumulator is loaded with either the most positive or the most negative value representable in the accumulator, depending on the direction of the overflow. The value of the accumulator at saturation is 07FFFFFFh (positive) or 080000000h (negative). If the OVM (overflow mode) status register bit is reset and an overflow occurs, the overflowed results are loaded into the accumulator with modification. (Note that logical operations cannot result in overflow.)

The CALU can execute a variety of branch instructions that depend on the status of the CALU and the accumulator. These instructions can be executed conditionally based on any meaningful combination of these status bits. For overflow management, these conditions include OV (branch on overflow) and EQ (branch on accumulator equal to zero). In addition, the BACC (branch to address in accumulator) instruction provides the ability to branch to an address specified by the accumulator (computed goto). Bit test instructions (BIT and BITT), which do not affect the accumulator, allow the testing of a specified bit of a word in data memory.



central arithmetic logic unit (continued)

The CALU also has an associated carry bit that is set or reset depending on various operations within the device. The carry bit allows more efficient computation of extended-precision products and additions or subtractions. It is also useful in overflow management. The carry bit is affected by most arithmetic instructions as well as the single-bit shift and rotate instructions. It is not affected by loading the accumulator, logical operations, or other such non-arithmetic or control instructions.

The ADDC (add to accumulator with carry) and SUBB (subtract from accumulator with borrow) instructions use the previous value of carry in their addition/subtraction operation.

The one exception to the operation of the carry bit is in the use of ADD with a shift count of 16 (add to high accumulator) and SUB with a shift count of 16 (subtract from high accumulator) instructions. This case of the ADD instruction can set the carry bit only if a carry is generated, and this case of the SUB instruction can reset the carry bit only if a borrow is generated; otherwise, neither instruction affects it.

Two conditional operands, C and NC, are provided for branching, calling, returning, and conditionally executing, based upon the status of the carry bit. The SETC, CLRC, and LST #1 instructions also can be used to load the carry bit. The carry bit is set to one on a hardware reset.

accumulator

The 32-bit accumulator is the registered output of the CALU. It can be split into two 16-bit segments for storage in data memory. Shifters at the output of the accumulator provide a left shift of 0 to 7 places. This shift is performed while the data is being transferred to the data bus for storage. The contents of the accumulator remain unchanged. When the postscaling shifter is used on the high word of the accumulator (bits 16–31), the MSBs are lost and the LSBs are filled with bits shifted in from the low word (bits 0–15). When the postscaling shifter is used on the low word, the LSBs are zero-filled.

The SFL and SFR (in-place one-bit shift to the left/right) instructions and the ROL and ROR (rotate to the left/right) instructions implement shifting or rotating of the contents of the accumulator through the carry bit. The SXM bit affects the definition of the SFR (shift accumulator right) instruction. When SXM = 1, SFR performs an arithmetic right shift, maintaining the sign of the accumulator data. When SXM = 0, SFR performs a logical shift, shifting out the LSBs and shifting in a zero for the MSB. The SFL (shift accumulator left) instruction is not affected by the SXM bit and behaves the same in both cases, shifting out the MSB and shifting in a zero. Repeat (RPT) instructions can be used with the shift and rotate instructions for multiple-bit shifts.

auxiliary registers and auxiliary-register arithmetic unit (ARAU)

The 240x provides a register file containing eight auxiliary registers (AR0–AR7). The auxiliary registers are used for indirect addressing of the data memory or for temporary data storage. Indirect auxiliary-register addressing allows placement of the data memory address of an instruction operand into one of the auxiliary registers. These registers are referenced with a 3-bit auxiliary register pointer (ARP) that is loaded with a value from 0 through 7, designating AR0 through AR7, respectively. The auxiliary registers and the ARP can be loaded from data memory, the ACC, the product register, or by an immediate operand defined in the instruction. The contents of these registers also can be stored in data memory or used as inputs to the CALU.

The auxiliary register file (AR0–AR7) is connected to the ARAU. The ARAU can autoindex the current auxiliary register while the data memory location is being addressed. Indexing either by ± 1 or by the contents of the AR0 register can be performed. As a result, accessing tables of information does not require the CALU for address manipulation; therefore, the CALU is free for other operations in parallel.

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internal memory

The TMS320LF240x devices are configured with the following memory modules:

- Dual-access random-access memory (DARAM)
- Single-access random-access memory (SARAM)
- Flash
- Boot ROM

dual-access RAM (DARAM)

There are 544 words \times 16 bits of DARAM on the 240x devices. The 240x DARAM allows writes to and reads from the RAM in the same cycle. The DARAM is configured in three blocks: block 0 (B0), block 1 (B1), and block 2 (B2). Block 1 contains 256 words and Block 2 contains 32 words, and both blocks are located only in data memory space. Block 0 contains 256 words, and can be configured to reside in either data or program memory space. The SETC CNF (configure B0 as program memory) and CLRC CNF (configure B0 as data memory) instructions allow dynamic configuration of the memory maps through software.

When using on-chip RAM, the 240x runs at full speed with no wait states. The ability of the DARAM to allow two accesses to be performed in one cycle, coupled with the parallel nature of the 240x architecture, enables the device to perform three concurrent memory accesses in any given machine cycle. Externally, the READY line or on-chip software wait-state generator can be used to interface the 2407 to slower, less expensive external memory.

single-access RAM (SARAM)

There are 2K words \times 16 bits of SARAM on some of the 240x devices.[†] The PON and DON bits select SARAM (2K) mapping in program space, data space, or both. See Table 19 for details on the SCSR2 register and the PON and DON bits. At reset, these bits are 11, and the on-chip SARAM is mapped in both the program and data spaces. The SARAM (starting at 8000h in program memory) is accessible in external memory space (for 2407 only), if the on-chip SARAM is not enabled.

Flash EEPROM

Flash EEPROM provides an attractive alternative to masked program ROM. Like ROM, Flash is nonvolatile. However, it has the advantage of “in-target” reprogrammability. The LF2407 incorporates one 32K \times 16-bit Flash EEPROM module in program space. The Flash module has multiple sectors that can be individually protected while erasing or programming. The sector size is non-uniform and partitioned as 4K/12K/12K/4K sectors.

Unlike most discrete Flash memory, the LF240x Flash does not require a dedicated state machine, because the algorithms for programming and erasing the Flash are executed by the DSP core. This enables several advantages, including: reduced chip size and sophisticated, adaptive algorithms. For production programming, the IEEE Standard 1149.1[‡] (JTAG) scan port provides easy access to the on-chip RAM for downloading the algorithms and Flash code. This Flash requires 5 V for programming (at V_{CCP} pin only) the array. The Flash runs at zero wait state while the device is powered at 3.3 V.

[†] See Table 1 for device-specific features.

[‡] IEEE Standard 1149.1–1990, IEEE Standard Test Access Port.

boot ROM

Boot ROM is a 256-word ROM memory mapped in program space 0000–00FF. This ROM will be enabled if the BOOT_EN pin is low during reset. The BOOT_EN bit (bit 3 of the SCSR2 register) will be set to 0 if the BOOT_EN pin is low at reset. Boot ROM can also be enabled by writing 0 to the SCSR2.3 bit and disabled by writing 1 to this bit.

The boot ROM has a generic bootloader to transfer code through SCI or SPI ports. The incoming code should disable the BOOT_ROM bit by writing 1 to bit 3 of the SCSR2 register, or else, the whole Flash array will not be enabled.

The boot ROM code always sets the PLL to x4 option. If the boot ROM is used, the CLKIN value should not exceed 7.5 MHz. Any CLKIN value greater than 7.5 MHz would force the DSP to run at speeds greater than 30 MHz, the maximum rated speed. Furthermore, when the bootloader is used, only specific values of CLKIN would result in a baud-lock for the SCI. Refer to the *TMS320LF/LC240x DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357) for more details about the bootloader operation.

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PERIPHERALS

The integrated peripherals of the TMS320x240x are described in the following subsections:

- Two event-manager modules (EVA, EVB)
- Enhanced analog-to-digital converter (ADC) module
- Controller area network (CAN) module
- Serial communications interface (SCI) module
- Serial peripheral interface (SPI) module
- PLL-based clock module
- Digital I/O and shared pin functions
- External memory interfaces (LF2407 only)
- Watchdog (WD) timer module

event manager modules (EVA, EVB)

The event-manager modules include general-purpose (GP) timers, full-compare/PWM units, capture units, and quadrature-encoder pulse (QEP) circuits. EVA's and EVB's timers, compare units, and capture units function identically. However, timer/unit names differ for EVA and EVB. Table 7 shows the module and signal names used. Table 7 shows the features and functionality available for the event-manager modules and highlights EVA nomenclature.

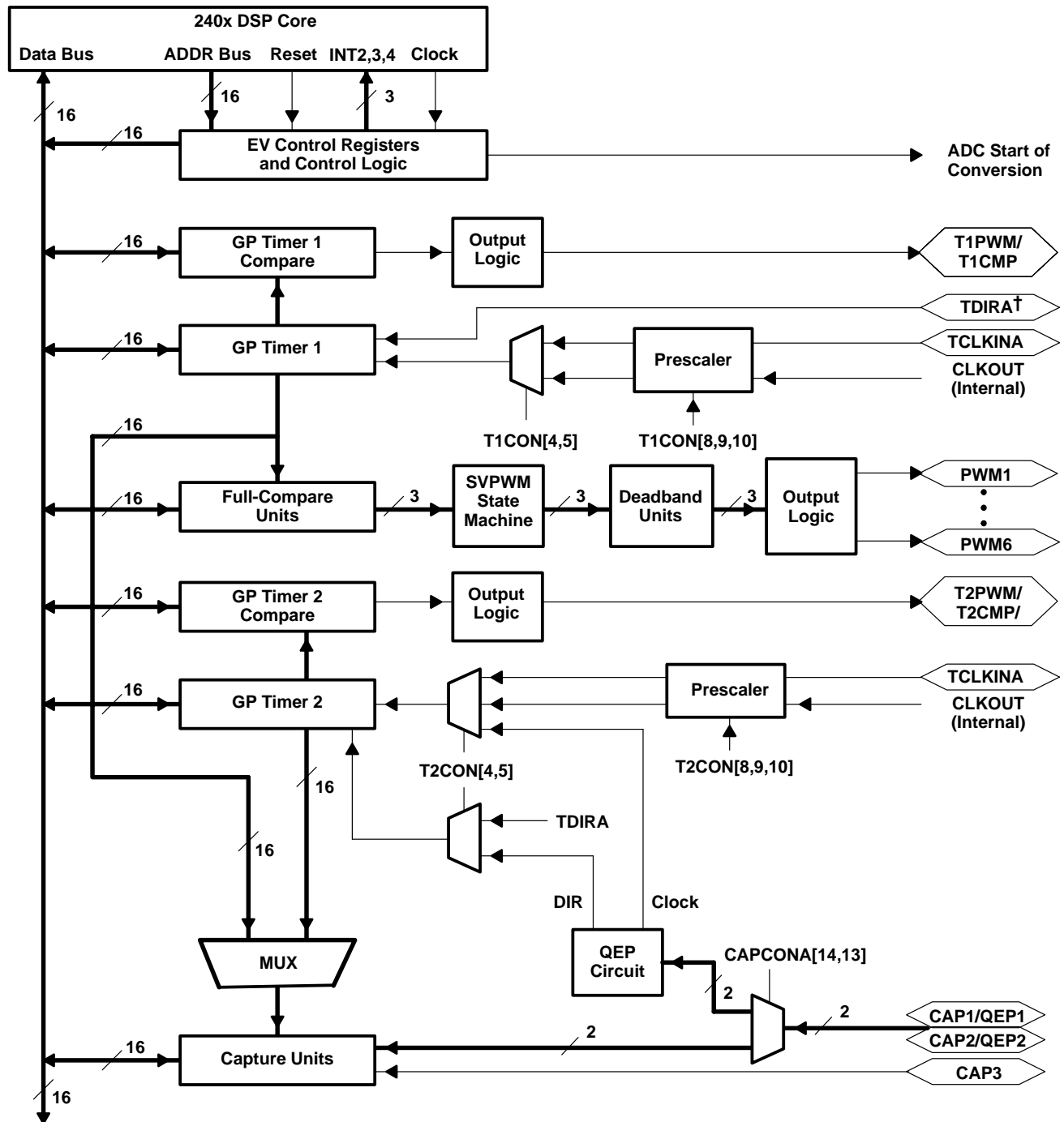
Event managers A and B have identical peripheral register sets with EVA starting at 7400h and EVB starting at 7500h. The paragraphs in this section describe the function of GP timers, compare units, capture units, and QEPs using EVA nomenclature. These paragraphs are applicable to EVB with regard to function—however, module/signal names would differ.

Table 7. Module and Signal Names for EVA and EVB

| EVENT MANAGER MODULES | EVA | | EVB | |
|-----------------------|-------------------------------------|----------------------------|-------------------------------------|-------------------------------|
| | MODULE | SIGNAL | MODULE | SIGNAL |
| GP Timers | Timer 1 Timer 2 | T1PWM/T1CMP T2PWM/T2CMP | Timer 3 Timer 4 | T3PWM/T3CMP T4PWM/T4CMP |
| Compare Units | Compare 1 Compare 2 Compare 3 | PWM1/2 PWM3/4 PWM5/6 | Compare 4 Compare 5 Compare 6 | PWM7/8 PWM9/10 PWM11/12 |
| Capture Units | Capture 1 Capture 2 Capture 3 | CAP1 CAP2 CAP3 | Capture 4 Capture 5 Capture 6 | CAP4 CAP5 CAP6 |
| QEP | QEP1 QEP2 | QEP1 QEP2 | QEP3 QEP4 | QEP3 QEP4 |
| External Inputs | Direction External Clock | TDIRA TCLKINA | Direction External Clock | TDIRB TCLKINB |



event manager modules (EVA, EVB) (continued)



† The 2402 device does not support external direction control. TDIR is not available.

Figure 6. Event Manager A Block Diagram

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DSP CONTROLLERS

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general-purpose (GP) timers

There are two GP timers. The GP timer x (x = 1 or 2 for EVA; x = 3 or 4 for EVB) includes:

- A 16-bit timer, up-/down-counter, TxCNT, for reads or writes
- A 16-bit timer-compare register, TxCMPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-period register, TxPR (double-buffered with shadow register), for reads or writes
- A 16-bit timer-control register, TxCON, for reads or writes
- Selectable internal or external input clocks
- A programmable prescaler for internal or external clock inputs
- Control and interrupt logic, for four maskable interrupts: *underflow*, *overflow*, *timer compare*, and *period interrupts*
- A selectable direction input pin (TDIRx) (to count up or down when directional up-/down-count mode is selected)

The GP timers can be operated independently or synchronized with each other. The compare register associated with each GP timer can be used for compare function and PWM-waveform generation. There are three continuous modes of operations for each GP timer in up- or up/down-counting operations. Internal or external input clocks with programmable prescaler are used for each GP timer. GP timers also provide the time base for the other event-manager submodules: GP timer 1 for all the compares and PWM circuits, GP timer 2/1 for the capture units and the quadrature-pulse counting operations. Double-buffering of the period and compare registers allows programmable change of the timer (PWM) period and the compare/PWM pulse width as needed.

full-compare units

There are three full-compare units on each event manager. These compare units use GP timer1 as the time base and generate six outputs for compare and PWM-waveform generation using programmable deadband circuit. The state of each of the six outputs is configured independently. The compare registers of the compare units are double-buffered, allowing programmable change of the compare/PWM pulse widths as needed.

programmable deadband generator

The deadband generator circuit includes three 8-bit counters and an 8-bit compare register. Desired deadband values (from 0 to 16 μ s) can be programmed into the compare register for the outputs of the three compare units. The deadband generation can be enabled/disabled for each compare unit output individually. The deadband-generator circuit produces two outputs (with or without deadband zone) for each compare unit output signal. The output states of the deadband generator are configurable and changeable as needed by way of the double-buffered ACTR register.

PWM waveform generation

Up to eight PWM waveforms (outputs) can be generated simultaneously by each event manager: three independent pairs (six outputs) by the three full-compare units with *programmable deadbands*, and two independent PWMs by the GP-timer compares.



PWM characteristics

Characteristics of the PWMs are as follows:

- 16-bit registers
- Programmable deadband for the PWM output pairs, from 0 to 16 μ s
- Minimum deadband width of 33.3 ns
- Change of the PWM carrier frequency for PWM frequency wobbling as needed
- Change of the PWM pulse widths within and after each PWM period as needed
- External-maskable power and drive-protection interrupts
- Pulse-pattern-generator circuit, for programmable generation of asymmetric, symmetric, and four-space vector PWM waveforms
- Minimized CPU overhead using auto-reload of the compare and period registers

capture unit

The capture unit provides a logging function for different events or transitions. The values of the selected GP timer counter is captured and stored in the two-level-deep FIFO stacks when selected transitions are detected on capture input pins, CAPx (x = 1, 2, or 3 for EVA; and x = 4, 5, or 6 for EVB). The capture unit consists of three capture circuits.

- Capture units include the following features:
 - One 16-bit capture control register, CAPCONx (R/W)
 - One 16-bit capture FIFO status register, CAPFIFOx
 - Selection of GP timer 1/2 (for EVA) or 3/4 (for EVB) as the time base
 - Three 16-bit 2-level-deep FIFO stacks, one for each capture unit
 - Three capture input pins (CAP1/2/3 for EVA, CAP4/5/6 for EVB)—one input pin per capture unit. [All inputs are synchronized with the device (CPU) clock. In order for a transition to be captured, the input must hold at its current level to meet two rising edges of the device clock. The input pins CAP1/2 and CAP4/5 can also be used as QEP inputs to the QEP circuit.]
 - User-specified transition (rising edge, falling edge, or both edges) detection
 - Three maskable interrupt flags, one for each capture unit

quadrature-encoder pulse (QEP) circuit

Two capture inputs (CAP1 and CAP2 for EVA; CAP4 and CAP5 for EVB) can be used to interface the on-chip QEP circuit with a quadrature encoder pulse. Full synchronization of these inputs is performed on-chip. Direction or leading-quadrature pulse sequence is detected, and GP timer 2/4 is incremented or decremented by the rising and falling edges of the two input signals (four times the frequency of either input pulse).

enhanced analog-to-digital converter (ADC) module

A simplified functional block diagram of the ADC module is shown in Figure 7. The ADC module consists of a 10-bit ADC with a built-in sample-and-hold (S/H) circuit. Functions of the ADC module include:

- 10-bit ADC core with built-in S/H
- Fast conversion time (S/H + Conversion) of 500 ns
- 16-channel, muxed inputs
- Autosequencing capability provides up to 16 “autoconversions” in a single session. Each conversion can be programmed to select any 1 of 16 input channels
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (i.e., two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
 - The digital value of the input analog voltage is derived by:

$$\text{Digital Value} = 1023 \times \frac{\text{Input Analog Voltage} - V_{\text{REFLO}}}{V_{\text{REFHI}} - V_{\text{REFLO}}}$$

- Multiple triggers as sources for the start-of-conversion (SOC) sequence
 - S/W – software immediate start
 - EVA – Event manager A (multiple event sources within EVA)
 - EVB – Event manager B (multiple event sources within EVB)
 - Ext – External pin (ADCSOC)
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS
- Sequencer can operate in “start/stop” mode, allowing multiple “time-sequenced triggers” to synchronize conversions
- EVA and EVB triggers can operate independently in dual-sequencer mode
- Sample-and-hold (S/H) acquisition time window has separate prescale control
- ADC calibration

Note: Refer to the following erratas for restrictions pertaining to the ADC calibration feature:

TMS320LF2402 DSP Controller Silicon Errata (literature number SPRZ157)

TMS320LF2406 DSP Controller Silicon Errata (literature number SPRZ159)

TMS320LF2407 DSP Controller Silicon Errata (literature number SPRZ158)

- Self-test

enhanced analog-to-digital converter (ADC) module (continued)

The ADC module in the 240x has been enhanced to provide flexible interface to event managers A and B. The ADC interface is built around a fast, 10-bit ADC module with total conversion time of 500 ns (S/H + conversion). The ADC module has 16 channels, configurable as two independent 8-channel modules to service event managers A and B. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. Figure 7 shows the block diagram of the 240x ADC module.

The two 8-channel modules have the capability to autosequence a series of conversions, each module has the choice of selecting any one of the respective eight channels available through an analog mux. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.

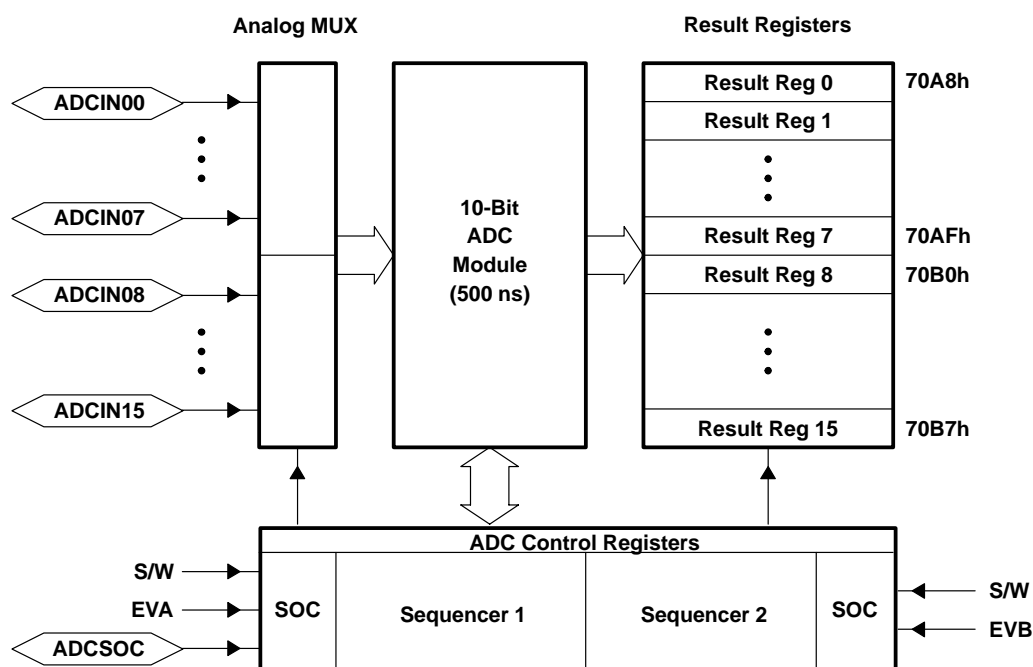


Figure 7. Block Diagram of the 240x ADC Module

To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCINn pins should not run in close proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (such as V_{CCA} , V_{REFHI} , and V_{SSA}) from the digital supply.

controller area network (CAN) module

The CAN module is a full-CAN controller designed as a 16-bit peripheral module and supports the following features:

- CAN specification 2.0B (active)
 - Standard data and remote frames
 - Extended data and remote frames
- Six mailboxes for objects of 0- to 8-byte data length
 - Two receive mailboxes, two transmit mailboxes
 - Two configurable transmit/receive mailboxes
- Local acceptance mask registers for mailboxes 0 and 1 and mailboxes 2 and 3
- Configurable standard or extended message identifier
- Programmable bit rate
- Programmable interrupt scheme
- Readable error counters
- Self-test mode
 - In this mode, the CAN module operates in a loop-back fashion, receiving its own transmitted message.

The CAN module is a 16-bit peripheral. The accesses are split into the control/status-registers accesses and the mailbox-RAM accesses.

CAN peripheral registers: The CPU can access the CAN peripheral registers only using 16-bit write accesses. The CAN peripheral always presents full 16-bit data to the CPU bus during read cycles.

controller area network (CAN) module (continued)

CAN controller architecture

Figure 8 shows the basic architecture of the CAN controller through this block diagram of the CAN Peripherals.

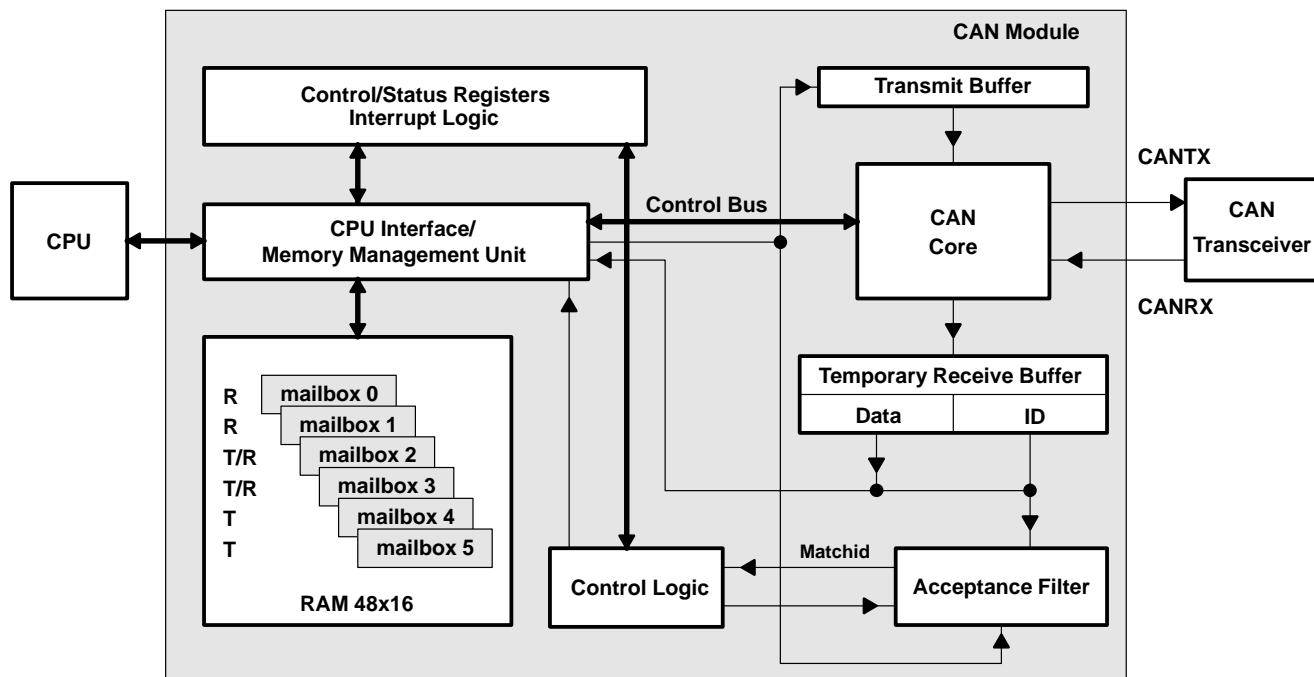


Figure 8. CAN Module Block Diagram

The mailboxes are situated in one 48-word x 16-bit RAM. It can be written to or read by the CPU or the CAN. The CAN write or read access, as well as the CPU read access, needs one clock cycle. The CPU write access needs two clock cycles. In these two clock cycles, the CAN performs a read-modify-write cycle and, therefore, inserts one wait state for the CPU.

Address bit 0 of the address bus used when accessing the RAM decides if the lower (0) or the higher (1) 16-bit word of the 32-bit word is taken. The RAM location is determined by the upper bits 5 to 1 of the address bus.

Table 8 shows the mailbox locations in RAM. One half-word has 16 bits.

CAN interrupt logic

There are two interrupt requests from the CAN module to the peripheral interrupt expansion (PIE) controller: the mailbox interrupt and the error interrupt. Both interrupts can assert either a high-priority request or a low-priority request to the CPU. Since CAN mailboxes can generate multiple interrupts, the software should read the CAN_IFR register for every interrupt and prioritize the interrupt service, or else, these multiple interrupts will not be recognized by the CPU and PIE hardware logic. Each interrupt routine should service all the interrupt bits that are set and clear them after service.

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CAN memory map

Table 8 shows the mailbox locations in the CAN module.

Table 8. Mailbox Addresses†

| ADDRESS OFFSET [5:0] | NAME | DESCRIPTION UPPER HALF-WORD ADDRESS BIT 0 = 1 | DESCRIPTION LOWER HALF-WORD ADDRESS BIT 0 = 0 |
|-------------------------|-----------|--|--|
| 00h | MSGID0 | Message ID for mailbox 0 | Message ID for mailbox 0 |
| 02h | MSGCTRL0 | Unused | RTR and DLC (bits 4 to 0) |
| 04h | Datalow0 | Databyte 0, Databyte 1 (DBO = 1) | Databyte 2, Databyte 3 (DBO = 1) |
| | | Databyte 3, Databyte 2 (DBO = 0) | Databyte 1, Databyte 0 (DBO = 0) |
| 06h | Datahigh0 | Databyte 4, Databyte 5 (DBO = 1) | Databyte 6, Databyte 7 (DBO = 1) |
| | | Databyte 7, Databyte 6 (DBO = 0) | Databyte 5, Databyte 4 (DBO = 0) |
| 08h | MSGID1 | Message ID for mailbox 1 | Message ID for mailbox 1 |
| 0Ah | MSGCTRL1 | Unused | RTR and DLC (bits 4 to 0) |
| 0Ch | Datalow1 | Databyte 0, Databyte 1 (DBO = 1) | Databyte 2, Databyte 3 (DBO = 1) |
| | | Databyte 3, Databyte 2 (DBO = 0) | Databyte 1, Databyte 0 (DBO = 0) |
| 0Eh | Datahigh1 | Databyte 4, Databyte 5 (DBO = 1) | Databyte 6, Databyte 7 (DBO = 1) |
| ... | ... | ... | ... |
| 28h | MSGID5 | Message ID for mailbox 5 | Message ID for mailbox 5 |
| 2Ah | MSGCTRL5 | Unused | RTR and DLC (bits 4 to 0) |
| 2Ch | Datalow5 | Databyte 0, Databyte 1 (DBO = 1) | Databyte 2, Databyte 3 (DBO = 1) |
| | | Databyte 3, Databyte 2 (DBO = 0) | Databyte 3, Databyte 2 (DBO = 0) |
| 2Eh | Datahigh5 | Databyte 4, Databyte 5 (DBO = 1) | Databyte 6, Databyte 7 (DBO = 1) |
| | | Databyte 7, Databyte 6 (DBO = 0) | Databyte 5, Databyte 4 (DBO = 0) |

† The DBO (data byte order) bit is located in the MCR register and is used to define the order in which the data bytes are stored in the mailbox when received and the order in which the data bytes are transmitted. Byte 0 is the first byte in the message and Byte 7 is the last one shown in the CAN message.

serial communications interface (SCI) module

The 240x devices include a serial communications interface (SCI) module. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register. Features of the SCI module include:

- Two external pins:
 - SCITXD: SCI transmit-output pin
 - SCIRXD: SCI receive-input pin
- NOTE: Both pins can be used as GPIO if not used for SCI.
- Baud rate programmable to 64K different rates
 - Up to 1875 Kbps at 30-MHz CPUCLK
- Data-word format
 - One start bit
 - Data-word length programmable from one to eight bits
 - Optional even/odd/no parity bit
 - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
 - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
 - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format
- Ten SCI module control registers located in the control register frame beginning at address 7050h

NOTE: All registers in this module are 8-bit registers that are connected to the 16-bit peripheral bus. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 9 shows the SCI module block diagram.

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serial communications interface (SCI) module (continued)

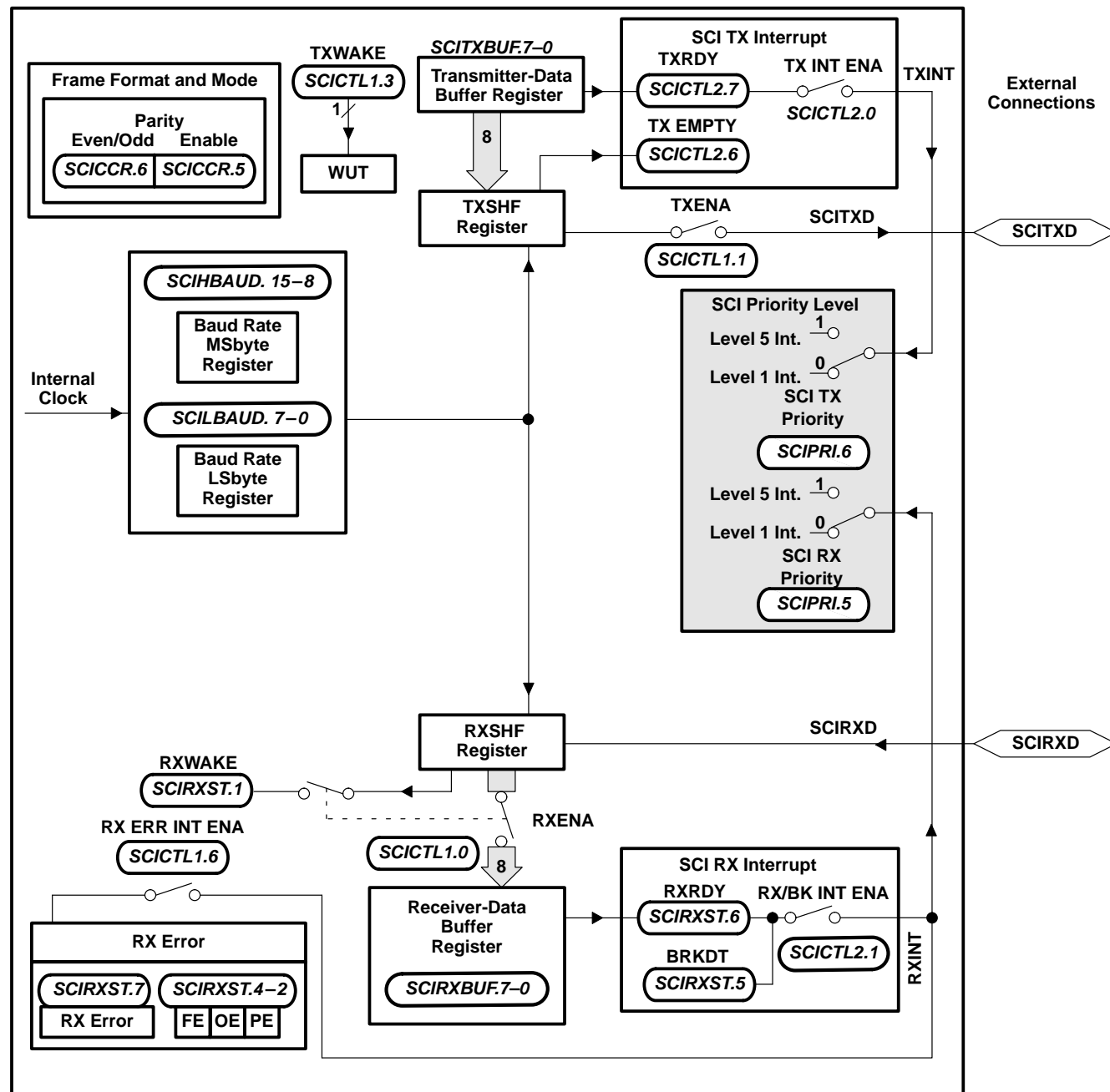


Figure 9. Serial Communications Interface (SCI) Module Block Diagram

serial peripheral interface (SPI) module

Some 240x devices include the four-pin serial peripheral interface (SPI) module. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
 - SPISOMI: SPI slave-output/master-input pin
 - SPISIMO: SPI slave-input/master-output pin
 - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
 - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO, if the SPI module is not used.

- Two operational modes: master and slave
- Baud rate: 125 different programmable rates/7.5 Mbps at 30-MHz CPUCCLK
- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
 - Falling edge without phase delay: SPICLK active high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
 - Falling edge with phase delay: SPICLK active high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge without phase delay: SPICLK inactive low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge with phase delay: SPICLK inactive low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

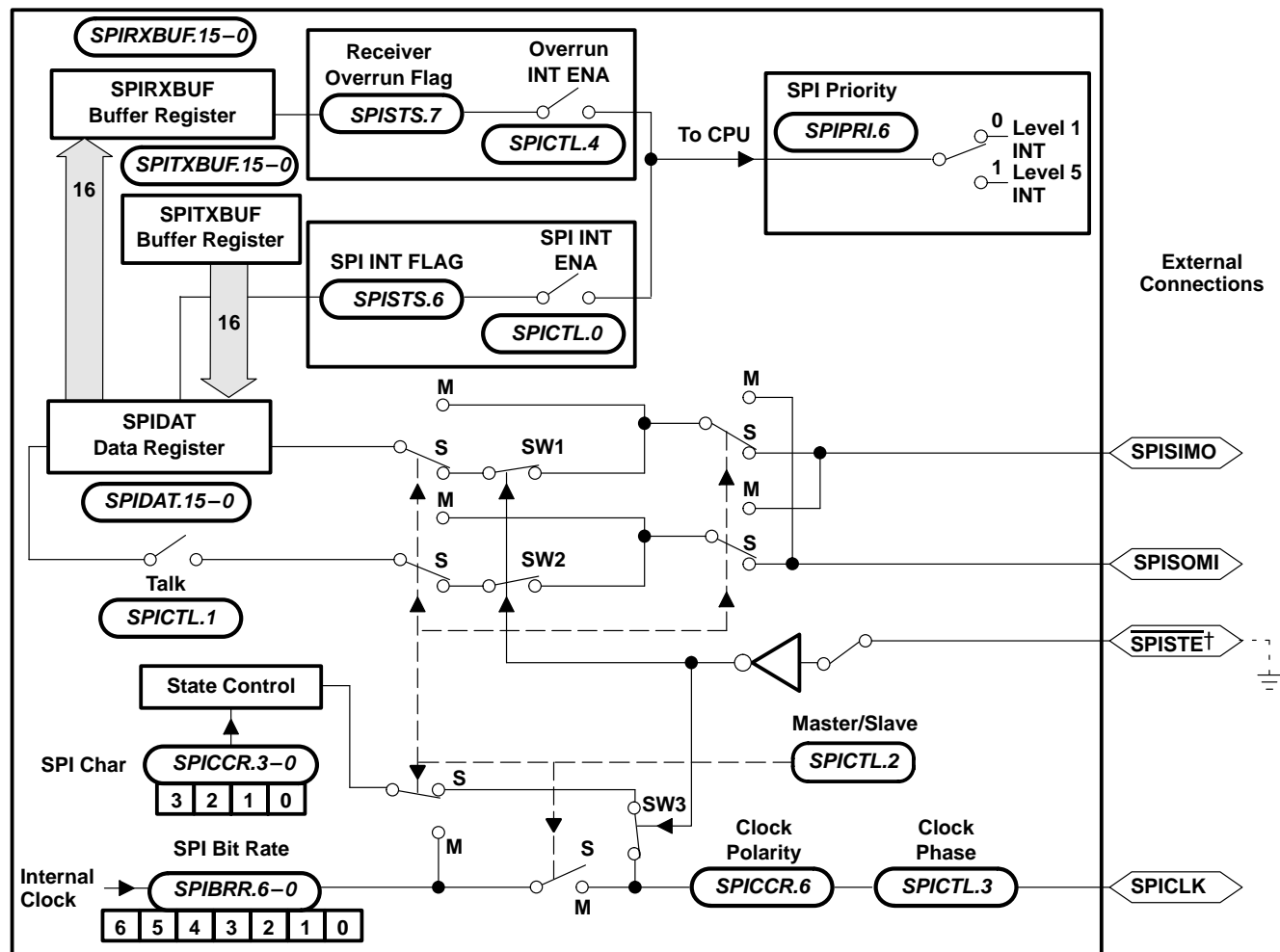
NOTE: All registers in this module are 16-bit registers that are connected to the 16-bit peripheral bus. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

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serial peripheral interface (SPI) module (continued)

Figure 10 is a block diagram of the SPI in slave mode.



NOTE A: The diagram is shown in the slave mode.

† The $\overline{\text{SPISTE}}$ pin is driven low externally. Note that SW1, SW2, and SW3 are closed in this configuration. Refer to the following erratas for restrictions on using the $\overline{\text{SPISTE}}$ pin:

TMS320LF2402 DSP Controller Silicon Errata (literature number SPRZ157)

TMS320LF2406 DSP Controller Silicon Errata (literature number SPRZ159)

TMS320LF2407 DSP Controller Silicon Errata (literature number SPRZ158)

Figure 10. Four-Pin Serial Peripheral Interface Module Block Diagram

PLL-based clock module

The 240x has an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 3-bit ratio control to select different CPU clock rates. See Figure 11 for the PLL Clock Module Block Diagram, Table 9 for clock rates, and Table 10 for the loop filter component values.

The PLL-based clock module provides two modes of operation:

- **Crystal-operation**
This mode allows the use of an external crystal/resonator to provide the time base to the device.
- **External clock source operation**
This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the XTAL1/CLKIN pin. In this case, an external oscillator clock is connected to the XTAL1/CLKIN pin.

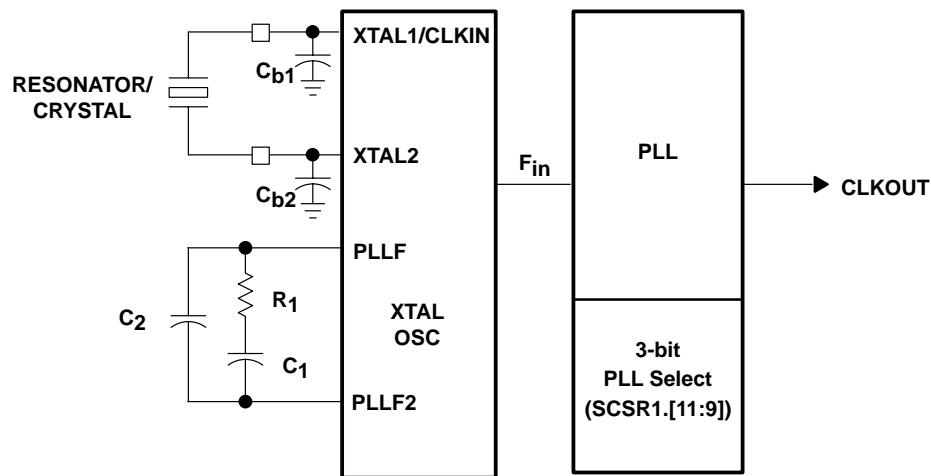


Figure 11. PLL Clock Module Block Diagram

Table 9. PLL Clock Selection Through Bits (11–9) in SCSR1 Register

| CLK PS2 | CLK PS1 | CLK PS0 | CLKOUT |
|---------|---------|---------|----------------------|
| 0 | 0 | 0 | $4 \times F_{in}$ |
| 0 | 0 | 1 | $2 \times F_{in}$ |
| 0 | 1 | 0 | $1.33 \times F_{in}$ |
| 0 | 1 | 1 | $1 \times F_{in}$ |
| 1 | 0 | 0 | $0.8 \times F_{in}$ |
| 1 | 0 | 1 | $0.66 \times F_{in}$ |
| 1 | 1 | 0 | $0.57 \times F_{in}$ |
| 1 | 1 | 1 | $0.5 \times F_{in}$ |

Default multiplication factor after reset is (1,1,1), i.e., $0.5 \times F_{in}$.

CAUTION:

The bootloader sets the PLL to x4 option. If the bootloader is used, the value of CLKIN used should not force CLKOUT to exceed the maximum rated device speed. See the “Boot ROM” section for more details.

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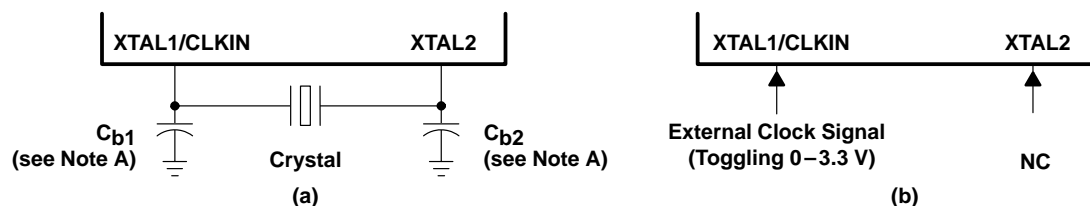
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external reference crystal clock option

The internal oscillator is enabled by connecting a crystal across the XTAL1/CLKIN and XTAL2 pins as shown in Figure 12a. The crystal should be in fundamental operation and parallel resonant, with an effective series resistance of 30 Ω and a power dissipation of 1 mW; it should be specified at a load capacitance of 20 pF.

external reference oscillator clock option

The internal oscillator is disabled by connecting a clock signal to XTAL1/CLKIN and leaving the XTAL2 input pin unconnected as shown in Figure 12b.



NOTE A: TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSP chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will ensure start-up and stability over the entire operating range.

Figure 12. Recommended Crystal/Clock Connection

loop filter

The PLL module uses an external loop filter circuit for jitter minimization. The components for the loop filter circuit are R1, C1, and C2. The capacitors (C1 and C2) must be non-polarized. This loop filter circuit is connected between the PLLF and PLLF2 pins (see Figure 11). For examples of component values of R1, C1, and C2 at a specified oscillator frequency (XTAL1), see Table 10.

Table 10. Loop Filter Component Values With Damping Factor = 2.0

| XTAL1/CLKIN FREQUENCY (MHz) | R1 (Ω) ($\pm 5\%$ TOLERANCE) | C1 (μF) ($\pm 20\%$ TOLERANCE) | C2 (μF) ($\pm 20\%$ TOLERANCE) |
|--------------------------------|--|--|--|
| 4 | 4.7 | 3.9 | 0.082 |
| 5 | 5.6 | 2.7 | 0.056 |
| 6 | 6.8 | 1.8 | 0.039 |
| 7 | 8.2 | 1.5 | 0.033 |
| 8 | 9.1 | 1 | 0.022 |
| 9 | 10 | 0.82 | 0.015 |
| 10 | 11 | 0.68 | 0.015 |
| 11 | 12 | 0.56 | 0.012 |
| 12 | 13 | 0.47 | 0.01 |
| 13 | 15 | 0.39 | 0.0082 |
| 14 | 15 | 0.33 | 0.0068 |
| 15 | 16 | 0.33 | 0.0068 |
| 16 | 18 | 0.27 | 0.0056 |
| 17 | 18 | 0.22 | 0.0047 |
| 18 | 20 | 0.22 | 0.0047 |
| 19 | 22 | 0.18 | 0.0039 |
| 20 | 24 | 0.15 | 0.0033 |

low-power modes

The 240x has an IDLE instruction. When executed, the IDLE instruction stops the clocks to all circuits in the CPU, but the clock output from the CPU continues to run. With this instruction, the CPU clocks can be shut down to save power while the peripherals (clocked with CLKOUT) continue to run. The CPU exits the IDLE state if it is reset, or, if it receives an interrupt request.

clock domains

All 240x-based devices have two clock domains:

1. CPU clock domain – consists of the clock for most of the CPU logic
2. System clock domain – consists of the peripheral clock (which is derived from CLKOUT of the CPU) and the clock for the interrupt logic in the CPU.

When the CPU goes into IDLE mode, the CPU clock domain is stopped while the system clock domain continues to run. This mode is also known as IDLE1 mode. The 240x CPU also contains support for a second IDLE mode, IDLE2. By asserting IDLE2 to the 240x CPU, both the CPU clock domain and the system clock domain are stopped, allowing further power savings. A third low-power mode, HALT mode, the deepest, is possible if the oscillator and WDCLK are also shut down when in IDLE2 mode.

Two control bits, LPM1 and LPM0, specify which of the three possible low-power modes is entered when the IDLE instruction is executed (see Table 11). These bits are located in the System Control and Status Register 1 (SCSR1), and they are described in the *TMS320LF/LC240x DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357).

Table 11. Low-Power Modes Summary

| LOW-POWER MODE | LPMx BITS SCSR1 [13:12] | CPU CLOCK DOMAIN | SYSTEM CLOCK DOMAIN | WDCLK STATUS | PLL STATUS | OSC STATUS | FLASH POWER | EXIT CONDITION |
|---------------------------------------|-------------------------------|------------------------|---------------------------|-----------------|---------------|---------------|----------------|--|
| CPU running normally | XX | On | On | On | On | On | On | — |
| IDLE1 – (LPM0) | 00 | Off | On | On | On | On | On | Peripheral Interrupt, External Interrupt, Reset, PDPINTA/B |
| IDLE2 – (LPM1) | 01 | Off | Off | On | On | On | On | Wakeup Interrupts, External Interrupt, Reset, PDPINTA/B |
| HALT – (LPM2) [PLL/OSC power down] | 1X | Off | Off | Off | Off | Off | Off | Reset, PDPINTA/B |

other power-down options

240x devices have clock-enable bits to the following on-chip peripherals: ADC, SCI, SPI, CAN, EVB, and EVA. Clock to these peripherals are disabled after reset; thus, start-up power can be low for the device.

Depending on the application, these peripherals can be turned on/off to achieve low power.

Refer to the SCSR1 register for details on the peripheral clock enable bits.

digital I/O and shared pin functions

The 240x has up to 41 general-purpose, bidirectional, digital I/O (GPIO) pins—most of which are shared between primary functions and I/O. Most I/O pins of the 240x are shared with other functions. The digital I/O ports module provides a flexible method for controlling both dedicated I/O and shared pin functions. All I/O and shared pin functions are controlled using eight 16-bit registers. These registers are divided into two types:

- Output Control Registers — used to control the multiplexer selection that chooses between the primary function of a pin or the general-purpose I/O function.
- Data and Control Registers — used to control the data and data direction of bidirectional I/O pins.

description of shared I/O pins

The control structure for shared I/O pins is shown in Figure 13, where each pin has three bits that define its operation:

- Mux control bit — this bit selects between the primary function (1) and I/O function (0) of the pin.
- I/O direction bit — if the I/O function is selected for the pin (mux control bit is set to 0), this bit determines whether the pin is an input (0) or an output (1).
- I/O data bit — if the I/O function is selected for the pin (mux control bit is set to 0) and the direction selected is an input, data is read from this bit; if the direction selected is an output, data is written to this bit.

The mux control bit, I/O direction bit, and I/O data bit are in the I/O control registers.

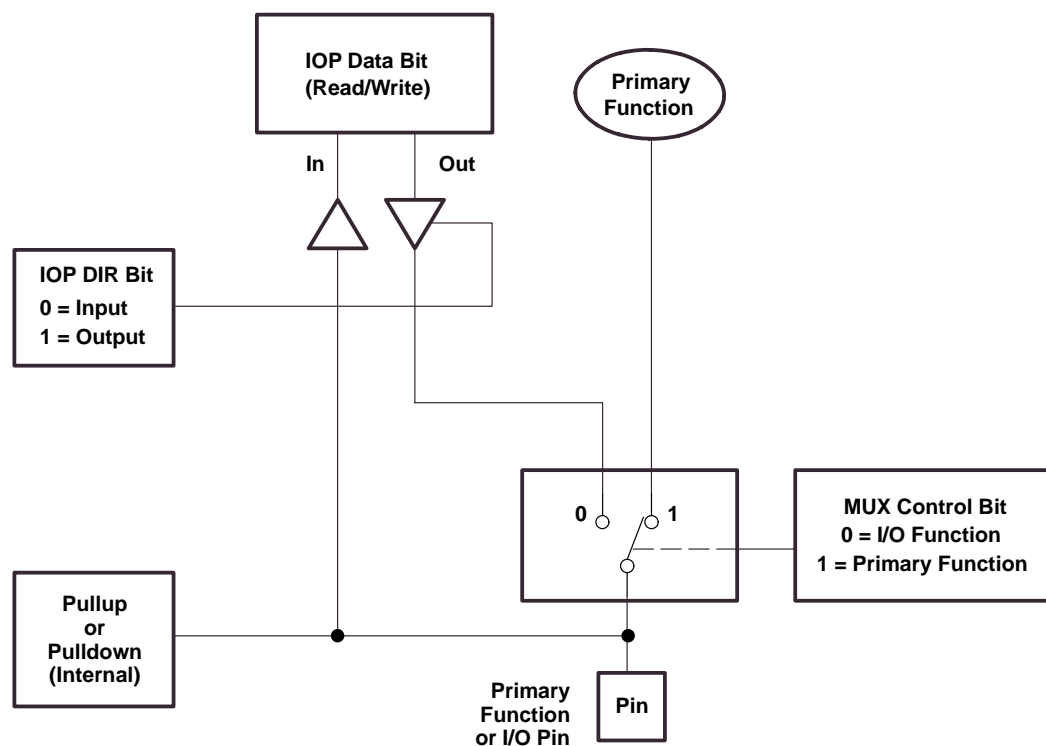


Figure 13. Shared Pin Configuration

A summary of shared pin configurations and associated bits is shown in Table 12.

description of shared I/O pins (continued)

Table 12. Shared Pin Configurations†

| PIN FUNCTION SELECTED | | MUX CONTROL REGISTER (name.bit #) | MUX CONTROL VALUE AT RESET (MCRx.n) | I/O PORT DATA AND DIRECTION‡ | | |
|----------------------------------|---------------------|--|---|------------------------------|---------------|--------------|
| (MCRx.n = 1) Primary Function | (MCRX.N = 0) I/O | | | REGISTER | DATA BIT NO.§ | DIR BIT NO.¶ |
| | | | | PORT A | | |
| SCITXD | IOPA0 | MCRA.0 | 0 | PADATDIR | 0 | 8 |
| SCIRXD | IOPA1 | MCRA.1 | 0 | PADATDIR | 1 | 9 |
| XINT1 | IOPA2 | MCRA.2 | 0 | PADATDIR | 2 | 10 |
| CAP1/QEP1 | IOPA3 | MCRA.3 | 0 | PADATDIR | 3 | 11 |
| CAP2/QEP2 | IOPA4 | MCRA.4 | 0 | PADATDIR | 4 | 12 |
| CAP3 | IOPA5 | MCRA.5 | 0 | PADATDIR | 5 | 13 |
| PWM1 | IOPA6 | MCRA.6 | 0 | PADATDIR | 6 | 14 |
| PWM2 | IOPA7 | MCRA.7 | 0 | PADATDIR | 7 | 15 |
| | | | | PORT B | | |
| PWM3 | IOPB0 | MCRA.8 | 0 | PBDATDIR | 0 | 8 |
| PWM4 | IOPB1 | MCRA.9 | 0 | PBDATDIR | 1 | 9 |
| PWM5 | IOPB2 | MCRA.10 | 0 | PBDATDIR | 2 | 10 |
| PWM6 | IOPB3 | MCRA.11 | 0 | PBDATDIR | 3 | 11 |
| T1PWM/T1CMP | IOPB4 | MCRA.12 | 0 | PBDATDIR | 4 | 12 |
| T2PWM/T2CMP | IOPB5 | MCRA.13 | 0 | PBDATDIR | 5 | 13 |
| TDIRA | IOPB6 | MCRA.14 | 0 | PBDATDIR | 6 | 14 |
| TCLKINA | IOPB7 | MCRA.15 | 0 | PBDATDIR | 7 | 15 |
| | | | | PORT C | | |
| W/R# | IOPC0 | MCRB.0 | 1 | PCDATDIR | 0 | 8 |
| BIO | IOPC1 | MCRB.1 | 1 | PCDATDIR | 1 | 9 |
| SPISIMO | IOPC2 | MCRB.2 | 0 | PCDATDIR | 2 | 10 |
| SPISOMI | IOPC3 | MCRB.3 | 0 | PCDATDIR | 3 | 11 |
| SPICLK | IOPC4 | MCRB.4 | 0 | PCDATDIR | 4 | 12 |
| SPISTE | IOPC5 | MCRB.5 | 0 | PCDATDIR | 5 | 13 |
| CANTX | IOPC6 | MCRB.6 | 0 | PCDATDIR | 6 | 14 |
| CANRX | IOPC7 | MCRB.7 | 0 | PCDATDIR | 7 | 15 |
| | | | | PORT D | | |
| XINT2/ADCSOC | IOPD0 | MCRB.8 | 0 | PDDATDIR | 0 | 8 |
| EMU0 | Reserved | MCRB.9 | 1 | PDDATDIR | 1 | 9 |
| EMU1 | Reserved | MCRB.10 | 1 | PDDATDIR | 2 | 10 |
| TCK | Reserved | MCRB.11 | 1 | PDDATDIR | 3 | 11 |
| TDI | Reserved | MCRB.12 | 1 | PDDATDIR | 4 | 12 |
| TDO | Reserved | MCRB.13 | 1 | PDDATDIR | 5 | 13 |
| TMS | Reserved | MCRB.14 | 1 | PDDATDIR | 6 | 14 |
| TMS2 | Reserved | MCRB.15 | 1 | PDDATDIR | 7 | 15 |

† Bold, italicized pin names indicate pin functions at reset.

‡ Valid only if the I/O function is selected on the pin

§ If the GPIO pin is configured as an output, these bits can be written to. If the pin is configured as an input, these bits are read from.

|| If the DIR bit is 0, the GPIO pin functions as an input. For a value of 1, the pin is configured as an output.

At reset, all LF240x devices come up with the W/R/IOPC0 pin in W/R mode. On devices that lack an external memory interface (e.g., LF2406 and LF2402), W/R mode is not functional and MCRB.0 must be set to a 0 if the IOPC0 pin is to be used.

|| Note that bits 15 through 9 of the MCRB register **must** be written as 1 only. Writing a 0 to any of these bits will cause unpredictable operation of the device.

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description of shared I/O pins (continued)

Table 12. Shared Pin Configurations† (Continued)

| PIN FUNCTION SELECTED | | MUX CONTROL REGISTER (name.bit #) | MUX CONTROL VALUE AT RESET (MCRx.n) | I/O PORT DATA AND DIRECTION‡ | | |
|----------------------------------|---------------------|--|---|------------------------------|---------------|--------------|
| (MCRx.n = 1) Primary Function | (MCRX.N = 0) I/O | | | REGISTER | DATA BIT NO.§ | DIR BIT NO.¶ |
| | | | | PORT E | | |
| CLKOUT | IOPE0 | MCRC.0 | 1 | PEDATDIR | 0 | 8 |
| PWM7 | IOPE1 | MCRC.1 | 0 | PEDATDIR | 1 | 9 |
| PWM8 | IOPE2 | MCRC.2 | 0 | PEDATDIR | 2 | 10 |
| PWM9 | IOPE3 | MCRC.3 | 0 | PEDATDIR | 3 | 11 |
| PWM10 | IOPE4 | MCRC.4 | 0 | PEDATDIR | 4 | 12 |
| PWM11 | IOPE5 | MCRC.5 | 0 | PEDATDIR | 5 | 13 |
| PWM12 | IOPE6 | MCRC.6 | 0 | PEDATDIR | 6 | 14 |
| CAP4/QEP3 | IOPE7 | MCRC.7 | 0 | PEDATDIR | 7 | 15 |
| | | | | PORT F | | |
| CAP5/QEP4 | IOPF0 | MCRC.8 | 0 | PFDATDIR | 0 | 8 |
| CAP6 | IOPF1 | MCRC.9 | 0 | PFDATDIR | 1 | 9 |
| T3PWM/T3CMP | IOPF2 | MCRC.10 | 0 | PFDATDIR | 2 | 10 |
| T4PWM/T4CMP | IOPF3 | MCRC.11 | 0 | PFDATDIR | 3 | 11 |
| TDIRB | IOPF4 | MCRC.12 | 0 | PFDATDIR | 4 | 12 |
| TCLKINB | IOPF5 | MCRC.13 | 0 | PFDATDIR | 5 | 13 |
| Reserved | IOPF6 | MCRC.14 | — | — | — | — |
| Reserved | Reserved | MCRC.15 | — | — | — | — |

† Bold, italicized pin names indicate pin functions at reset.

‡ Valid only if the I/O function is selected on the pin

§ If the GPIO pin is configured as an output, these bits can be written to. If the pin is configured as an input, these bits are read from.

¶ If the DIR bit is 0, the GPIO pin functions as an input. For a value of 1, the pin is configured as an output.

At reset, all LF240x devices come up with the W/R/IOPC0 pin in W/R mode. On devices that lack an external memory interface (e.g., LF2406 and LF2402), W/R mode is not functional and MCRB.0 must be set to a 0 if the IOPC0 pin is to be used.

// Note that bits 15 through 9 of the MCRB register **must** be written as 1 only. Writing a 0 to any of these bits will cause unpredictable operation of the device.

digital I/O control registers

Table 13 lists the registers available in the digital I/O module. As with other 240x peripherals, these registers are memory-mapped to the data space.

Table 13. Addresses of Digital I/O Control Registers

| ADDRESS | REGISTER | NAME |
|---------|----------|--|
| 7090h | MCRA | I/O mux control register A |
| 7092h | MCRB | I/O mux control register B |
| 7094h | MCRC | I/O mux control register C |
| 7095h | PEDATDIR | I/O port E data and direction register |
| 7096h | PFDATDIR | I/O port F data and direction register |
| 7098h | PADATDIR | I/O port A data and direction register |
| 709Ah | PBDATDIR | I/O port B data and direction register |
| 709Ch | PCDATDIR | I/O port C data and direction register |
| 709Eh | PDDATDIR | I/O port D data and direction register |



external memory interface (LF2407)

The TMS320LF2407 can address up to $64K \times 16$ words of memory (or registers) in each of the program, data, and I/O spaces. On-chip memory, when enabled, occupies some of this off-chip range.

The CPU of the TMS320LF2407 schedules a program fetch, data read, and data write on the same machine cycle. This is because from on-chip memory, the CPU can execute all three of these operations in the same cycle. However, the external interface multiplexes the internal buses to one address bus and one data bus. The external interface sequences these operations to complete first the data write, then the data read, and finally the program read.

The LF2407 supports a wide range of system interfacing requirements. Program, data, and I/O address spaces provide interface to memory and I/O, thereby maximizing system throughput. The full 16-bit address and data buses, along with the \overline{PS} , \overline{DS} , and \overline{IS} space-select signals, allow addressing of 64K 16-bit words in program, data, and I/O space. Since on-chip peripheral registers occupy positions of data-memory space (7000–7FFF), the externally addressable data-memory space is 32K 16-bit words (8000–FFFF). Note that the global memory space of the C2xx core is not used for 240x DSP devices. Therefore, the global memory allocation register (GREG) is reserved for all these devices.

Input/output (I/O) design is simplified by having I/O space treated the same way as memory. I/O devices are accessed in the I/O address space using the processor's external address and data buses in the same manner as memory-mapped devices.

The LF2407 external parallel interface provides various control signals to facilitate interfacing to the device. The R/\overline{W} output signal is provided to indicate whether the current cycle is a read or a write. The \overline{STRB} output signal provides a timing reference for all external cycles. For convenience, the device also provides the \overline{RD} and the \overline{WE} output signals, which indicate a read cycle and a write cycle, respectively, along with timing information for those cycles. The availability of these signals minimizes external gating necessary for interfacing external devices to the LF2407.

The 2407 provides \overline{RD} and $\overline{W/R}$ signals to help the zero-wait-state external memory interface. At higher CLKOUT speeds, \overline{RD} may not meet the slow memory device's timing. In such instances, the $\overline{W/R}$ signal could be used as an alternative signal with some tradeoffs. See the timings for details.

The TMS320LF2407 supports zero-wait-state reads on the external interface. However, to avoid bus conflicts, writes take two cycles. This allows the TMS320LF2407 to buffer the transition of the data bus from input to output (or from output to input) by a half cycle. In most systems, the TMS320LF2407 ratio of reads to writes is significantly large to minimize the overhead of the extra cycle on writes.

wait-state generation (LF2407 only)

Wait-state generation is incorporated in the LF2407 without any external hardware for interfacing the LF2407 with slower off-chip memory and I/O devices. Adding wait states lengthens the time the CPU waits for external memory or an external I/O port to respond when the CPU reads from or writes to that external memory or I/O port. Specifically, the CPU waits one extra cycle (one CLKOUT cycle) for every wait state. The wait states operate on CLKOUT cycle boundaries.

To avoid bus conflicts, writes from the LF2407 always take at least two CLKOUT cycles. The LF2407 offers two options for generating wait states:

- **READY Signal.** With the READY signal, you can externally generate any number of wait states. The READY pin has no effect on accesses to *internal* memory.
- **On-Chip Wait-State Generator.** With this generator, you can generate zero to seven wait states.

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generating wait states with the READY signal

When the READY signal is low, the LF2407 waits one CLKOUT cycle and then checks READY again. The LF2407 does not continue executing until the READY signal is driven high; therefore, if the READY signal is not used, it should be pulled high.

The READY pin can be used to generate any number of wait states. However, when the LF2407 operates at full speed, it may not respond fast enough to provide a READY-based wait state for the first cycle. For extended wait states using external READY logic, the on-chip wait-state generator should be programmed to generate at least one wait state.

generating wait states with the LF2407 on-chip software wait-state generator

The software wait-state generator can be programmed to generate zero to seven wait states for a given off-chip memory space (program, data, or I/O), regardless of the state of the READY signal. These zero to seven wait states are controlled by the wait-state generator register (WSGR) (I/O FFFFh). For more detailed information on the WSGR and associated bit functions, refer to the *TMS320LF/LC240x DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357).

watchdog (WD) timer module

The x240x devices include a watchdog (WD) timer module. The WD function of this module monitors software and hardware operation by generating a system reset if it is not periodically serviced by software by having the correct key written. The WD timer operates independently of the CPU. It does not need any CPU initialization to function. When a system reset occurs, the WD timer defaults to the fastest WD timer rate available (WDCLK signal = CLKOUT/512). As soon as reset is released internally, the CPU starts executing code, and the WD timer begins incrementing. This means that, to avoid a premature reset, WD setup should occur early in the power-up sequence. See Figure 14 for a block diagram of the WD module. The WD module features include the following:

- WD Timer
 - Seven different WD overflow rates
 - A WD-reset key (WDKEY) register that clears the WD counter when a correct value is written, and generates a system reset if an incorrect value is written to the register
 - WD check bits that initiate a system reset if an incorrect value is written to the WD control register (WDCR)
- Automatic activation of the WD timer, once system reset is released
 - Three WD control registers located in control register frame beginning at address 7020h.

NOTE: All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte, the upper byte is read as zeros. Writing to the upper byte has no effect.

Figure 14 shows the WD block diagram. Table 14 shows the different WD overflow (time-out) selections.

The watchdog can be disabled in software by writing '1' to bit 6 of the WDCR register (WDCR.6) while bit 5 of the SCSR2 register (SCSR2.5) is 1. If SCSR2.5 is 0, the watchdog will not be disabled. SCSR2.5 is equivalent to the WDDIS pin of the TMS320F243/241 devices.

The diagram shows the Watchdog Reset Logic. It includes a 6-Bit Free-Running Counter, an 8-Bit Watchdog Counter, a Watchdog Reset Key Register, a 55 + AA Detector, and various registers (WDCR.2-0, WDCR.6 WDDIS, WDCR.5-3†, WDFLAG WDCR.7). The logic involves clock division (÷512), counters, and logic gates (AND, OR) to generate the System Reset Request signal.

Figure 14. Block Diagram of the WD Module

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watchdog (WD) timer module (continued)

Table 14. WD Overflow (Time-out) Selections

| WD PRESCALE SELECT BITS | | | WDCLK DIVIDER | WATCHDOG CLOCK RATE† |
|-------------------------|-------|-------|---------------|-------------------------|
| WDPS2 | WDPS1 | WDPS0 | | FREQUENCY (Hz) |
| 0 | 0 | X‡ | 1 | WDCLK/1 |
| 0 | 1 | 0 | 2 | WDCLK/2 |
| 0 | 1 | 1 | 4 | WDCLK/4 |
| 1 | 0 | 0 | 8 | WDCLK/8 |
| 1 | 0 | 1 | 16 | WDCLK/16 |
| 1 | 1 | 0 | 32 | WDCLK/32 |
| 1 | 1 | 1 | 64 | WDCLK/64 |

† WDCLK = CLKOUT/512

‡ X = Don't care

development support

Texas Instruments (TI) offers an extensive line of development tools for the x240x generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of x240x-based applications:

Software Development Tools:

Assembler/linker
Simulator
Optimizing ANSI C compiler
Application algorithms
C/Assembly debugger and code profiler

Hardware Development Tools:

Emulator XDS510™ (supports x24x multiprocessor system debug)
TMS320LF2407 EVM (Evaluation module for 2407 DSP)

The *TMS320 DSP Development Support Reference Guide* (literature number SPRU011) contains information about development support products for all TMS320™ DSP family member devices, including documentation. Refer to this document for further information about TMS320™ DSP documentation or any other TMS320™ DSP support products from Texas Instruments. There is also an additional document, the *TMS320 Third-Party Support Reference Guide* (literature number SPRU052), which contains information from other companies in the industry regarding products related to the TMS320™ DSPs. To receive copies of TMS320™ DSP literature, contact the Literature Response Center at 800-477-8924.

See Table 15 and Table 16 for complete listings of development support tools for the x240x. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

Table 15. Development Support Tools

| DEVELOPMENT TOOL | PLATFORM | PART NUMBER |
|--|-------------------------------------|----------------|
| Software – Code Generation Tools | | |
| Assembler/Linker | PC™, OS/2™, Windows 3.x/Windows™ 95 | TMDS3242850-02 |
| C Compiler/Assembler/Linker | PC, OS/2, Windows 3.x/Windows 95 | TMDS3242855-02 |
| C Compiler/Assembler/Linker | Open Windows, HP9000, SPARC™ | TMDS3242555-08 |
| Software – Simulation | | |
| C2xx Simulator | SPARC, Open Windows | TMDX324x551-09 |
| Software – Emulation Debug Tools | | |
| Code Composer 4.10, Code Generation 7.0 | PC, Windows 3.x, OS/2 | TMDS324012xx |
| TI C Source Debugger – WS | SPARC, SunOS™ | TMDX324062xx |
| Hardware – Emulation Debug Tools | | |
| XDS510XL™ Board (ISA card), w/JTAG cable | PC | TMDS00510 |
| XDS510PP™ Pod (Parallel Port) w/JTAG cable | PC | TMDS00510PP |
| XDS510WS™ Box w/JTAG cable | SPARC | TMDS00510WS |

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XDS510XL, XDS510PP, and XDS510WS are trademarks of Texas Instruments.



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development support (continued)

Table 16. TMS320x24x-Specific Development Tools

| DEVELOPMENT TOOL | PLATFORM | PART NUMBER |
|------------------------------------|-----------------------------|--------------|
| Hardware – Evaluation/Starter Kits | | |
| TMS320LF2407 EVM | PC, Windows 95, Windows™ 98 | TMDX3P701016 |
| TMS320F240 EVM | PC, Windows 3.x | TMDX326P124X |
| TMS320F243 EVM | PC, Windows 95 | TMDS3P604030 |

The LF2407 Evaluation Module (EVM) provide designers of motor and motion control applications with a complete and cost-effective way to take their designs from concept to production. These tools offer both a hardware and software development environment and include:

- Flash-based LF240x evaluation board
- Code Generation Tools
- Assembler/Linker
- C Compiler
- Source code debugger
- C24x™ Debugger
- Code Composer IDE
- XDS510PP™ JTAG-based emulator
- Sample applications code
- Universal 5-V DC power supply
- Documentation and cables

device and development support tool nomenclature

To designate the stages in the product development cycle, Texas Instruments assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS). This development flow is defined below.

Support tool development evolutionary flow:

TMDX Development support product that has not completed TI's internal qualification testing

TMDS Fully qualified development support product

TMX and TMP devices and TMDX development support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

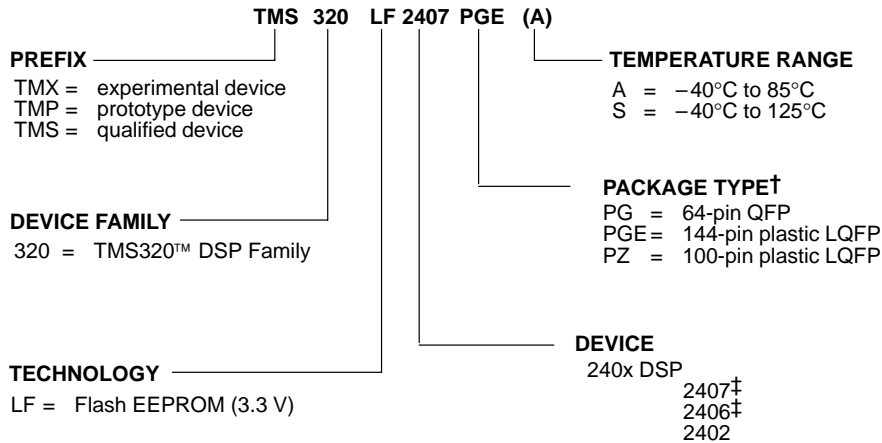
TMS devices and TMDS development support tools have been fully characterized, and the quality and reliability of the device have been fully demonstrated. TI's standard warranty applies.



device and development support tool nomenclature (continued)

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PG, PGE, and PZ) and temperature range (for example, A). Figure 15 provides a legend for reading the complete device name for any TMS320x2xx family member. Refer to the timing section for specific options that are available on 240x devices.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.



† QFP = Quad Flatpack

LQFP = Low-Profile Quad Flatpack

‡ The package dimensions of the 2407 and 2406 devices correspond to the LQFP package. These devices were stated to be in TQFP packaging in the TMX data sheets. The package dimensions have **not** changed; only the package designation has changed.

Figure 15. TMS320LF240x Device Nomenclature

Table 17. Ordering Information

| ORDERABLE DEVICE | PACKAGE | PINS | TEMPERATURE (°C) |
|------------------|---------|------|------------------|
| TMS320LF2407PGEA | PGE | 144 | –40°C to 85°C |
| TMS320LF2407PGES | PGE | 144 | –40°C to 125°C |
| TMS320LF2406PZA | PZ | 100 | –40°C to 85°C |
| TMS320LF2406PZS | PZ | 100 | –40°C to 125°C |
| TMS320LF2402PGA | PG | 64 | –40°C to 85°C |
| TMS320LF2402PGS | PG | 64 | –40°C to 125°C |

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documentation support

Extensive documentation supports all of the TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets, such as this document, with design specifications; complete user's guides for all devices and development support tools; and hardware and software applications. Useful reference documentation includes:

- User Guides
 - *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357)
 - *TMS320C240 DSP Controllers CPU, System, and Instruction Set Reference Guide* (literature number SPRU160)
- Data Sheets
 - *TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP Controllers* (literature number SPRS094)
 - *TMS320LF2407A, TMS320LF2406A, TMS320LF2403A, TMS320LF2402A, TMS320LC2406A, TMS320LC2404A, TMS320LC2402A DSP Controllers* (literature number SPRS145)
- Application Reports
 - *3.3V DSP for Digital Motor Control* (literature number SPRA550)

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Updated information on the TMS320™ DSP controllers can be found on the worldwide web at: <http://www.ti.com>.

To send comments regarding the 240x data sheet (SPRS094), use the comments@books.sc.ti.com email address, which is a repository for feedback. For questions and support, contact the Product Information Center listed at the <http://www.ti.com/sc/docs/pic/home.htm> site.



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absolute maximum ratings over operating free-air temperature ranges (unless otherwise noted)[†]

| | |
|--|------------------|
| Supply voltage range, V_{DD} , PLLVCCA, V_{DDO} , and V_{CCA} (see Note 1) | – 0.3 V to 4.6 V |
| V_{CCP} range | – 0.3 V to 5.5 V |
| Input voltage range, V_{IN} | – 0.3 V to 4.6 V |
| Output voltage range, V_O | – 0.3 V to 4.6 V |
| Input clamp current, I_{IK} ($V_{IN} < 0$ or $V_{IN} > V_{CC}$) | ± 20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 20 mA |
| Operating free-air temperature range, T_A : A version | – 40°C to 85°C |
| S version | – 40°C to 125°C |
| Junction temperature range, T_J | – 40°C to 150°C |
| Storage temperature range, T_{stg} | – 65°C to 150°C |

[†] Clamp current stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions^{‡§}

| | | | MIN | NOM | MAX | UNIT |
|-----------------------------------|--|--|------|-----|------|--------|
| V _{DD} /V _{DDO} | Supply voltage | V _{DDO} = V _{DD} ± 0.3 V | 3 | 3.3 | 3.6 | V |
| V _{SS} | Supply ground | | 0 | 0 | 0 | V |
| PLL _{VCCA} | PLL supply voltage | | 3 | 3.3 | 3.6 | V |
| V _{CCA} [¶] | ADC supply voltage | | 3 | 3.3 | 3.6 | V |
| V _{CCP} | Flash programming supply voltage | | 4.75 | 5 | 5.25 | V |
| f _{CLKOUT} | Device clock frequency (system clock) | | 2 | | 30 | MHz |
| V _{IH} [#] | High-level input voltage | All inputs | 2 | | | V |
| V _{IL} | Low-level input voltage | All inputs | | | 0.8 | V |
| I _{OH} | High-level output source current, V _{OH} = 2.4 V | Output pins Group 1 | | | – 2 | mA |
| | | Output pins Group 2 | | | – 4 | mA |
| | | Output pins Group 3 | | | – 8 | mA |
| I _{OL} | Low-level output sink current, V _{OL} = V _{OL} MAX | Output pins Group 1 | | | 2 | mA |
| | | Output pins Group 2 | | | 4 | mA |
| | | Output pins Group 3 | | | 8 | mA |
| T _A | Free-air temperature | A version | – 40 | | 85 | °C |
| | | S version | – 40 | | 125 | °C |
| T _J | Junction temperature | | – 40 | 25 | 150 | °C |
| N _f | Flash endurance for the array (Write/erase cycles) | – 40°C to 85°C | 100 | 1K | | cycles |

[‡] Refer to the mechanical data package page for thermal resistance values, θ_{JA} (junction-to-ambient) and θ_{JC} (junction-to-case).

[§] The drive strength of the EVA PWM pins and the EVB PWM pins are *not* identical.

[¶] V_{CCA} should not exceed V_{DD} by 0.3 V.

[#] The input buffers used in 240x/240xA are *not* 5-V compatible.

^{||} Primary signals and their groupings:

Group 1: PWM1–PWM6, T1PWM, T2PWM, CAP1–CAP6, TCLKINA, RS, IOPF6, IOPC1, TCK, TDI, TMS, XF, A0–A15

Group 2: PS/DS/IS, RD, W/R, STRB, R/W, VIS_OE, D0–D15, T3PWM, T4PWM, PWM7–PWM12, CANTX, CANRX, SPICLK, SPISOMI, SPISIMO, SPISTE, EMU0, EMU1, TDO, TMS2

Group 3: TDIRA, TDIRB, SCIRXD, SCITXD, XINT1, XINT2, CLKOUT, TCLKINB



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electrical characteristics over recommended operating free-air temperature ranges (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--|--|------------------------|-----|---------|---------|
| V _{OH} | High-level output voltage | V _{DD} = 3.0 V, I _{OH} = I _{OH} MAX | 2.4 | | | V |
| | | All outputs at 50 μ A | V _{DDO} – 0.2 | | | |
| V _{OL} | Low-level output voltage | I _{OL} = I _{OL} MAX | | | 0.4 | V |
| I _{IL} | Input current (low level) | V _{DD} = 3.3 V, V _{IN} = 0 V | –9 | –16 | –25 | μ A |
| | | | | | | |
| I _{IH} | Input current (high level) | V _{DD} = 3.3 V, V _{IN} = V _{DD} | 9 | 16 | 25 | μ A |
| | | | | | | |
| I _{OZ} | Output current, high-impedance state (off-state) | V _O = V _{DD} or 0 V | | | \pm 2 | μ A |
| C _i | Input capacitance | | | 2 | | pF |
| C _O | Output capacitance | | | 3 | | pF |

current consumption by power-supply pins over recommended operating free-air temperature ranges at 30-MHz CLOCKS (TMS320LF2407)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---------------------|---|-----|-----|-----|------|
| I _{DD} [†] | Operational Current | Clock to all peripherals is enabled. CPU is running a simple loop code and no I/O pins are switching. | | 75 | 100 | mA |
| I _{CCA} | ADC module current | | | 5 | 15 | mA |

[†] I_{DD} is the current flowing into the V_{DD}, V_{DDO}, and PLLV_{CCA} pins.

current consumption by power-supply pins over recommended operating free-air temperature ranges at 30-MHz CLOCKS (TMS320LF2406)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---------------------|---|-----|-----|-----|------|
| I _{DD} [†] | Operational Current | Clock to all peripherals is enabled. CPU is running a simple loop code and no I/O pins are switching. | | 75 | 100 | mA |
| I _{CCA} | ADC module current | | | 5 | 15 | mA |

[†] I_{DD} is the current flowing into the V_{DD}, V_{DDO}, and PLLV_{CCA} pins.

current consumption by power-supply pins over recommended operating free-air temperature ranges at 30-MHz CLOCKS (TMS320LF2402)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|---------------------|---|-----|-----|-----|------|
| I _{DD} [†] | Operational Current | Clock to all peripherals is enabled. CPU is running a simple loop code and no I/O pins are switching. | | 65 | 90 | mA |
| I _{CCA} | ADC module current | | | 5 | 15 | mA |

[†] I_{DD} is the current flowing into the V_{DD}, V_{DDO}, and PLLV_{CCA} pins.



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current consumption by power-supply pins over recommended operating free-air temperature ranges during low-power modes at 30-MHz CLOCKOUT (TMS320LF2407)

| PARAMETER | MODE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|------|---|-----|-----|-----|------|
| I_{DD}^{\dagger} Operational Current | LPM0 | Clock to all peripherals is enabled. No I/O pins are switching. | | 60 | 80 | mA |
| I_{CCA} ADC module current | | | | 0.2 | 1 | mA |
| I_{DD}^{\dagger} Operational Current | LPM1 | Clock to all peripherals is disabled. No I/O pins are switching. | | 40 | 60 | mA |
| I_{CCA} ADC module current | | | | 0 | 0 | mA |
| I_{DD}^{\dagger} Operational Current | LPM2 | Clock to all peripherals is disabled. | | 10 | 30 | mA |
| I_{CCA} ADC module current | | | | 0 | 0 | mA |

$\dagger I_{DD}$ is the current flowing into the V_{DD} , V_{DDO} , and PLL_{VCCA} pins.

current consumption by power-supply pins over recommended operating free-air temperature ranges during low-power modes at 30-MHz CLOCKOUT (TMS320LF2406)

| PARAMETER | MODE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|------|---|-----|-----|-----|------|
| I_{DD}^{\dagger} Operational Current | LPM0 | Clock to all peripherals is enabled. No I/O pins are switching. | | 60 | 80 | mA |
| I_{CCA} ADC module current | | | | 0.2 | 1 | mA |
| I_{DD}^{\dagger} Operational Current | LPM1 | Clock to all peripherals is disabled. No I/O pins are switching. | | 40 | 60 | mA |
| I_{CCA} ADC module current | | | | 0 | 0 | mA |
| I_{DD}^{\dagger} Operational Current | LPM2 | Clock to all peripherals is disabled. | | 10 | 30 | mA |
| I_{CCA} ADC module current | | | | 0 | 0 | mA |

$\dagger I_{DD}$ is the current flowing into the V_{DD} , V_{DDO} , and PLL_{VCCA} pins.

current consumption by power-supply pins over recommended operating free-air temperature ranges during low-power modes at 30-MHz CLOCKOUT (TMS320LF2402)

| PARAMETER | MODE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|------|---|-----|-----|-----|------|
| I_{DD}^{\dagger} Operational Current | LPM0 | Clock to all peripherals is enabled. No I/O pins are switching. | | 50 | 70 | mA |
| I_{CCA} ADC module current | | | | 0.2 | 1 | mA |
| I_{DD}^{\dagger} Operational Current | LPM1 | Clock to all peripherals is disabled. No I/O pins are switching. | | 40 | 60 | mA |
| I_{CCA} ADC module current | | | | 0 | 0 | mA |
| I_{DD}^{\dagger} Operational Current | LPM2 | Clock to all peripherals is disabled. | | 10 | 30 | mA |
| I_{CCA} ADC module current | | | | 0 | 0 | mA |

$\dagger I_{DD}$ is the current flowing into the V_{DD} , V_{DDO} , and PLL_{VCCA} pins.



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current consumption graph

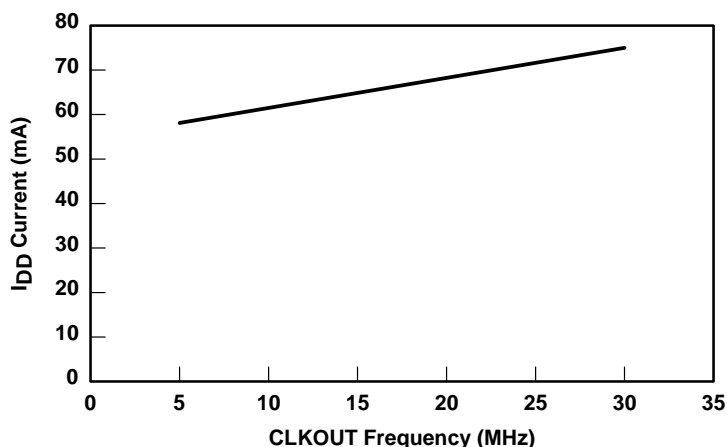


Figure 16. LF2407 Typical Current Consumption (With Peripheral Clocks Enabled)

reducing current consumption

240x DSPs incorporate a unique method to reduce the device current consumption. A reduction in current consumption can be achieved by turning off the clock to any peripheral module which is not used in a given application. Table 18 indicates the typical reduction in current consumption achieved by turning off the clocks to various peripherals. Refer to the *TMS320LF/LC240x DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357) for further information on how to turn off the clock to the peripherals.

Table 18. Typical Current Consumption by Various Peripherals (at 30 MHz)

| PERIPHERAL MODULE | CURRENT REDUCTION (mA) |
|-------------------|------------------------|
| CAN | 6.3 |
| EVA | 4.6 |
| EVB | 4.6 |
| ADC | 2.8 |
| SCI | 1.4 |
| SPI | 1.0 |

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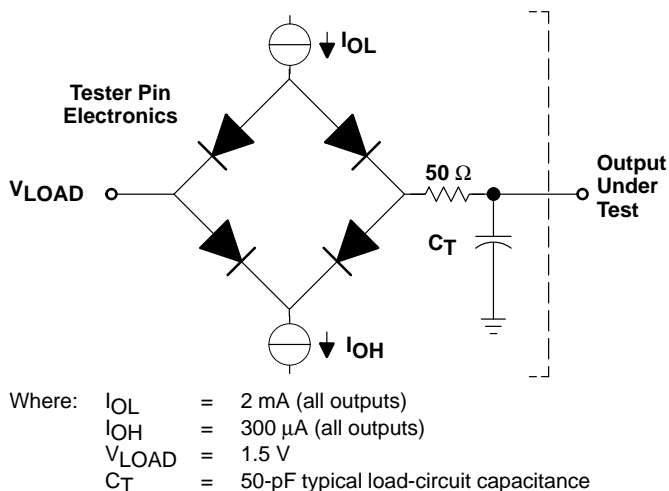


Figure 17. Test Load Circuit

signal transition levels

The data in this section is shown for the 3.3-V version. Note that some of the signals use different reference voltages, see the recommended operating conditions table. Output levels are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.8 V.

Figure 18 shows output levels.

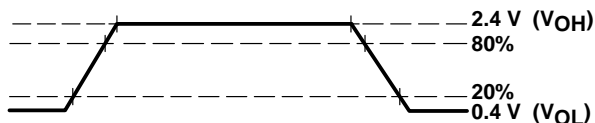


Figure 18. Output Levels

Output transition times are specified as follows:

- For a *high-to-low transition*, the level at which the output is said to be no longer high is below 80% of the total voltage range and lower and the level at which the output is said to be low is 20% of the total voltage range and lower.
- For a *low-to-high transition*, the level at which the output is said to be no longer low is 20% of the total voltage range and higher and the level at which the output is said to be high is 80% of the total voltage range and higher.

Figure 19 shows the input levels.

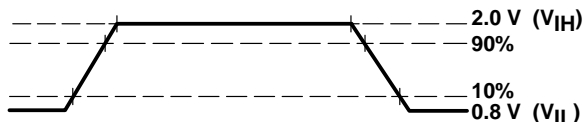


Figure 19. Input Levels

Input transition times are specified as follows:

- For a *high-to-low transition* on an input signal, the level at which the input is said to be no longer high is 90% of the total voltage range and lower and the level at which the input is said to be low is 10% of the total voltage range and lower.
- For a *low-to-high transition* on an input signal, the level at which the input is said to be no longer low is 10% of the total voltage range and higher and the level at which the input is said to be high is 90% of the total voltage range and higher.

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timing parameter symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

| | | | |
|-----|--------------|----|---|
| A | A[15:0] | MS | Memory strobe pins \overline{IS} , \overline{DS} , or \overline{PS} |
| CI | XTAL1/CLKIN | R | READY |
| CO | CLKOUT | RD | Read cycle or \overline{RD} |
| D | D[15:0] | RS | RESET pin \overline{RS} |
| INT | XINT1, XINT2 | W | Write cycle or \overline{WE} |

Lowercase subscripts and their meanings:

| | |
|----|------------------------|
| a | access time |
| c | cycle time (period) |
| d | delay time |
| f | fall time |
| h | hold time |
| r | rise time |
| su | setup time |
| t | transition time |
| v | valid time |
| w | pulse duration (width) |

Letters and symbols and their meanings:

| | |
|---|--|
| H | High |
| L | Low |
| V | Valid |
| X | Unknown, changing, or don't care level |
| Z | High impedance |

general notes on timing parameters

All output signals from the 240x devices (including CLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, refer to the appropriate cycle description section of this data sheet.



external reference crystal/clock with PLL circuit enabled

timings with the PLL circuit enabled

| PARAMETER | | MIN | MAX | UNIT |
|-----------|-----------|-----|-----|------|
| f_x | Resonator | 4 | 13 | MHz |
| | Crystal | 4 | 20 | |
| | CLKIN | 4 | 20 | |

† Input frequency should be adjusted (CLK PS bits in SCSR1 register) such that CLKOUT = 30 MHz maximum, 4 MHz minimum.

switching characteristics over recommended operating conditions [$H = 0.5 t_{c(CO)}$] (see Figure 20)

| PARAMETER | PLL MODE | MIN | TYP | MAX | UNIT |
|--|------------------|-----|-----|------------------|------|
| $t_{c(CO)}$ Cycle time, CLKOUT | $\times 4$ mode† | 33 | | | ns |
| $t_f(CO)$ Fall time, CLKOUT | | | 4 | | ns |
| $t_r(CO)$ Rise time, CLKOUT | | | 4 | | ns |
| $t_w(COL)$ Pulse duration, CLKOUT low | | H–3 | H | H+3 | ns |
| $t_w(COH)$ Pulse duration, CLKOUT high | | H–3 | H | H+3 | ns |
| t_t Transition time, PLL synchronized after \overline{RS} pin high | | | | $4096 t_{c(CI)}$ | ns |

† Input frequency should be adjusted (CLK PS bits in SCSR1 register) such that CLKOUT = 30 MHz maximum, 4 MHz minimum.

timing requirements (see Figure 20)

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_{c(CI)}$ Cycle time, XTAL1/CLKIN | | 250 | ns |
| $t_f(CI)$ Fall time, XTAL1/CLKIN | | 5 | ns |
| $t_r(CI)$ Rise time, XTAL1/CLKIN | | 5 | ns |
| $t_w(CIL)$ Pulse duration, XTAL1/CLKIN low as a percentage of $t_{c(CI)}$ | 40 | 60 | % |
| $t_w(CIH)$ Pulse duration, XTAL1/CLKIN high as a percentage of $t_{c(CI)}$ | 40 | 60 | % |

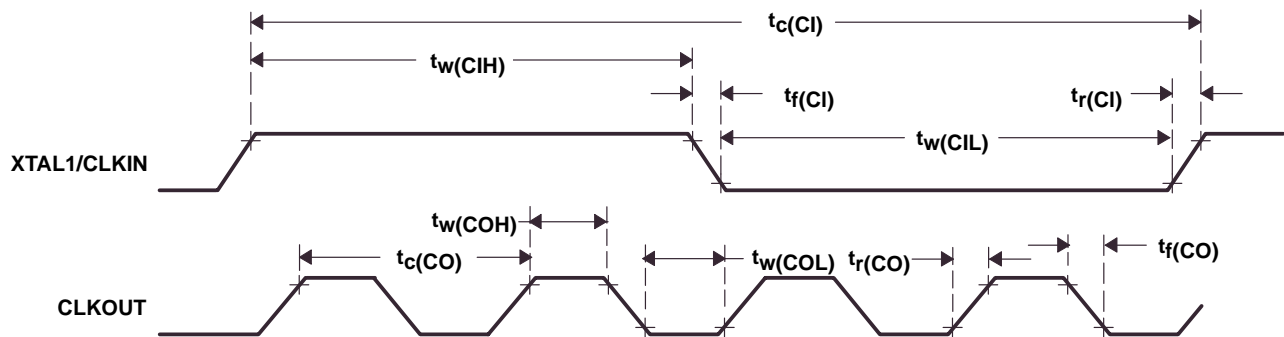


Figure 20. CLKIN-to-CLKOUT Timing with PLL and External Clock in $\times 4$ Mode

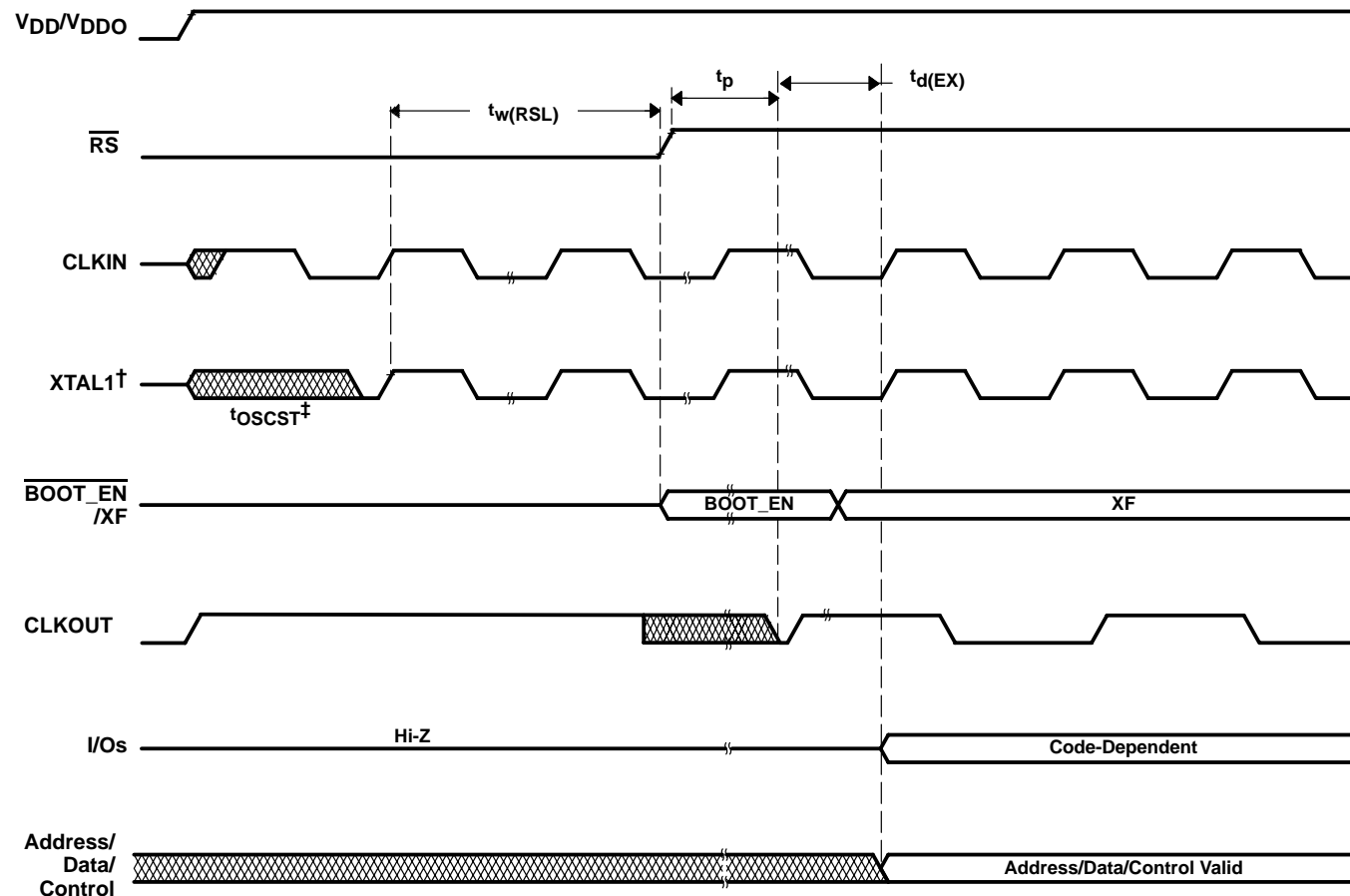
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$\overline{\text{RS}}$ timings

timing requirements for a reset [$H = 0.5t_{c(CO)}$] (see Figure 21 and Figure 22)

| | | MIN | NOM | MAX | UNIT |
|---------------|---|--------------|-----|-----------------|--------|
| $t_{w(RSL)}$ | Pulse duration, stable CLKIN to $\overline{\text{RS}}$ high | $8t_{c(CI)}$ | | | cycles |
| $t_{w(RSL2)}$ | Pulse duration, $\overline{\text{RS}}$ low | $8t_{c(CI)}$ | | | cycles |
| t_p | PLL lock-up time | | | $4096t_{c(CI)}$ | cycles |
| $t_d(EX)$ | Delay time, reset vector executed after PLL lock time | | 36H | | ns |

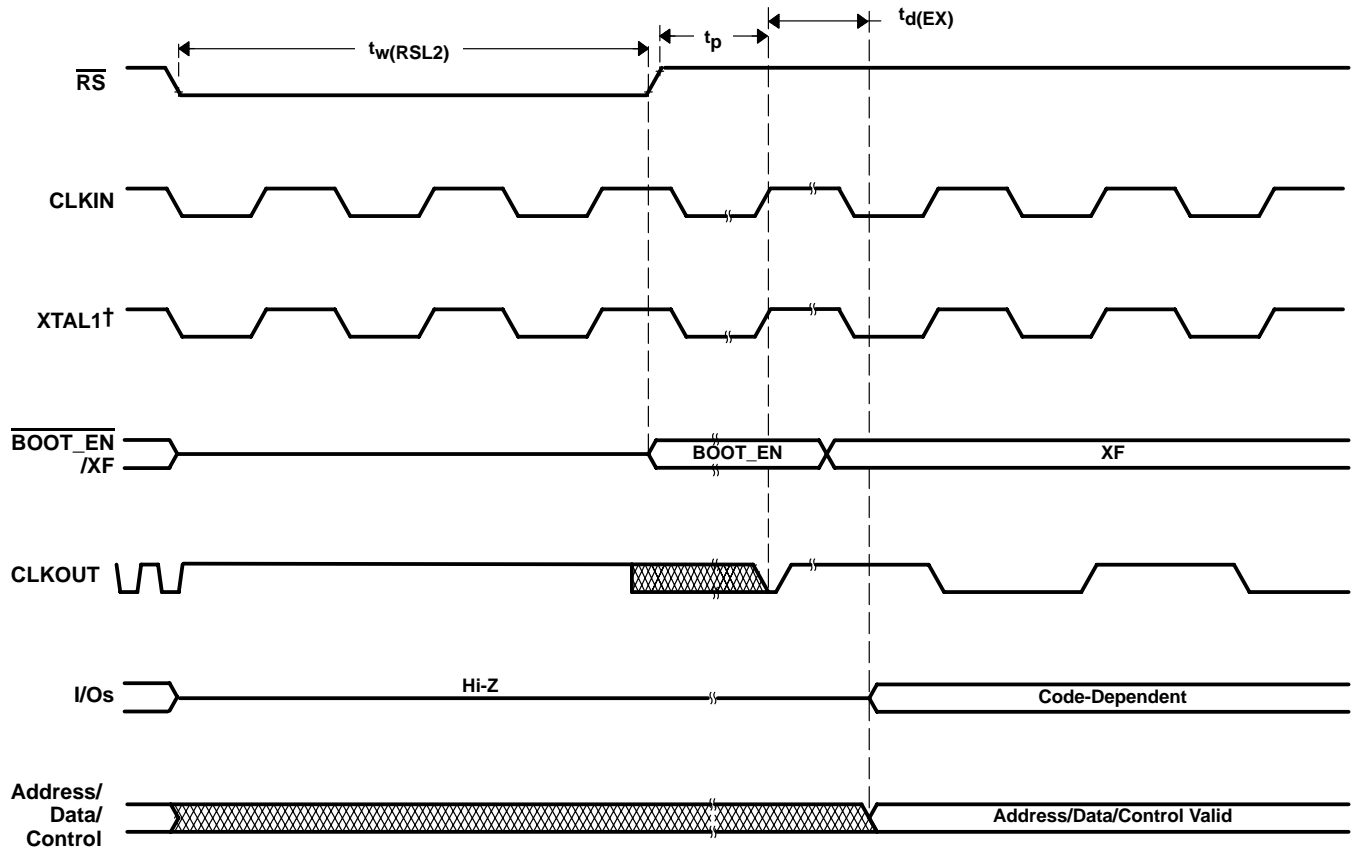


† XTAL1 refers to internal oscillator clock if on-chip oscillator is used.

‡ t_{OSCST} is the oscillator start-up time, which is dependent on crystal/resonator and board design.

Figure 21. Power-on Reset

RS timings (continued)



† XTAL1 refers to internal oscillator clock if on-chip oscillator is used.

Figure 22. Warm Reset

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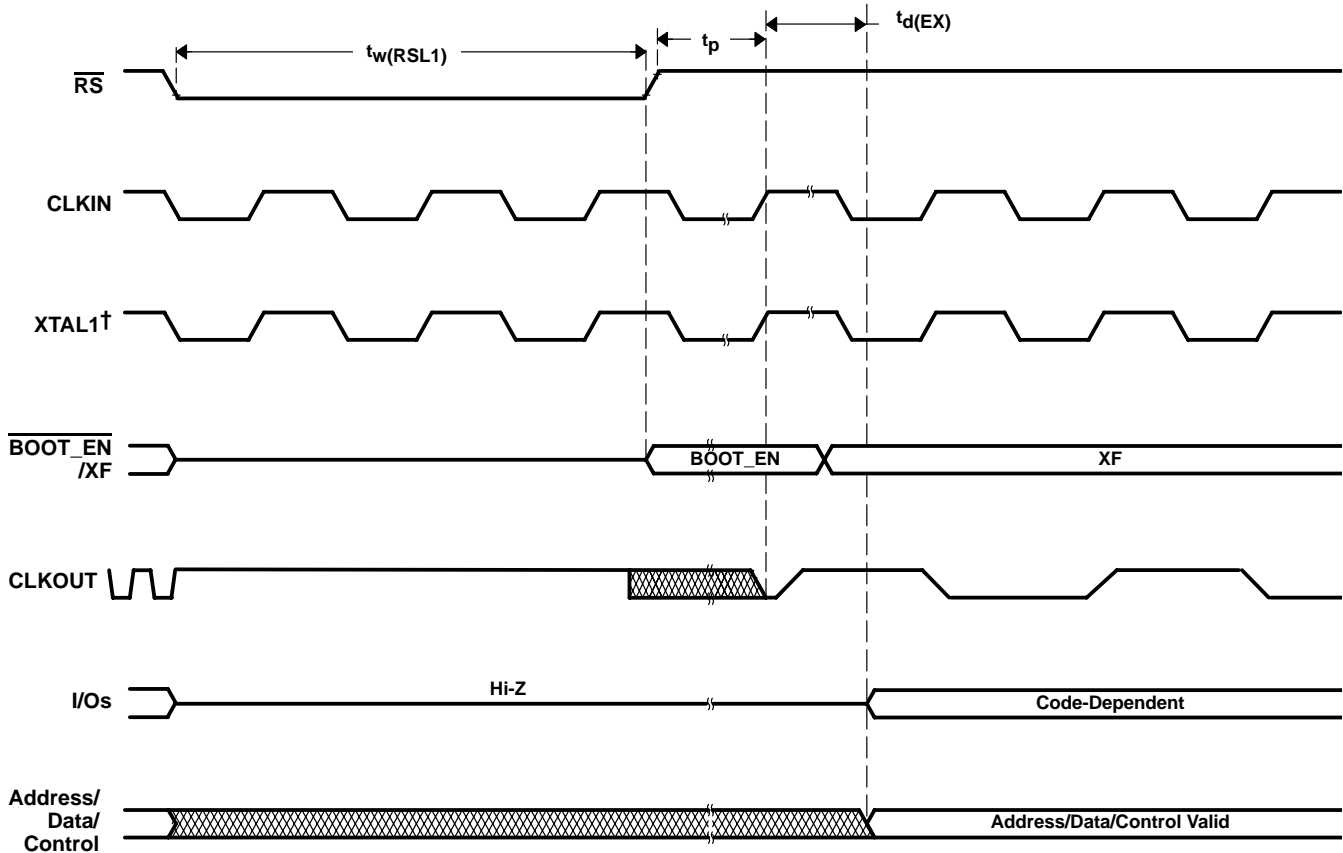
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RS timings (continued)

switching characteristics over recommended operating conditions for a reset [$H = 0.5t_{c(CO)}$]
(see Figure 23)

| PARAMETER | | MIN | MAX | UNIT |
|---------------|---|----------------|-----------------|------|
| $t_{w(RSL1)}$ | Pulse duration, \overline{RS} low† | $128t_{c(CI)}$ | | ns |
| $t_d(EX)$ | Delay time, reset vector executed after PLL lock time | 36H | | ns |
| t_p | PLL lock time (input cycles) | | $4096t_{c(CI)}$ | ns |

† The parameter $t_{w(RSL1)}$ refers to the time \overline{RS} is an output.



† XTAL1 refers to internal oscillator clock if on-chip oscillator is used.

Figure 23. Watchdog Initiated Reset

low-power mode timings

switching characteristics over recommended operating conditions [$H = 0.5t_{c(CO)}$]
(see Figure 24, Figure 25, and Figure 26)

| PARAMETER | | LOW-POWER MODES | | MIN | TYP | MAX | UNIT |
|---------------------------|---|------------------------------|------|--------------------------------|-----|-----|------|
| t _d (WAKE-A) | Delay time, CLKOUT switching to program execution resume | IDLE1 | LPM0 | 12 × t _c (CO) | | | ns |
| | | IDLE2 | LPM1 | 15 × t _c (CO) | | | |
| t _d (IDLE-COH) | Delay time, Idle instruction executed to CLKOUT high | IDLE2 | LPM1 | 4t _c (CO) | | | ns |
| t _d (WAKE-OSC) | Delay time, wakeup interrupt asserted to oscillator running | HALT {PLL/OSC power down} | LPM2 | OSC start-up and PLL lock time | | | ms |
| t _d (IDLE-OSC) | Delay time, Idle instruction executed to oscillator power off | | | 4t _c (CO) | | | ns |
| t _d (EX) | Delay time, reset vector executed after \overline{RS} high | | | 36H | | | ns |

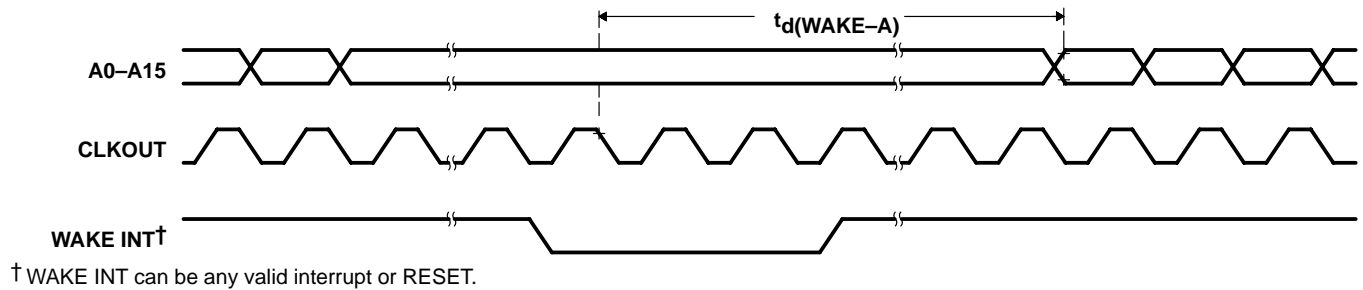


Figure 24. IDLE1 Entry and Exit Timing – LPM0

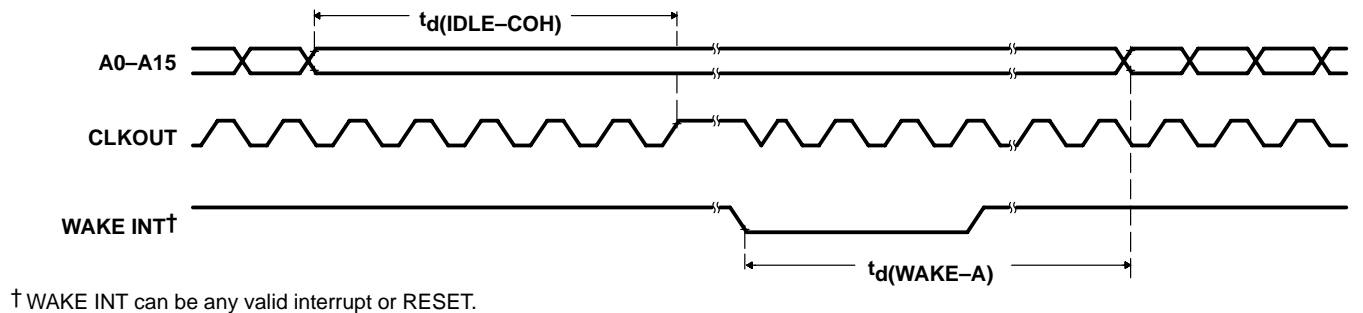


Figure 25. IDLE2 Entry and Exit Timing – LPM1

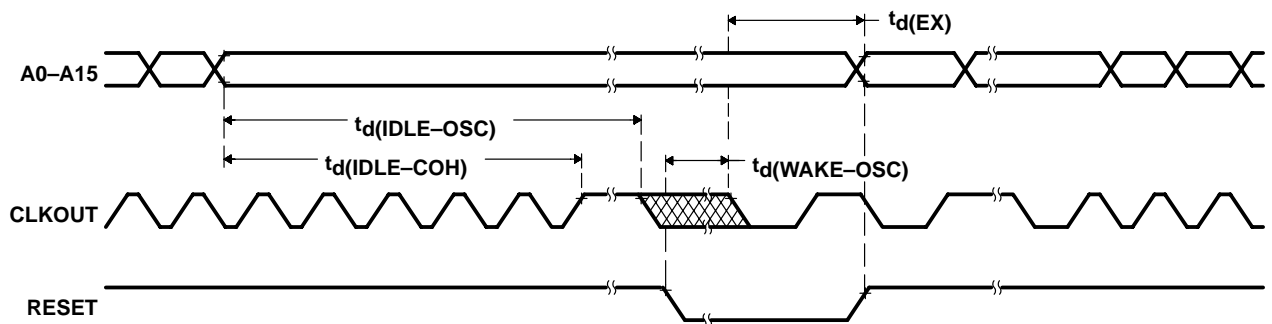


Figure 26. HALT Mode – LPM2

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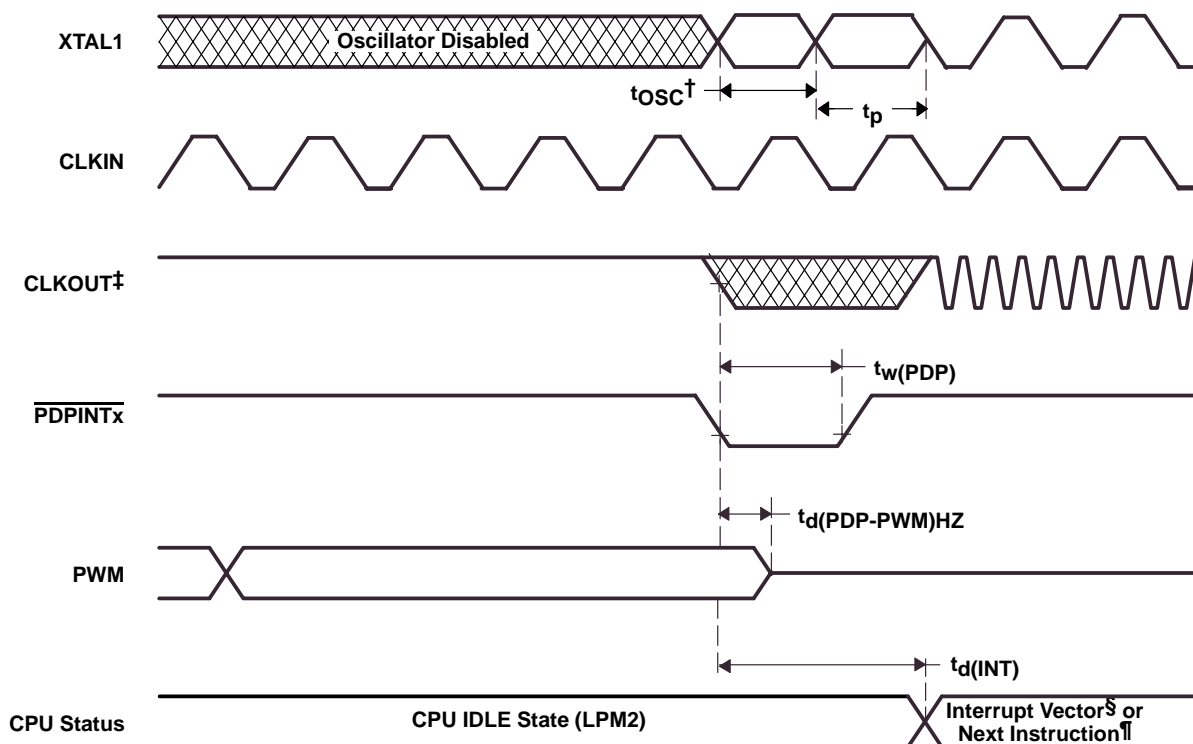
LPM2 wakeup timings

switching characteristics over recommended operating conditions (see Figure 27)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------------------------|---|-----------------------------|-----|------|
| $t_d(\text{PDP-PWM})_{\text{HZ}}$ | Delay time, $\overline{\text{PDPINTx}}$ low to PWM high-impedance state | | 12 | ns |
| $t_d(\text{INT})$ | Delay time, INT low/high to interrupt-vector fetch | $10t_{\text{C}}(\text{CO})$ | | ns |

timing requirements [$H = 0.5t_{\text{C}}(\text{CO})$] (see Figure 27)

| | MIN | NOM | MAX | UNIT |
|-------------------|-----|---------|-------------------------------|--------|
| $t_w(\text{INT})$ | | $2H+15$ | | ns |
| $t_w(\text{PDP})$ | | $4H+5$ | | ns |
| t_p | | | $4096t_{\text{C}}(\text{CI})$ | cycles |



$\dagger t_{\text{OSC}}$ is the oscillator start-up time.

\ddagger CLKOUT frequency after LPM2 wakeup will be the same as that upon entering LPM2 (x4 shown as an example).

\S PDPINTx interrupt vector, if PDPINTx interrupt is enabled.

\P If PDPINTx interrupt is disabled.

Figure 27. LPM2 Wakeup Using $\overline{\text{PDPINTx}}$

XF, $\overline{\text{BIO}}$, and $\text{MP}/\overline{\text{MC}}$ timings

switching characteristics over recommended operating conditions (see Figure 28)

| PARAMETER | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_d(\text{XF})$ Delay time, CLKOUT high to XF high/low | -3 | 7 | ns |

timing requirements (see Figure 28)

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_{\text{su}}(\text{BIO})\text{CO}$ Setup time, $\overline{\text{BIO}}$ or $\text{MP}/\overline{\text{MC}}$ low before CLKOUT low | 0 | | ns |
| $t_{\text{h}}(\text{BIO})\text{CO}$ Hold time, $\overline{\text{BIO}}$ or $\text{MP}/\overline{\text{MC}}$ low after CLKOUT low | 19 | | ns |

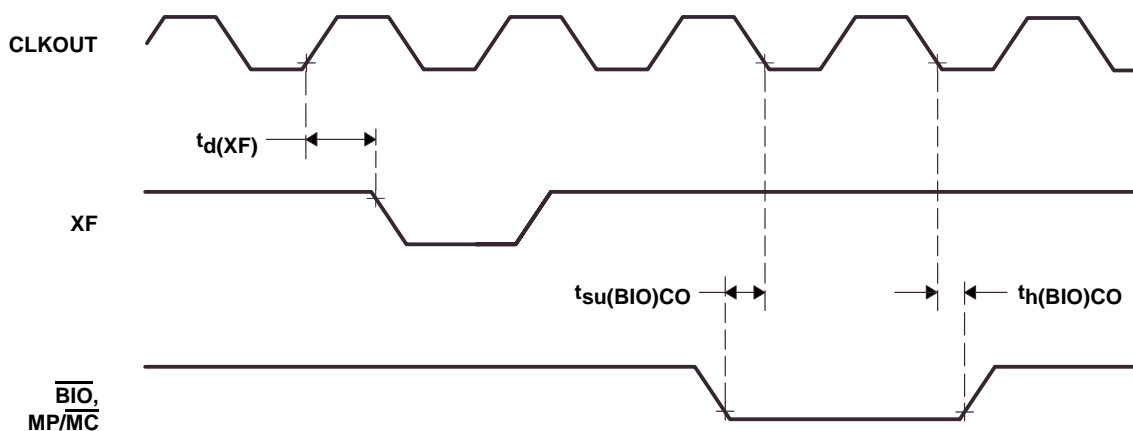


Figure 28. XF and $\overline{\text{BIO}}$ Timing

TIMING EVENT MANAGER INTERFACE

PWM timings

PWM refers to all PWM outputs on EVA and EVB.

switching characteristics over recommended operating conditions for PWM timing
[H = 0.5t_{c(CO)}] (see Figure 29)

| PARAMETER | | MIN | MAX | UNIT |
|----------------------------------|---|------|-----|------|
| t _{w(PWM)} [†] | Pulse duration, PWMx output high/low | 2H+5 | | ns |
| t _{d(PWM)CO} | Delay time, CLKOUT low to PWMx output switching | | 15 | ns |

[†] PWM outputs may be 100%, 0%, or increments of t_{c(CO)} with respect to the PWM period.

timing requirements[‡] [H = 0.5t_{c(CO)}] (see Figure 30)

| | | MIN | MAX | UNIT |
|-------------------------|--|------------------------|-----|------|
| t _{w(TMRDIR)} | Pulse duration, TMRDIR low/high | 4H+5 | | ns |
| t _{w(TMRCLK)} | Pulse duration, TMRCLK low as a percentage of TMRCLK cycle time | 40 | 60 | % |
| t _{wh(TMRCLK)} | Pulse duration, TMRCLK high as a percentage of TMRCLK cycle time | 40 | 60 | % |
| t _{c(TMRCLK)} | Cycle time, TMRCLK | 4 × t _{c(CO)} | | ns |

[‡] Parameter TMRDIR is equal to the pin TDIRx, and parameter TMRCLK is equal to the pin TCLKINx.

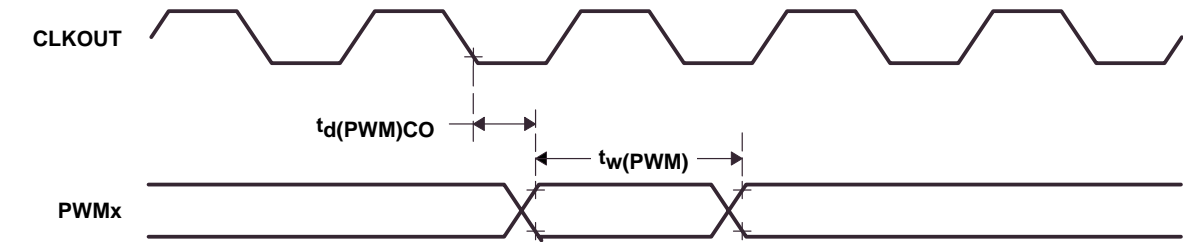
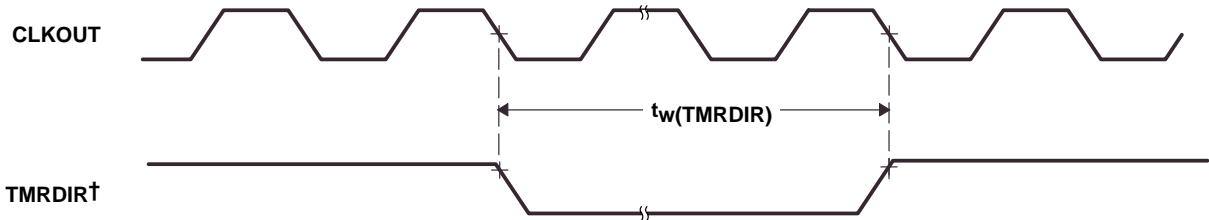


Figure 29. PWM Output Timing



[†] Parameter TMRDIR is equal to the pin TDIRx.

Figure 30. Capture/TMRDIR Timing

capture and QEP timings

CAP refers to all QEP and capture input pins.

timing requirements [$H = 0.5t_{c(CO)}$] (see Figure 31)

| | MIN | MAX | UNIT |
|--|--------|-----|------|
| $t_w(CAP)$ Pulse duration, CAPx input low/high | 4H +15 | | ns |

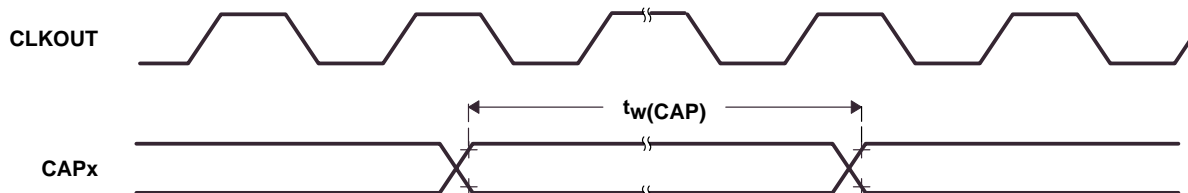


Figure 31. Capture Input and QEP Timing

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interrupt timings

INT refers to XINT1 and XINT2. PDP refers to $\overline{\text{PDPINTx}}$.

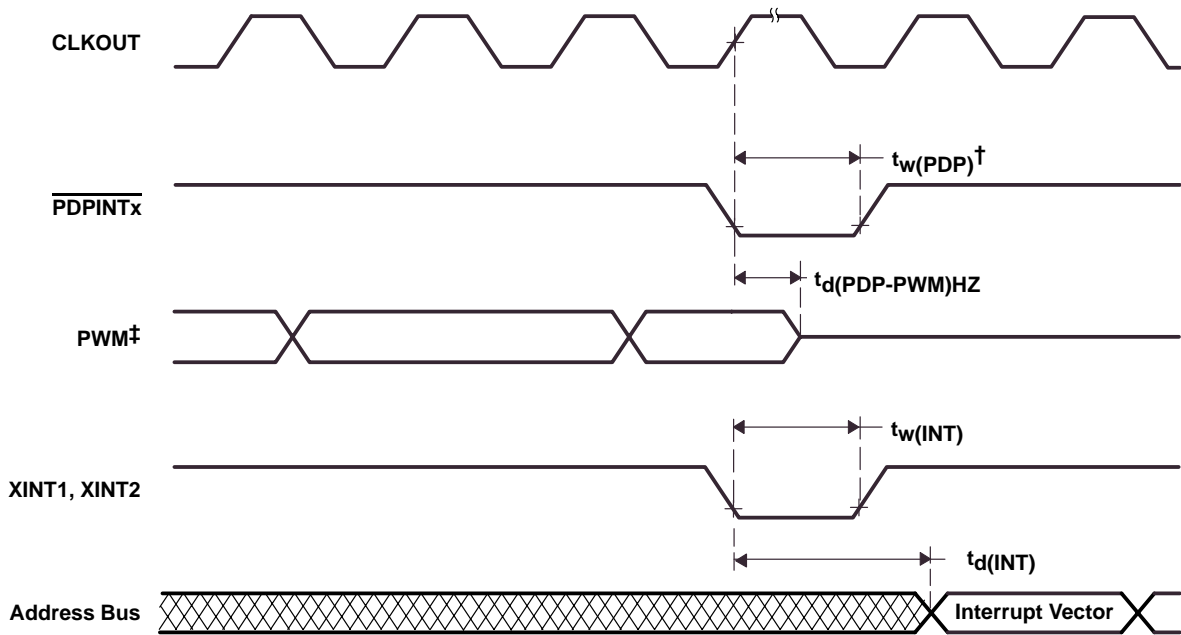
switching characteristics over recommended operating conditions (see Figure 32)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------------------------|---|--------------------|-----|------|
| $t_d(\text{PDP-PWM})_{\text{HZ}}$ | Delay time, $\overline{\text{PDPINTx}}$ low to PWM high-impedance state | | 12 | ns |
| $t_d(\text{INT})$ | Delay time, INT low/high to interrupt-vector fetch | $10t_c(\text{CO})$ | | ns |

timing requirements [$H = 0.5t_c(\text{CO})$] (see Figure 32)

| | MIN | NOM | MAX | UNIT |
|---------------------------|---|-----|-----|------|
| $t_w(\text{INT})$ | Pulse duration, INT input low/high | | | ns |
| $t_w(\text{PDP})^\dagger$ | Pulse duration, $\overline{\text{PDPINTx}}$ input low | | | ns |

† To maintain compatibility with 240xA and other future devices, it is suggested that $\overline{\text{PDPINTx}}$ be driven low for a minimum of 7 or 13 CLKOUT cycles. See SPRS145 for more details.



† To maintain compatibility with 240xA and other future devices, it is suggested that $\overline{\text{PDPINTx}}$ be driven low for a minimum of 7 or 13 CLKOUT cycles. See SPRS145 for more details.

‡ PWM refers to all the PWM pins in the device (i.e., PWMn and TnPWM pins). The state of the PWM pins after $\overline{\text{PDPINTx}}$ is taken high depends on the state of the FCOMPOE bit.

Figure 32. External Interrupts Timing

general-purpose input/output timings

switching characteristics over recommended operating conditions (see Figure 33)

| PARAMETER | | | MIN | MAX | UNIT |
|----------------|---|-----------|-----|-----|------|
| $t_{d(GPO)CO}$ | Delay time, CLKOUT low to GPIO low/high | All GPIOs | | 9 | ns |
| $t_r(GPO)$ | Rise time, GPIO switching low to high | All GPIOs | | 8 | ns |
| $t_f(GPO)$ | Fall time, GPIO switching high to low | All GPIOs | | 6 | ns |

timing requirements [$H = 0.5t_{c(CO)}$] (see Figure 34)

| | | | MIN | MAX | UNIT |
|------------|------------------------------|--|---------|-----|------|
| $t_w(GPI)$ | Pulse duration, GPI high/low | | $2H+15$ | | ns |

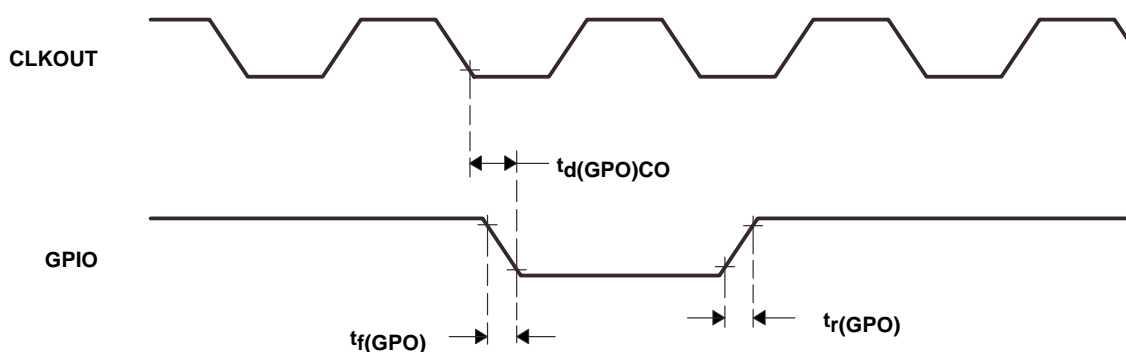


Figure 33. General-Purpose Output Timing

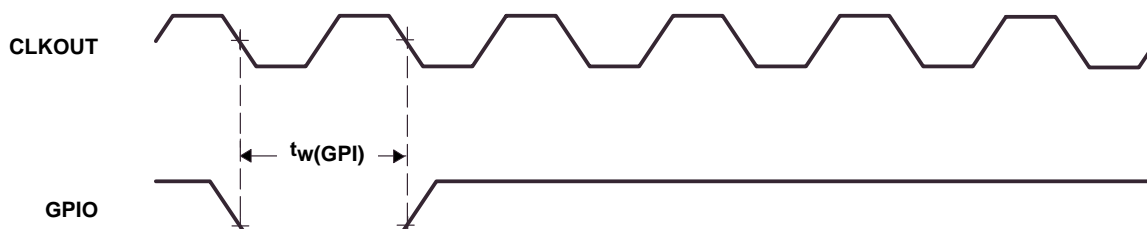


Figure 34. General-Purpose Input Timing

SPI MASTER MODE TIMING PARAMETERS

SPI master mode timing information is listed in the following tables.

SPI master mode external timing parameters (clock phase = 0)^{†‡} (see Figure 35)

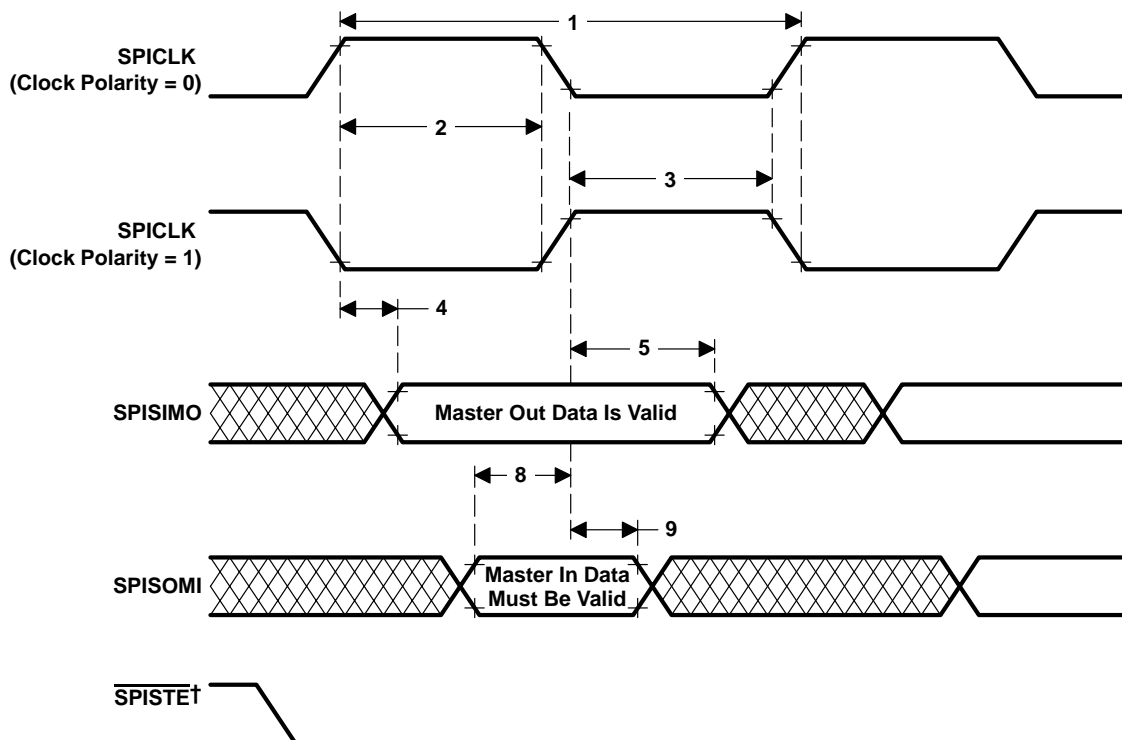
| NO. | | | SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2 | | SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3 | | UNIT |
|-----|------------------------------|--|---|------------------------|---|--|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_c(\text{SPC})_M$ | Cycle time, SPICLK | $4t_c(\text{CO})$ | $128t_c(\text{CO})$ | $5t_c(\text{CO})$ | $127t_c(\text{CO})$ | ns |
| 2§ | $t_w(\text{SPCH})_M$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_c(\text{SPC})_M - 10$ | $0.5t_c(\text{SPC})_M$ | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO}) - 10$ | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO})$ | ns |
| | $t_w(\text{SPCL})_M$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_c(\text{SPC})_M - 10$ | $0.5t_c(\text{SPC})_M$ | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO}) - 10$ | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO})$ | |
| 3§ | $t_w(\text{SPCL})_M$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_c(\text{SPC})_M - 10$ | $0.5t_c(\text{SPC})_M$ | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO}) - 10$ | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO})$ | ns |
| | $t_w(\text{SPCH})_M$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_c(\text{SPC})_M - 10$ | $0.5t_c(\text{SPC})_M$ | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO}) - 10$ | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO})$ | |
| 4§ | $t_d(\text{SPCH-SIMO})_M$ | Delay time, SPICLK high to SPISIMO valid (clock polarity = 0) | - 10 | 10 | - 10 | 10 | ns |
| | $t_d(\text{SPCL-SIMO})_M$ | Delay time, SPICLK low to SPISIMO valid (clock polarity = 1) | - 10 | 10 | - 10 | 10 | |
| 5§ | $t_v(\text{SPCL-SIMO})_M$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0) | $0.5t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO}) - 10$ | | ns |
| | $t_v(\text{SPCH-SIMO})_M$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1) | $0.5t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO}) - 10$ | | |
| 8§ | $t_{su}(\text{SOMI-SPCL})_M$ | Setup time, SPISOMI before SPICLK low (clock polarity = 0) | 0 | | 0 | | ns |
| | $t_{su}(\text{SOMI-SPCH})_M$ | Setup time, SPISOMI before SPICLK high (clock polarity = 1) | 0 | | 0 | | |
| 9§ | $t_v(\text{SPCL-SOMI})_M$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0) | $0.25t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO}) - 10$ | | ns |
| | $t_v(\text{SPCH-SOMI})_M$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1) | $0.25t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO}) - 10$ | | |

[†] The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.

[‡] t_c = system clock cycle time = $1/\text{CLKOUT} = t_c(\text{CO})$

[§] The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

PARAMETER MEASUREMENT INFORMATION



† The $\overline{\text{SPISTET}}$ signal must be active before the SPI communication stream starts; the $\overline{\text{SPISTET}}$ signal must remain active until the SPI communication stream is complete.

Figure 35. SPI Master Mode External Timing (Clock Phase = 0)

SPI master mode external timing parameters (clock phase = 1)^{†‡} (see Figure 36)

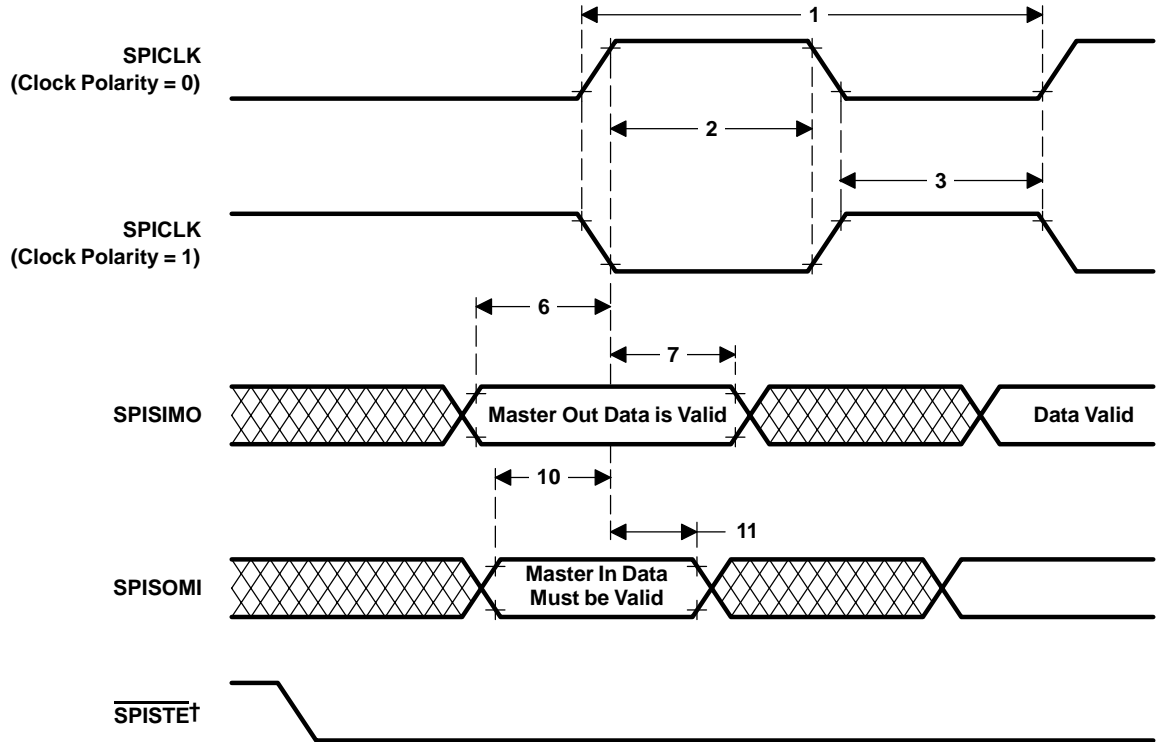
| NO. | | | SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2 | | SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3 | | UNIT |
|-----|------------------------------|--|---|------------------------|---|--|------|
| | | | MIN | MAX | MIN | MAX | |
| 1 | $t_c(\text{SPC})_M$ | Cycle time, SPICLK | $4t_c(\text{CO})$ | $128t_c(\text{CO})$ | $5t_c(\text{CO})$ | $127t_c(\text{CO})$ | ns |
| 2§ | $t_w(\text{SPCH})_M$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_c(\text{SPC})_M - 10$ | $0.5t_c(\text{SPC})_M$ | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO}) - 10$ | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO})$ | ns |
| | $t_w(\text{SPCL})_M$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_c(\text{SPC})_M - 10$ | $0.5t_c(\text{SPC})_M$ | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO}) - 10$ | $0.5t_c(\text{SPC})_M - 0.5t_c(\text{CO})$ | |
| 3§ | $t_w(\text{SPCL})_M$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_c(\text{SPC})_M - 10$ | $0.5t_c(\text{SPC})_M$ | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO}) - 10$ | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO})$ | ns |
| | $t_w(\text{SPCH})_M$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_c(\text{SPC})_M - 10$ | $0.5t_c(\text{SPC})_M$ | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO}) - 10$ | $0.5t_c(\text{SPC})_M + 0.5t_c(\text{CO})$ | |
| 6§ | $t_{su}(\text{SIMO-SPCH})_M$ | Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0) | $0.5t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M - 10$ | | ns |
| | $t_{su}(\text{SIMO-SPCL})_M$ | Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1) | $0.5t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M - 10$ | | |
| 7§ | $t_v(\text{SPCH-SIMO})_M$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0) | $0.5t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M - 10$ | | ns |
| | $t_v(\text{SPCL-SIMO})_M$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1) | $0.5t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M - 10$ | | |
| 10§ | $t_{su}(\text{SOMI-SPCH})_M$ | Setup time, SPISOMI before SPICLK high (clock polarity = 0) | 0 | | 0 | | ns |
| | $t_{su}(\text{SOMI-SPCL})_M$ | Setup time, SPISOMI before SPICLK low (clock polarity = 1) | 0 | | 0 | | |
| 11§ | $t_v(\text{SPCH-SOMI})_M$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | $0.25t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M - 10$ | | ns |
| | $t_v(\text{SPCL-SOMI})_M$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | $0.25t_c(\text{SPC})_M - 10$ | | $0.5t_c(\text{SPC})_M - 10$ | | |

[†] The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.

[‡] t_c = system clock cycle time = $1/\text{CLKOUT} = t_c(\text{CO})$

§ The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

PARAMETER MEASUREMENT INFORMATION



† The $\overline{\text{SPISTET}}$ signal must be active before the SPI communication stream starts; the $\overline{\text{SPISTET}}$ signal must remain active until the SPI communication stream is complete.

Figure 36. SPI Master Mode External Timing (Clock Phase = 1)

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SPI SLAVE MODE TIMING PARAMETERS

Slave mode timing information is listed in the following tables.

SPI slave mode external timing parameters (clock phase = 0)^{†‡} (see Figure 37)

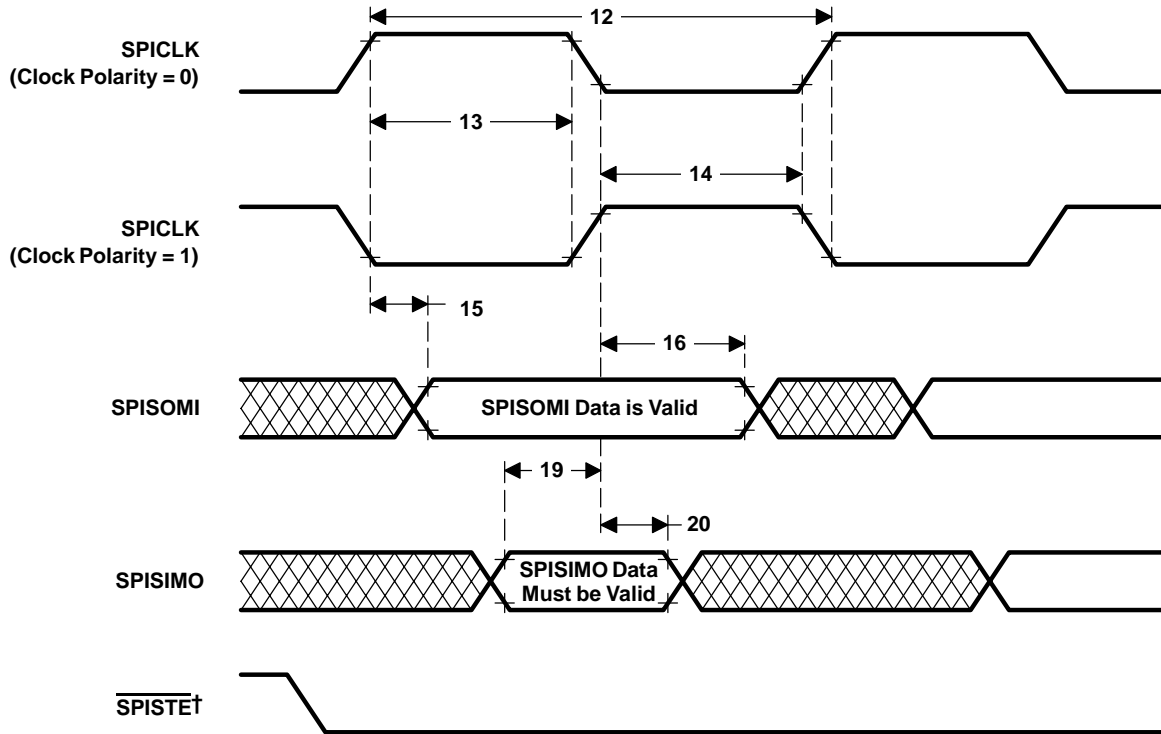
| NO. | | | MIN | MAX | UNIT |
|-----|-----------------------------|---|------------------------------|-----------------------|------|
| 12 | $t_c(\text{SPC})S$ | Cycle time, SPICLK | $4t_c(\text{CO})^{\dagger}$ | | ns |
| 13§ | $t_w(\text{SPCH})S$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_c(\text{SPC})S - 10$ | $0.5t_c(\text{SPC})S$ | ns |
| | $t_w(\text{SPCL})S$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_c(\text{SPC})S - 10$ | $0.5t_c(\text{SPC})S$ | |
| 14§ | $t_w(\text{SPCL})S$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_c(\text{SPC})S - 10$ | $0.5t_c(\text{SPC})S$ | ns |
| | $t_w(\text{SPCH})S$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_c(\text{SPC})S - 10$ | $0.5t_c(\text{SPC})S$ | |
| 15§ | $t_d(\text{SPCH-SOMI})S$ | Delay time, SPICLK high to SPISOMI valid (clock polarity = 0) | $0.375t_c(\text{SPC})S - 10$ | | ns |
| | $t_d(\text{SPCL-SOMI})S$ | Delay time, SPICLK low to SPISOMI valid (clock polarity = 1) | $0.375t_c(\text{SPC})S - 10$ | | |
| 16§ | $t_v(\text{SPCL-SOMI})S$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0) | $0.75t_c(\text{SPC})S$ | | ns |
| | $t_v(\text{SPCH-SOMI})S$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1) | $0.75t_c(\text{SPC})S$ | | |
| 19§ | $t_{su}(\text{SIMO-SPCL})S$ | Setup time, SPISIMO before SPICLK low (clock polarity = 0) | 0 | | ns |
| | $t_{su}(\text{SIMO-SPCH})S$ | Setup time, SPISIMO before SPICLK high (clock polarity = 1) | 0 | | |
| 20§ | $t_v(\text{SPCL-SIMO})S$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0) | $0.5t_c(\text{SPC})S$ | | ns |
| | $t_v(\text{SPCH-SIMO})S$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1) | $0.5t_c(\text{SPC})S$ | | |

[†] The MASTER/SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.

[‡] t_c = system clock cycle time = $1/\text{CLKOUT} = t_c(\text{CO})$

[§] The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

PARAMETER MEASUREMENT INFORMATION



† The $\overline{\text{SPISTE}}$ signal must be active before the SPI communication stream starts; the $\overline{\text{SPISTE}}$ signal must remain active until the SPI communication stream is complete.

Figure 37. SPI Slave Mode External Timing (Clock Phase = 0)

TMS320LF2407, TMS320LF2406, TMS320LF2402

DSP CONTROLLERS

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SPI slave mode external timing parameters (clock phase = 1)^{†‡} (see Figure 38)

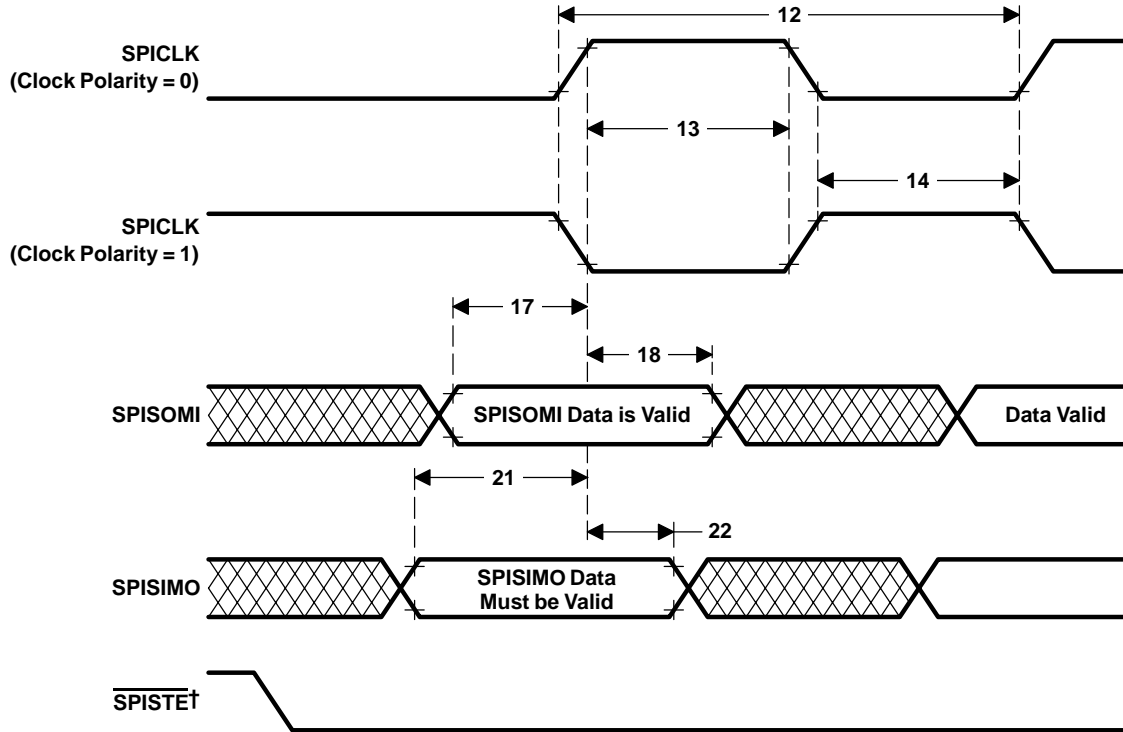
| NO. | | | MIN | MAX | UNIT |
|-----|-----------------------------|---|----------------------------|-----------------------|------|
| 12 | $t_c(\text{SPC})S$ | Cycle time, SPICLK | $8t_c(\text{CO})$ | | ns |
| 13§ | $t_w(\text{SPCH})S$ | Pulse duration, SPICLK high (clock polarity = 0) | $0.5t_c(\text{SPC})S - 10$ | $0.5t_c(\text{SPC})S$ | ns |
| | $t_w(\text{SPCL})S$ | Pulse duration, SPICLK low (clock polarity = 1) | $0.5t_c(\text{SPC})S - 10$ | $0.5t_c(\text{SPC})S$ | |
| 14§ | $t_w(\text{SPCL})S$ | Pulse duration, SPICLK low (clock polarity = 0) | $0.5t_c(\text{SPC})S - 10$ | $0.5t_c(\text{SPC})S$ | ns |
| | $t_w(\text{SPCH})S$ | Pulse duration, SPICLK high (clock polarity = 1) | $0.5t_c(\text{SPC})S - 10$ | $0.5t_c(\text{SPC})S$ | |
| 17§ | $t_{su}(\text{SOMI-SPCH})S$ | Setup time, SPISOMI before SPICLK high (clock polarity = 0) | $0.125t_c(\text{SPC})S$ | | ns |
| | $t_{su}(\text{SOMI-SPCL})S$ | Setup time, SPISOMI before SPICLK low (clock polarity = 1) | $0.125t_c(\text{SPC})S$ | | |
| 18§ | $t_v(\text{SPCH-SOMI})S$ | Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0) | $0.75t_c(\text{SPC})S$ | | ns |
| | $t_v(\text{SPCL-SOMI})S$ | Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1) | $0.75t_c(\text{SPC})S$ | | |
| 21§ | $t_{su}(\text{SIMO-SPCH})S$ | Setup time, SPISIMO before SPICLK high (clock polarity = 0) | 0 | | ns |
| | $t_{su}(\text{SIMO-SPCL})S$ | Setup time, SPISIMO before SPICLK low (clock polarity = 1) | 0 | | |
| 22§ | $t_v(\text{SPCH-SIMO})S$ | Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0) | $0.5t_c(\text{SPC})S$ | | ns |
| | $t_v(\text{SPCL-SIMO})S$ | Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1) | $0.5t_c(\text{SPC})S$ | | |

[†] The MASTER/SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is set.

[‡] t_c = system clock cycle time = $1/\text{CLKOUT} = t_c(\text{CO})$

[§] The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

PARAMETER MEASUREMENT INFORMATION



† The $\overline{\text{SPISTE}}$ signal must be active before the SPI communication stream starts; the $\overline{\text{SPISTE}}$ signal must remain active until the SPI communication stream is complete.

Figure 38. SPI Slave Mode External Timing (Clock Phase = 1)

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external memory interface *read* timings

switching characteristics over recommended operating conditions for an external memory interface read at 30 MHz [$H = 0.5t_{c(CO)}$] (see Figure 39)

| PARAMETER | MIN | MAX | UNIT |
|--|-------|-----|------|
| $t_d(COL-CNTL)$ Delay time, CLKOUT low to control valid | | 6 | ns |
| $t_d(COL-CNTH)$ Delay time, CLKOUT low to control inactive | | 6 | ns |
| $t_d(COL-ARD)$ Delay time, CLKOUT low to address valid | | 8 | ns |
| $t_d(COH-RDL)$ Delay time, CLKOUT high to \overline{RD} strobe active | | 6 | ns |
| $t_d(COL-RDH)$ Delay time, CLKOUT low to \overline{RD} strobe inactive high | -8 | 1 | ns |
| $t_d(COL-SL)$ Delay time, CLKOUT low to \overline{STRB} strobe active low | | 6 | ns |
| $t_d(COL-SH)$ Delay time, CLKOUT low to \overline{STRB} strobe inactive high | | 6 | ns |
| $t_d(WRN)$ Delay time, W/\overline{R} going low to R/\overline{W} rising | | 5 | ns |
| $t_h(A)COL$ Hold time, address valid after CLKOUT low | 2 | | ns |
| $t_{su}(A)RD$ Setup time, address valid before \overline{RD} strobe active low | H - 7 | | ns |
| $t_h(A)RD$ Hold time, address valid after \overline{RD} strobe inactive high | 0 | | ns |

timing requirements [$H = 0.5t_{c(CO)}$] (see Figure 39)

| | MIN | MAX | UNIT |
|---|-----|---------|------|
| $t_a(A)$ Access time, read data from address valid | | 2H - 13 | ns |
| $t_a(RD)$ Access time, read data from \overline{RD} low | | H - 7 | ns |
| $t_{su}(D)RD$ Setup time, read data before \overline{RD} strobe inactive high | 10 | | ns |
| $t_h(D)RD$ Hold time, read data after \overline{RD} strobe inactive high | 0 | | ns |
| $t_h(AIV-D)$ Hold time, read data after address invalid | 0 | | ns |



external memory interface *read* timings (continued)

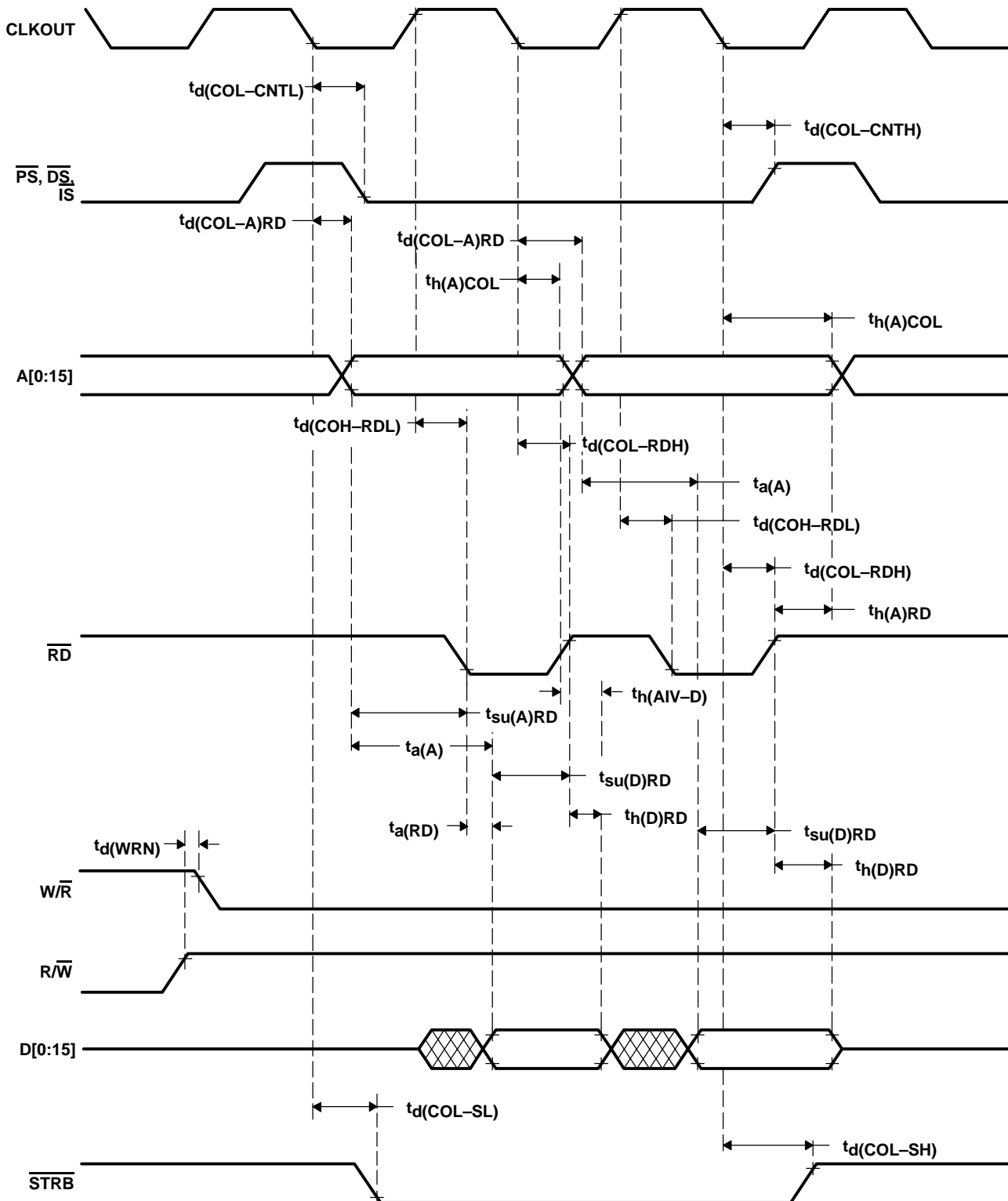


Figure 39. Memory Interface Read/Read Timings

TMS320LF2407, TMS320LF2406, TMS320LF2402

DSP CONTROLLERS

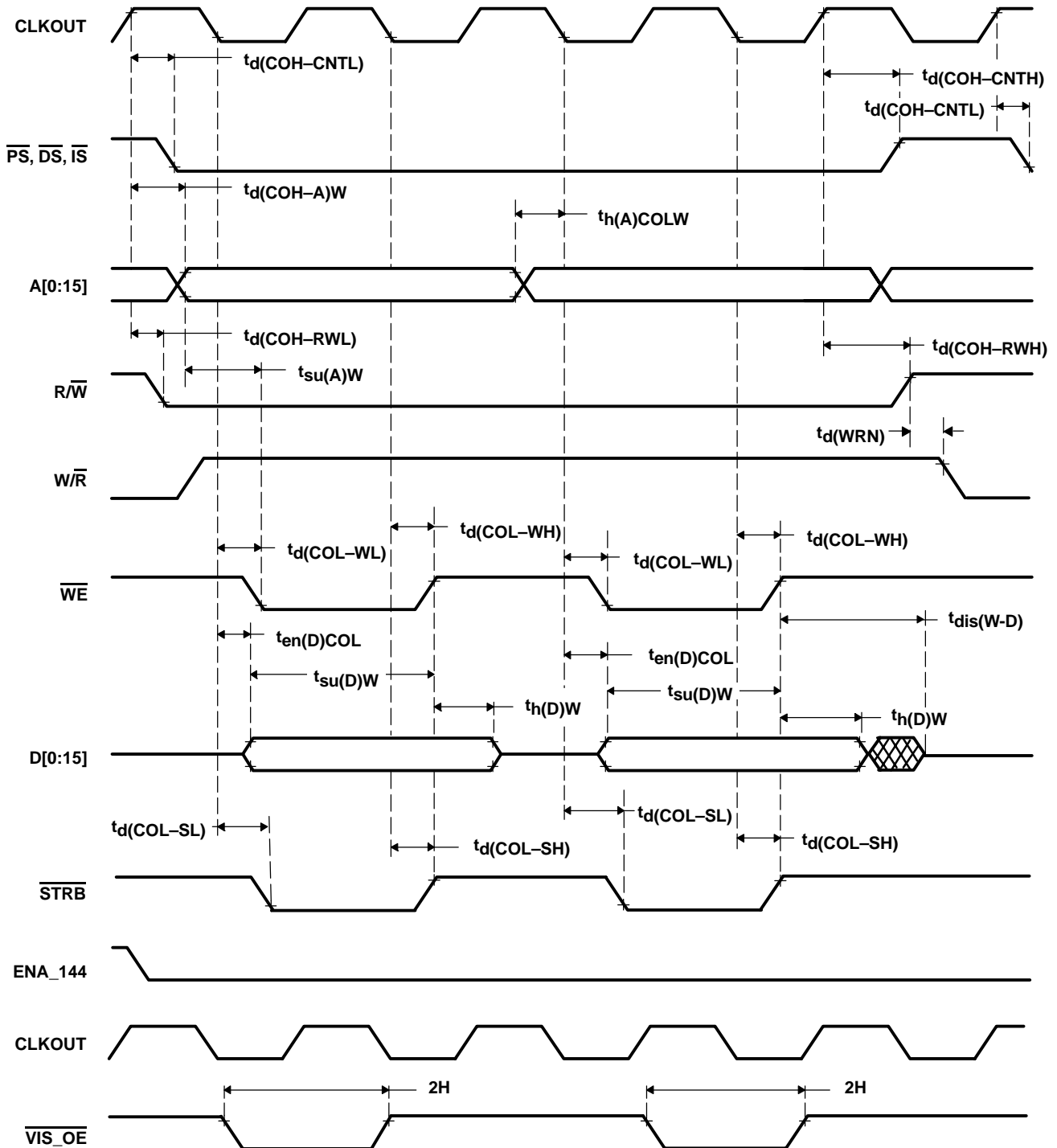
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external memory interface *write* timings

switching characteristics over recommended operating conditions for an external memory interface write at 30 MHz [$H = 0.5t_{c(CO)}$] (see Figure 40)

| PARAMETER | MIN | MAX | UNIT |
|---|-------|-----|------|
| $t_d(COH-CNTL)$ Delay time, CLKOUT high to control valid | | 6 | ns |
| $t_d(COH-CNTH)$ Delay time, CLKOUT high to control inactive | | 6 | ns |
| $t_d(COH-A)W$ Delay time, CLKOUT high to address valid | | 10 | ns |
| $t_d(COH-RWL)$ Delay time, CLKOUT high to R/\overline{W} low | | 6 | ns |
| $t_d(COH-RWH)$ Delay time, CLKOUT high to R/\overline{W} high | | 6 | ns |
| $t_d(COL-WL)$ Delay time, CLKOUT low to \overline{WE} strobe active low | | 7 | ns |
| $t_d(COL-WH)$ Delay time, CLKOUT low to \overline{WE} strobe inactive high | | 7 | ns |
| $t_d(WRN)$ Delay time, W/\overline{R} going low to R/\overline{W} rising | | 5 | ns |
| $t_{en(D)COL}$ Enable time, data bus driven from CLKOUT low | -3 | | ns |
| $t_d(COL-SL)$ Delay time, CLKOUT low to \overline{STRB} active low | | 6 | ns |
| $t_d(COL-SH)$ Delay time, CLKOUT low to \overline{STRB} inactive high | | 6 | ns |
| $t_h(A)COLW$ Hold time, address valid after CLKOUT low | -5 | | ns |
| $t_{su(A)W}$ Setup time, address valid before \overline{WE} strobe active low | H-9 | | ns |
| $t_{su(D)W}$ Setup time, write data before \overline{WE} strobe inactive high | 2H-17 | | ns |
| $t_h(D)W$ Hold time, write data after \overline{WE} strobe inactive high | 0 | | ns |
| $t_{dis(W-D)}$ Disable time, data bus high impedance from \overline{WE} high | 5 | | ns |

external memory interface *write* timings (continued)



NOTE A: $\overline{\text{VIS_OE}}$ will be visible at pin 97 of LF2407 when ENA_144 is low along with BVIS bits (10,9 of WSGR register – FFFFh@I/O) set to 10 or 11. CLKOUT and $\overline{\text{VIS_OE}}$ indicate internal memory write cycles (program/data). During $\overline{\text{VIS_OE}}$ cycles, the external bus will be driven. CLKOUT is to be used along with $\overline{\text{VIS_OE}}$ for trace capabilities.

Figure 40. Address Visibility Mode

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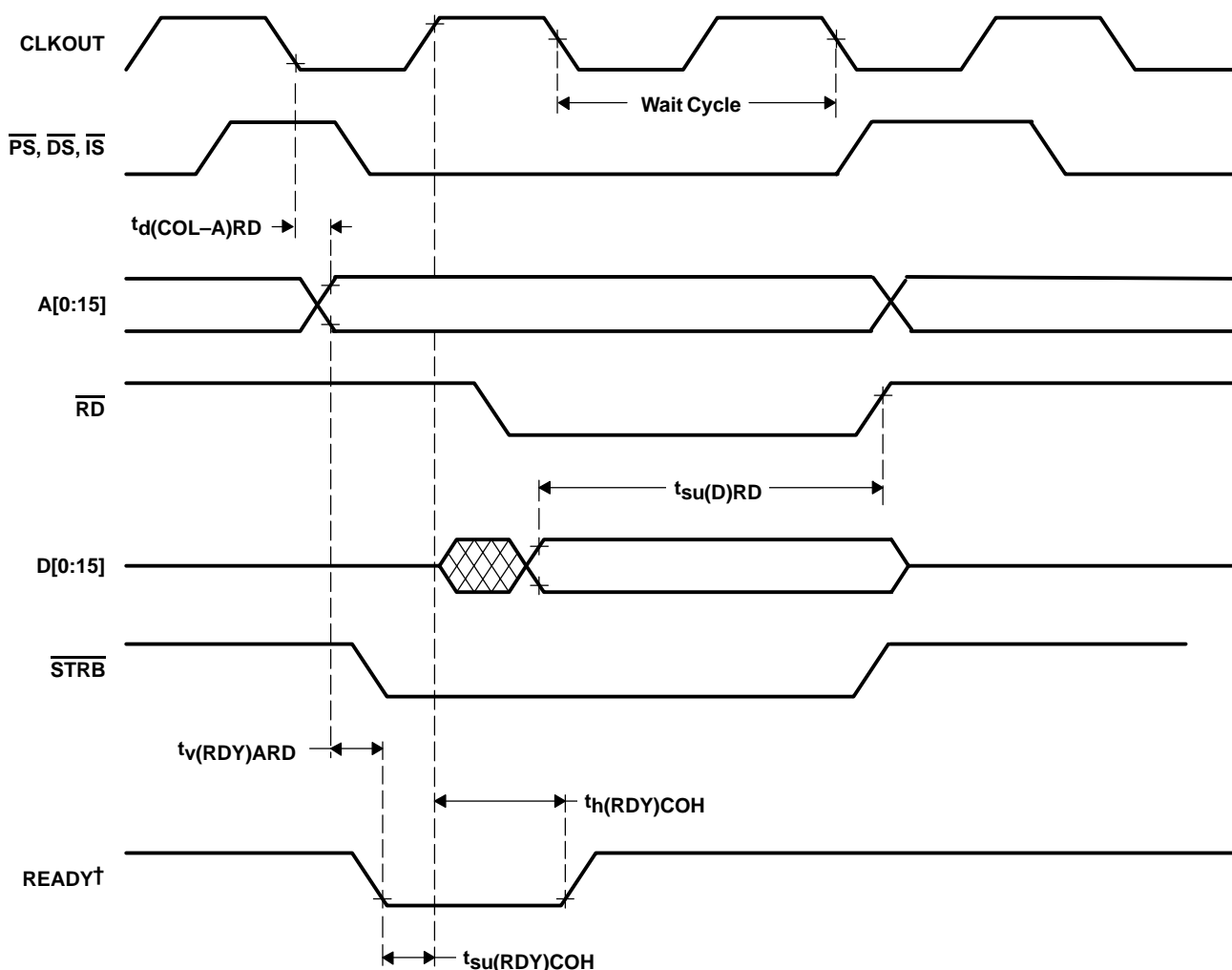
external memory interface *ready-on-read* timings

switching characteristics over recommended operating conditions for an external memory interface ready-on-read (see Figure 41)

| PARAMETER | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_d(\text{COL-A})\text{RD}$ Delay time, CLKOUT low to address valid | | 8 | ns |

timing requirements for an external memory interface ready-on-read (see Figure 41)

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_h(\text{RDY})\text{COH}$ Hold time, READY after CLKOUT high | -3 | | ns |
| $t_{su}(\text{D})\text{RD}$ Setup time, read data before $\overline{\text{RD}}$ strobe inactive high | 10 | | ns |
| $t_v(\text{RDY})\text{ARD}$ Valid time, READY after address valid on read | | -2 | ns |
| $t_{su}(\text{RDY})\text{COH}$ Setup time, READY before CLKOUT high | 22 | | ns |



† The WSGR register must be programmed before the READY pin can be used. See the READY pin description for more details.

Figure 41. Ready-on-Read Timings



external memory interface *ready-on-read* timings (continued)

timing requirements for an external memory interface ready-on-read with one software wait state and one external wait state (see Figure 42)

| | | MIN | MAX | UNIT |
|------------------|---|-----|-----|------|
| $t_{h(RDY)COH}$ | Hold time, READY after CLKOUT high | 14 | | ns |
| $t_{su(RDY)COH}$ | Setup time, READY before CLKOUT high | 7 | | ns |
| $t_d(COL-A)RD$ | Delay time, CLKOUT low to address valid | | 8 | ns |

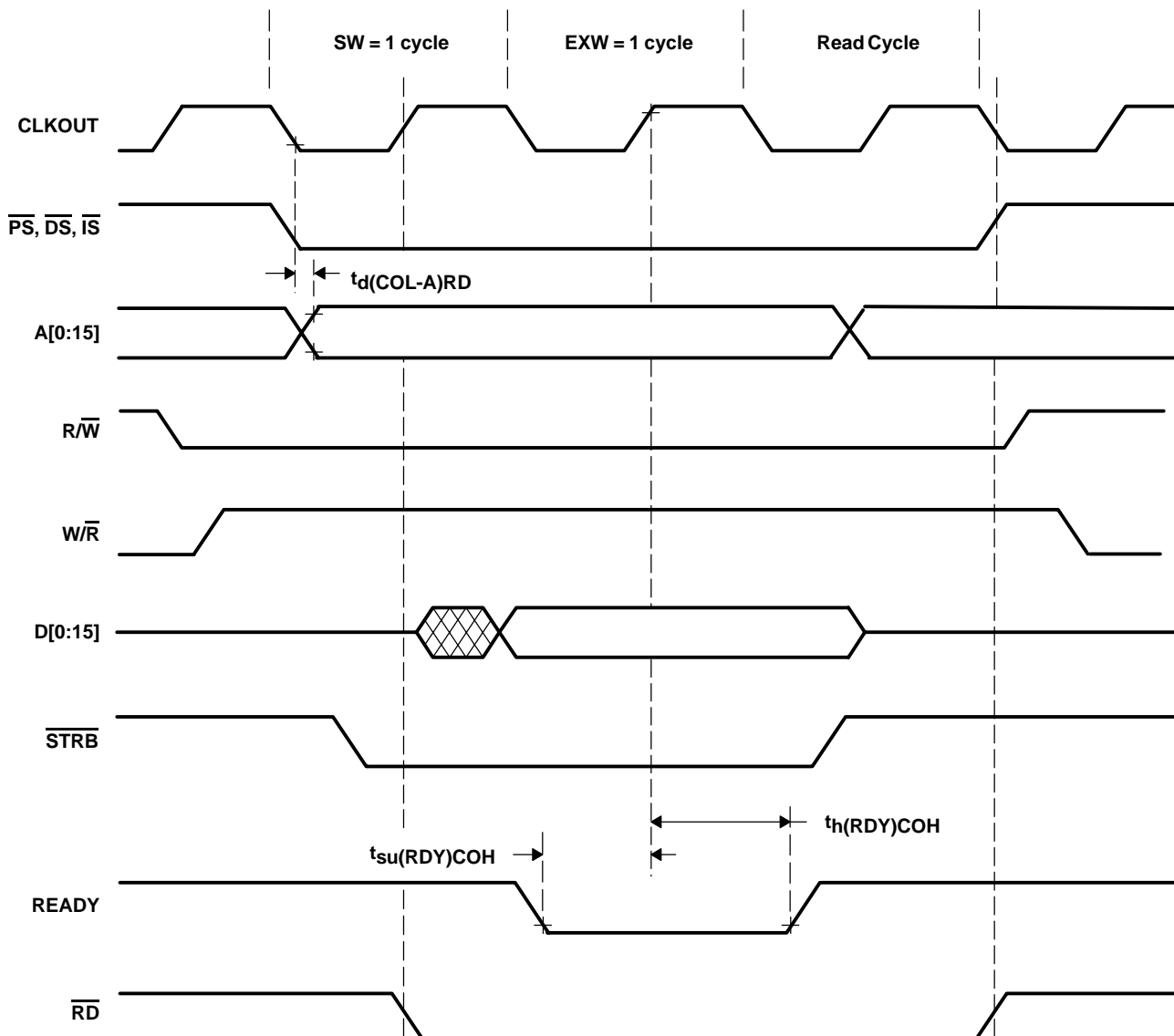


Figure 42. Ready-on-Read Timings With One Software Wait (SW) State and One External Wait (EXW) State

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external memory interface *ready-on-write* timings

switching characteristics over recommended operating conditions for an external memory interface ready-on-write (see Figure 43)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------|--|-----|-----|------|
| $t_{d(COH-A)W}$ | Delay time, CLKOUT high to address valid | | 10 | ns |

timing requirements for an external memory interface ready-on-write [$H = 0.5t_{c(CO)}$]
(see Figure 43)

| | | MIN | MAX | UNIT |
|------------------|--|-------|-----|------|
| $t_{h(RDY)COH}$ | Hold time, READY after CLKOUT high | -3 | | ns |
| $t_{su(D)W}$ | Setup time, write data before \overline{WE} strobe inactive high | 2H-17 | | ns |
| $t_{v(RDY)AW}$ | Valid time, READY after address valid on write | | -3 | ns |
| $t_{su(RDY)COH}$ | Setup time, READY before CLKOUT high | 22 | | ns |

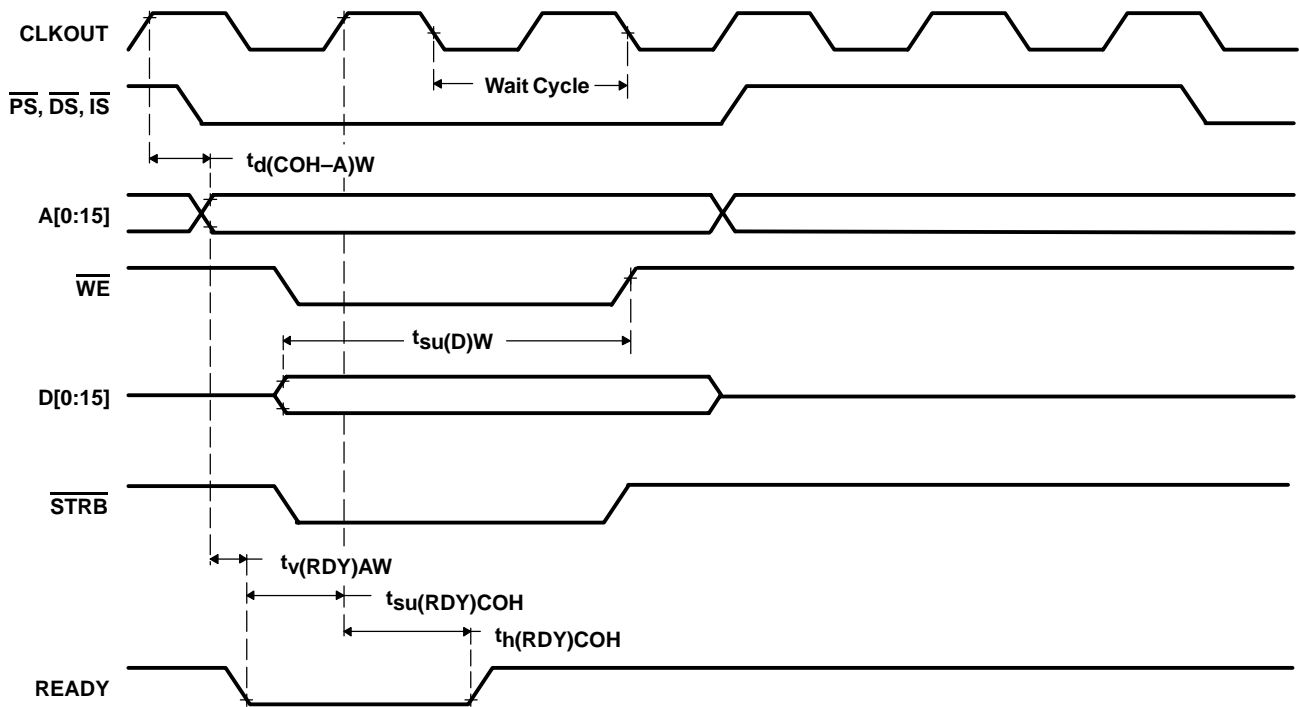


Figure 43. Ready-on-Write Timings

external memory interface *ready-on-write* timings (continued)

timing requirements for an external memory interface ready-on-write with one software wait state and one external wait state (see Figure 44)

| | | MIN | MAX | UNIT |
|---------------|--|-----|-----|------|
| $t_{h(RDY)}$ | Hold time, READY after CLKOUT high | 14 | | ns |
| $t_{su(RDY)}$ | Setup time, READY before CLKOUT high | 7 | | ns |
| $t_d(COH-A)W$ | Delay time, CLKOUT high to address valid | | 10 | ns |

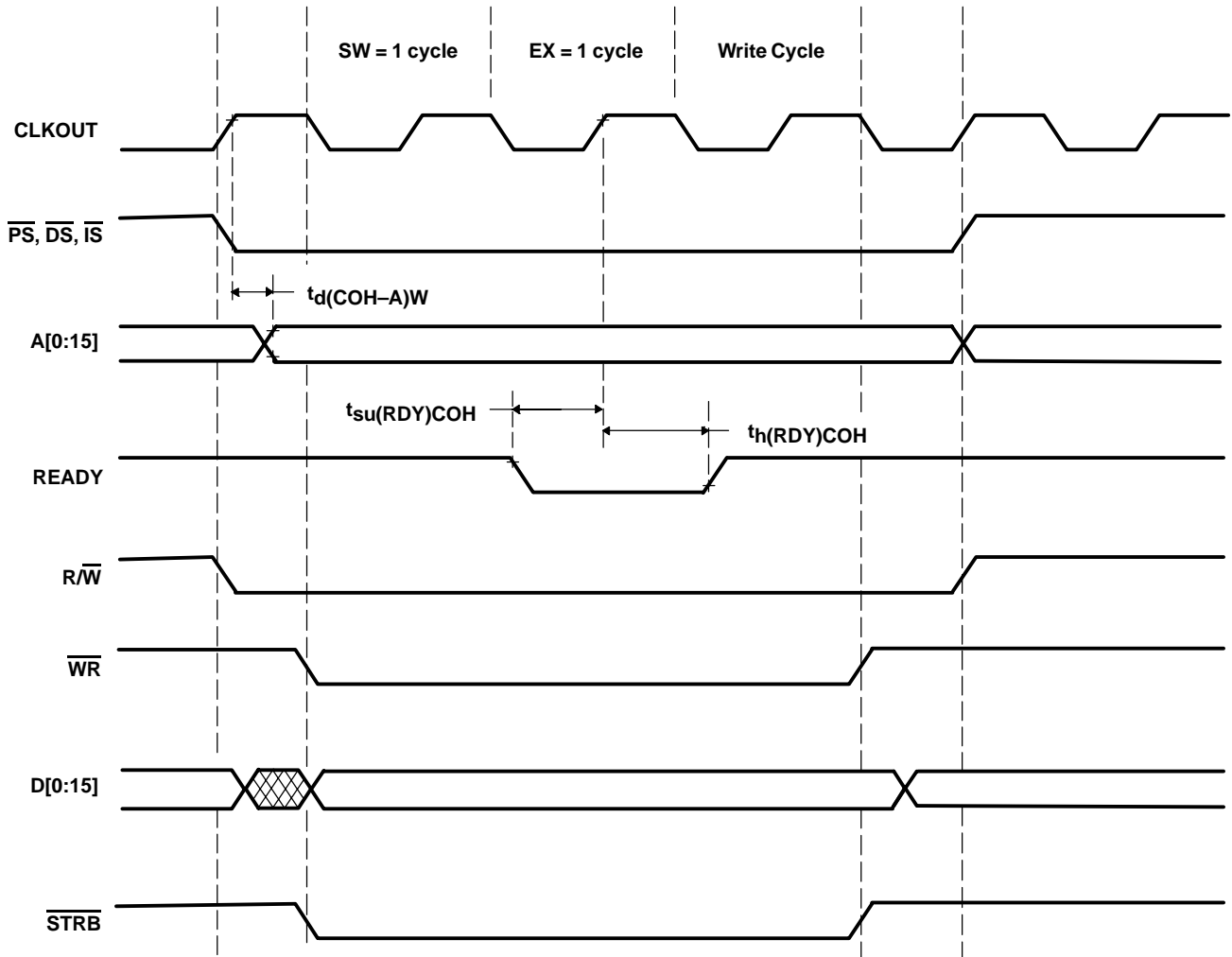


Figure 44. Ready-on-Write Timings With One Software Wait State and One External Wait State

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10-bit analog-to-digital converter (ADC)

The 10-bit ADC has a separate power bus for its analog circuitry. These pins are referred to as V_{CCA} and V_{SSA} . The power bus isolation is to enhance ADC performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS} and V_{CC} from coupling into the ADC analog stage. All ADC specifications are given with respect to V_{SSA} unless otherwise noted.

Resolution 10-bit (1024 values)
Monotonic Assured
Output conversion mode 000h to 3FFh (000h for $V_I \leq V_{SSA}$; 3FFh for $V_I \geq V_{CCA}$)
Conversion time (including sample time) 500 ns

recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-------------|---------------------------------------|-------------|-----|-------------|------|
| V_{CCA} | Analog supply voltage | 3.0 | 3.3 | 3.6 | V |
| V_{SSA} | Analog ground | | 0 | | V |
| V_{REFHI} | Analog supply reference source† | V_{REFLO} | | V_{CCA} | V |
| V_{REFLO} | Analog ground reference source† | V_{SSA} | | V_{REFHI} | V |
| V_{AI} | Analog input voltage, ADCIN00–ADCIN07 | V_{REFLO} | | V_{REFHI} | V |

† V_{REFHI} and V_{REFLO} must be stable, within $\pm 1/2$ LSB of the required resolution, during the entire conversion time.

ADC operating frequency

| | MIN | MAX | UNIT |
|-------------------------|-----|-----|------|
| ADC operating frequency | 4 | 30 | MHz |

operating characteristics over recommended operating condition ranges†

| PARAMETER | | DESCRIPTION | MIN | TYP | MAX | UNIT |
|----------------------|------------------------------------|--|-----|------|-----|------|
| I _{CCA} | Analog supply current | V _{CCA} = 3.3 V | | 10 | 15 | mA |
| | | V _{CCA} = V _{REFHI} = 3.3 V | | | 1 | μA |
| I _{ADREFHI} | ADV _{REFHI} input current | | | 0.75 | 1.5 | mA |
| I _{ADCIN} | Analog input leakage | | | | 1 | μA |
| C _{ai} | Analog input capacitance | Typical capacitive load on analog input pin | | 10 | | pF |
| | | | | 30 | | |
| E _{DNL} | Differential nonlinearity error | Difference between the actual step width and the ideal value | | | ± 2 | LSB |
| E _{INL} | Integral nonlinearity error | Maximum deviation from the best straight line through the ADC transfer characteristics, excluding the quantization error | | | ± 2 | LSB |
| t _d (PU) | Delay time, power-up to ADC valid | Time to stabilize analog stage after power-up | | | 10 | μs |
| Z _{AI} | Analog input source impedance | Analog input source impedance needed for conversions to remain within specifications at min t _w (SH) | | 67 | 10 | Ω |

† Absolute resolution = 3.22 mV. At V_{REFHI} = 3.3 V and V_{REFLO} = 0 V, this is one LSB. As V_{REFHI} decreases, V_{REFLO} increases, or both, the LSB size decreases. Therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.

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internal ADC module timings† (see Figure 45)

| | | MIN | MAX | UNIT |
|---------------|---|--------------|-------------|------|
| $t_c(AD)$ | Cycle time, ADC prescaled clock | 33.3 | | ns |
| $t_w(SHC)$ | Pulse duration, total sample/hold and conversion time‡ | 500 | | ns |
| $t_w(SH)$ | Pulse duration, sample and hold time | $2t_c(AD)$ § | $32t_c(AD)$ | ns |
| $t_w(C)$ | Pulse duration, total conversion time | $10t_c(AD)$ | | ns |
| $t_d(SOC-SH)$ | Delay time, start of conversion to beginning of sample and hold | $3t_c(CO)$ | | ns |
| $t_d(EOC)$ | Delay time, end of conversion to data loaded into result register | $2t_c(CO)$ | | ns |
| $t_d(ADCINT)$ | Delay time, ADC flag to ADC interrupt | $2t_c(CO)$ | | ns |

† The ADC timing diagram represents a typical conversion sequence. Refer to the ADC chapter in the *TMS320LF/LC240x DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357) for more details.

‡ The total sample/hold and conversion time is determined by the summation of $t_d(SOC-SH)$, $t_w(SH)$, $t_w(C)$, and $t_d(EOC)$.

§ Can be varied by ACQ Prescaler bits in the ADCCTRL1 register

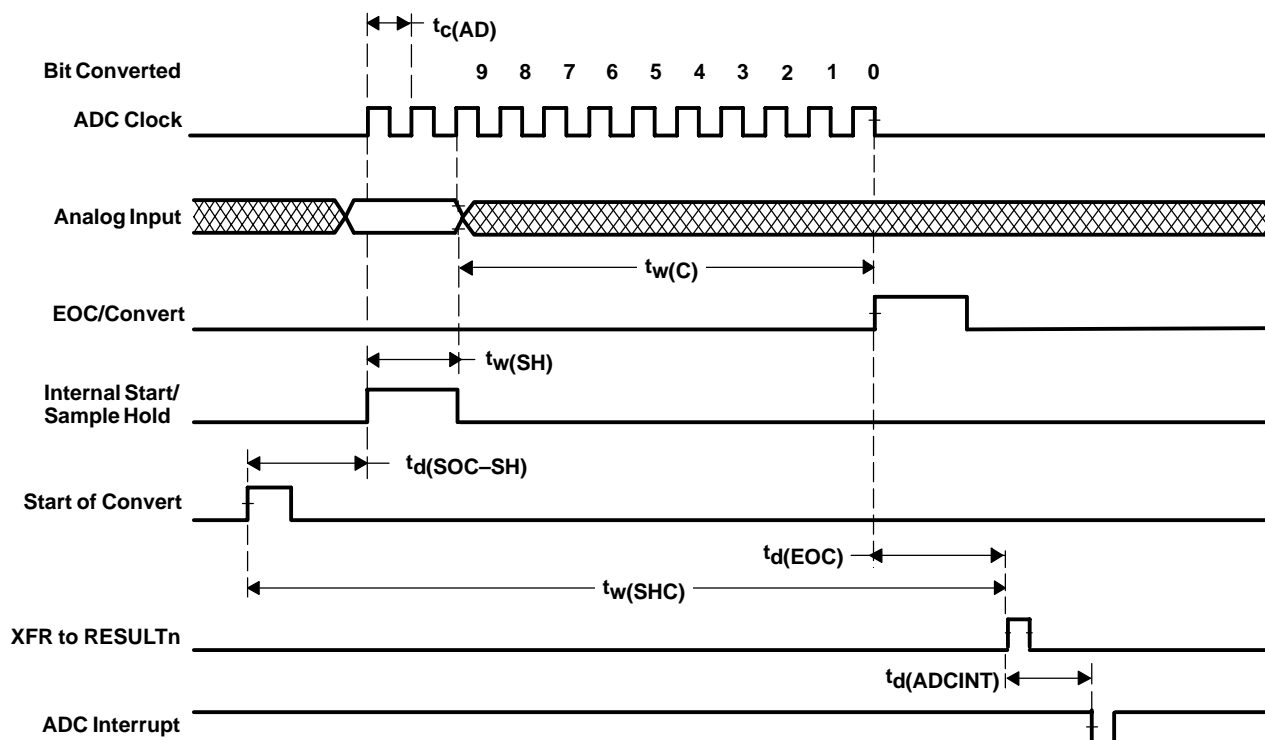


Figure 45. Analog-to-Digital Internal Module Timing

Flash parameters @30 MHz CLOCKOUT

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|-----|------|
| Clear/Programming time† | Time/Word (16-bit) | | 35 | | μs |
| | Time/4K Sector | | 150 | | ms |
| | Time/12K Sector | | 500 | | ms |
| Erase time† | Time/4K Sector | | 500 | | ms |
| | Time/12K Sector | | 1.3 | | s |
| I _{CCP} (V _{CCP} pin current) | Indicates the typical/maximum current consumption during the Clear-Erase-Program (C-E-P) cycle | | 5 | 15 | mA |

† The indicated time does not include the time it takes to load the C-E-P algorithm and the code (to be programmed) onto on-chip RAM. The values specified are when V_{DD} = 3.3 V and V_{CCP} = 5 V, and any deviation from these values could affect the timing parameters. Aging and process variance could also impact the timing parameters.

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peripheral register description

Table 19 is a collection of all the programmable registers of the LF240x and is provided as a quick reference.

Table 19. LF240x DSP Peripheral Register Description

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|------------------------|---|-----------|----------------|-----------|----------------|---------------|-----------|-----------|---------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| | DATA MEMORY SPACE | | | | | | | | |
| | CPU STATUS REGISTERS | | | | | | | | |
| | ARP | | | OV | OVM | 1 | INTM | DP(8) | ST0 |
| | DP(7) | DP(6) | DP(5) | DP(4) | DP(3) | DP(2) | DP(1) | DP(0) | |
| | ARB | | | CNF | TC | SXM | C | 1 | ST1 |
| | 1 | 1 | 1 | XF | 1 | 1 | PM | | |
| | GLOBAL MEMORY AND CPU INTERRUPT REGISTERS | | | | | | | | |
| 00004h | — | — | — | — | — | — | — | — | IMR |
| | — | — | INT6 MASK | INT5 MASK | INT4 MASK | INT3 MASK | INT2 MASK | INT1 MASK | |
| 00005h | Reserved | | | | | | | | GREG |
| 00006h | — | — | — | — | — | — | — | — | IFR |
| | — | — | INT6 FLAG | INT5 FLAG | INT4 FLAG | INT3 FLAG | INT2 FLAG | INT1 FLAG | |
| | SYSTEM REGISTERS | | | | | | | | |
| 07010h | IRQ0.15 | IRQ0.14 | IRQ0.13 | IRQ0.12 | IRQ0.11 | IRQ0.10 | IRQ0.9 | IRQ0.8 | PIRQR0 |
| | IRQ0.7 | IRQ0.6 | IRQ0.5 | IRQ0.4 | IRQ0.3 | IRQ0.2 | IRQ0.1 | IRQ0.0 | |
| 07011h | IRQ1.15 | IRQ1.14 | IRQ1.13 | IRQ1.12 | IRQ1.11 | IRQ1.10 | IRQ1.9 | IRQ1.8 | PIRQR1 |
| | IRQ1.7 | IRQ1.6 | IRQ1.5 | IRQ1.4 | IRQ1.3 | IRQ1.2 | IRQ1.1 | IRQ1.0 | |
| 07012h | IRQ2.15 | IRQ2.14 | IRQ2.13 | IRQ2.12 | IRQ2.11 | IRQ2.10 | IRQ2.9 | IRQ2.8 | PIRQR2 |
| | IRQ2.7 | IRQ2.6 | IRQ2.5 | IRQ2.4 | IRQ2.3 | IRQ2.2 | IRQ2.1 | IRQ2.0 | |
| 07013h | Illegal | | | | | | | | |
| 07014h | IAK0.15 | IAK0.14 | IAK0.13 | IAK0.12 | IAK0.11 | IAK0.10 | IAK0.9 | IAK0.8 | PIACKR0 |
| | IAK0.7 | IAK0.6 | IAK0.5 | IAK0.4 | IAK0.3 | IAK0.2 | IAK0.1 | IAK0.0 | |
| 07015h | IAK1.15 | IAK1.14 | IAK1.13 | IAK1.12 | IAK1.11 | IAK1.10 | IAK1.9 | IAK1.8 | PIACKR1 |
| | IAK1.7 | IAK1.6 | IAK1.5 | IAK1.4 | IAK1.3 | IAK1.2 | IAK1.1 | IAK1.0 | |
| 07016h | IAK2.15 | IAK2.14 | IAK2.13 | IAK2.12 | IAK2.11 | IAK2.10 | IAK2.9 | IAK2.8 | PIACKR2 |
| | IAK2.7 | IAK2.6 | IAK2.5 | IAK2.4 | IAK2.3 | IAK2.2 | IAK2.1 | IAK2.0 | |
| 07017h | Illegal | | | | | | | | |
| 07018h | — | CLKSRC | LPM1 | LPM0 | CLK PS2 | CLK PS1 | CLK PS0 | — | SCSR1 |
| | ADC CLKEN | SCI CLKEN | SPI CLKEN | CAN CLKEN | EVB CLKEN | EVA CLKEN | — | ILLADR | |
| 07019h | — | — | — | — | — | — | — | — | SCSR2 |
| | — | — | WD OVERRIDE | XMIF HI Z | <u>BOOT_EN</u> | MP/ <u>MC</u> | DON | PON | |
| 0701Ah to 0701Bh | Illegal | | | | | | | | |
| 0701Ch | DIN15 | DIN14 | DIN13 | DIN12 | DIN11 | DIN10 | DIN9 | DIN8 | DINR |
| | DIN7 | DIN6 | DIN5 | DIN4 | DIN3 | DIN2 | DIN1 | DIN0 | |
| 0701Dh | Illegal | | | | | | | | |
| 0701Eh | V15 | V14 | V13 | V12 | V11 | V10 | V9 | V8 | PIVR |
| | V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 | |
| 0701Fh | Illegal | | | | | | | | |

Indicates change with respect to the F243/F241, C242 device register maps.

peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|---|-----------------------------|-------------------|---------------------|--------------------|-------------------|-------------------|-------------------|-------------------|----------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| 07020h to 07022h | WD CONTROL REGISTERS | | | | | | | | |
| | Illegal | | | | | | | | |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07023h | Illegal | | | | | | | | WDCNTR |
| 07024h | Illegal | | | | | | | | WDKEY |
| 07025h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07026h to 07028h | Illegal | | | | | | | | |
| 07029h | WD FLAG | WDDIS | WDCHK2 | WDCHK1 | WDCHK0 | WDPS2 | WDPS1 | WDPS0 | WDCR |
| 0702Ah to 0703Fh | Illegal | | | | | | | | SPICCR |
| SERIAL PERIPHERAL INTERFACE (SPI) CONFIGURATION CONTROL REGISTERS | | | | | | | | | |
| 07040h | SPI SW RESET | CLOCK POLARITY | — | — | SPI CHAR3 | SPI CHAR2 | SPI CHAR1 | SPI CHAR0 | |
| 07041h | — | — | — | OVERRUN INT ENA | CLOCK PHASE | MASTER/ SLAVE | TALK | SPI INT ENA | SPICTL |
| 07042h | RECEIVER OVERRUN FLAG | SPI INT FLAG | TX BUF FULL FLAG | — | — | — | — | — | SPISTS |
| 07043h | Illegal | | | | | | | | SPIBRR |
| 07044h | — | SPI BIT RATE 6 | SPI BIT RATE 5 | SPI BIT RATE 4 | SPI BIT RATE 3 | SPI BIT RATE 2 | SPI BIT RATE 1 | SPI BIT RATE 0 | |
| 07045h | Illegal | | | | | | | | |
| 07046h | ERXB15 | ERXB14 | ERXB13 | ERXB12 | ERXB11 | ERXB10 | ERXB9 | ERXB8 | SPIRXEMU |
| | ERXB7 | ERXB6 | ERXB5 | ERXB4 | ERXB3 | ERXB2 | ERXB1 | ERXB0 | |
| 07047h | RXB15 | RXB14 | RXB13 | RXB12 | RXB11 | RXB10 | RXB9 | RXB8 | SPIRXBUF |
| | RXB7 | RXB6 | RXB5 | RXB4 | RXB3 | RXB2 | RXB1 | RXB0 | |
| 07048h | TXB15 | TXB14 | TXB13 | TXB12 | TXB11 | TXB10 | TXB9 | TXB8 | SPITXBUF |
| | TXB7 | TXB6 | TXB5 | TXB4 | TXB3 | TXB2 | TXB1 | TXB0 | |
| 07049h | SDAT15 | SDAT14 | SDAT13 | SDAT12 | SDAT11 | SDAT10 | SDAT9 | SDAT8 | SPIDAT |
| | SDAT7 | SDAT6 | SDAT5 | SDAT4 | SDAT3 | SDAT2 | SDAT1 | SDAT0 | |
| 0704Ah to 0704Eh | Illegal | | | | | | | | SPIPRI |
| 0704Fh | — | SPI PRIORITY | SPI SUSP SOFT | SPI SUSP FREE | — | — | — | — | |

Indicates change with respect to the F243/F241, C242 device register maps.

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peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|------------------|---|-----------------|----------------|---------------|----------------|----------------|----------------|-------------|----------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| | SERIAL COMMUNICATIONS INTERFACE (SCI) CONFIGURATION CONTROL REGISTERS | | | | | | | | |
| 07050h | STOP BITS | EVEN/ODD PARITY | PARITY ENABLE | LOOP BACK ENA | ADDR/IDLE MODE | SCI CHAR2 | SCI CHAR1 | SCI CHAR0 | SCICCR |
| 07051h | — | RX ERR INT ENA | SW RESET | — | TXWAKE | SLEEP | TXENA | RXENA | SCICTL1 |
| 07052h | BAUD15 (MSB) | BAUD14 | BAUD13 | BAUD12 | BAUD11 | BAUD10 | BAUD9 | BAUD8 | SCIHBAUD |
| 07053h | BAUD7 | BAUD6 | BAUD5 | BAUD4 | BAUD3 | BAUD2 | BAUD1 | BAUD0 (LSB) | SCILBAUD |
| 07054h | TXRDY | TX EMPTY | — | — | — | — | RX/BK INT ENA | TX INT ENA | SCICTL2 |
| 07055h | RX ERROR | RXRDY | BRKDT | FE | OE | PE | RXWAKE | — | SCIRXST |
| 07056h | ERXDT7 | ERXDT6 | ERXDT5 | ERXDT4 | ERXDT3 | ERXDT2 | ERXDT1 | ERXDT0 | SCIRXEMU |
| 07057h | RXDT7 | RXDT6 | RXDT5 | RXDT4 | RXDT3 | RXDT2 | RXDT1 | RXDT0 | SCIRXBUF |
| 07058h | Illegal | | | | | | | | |
| 07059h | TXDT7 | TXDT6 | TXDT5 | TXDT4 | TXDT3 | TXDT2 | TXDT1 | TXDT0 | SCITXBUF |
| 0705Ah to 0705Eh | Illegal | | | | | | | | |
| 0705Fh | — | SCITX PRIORITY | SCIRX PRIORITY | SCI SOFT | SCI FREE | — | — | — | SCIPRI |
| 07060h to 0706Fh | Illegal | | | | | | | | |
| | EXTERNAL INTERRUPT CONTROL REGISTERS | | | | | | | | |
| 07070h | XINT1 FLAG | — | — | — | — | — | — | — | XINT1CR |
| | — | — | — | — | — | XINT1 POLARITY | XINT1 PRIORITY | XINT1 ENA | |
| 07071h | XINT2 FLAG | — | — | — | — | — | — | — | XINT2CR |
| | — | — | — | — | — | XINT2 POLARITY | XINT2 PRIORITY | XINT2 ENA | |
| 07072h to 0708Fh | Illegal | | | | | | | | |
| | DIGITAL I/O CONTROL REGISTERS | | | | | | | | |
| 07090h | MCRA.15 | MCRA.14 | MCRA.13 | MCRA.12 | MCRA.11 | MCRA.10 | MCRA.9 | MCRA.8 | MCRA |
| | MCRA.7 | MCRA.6 | MCRA.5 | MCRA.4 | MCRA.3 | MCRA.2 | MCRA.1 | MCRA.0 | |
| 07091h | Illegal | | | | | | | | |
| 07092h | MCRB.15 | MCRB.14 | MCRB.13 | MCRB.12 | MCRB.11 | MCRB.10 | MCRB.9 | MCRB.8 | MCRB |
| | MCRB.7 | MCRB.6 | MCRB.5 | MCRB.4 | MCRB.3 | MCRB.2 | MCRB.1 | MCRB.0 | |
| 07093h | Illegal | | | | | | | | |
| 07094h | MCRC.15 | MCRC.14 | MCRC.13 | MCRC.12 | MCRC.11 | MCRC.10 | MCRC.9 | MCRC.8 | MCRC |
| | MCRC.7 | MCRC.6 | MCRC.5 | MCRC.4 | MCRC.3 | MCRC.2 | MCRC.1 | MCRC.0 | |
| 07095h | E7DIR | E6DIR | E5DIR | E4DIR | E3DIR | E2DIR | E1DIR | E0DIR | PEDATDIR |
| | IOPE7 | IOPE6 | IOPE5 | IOPE4 | IOPE3 | IOPE2 | IOPE1 | IOPE0 | |

Indicates change with respect to the F243/F241, C242 device register maps.



peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG | |
|---|---|---------------------------|-----------------|-------------------|-----------------------|-----------------------|------------------|--------------------|-------------|-----------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | | |
| 07096h | DIGITAL I/O CONTROL REGISTERS (CONTINUED) | | | | | | | | PFDATDIR | |
| | — | F6DIR | F5DIR | F4DIR | F3DIR | F2DIR | F1DIR | F0DIR | | |
| | — | IOPF6 | IOPF5 | IOPF4 | IOPF3 | IOPF2 | IOPF1 | IOPF0 | | |
| 07098h | A7DIR | A6DIR | A5DIR | A4DIR | A3DIR | A2DIR | A1DIR | A0DIR | PADATDIR | |
| | IOPA7 | IOPA6 | IOPA5 | IOPA4 | IOPA3 | IOPA2 | IOPA1 | IOPA0 | | |
| 07099h | Illegal | | | | | | | | PBDATDIR | |
| 0709Ah | B7DIR | B6DIR | B5DIR | B4DIR | B3DIR | B2DIR | B1DIR | B0DIR | | |
| | IOPB7 | IOPB6 | IOPB5 | IOPB4 | IOPB3 | IOPB2 | IOPB1 | IOPB0 | | |
| 0709Bh | Illegal | | | | | | | | PCDATDIR | |
| 0709Ch | C7DIR | C6DIR | C5DIR | C4DIR | C3DIR | C2DIR | C1DIR | C0DIR | | |
| | IOPC7 | IOPC6 | IOPC5 | IOPC4 | IOPC3 | IOPC2 | IOPC1 | IOPC0 | | |
| 0709Dh | Illegal | | | | | | | | PDDATDIR | |
| 0709Eh | — | — | — | — | — | — | — | D0DIR | | |
| | — | — | — | — | — | — | — | IOPD0 | | |
| 0709Fh | Illegal | | | | | | | | ADCCTRL1 | |
| ANALOG-TO-DIGITAL CONVERTER (ADC) REGISTERS | | | | | | | | | | |
| 070A0h | — | ADC S/W RESET | SOFT | FREE | ACQ PRESCALE3 | ACQ PRESCALE2 | ACQ PRESCALE1 | ACQ PRESCALE0 | | |
| | CONV PRE- SCALE (CPS) | CONTIN- UOUS RUN | INT PRIORITY | SEQ1/2 CASCADE | CALIB EN | BRIDGE EN | HI / LO | FSTEST EN | | |
| 070A1h | EVB SOC EN SEQ1 | Reset SEQ1 Start CALIB | SOC SEQ1 | SEQ1 BUSY | INT ENA SEQ1 Mode1 | INT ENA SEQ1 Mode0 | INT FLAG SEQ1 | EVA SOC EN SEQ1 | | ADCCTRL2 |
| | EXT SOC EN SEQ1 | Reset SEQ2 | SOC SEQ2 | SEQ2 BUSY | INT ENA SEQ2 Mode1 | INT ENA SEQ2 Mode0 | INT FLAG SEQ2 | EVB SOC EN SEQ2 | | |
| 070A2h | — | — | — | — | — | — | — | — | | MAXCONV |
| | — | MAXCONV2 2 | MAXCONV2 1 | MAXCONV2 0 | MAXCONV1 3 | MAXCONV1 2 | MAXCONV1 1 | MAXCONV1 0 | | |
| 070A3h | CONV 3 | CONV 3 | CONV 3 | CONV 3 | CONV 2 | CONV 2 | CONV 2 | CONV 2 | | CHSELSEQ1 |
| | CONV 1 | CONV 1 | CONV 1 | CONV 1 | CONV 0 | CONV 0 | CONV 0 | CONV 0 | | |
| 070A4h | CONV 7 | CONV 7 | CONV 7 | CONV 7 | CONV 6 | CONV 6 | CONV 6 | CONV 6 | CHSELSEQ2 | |
| | CONV 5 | CONV 5 | CONV 5 | CONV 5 | CONV 4 | CONV 4 | CONV 4 | CONV 4 | | |
| 070A5h | CONV 11 | CONV 11 | CONV 11 | CONV 11 | CONV 10 | CONV 10 | CONV 10 | CONV 10 | CHSELSEQ3 | |
| | CONV 9 | CONV 9 | CONV 9 | CONV 9 | CONV 8 | CONV 8 | CONV 8 | CONV 8 | | |
| 070A6h | CONV 15 | CONV 15 | CONV 15 | CONV 15 | CONV 14 | CONV 14 | CONV 14 | CONV 14 | CHSELSEQ4 | |
| | CONV 13 | CONV 13 | CONV 13 | CONV 13 | CONV 12 | CONV 12 | CONV 12 | CONV 12 | | |
| 070A7h | — | — | — | — | SEQ CNTR3 | SEQ CNTR2 | SEQ CNTR1 | SEQ CNTR0 | AUTO_SEQ_SR | |
| | SEQ2 STATE 3 | SEQ2 STATE 2 | SEQ2 STATE 1 | SEQ2 STATE 0 | SEQ1 STATE 3 | SEQ1 STATE 2 | SEQ1 STATE 1 | SEQ1 STATE 0 | | |
| 070A8h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT0 | |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 070A9h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT1 | |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| 070AAh | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT2 | |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | | |

Indicates change with respect to the F243/F241, C242 device register maps.

TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP CONTROLLERS

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peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|------------------------|---|--------|--------|--------|--------|--------|-------|-------|-------------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| | ANALOG-TO-DIGITAL CONVERTER (ADC) REGISTERS (CONTINUED) | | | | | | | | |
| 070ABh | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT3 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070ACh | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT4 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070ADh | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT5 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070AEh | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT6 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 00 | 0 | |
| 070AFh | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT7 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B0h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT8 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B1h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT9 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B2h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT10 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B3h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT11 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B4h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT12 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B5h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT13 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B6h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT14 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B7h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | RESULT15 |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B8h | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | CALIBRATION |
| | D1 | D0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| 070B9h to 070FFh | Illegal | | | | | | | | |
| | CONTROLLER AREA NETWORK (CAN) CONFIGURATION CONTROL REGISTERS | | | | | | | | |
| 07100h | — | — | — | — | — | — | — | — | MDER |
| | MD3 | MD2 | ME5 | ME4 | ME3 | ME2 | ME1 | ME0 | |
| 07101h | TA5 | TA4 | TA3 | TA2 | AA5 | AA4 | AA3 | AA2 | TCR |
| | TRS5 | TRS4 | TRS3 | TRS2 | TRR5 | TRR4 | TRR3 | TRR2 | |
| 07102h | RFP3 | RFP2 | RFP1 | RFP0 | RML3 | RML2 | RML1 | RML0 | RCR |
| | RMP3 | RMP2 | RMP1 | RMP0 | OPC3 | OPC2 | OPC1 | OPC0 | |
| 07103h | — | — | SUSP | CCR | PDR | DBO | WUBA | CDR | MCR |
| | ABO | STM | — | — | — | — | MBNR1 | MBNR0 | |
| 07104h | — | — | — | — | — | — | — | — | BCR2 |
| | BRP7 | BRP6 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 | |

Indicates change with respect to the F243/F241, C242 device register maps.



peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|------------------------|---|---------|---------|---------|---------|---------|---------|---------|----------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| | CONTROLLER AREA NETWORK (CAN) CONFIGURATION CONTROL REGISTERS (CONTINUED) | | | | | | | | |
| 07105h | — | — | — | — | — | SBG | SJW1 | SJW0 | BCR1 |
| | SAM | TSEG1–3 | TSEG1–2 | TSEG1–1 | TSEG1–0 | TSEG2–2 | TSEG2–1 | TSEG2–0 | |
| 07106h | — | — | — | — | — | — | — | FER | ESR |
| | BEF | SA1 | CRCE | SER | ACKE | BO | EP | EW | |
| 07107h | — | — | — | — | — | — | — | — | GSR |
| | — | — | SMA | CCE | PDA | — | RM | TM | |
| 07108h | TEC7 | TEC6 | TEC5 | TEC4 | TEC3 | TEC2 | TEC1 | TEC0 | CEC |
| | REC7 | REC6 | REC5 | REC4 | REC3 | REC2 | REC1 | REC0 | |
| 07109h | — | — | MIF5 | MIF4 | MIF3 | MIF2 | MIF1 | MIF0 | CAN_IFR |
| | — | RMLIF | AAIF | WDIF | WUIF | BOIF | EPIF | WLIF | |
| 0710Ah | MIL | — | MIM5 | MIM4 | MIM3 | MIM2 | MIM1 | MIM0 | CAN_IMR |
| | EIL | RMLIM | AAIM | WDIM | WUIM | BOIM | EPIM | WLIM | |
| 0710Bh | LAMI | — | — | LAM0–28 | LAM0–27 | LAM0–26 | LAM0–25 | LAM0–24 | LAM0_H |
| | LAM0–23 | LAM0–22 | LAM0–21 | LAM0–20 | LAM0–19 | LAM0–18 | LAM0–17 | LAM0–16 | |
| 0710Ch | LAM0–15 | LAM0–14 | LAM0–13 | LAM0–12 | LAM0–11 | LAM0–10 | LAM0–9 | LAM0–8 | LAM0_L |
| | LAM0–7 | LAM0–6 | LAM0–5 | LAM0–4 | LAM0–3 | LAM0–2 | LAM0–1 | LAM0–0 | |
| 0710Dh | LAMI | — | — | LAM1–28 | LAM1–27 | LAM1–26 | LAM1–25 | LAM1–24 | LAM1_H |
| | LAM1–23 | LAM1–22 | LAM1–21 | LAM1–20 | LAM1–19 | LAM1–18 | LAM1–17 | LAM1–16 | |
| 0710Eh | LAM1–15 | LAM1–14 | LAM1–13 | LAM1–12 | LAM1–11 | LAM1–10 | LAM1–9 | LAM1–8 | LAM1_L |
| | LAM1–7 | LAM1–6 | LAM1–5 | LAM1–4 | LAM1–3 | LAM1–2 | LAM1–1 | LAM1–0 | |
| 0710Fh to 071FFh | Illegal | | | | | | | | |
| | Message Object #0 | | | | | | | | |
| 07200h | IDL–15 | IDL–14 | IDL–13 | IDL–12 | IDL–11 | IDL–10 | IDL–9 | IDL–8 | MSGID0L |
| | IDL–7 | IDL–6 | IDL–5 | IDL–4 | IDL–3 | IDL–2 | IDL–1 | IDL–0 | |
| 07201h | IDE | AME | AAM | IDH–28 | IDH–27 | IDH–26 | IDH–25 | IDH–24 | MSGID0H |
| | IDH–23 | IDH–22 | IDH–21 | IDH–20 | IDH–19 | IDH–18 | IDH–17 | IDH–16 | |
| 07202h | — | — | — | — | — | — | — | — | MSGCTRL0 |
| | — | — | — | RTR | DLC3 | DLC2 | DLC1 | DLC0 | |
| 07203h | Reserved | | | | | | | | |
| 07204h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX0A |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07205h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX0B |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07206h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX0C |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07207h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX0D |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

Indicates change with respect to the F243/F241, C242 device register maps.

TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP CONTROLLERS

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peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|---|----------|--------|--------|--------|--------|--------|--------|--------|----------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| CONTROLLER AREA NETWORK (CAN) CONFIGURATION CONTROL REGISTERS (CONTINUED) | | | | | | | | | |
| Message Object #1 | | | | | | | | | |
| 07208h | IDL-15 | IDL-14 | IDL-13 | IDL-12 | IDL-11 | IDL-10 | IDL-9 | IDL-8 | MSGID1L |
| | IDL-7 | IDL-6 | IDL-5 | IDL-4 | IDL-3 | IDL-2 | IDL-1 | IDL-0 | |
| 07209h | IDE | AME | AAM | IDH-28 | IDH-27 | IDH-26 | IDH-25 | IDH-24 | MSGID1H |
| | IDH-23 | IDH-22 | IDH-21 | IDH-20 | IDH-19 | IDH-18 | IDH-17 | IDH-16 | |
| 0720Ah | — | — | — | — | — | — | — | — | MSGCTRL1 |
| | — | — | — | RTR | DLC3 | DLC2 | DLC1 | DLC0 | |
| 0720Bh | Reserved | | | | | | | | |
| 0720Ch | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX1A |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0720Dh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX1B |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0720Eh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX1C |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0720Fh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX1D |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Message Object #2 | | | | | | | | | |
| 07210h | IDL-15 | IDL-14 | IDL-13 | IDL-12 | IDL-11 | IDL-10 | IDL-9 | IDL-8 | MSGID2L |
| | IDL-7 | IDL-6 | IDL-5 | IDL-4 | IDL-3 | IDL-2 | IDL-1 | IDL-0 | |
| 07211h | IDE | AME | AAM | IDH-28 | IDH-27 | IDH-26 | IDH-25 | IDH-24 | MSGID2H |
| | IDH-23 | IDH-22 | IDH-21 | IDH-20 | IDH-19 | IDH-18 | IDH-17 | IDH-16 | |
| 07212h | — | — | — | — | — | — | — | — | MSGCTRL2 |
| | — | — | — | RTR | DLC3 | DLC2 | DLC1 | DLC0 | |
| 07213h | Reserved | | | | | | | | |
| 07214h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX2A |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07215h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX2B |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07216h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX2C |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07217h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX2D |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Message Object #3 | | | | | | | | | |
| 07218h | IDL-15 | IDL-14 | IDL-13 | IDL-12 | IDL-11 | IDL-10 | IDL-9 | IDL-8 | MSGID3L |
| | IDL-7 | IDL-6 | IDL-5 | IDL-4 | IDL-3 | IDL-2 | IDL-1 | IDL-0 | |
| 07219h | IDE | AME | AAM | IDH-28 | IDH-27 | IDH-26 | IDH-25 | IDH-24 | MSGID3H |
| | IDH-23 | IDH-22 | IDH-21 | IDH-20 | IDH-19 | IDH-18 | IDH-17 | IDH-16 | |
| 0721Ah | — | — | — | — | — | — | — | — | MSGCTRL3 |
| | — | — | — | RTR | DLC3 | DLC2 | DLC1 | DLC0 | |
| 0721Bh | Reserved | | | | | | | | |
| 0721Ch | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX3A |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

Indicates change with respect to the F243/F241, C242 device register maps.



peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 BIT 7 | BIT 14 BIT 6 | BIT 13 BIT 5 | BIT 12 BIT 4 | BIT 11 BIT 3 | BIT 10 BIT 2 | BIT 9 BIT 1 | BIT 8 BIT 0 | REG |
|--|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|----------|
| CONTROLLER AREA NETWORK (CAN) CONFIGURATION CONTROL REGISTERS (CONTINUED) | | | | | | | | | |
| 0721Dh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX3B |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0721Eh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX3C |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0721Fh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX3D |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Message Object #4 | | | | | | | | | |
| 07220h | IDL-15 | IDL-14 | IDL-13 | IDL-12 | IDL-11 | IDL-10 | IDL-9 | IDL-8 | MSGID4L |
| | IDL-7 | IDL-6 | IDL-5 | IDL-4 | IDL-3 | IDL-2 | IDL-1 | IDL-0 | |
| 07221h | IDE | AME | AAM | IDH-28 | IDH-27 | IDH-26 | IDH-25 | IDH-24 | MSGID4H |
| | IDH-23 | IDH-22 | IDH-21 | IDH-20 | IDH-19 | IDH-18 | IDH-17 | IDH-16 | |
| 07222h | — | — | — | — | — | — | — | — | MSGCTRL4 |
| | — | — | — | RTR | DLC3 | DLC2 | DLC1 | DLC0 | |
| 07223h | Reserved | | | | | | | | |
| 07224h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX4A |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07225h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX4B |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07226h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX4C |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07227h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX4D |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Message Object #5 | | | | | | | | | |
| 07228h | IDL-15 | IDL-14 | IDL-13 | IDL-12 | IDL-11 | IDL-10 | IDL-9 | IDL-8 | MSGID5L |
| | IDL-7 | IDL-6 | IDL-5 | IDL-4 | IDL-3 | IDL-2 | IDL-1 | IDL-0 | |
| 07229h | IDE | AME | AAM | IDH-28 | IDH-27 | IDH-26 | IDH-25 | IDH-24 | MSGID5H |
| | IDH-23 | IDH-22 | IDH-21 | IDH-20 | IDH-19 | IDH-18 | IDH-17 | IDH-16 | |
| 0722Ah | — | — | — | — | — | — | — | — | MSGCTRL5 |
| | — | — | — | RTR | DLC3 | DLC2 | DLC1 | DLC0 | |
| 0722Bh | Reserved | | | | | | | | |
| 0722Ch | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX5A |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0722Dh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX5B |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0722Eh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX5C |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0722Fh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | MBX5D |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07230h to 073FFh | Illegal | | | | | | | | |

Indicates change with respect to the F243/F241, C242 device register maps.

TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP CONTROLLERS

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peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|------------------------|--|----------|----------|----------|----------|----------|----------|------------|---------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| | GENERAL-PURPOSE (GP) TIMER CONFIGURATION CONTROL REGISTERS – EVA | | | | | | | | |
| 07400h | — | T2STAT | T1STAT | — | | T2TOADC | | T1TOADC(1) | GPTCONA |
| | T1TOADC(0) | TCOMPOE | — | | T2PIN | | T1PIN | | |
| 07401h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T1CNT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07402h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T1CMPR |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07403h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T1PR |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07404h | FREE | SOFT | — | TMODE1 | TMODE0 | TPS2 | TPS1 | TPS0 | T1CON |
| | — | TENABLE | TCLKS1 | TCLKS0 | TCLD1 | TCLD0 | TECMPR | — | |
| 07405h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T2CNT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07406h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T2CMPR |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07407h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T2PR |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07408h | FREE | SOFT | — | TMODE1 | TMODE0 | TPS2 | TPS1 | TPS0 | T2CON |
| | T2SWT1 | TENABLE | TCLKS1 | TCLKS0 | TCLD1 | TCLD0 | TECMPR | SELT1PR | |
| 07409h to 07410h | Illegal | | | | | | | | |
| | FULL AND SIMPLE COMPARE UNIT REGISTERS – EVA | | | | | | | | |
| 07411h | CENABLE | CLD1 | CLD0 | SVENABLE | ACTRLD1 | ACTRLD0 | FCOMPOE | — | COMCONA |
| | — | — | — | — | — | — | — | — | |
| 07412h | Illegal | | | | | | | | |
| 07413h | SVRDIR | D2 | D1 | D0 | CMP6ACT1 | CMP6ACT0 | CMP5ACT1 | CMP5ACT0 | ACTRA |
| | CMP4ACT1 | CMP4ACT0 | CMP3ACT1 | CMP3ACT0 | CMP2ACT1 | CMP2ACT0 | CMP1ACT1 | CMP1ACT0 | |
| 07414h | Illegal | | | | | | | | |
| 07415h | — | — | — | — | DBT3 | DBT2 | DBT1 | DBT0 | DBTCONA |
| | EDBT3 | EDBT2 | EDBT1 | DBTPS2 | DBTPS1 | DBTPS0 | — | — | |
| 07416h | Illegal | | | | | | | | |
| 07417h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CMPR1 |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07418h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CMPR2 |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07419h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CMPR3 |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0741Ah to 0741Fh | Illegal | | | | | | | | |

Indicates change with respect to the F243/F241, C242 device register maps.

peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|------------------------|---|---------|----------|--------|-----------------|-----------------|-----------------|-----------------|----------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| | CAPTURE UNIT REGISTERS – EVA | | | | | | | | |
| 07420h | CAPRES | CAPQEPN | | CAP3EN | — | CAP3TSEL | CAP12TSEL | CAP3TOADC | CAPCONA |
| | CAP1EDGE | | CAP2EDGE | | CAP3EDGE | | — | | |
| 07421h | Illegal | | | | | | | | |
| 07422h | — | | CAP3FIFO | | CAP2FIFO | | CAP1FIFO | | CAPFIFOA |
| | — | — | — | — | — | — | — | — | |
| 07423h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP1FIFO |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07424h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP2FIFO |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07425h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP3FIFO |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07426h | Illegal | | | | | | | | |
| 07427h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP1FBOT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07428h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP2FBOT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07429h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP3FBOT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0742Ah to 0742Bh | Illegal | | | | | | | | |
| | EVENT MANAGER (EVA) INTERRUPT CONTROL REGISTERS | | | | | | | | |
| 0742Ch | — | — | — | — | — | T1OFINT ENA | T1UFINT ENA | T1CINT ENA | EVAIMRA |
| | T1PINT ENA | — | — | — | CMP3INT ENA | CMP2INT ENA | CMP1INT ENA | PDPINTA ENA | |
| 0742Dh | — | — | — | — | — | — | — | — | EVAIMRB |
| | — | — | — | — | T2OFINT ENA | T2UFINT ENA | T2CINT ENA | T2PINT ENA | |
| 0742Eh | — | — | — | — | — | — | — | — | EVAIMRC |
| | — | — | — | — | — | CAP3INT ENA | CAP2INT ENA | CAP1INT ENA | |
| 0742Fh | — | — | — | — | — | T1OFINT FLAG | T1UFINT FLAG | T1CINT FLAG | EVAIFRA |
| | T1PINT FLAG | — | — | — | CMP3INT FLAG | CMP2INT FLAG | CMP1INT FLAG | PDPINTA FLAG | |
| 07430h | — | — | — | — | — | — | — | — | EVAIFRB |
| | — | — | — | — | T2OFINT FLAG | T2UFINT FLAG | T2CINT FLAG | T2PINT FLAG | |
| 07431h | — | — | — | — | — | — | — | — | EVAIFRC |
| | — | — | — | — | — | CAP3INT FLAG | CAP2INT FLAG | CAP1INT FLAG | |
| 07432h to 074FFh | Illegal | | | | | | | | |

Indicates change with respect to the F243/F241, C242 device register maps.

TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP CONTROLLERS

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peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|--|------------|-----------|----------|----------|-----------|-----------|-----------|------------|---------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| GENERAL-PURPOSE (GP) TIMER CONFIGURATION CONTROL REGISTERS – EVB | | | | | | | | | |
| 07500h | — | T4STAT | T3STAT | — | | T4TOADC | | T3TOADC(1) | GPTCONB |
| | T3TOADC(0) | TCOMPOEB | — | | T4PIN | | T3PIN | | |
| 07501h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T3CNT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07502h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T3CMPR |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07503h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T3PR |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07504h | FREE | SOFT | — | TMODE1 | TMODE0 | TPS2 | TPS1 | TPS0 | T3CON |
| | — | TENABLE | TCLKS1 | TCLKS0 | TCLD1 | TCLD0 | TECMPR | — | |
| 07505h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T4CNT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07506h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T4CMPR |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07507h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | T4PR |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07508h | FREE | SOFT | — | TMODE1 | TMODE0 | TPS2 | TPS1 | TPS0 | T4CON |
| | T4SWT3 | TENABLE | TCLKS1 | TCLKS0 | TCLD1 | TCLD0 | TECMPR | SELT3PR | |
| 07509h to 07510h | Reserved | | | | | | | | |
| FULL AND SIMPLE COMPARE UNIT REGISTERS– EVB | | | | | | | | | |
| 07511h | CENABLE | CLD1 | CLD0 | SVENABLE | ACTRLD1 | ACTRLD0 | FCOMPOEB | — | COMCONB |
| | — | — | — | — | — | — | — | — | |
| 07512h | Reserved | | | | | | | | |
| 07513h | SVRDIR | D2 | D1 | D0 | CMP12ACT1 | CMP12ACT0 | CMP11ACT1 | CMP11ACT0 | ACTRB |
| | CMP10ACT1 | CMP10ACT0 | CMP9ACT1 | CMP9ACT0 | CMP8ACT1 | CMP8ACT0 | CMP7ACT1 | CMP7ACT0 | |
| 07514h | Reserved | | | | | | | | |
| 07515h | — | — | — | — | DBT3 | DBT2 | DBT1 | DBT0 | DBTCONB |
| | EDBT3 | EDBT2 | EDBT1 | DBTPS2 | DBTPS1 | DBTPS0 | — | — | |
| 07516h | Reserved | | | | | | | | |
| 07517h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CMPR4 |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07518h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CMPR5 |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07519h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CMPR6 |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0751Ah to 0751Fh | Reserved | | | | | | | | |

Indicates change with respect to the F243/F241, C242 device register maps.

peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|------------------|---|---------|----------|--------|--------------|--------------|--------------|--------------|----------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| | CAPTURE UNIT REGISTERS– EVB | | | | | | | | |
| 07520h | CAPRES | CAPQEPN | | CAP6EN | — | CAP6TSEL | CAP45SEL | CAP6TOADC | CAPCONB |
| | CAP4EDGE | | CAP5EDGE | | CAP6EDGE | | — | | |
| 07521h | Reserved | | | | | | | | |
| 07522h | — | | CAP6FIFO | | CAP5FIFO | | CAP4FIFO | | CAPFIFOB |
| | — | — | — | — | — | — | — | — | |
| 07523h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP4FIFO |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07524h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP5FIFO |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07525h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP6FIFO |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07526h | Reserved | | | | | | | | |
| 07527h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP4FBOT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07528h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP5FBOT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 07529h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | CAP6FBOT |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0752Ah to 0752Bh | Reserved | | | | | | | | |
| | EVENT MANAGER (EVB) INTERRUPT CONTROL REGISTERS | | | | | | | | |
| 0752Ch | — | — | — | — | — | T3OFINT ENA | T3UFINT ENA | T3CINT ENA | EVBIMRA |
| | T3PINT ENA | — | — | — | CMP6INT ENA | CMP5INT ENA | CMP4INT ENA | PDPINTB ENA | |
| 0752Dh | — | — | — | — | — | — | — | — | EVBIMRB |
| | — | — | — | — | T4OFINT ENA | T4UFINT ENA | T4CINT ENA | T4PINT ENA | |
| 0752Eh | — | — | — | — | — | — | — | — | EVBIMRC |
| | — | — | — | — | — | CAP6INT ENA | CAP5INT ENA | CAP4INT ENA | |
| 0752Fh | — | — | — | — | — | T3OFINT FLAG | T3UFINT FLAG | T3CINT FLAG | EVBIFRA |
| | T3PINT FLAG | — | — | — | CMP6INT FLAG | CMP5INT FLAG | CMP4INT FLAG | PDPINTB FLAG | |
| 07530h | — | — | — | — | — | — | — | — | EVBIFRB |
| | — | — | — | — | T4OFINT FLAG | T4UFINT FLAG | T4CINT FLAG | T4PINT FLAG | |
| 07531h | — | — | — | — | — | — | — | — | EVBIFRC |
| | — | — | — | — | — | CAP6INT FLAG | CAP5INT FLAG | CAP4INT FLAG | |
| 07532h to 0753Fh | Reserved | | | | | | | | |

Indicates change with respect to the F243/F241, C242 device register maps.

TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP CONTROLLERS

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peripheral register description (continued)

Table 19. LF240x DSP Peripheral Register Description (Continued)

| ADDR | BIT 15 | BIT 14 | BIT 13 | BIT 12 | BIT 11 | BIT 10 | BIT 9 | BIT 8 | REG |
|--------|--|-------------|-------------|-------------|---------------|---------------|---------------|---------------|-------|
| | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | |
| | PROGRAM MEMORY SPACE – FLASH REGISTERS | | | | | | | | |
| 0xx00h | — | — | — | — | — | — | — | — | PMPC |
| | — | — | — | — | PWR DWN | KEY1 | KEY0 | EXEC | |
| 0xx01h | — | — | — | — | — | — | WSVER EN | PRECND Mode1 | CTRL† |
| | PRECND Mode0 | ENG/R Mode2 | ENG/R Mode1 | ENG/R Mode0 | FCM3 | FCM2 | FCM1 | FCM0 | |
| 0xx02h | | | | | | | | | WADDR |
| 0xx03h | | | | | | | | | WDATA |
| 0xx04h | — | — | — | — | — | — | — | — | TCR |
| | — | — | — | — | — | — | — | — | |
| 0xx05h | — | — | — | — | — | — | — | — | ENAB |
| | — | — | — | — | — | — | — | — | |
| 0xx06h | — | — | — | — | — | — | — | — | SECT |
| | — | — | — | — | SECT 4 ENABLE | SECT 3 ENABLE | SECT 2 ENABLE | SECT 1 ENABLE | |
| | I/O MEMORY SPACE | | | | | | | | |
| 0FF0Fh | — | — | — | — | — | — | — | — | FCMR |
| | — | — | — | — | — | — | — | — | |
| | WAIT-STATE GENERATOR CONTROL REGISTER | | | | | | | | |
| 0FFFFh | — | — | — | — | — | BVIS.1 | BVIS.0 | ISWS.2 | WSGR |
| | ISWS.1 | ISWS.0 | DSWS.2 | DSWS.1 | DSWS.0 | PSWS.2 | PSWS.1 | PSWS.0 | |

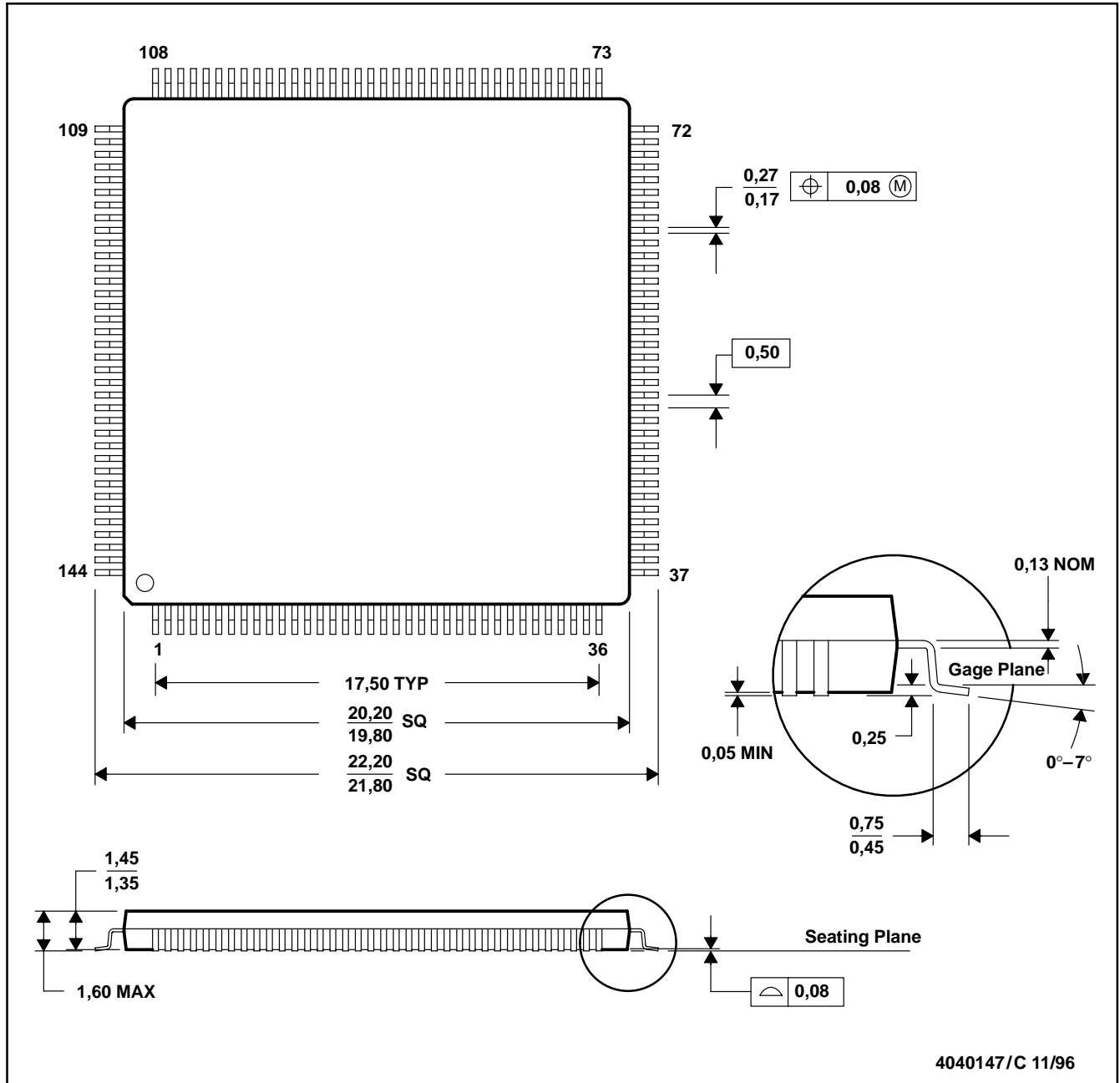
Indicates change with respect to the F243/F241, C242 device register maps.

† Register shown with bits set in **register mode**.

MECHANICAL DATA

PGE (S-PQFP-G144)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

Typical Thermal Resistance Characteristics

| PARAMETER | DESCRIPTION | °C/W |
|---------------|---------------------|------|
| Θ_{JA} | Junction-to-ambient | 32 |
| Θ_{JC} | Junction-to-case | 8 |

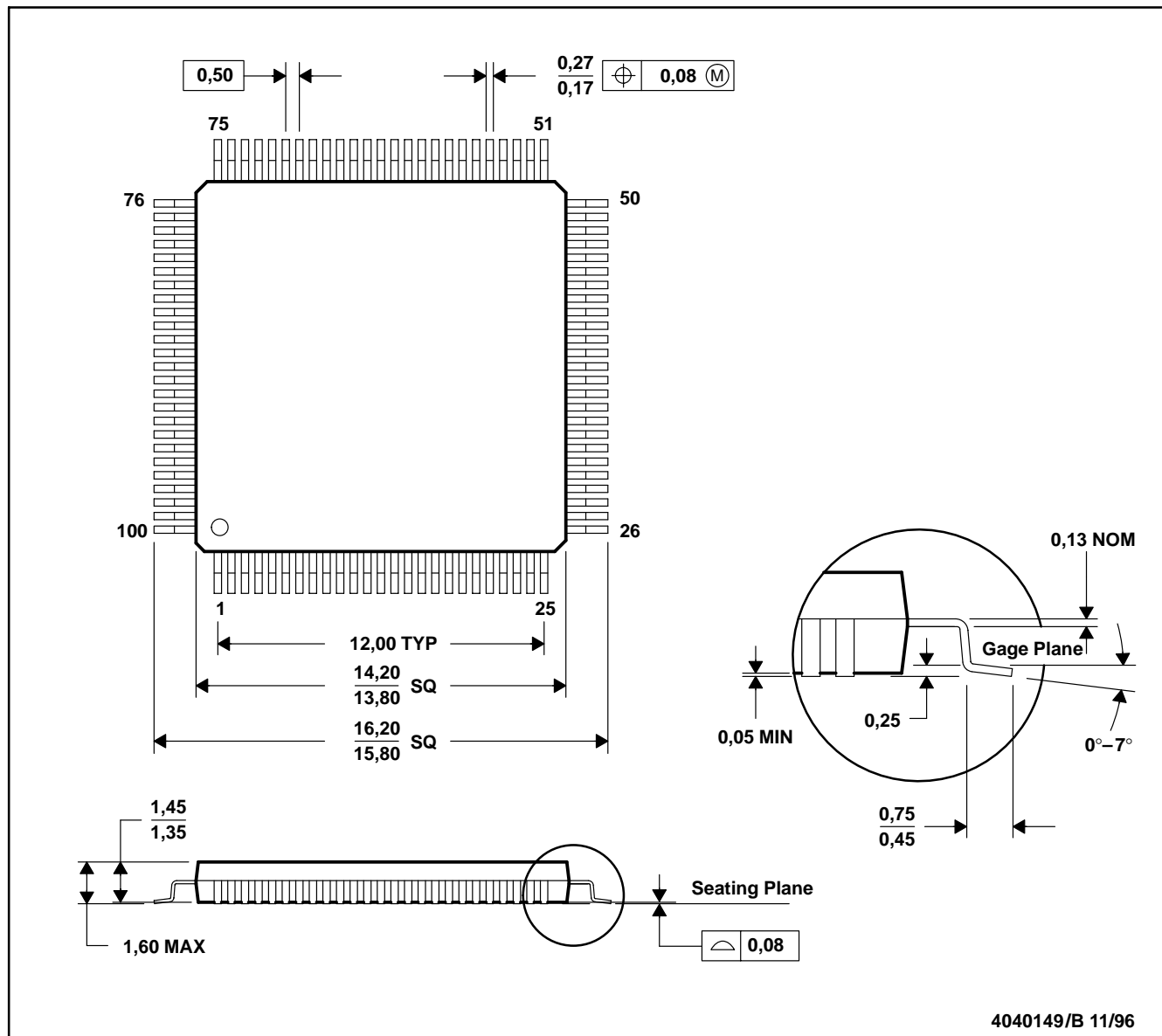
TMS320LF2407, TMS320LF2406, TMS320LF2402 DSP CONTROLLERS

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MECHANICAL DATA

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

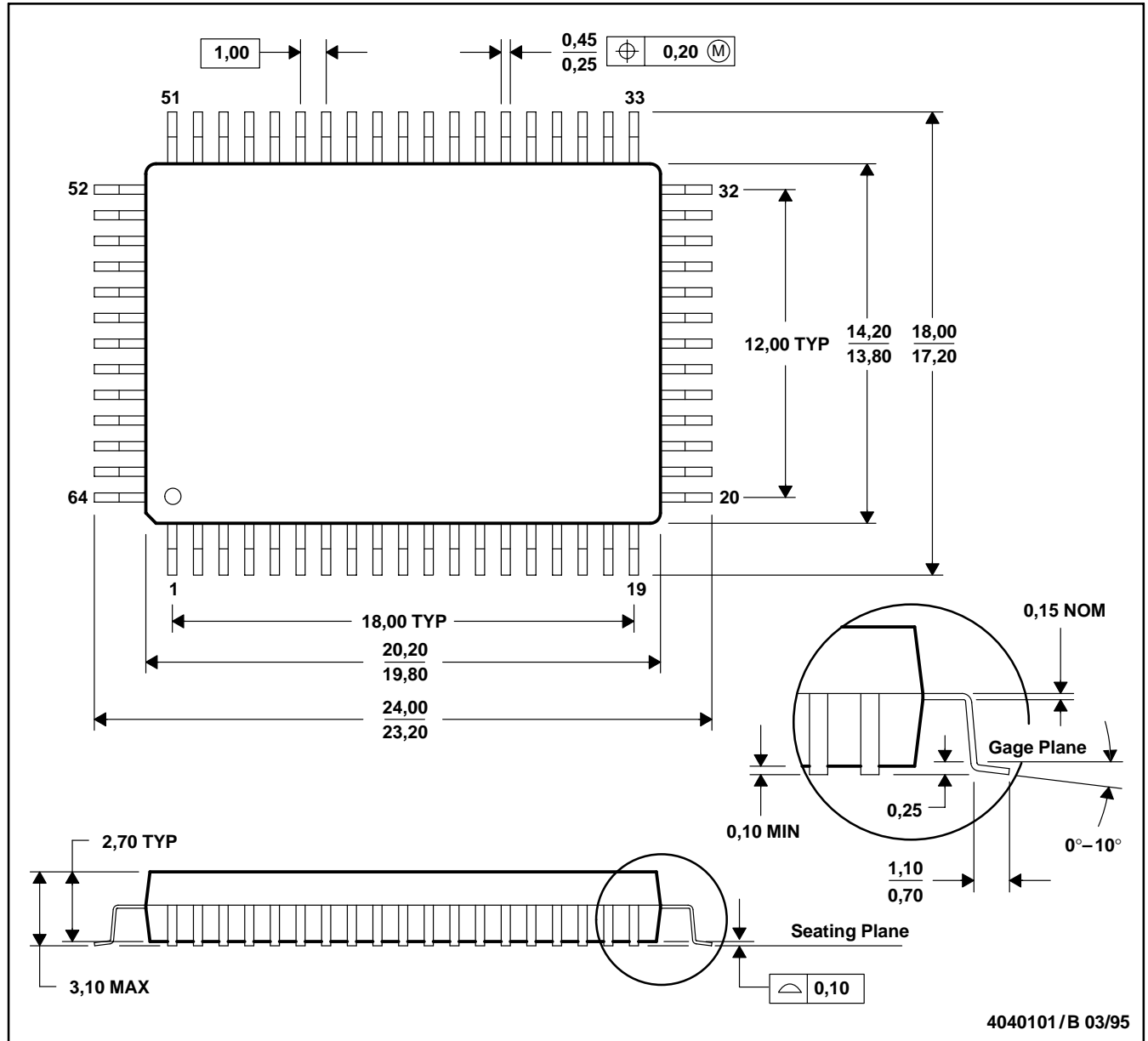
Typical Thermal Resistance Characteristics

| PARAMETER | DESCRIPTION | °C/W |
|---------------|---------------------|------|
| θ_{JA} | Junction-to-ambient | 42 |
| θ_{JC} | Junction-to-case | 8 |

MECHANICAL DATA

PG (R-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Contact field sales office to determine if a tighter coplanarity requirement is available for this package.

Typical Thermal Resistance Characteristics

| PARAMETER | DESCRIPTION | °C/W |
|---------------|---------------------|------|
| θ_{JA} | Junction-to-ambient | 35 |
| θ_{JC} | Junction-to-case | 11 |

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