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High stability current supply design for atomic resolution electron microscopy

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Abstract: An integrated ultra stable current supply architecture for use in atomic resolution electron microscopy has been proposed, designed, and simulated. The system is designed to have an overall stability of .01 ppm/°C, with similar stability for 20% changes in line voltage, and a drift in current of approximately 6×10^{-10} min^{-1}, all at 1 A output current.

Keywords: electron microscopy, high stability current supplies

Classification: Integrated circuits

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1 Introduction

With the advent of aberration corrected electron microscopes over the last half-decade and the quest for spatial resolution of atom dimensions (.05 nm) [1], the need for ultra stable current supplies for the magnetic lenses generally used to focus electrons becomes paramount. To reach the goal of 0.05 nm spatial resolution, the stability of the current in the final focusing

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electron lenses needs to be at least 0.01 ppm over many minutes and per degree C around room temperature. This is an order of magnitude better than the current supplies presently being used [2]. The current supply that will be described here must supply the coils of a multipolar magnet with the current necessary to generate the desired focusing magnetic field; this magnetic field must have better than 0.01 ppm stability over a wide range of temperature and input voltage variations. Linear current regulator supplies can fulfill these specifications but their low efficiency would increase the temperature inside the rack of power supplies such that current stability would be difficult to maintain because the control circuitry is thermally sensitive. Switch-mode current supplies have high efficiency, but their inherently noisy performance is incompatible with our stability requirements. Hence, in this paper the mixed linear-switch mode topology shown in Figure. 1 is proposed that combines the efficiency of switch mode regulator power supplies with the stability of linear regulator supplies.

2 Circuit analysis and design

The system was simulated using the standard Microsim PSPICE, using a 0.5 μm bipolar, CMOS, and DMOS (BCD) technology. The proposed block diagram of the current supply is shown in Fig. 1. The proposed load for this design is an inductor in the range of 10 mH to 10,000 mH with an Electrical Series Resistance (ESR) in the range of 1 to 5 ohms. No capacitance has been assumed in this simulation.

The system shown in Figure 1 is the proposed architecture of a linear mode (Current Regulator) and switch mode (Hysteretic Regulator) combination used to create a stable current. The Bandgap Voltage Reference Complex provides an ultra stable 600 mV reference voltage (0.003 ppm/°C)

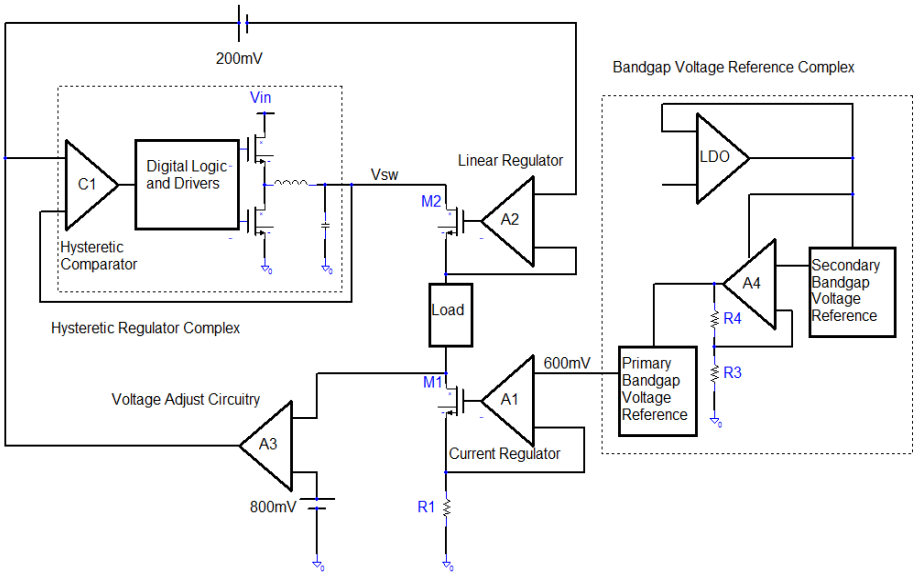

Fig. 1. The complete block diagram of the proposed mixed-mode current supply.

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to the amplifier A1 of the Current Regulator. The Primary Bandgap Voltage reference is a second order system where the non-linearity of the reference voltage to temperature variations is, to a large degree, corrected. In order to keep the 600 mV reference voltage as stable as possible, regardless of the input supply variations, the Primary Bandgap Voltage Reference is, first, isolated from the input supply by an internal LDO which creates a low voltage supply for the internal circuitries, including the Secondary Bandgap Voltage Reference and the amplifier A4. The Secondary Bandgap Voltage Reference and A4, in turn, power up the Primary Bandgap Voltage Reference.

The 600 mV is converted to a current by the relation:

$$I = V_{600\,mV}/R1 \tag{1}$$

In order to minimize the heat generation that can jeopardize the ultimate stability of the load current, the differential drain to source voltage of transistor M1 must be minimized as much as possible. Consequently, the Hysteretic Regulator steps down the input voltage until a 200 mV drain to source voltage across M1 is set. The Linear Regulator filters the noisy output of the Hysteretic Regulator as shown in Figure 2. Since the voltage across different loads can change, the output of the Hysteretic Regulator must adapt accordingly by varying its reference voltage. The reference voltages of the Hysteretic and Linear Regulators are driven by the output of an outer feedback control loop. The output of the Voltage Adjust Circuitry corrects until 800 mV is set at the drain of transistor M1. Consequently, the Hysteretic Regulator output adapts automatically to the load following the equation:

$$\begin{aligned} V_{sw} &= V_{\text{Primary BG}} + V_{\text{M1 (drain\_source)}} + R_{Load}I_{Load} \\ &\quad + V_{\text{M2 (drain\_source)}} \text{with } I_{Load} = V_{BG}/R1 \end{aligned} \tag{2}$$

MOSFETs M1 and M2 operate as linear regulators with drain-to-source voltages of only 200 mV, as shown in Figure 1, resulting in a highly efficient power supply. For this design, the following specifications were considered:

1. Input Voltage: $V_{in(max)} = 20\,V$ $V_{in(min)} = 4\,V$;
2. Output Voltage: $V_{out(max)} = 19\,V$ $V_{out(min)} = 1\,V$;
3. Load Current: 1 A.

The other advantage of using the Voltage Adjust Circuitry as a control element is an increase of the output impedance of the Current Regulator by the open loop gain of amplifier A3. This combination of switch mode power supplies with linear mode power supplies, results in better thermal and noise performance, and has been attempted before in such state of the art designs for stable voltage sources as the LTM8048 from Linear Technology Corporation [3]. In the particular architecture for this design, the input voltage is, with high efficiency ($< 95\%$), stepped down until the drain of transistor M1 is regulated at 800 mV. Unlike conventional Pulse Width Modulators, where

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the frequency is fixed, in Hysteretic Regulators the frequency is varied to obtain the desired output voltage. The switching frequency can be quantified through the following design equation:

$$\text{Frequency}_{(\text{Hysteretic\_Regulator})} = \frac{2\text{I}_{\text{out}}\left(\frac{\text{I}_{\text{peak\_PFM}}}{2} - \text{I}_{\text{out}}\right)}{\text{I}_{\text{peak\_PFM}}\text{xV}_{\text{r}}\text{xC}_{\text{out}}} \tag{3}$$

where $\text{I}_{\text{peak\_PFM}}$ is the inductor peak current and it is set to 4 A, V_{R} is the output peak to peak ripple of the hysteretic regulator which is set to be around 50 mV, and C_{out} is the output capacitor with a value of 800 uF. The design equation indicates a switching frequency of 12.5 KHz at an output current of 1 A. The Linear Regulator (A2, M2) filters the ripple generated by the Hysteretic Regulator, as shown in Figure 2, by the following relationship [4]:

$$\text{V}_{\text{out\_ripple}} = \frac{\frac{\text{R}_{\text{drain\_source\_M2}}}{\text{A}_{2(\text{s})}\beta}}{\text{R}_{\text{drain\_source\_M2}} + \frac{\text{R}_{\text{drain\_source\_M2}}}{\text{A}_{2(\text{s})}\beta}}\text{V}_{\text{in}_{\text{r}}\text{ipple}} \approx \frac{1}{\text{A}_{2(\text{s})}\beta}\text{V}_{\text{in\_ripple}} \tag{4}$$

where $\text{R}_{\text{drain\_source\_M2}}$ is 25 ohms, $\text{A2}_{(\text{s})}$ is the open loop gain of the wide band amplifier A2 at 12.5 KHz which is about 800 V/V, and β is the feedback factor that is unity.

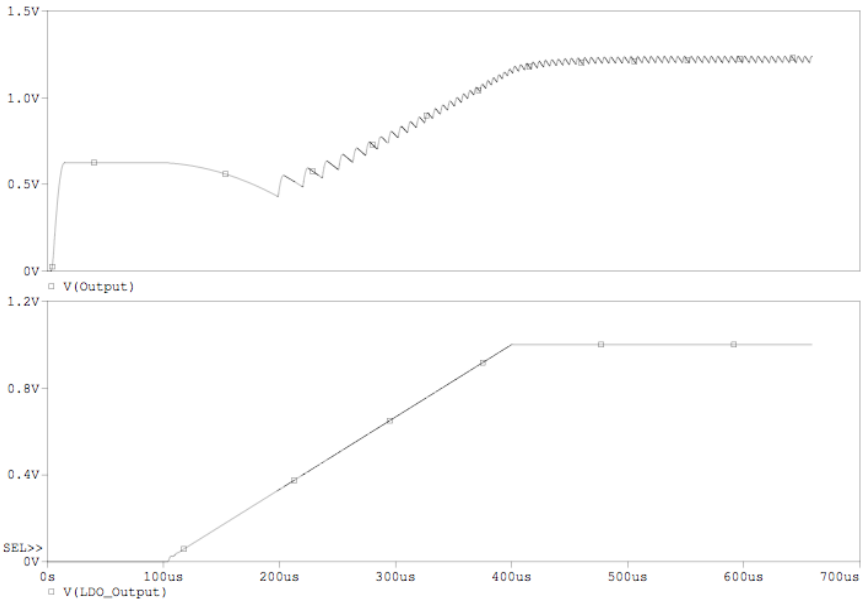

Fig. 2. Output of the Hysteretic Regulator on the top and output of the Linear Regulator on the bottom.

The ripple at the output of the Linear Regulator will be 62.5 uV. The ripple current generated through the load can be quantified by the following relationship:

$$\text{I}_{\text{ripple}} = \frac{\text{V}_{\text{out\_ripple}}}{\text{Output Impedance}} = \frac{\text{V}_{\text{out\_ripple}}}{\text{R}_{\text{drain\_source\_M1}} * (1 + \text{A1}_{(\text{s})}) * \text{A3}_{(\text{s})}} \tag{5}$$

where $\text{R}_{\text{drain\_source\_M1}}$ is 25 ohms, $\text{A1}_{(s)}$ is the open loop gain of amplifier A1 at 12.5 KHz which is about 3.16 dB, and $\text{A3}_{(s)}$ is the open loop gain of

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amplifier A3 at 12.5 KHz which is 40 dB. Consequently, the ripple current has been attenuated to a value of only 2.5 nA. If the input voltage to the system changes from 4 V to 20 V the load current will change by

$$\Delta I_{LOAD} = \frac{\Delta V_{DC}}{R_{drain_source\_M1} * (1 + A1_{DC}) * A3_{DC}} \tag{6}$$

where $A1_{(DC)}$ is the low frequency open loop gain of amplifier A1 which is 80 dB, and $A3_{(DC)}$ is the low frequency open loop gain of amplifier A3 that is 100 dB. The current change through the load as the result of this voltage variation will be 0.64 nA. Since the Secondary Bandgap Voltage Reference and A4 power up the Primary Bandgap Voltage Reference, the Power Supply Rejection Ratio (PSRR) of the complex is given by [5]:

$$PSRR_{COMPLEX} = PSRR_{LDO} * PSRR_{Secondary\ Bandgap} * PSRR_{Primary\ Bandgap} \tag{7}$$

where the low frequency $PSRR_{LDO}$ is 60 dB, $PSRR_{Secondary\ Bandgap}$ is 60 dB, and $PSRR_{Primary\ Bandgap}$ is 80 dB. The output voltage change as the result of DC input supply changes will then be:

$$\Delta V_{600\,mV} = \frac{\nabla V_{in}}{PSRR_{COMPLEX}} = \frac{16\,V}{200\,dB} = 1.6\,nV \tag{8}$$

3 Simulation results

According to the simulation results, the temperature stability of the load current is best between temperatures of 19°C to 22.5°C as shown in Figure 3 for the loads described in section 2. The temperature coefficient (TC) can be expressed by the following relationship:

$$TC_{ref} = \frac{1}{Reference} * \frac{\Delta Reference}{\Delta Temperature} = \frac{1}{1A}\frac{5\,nA}{2.5°C} = 3.33\,nA/°C \tag{9}$$

The effects of line regulation, temperature dependence can be summed up into one specification, the stability. Stability refers to total current variation and can be described by the total current variation shown in the following equation:

$$Stability(ppm) = \frac{I_{ripple} + \Delta I_{LOAD} + \frac{\Delta V_{600\,mV}}{600\,m\Omega} + TC_{ref} * \Delta T}{1\,A} * 10^6 \tag{10}$$

and this leads to a stability of 0.013 ppm at temperatures of 19°C to 22°C and ΔV_{LINE} of 4 V to 20 V.

The proposed architecture keeps the power loss at minimum (thus minimum heat production) by keeping the voltage drops across the linear power devices at 200 mV. The Linear power devices (M1 and M2) in this system are forced to operate with drain to source voltages of only 200 mV, and the hysteretic regulator operates with 95% efficiency. The proposed system has the temperature stability of 0.013 ppm at the temperature of 19°C to 22°C. However, in the case that the system is enclosed in the typical SOIC-8 package, the stability of 0.013 ppm at room temperature is not achievable due to a temperature rise of 22.5°C at 1 Amp output current. If such a package

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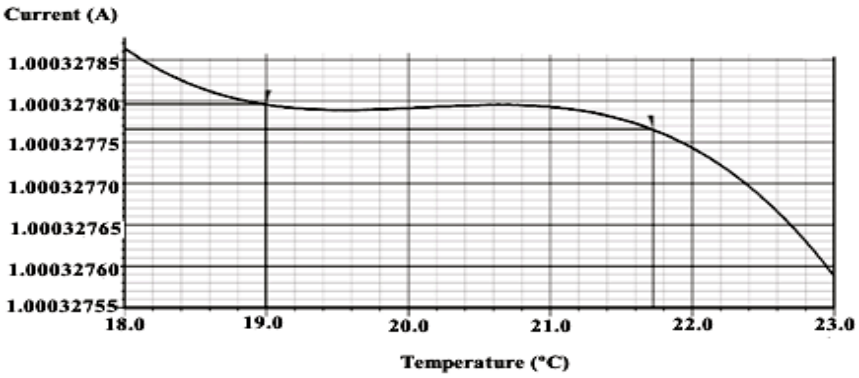

Fig. 3. Temperature dependence of the output current from the entire circuit showing a current stability of 0.01 ppm/°C in the range of 20.5 plus/minus 1 degree.

is used, this temperature rise could be compensated by enclosing the entire system in a temperature controlled environment, since a temperature control of only plus or minus 1.0°C is needed.

4 Conclusions

The proposed architecture shown in Fig. 1 plays a fundamental role in the success of this design. It combines the benefits of a linear system and a switching system to achieve the optimal conditions of a combined system. It minimizes the heat generation by using the switching method for stepping the voltage down and allows, but uses a manageable degree of heat generation. Then, the linear mode regulator filters the noise with the lowest amount of heat loss possible. The key properties of the current supply system such as its power supply rejection ratio, output impedance, linearity, and noise suppression are further enhanced by the open loop gain ($A_{3(s)}$) of the voltage adjust circuitry that is 80 dB in this design. The stability of the current is ultimately based upon the stability of the bandgap reference voltage complex. The proposed bandgap reference complex provides the 0.01 ppm/°C stability required for a highly stable voltage within the temperature range of 19.0°C to 22.0°C, where the current supply will be implemented. For higher power loads, where higher voltages are required, this particular architecture can be used with the exception that the power transistors must have higher voltage ratings. For that design, the switching transistors in the Hysteretic Regulator Complex and transistors M1 and M2 must be high voltage transistors. On all BCD processes, the availability of DMOS transistors will simplify this architectural modification.

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