

HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

FEATURES

- Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard
- Operate With a Single 3.3-V Supply
- Designed for Signaling Rate of up to 400 Mbps
- Differential Input Thresholds ± 100 mV Max
- Typical Propagation Delay Time of 2.1 ns
- Power Dissipation 60 mW Typical Per Receiver at 200 MHz
- Bus-Terminal ESD Protection Exceeds 8 kV
- Low-Voltage TTL (LVTTTL) Logic Output Levels
- Pin Compatible With AM26LS32, MC3486, and μ A9637
- Open-Circuit Fail-Safe

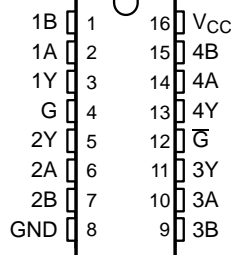
DESCRIPTION

The SN55LVDS32, SN65LVDS32, SN65LVDS3486, and SN65LVDS9637 are differential line receivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four differential receivers provides a valid logical output state with a ± 100 -mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.

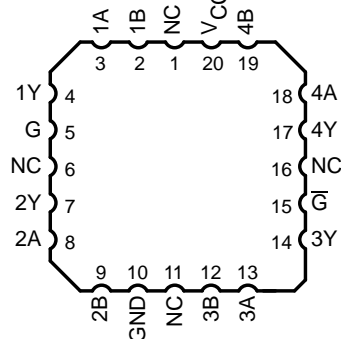
The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω . The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer depends on the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS32, SN65LVDS3486, and SN65LVDS9637 are characterized for operation from -40°C to 85°C . The SN55LVDS32 is characterized for operation from -55°C to 125°C .

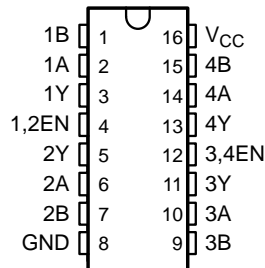
**SN55LVDS32 . . . J OR W
SN65LVDS32 . . . D OR PW**
(Marked as LVDS32 or 65LVDS32)
(TOP VIEW)



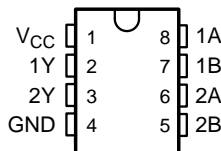
SN55LVDS32FK
(TOP VIEW)



SN65LVDS3486D (Marked as LVDS3486)
(TOP VIEW)



SN65LVDS9637D (Marked as DK637 or LVDS37)
SN65LVDS9637DGN (Marked as L37)
SN65LVDS9637DGK (Marked as AXF)
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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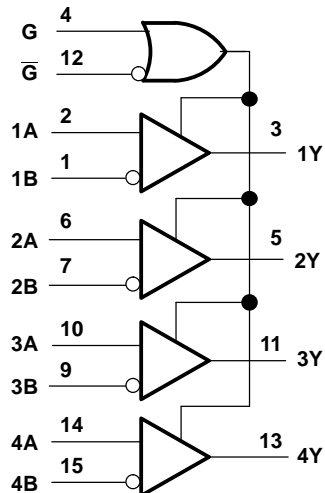


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

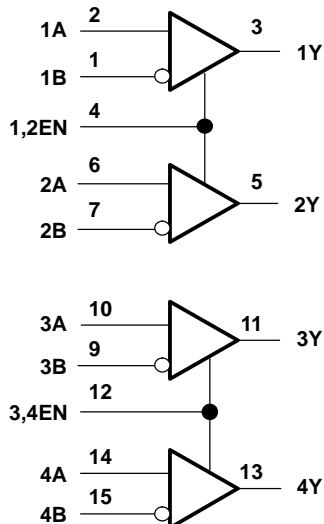
AVAILABLE OPTIONS

T _A	PACKAGE					
	SMALL OUTLINE		MSOP	CHIP CARRIER (FK)	CERAMIC DIP (J)	FLAT PACK (W)
	(D)	(PW)				
–40°C to 85°C	SN65LVDS32D	SN65LVDS32PW	—	—	—	—
	SN65LVDS3486D	—	—	—	—	—
	SN65LVDS9637D	—	SN65LVDS9637DGN	—	—	—
	—	—	SN65LVDS9637DGK	—	—	—
–55°C to 125°C	—	—	—	SNJ55LVDS32FK	SNJ55LVDS32J	SNJ55LVDS32W SN55LVDS32W

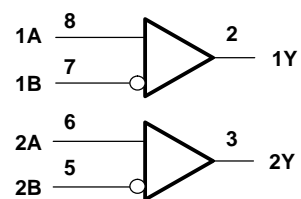
**'LVDS32 logic diagram
(positive logic)**



**SN65LVDS3486D logic diagram
(positive logic)**



**SN65LVDS9637D logic diagram
(positive logic)**

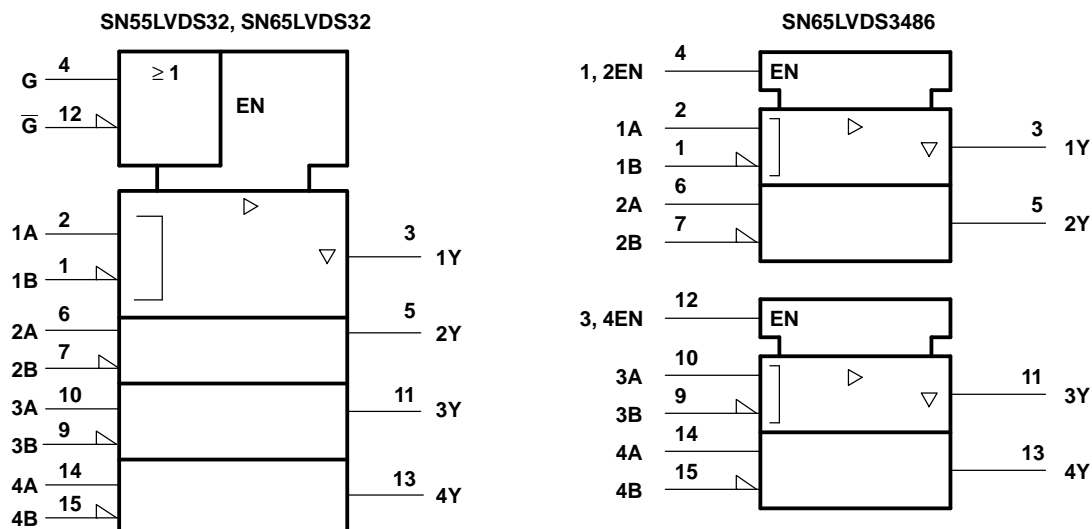


FUNCTION TABLES

SN55LVDS32, SN65LVDS32 ⁽¹⁾				SN65LVDS3486 ⁽¹⁾		
DIFFERENTIAL INPUT A, B	ENABLES		OUTPUT Y	DIFFERENTIAL INPUT A, B	ENABLE EN	OUTPUT Y
	G	Ḡ				
V _{ID} ≥ 100 mV	H	X	H	V _{ID} ≥ 100 mV	H	H
–100 mV < V _{ID} < 100 mV	H	X	?	–100 mV < V _{ID} < 100 mV	H	?
V _{ID} ≤ –100 mV	H	X	L	V _{ID} ≤ –100 mV	H	L
X	L	H	Z	X	L	Z
Open	H	X	H	Open	H	H
	X	L	H			

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

logic symbols†

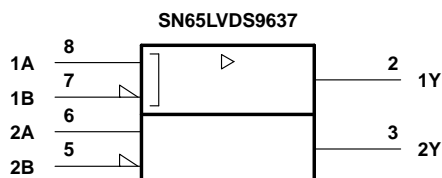


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Function Table
SN65LVDS9637

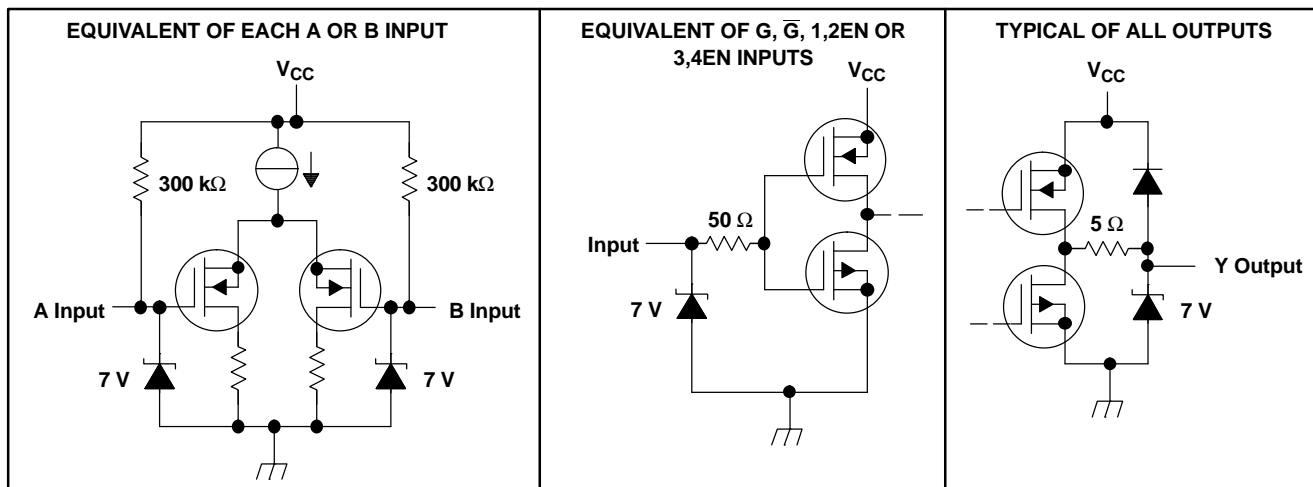
DIFFERENTIAL INPUT A, B	OUTPUT Y
$V_{ID} \geq 100 \text{ mV}$	H
$-100 \text{ mV} < V_{ID} < 100 \text{ mV}$?
$V_{ID} \leq -100 \text{ mV}$	L
Open	H
H = high level, L = low level, ? = indeterminate	

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		UNIT
V _{CC}	Supply voltage range ⁽²⁾	–0.5 V to 4 V
V _I	Input voltage range	–0.5 V to V _{CC} + 0.5 V
	Enables and output	–0.5 V to 4 V
Continuous total power dissipation		See Dissipation Rating Table
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C
T _{stg}	Storage temperature range	–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	—
D (16)	950 mW	7.6 mW/°C	608 mW	494 mW	—
DGK	425 mW	3.4 mW/°C	272 mW	221 mW	—
DGN ⁽²⁾	2.14 W	17.1 mW/°C	1.37 W	1.11 W	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
PW (16)	774 mW	6.2 mW/°C	496 mW	402 mW	—
W	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

- (1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.
- (2) The PowerPAD™ must be soldered to a thermal land on the printed-circuit board. See the application note *PowerPAD Thermally Enhanced Package* (SLMA002).

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	G, \overline{G} , 1,2EN, or 3,4EN	2			V
V_{IL}	Low-level input voltage	G, \overline{G} , 1,2EN, or 3,4EN			0.8	V
$ V_{ID} $	Magnitude of differential input voltage		0.1		0.6	V
V_{IC}	Common-mode input voltage (see Figure 1)		$\frac{ V_{ID} }{2}$	$2.4 - \frac{ V_{ID} }{2}$		V
				$V_{CC} - 0.8$		
T_A	Operating free-air temperature	SN65 prefix	–40		85	°C
		SN55 prefix	–55		125	

COMMON-MODE INPUT VOLTAGE RANGE vs DIFFERENTIAL INPUT VOLTAGE

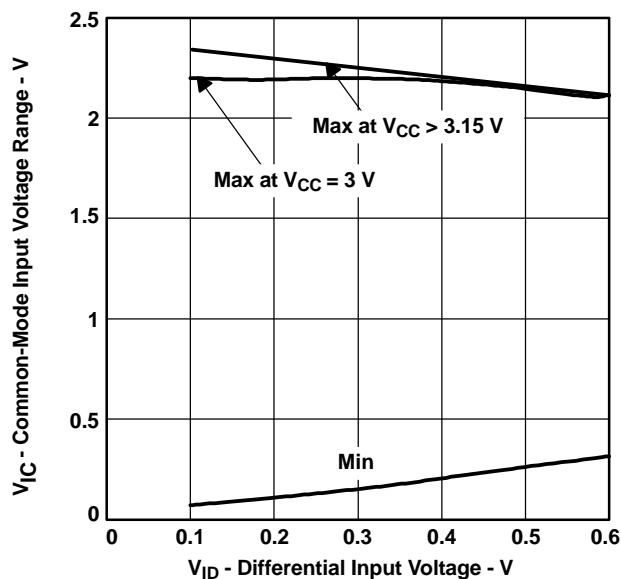


Figure 1. V_{IC} Versus V_{ID} and V_{CC}

SN55LVDS32 ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{ITH+} Positive-going differential input voltage threshold	See Figure 2, Table 1, and ⁽²⁾			100	mV
V _{ITH-} Negative-going differential input voltage threshold ⁽³⁾	See Figure 2, Table 1, and ⁽²⁾	–100			mV
V _{OH} High-level output voltage	I _{OH} = –8 mA	2.4			V
V _{OL} Low-level output voltage	I _{OL} = 8 mA			0.4	V
I _{CC} Supply current	Enabled, No load		10	18	mA
	Disabled		0.25	0.5	
I _I Input current (A or B inputs)	V _I = 0	–2	–10	–20	μA
	V _I = 2.4 V	–1.2	–3		
I _{I(OFF)} Power-off input current (A or B inputs)	V _{CC} = 0, V _I = 2.4 V		6	20	μA
I _{IH} High-level input current (EN, G, or \overline{G} inputs)	V _{IH} = 2 V			10	μA
I _{IL} Low-level input current (EN, G, or \overline{G} inputs)	V _{IL} = 0.8 V			10	μA
I _{OZ} High-impedance output current	V _O = 0 or V _{CC}			±12	μA

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

(2) |V_{ITH}| = 200 mV for operation at –55°C

(3) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

SN55LVDS32 SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} Propagation delay time, low-to-high-level output	C _L = 10 pF, See Figure 3	1.3	2.3	6	ns
t _{PHL} Propagation delay time, high-to-low-level output		1.4	2.2	6.1	ns
t _{sk(o)} Channel-to-channel output skew ⁽¹⁾			0.1		ns
t _r Output signal rise time, 20% to 80%			0.6		ns
t _f Output signal fall time, 80% to 20%			0.7		ns
t _{PHZ} Propagation delay time, high-level-to-high-impedance output	See Figure 4		6.5	12	ns
t _{PLZ} Propagation delay time, low-level-to-high-impedance output			5.5	12	ns
t _{PZH} Propagation delay time, high-impedance-to-high-level output			8	14	ns
t _{PZL} Propagation delay time, high-impedance-to-low-level output			3	12	ns

(1) t_{sk(o)} is the maximum delay time difference between drivers on the same device.

SN65LVDSxxxx ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LVDS32 SN65LVDS3486 SN65LVDS9637			UNIT
			MIN	TYP ⁽¹⁾	MAX	
V _{IT+}	Positive-going differential input voltage threshold	See Figure 2 and Table 1			100	mV
V _{IT-}	Negative-going differential input voltage threshold ⁽²⁾	See Figure 2 and Table 1	–100			mV
V _{OH}	High-level output voltage	I _{OH} = –8 mA	2.4			V
		I _{OH} = –4 mA	2.8			
V _{OL}	Low-level output voltage	I _{OL} = 8 mA			0.4	V
I _{CC}	Supply current	SN65LVDS32, SN65LVDS3486 Enabled, No load		10	18	mA
		Disabled		0.25	0.5	
		SN65LVDS9637 No load		5.5	10	
I _I	Input current (A or B inputs)	V _I = 0	–2	–10	–20	μA
		V _I = 2.4 V	–1.2	–3		
I _{I(OFF)}	Power-off input current (A or B inputs)	V _{CC} = 0, V _I = 3.6 V		6	20	μA
I _{IH}	High-level input current (EN, G, or \overline{G} inputs)	V _{IH} = 2 V			10	μA
I _{IL}	Low-level input current (EN, G, or \overline{G} inputs)	V _{IL} = 0.8 V			10	μA
I _{OZ}	High-impedance output current	V _O = 0 or V _{CC}			±10	μA

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

SN65LVDSxxxx SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LVDS32 SN65LVDS3486 SN65LVDS9637			UNIT
			MIN	TYP	MAX	
t _{PLH}	Propagation delay time, low-to-high-level output	C _L = 10 pF, See Figure 3	1.5	2.1	3	ns
t _{PHL}	Propagation delay time, high-to-low-level output		1.5	2.1	3	ns
t _{sk(p)}	Pulse skew (t _{PHL} – t _{PLH})			0	0.4	ns
t _{sk(o)}	Channel-to-channel output skew ⁽¹⁾			0.1	0.3	ns
t _{sk(pp)}	Part-to-part skew ⁽²⁾				1	ns
t _r	Output signal rise time, 20% to 80%			0.6		ns
t _f	Output signal fall time, 80% to 20%			0.7		ns
t _{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		6.5	12	ns
t _{PLZ}	Propagation delay time, low-level-to-high-impedance output			5.5	12	ns
t _{PZH}	Propagation delay time, high-impedance-to-high-level output			8	12	ns
t _{PZL}	Propagation delay time, high-impedance-to-low-level output			3	12	ns

(1) t_{sk(o)} is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

(2) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

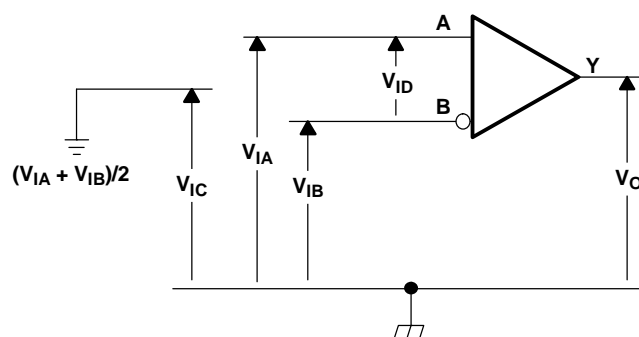
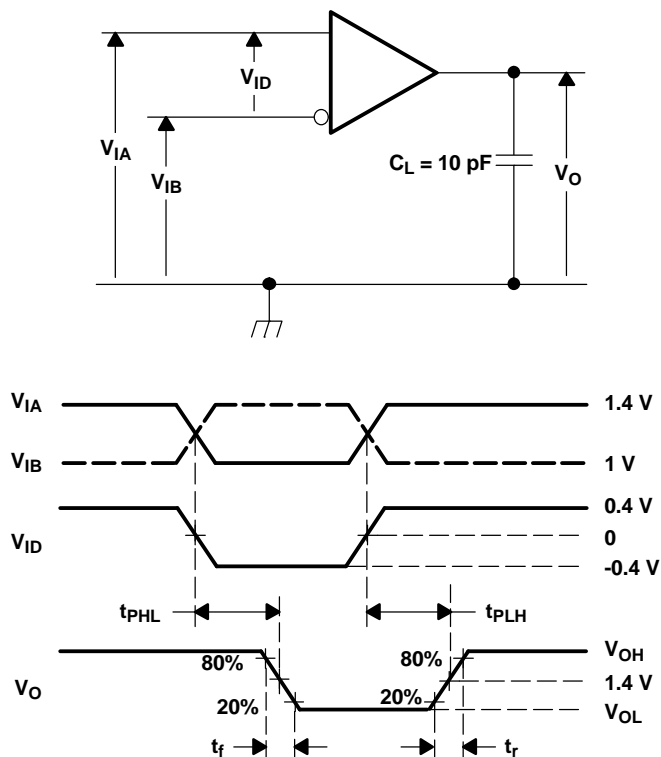


Figure 2. Voltage Definitions

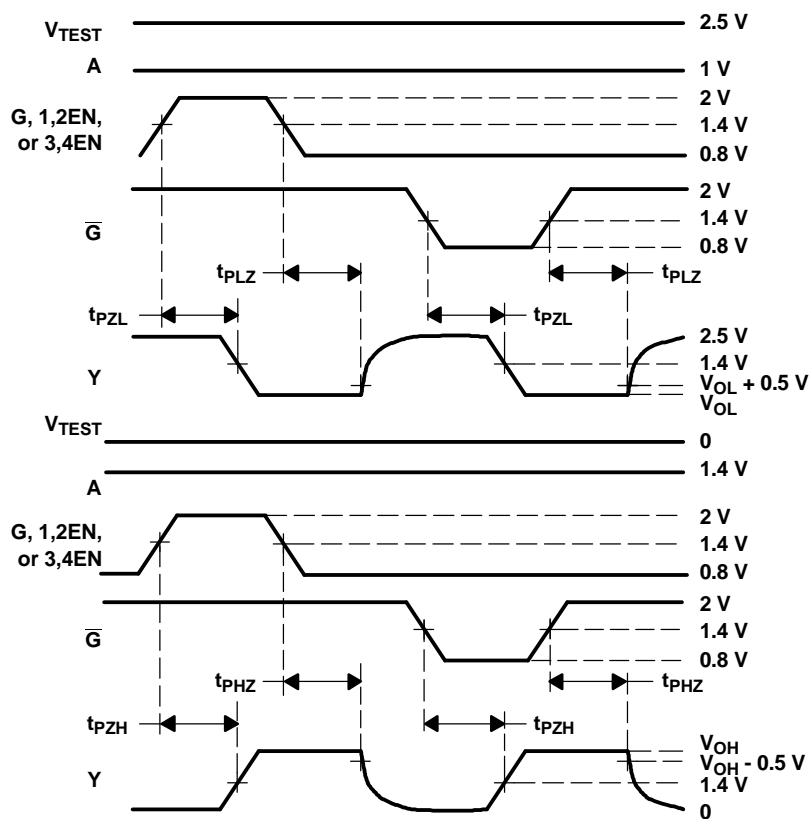
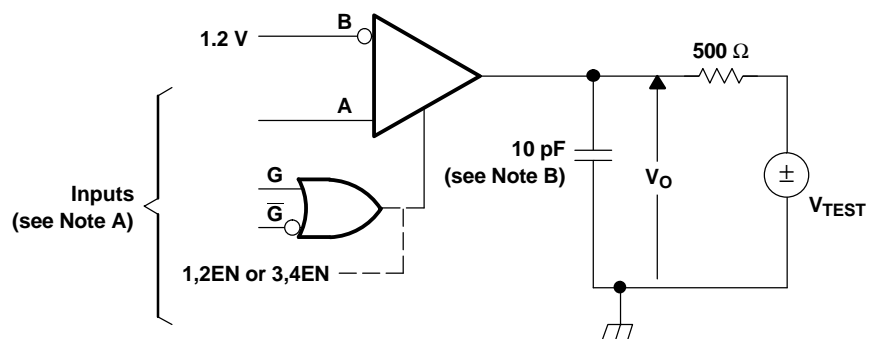
Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage
$V_{IA}(V)$	$V_{IB}(V)$	$V_{ID}(mV)$	$V_{IC}(V)$
1.25	1.15	100	1.2
1.15	1.25	-100	1.2
2.4	2.3	100	2.35
2.3	2.4	-100	2.35
0.1	0	100	0.05
0	0.1	-100	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3



- All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1 \text{ ns}$, pulse repetition rate (PRR) = 50 Mpps, pulse width = $10 \pm 0.2 \text{ ns}$.
- C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 3. Timing Test Circuit and Waveforms



- A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.
- B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable- and Disable-Time Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

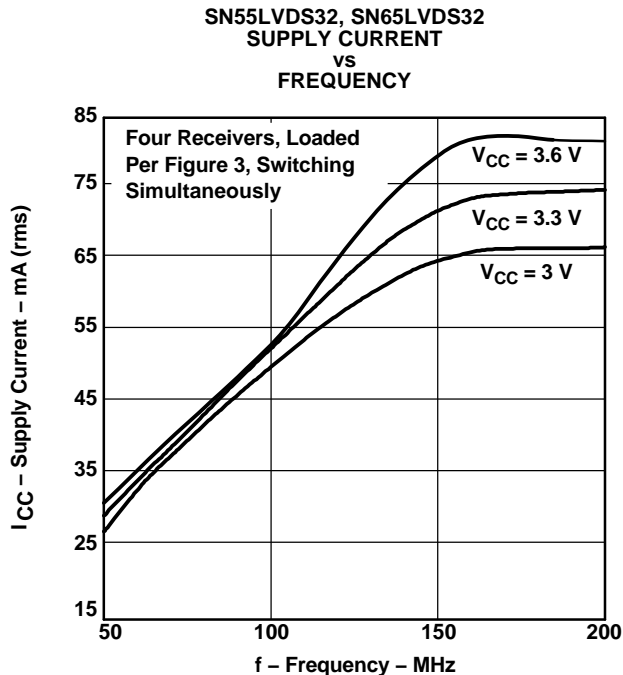


Figure 5.

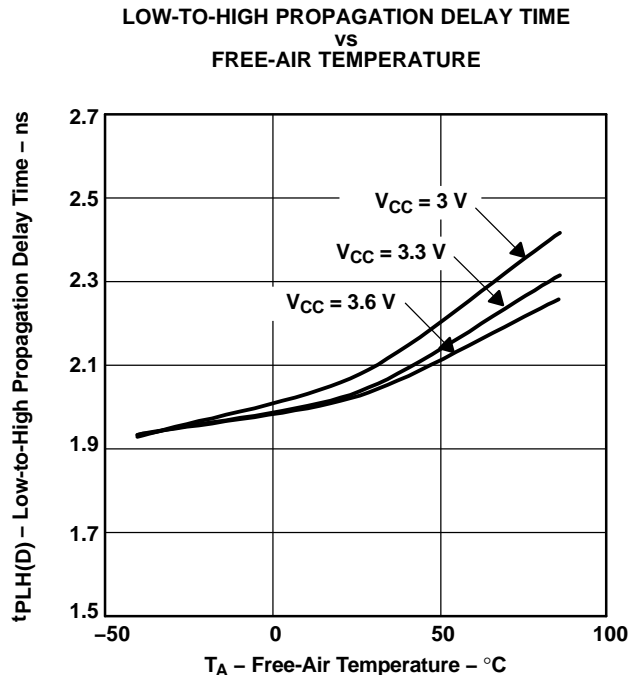


Figure 6.

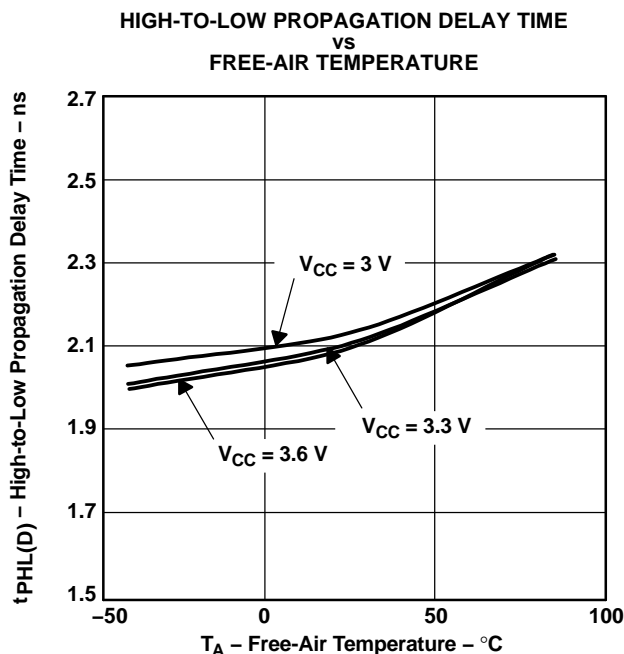


Figure 7.

TYPICAL CHARACTERISTICS (continued)

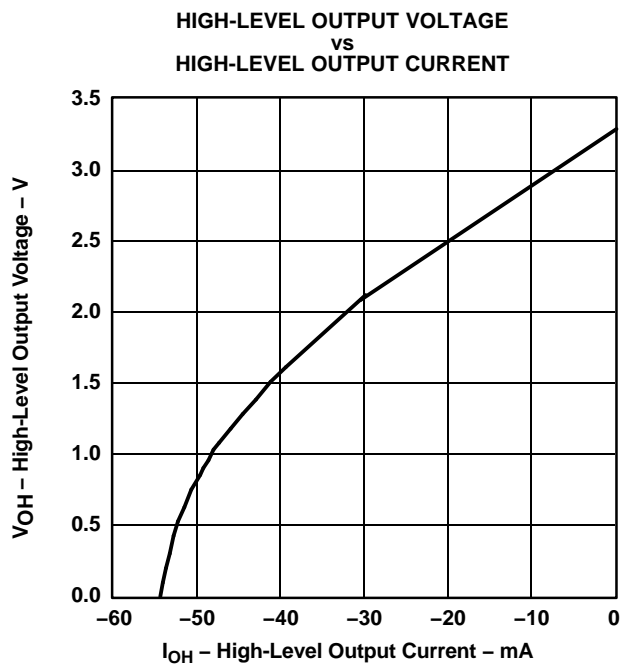


Figure 8.

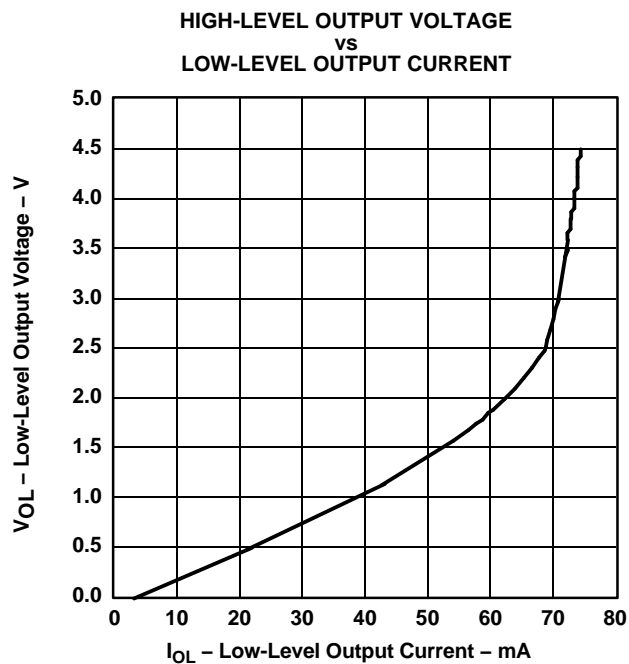


Figure 9.

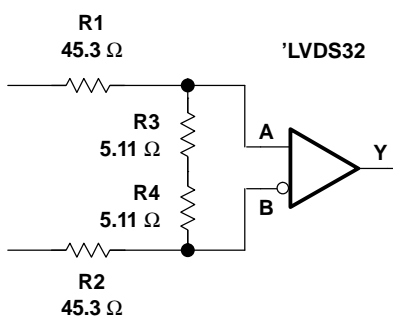
APPLICATION INFORMATION

USING AN LVDS RECEIVER WITH RS-422 DATA

Receipt of data from a TIA/EIA-422 line driver can be accomplished using a TIA/EIA-644 line receiver with the addition of an attenuator circuit. This technique gives the user a high-speed and low-power 422 receiver.

If the ground noise between the transmitter and receiver is not a concern (less than ± 1 V), the answer can be as simple as shown in Figure 10. A resistor divider circuit in front of the LVDS receiver attenuates the 422 differential signal to LVDS levels.

The resistors present a total differential load of $100\ \Omega$ to match the characteristic impedance of the transmission line and to reduce the signal 10:1. The maximum 422 differential output signal, or 6 V, is reduced to 600 mV. The high input impedance of the LVDS receiver prevents input bias offsets and maintains a greater than 200-mV differential input voltage threshold at the inputs to the divider. This circuit is used in front of each LVDS channel that also receives 422 signals.



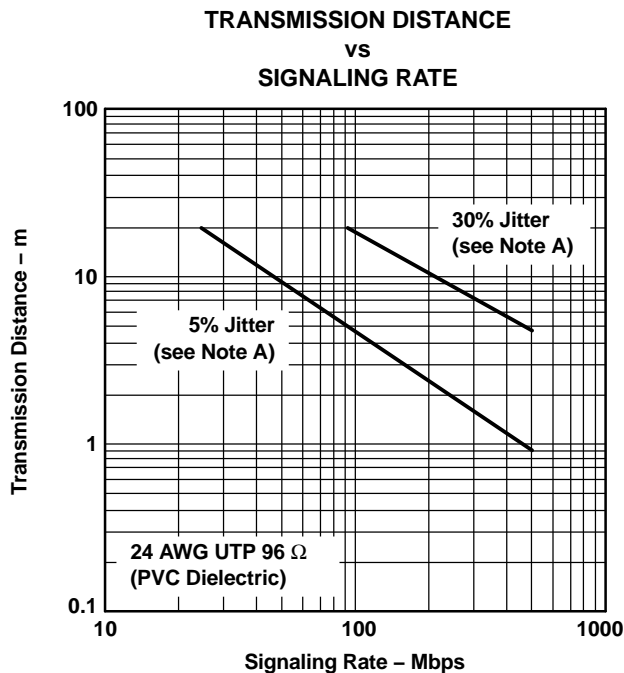
NOTE: The components used were standard values. (1) R1, R2 = NRC12F45R3TR, NIC components, 45.3 Ω , 1/8 W, 1%, 1206 package (2) R3, R4 = NRC12F5R11TR, NIC components, 5.11 Ω , 1/8 W, 1%, 1206 package (3) The resistor values do not need to be 1% tolerance. However, it can be difficult locating a supplier of resistors having values less than 100 Ω in stock and readily available. The user may find other suppliers with comparable parts having tolerances of 5% or even 10%. These parts are adequate for use in this circuit.

Figure 10. RS-422 Data Input to an LVDS Receiver Under Low Ground-Noise Conditions

If ground noise between the RS-422 driver and LVDS receiver is a concern, the common-mode voltage must be attenuated. The circuit must then be modified to connect the node between R3 and R4 to the LVDS receiver ground. This modification to the circuit increases the common-mode voltage from ± 1 V to greater than ± 4.5 V.

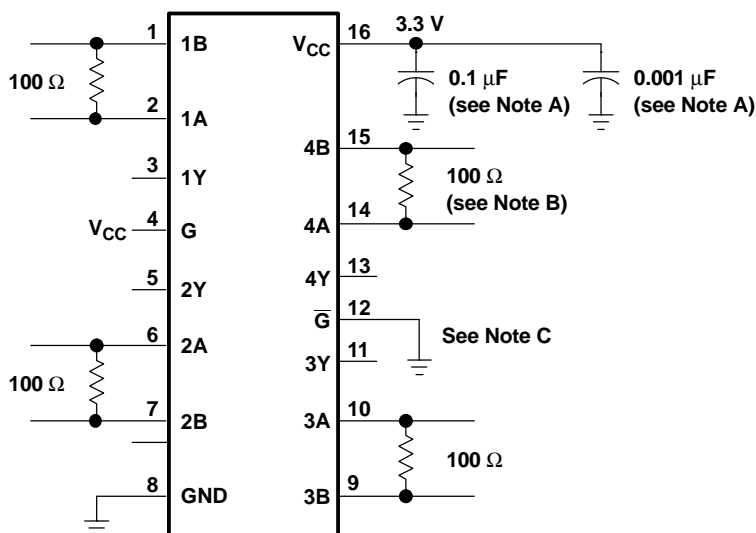
The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual-supply requirements.

APPLICATION INFORMATION (continued)



- A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

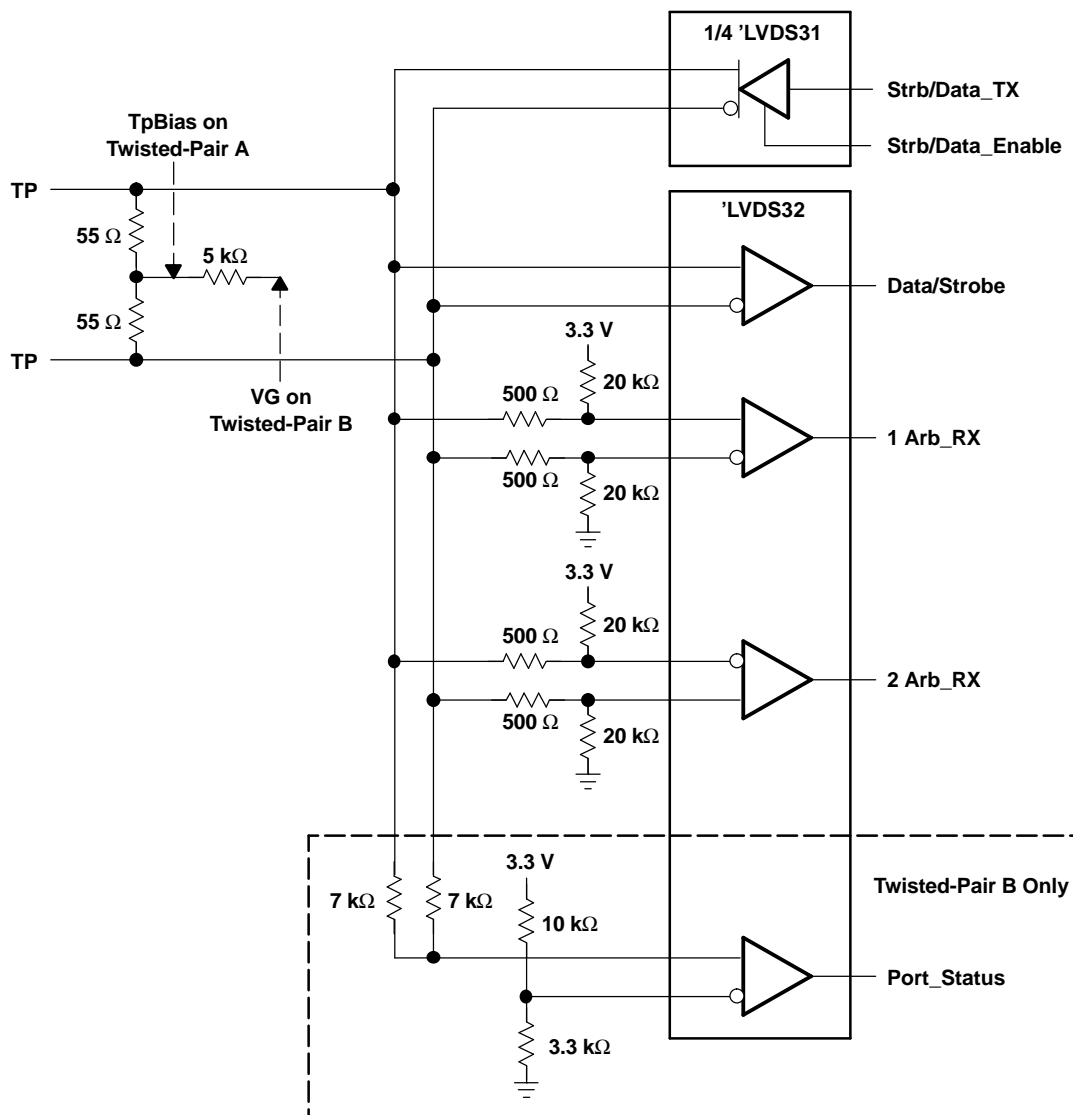
Figure 11. Typical Transmission Distance Versus Signaling Rate



- A. Place a 0.1- μ F and a 0.001- μ F Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
- B. The termination resistance value should match the nominal characteristic impedance of the transmission media with $\pm 10\%$.
- C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 12. Typical Application Circuit Schematic

APPLICATION INFORMATION



- A. Resistors are leadless, thick film (0603), 5% tolerance.
- B. Decoupling capacitance is not shown but recommended.
- C. V_{CC} is 3 V to 3.6 V.
- D. The differential output voltage of the 'LVDS31 can exceed that allowed by IEEE1394.

Figure 13. 100-Mbps IEEE 1394 Transceiver

FAIL-SAFE

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers in that its output logic state can be indeterminate when the differential input voltage is between -100 mV and 100 mV if it is within its recommended input common-mode voltage range. However, TI LVDS receivers handle the open-input circuit situation differently.

APPLICATION INFORMATION (continued)

Open-input circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near V_{CC} through 300-k Ω resistors (see Figure 14). The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level, regardless of the differential input voltage.

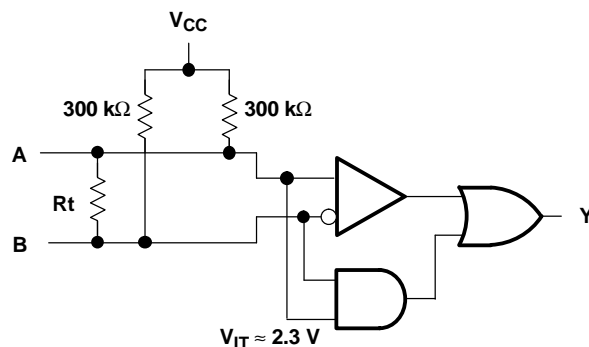
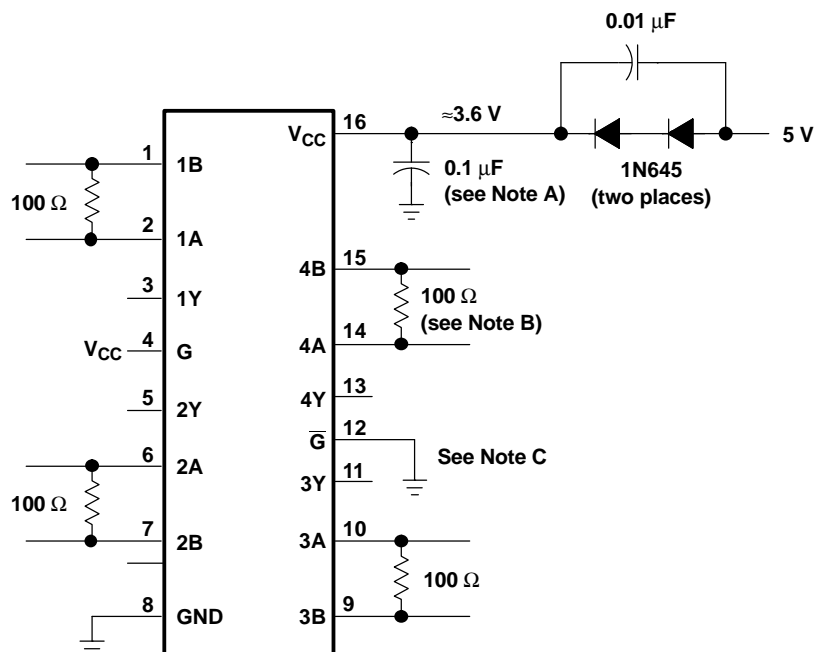


Figure 14. Open-Circuit Fail-Safe of LVDS Receiver

It is only under these conditions that the output of the receiver is valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, R_t , does not affect the fail-safe function as long as it is connected as shown in Figure 14. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.



- Place a 0.1- μ F Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.
- The termination resistance value should match the nominal characteristic impedance of the transmission media with $\pm 10\%$.
- Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 15. Operation With 5-V Supply

APPLICATION INFORMATION (continued)

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* ([SLLA014](#))
- *Interface Circuits for TIA/EIA-644 (LVDS)* ([SLLA038](#))
- *Reducing EMI With LVDS* ([SLLA030](#))
- *Slew Rate Control of LVDS Circuits* ([SLLA034](#))
- *Using an LVDS Receiver With TIA/EIA-422 Data* ([SLLA031](#))
- *Low Voltage Differential Signaling (LVDS) EVM* ([SLLA033](#))

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9762201Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9762201Q2A SNJ55 LVDS32FK	Samples
5962-9762201QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9762201QE A SNJ55LVDS32J	Samples
5962-9762201QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9762201QF A SNJ55LVDS32W	Samples
SN55LVDS32W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55LVDS32W	Samples
SN65LVDS32D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32	Samples
SN65LVDS32DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32	Samples
SN65LVDS32DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32	Samples
SN65LVDS32DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32	Samples
SN65LVDS32NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32	Samples
SN65LVDS32PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32	Samples
SN65LVDS32PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32	Samples
SN65LVDS32PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS32	Samples
SN65LVDS3486D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486	Samples
SN65LVDS3486DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486	Samples
SN65LVDS3486DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS3486DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3486	Samples
SN65LVDS9637D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637	Samples
SN65LVDS9637DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637	Samples
SN65LVDS9637DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF	Samples
SN65LVDS9637DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF	Samples
SN65LVDS9637DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF	Samples
SN65LVDS9637DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXF	Samples
SN65LVDS9637DGN	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37	Samples
SN65LVDS9637DGNG4	ACTIVE	MSOP- PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37	Samples
SN65LVDS9637DGNR	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37	Samples
SN65LVDS9637DGNRG4	ACTIVE	MSOP- PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L37	Samples
SN65LVDS9637DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637	Samples
SN65LVDS9637DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK637	Samples
SNJ55LVDS32FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9762201Q2A SNJ55 LVDS32FK	Samples
SNJ55LVDS32J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9762201QE A SNJ55LVDS32J	Samples
SNJ55LVDS32W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9762201QF A SNJ55LVDS32W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN55LVDS32 :

● Catalog: [SN75LVDS32](#)

● Space: [SN55LVDS32-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

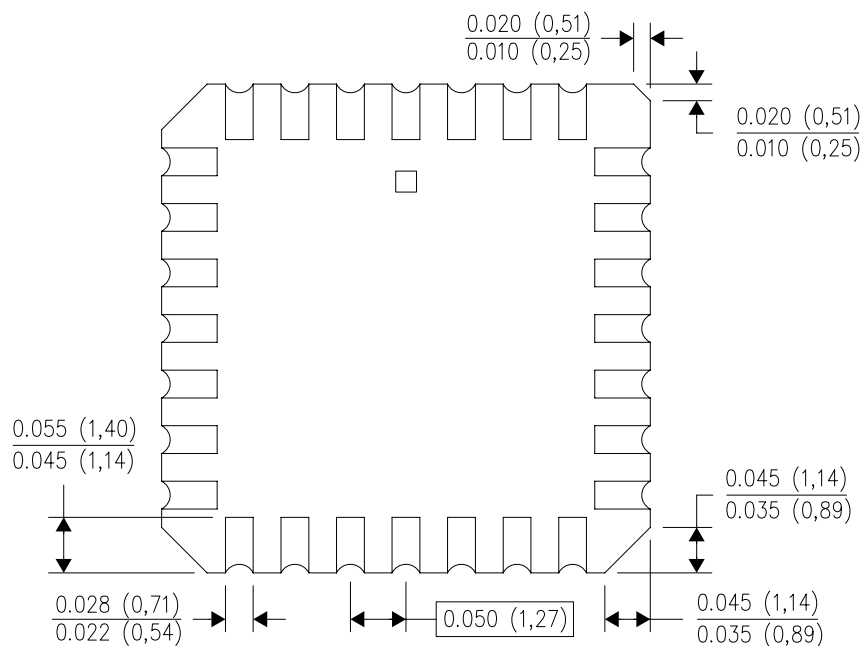
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

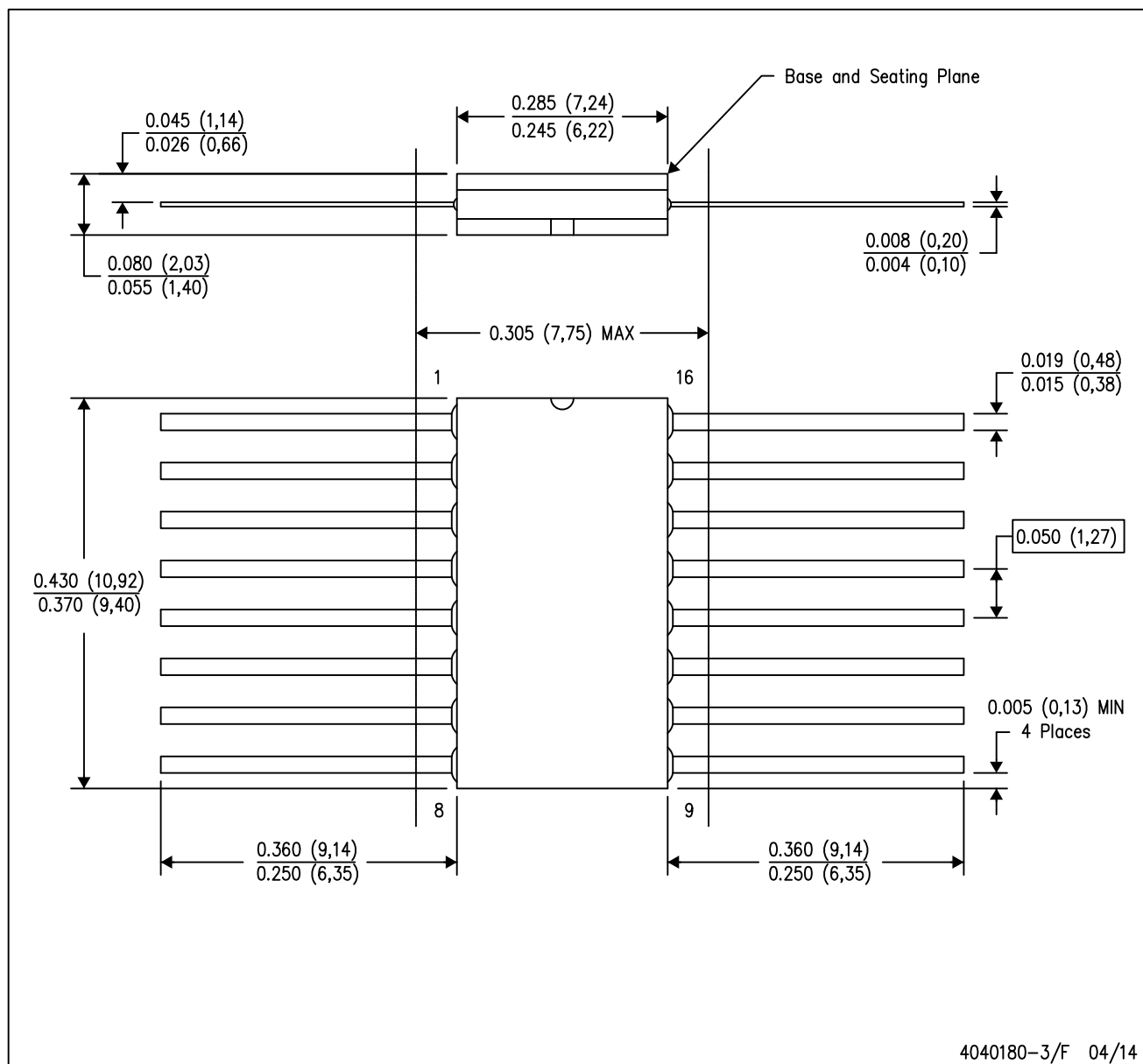
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

PW (R-PDSO-G16)

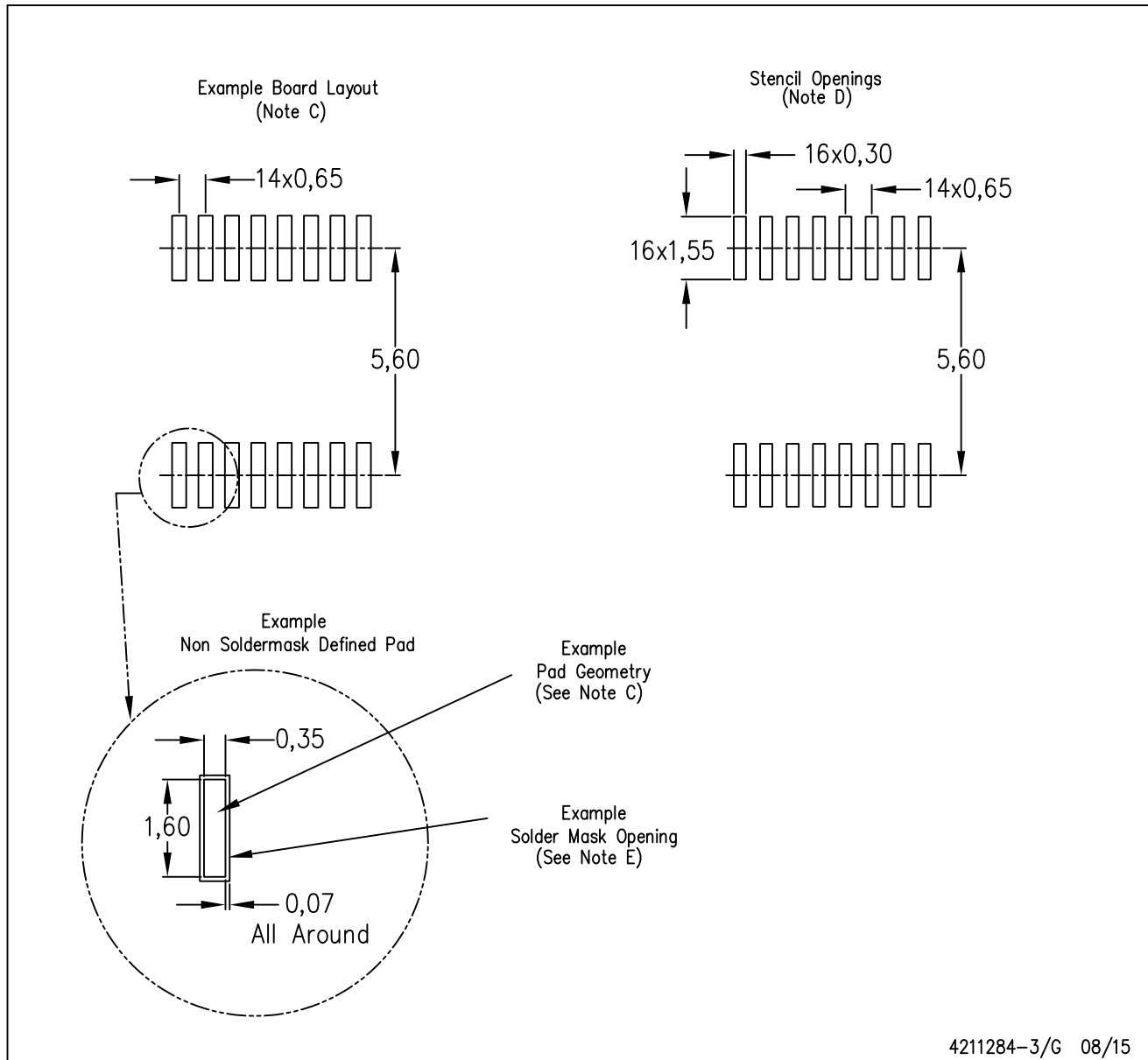
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

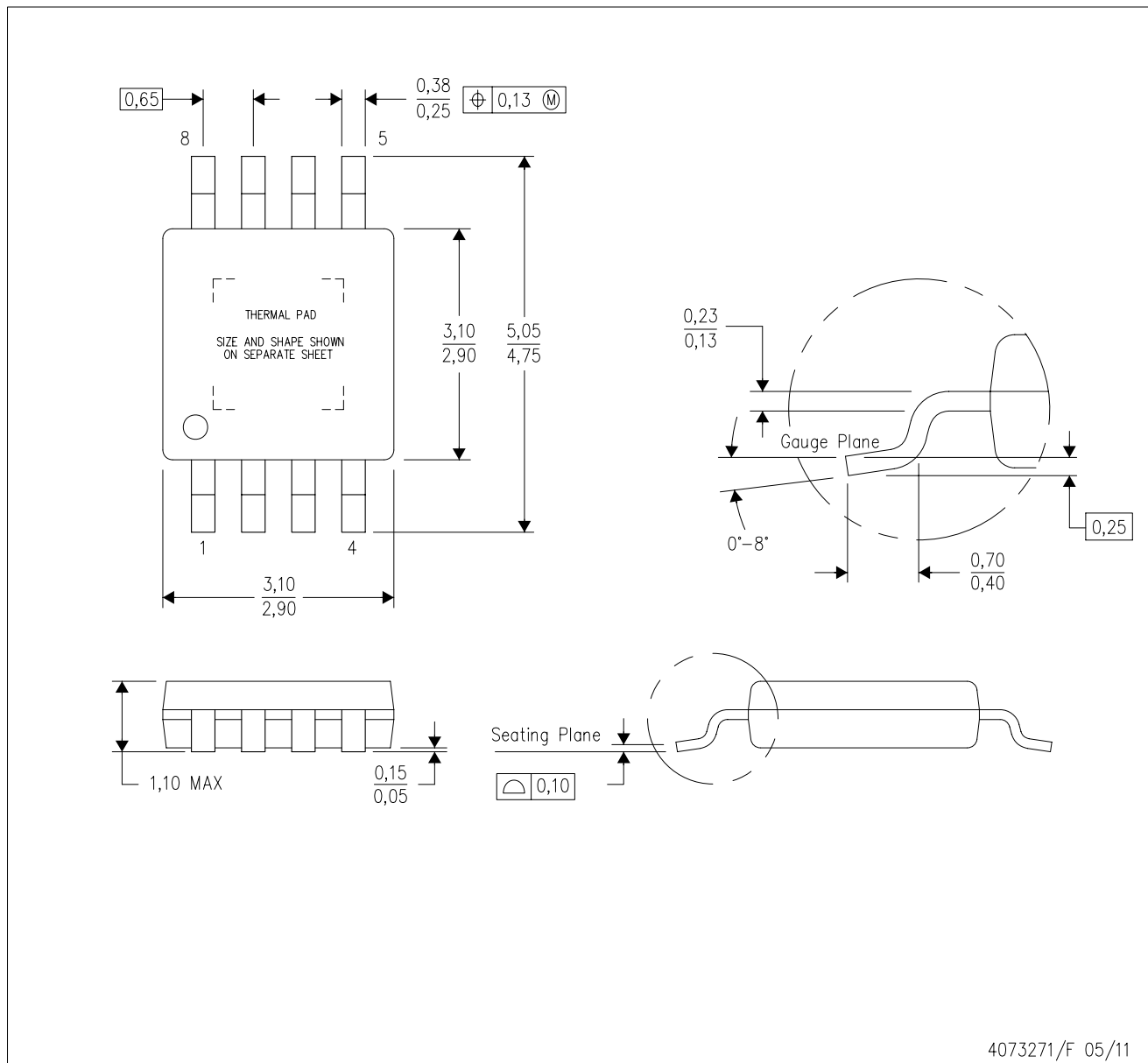


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGN (S-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

DGN (S-PDSO-G8)

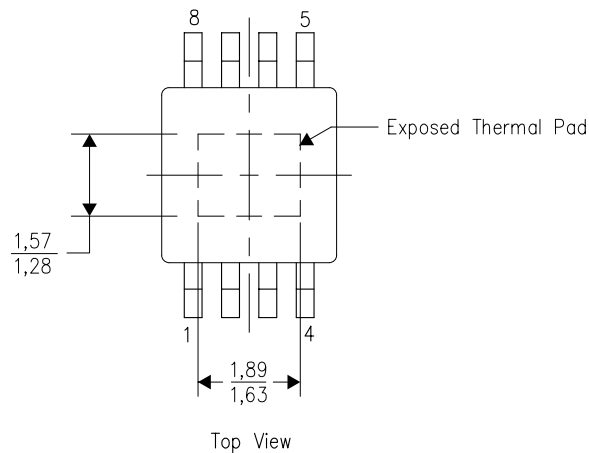
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

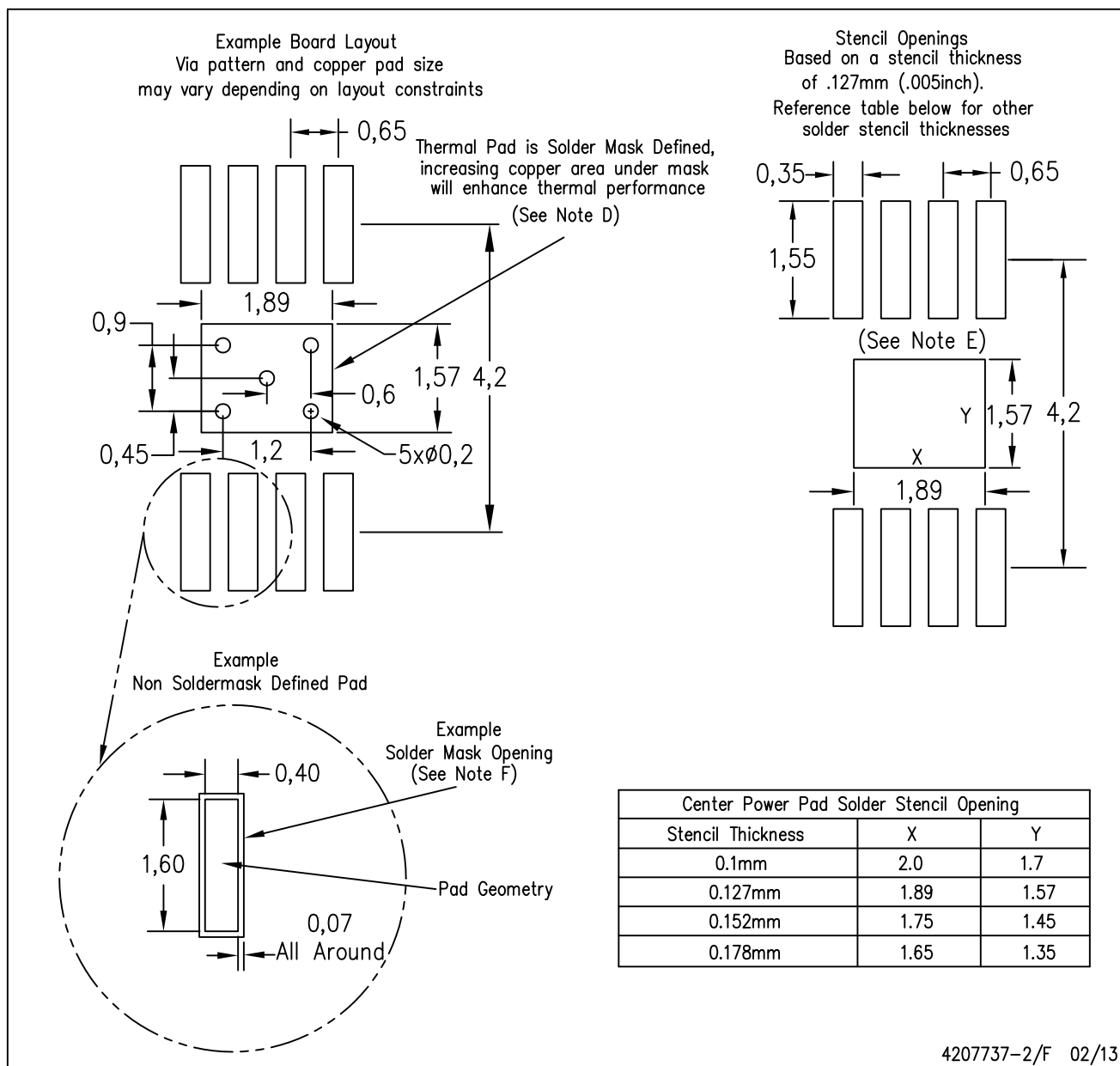
4206323-2/1 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL OUTLINE



4207737-2/F 02/13

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

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