Master of Science Thesis in Electrical Engineering
Department of Electrical Engineering, Linköping University, 2017

Power-Efficient Settling Time Reduction Techniques for a Folded-Cascode Amplifier in 1.8 V, 0.18 μm CMOS

Jimmy Johansson

LINKÖPING UNIVERSITY

Master of Science Thesis in Electrical Engineering

Power-Efficient
Settling Time Reduction Techniques for a
Folded-Cascode Amplifier in 1.8 V, 0.18 μm CMOS

Jimmy Johansson

LiTH-ISY-EX--17/5061--SE

Supervisor: **Dr. Prakash Harikumar**
Fingerprint Cards AB, Linköping
Martin Nielsen Lönn
ISY, Linköpings universitet

Examiner: **Dr. J Jacob Wikner**
ISY, Linköpings universitet

Division of Integrated Circuits and Systems
Department of Electrical Engineering
Linköping University
SE-581 83 Linköping, Sweden

Abstract

Testability is crucial in today's complex industrial system on chips (SoCs), where sensitive on-chip analog voltages need to be measured. In such cases, an operational amplifier (opamp) is required to sufficiently buffer the signals before they can drive the chip pad and probe parasitics. A single-stage opamp offers an attractive choice since it is power efficient and eliminates the need for frequency compensation. However, it has to satisfy demanding specifications on its stability, input common mode range, output swing, settling time, closed-loop gain and offset voltage. In this work, the settling time performance of a conventional folded-cascode (FC) opamp is substantially improved.

Settling time of an opamp consists of two major components, namely the slewing period and the linear settling period. In order to reduce the settling time significantly without incurring excessive area and power penalty, a prudent circuit implementation that minimizes both these constituents is essential. In this work, three different slew rate enhancement (SRE) circuits have been evaluated through extensive simulations. The SRE candidate providing robust slew rate improvement was combined with a current recycling folded cascode structure, resulting in lower slewing and linear settling time periods. Exhaustive simulations on a FC cascode amplifier with complementary inputs illustrate the effectiveness of these techniques in settling time reduction over all envisaged operating conditions.

Acknowledgments

It has been an challenging and interesting journey. I would like to give special thanks to the following persons for helping me throughout the work.

- Dr. Prakash Harikumar, Fingerprint Cards AB, for being my supervisor and for consistently being available with good advice during this work.
- Dr. J Jacob Wikner, Linköping University, for being my examiner.
- Carl-Fredrik Tengberg, Linköping University, for being my classmate over the years and for endless discussions about everything under the sun during this work.
- Jianxing Dai, Linköping University, for being my office-mate and opponent during this work.

Linköping, June 2017
Jimmy Johansson

Contents

List of Figures

List of Tables

Notation

Abbreviations

Abbreviations	Description
ADC	Analog-to-Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
DAC	Digital-to-Analog Converter
FC	Folded-Cascode
Hi-Lo	High to low transition
IC	Integrated Circuit
Lo-Hi	Low to high transition
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MUX	Multiplexer
NMOS	Negative-Channel Metal-Oxide Semiconductor
Opamp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PMOS	Positive-Channel Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PDK	Process Design Kit
RFC	Recycling Folded-Cascode
SoC	System-on-Chip
SR	Slew Rate
SRE	Slew Rate Enhancement

1

Introduction

This chapter will give the reader an insight of the thesis and cover the motivation and purpose for the specific problem statement, as well as the methodology that was used to achieve the final results. It will also give the reader an overview of how the document is organized.

1.1 Motivation and Purpose

Today's System-on-Chips (SoCs) are complex circuits which include numerous analog and digital functional blocks. In a commercial SoC, it is crucial to have the provision of external pins to monitor vital on-chip signals in order to enhance testability. For digital signals, buffers consisting of tapered inverters are typically used to drive the large capacitive load posed by the I/O pad and tester probe combination.

However, sensitive analog signals such as on-chip reference voltages require operational amplifiers to sufficiently buffer the signals before they can drive the chip pad and tester probe parasitics. In this case, the operational amplifier has to satisfy demanding specifications on its stability, input common range, bandwidth, settling time, closed-loop gain and offset voltage.

The next generation of mixed-signal integrated circuits (ICs) are calling for larger bandwidths and the ability to process high-frequency signals, which has led to higher demands on the speed of the buffer amplifier. The buffer amplifier must faithfully reproduce the input signal with a high degree of accuracy, which drives a large capacitive load. The buffer amplifier in some applications must be designed and optimized for settling time. Settling time is defined as time required to respond to a change of the amplifier input.

The purpose of this thesis is to investigate settling time reduction in a single-stage amplifier targeting a buffer application. The tasks involves literature survey to identify existing techniques on this topic and adapt the suitable candidate(s) to substantially reduce the settling time of a conventional folded-cascode amplifier without entailing large increase in area and excessive power consumption.

1.2 Background

Single-stage operational amplifiers (opamps) are widely used in SoCs due to their power efficiency while the satisfying crucial performance requirements in analog signal processing applications. As discussed in Chapter 1.1, faster settling time to the desired accuracy facilitates increased speed of analog signal processing.

In this work, the core of a folded-cascode (FC) amplifier with complementary inputs is available and the thesis investigates and implements the most power-and-area-efficient technique(s) for settling time improvement while avoiding degradation of other specifications in the given amplifier.

1.3 Problem Formulation

The goal of this thesis is to reduce the total settling time of a given amplifier design, by improving its small-signal and large-signal performance. Two different approaches is considered in order to reduce the settling time, an optimization of the given amplifier design and an introduction of settling time reduction technique(s) respectively.

The following questions will be considered in this thesis:

- How much can the settling time be reduced by optimizing the given amplifier design?
- Is there any settling time reduction technique(s) that can be introduced to the given amplifier design, and how much will it reduce the settling time?
- How much can the settling time be reduced with a combination of an improvement of the given design together with an settling time reduction technique?
- Is it possible to combine different settling time reduction techniques for better settling time reduction?

The changes done to the given amplifier and the introduction of different settling time reduction techniques must be implemented without a large increase in area and power consumption and also avoiding large degradation of other performance parameters.

1.4 Methodology

The adopted method consists of an initial literature survey about analog CMOS circuit design, in order to understand different architectures of the operational amplifier. Based on the implemented amplifier topology, important performance parameters for a folded-cascode amplifier were derived. Approximate expressions for small-signal and large-signal performance parameters were obtained. The purpose of these derivations was to obtain different handles to use in order to tune the performance of the amplifier.

Simultaneously, simulations on the implemented structure were executed to familiarize with the impact of design choices and the process design kit (PDK) parameters. The simulation scenarios included different Process corners, supply Voltage variations and the relevant Temperature ranges, i.e. PVT variations. Monte Carlo simulations over worst-case temperature and supply voltage conditions were also executed, in order to evaluate the impact of device mismatch.

While characterizing the existing amplifier, a literature survey about settling time reduction techniques was also done. Several scientific papers and articles proposed different techniques to boost the slew rate, without affecting other performance parameters of an already implemented amplifier. Other papers and articles also proposed a modified structure of the conventional folded-cascode, in order to achieve a general performance enhancement, called the recycling folded-cascode amplifier. The task was to understand, assess and incorporate these techniques. Four different techniques and structure were evaluated, due to its promising proposed results and the ease of implementation. To achieve as large improvement necessary for the settling time specification, a combination of device size optimization of the existing amplifier, implementation of a slew rate enhancement technique, and implementation of a recycling folded-cascode structure was done.

1.5 Organization and Scope

The thesis lays emphasis on the settling time reduction for a single-stage folded-cascode amplifier. It will present several slew rate enhancement (SRE) solutions that can be applied to an existing amplifier. The different techniques will be described and analyzed over process, supply voltage and temperature (PVT) variations, and device mismatch conditions. The thesis will present the most suitable and robust solution for settling time reduction in a folded-cascode amplifier, together with simulation results on a transistor schematic level. Chapters 2-4 in this document will cover the background and theory, and Chapter 5 will describe the method used in this thesis. The simulation results together with a discussion will be presented in Chapter 6, and future work directions will be presented in Chapter 7.

The thesis is organized as followed.

- **Chapter 2** describes the basics of opamps, various opamp topologies and their crucial specifications.
- **Chapter 3** describes the folded-cascode amplifier together with its benefits and disadvantages. The chapter will present a small-signal and large-signal analysis for different folded-cascode architectures together with derivations of important performance parameters.
- **Chapter 4** describes different settling time reduction techniques that were examined and implemented in this thesis. This chapter describes different slew rate enhancement techniques and the recycling folded-cascode structure.
- **Chapter 5** presents the actual implementation of the analog test buffer application. It describes the test buffer setup, the application of enhancement circuits and simulation procedure.
- **Chapter 6** covers the simulation results from the implemented techniques described in Chapter 5, together with an discussion about the work done in this thesis.
- **Chapter 7** presents a conclusion and outlines the directions for future work.

Finally, the **Appendix A** provides the questions and answers from the opposition of this work.

2

Operational Amplifier

Operational amplifiers (opamps) are important building blocks. The opamp is used to realize functions ranging from high-speed amplifications or filtering to bandgap reference generation and can be designed in many different levels of complexity. As the transistor channel lengths and the supply voltage scale down with each generation of CMOS technology, the design of the operational amplifier becomes more challenging [1].

This chapter will give a description of the operational amplifier and review some of the important performance parameters, such as the DC gain, the slew rate (SR) concept, small-signal bandwidth, the importance of supply noise rejection etc. It will also enumerate different opamp architectures.

2.1 The Operational Amplifier

Most integrated opamps have differential inputs realized with a differential transistor pair. A simple implementation of a differential input, single-ended amplifier is shown in Fig. 2.1. This circuit is realized by an NMOS input differential pair and an active current-mirror using PMOS transistors. The differential input transistor pair could also be realized using PMOS transistors, with an active current-mirror using NMOS transistors, though the changes in the performance and trade-offs between the two approaches will not be discussed here.

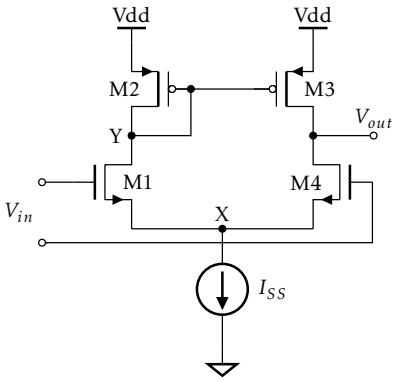


Fig. 2.1: *Simple four-device operational amplifier schematic.*

To describe different performance parameters of an opamp, both small-signal and large-signal analyses need to be considered. From a small-signal analysis of the opamp seen in Fig. 2.1, the gain can be expressed as $|A_V| = G_m R_{out}$, where G_m is the transconductance of the amplifier and R_{out} is the resistance seen at the output of the amplifier, which can be calculated separately. In order to calculate G_m we assume that the node X is a virtual ground, and therefore the circuit is symmetric [1]. Given that that M1 and M4 are of the same size, i.e. $g_{m1} = g_{m4}$, the small signal currents yields to $I_{D1} = |I_{D2}| = |I_{D3}| = g_{m1} V_{in}/2$ and $I_{D4} = -g_{m4} V_{in}/2$, hence $I_{out} = -g_{m1} V_{in}$ and therefore $|G_m| = g_{m1}$. While the calculation of R_{out} is less straightforward, it can be shown that the resistance seen at the output is equal to $(r_{ds2} \| r_{ds4})$ [2]. This result assumes that the output impedance is purely resistive. If there is a capacitive load, C_L, at the output the output impedance is equal to $R_{out} \| (1/sC_L)$, then the transfer function is given by

$$|A_V| = \frac{V_{out}}{V_{in}} = g_{m1} Z_{out} = \frac{g_{m1}}{g_{ds2} + g_{ds4} + sC_L}. \tag{2.1}$$

The above calculations have assumed an ideal tail current source, I_{SS}. In reality, the gain will be affected by the output impedance of the current source, but the error is relativity small [1]. Equation (2.1) can be rearranged as

$$|A_V| = \frac{\dfrac{g_{m1}}{g_{ds2} + g_{ds4}}}{1 + \dfrac{s}{\dfrac{g_{ds2} + g_{ds4}}{C_L}}} = \frac{A_0}{1 + \dfrac{s}{p_1}}, \tag{2.2}$$

where the A_0 represents the DC gain and P_1 the dominant pole. The unity-gain frequency can be approximated to

$$\omega_u \approx A_0 P_1 \approx \frac{g_{m1}}{C_L}. \tag{2.3}$$

As seen from (2.3) the unity-gain frequency is determined by the load capacitance, C_L. In order to achieve higher gain, the output resistance can be increased by cascoded load transistors, but at a cost of output swing and additional poles [1]. These configurations are also called "telescopic" cascode opamps, which will be discussed in Section 2.3.

If the same circuit is examined from a large-signal perspective, the slewing at the output from a large input step can be defined. If V_{in} experiences a large voltage change, ΔV, the current going through transistor M1 is increased by $g_{m1}\Delta V/2$, and the current through M4 is decreased by the same amount. The increased current flowing though M1 is mirrored to the output node, V_{out}, by the mirroring action of M2 and M3, hence the current charging the capacitive load, C_L, is equal to $g_{m1}\Delta V/2$. If the voltage change at the input is so large that transistor M1 absorbs all the current provided by I_{SS}, transistor M2 turns off. This generates a ramp at the output with a slope equal to I_{SS}/C_L, defining the slew rate of the circuit [1].

2.2 Performance Parameters

Decades ago the opamp was designed to serve as a general-purpose building block. The effort was to design an ideal opamp with high input impedance, low output impedance, and very high gain, but at a cost of other performance parameters, such as power dissipation, output voltage swing, input offset, noise suppression and speed. Today's designs proceed with the consideration of the trade-offs between several parameters, which in turn requires a multi-dimensional compromise in the implementation. For example, if the gain error is important while the speed is not, an amplifier topology is chosen that improves the gain error while possibly sacrificing the speed performance [1]. This section will describe some of the opamp parameters to provide the reader of an understanding why each of them may become important.

2.2.1 Gain

Usually, the opamp has a high gain that typically ranges from 10^1 to 10^5. The open-loop gain of the amplifier determines the precision of opamp-based feedback systems. Since the amplifier is often implemented in a feedback configuration, their open-loop gain is chosen according to the precision required for the closed-loop circuit. Considering parameters such output voltage swings and speed, the minimum required gain must be known. A high open-loop gain can also be required to suppress non-linearity in the amplifier [1].

2.2.2 Input Range and Output Swing

The output swing indicates the range of output voltages for which the opamp maintain linear transfer characteristics. Most of the differential amplifiers can not output a voltage spanning the, sometimes called rail-to-rail output. Most system today employing opamps require a large output swing to be able to support a wide range of signal amplitudes. While the differential input range is usually much smaller than the output swing, the input common-mode signal level may have the need for wide ranges in some applications. For example, when an amplifier is applied in a unity-gain buffer application, the output swing is nearly equal to the input swing. If we consider a simple unity-gain buffer shown in Fig. 2.2, the voltage swings are limited by the input transistor pair rather than the cascoded transistors at the output, by approximately one threshold voltage higher than allowed by the output transistors M7-M10 [1].

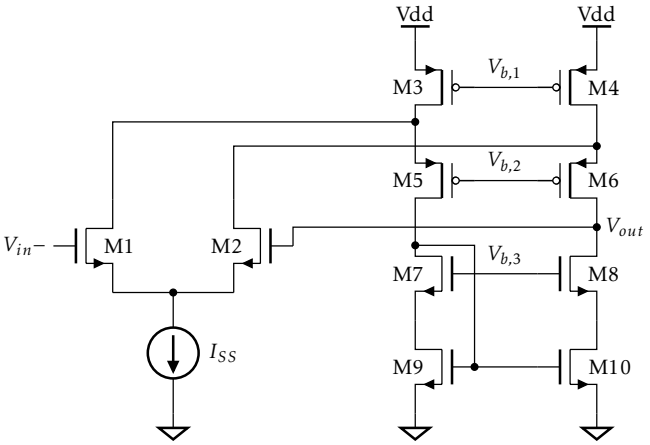


Fig. 2.2: *Unity-gain single-stage buffer amplifier schematic.*

One approach to extending the input common-mode range is to include both NMOS and PMOS input differential transistor pairs. In these applications one pair remains active when the other pair is off, and vice versa. The maximum voltage swing trades with bias currents, device sizes, and speed, and therefore has been a principal challenge in today's designs [1].

2.2.3 Small-Signal Bandwidth

As the frequency of operation increases in many applications, the high-frequency behavior plays an important role for operational amplifiers. The small-signal bandwidth is defined usually by the unity-gain frequency, f_u, which is the frequency where the open-loop gain is equal to 0 dB. As shown in Fig. 2.3, the open-loop gain starts to drop at higher frequencies, creating larger errors in the feedback system. The unity-gain frequency can be determined by a small-signal analysis, explained in Chapter 2.1.

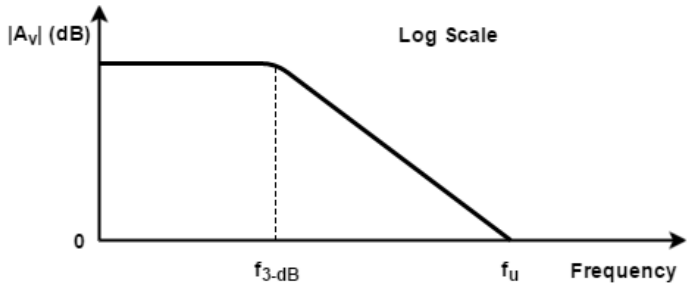


Fig. 2.3: *Bode plot of gain roll-off with frequency.*

The frequency when the open-loop gain drops by 3 dB, called the 3-dB frequency, f_{3-dB}, may also be measured to allow an easier prediction of the closed-loop frequency response [1].

2.2.4 Input Offset and Noise

In order to determine the minimum signal level that can be processed with good quality, the input offset and noise must be considered in an opamp design. Variations in the manufacturing of CMOS circuits cause mismatches of devices, which leads to input offset in the opamp. As a result, the ability to suppress input common-mode variations seen at the output decreases. Input common-mode variations disturb bias points, altering the small-signal gain and possibly limiting the output voltage swings [1].

Besides the input offset in an opamp, the analog signals processed in the opamp are also corrupted by two different types of noise, environmental noise and device electronic noise. Environmental noise refers to the random disturbances that the amplifier experiences through ground lines, supply lines or the substrate of the circuit [1]. The device electric noise can be divided into two different types of noise, thermal noise, and flicker noise respectively. The most significant thermal noise source is the noise generated in the channel of the MOSFET. Flicker noise, also called the $1/f$-noise, refers to the noisy phenomenon from the interface between the silicon substrate and the gate oxide in a MOSFET. Unlike the thermal noise, the average power of the flicker noise is more difficult to predict [1].

In many differential amplifier topologies, several devices contribute to offset and noise. For example, the circuit shown in Fig. 2.1 suffers from input referred noise contributions of all transistors, M1-M4 [1].

2.2.5 Power Supply Rejection

Opamps are often connected to noisy supply lines in mixed-signal systems, mentioned as "environmental" noise in Section 2.2.4. Thus, it is important for the amplifier to be able to suppress supply noise, especially when the noise frequency increases. For this reason, it is important to understand how the noise appears at the output of the opamp. The ability to suppress noise from the power supply, Power Supply Rejection Ratio (PSRR), is defined as the gain from the input to the output divided by the gain from the supply to the output. If we again consider the opamp in Fig. 2.1 and assuming that the supply voltage varies. The diode-connected device, M2, clamps node X to the supply, hence the voltage level at node X and V_{out} will experience approximately the same voltage variations as the supply voltage, assuming that the circuit is perfectly symmetric, i.e. $V_X = V_{out}$. This means that the gain from the supply to the output is close to unity, hence the PSRR of the opamp is equal to A_0 given in (2.2) [1].

2.2.6 Settling Time

Settling time is defined as the time required for the opamp output node to settle within a specified error voltage band in response to a voltage step applied at the opamp input. Settling time can be divided into three different periods, a very short period of propagation delay, a large-signal dependent slewing (nonlinear) period and a small-signal dependent linear period [3]. The settling time definition can be seen in Fig. 2.4, where (1) indicates the slewing period, (2) the linear settling time and (3) the total settling time. The propagation delay is usually very short compared to the other periods, hence propagation delay is neglected in this thesis.

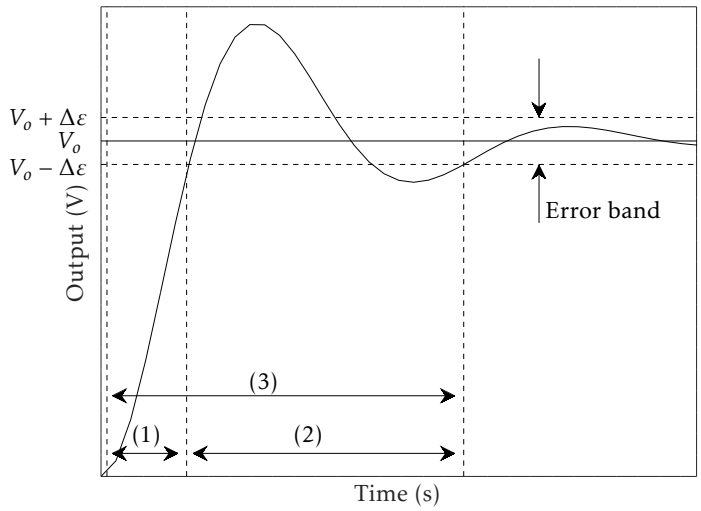


Fig. 2.4: *Graph of settling time periods (nonlinear scale).*

The settling time is most of the time very difficult to predict, since it is determined by a combination of amplifier characteristics, both linear as well as nonlinear. It is also a closed-loop parameter, hence it cannot be approximately calculated from open-loop parameters such as small-signal bandwidth, slew rate etc. [3, 4].

The linear settling time is due to the finite unity-gain frequency of the opamp. Thus it will set a finite minimum value for the overall settling time independent of the opamp output step size. In contrast, the nonlinear settling time behavior, the slew rate, strongly depends on the step size applied to the opamp. If the step size of the output signal level is really small, the opamp will never reach the slewing condition at all, hence the nonlinear settling time is zero.

Linear Settling For example, if we consider a single-pole opamp in a buffer configuration which has a phase margin of 90°, the settling time behavior can be analyzed quite easily. For the closed-loop amplifier, the step response can be derived from the transient response of any first-order circuits, and is given by

$$V_{out}(t) = V_{in,step}(t)(1 - e^{-t/\tau}), \tag{2.4}$$

where τ is the time constant of the closed-loop amplifier and is given by

$$\tau = \frac{1}{\omega_{-3dB}} = \frac{1}{\beta\omega_u}. \tag{2.5}$$

In a unity-gain buffer configuration, β is equal to one, hence τ is equal to $1/\omega_u$. With the exponential relationship shown in (2.4), the time required for a single-pole amplifier to settle within a specified error band can be found. For example, if the error band is specified to 1 % accuracy, then $e^{-t/\tau}$ is allowed to reach the value 0.01, which is achieved at a time of 4.6τ. If the error band is specified to 0.1% accuracy, the settling time needed becomes approximately 7τ etc. From these calculations, the needed unity-gain frequency for a specified settling time needed can be estimated [1, 2].

Nonlinear Settling (Slewing) When a large input step is applied to the opamp and the output displays a linear ramp having a constant slope, we say that the opamp experiences "slewing". The slope of the output signal is called slew rate. As described in Section 2.1, the slew rate indicates how fast the amplifier can change its output voltage in the slewing period and is given by

$$SR = \frac{I_{SS}}{C_L}, \tag{2.6}$$

where I_{SS} is the total available tail current in the opamp, and C_L is the capacitive load. The slewing time is indicated as (1) in Fig. 2.4

Slewing is an undesirable effect in high-speed circuits that processes large signals. While the small-signal bandwidth of an opamp may suggest a fast time-domain response, the large-signal speed may be limited by the inability to charge and discharge the dominant capacitor in the amplifier. As discussed in Section 2.1, the slew rate depends on how fast you can charge the capacitive load at the output, C_L. Since the relationship between the input and output during slewing is nonlinear, the output signal of a slewing amplifier is exposed to substantial distortion [1].

2.3 Topologies

The opamp can be realized by many different architectures/topologies. Either the opamp consists of a single-stage amplifier or a multi-stage amplifier. This chapter will give a brief introduction to the two different approaches.

2.3.1 Single-Stage Amplifier

The single-stage amplifier in a cascode configuration is a commonly used architecture in integrated circuit (IC) design. These configurations consist of a common-source connected transistor that feeds into a common-gate-connected transistor. Two examples of the cascoding technique can be seen in Fig. 2.5. Fig. 2.5 (a) has both an NMOS common source transistor and an NMOS common gate cascode transistor. This configuration is commonly called a telescopic-cascode amplifier. Fig. 2.5 (b) has an NMOS drive transistor, but a PMOS transistor for the cascode transistor, hence "folding" the small-signal current and is therefore commonly called a folded-cascode amplifier [2].

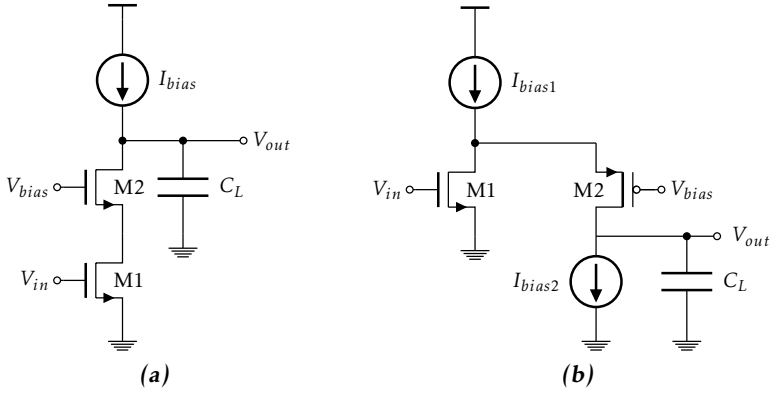


Fig. 2.5: *Schematic of cascode gain stages.*

There are two major benefits using cascode stages. The first is that they limit the voltage across the input transistor, thus minimizing short-channel effects, which is important in modern IC design. The second is that the cascode stage has a large output impedance, which results in a quite large gain, when the current sources are realized with high-quality current mirrors [2].

The major drawback with telescopic-cascode amplifiers is the restricted input range and output swing and their difficulty to short their inputs and outputs together, e.g. when implementing the amplifier as a unity-gain buffer. To understand this difficulty, we consider a telescopic-cascode amplifier in a unity-gain feedback topology shown in Fig. 2.6. To determine the voltage range of this amplifier we need to determine the conditions where M7 and M8 operate in saturation region, therefore $V_{out} \leq V_X + V_{TH8}$ and $V_{out} \geq V_{bias} - V_{TH6}$. Since $V_X = V_{bias} - V_{GS6}$, hence $V_{bias} - V_{TH6} \leq V_{out} \leq V_{bias} - V_{GS6} + V_{TH8}$. The voltage range, $V_{max} - V_{min}$, is then equal to $V_{TH6} - (V_{GS6} - V_{TH8})$, which is maximized by minimizing the overdrive voltage of M6, but always less than V_{TH8}. Thus it is not possible to use a telescopic-cascode opamp in a unity-gain feedback configuration [1].

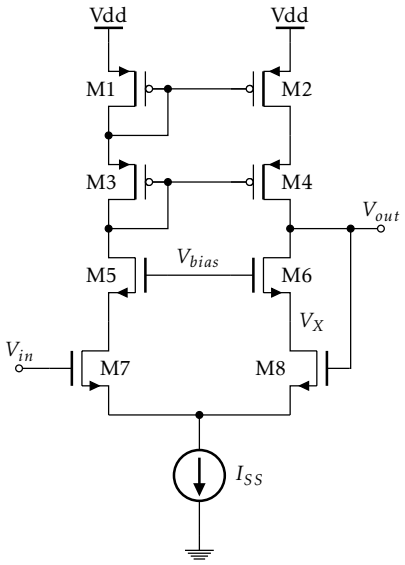


Fig. 2.6: *Schematic of a telescopic-cascode opamp with input and output shorted.*

2.3.2 Multi-Stage Amplifier

The single-stage amplifier discussed in 2.3.1 suffers from a "one-stage" nature by only allowing a small-signal current produced by the input transistor pair to flow directly through the output impedance, thus limiting the gain to the product of the input pair transconductance and the output impedance. Single-stage amplifiers also limits the output swing when cascoding such circuits in order to achieve a higher gain [1]. In some applications, the output swing and/or gain provided by cascoded opamps are not adequate. In such applications a two-stage amplifier can be used, where the first stage provides a high gain and the second provides a large swing, realized in Fig. 2.7.

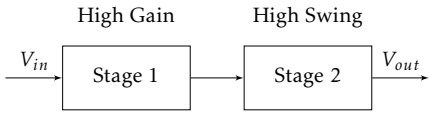


Fig. 2.7: *A simple illustration of a two-stage opamp.*

Each stage can be realized by various amplifier topologies. The second stage is typically configured to provide maximum output swing. The disadvantage in using a multi-stage amplifier is that each gain stage introduces at least one pole in the open-loop transfer function, hence making it more difficult to guarantee stability in a feedback configuration [1]. There are several frequency compensation techniques in order to achieve stability in a multi-stage amplifiers. This thesis will focus on the single-stage amplifier, hence the design and compensation techniques of multi-stage amplifier will not be covered here. A general model of the design procedure for a multi-stage amplifier can be found in [5] and [6]. Some modern compensation architectures are shown in [7], [8] and [9], together with settling time and noise optimization in [10].

3

The Folded-Cascode Amplifier

This chapter will describe the folded-cascode operational amplifier, analyze its equivalent small-signal model and derive expressions for the key parameters such as gain, unity-gain frequency, dominant pole and non-dominant poles. Different structures of FC including single-ended, complementary input and fully differential architectures will be covered.

3.1 Single-Ended Folded-Cascode Amplifier

The folded-cascode cell described in Chapter 2 can easily be applied to a single-stage opamp to provide a single-ended output, where an NMOS cascode current mirror converts the differential currents of the output branches to a single output, as shown in Fig. 3.1 [1].

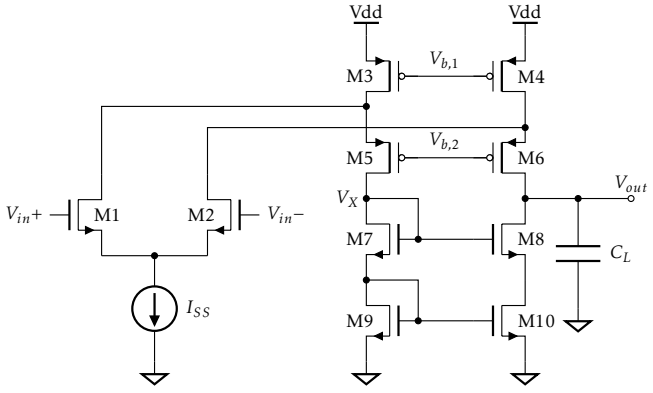


Fig. 3.1: *Schematic of a single-ended folded-cascode amplifier.*

The cascode current mirror application in Fig. 3.1 suffers from two disadvantages. First the structure is limiting the output swing, where node $V_X = V_{GS9} + V_{GS7}$, limiting the minimum value of V_{out} to $V_{GS9} + V_{GS7} - V_{TH8}$. Second, the node at V_X introduces a pole. In order to solve the former issue, the circuit can be modified as shown in Fig. 3.2, thus increasing the output swing with one NMOS threshold voltage [1, 11].

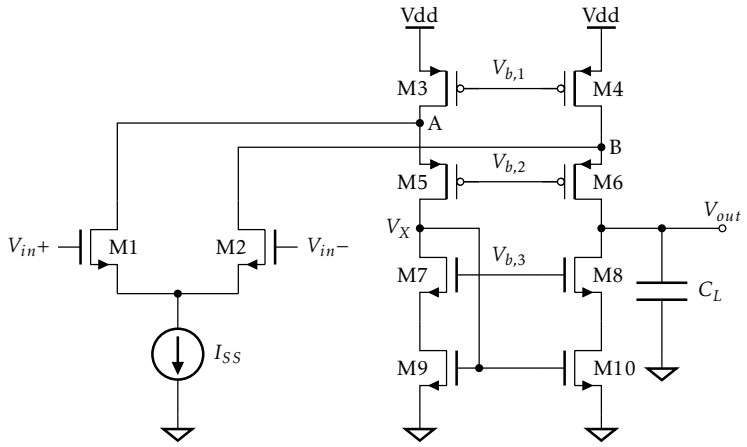
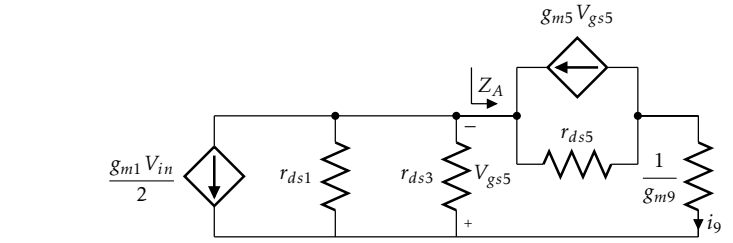
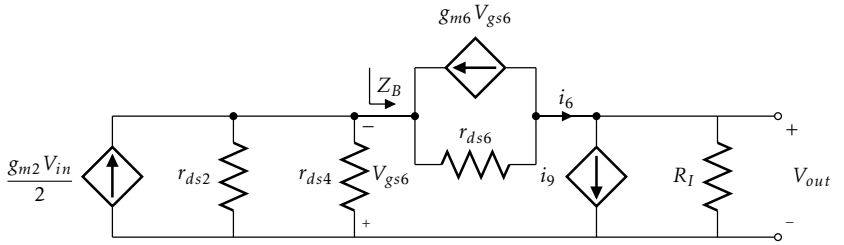


Fig. 3.2: *Modified single-ended folded-cascode amplifier schematic.*

In order to analyze the circuit, the small-signal model of the single-ended structure in Fig. 3.2, is shown in Fig. 3.3. The small-signal schematic is divided into two different models where Fig. 3.3 (a) shows the contribution of the "left branch", consisting of devices M1, M3, M5, M7 and M9, and Fig. 3.3 (b) shows the contribution of the "right branch", consisting of devices M2, M4, M6, M8 and M10 [11].



***(a)** Left Branch*



***(b)** Right Branch*

***Fig. 3.3:** Small-signal model of single-ended folded-cascode structure.*

The resistances looking into the source of the cascoded transistors M7 and M8, denoted as Z_A and Z_B in Fig. 3.3, can be derived as

$$Z_A = \frac{r_{ds5} + (1/g_{m9})}{1 + g_{m5} r_{ds5}} \approx \frac{1}{g_{m5}}, \tag{3.1}$$

$$Z_B = \frac{r_{ds6} + R_I}{1 + g_{m6} r_{ds6}} \approx \frac{R_I}{g_{m6} r_{ds6}}, \tag{3.2}$$

where $R_I = g_{m8}\, r_{ds8}\, r_{ds10}$ and by assuming $g_m\, r_o >> 1$. The voltage transfer function can be found as follows. The current i_9 in Fig. 3.3(a) can be written as

$$\begin{aligned} i_9 &= \frac{g_{m1} V_{in}}{2} \left(\frac{r_{ds1} \| r_{ds3}}{Z_A + (r_{ds1} \| r_{ds3})} \right) \\ &= \frac{g_{m1} V_{in}}{2} \left(\frac{g_{m5} (r_{ds1} \| r_{ds3})}{1 + g_{m5} (r_{ds1} \| r_{ds3})} \right) \\ &\approx \frac{g_{m1} V_{in}}{2}. \end{aligned} \tag{3.3}$$

The current i_6 in Fig. 3.3(b) can be derived similar to i_9 and can be expressed as

$$
\begin{aligned}
i_6 &= \frac{g_{m2}V_{in}}{2}\left(\frac{r_{ds2}\|r_{ds4}}{\dfrac{R_I}{g_{m6}r_{ds6}}+(r_{ds2}\|r_{ds4})}\right)\\
&= \frac{g_{m2}V_{in}}{2}\left(\frac{1}{\dfrac{R_I}{(g_{m6}r_{ds6})(r_{ds2}\|r_{ds4})}+1}\right)\\
&\approx \frac{g_{m2}V_{in}}{2}\left(\frac{1}{\dfrac{R_I(g_{ds2}g_{ds4})}{g_{m6}r_{ds6}}+1}\right)\\
&= \frac{g_{m2}V_{in}}{2(K+1)},
\end{aligned}
\tag{3.4}
$$

where a low-frequency unbalance factor K is defined as

$$K = \frac{R_I(g_{ds2}g_{ds4})}{g_{m6}r_{ds6}}, \tag{3.5}$$

and has a typical value greater than one [11]. The output voltage V_{out} is equal to the sum of i_9 and i_6 flowing through R_{out}, and is given by

$$V_{out} = (i_9 + i_6)R_{out} = V_{in}\left(\frac{g_{m1}}{2}+\frac{g_{m2}}{2(K+1)}\right)R_{out}. \tag{3.6}$$

Assuming that the input pair transistors are of the same size, i.e. $g_{m1} \approx g_{m2}$, we can express the final voltage transfer function as

$$\frac{V_{out}}{V_{in}} = \left(\frac{2+K}{2(K+1)}\right)g_{m1}R_{out}, \tag{3.7}$$

where the output resistance is given by

$$R_{out} = (g_{m8}r_{ds8}r_{ds10})\|\|(g_{m6}r_{ds6}(r_{ds2}\|r_{ds4}). \tag{3.8}$$

The frequency response of the single-ended folded-cascode is determined primarily by the output pole, which is given by

$$p_o = \frac{-1}{R_{out}C_L}, \tag{3.9}$$

where the C_L is the load capacitance of the amplifier. To ensure that the output pole is dominant, the magnitude of the parasitic and mirrored poles must be much larger than the unity-gain frequency which is equal to the product of (3.9) and (3.7) [11].

The non-dominant poles are located at node A and B in Fig. 3.2, at the drains of M5 and the sources of M7 and M8 [11]. The approximate expression for each pole is

$$p_A = \frac{-1}{Z_A C_A} = \frac{-g_{m5}}{C_{gs5} + 2C_{db}}, \tag{3.10}$$

$$p_B = \frac{-1}{Z_B C_B} = \frac{-g_{m6}}{C_{gs} + 2C_{db}}, \tag{3.11}$$

$$p_{M5,D} = \frac{-g_{m9}}{2C_{gs} + 2C_{db}}, \tag{3.12}$$

$$p_{M7,S} = \frac{-(g_{m7} r_{ds7} g_{m9})}{C_{gs} + C_{db}}, \tag{3.13}$$

$$p_{M8,S} = \frac{-g_{m8}}{C_{gs} + C_{db}}, \tag{3.14}$$

where C_{gs} and C_{db} is the parasitic capacitances between gate and source terminals and drain and bulk terminals of a device respectively. By doing a large-signal analysis as in Chapter 2.1, it can be shown that the slew rate yields to I_{SS}/C_L [1].

3.2 Complementary Input Single-Ended Folded-Cascode Amplifier

The folded-cascode amplifier structure discussed in 3.1 evolved to achieve large differential output swing. But when considering the differential input swings, this structure has a lower limit. If we consider the folded-cascode amplifier in a unity-gain buffer application shown in Fig. 3.4, where the input swing is approximately equal to the output swing, the voltage swing is limited by $V_{in,min} \approx V_{out,min} = V_{GS2} + V_{I_{SS}}$, nearly one threshold voltage higher than allowable provided by M_7-M_{10} [1].

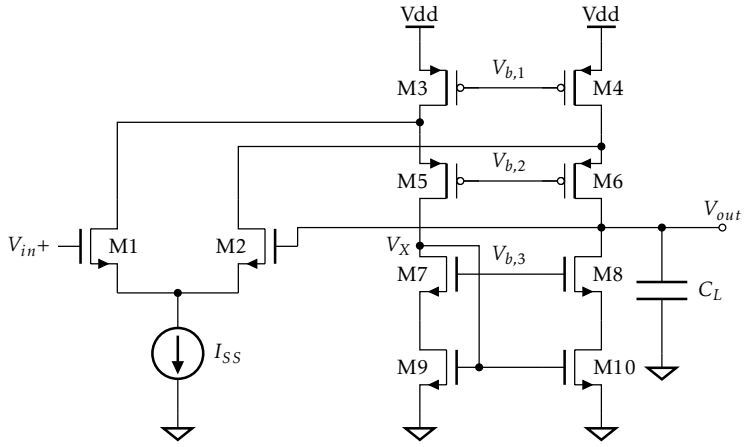


Fig. 3.4: *Schematic of a single-ended amplifier in unity-gain buffer configuration.*

If the input voltage falls below this minimum voltage the transistor in the current source, I_{SS}, enters triode region, which in this case is decreasing the bias current of the differential input pair and hence lowering the transconductance of the amplifier. A better approach to extend the input voltage swing of the amplifier is to integrate both an NMOS transistor pair together with a PMOS transistor pair. This approach is illustrated in Fig. 3.5, where one input transistor pair is active while the other one is turned off, and vice versa. As the input common mode range approaches V_{DD}, in this case, the PMOS transistor pair's transconductance drops and eventually reaches zero. On the other hand, the NMOS transistor pair remains active, which allows normal operation. When the common mode range approaches ground potential, the M1 and M2 begin to turn off but M1p and M2p are properly functional. Thus, while using this architecture the performance parameters such as speed, gain and noise may vary [1].

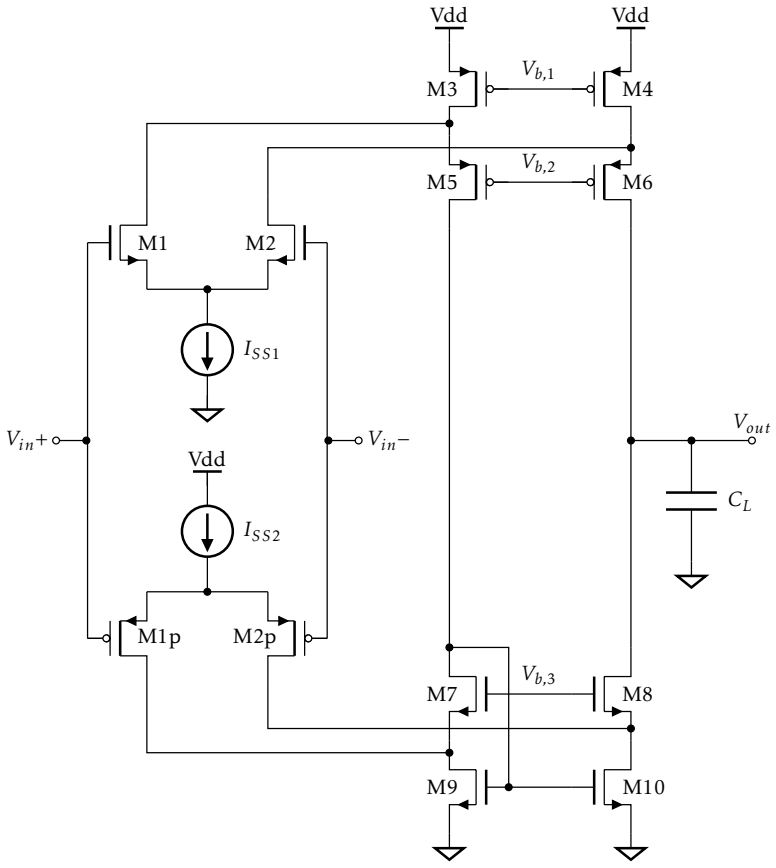


Fig. 3.5: *Schematic of the complementary input pairs for extended input range.*

The small-signal analysis for the complementary input structure follows the same procedure as in Section 3.1. However, a more difficult and extensive algebra is needed in order to derive the small-signal parameters. Thus as shown in [12], the parameters are approximately the same as in the single-ended folded-cascode structure, if one assumes that the dominant pole is located at the output node, the output impedance can be expressed as

$$R_{out} = (g_{m8} r_{ds8} (r_{ds10} \| r_{ds2p})) \| (g_{m6} r_{ds6} (r_{ds4} \| r_{ds2})), \tag{3.15}$$

and unity-gain frequency as

$$\omega_{ug} = \frac{g_{m,M1/M2} + g_{m,M1p/M2p}}{C_L}. \tag{3.16}$$

This structure has been considered in other research work and can be studied in detail in [13], [12] and [14].

3.3 Fully Differential Folded-Cascode Amplifier

The folded-cascode amplifier can be used in differential input differential output configuration. A realization of the differential folded-cascode architecture is shown in Fig. 3.6.

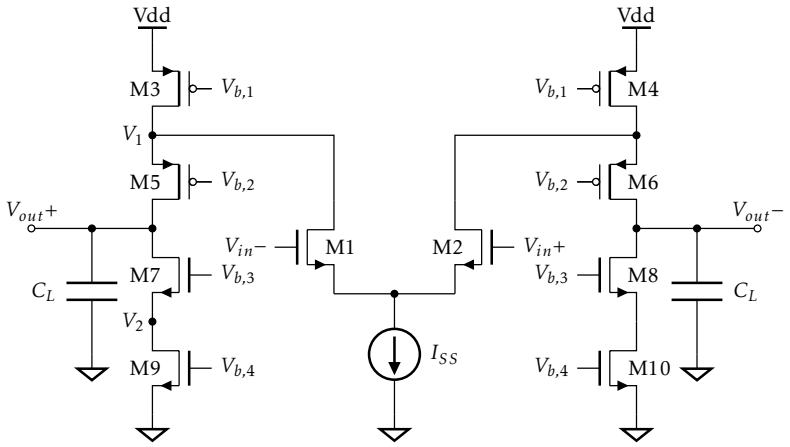


Fig. 3.6: *Schematic of a differential folded-cascode amplifier.*

The architecture may also be implemented with PMOS input transistors and NMOS cascoded transistors. As seen in Fig. 3.6, the differential folded-cascode is a fully-symmetric structure and thus the half-circuit concept can be applied when doing the small-signal analysis [1]. This concept is a powerful analyzing technique for differential pairs with fully differential inputs. In order to do a small-signal analysis of the differential folded-cascode amplifier, the half-circuit concept is applied and the small-signal model of the circuit can be seen in Fig. 3.7.

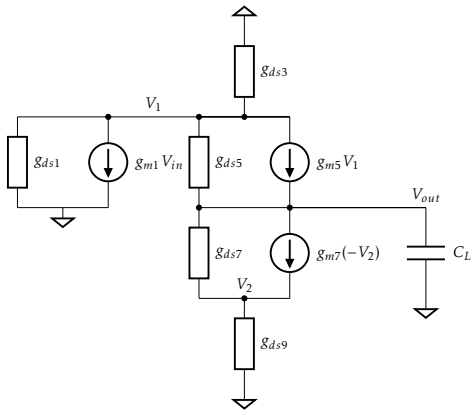


Fig. 3.7: *Small-signal model of Fig. 3.6.*

By ignoring high-frequency poles and zeros and use the lemma that the voltage gain in a linear circuit is equal to $-G_m R_{out}$, we can determine the small-signal transfer function of the folded-cascode amplifier [1, 2]. The R_{out} in the previous statement represents the output resistance of the circuit when the input is zero and G_m denotes the transconductance when the output is shorted. Then we can write the transfer function as

$$A_V = \frac{V_{out}}{V_{in}} = G_m R_{out} = \frac{G_m}{G_{out}}. \tag{3.17}$$

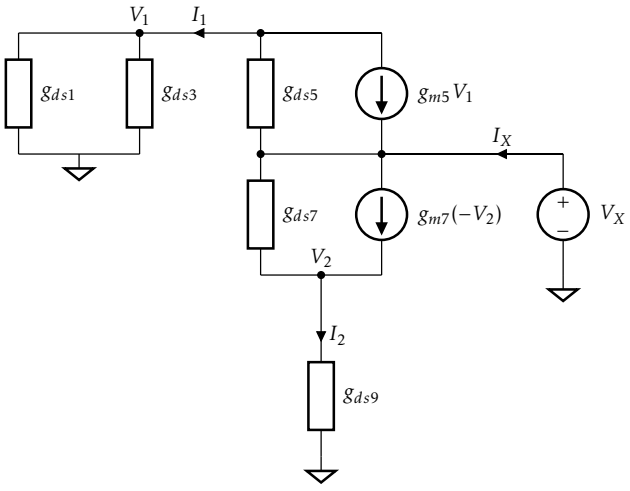


Fig. 3.8: *Small-signal model for R_{out} expression.*

As seen in (3.17), we need to determine R_{out} and G_m. In order to calculate R_{out} the input voltage is set to zero and an external voltage supply, V_X, is applied at the output. The output resistance is then equal to $R_{out} = V_x / I_X$, and thus $G_{out} = I_X / V_X$. The small-signal model is redrawn according to Fig. 3.8 where the voltages V_1 and V_2 is given by

$$V_1 = \frac{I_1}{g_{ds1} + g_{ds3}}, \tag{3.18}$$

$$V_2 = \frac{I_2}{g_{ds9}}, \tag{3.19}$$

where

$$I_X = I_1 + I_2. \tag{3.20}$$

A node analysis at V_X gives

$$I_1 = -g_{m5} V_1 + (V_x - V_1) g_{ds5}, \tag{3.21}$$

$$I_2 = -g_{m7}\, V_2 + (V_x - V_2)\, g_{ds7}. \tag{3.22}$$

Substituting V_1 and V_2 from (3.18) and (3.19) to (3.21) and (3.22) gives

$$I_1 = -I_1 \frac{g_{m5}}{g_{ds1} + g_{ds3}} + V_X\, g_{ds5} - I_1 \frac{g_{ds5}}{g_{ds1} + g_{ds3}}, \tag{3.23}$$

$$I_2 = -I_2 \frac{g_{m7}}{g_{ds9}} + V_X\, g_{ds7} - I_2 \frac{g_{ds7}}{g_{ds9}}. \tag{3.24}$$

By rearranging (3.23) and (3.24) we get

$$I_1 = V_X \frac{g_{ds5}\,(g_{ds1} + g_{ds3})}{(g_{ds1} + g_{ds3}) + g_{m5} + g_{ds5}}, \tag{3.25}$$

$$I_2 = V_X \frac{g_{ds9}\, g_{ds7}}{g_{ds9} + g_{m7} + g_{ds7}}. \tag{3.26}$$

Substituting I_1 and I_2 from (3.25) and (3.26) to (3.20) gives

$$I_X = V_X \left(\frac{g_{ds5}\,(g_{ds1} + g_{ds3})}{(g_{ds1} + g_{ds3}) + g_{m5} + g_{ds5}} + \frac{g_{ds9}\, g_{ds7}}{g_{ds9} + g_{m7} + g_{ds7}}\right). \tag{3.27}$$

Assuming that $g_m >> g_{ds}$ in (3.27), gives the following expression

$$\frac{I_X}{V_X} = \frac{g_{ds5}\,(g_{ds1} + g_{ds3})}{g_{m5}} + \frac{g_{ds9}\, g_{ds7}}{g_{m7}} = G_{out}. \tag{3.28}$$

In the same manner we calculate G_m by shorting the output to ground. The small-signal model is now redrawn according to Fig. 3.9.

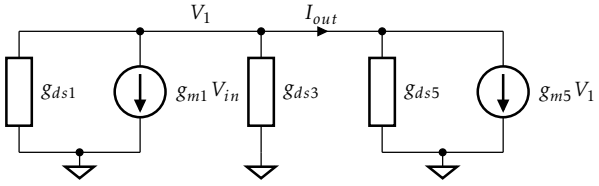


Fig. 3.9: *Small-signal model for G_m expression.*

A node analysis at V_1 gives the following expression

$$g_{m1}\, V_{in} + V_1\,(g_{ds1} + g_{ds3}) + I_{out} = 0. \tag{3.29}$$

According to Fig. 3.9 we get

$$V_1 = \frac{I_{out}}{(g_{ds5} + g_{m5})}. \tag{3.30}$$

Defining $G_m = I_{out} / V_{in}$ and substituting V_1 from (3.30) to (3.29) gives

$$G_m = \frac{I_{out}}{V_{in}} = -g_{m1}\,\frac{g_{ds5} + g_{m5}}{g_{ds1} + g_{ds3} + g_{ds5} + g_{m5}}. \tag{3.31}$$

Assuming $g_m >> g_{ds}$. The expression for G_m is given by

$$G_m = -g_{m1}. \tag{3.32}$$

The expression for the voltage gain according to (3.17), is then equal to

$$A_V = \frac{-\,g_{m1}}{g_{out}} = \frac{-\,g_{m1}}{\dfrac{g_{ds5}\,(g_{ds1} + g_{ds3})}{g_{m5}} + \dfrac{g_{ds9}\,g_{ds7}}{g_{m7}}}. \tag{3.33}$$

The dominant pole is given by

$$p_1 = \frac{g_{out}}{C_L}, \tag{3.34}$$

and unity-gain frequency can approximately be expressed as

$$\omega_u \approx A_0\,p_1 \approx \frac{g_{m1}}{C_L}, \tag{3.35}$$

where C_L is the load capacitance of the amplifier seen in Fig. 3.6.

All the performance parameters expressions derived in this chapter can be used as handles when designing a folded-cascode amplifier or optimizing the amplifier for specific performance parameters. We see that that the performance parameters for all folded-cascode structures covered in this chapter depends on the same factors, i.e. the gain is defined by the transconductance of the input transistors and the resistance seen at the output, the unity-gain frequency is defined by the transconductance of the input transistors and the capacitive load and the dominant pole is defined by the output resistance and the capacitive load.

4

Settling Time Reduction Techniques

For high-speed applications, a fast settling opamp is a common and critical requirement [15]. As described in Chapter 2, the settling time is divided into two different periods, one which depends on the large-signal behavior, i.e. the slew rate of the amplifier, and another that depends on the small-signal behavior, i.e. the unity-gain frequency. To reduce the total settling time of an amplifier, the small-signal and/or the large-signal performance must be improved.

This chapter will describe three slew rate enhancement (SRE) techniques, proposed in [15], [16] and [17], which aim at improving the large-signal performance of an amplifier, without affecting the small-signal behavior. It will also describe the recycling folded-cascode structure proposed in [18], which aim at improving both the small-signal and large-signal behavior.

4.1 Slew Rate Enhancement Techniques

This section will cover the principle of operation of the proposed slew rate enhancement techniques. It will describe the three different slew rate techniques in detail together with some design considerations.

4.1.1 Principle of Operation

The slewing period, which is the result of limited available current of the input stage to charge or discharge the load capacitance forms a substantial portion of the total settling time. Hence, to improve the slew rate of an amplifier, the total available current charging the load capacitance needs to be increased. As calculated in Chapter 2.1, the slew rate is defined by the total available bias current of the amplifier, hence increasing the provided bias currents will give a better slew

rate performance. However, this approach leads to wasteful power dissipation [17].

A more efficient approach is to implement a structure that detects the large-signal transients during operation and injects/sinks current to/from the output node during that period. A block diagram illustrating the functionality of such SRE circuits is shown in Fig. 4.1. The sensing circuit detects both low to high (Lo-Hi) and high to low (Hi-Lo) large-signal transients. The driving circuit provides the additional current required to rapidly charge/discharge the load capacitor. The SRE circuit needs to be implemented without changing the small-signal behavior, i.e. not affecting the linear settling time of the amplifier [19].

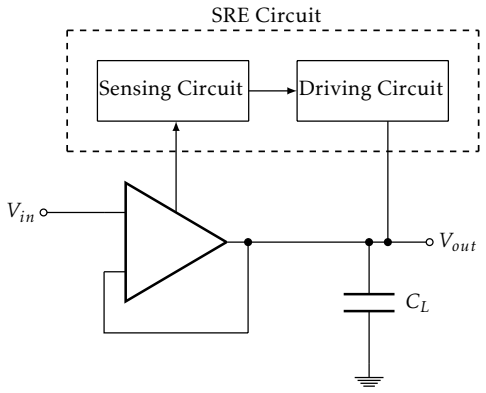


Fig. 4.1: *Block diagram of the SRE concept [18].*

Different SRE circuits have been developed based on different sensing and driving circuits, which ideally lower the slewing time together with an unchanged linear settling time, resulting in a reduced total settling time. There are two types of sensing circuits considered in this chapter, one that detects a large-signal transient at the input and one at an intermediate node of the core amplifier. Three different SRE techniques have been considered in this thesis, one technique using intermediate node sensing and two techniques using input-referred sensing. The proposed enhancement techniques will be described in Sections 4.1.2-4.1.4. Other proposed SRE techniques can be studied in [20], [21] and [22].

4.1.2 Slew Rate Enhancement Technique 1

The following technique is proposed in [15], where a slew rate enhancement circuit has been designed, tested and implemented. This technique will further in this document be referred to as SRE1. The SRE1 can be implemented in both a current-mirror and a folded-cascode amplifier. However, this chapter will only consider the folded-cascode application in view of the suitability for this thesis. The proposed SRE circuit for the folded-cascode application is shown in Fig. 4.2, where device Ma and Mb are the load devices of the core amplifier (same as M7 and M9 shown in Fig. 3.5) and devices M2-M8, Mp and Mn provide the slewing increased capability [15].

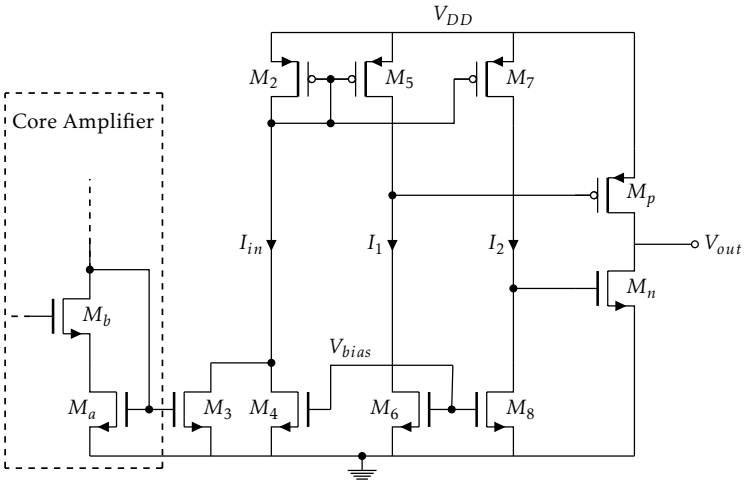


Fig. 4.2: *Schematic of the SRE1 circuit.*

A large signal step is detected by M3, which is connected to the gate of the load device of the amplifier, such that the sensing circuit can detect both positive and negative slewing. The input current of the SRE, I_{in}, depends on the current flow at the output stage of the core amplifier, i.e. if the voltage at the positive input of the amplifier increases, the current I_{in} increases. By detecting the change of this signal dependent current, devices Mp and Mn will be switched on and off according to the voltage provided to the respective gate terminal [15].

Transistors M5 and M6 control the switching of transistor Mp. During positive slewing, Mp will turn on and inject dynamic current to the output node, thus charging the load capacitance. The same idea is applied for negative slewing, where transistors M7 and M8 turn on Mn, and hence sinking current from the output node, i.e. discharging the load capacitance.

In order to achieve this functionality, the device sizes need to be properly designed. During static state, i.e. when no slewing occurs, the sizes of transistor M5 and M6 are designed such that if they operate in the saturation region. The drains

of the transistors are connected together, hence the current flowing through them is given by $I_1 = min(I_{in}, I_6)$. By precise device sizing the circuit needs to be designed such that $I_1 = I_6$ during the static state, hence M5 is forced to operate in the triode region. In this way the gate terminal of Mp is pulled close to the supply, i.e. Mp is turned off. This also applies to transistors M7 and M8, where the current flowing through them is given by $I_2 = min(I_{in}, I_8)$, where $I_2 = I_{in}$ during static state, i.e. turning off Mn as well. As both Mp and Mn are in the cut-off region when no slewing occurs, the SRE does not affect the small-signal performance of the core amplifier during normal operation[15].

During positive slewing, I_{in} increases and equals to I_6, which will force M5 to enter saturation region and force M6 to enter triode region. Then the voltage at the gate terminal of Mp is pulled to ground, which causes Mp to be heavily turned on. During this transition, I_2 will still be equal to I_{in}, so that Mn is kept in cut-off region. This will cause the SRE circuit to charge the load capacitance with additional current during positive slewing, hence increasing the slew rate of the amplifier. Similarly, M7 and M8 are forced into triode and saturation region respectively during negative slewing. This will cause Mn to be heavily turned on (and Mp turned off), sinking current from the load capacitance [15].

The operation regions of M5-M8, Mp, and Mn during different states are summarized in Table. 4.1.

Table 4.1: *SRE1 transistor operation regions [15].*

	Static State	**Positive Slewing**	**Negative Slewing**
M5	Triode	Saturation	Triode
M6	Saturation	Triode	Saturation
Mp	Off	Triode	Off
M7	Saturation	Saturation	Triode
M8	Triode	Triode	Saturation
Mn	Off	Off	Triode

As stated earlier, the SRE does not affect the small-signal behaviour of the core amplifier during normal operation. Hence the SRE and the core amplifier can be sized separately. The core amplifier can be sized in order to meet small-signal performance parameter specifications, and the SRE can be sized in order to conserve area and optimize speed [15].

4.1.3 Slew Rate Enhancement Technique 2

The second technique considered in this thesis is based on the research work from [16], which presents a novel slew rate enhancement circuit for CMOS amplifiers, further on this technique will be referred to as SRE2. Similarly to SRE1 discussed in Section 4.1.2, the slew rate is improved by an external circuit that detects large-signal transitions at the input of the amplifier and activates a driving circuit, to charge and discharge the output node. The schematic of the proposed enhancement circuit is shown in Fig. 4.3 and can be incorporated into practically any amplifier structure [16].

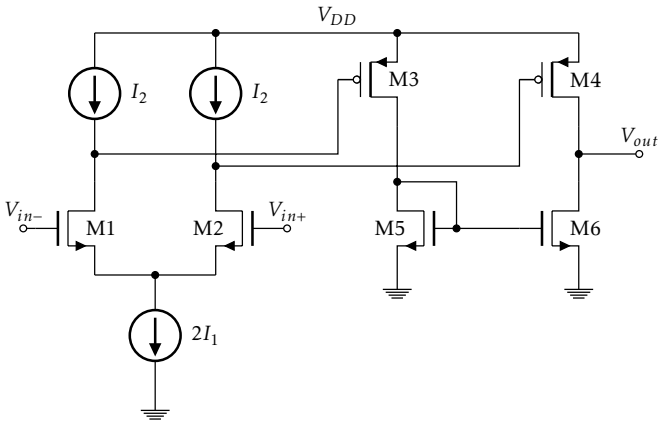


Fig. 4.3: *Schematic of the SRE2 circuit.*

To describe the principle of operation of the SRE we consider the schematic shown in Fig. 4.3, where the differential inputs, V_{in-}/V_{in+}, and the output, V_{out}, are connected to the input and output terminals of the core amplifier respectively. The differential transistor pair, M1-M2, is used to detect large signal transients. To simplify the explanation of the circuit, the load devices connected to the input pair is realized by two ideally current sources, carrying a current of I_2 each. The tail current attached to the differential pair are designed to carry a current equal to $2I_1$. In reality the currents, I_1 and I_2, are provided by carefully designed current-mirrors, where I_1 is designed to be slightly lower than I_2 [16].

Under normal conditions, i.e. when no slewing occurs, the potentials at the input terminals V_{in-} and V_{in+} are ideally the same, thus carrying a current of I_1 each. Since $I_1 < I_2$, the devices that provides the current I_2 are forced to operate in the triode region, pulling the voltage at the drains of M1 and M2 close to V_{DD}, ensuring that transistors M3 and M4 remains in the cut-off region when no slewing occurs[16].

When a large signal transient occurs (in a closed loop configuration), the large potential differences at the input terminal is sensed by the SRE. For example, whenever V_{in+} exhibits a much larger potential than V_{in-}, M2 quickly pulls its

drain terminal to ground, hence M4 is heavily turned on. In this condition, M4 provides a large current that charges the load capacitance of the amplifier. As the output voltage gets closer to its final value, the voltage difference at the input terminals goes to zero, hence the drain terminal of M2 returns to supply potential, turning off M4. In the same way, when the output has to slew in the negative direction, M3 quickly turns on, which provides a current that are mirrored by M5-M6 to the output, hence sinks current from the load capacitance of the amplifier [17].

By using this approach, the transistors in the SRE circuit are normally off during small-signal operations, hence the small-signal performance of the core amplifier will not be affected by implementing this technique. Hence the core amplifier can be sized separately in order to meet important performance parameters and at the same time, the device sizes in the SRE circuit can be optimized to improve speed and conserve area [17].

In order to make this technique useful, is is important that the condition $I_1 < I_2$ is satisfied. The ratio between the two currents determines the input voltage difference at which the SRE is activated. By defining this voltage as V_a, it can be shown from a large-signal analysis that V_a is approximately given by

$$V_a = \left(\frac{I_2}{I_1} - 1\right)\sqrt{\frac{I_1}{K}} \tag{4.1}$$

where K is the conductance parameter of the transistor M1 and M2 [17]. In order to prevent the SRE from being incorrectly activated during normal operation, V_a should be large enough to exceed the input offset of the input differential pairs, thus the exact ratio of I_1 and I_2 is not critical [16].

4.1.4 Slew Rate Enhancement Technique 3

If we decrease the load capacitance for a given amplifier design, the slew rate will increase proportionally. This will only continue if the rise and fall times of the circuit is larger than the response time of the SRE discussed in 4.1.3. Therefore a third SRE technique is considered in this thesis. This technique is a modified version of SRE2 and is based on the research work from [17]. For simplicity, this technique will be referred to as SRE3 further on in this document.

One major drawback of SRE2 is the response time for a high-to-low transition. This transition is slower than the low-to-high transition due to the extra time delay needed for mirroring the current from M3 to the output node, seen in Fig. 4.3 [17]. This response time can be improved by modifying the SRE2 circuit. The principle of operation is almost the same as in SRE2, however, in this structure, the detection for a positive and a negative slewing is done by two complementary differential pairs, instead of one. If we consider the circuit shown in Fig. 4.4, the extra delay involved in turning the slewing current up-side-down for the high-to-low transition is removed by introducing a PMOS input transistor pair [17].

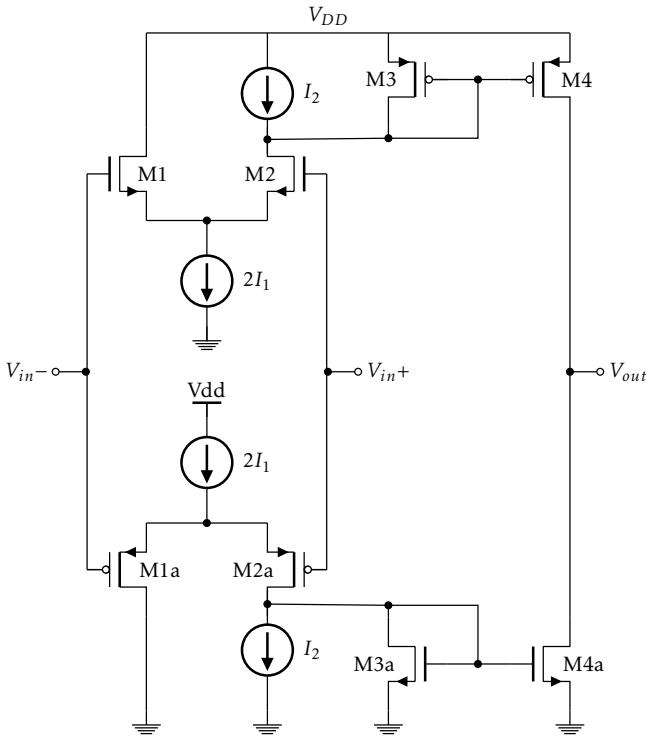


Fig. 4.4: *Schematic of the SRE3 circuit.*

This structure also includes two diode connected clamp transistors, M3 and M3a, which prevent eventual overshoots that can occur at the end of the large-signal transitions. These transistors will regulate the drive strength, making it more robust under some temperature and process variations. Since SRE3 improves the speed of the Hi-Lo transition by introducing one extra input transistor pair together with its biasing circuitry, static power consumption is increased. The compromise between speed and power consumption can be achieved by properly sizing the two transistor pairs M3-M4 and M3a-M4a. This SRE circuit will be useful in applications that need very high slew rates for relatively small capacitive loads [17].

4.2 Recycling Folded-Cascode Amplifier

While the technique presented in Section 4.1 focus on slew rate improvement without affecting the small-signal performance, this chapter will show a modified version of the conventional folded-cascode amplifier, in order achieve a general performance enhancement of the core amplifier. The modified version shown in this chapter is called the recycling folded-cascode (RFC), and was first proposed in [18] and further examined in [23]. The RFC architecture has also been used in other research works, [24], [25], [26], where it has has been proven that the RFC improves the DC gain, unity-gain bandwidth, and slew rate compared with conventional FC amplifiers with the same power consumption.

The basic idea of the RFC is to recycle (or reuse) previously idle devices in the signal path to perform additional tasks, hence improving the performance of the amplifier for the same amount of power consumption [23]. Compared to the SRE techniques, which only enhance the large-signal behaviour for the amplifier, this structure will also improve small-signal parameters that reduces the total settling time of the amplifier. The RFC technique proved to be very useful in order to achieve promising results in this thesis. This chapter will give a brief presentation of the recycling technique, and how the different performance parameters are improved.

4.2.1 Modifications of the Conventional Folded-Cascode

If we consider a conventional folded-cascode shown in Fig. 4.5, the transistors M3 and M4 provides a folding node for the small-signal current generated by the input transistor pair, as discussed in Chapter 3. They are also conducting the most current in the amplifier, which is really inefficient if considered that their only task is to provide a folding node. To address this inefficiency, a RFC amplifier can be implemented. The idea of the RFC amplifier is to rearrange and split transistors in order to convert M3 and M4 to driving transistors instead, hence recycling the current in the idle transistors [23].

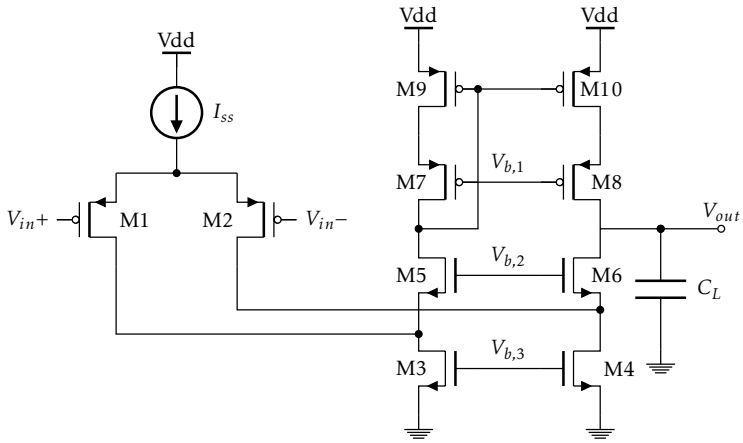


Fig. 4.5: *Conventional folded-cascode amplifier schematic.*

From a conventional FC opamp, the RFC structure can be obtained using simple modifications. The circuit of the RFC amplifier can be seen in Fig. 4.6. In this structure, the input transistor pair has been split into four devices and is represented by M1a/M1b and M2a/M2b. Each of these pairs is driven by the same input, hence retaining the same input capacitance as in Fig. 4.5. The transistors M3 and M4 are also split, with a ratio 1:K, into M3a/M3b and M4a/M4b to form current mirrors. These current mirrors together with the cross-over connection are used such that the small signal currents added at the sources of M5 and M6 are in phase. To ensure accurate mirroring in M3a/M3b and M4a/M4b, transistor M11 and M12 are included [18], [23].

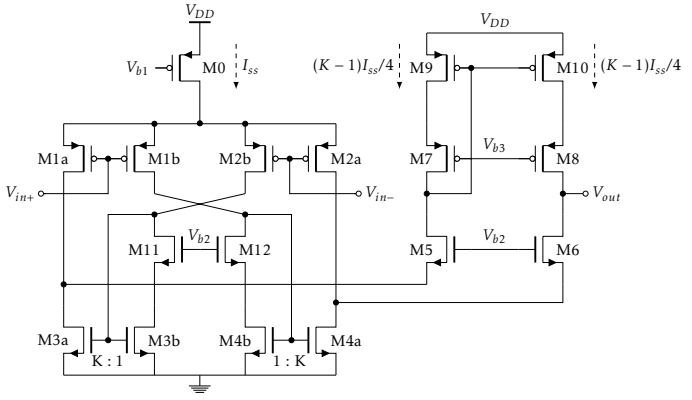


Fig. 4.6: *The recycling folded-cascode amplifier schematic [23].*

4.2.2 Recycling Folded-Cascode Characteristics

In [18], it is shown that the RFC provides enhanced features over the conventional FC. In this analysis, the devices are assumed to operate in saturation region and $K = 3$, to maintain equal power and areas of the FC [23].

First of all, it is shown that the transconductance is improved. From a small-signal analysis, the transconductance of the RFC is shown to be equal to $g_{m1a}(1 + K)$, where M1 in the FC is twice the size of M1a in the RFC, hence $g_{m1} = 2g_{m1a}$. Together with a device sizing ratio, K, it appears that the transconductance of the RFC is twice than the transconductance of the conventional FC. Hence the RFC has twice the unity-gain bandwidth for the same amount of power consumption. It is also shown that the RFC has a larger output impedance than the FC structure, hence the DC gain is also improved [23].

For the given modifications, the slew rate of the RFC is also enhanced compared to the conventional FC. If we assume that a large signal is applied to the input of the RFC, V_{in} will approach V_{DD}, i.e. transistor M1a and M1b turn off, which forces transistors M4b, M4a, and M6 into the cut-off region. Hence M2a is driven into the deep triode region, which redirects the available current through M2b. The current through M2b is then mirrored by M3a/M3b with a factor of K and then again mirrored by a factor of 1 to the output node. Hence the output capacitance is charged with a current of KI_{ss}, thus the slew rate is equal to KI_{ss}/C_L. Compared to the slew rate given in (3.32), the slew rate of the RFC structure is enhanced with a factor or K in the modified structure [23].

Since the RFC structure and the proposed SRE techniques offers benefits such as increased unity-gain frequency and slew rate without increasing area and power penalty, it has been utilized to reduce the settling time of the opamp in this thesis work.

5

Analog Test Buffer Application

The goal of this thesis is to reduce the settling time for a single-stage FC amplifier using different techniques to improve both the slew rate and unity-gain frequency. To be able to examine this topic, a single-ended FC amplifier was designed in a 180 nm CMOS process as the starting point. The amplifier is intended for test buffer applications and is used in unity-gain feedback configuration. This chapter will describe the given test buffer implementation, together with the the characteristics of the PDK used and how the enhancement techniques were implemented and tested.

5.1 Test Buffer Implementation

The implemented test buffer is used to buffer on-chip analog reference signal for off-chip measurement. An overview of the test buffer setup can be seen in Fig. 5.1. The on-chip reference signals are provided to a multiplexer (MUX), that redirects one of the signals to the non-inverting input of the amplifier. The amplifier is implemented as a unity-gain buffer, where its output is shorted to its inverting input, and uses a complementary input, single-ended folded-cascode topology, as discussed in Chapter 3.2. The amplifier is then used to drive the external pad and tester probe for off-chip measurement. The pad parasitics are realized with R_{pad} and the parasitic loads from the test probe are realized with C_L and R_L.

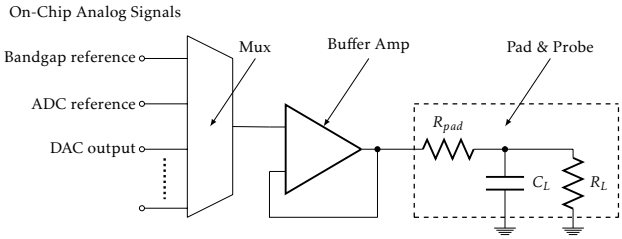


Fig. 5.1: *Schematic of the test buffer setup.*

5.1.1 Amplifier Architecture

The given buffer opamp seen in Fig. 5.1, is implemented using a complementary input, single-ended FC amplifier together with a biasing network. The biasing network consists of a bandgap reference using low-voltage cascode current mirrors. Due to the scope of this thesis, the biasing network will not be studied in detail. The opamp structure can be seen in Fig. 5.2, where I_{ref1} and I_{ref2} are the reference currents used by the biasing network to provide the biasing voltages V_{biasN}, $V_{biasP,1}$ and $V_{biasP,2}$. V_X indicates the node for large-signal transient detection used in SRE1, as discussed in Chapter 4.1.2.

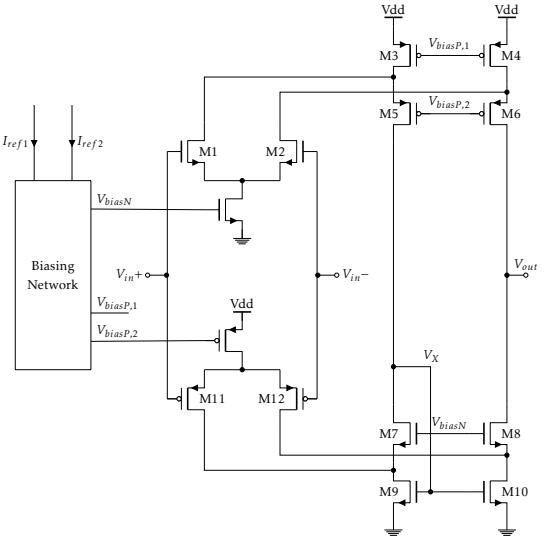


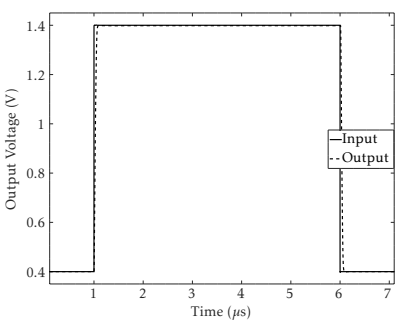
Fig. 5.2: *Schematic of the given amplifier in buffer application.*

The performance specifications of the given amplifier can be seen in Table. 5.1. It shows the performance values of the given opamp during nominal condition and the worst-case value for each parameter over the entire set of PVT and Monte-Carlo simulations. As seen in Table 5.1, the worst-case settling time is approximately 1000 ns, and the goal of this thesis was to reduce the settling time by a factor of 10, i.e. reduce the settling time below 100 ns. The settling time is defined by a 0.1 % error band, and was given from the provided specification in this thesis.

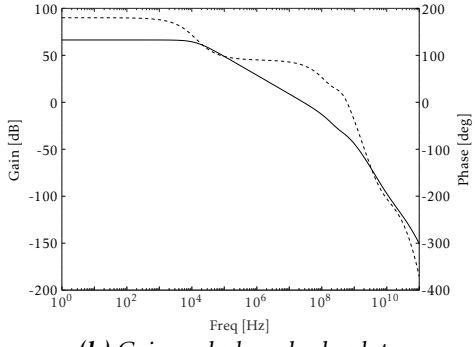
Table 5.1: *Performance parameters of implemented FC*

Parameter	Nominal	Worst-case
SR+/SR- [V/us]	18.3/20.7	8.5/10.4
Settling Time Lo-Hi [ns] (0.1 % of input step)	81.4	1020.0
Settling Time Hi-Lo [ns] (0.1 % of input step)	127.0	349.5
Unity-Gain Freq. [MHz]	27.21	15.49
Gain [dB]	66.3	45.2
Phase Margin [deg]	78.6	75.4
Gain Margin [deg]	36.0	34.3
Idc [mA]	0.891	1.425
Itran (avg.) [mA]	0.837	1.352
Power Consumption [mW]	1.507	2.677
Input Offset [mV]	0.231	4.556

To give a full overview of the implemented test buffer, the 1 V input step transient response can be seen in Fig. 5.3 (a), together with its bode characteristics in (b), where the dashed line shows the phase over frequency, and the solid line the gain over frequency.



(a) *1 V step input response.*



(b) *Gain and phase bode plot.*

Fig. 5.3: *Transient response and bode plot of implemented FC.*

5.1.2 Device Characteristics

The test buffer is designed in a 1.8 V, 180 nm CMOS technology. The intrinsic gain of the MOS transistors defined as g_m/g_{ds} and is an important factor in analog design. Fig. 5.4 shows the intrinsic gain vs. V_{DS} for the minimum sized NMOS transistor used in this thesis. For NMOS, V_{TH} = 450 mV and for PMOS, V_{TH} = 500 mV. It is seen that the intrinsic gain is increases when V_{GS} gets closer to the threshold voltage. The maximum intrinsic gain obtained from a device is approximately 35 V/V.

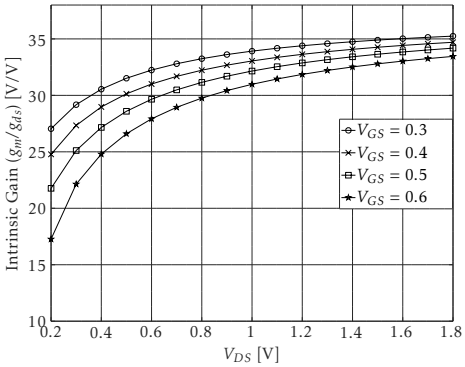


Fig. 5.4: *Nominal intrinsic gain of minimum-sized NMOS transistor.*

The subthreshold leakage of the MOS device is an important contributor to static power in an analog low-power designs. For the MOS transistors, the subthreshold leakage current increases with temperature while the threshold voltage reduces with temperature. The variation of leakage current and threshold voltage with temperature for a minimum-sized, standard-V_{TH} device used in this thesis, are shown in Fig. 5.5.

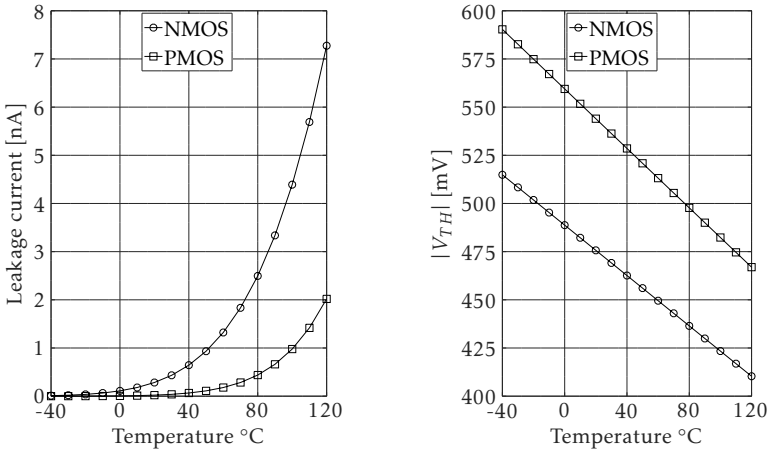


Fig. 5.5: *Variation of leakage current and threshold voltage with temperature.*

5.2 Simulation Setup

All structures presented in this thesis were simulated over all process, temperature and supply voltage variations, including Monte-Carlo simulations to examine the mismatch behaviour of the circuit. The process corners included 12 different device process variations, such as typical-typical (TT), slow-slow (SS), slow-fast (SF), fast-fast(FF) etc. The voltage corners ranged from ±10 % of the supply voltage and the temperature corners ranged from $-40\ ^{\circ}C$ to $+85\ ^{\circ}C$. The PVT corner conditions can be seen in Table. 5.2.

Table 5.2: *Corner Conditions.*

Corner Parameter	Nominal	Min	Max
Supply Voltage [V]	1.8	1.62	1.98
Temperature [°C]	25	-40	85
Process	Nom	All Process Corners	

The testbench used for analyzing the opamp can be seen in Fig. 5.6, where the voltage source, V_{in}, was used to apply a large signal step, in order to analyze both the slewing and linear behaviour of the amplifier. All settling time measurements were taken at the output, V_{out}. The pad resistance, R_{pad}, and test probe loads, C_L and R_L, were included in all simulations, where $R_{pad} = 200\ \Omega$, $C_L = 15$ pF and $R_L = 10\ \text{M}\Omega$.

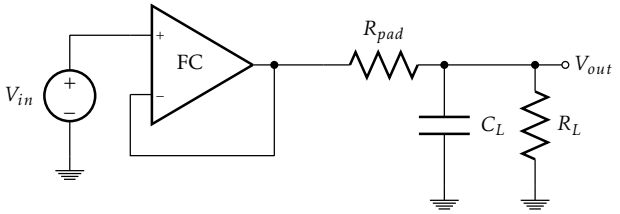


Fig. 5.6: *Schematic of the test buffer testbench.*

In order to measure the settling time of the amplifier, a 1 V step was applied at the input. In order to ensure that the step was applied within reasonable ranges between ground and supply, the input step was applied from $(V_{DD}/2) - 0.5$ to $(V_{DD}/2) + 0.5$, i.e. adapting over different supply voltage variations. If the applied step was close to either rail, the voltage headroom for several devices became too small, hence they entered the cut-off region. The different input steps over the supply voltage variations is shown in Table. 5.3.

Table 5.3: *Simulation input steps.*

Supply Voltage [V]	Input Step [V]
1.62	0.31 to 1.31
1.8	0.4 to 1.4
1.98	0.49 to 1.49

All simulations were executed using Cadence Virtuoso, and the simulation results are presented in Chapter 6.

5.3 Test Buffer Improvement

The first approach to reduce the settling time of the given test buffer application, was to examine if improvement could be achieved without changing the amplifier structure, i.e. only by resizing the devices of the amplifier. The resizing was done in order to ensure a robust improved design over all PVT conditions and mismatch scenarios, before applying any SRE technique or RFC structure to it. After the device size optimization of the given amplifier, SRE techniques discussed in Chapter 4.1, and the recycling FC structure, discussed in Chapter 4.2, were incorporated and tested.

5.3.1 Size Optimization of the Implemented Folded-Cascode

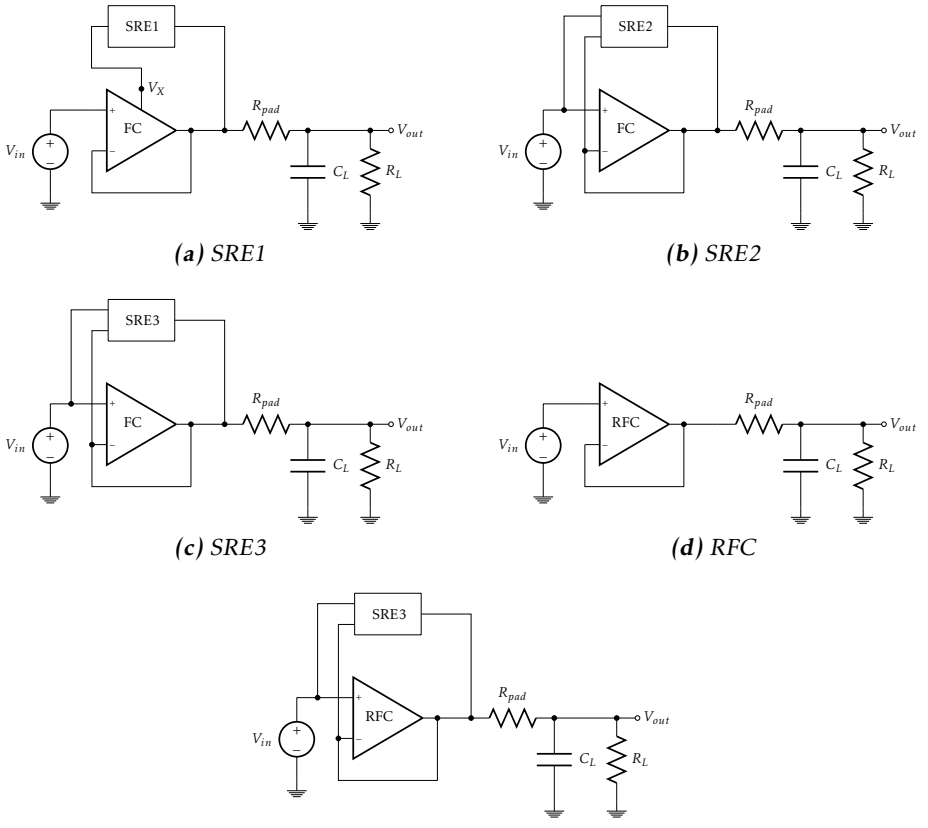
The first task of the thesis was to examine if the amplifier performance could be improved without changing its architecture or adding additional enhancement circuits to it. The two main reasons for this were, first to reduce the settling time spread over PVT and mismatch conditions, to ensure a robust core amplifier design before including proposed improvement techniques, and second to reduce the area and power consumption, if possible.

As seen in Table. 5.1, the settling time variation of the given opamp is very large over the different PVT conditions. To solve this issue, an iterative and extensive device sizing was done, in order to find a good balance between all performance parameters and the spread of total settling time. The resizing was done with the aid of performance parameters derived in Section 3.2. The resized version of the given amplifier achieved smaller settling time spread over PVT and mismatch conditions, as well as lowered power consumption. The simulation results are presented and discussed in 6.1.

The given amplifier was replaced with the optimized amplifier before analyzing the effects of the SRE techniques and the RFC structure. Hence the optimized amplifier will be considered as the core amplifier further on in this document.

5.3.2 SRE and RFC Implementation

After optimizing the given amplifier, the SRE techniques and the RFC structure, discussed in Chapter 4.1 and 4.2 were implemented in the opamp design. To analyze the different enhancement circuits the same testbench as discussed in chapter 5.2 was used. The absence of the parasitic inductance from the bond wire was noticed at a late stage in this work. Instead of adding a model of the bond wire, the test bench was kept the same for all structures in order to compare their simulation results. A total of five different enhancement structure were examined, three structures including the three different SRE techniques (SRE1, SRE2 and SRE3), one structure including the RFC structure and one structure including a combination of the SRE3 technique and the RFC structure. The five different test setups are shown in Fig. 5.7.



(a) *SRE1*

(b) *SRE2*

(c) *SRE3*

(d) *RFC*

(e) *RFC + SRE3*

Fig. 5.7: *Schematics of the enhancement circuit test setups.*

Fig. 5.7 (a) shows the implementation of the SRE1 technique, where the input of the SRE is connected to the intermediate node, V_X, of the core amplifier seen in Fig. 5.2. The bias reference voltage used in SRE1, V_{bias} (shown in Fig. 4.2), is provided by the same biasing network used in the core amplifier. The SRE1 circuit was sized according to the proposed structure described in Chapter 4.1.2, and the simulation results are presented in Section 6.2.

Fig. 5.7 (b) and (c) shows the implementation of the SRE2 and the SRE3 technique respectively. Both techniques use an input referred sensing circuit, hence attached to the inverting and non-inverting inputs of the core amplifier. The current sources, I_1 and I_2, used in the circuits (shown in Fig.4.3 and Fig. 4.4), are provided by a mirrored current from the biasing network of the core amplifier. The devices were sized according to the proposed sizing strategy described in Sections 4.1.3 and 4.1.4. The simulation results from the implementation of SRE2 and SRE are presented in Sections 6.3 and 6.4 respectively.

Fig. 5.7 (d) shows the implementation of the RFC structure. The RFC were designed according to the recycling structure shown in Fig. 4.6. The input pair transistors, $M1a/M1b$ and $M2a/M2b$ were split in two, and the transistors $M3a/M3b$ and $M4a/M4b$ were split with a ratio 3:1 and 1:3 respectively. The total size of the transistors remained the same as the core amplifier. The simulation results of the RFC structure are presented in chapter 6.5

Fig. 5.7 (e) shows the implementation of the combined structure between the SRE3 technique and the RFC structure. Some new sizing of the SRE3 circuits were made in order to achieve promising results. The major sizing changes were done at the clamp transistors $M3$ and $M3a$, shown in Fig.4.4, in order to prevent some unwanted overshoots that occurred at the end of the transitions for some PVT conditions. By implementing this structure, some promising results were achieved. The simulation results are presented in Section 6.6.

6

Results and Discussion

Throughout the thesis a total of five different improved FC amplifier structures were implemented and tested. One for each SRE technique presented in Chapter 4.1, the RFC amplifier structure presented in Chapter 4.2 and one combination of SRE3 together with the RFC amplifier structure. This chapter will present the simulation results from the improved resized amplified and the results from each implementation, together with a discussion. I order to ensure a certain settling time performance of the amplifier after chip manufacturing, the worst-case scenarios were considered. For each performance parameter, the worst-case value among all simulations (PVT corners, Monte-Carlo included) will be presented for each structure. The simulation setup is described in Section 5.2 and the PVT corner conditions used in the simulations is shown in Table 5.2.

6.1 Resized Amplifier Simulation Results

The given amplifier, referred as the original amplifier in this chapter, and the resized version were both simulated over the same PVT conditions. Table 6.1 shows the performance parameter values for the nominal condition, i.e. V_{DD} = 1.8 V, typical process corner and temperature = 25°C, and the worst-case value of all parameters.

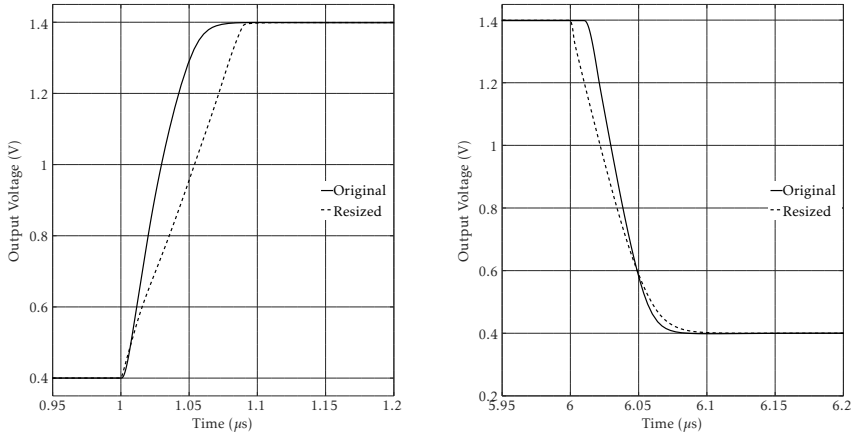
An overall reduction in size of the amplifier was achieved, except for the input transistor pair, which were sized slightly wider. By resizing the given FC amplifier, a lower power consumption was achieved and the worst-case settling time for the Lo-Hi transition was reduced by almost 50 %. By sizing up the input pair, together with a resizing of the load transistors, the gain was slightly enhanced, which contributed to the reduction of the settling time spread over PVT corners. However, the slew rate in both Lo-Hi and Hi-Lo transitions were diminished as

compared to the original amplifier.

Table 6.1: *Nominal and worst-case simulation results (original vs. resized).*

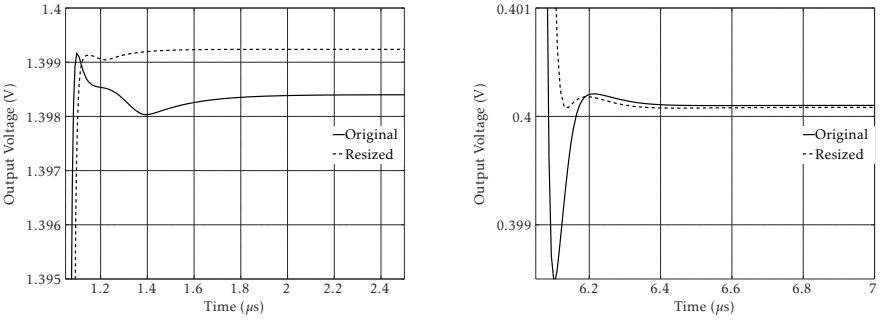
	Nominal		Worst-case	
Parameter	**Original**	**Resized**	**Original**	**Resized**
SR+/SR- [V/us]	18.3/20.7	11.0/14.6	8.5/10.4	3.9/6.8
Settling Time Lo-Hi [ns] (0.1 % of input step)	81.4	104.3	1020.0	383.3
Settling Time Hi-Lo [ns] (0.1 % of input step)	127.0	106.6	349.5	324.4
Unity-Gain Freq. [MHz]	27.2	26.1	15.5	15.0
Gain [dB]	66.34	70.65	45.24	48.36
Phase Margin [deg]	78.59	76.55	75.44	72.48
Gain Margin [deg]	36.0	28.0	34.3	22.5
Idc [mA]	0.890	0.458	1.425	0.723
Itran (avg.) [mA]	0.837	0.422	1.352	0.678
Power Consumption [mW]	1.507	0.760	2.677	1.343
Input Offset [mV]	0.231	0.130	4.556	3.289

The idea was to compensate the reduction in slew rate with proposed SRE techniques, hence this sacrifice was considered acceptable. The effect of the slew rate reduction can be seen in Fig. 6.1, where Fig. 6.1 (a) shows the Lo-Hi output transition, and Fig. 6.1 (b) the Hi-Lo output. While the slew rate was sacrificed, the linear settling improved, and the effect from this can be seen in Fig. 6.2, where Fig. 6.2 (a) and Fig. 6.2 (b) shows the linear settling for the Lo-Hi and Hi-Lo transition respectively.



(a) *Lo-Hi Transition* ***(b)*** *Hi-Lo Transition*

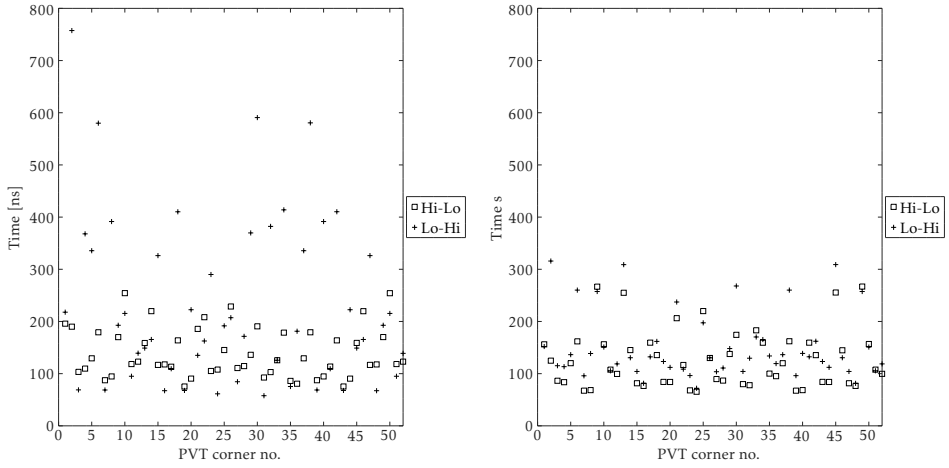
Fig. 6.1: *Output transients (Original vs. Resized).*



(a) *Lo-Hi Transition* ***(b)*** *Hi-Lo Transition*

Fig. 6.2: *Linear settling behaviour (Original vs. Resized).*

The settling time variations over all PVT corners are shown in Fig. 6.3, where Fig. 6.3 (a) and Fig. 6.3 (b) presents the total settling time for both Lo-Hi and Hi-Lo transition against all PVT corners, for the original and resized amplifier respectively.



(a) *Original* ***(b)*** *Resized*

Fig. 6.3: *Settling time variation over PVT corners (Original vs. Resized).*

It is seen that the worst-case settling time and settling time spread over PVT corners are reduced due to the resizing effort. Monte-Carlo simulation results from the original amplifier and the resized amplifier is shown in Table 6.2.

Table 6.2: *Worst-case PVT Monte-Carlo simulation results (original vs. resized).*

	Original				Resized			
Parameter	**Min**	**Max**	**Mean**	**Std Dev**	**Min**	**Max**	**Mean**	**Std Dev**
SR+/SR- [V/us]	11.92/15.38	18.24/20.92	14.95/17.9	1.07/0.95	8.62/10.63	14.48/15.18	11.2/12.48	0.99/0.73
Settling Time Lo-Hi [ns] (0.1 % of input step)	119.9	1020.0	669.6	217.0	98.03	383.3	254.1	74.85
Settling Time Hi-Lo [ns] (0.1 % of input step)	168.4	349.5	200.0	27.3	110.7	324.4	151.9	41.65
Unity-Gain Freq. [MHz]	17.63	24.57	21.17	1.14	16.33	22.93	19.86	1.13
Gain [dB]	45.24	64.68	57.23	5.88	48.36	68.71	60.42	6.232
Phase Margin [deg]	78.73	83.32	81.21	1.01	77.43	82.11	79.92	1.11
Gain Margin [deg]	35.99	38.35	36.94	0.37	31.81	36.62	34.43	0.688
Idc [mA]	0.684	1.244	0.920	0.122	0.347	0.619	0.463	0.055
Itran (avg.) [mA]	0.654	1.188	0.883	0.118	0.324	0.577	0.434	0.051
Power Consumption [mW]	1.059	1.925	1.431	0.191	0.525	0.935	0.704	0.082
Input Offset [mV]	0.005	4.556	1.153	0.861	0.003	3.289	0.787	0.609
Applied Input Step [Vpp]	1							
Load Capacitance [pF]	15							
Technology	0.18 um CMOS							

6.2 SRE1 Implementation Results

The nominal and worst-case PVT condition simulation results from the implementation of the SRE1 technique are shown in Table. 6.3. If we compare the nominal PVT condition simulation result of SRE1 with the results from the resized amplifier, we notice that the attached circuitry does not have a major impact on the small signal parameters of the amplifier, as stated in Section 4.1.2. We also see that the SRE circuit works as expected and enhances the slew rate for both Hi-Lo and Lo-Hi transition. With a negligible change in the small signal behaviour and a increase of slew rate, the total settling time was reduced.

Table 6.3: *Nominal and worst PVT simulation results for SRE1*

	SRE1	
Parameter	**Nominal**	**Worst PVT**
SR+/SR- [V/us]	24.4/61.6	9.0/7.5
Settling Time Lo-Hi [ns] (0.1 % of input step)	89.6	292.7
Settling Time Hi-Lo [ns] (0.1 % of input step)	93.2	2390.0
Unity-Gain Freq. [MHz]	25.9	14.9
Gain [dB]	70.64	49.15
Phase Margin [deg]	75.8	71.7
Gain Margin [deg]	32.24	24.01
Idc [mA]	0.630	0.996
Itran (avg.) [mA]	0.607	0.954
Power Consumption [mW]	1.092	1.890
Input Offset [mV]	0.109	1.138

However, the SRE1 technique had some major issues in some PVT conditions. As seen in the Worst PVT column in Table 6.3, the Hi-Lo settling time exceeds almost 2400 ns, which is unacceptable. This behavior got even worse in device mismatch situations as seen in the Monte-Carlo simulation results over the worst supply voltage and temperature condition in Table 6.4.

Table 6.4: *Worst-case Monte-Carlo simulation results for SRE1.*

	SRE 1			
Parameter	**Min**	**Max**	**Mean**	**Std Dev**
SR+/SR- [V/us]	9.1/32.0	22.3/53.6	15.2/44.3	4.2/3.0
Settling Time Lo-Hi [ns] (0.1 % of input step)	110.6	375.5	252.4	73.37
Settling Time Hi-Lo [ns] (0.1 % of input step)	113.9	3081.0	823.3	647.8
Unity-Gain Freq. [MHz]	16.3	22.9	19.6	1.1
Gain [dB]	48.29	68.63	60.32	6.21
Phase Margin [deg]	76.7	81.8	79.3	1.1
Gain Margin [deg]	33.9	36.8	35.2	0.5
Idc [mA]	0.476	0.852	0.638	0.076
Itran (avg.) [mA]	0.467	0.804	0.618	0.066
Power Consumption [mW]	0.757	1.302	1.001	0.106
Input Offset [mV]	0.002	3.297	0.805	0.627
Supply Voltage [V]	1.62			
Temperature [°C]	85			
Applied Input Step [Vpp]	1			
Load Capacitance [pF]	15			
Technology	0.18 μm CMOS			

The settling time variations can be seen in Fig. 6.4, which shows the spread of settling time for the Lo-Hi transition and the Hi-Lo transition over the PVT corners. We see that the settling time spread for the Hi-Lo transition is very large for many PVT conditions.

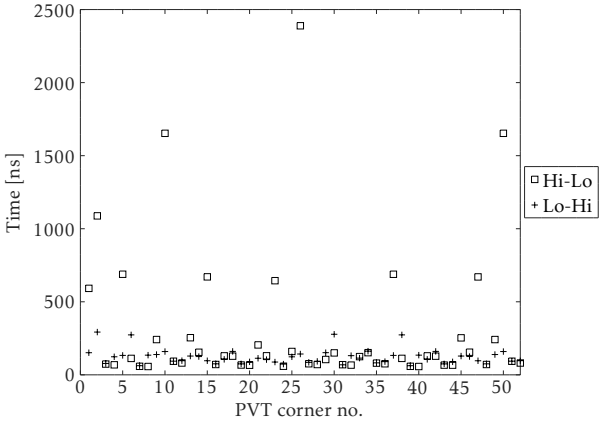


Fig. 6.4: *Settling time over PVT corners - SRE1.*

The reason for this was that the intermediate sensing node, V_X (seen in Fig. 5.2), and the provided bias voltage, V_{bias} (seen in Fig. 4.2), had large variations over the PVT corners. Due to these variations, the required operation regions in order to provide slewing capability (seen in Table. 4.1), could not be satisfied for all PVT conditions. In these cases, oscillations were seen at the output node, before it settled.

6.3 SRE2 Implementation Results

The nominal and worst-case PVT condition simulation results from the implementation of the SRE2 technique is shown in Table. 6.5. We see that the implementation of the SRE2 technique does not affect the small signal behaviour of the core amplifier, as stated in Section 4.1.3. We also see that the slew rate in a Lo-Hi transition is enhanced in both nominal condition and the worst-case PVT condition, though the slew rate for the Hi-Lo transition is unaffected by the circuit.

Table 6.5: *Nominal and worst PVT simulation results for SRE2*

	SRE2	
Parameter	**Nominal**	**Worst PVT**
SR+/SR- [V/us]	106.1/14.1	58.0/6.7
Settling Time Lo-Hi [ns] (0.1 % of input step)	54.9	414.9
Settling Time Hi-Lo [ns] (0.1 % of input step)	108.2	269.3
Unity-Gain Freq. [MHz]	25.9	14.8
Gain [dB]	70.6	49.3
Phase Margin [deg]	76.0	64.6
Gain Margin [deg]	25.6	21.3
Idc [mA]	0.510	0.794
Itran (avg.) [mA]	0.459	0.742
Power Consumption [mW]	0.825	1.469
Input Offset [mV]	0.128	1.207

Compared with the SRE1 technique, the implementation of SRE2 shows a more stable solution for settling time reduction. Though the circuit does not work as expected for a Hi-Lo transition, due to the extra time delay needed for mirroring the current from M3 to the output node (seen in Fig. 4.3), the slew rate in a Hi-Lo transition is left unchanged. We also see that the implementation of the SRE2 technique increases the spread of settling time in worst-case PVT condition. Time was not spent to finding the root cause of this effect. It could be a result of the current mirroring at the output stage of the SRE. Instead of an in-depth investigation into this degradation in the SRE2 technique, the SRE3 structure was implemented and tested.

Table 6.6: *Worst-case Monte-Carlo simulation results for SRE2*

	SRE 2			
Parameter	**Min**	**Max**	**Mean**	**Std Dev**
SR+/SR- [V/us]	58.8/10.33	93.0/14.9	78.9/12.2	6.9/0.7
Settling Time Lo-Hi [ns] (0.1 % of input step)	80.9	534.4	335.8	128.3
Settling Time Hi-Lo [ns] (0.1 % of input step)	114.7	334.0	161.8	46.6
Unity-Gain Freq. [MHz]	16.0	23.3	19.6	1.1
Gain [dB]	48.0	68.5	60.3	6.2
Phase Margin [deg]	76.1	81.9	79.5	1.2
Gain Margin [deg]	29.1	35.8	312.0	1.2
Idc [mA]	0.385	0.663	0.510	0.057
Itran (avg.) [mA]	0.349	0.607	0.465	0.052
Power Consumption [mW]	0.565	0.983	0.753	0.084
Input Offset [mV]	0.004	3.246	0.771	0.586
Supply Voltage [V]	1.62			
Temperature [°C]	85			
Applied Input Step [Vpp]	1			
Load Capacitance [pF]	15			
Technology	0.18 μm CMOS			

Monte-Carlo simulation results for the worst-case supply voltage and temperature condition are presented in Table. 6.6 and the settling time spread over PVT corners are shown in Fig. 6.5. Compared to the SRE1 technique, the implementation of SRE2 achieved better results.

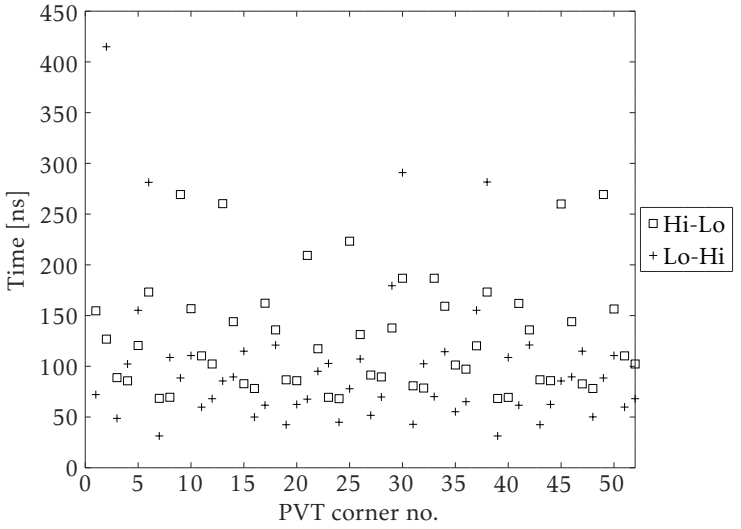


Fig. 6.5: *Settling time over PVT corners - SRE2.*

6.4 SRE3 Implementation Results

The nominal and worst-case PVT condition simulation results of the improved version of the SRE3 technique are presented in Table. 6.7. As expected the implementation of SRE3 does not affect the small signal behaviour of the amplifier. The SRE3 enhances the slew rate in both Lo-Hi and Hi-lo large-signal transitions, compared to the SRE2 technique. By introducing the clamp transistors M3 and M3a (shown in Fig. 4.4) a reduction of settling time spread over PVT conditions was achieved.

Table 6.7: *Nominal and worst PVT simulation results for SRE3*

	SRE3	
Parameter	**Nominal**	**Worst PVT**
SR+/SR- [V/us]	124.3/213.4	65.3/12.3
Settling Time Lo-Hi [ns] (0.1 % of input step)	60.7	165.5
Settling Time Hi-Lo [ns] (0.1 % of input step)	65.1	202.8
Unity-Gain Freq. [MHz]	26.0	14.9
Gain [dB]	70.6	49.3
Phase Margin [deg]	76.5	69.13
Gain Margin [deg]	26.24	21.7
Idc [mA]	0.572	0.890
Itran (avg.) [mA]	0.488	0.792
Power Consumption [mW]	0.878	1.569
Input Offset [mV]	0.130	1.222

The Monte-Carlo simulation results, shown in Table. 6.8, also shows a good performance over mismatch conditions. The settling time variation over PVT conditions can be seen in Fig. 6.6.

Table 6.8: *Worst-case Monte-Carlo simulation results for SRE3*

	SRE 3			
Parameter	**Min**	**Max**	**Mean**	**Std Dev**
SR+/SR- [V/us]	86.6/9.32	126.7/210.6	102.7/193.0	7.4/14.3
Settling Time Lo-Hi [ns] (0.1 % of input step)	49.7	187.4	68.2	8.8
Settling Time Hi-Lo [ns] (0.1 % of input step)	54.6	246.7	107.2	15.1
Unity-Gain Freq. [MHz]	16.8	34.5	20.7	2.0
DC Gain [dB]	50.5	71.2	55.3	4.9
Phase Margin [deg]	36.6	81.1	79.4	2.3
Gain Margin [deg]	19.3	36.2	30.9	2.4
Idc [mA]	0.278	0.622	0.488	0.061
Itran (avg.) [mA]	0.233	0.550	0.428	0.057
Power Consumption [mW]	0.377	0.891	0.694	0.091
Input Offset [mV]	0.01	3.305	0.819	0.604
Supply Voltage [V]	1.62			
Temperature [°C]	-40			
Applied Input Step [Vpp]	1			
Load Capacitance [pF]	15			
Technology	0.18 μm CMOS			

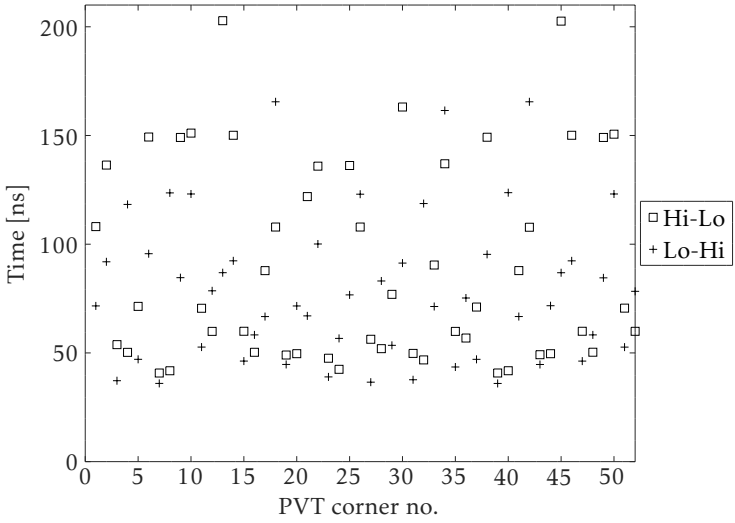


Fig. 6.6: *Settling time over PVT corners - SRE3.*

SRE3 shows the best settling time performance among the studied SRE techniques. The circuit shows good stability over the all PVT conditions and mismatch behaviour. The small signal behavior of the amplifier and output swing were unaffected. The slew rate for both Lo-Hi and Hi-Lo transitions are enhanced and the settling time spread is reduced. Hence SRE3 is a good candidate for settling time improvement in a FC amplifier.

6.5 RFC Implementation Results

The nominal and worst-case PVT condition simulation results from the implemented RFC structure can be seen in Fig. 6.9. The simulation results for the nominal PVT condition show that the RFC structure reuses the current of the previously idle devices in an efficient way, hence the reduced power consumption compared with the conventional FC amplifier. A general enhancement in both large signal and small signal performance was achieved with this structure. The result shows improved DC gain, unity-gain frequency and slew rate, which reduced the total settling time of the RFC amplifier.

Table 6.9: *Nominal and worst PVTsimulation results for RFC*

	RFC	
Parameter	**Nominal**	**Worst PVT**
SR+/SR- [V/us]	22.7/24.3	9.1/11.8
Settling Time Lo-Hi [ns] (0.1 % of input step)	72.9	148.3
Settling Time Hi-Lo [ns] (0.1 % of input step)	85.0	415.1
Unity-Gain Freq. [MHz]	39.9	24.1
Gain [dB]	78.0	59.6
Phase Margin [deg]	60.28	56.4
Gain Margin [deg]	15.5	13.8
Idc [mA]	0.416	0.581
Itran (avg.) [mA]	0.253	0.442
Power Consumption [mW]	0.454	0.875
Input Offset [mV]	0.057	0.336

Table 6.10: *Worst-case Monte-Carlo simulation results for RFC*

	RFC			
Parameter	**Min**	**Max**	**Mean**	**Std Dev**
SR+/SR- [V/us]	8.2/13.2	20.8/20.8	14.7/17.4	2.0/1.3
Settling Time Lo-Hi [ns] (0.1 % of input step)	73.6	155.4	97.3	11.4
Settling Time Hi-Lo [ns] (0.1 % of input step)	103.6	314.6	159.6	24.0
Unity-Gain Freq. [MHz]	24.8	41.2	34.4	2.6
DC Gain [dB]	57.6	76.7	72.1	3.7
Phase Margin [deg]	60.6	66.8	62.8	1.1
Gain Margin [deg]	15.6	19.9	16.6	0.6
Idc [mA]	0.274	0.383	0.323	0.018
Itran (avg.) [mA]	0.143	0.206	0.173	0.010
Power Consumption [mW]	0.232	0.334	0.280	0.017
Input Offset [mV]	0.0004	2.376	0.594	0.461
Supply Voltage [V]	1.62			
Temperature [°C]	-40			
Applied Input Step [Vpp]	1			
Load Capacitance [pF]	15			
Technology	0.18 μm CMOS			

The Monte-Carlo simulation results for the worst-case supply voltage and temperature condition are presented in Table. 6.10 and the settling time spread over PVT corners are presented in Fig. 6.7. From these results we see a lower settling time spread for the Lo-Hi transition, but a worse spread in the Hi-Lo transition compared with the conventional FC amplifier. This behavior will be discussed in Section 6.6

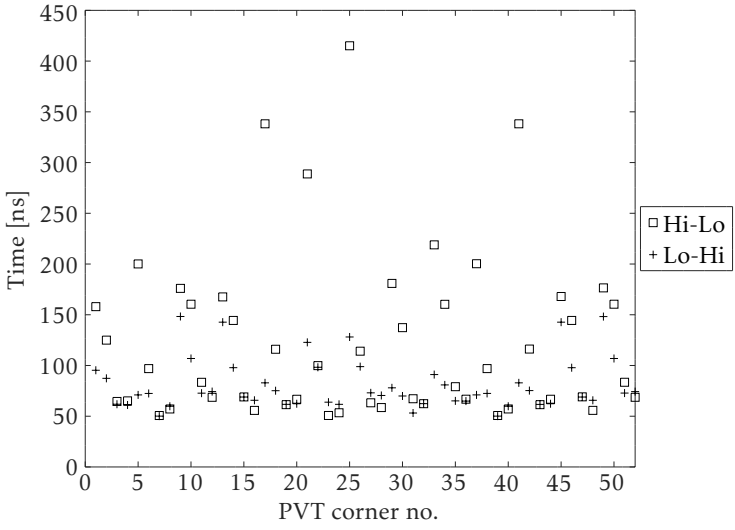


Fig. 6.7: *Settling time over PVT corners - RFC.*

Compared to the SRE techniques, which only enhance the large-signal behaviour of the amplifier, this structure shows an improvement in both the large signal and small-signal behavior.

6.6 RFC-SRE3 Implementation Results

Both the RFC structure and the SRE3 technique showed good performance with regard to settling time reduction. Since the RFC structure offered an overall performance enhancement of the amplifier and the SRE3 technique increased the slew rate in both Lo-Hi/Hi-Lo large-signal transitions, a combination of these two was tested. Simulation results for nominal PVT condition and the worst-case PVT condition is shown in Table. 6.11.

Table 6.11: *Nominal and worst PVT simulation results for RFC+SRE3*

	RFC-SRE3	
Parameter	**Nominal**	**Worst PVT**
SR+/SR- [V/us]	47.1/37.7	18.1/13.3
Settling Time Lo-Hi [ns] (0.1 % of input step)	48.5	89.1
Settling Time Hi-Lo [ns] (0.1 % of input step)	72.5	408.2
Unity-Gain Freq. [MHz]	38.9	23.4
Gain [dB]	77.9	60.0
Phase Margin [deg]	61.1	57.4
Gain Margin [deg]	16.1	14.2
Idc [mA]	0.528	0.734
Itran (avg.) [mA]	0.315	0.556
Power Consumption [mW]	0.568	1.100
Input Offset [mV]	0.063	0.344

We see that the combination shows great potential for settling time reduction of a FC amplifier. The settling time spread for a Lo-Hi transition is reduced by almost 70 % compared to the resized version of the amplifier. However, the structure also shows some instability over the some PVT conditions, and the worst-case settling time value for the Hi-Lo transition are almost doubled compared to the resized version of the core amplifier. The RFC-SRE3 implementation also showed similar results in mismatch scenarios, seen in the worst-case Monte-Carlo simulation results in Table. 6.12.

Table 6.12: *Worst-case Monte-Carlo simulation results for RFC-SRE3.*

	RFC-SRE3			
Parameter	**Min**	**Max**	**Mean**	**Std Dev**
SR+/SR- [V/us]	17.0/13.6	46.6/56.0	25.3/37.0	4.6/8.6
Settling Time Lo-Hi [ns] (0.1 % of input step)	48.4	88.1	68.2	7.4
Settling Time Hi-Lo [ns] (0.1 % of input step)	112.0	375.2	170.3	25.5
Unity-Gain Freq. [MHz]	25.5	39.3	33.3	2.4
DC Gain [dB]	57.8	76.7	72.0	3.8
Phase Margin [deg]	55.4	67.0	63.8	1.1
Gain Margin [deg]	16.4	19.9	17.3	0.6
Idc [mA]	0.339	0.478	0.405	0.024
Itran (avg.) [mA]	0.189	0.268	0.231	0.014
Power Consumption [mW]	0.306	0.435	0.374	0.023
Input Offset [mV]	0.0002	2.357	0.586	0.442
Supply Voltage [V]	1.62			
Temperature [°C]	-40			
Applied Input Step [Vpp]	1			
Load Capacitance [pF]	15			
Technology	0.18 um CMOS			

The settling time variations over all PVT corners is shown in Fig. 6.8. Although the spread for settling time in Lo-Hi transition is very low, the settling time spread for the Hi-Lo transition shows that the combination is vulnerable to PVT variations. After a more detailed study of the simulation results, it was noticed that these large spreads in settling time for the Hi-Lo transitions occurred at V_{DD} = 1.62 V. The simulation showed that some output transistors of the amplifier operated in cut-off region at a DC voltage level of 0.31 V, which considers with the lower limit of the voltage pulse applied at the amplifier input as shown in Table 5.3. Due to output transistors going into cut-off region for 0.31 V voltage level at the amplifier output, the DC gain was reduced below 35 dB.

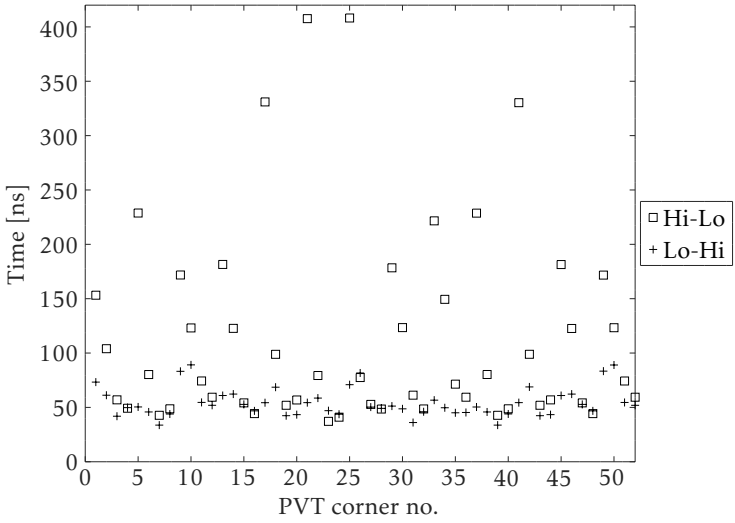


Fig. 6.8: *Settling time over PVT corners - RFC-SRE3.*

Another factor which can potentially contribute to the longer settling time for Hi-Lo transitions is that the RFC structure is applied to a conventional FC amplifier in [23] without complementary inputs. In this thesis, the RFC structure was implemented for the NMOS input pair and PMOS output transistors, while the PMOS input pair structure was left unchanged. This could cause some unbalance.

By shifting the input step 100 mV towards the voltage supply, i.e. a applied input step from 0.41 V to 1.41 V at 1.62 V voltage supply condition, a better performance was achieved. The settling time variation over PVT corners from the new simulation can be seen in Fig. 6.9.

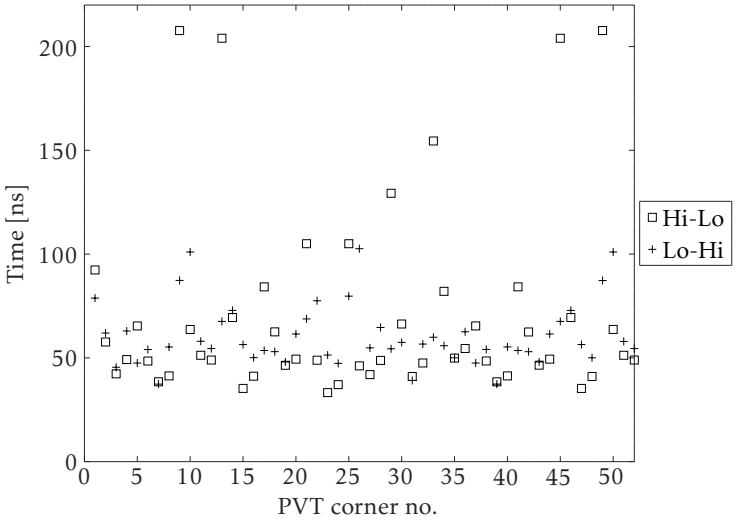


Fig. 6.9: *Settling time over PVT corners - RFC-SRE3 with shifted input step.*

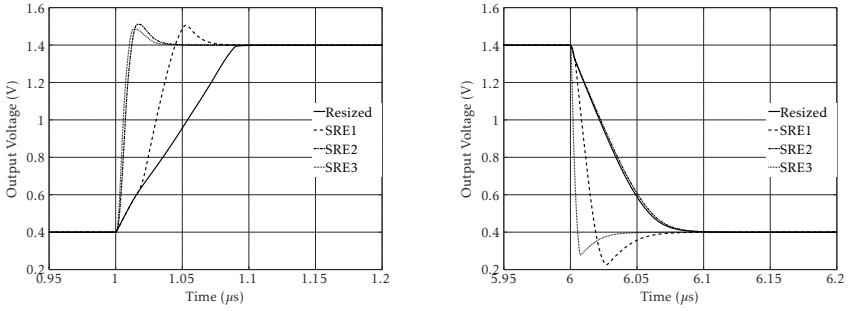
The settling time spread for a Hi-Lo transition was reduced by nearly half. However, while shifting the input step closer to the supply voltage, we start to see some larger spreads in the Lo-Hi transition settling time as well. Table 6.13 shows the simulation results for nominal and worst-case PVT condition for a shifter input step.

Table 6.13: *Nominal and worst PVT simulation results for RFC+SRE3 with 100 mV shifted input step.*

	RFC-SRE3	
Parameter	**Nominal**	**Worst PVT**
SR+/SR- [V/us]	42.0/39.6	16.0/17.4
Settling Time Lo-Hi [ns] (0.1 % of input step)	45.6	102.6
Settling Time Hi-Lo [ns] (0.1 % of input step)	49.5	207.7
Unity-Gain Freq. [MHz]	38.9	23.4
Gain [dB]	77.9	60
Phase Margin [deg]	61.1	57.4
Gain Margin [deg]	16.1	14.2
Idc [mA]	0.528	0.734
Itran (avg.) [mA]	0.357	0.583
Power Consumption [mW]	0.643	1.155
Input Offset [mV]	0.063	0.344

6.7 Results Summary

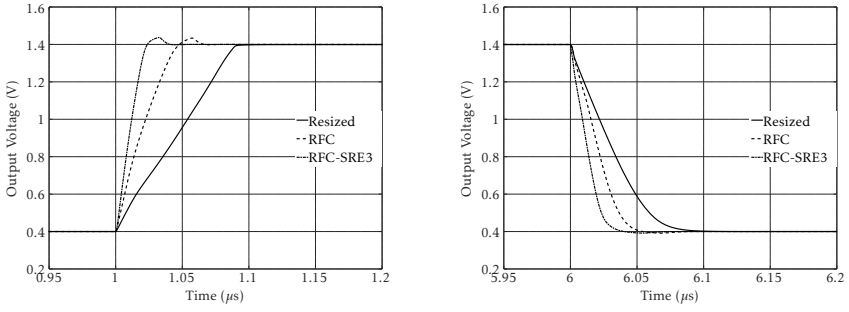
A total of five different settling time improvement structures were tested throughout this thesis. All structures listed in Fig. 5.7 except SRE2 (Fig. 5.7 (b)) worked well under nominal PVT conditions. However, when these structures are exposed to large process, supply voltage and temperature variations, all of them suffered performance degradation. For comparison, the settling transients of the three different SRE techniques are presented in Fig. 6.10, where Fig. 6.10 (a) and Fig. 6.10 (b) shows the rising and falling output transitions respectively.



(a) Lo-Hi Transition *(b) Hi-Lo Transition*

Fig. 6.10: *Settling transients for SRE techniques in nominal condition.*

In these graphs we clearly see the benefits of an SRE implementation. From previous discussed results, SRE3 showed the best performance of the three evaluated techniques. Hence it was combined with the RFC structure. The settling transients of the RFC structure and the combined RFC-SRE3 structure are presented in Fig. 6.11.



(a) Lo-Hi Transition *(b) Hi-Lo Transition*

Fig. 6.11: *Settling transients for RFC structures in nominal condition.*

As seen in Fig. 6.11 (a) and (b), the implementation of the RFC structure shows faster slewing in both rising and falling transitions, as well as an improved linear settling. The slewing periods are even further reduced when attaching the SRE3 circuit to it. It is worth noting, that the behaviors shown in Fig. 6.10 and Fig. 6.11 are for nominal PVT condition, and is not maintained for all PVT conditions, as discussed in Section 6.6. Comparison of the five different structures and the original and resized amplifiers is summarized in Table. 6.14.

Table 6.14: *Simulation results summary of settling time reduction schemes.*

	Original	**Resized**	**SRE1**	**SRE2**	**SRE3**	**RFC**	**RFC-SRE3**
Settling Time Lo-Hi [ns]	1020.0	383.3	375.5	534.4	187.4	155.4	89.1
Settling Time Hi-Lo [ns]	349.5	324.4	3081.0	334.0	246.7	415.1	408.2
Idc [mA]	1.425	0.723	0.996	0.794	0.890	0.581	0.734
Itran (avg.) [mA]	1.352	0.678	0.954	0.742	0.792	0.442	0.556
Power Consumption [mW]	2.677	1.343	1.890	1.469	1.569	0.875	1.100

From the summary we see that the best performance, in terms of settling time and power consumption, was achieved with the RFC-STE3 implementation. An approximately 90 % reduction in rising settling time was achieved, and at the same time reduce the total power consumption by almost 75 %. However, the RFC-SRE3 have some stability issues in the falling transition and do not improve the falling settling time. Due to the scope and time limitations of this thesis, the layout for the different structures were not designed, hence no area sizes are provided. To give an approximation of the area consumed by the different structures an area size estimation was done in Cadence Virtuoso. From the estimation, the implementation of the SRE3 technique increased the total area of the amplifier by 18 %, which also showed to be the largest area increase compared to the other structures. Conclusions and directions for future work will be presented in Chapter 7.

7

Conclusions and Future Work

Based on the problem formulation outlined in Section 1.3, this thesis presented five different structures that can be used for settling time reduction in a conventional FC opamp. The amplifier architecture and the enhancement circuits were designed and implemented in a 1.8 V, 0.18 μm CMOS process. The circuits were evaluated and simulated over different PVT and mismatch conditions, where worst-case performance parameters values were obtained. A resized version of the original amplifier was designed and evaluated, which achieved a settling time reduction for the Lo-Hi large-signal transition of approximately 60 % and a power consumption reduction of nearly 50 %. Different SRE techniques and a RFC structure were implemented in the resized FC amplifier, where a Lo-Hi settling time reduction of 85 % was achieved from the RFC structure. The best performance, in terms of settling time and power consumption, was achieved from a combined implementation of the RFC structure and the SRE3 technique. The implementation of the combined structure reduced the Lo-Hi setting time by approximately 90 % and the power consumption with almost 75 %.

Regarding the Hi-Lo transitions, the results presented in Chapter 6 illustrate that the resized amplifier as well as the five test structures reduced the settling time as compared to that in the original FC amplifier for the nominal PVT condition. However, it is seen from Table. 6.14 that the worst-case Hi-Lo transition is only reduced by 30 % using the SRE3 technique. Employment of the SRE1 technique resulted in an unacceptably degraded Hi-Lo settling time of 3081 ns. The remaining four structures produced only a variation of approximately ± 10 % for the worst-case Hi-Lo settling time period of the original amplifier.

7.1 Future Work

Based on the experience gained during the thesis work and the design challenges encountered, following topics have the potential for further investigation in this context.

- The worst-case value of the Hi-Lo settling time could not be improved by the use of the various modifications/enhancements elaborated upon in this work. It would be beneficial to analyze this shortcoming in detail for some of the structures and implement possible changes to address this drawback.
- Although the RFC structure resulted in enhancing the small-signal and large-signal performance of the amplifier, its inclusion adversely impacted the minimum output voltage level that could be supported. A lack of symmetry in the application of the RFC to the given amplifier is also a cause for concern. Hence both these aspects may be studied in detail to determine possible improvements.
- During the course of the thesis work spanning 20 weeks, various techniques to achieve power- and area-efficient settling time reduction were surveyed and implemented. Increased efforts on optimizing the SRE3 technique, which exhibited better PVT robustness, can be undertaken.

Single-stage amplifiers such as the FC amplifier are widely utilized in the industry/academia due to their numerous benefits. Settling time is a crucial parameter for these amplifiers and power efficient settling time reduction continues to be an area of active research [27–29]. The recently proposed signal and transient-current boosting (STCB) [27] circuit which enhances the small-signal performance and slew rate of a single-stage amplifier vividly illustrates the recent advances in this field.

Bibliography

[1] B. Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill higher education. Tata McGraw-Hill, 2002. ISBN 9780070529038. Cited on pages 5, 6, 7, 8, 9, 10, 12, 14, 15, 17, 18, 21, 22, 24, and 25.

[2] D. Johns and K.W. Martin. *Analog integrated circuit design*. John Wiley & Sons, 1997. ISBN 9780471144489. Cited on pages 6, 12, 13, and 25.

[3] R. I. Demrow. *Settling Time of Operational Amplifiers*. Analog Devices, inc, 1970. Cited on page 11.

[4] C. T. Chuang. "Analysis of the settling behavior of an operational amplifier". *IEEE J. Solid-State Circuits*, 17(1):74–80, Feb 1982. Cited on page 11.

[5] M. Tan and W. H. Ki. "A generic model for constructing three-stage amplifiers". In *2016 IEEE Int. Symp. Circuits Syst. (ISCAS)*, pages 466–469, May 2016. Cited on page 15.

[6] R. Mita, G. Palumbo, and S. Pennisi. "Well-defined design procedure for a three-stage CMOS OTA". In *2005 IEEE Int. Symp. Circuits Syst.*, pages 2579–2582 Vol. 3, May 2005. Cited on page 15.

[7] G. Di Cataldo, A. Dario Grasso, G. Palumbo, and S. Pennisi. "Single-miller all-passive compensation network for three-stage OTAs". In *2015 European Conf. Circuit Theory and Design (ECCTD)*, pages 1–4, Aug 2015. Cited on page 15.

[8] S. S. Chong and P. K. Chan. "Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load". *IEEE J. Solid-State Circuits*, 47(9):2227–2234, Sept 2012. Cited on page 15.

[9] D. Marano, A. D. Grasso, G. Palumbo, and S. Pennisi. "Optimized active single-miller capacitor compensation with inner half-feedforward stage for very high-load three-stage OTAs". *IEEE Trans. on Circuits Syst. I*, 63(9): 1349–1359, Sept 2016. Cited on page 15.

[10] S. Seth and B. Murmann. "Settling time and noise optimization of a three-stage operational transconductance amplifier". *IEEE Trans. Circuits Syst. I*, 60(5):1168–1174, May 2013. Cited on page 15.

[11] P.E. Allen and D.R. Holberg. *CMOS Analog Circuit Design*. Oxford series in electrical and computer engineering. Oxford University Press, 2002. ISBN 9780195116441. Cited on pages 18, 20, and 21.

[12] B. Lipka, U. Kleine, J. C. Scheytt, and K. Schmalz. "Design of a complementary folded-cascode operational amplifier". In *2009 IEEE Int. SOC Conference (SOCC)*, pages 111–114, Sept 2009. Cited on page 23.

[13] M. K. Hati and T. K. Bhattacharyya. "A power efficient and constant-gm 1.8 V CMOS operational transconductance amplifier with rail-to-rail input and output ranges for charge pump in phase-locked loop". In *2012 International Conference on Devices, Circuits and Systems (ICDCS)*, pages 38–43, March 2012. Cited on page 23.

[14] R. E. Vallee and E. I. El-Masry. "A very high-frequency CMOS complementary folded cascode amplifier". *IEEE J. Solid-State Circuits*, 29(2):130–133, Feb 1994. Cited on page 23.

[15] Hoi Lee and P. K. T. Mok. "Single-point-detection slew-rate enhancement circuits for single-stage amplifiers". In *Proc. IEEE Int. Symp. Circuits and Syst. (ISCAS)*, volume 2, pages II–831–II–834 vol.2, 2002. Cited on pages 29, 31, and 32.

[16] K. Nagaraj. "Slew rate enhancement technique for CMOS output buffers". *Electronics Letters*, 25(19):1304–1305, Sept 1989. Cited on pages 29, 33, and 34.

[17] K. Nagaraj. "CMOS amplifiers incorporating a novel slew rate enhancement technique". In *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pages 11.6/1–11.6/5, May 1990. Cited on pages 29, 30, 34, 35, and 36.

[18] R. Assaad and J. Silva-Martinez. "Enhancing general performance of folded cascode amplifier by recycling current". *Electronics Letters*, 43(23), Nov 2007. Cited on pages 29, 36, 37, and 38.

[19] Hoi Lee, P. K. T. Mok, and Ka Nang Leung. "Design of low-power analog drivers based on slew-rate enhancement circuits for CMOS low-dropout regulators". *IEEE Trans. Circuits Syst. II*, 52(9):563–567, Sept 2005. Cited on page 30.

[20] M. Rezaei, E. Zhian-Tabasy, and S. J. Ashtiani. "Slew rate enhancement method for folded-cascode amplifiers". *Electronics Letters*, 44(21):1226–1228, October 2008. Cited on page 30.

[21] S. Bu, H. W. Tse, K. N. Leung, J. Guo, and M. Ho. "Gain and slew rate enhancement for amplifiers through current starving and feeding". In *2015*

IEEE Int. Symp. Circuits and Syst. (ISCAS), pages 2073–2076, May 2015. Cited on page 30.

[22] C. Cai and D. Chen. "A slew-rate enhancement technique for fully differential amplifier without inducing trojan state". In *IEEE Int. Midwest Symp. Circuits and Syst. (MWSCAS)*, pages 1–4, Aug 2015. Cited on page 30.

[23] R. S. Assaad and J. Silva-Martinez. "The recycling folded cascode: A general enhancement of the folded cascode amplifier". *IEEE J. Solid-State Circuits*, 44(9):2535–2542, Sept 2009. Cited on pages 36, 37, 38, and 63.

[24] M. Ahmed, I. Shah, F. Tang, and A. Bermak. "An improved recycling folded cascode amplifier with gain boosting and phase margin enhancement". In *2015 IEEE Int. Symp. Circuits and Syst. (ISCAS)*, pages 2473–2476, May 2015. Cited on page 36.

[25] M. Akbari. "Single-stage fully recycling folded cascode OTA for switched capacitor circuits". *Electronics Letters*, 51(13):977–979, 2015. Cited on page 36.

[26] S. Cerida, E. Raygada, C. Silva, and M. Monge. "A low-noise fully differential recycling folded cascode neural amplifier". In *2015 IEEE 6th Latin American Symp. Circuit Syst. (LASCAS)*, pages 1–4, Feb 2015. Cited on page 36.

[27] K. H. Mak and K. N. Leung. "A signal- and transient-current boosting amplifier for large capacitive load applications". *IEEE Trans. Circuits Syst. I*, 61(10):2777–2785, Oct 2014. Cited on page 68.

[28] K. H. Mak, M. Ho, K. N. Leung, and W. L. Goh. "Design considerations of STCB OTA in CMOS 65 nm with large capacitive loads". In *IEEE Int. Symp. Circuits and Syst. (ISCAS)*, pages 2465–2468, May 2015. Not cited.

[29] K. H. Mak, M. W. Lau, J. Guo, T. W. Mui, M. Ho, W. L. Goh, and K. N. Leung. "A 0.7 V 24 μA hybrid OTA driving 15 nF capacitive load with 1.46 MHz GBW". *IEEE J. Solid-State Circuits*, 50(11):2750–2757, Nov 2015. Cited on page 68.

Appendix

A

Appendix

This appendix will present the questions and answers from the opposition of this thesis. The question together with answers is provided in A.1.

A.1 Opposition Questions and Answers

The following questions was provided by the opponent

- Q1: What criteria do you adopt to choose the references? For example, are they chosen for the reason of good performance or most cited?

  A1: When doing the literature survey I looked for papers and articles related to settling time reduction and slew rate enhancement. I chose the papers that proposed promising results, and was fairly easy to implement and evaluate. (Answered at page 3 in Section 1.4)

- Q2: Is there any other important specifications than the settling time?

  A2: Yes, there is a lot of important performance parameters when designing an amplifier. During this thesis I have focused on the parameters that affects the settling time of the opamp, such as unity-gain frequency, DC gain and slew rate. While improving these parameters I needed to avoid large degradation of other parameters, such as power consumption and input offset etc. By consistently getting feedback from my supervisor, I knew that the degradation of other performance parameters were still within acceptable ranges. (Answered in Chapter 2)

- Q3: On page 42 in Section 6.1, why do you model the load as RC? What about the bond wires in the package?

A3: When starting this thesis I was given an already designed amplifier together with a testbench. In this testbench, the inductance from the bond wire was not modeled. I realized that after ten weeks into the thesis work. Instead of re-simulate all structures, I kept the original testbench throughout my work to have the same simulation conditions for all structures. I did add the inductance for the RFC-SRE3 implementation after my work was done, and I did not see any major changes in performance of the amplifier. (Answered at page 46 in Section 5.3.2)

- Q4: On page 42 in Section 6.1.1, how is the bias voltages and currents provided to the amplifier?

  A4: The biasing network was not studied in detail in this work, hence not explained in detail. In short, the biasing network provides the bias voltages from two reference currents together with current mirrors. (Answered at page 40 in Section 5.1.1)

- Q5: On page 42 in Section 6.1.1, why do you define the error band to be 0.1 % of the input step size?

  A5: The error band specification was used in the given amplifier simulation setup and was provided by the supervisor. I kept this specification in order to compare the simulation results from the new structures with the original design. (Answered at page 41 in Section 5.1.1)

- Q6: What is the strategy behind the "worst-worst" simulation method of the project? Why did you use this strategy for all the simulation and result evaluations?

  A6: I order to ensure a certain settling time performance of the amplifier after chip manufacturing, the worst-case scenarios were considered. This was also a specification provided by the company and the supervisor. (Answered at page 49 in Chapter 6)

- Q7: On page 55 in Table 7.3, you simulate the SRE1 structure and got a settling time over 3000 ns, which is far deviated from the settling time result for a nominal condition. Why did the settling time deviate that much?

  A7: My conclusions why the settling time "exploded" for some PVT conditions, is that the intermediate node where the SRE1 senses a large-signal transient is really sensitive to PVT variations and the signal swing at that node is really low. Due to this, it is difficult to size the different transistors in order to push them in to correct regions during slewing conditions. It also depends on a stable bias voltage provided to the circuit, which in this case also could cause problems. In such cases, when the settling time exceeded over 3000 ns, oscillations were seen at the output node, before it settled. (Answered at page 55 in Section 6.2)

- Q8: In Chapter 7, you list the phase margins as one of the performance parameters. How can you define a good phase margin of the amplifier?

  A8: It is difficult to define the optimal phase margin. For example, a 60 degree phase margin can be better than a 90 degree phase margin, considering the settling time performance of the amplifier. I list the phase margin in the simulation results in order to see if the amplifier had any stability issues due to its phase margin. I kept the phase margin listed in the simulation results to give the reader a full overview of the performance parameters. (Answered at page 12 in Section 2.2.6)

- Q9: In Chapter 4, you claim that the SREs can be optimized to improve speed and conserve area. How much area did the SREs take up in the whole circuit?

  A9: I did not do the layout for the different structures, hence I did not provide any numbers on area. By doing an area size estimation in the Cadence Virtuoso software, the SRE3 technique consumed the most area. From the estimation, the implementation of the SRE3 technique increased the total area by 18 %, which was considered area-efficient for the settling time reduction achieved. (Answered at page 66 in Section 6.7)

- Q10: On page 66 you show the power consumption. How power efficient are the SREs?

  A10: The total increase of power consumption by implementing the RFC-SRE3 structure is approximately 20 %, which was considered power-efficient for a settling time reduction by almost 75 % in the Lo-Hi transition. (Answered at page 66 in Section 6.7)