

Performance Optimization of a DC-DC Converter with Series-Parallel Resonant Circuit

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Optymalizacja Parametrów Pracy Przetwornicy DC-DC z szeregowo-równoległy obwodem rezonansowym

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Abstract: The demand for high performance is constantly presenting pressure for development of more efficient power converters. The trend for smaller devices (e.g. TV sets, car battery chargers) put high constraints on physical volume of the power supply. By improving converter efficiency it is possible to save space on power components (i.e. power switches, inductors, transformers) and heat dissipation components (i.e. radiators). As traditional hard-switching solutions produce insufficient results, the attention shifts towards resonant converters. These converters by applying soft-switching techniques allow for higher efficiencies. Since the resonant converters introduce their own problems to the design, the researchers focused on developing various topologies of the resonant tanks. The development of higher order LCC, LLC and LCLC topologies helped in mitigating of some problems in designing resonant converters. Concurrently, the most popular control method for resonant converters has been the FM control. This method is easy to understand and implement, which is why it is used so widely. However, the FM control has poor efficiency at loads lower than 40%. Since many of the power supplies don't work constantly at heavy load conditions, there is a need for efficiency improvement at lower loads. The topic of resonant control methods is being researched very heavily. Many solutions have been presented in latest papers, however there is still room for improvements. The Sequential Cycle Stealing Control (SCSC) based on patented solution (PCT/EP2012/064379) has not been researched yet. Therefore, the thesis is focused of research and development of the SCSC. The method improves efficiency by introducing selective stealing of converter switching cycles. During the time when the switching impulses are generated, the ZVS conditions are ensured. During the time when switching impulses are not generated (i.e. stolen), one of the half-bridge switches stays constantly turned on, while the other is turned off. This reduces the resistance in the resonant tank and allows for longer free oscillations of the resonant tank, thus conserving energy in the converter. An important part of the SCSC is the synchronization of the first switch event (after the free oscillation period) with the current of the resonant tank. By applying such control mechanism, the power components are better utilized, which directly leads to improvement of resonant converter performance.

The thesis provides a short introduction to resonant converter topologies and covers selected state-of-the-art control methods. The focus is then directed at design considerations for SCSC dedicated to LCLC resonant converter. The step response of LCLC resonant tank is analyzed and a practical implementation of SCS controller is presented. The resulting physical model is then verified by measurements.

Optymalizacja parametrów pracy przetwornicy DC-DC z szeregowo-równoległym obwodem rezonansowym

Mgr inż. Rafał Widórek

Streszczenie: Zapotrzebowanie na przetwornice mocy o wysokiej sprawności ciągle wzrasta. Trend ciągłej miniaturyzacji urządzeń użytkowych sprawia, że dostępne miejsce dla zasilacza jest stopniowo ograniczane. Zwiększenie sprawności energetycznej zasilacza umożliwia użycie mniejszych elementów mocy (np. tranzystory mocy, indukcyjności, dławiki, transformatory) oraz mniejszych radiatorów. Mając na uwadze rosnące ceny energii elektrycznej poprawa sprawności energetycznej zasilacza o 1% kosztem jego wyższej ceny staje się coraz bardziej atrakcyjnym rozwiązaniem, gdyż inwestycja ta jest w stanie się zwrócić po roku ciągłego użytkowania urządzenia. Tradycyjne rozwiązania stosujące twarde przełączanie coraz częściej nie są w stanie dać satysfakcjonujących wyników, dlatego zainteresowanie kieruje się w stronę rezonansowych przetwornic energii. Poprzez wykorzystanie technik miękkiego przełączania, rezonansowe przetwornice są w stanie osiągać wyższe sprawności. Z powodu występowania problemów związanych z rezonansowymi przetwornicami, ostatnie badania skupiały się na opracowaniu nowych topologii obwodów rezonansowych oraz metod ich projektowania. Opracowanie topologii wyższych rzędów takich jak LCC, LLC czy LCLC rozwiązało niektóre wady przetwornic rezonansowych. Równolegle, jedną z najbardziej rozpowszechnionych metod sterowania przetwornicami jest modulacja częstotliwości (FM). Metoda ta jest relatywnie łatwa w analizie i implementacji i dlatego jest szeroko stosowana. Niestety, sterowanie FM charakteryzuje się słabą sprawnością dla obciążeń poniżej 40%. Potrzeba poprawy sprawności w tym zakresie wynika bezpośrednio z faktu, że zasilacz rzadko pracuje pod ciągłym pełnym obciążeniem. Tematyka sterowania rezonansowymi przetwornicami jest zatem bardzo atrakcyjnym polem do badań naukowych. Wiele rozwiązań opublikowanych w ostatnich latach pokazuje, że temat ten nie został przebadany wystarczająco dokładnie. Jedno z ostatnich rozwiązań – Sequential Cycle Stealing (SCS) – bazujące na patentie PCT/EP2012/064379 nie zostało jeszcze przebadane. W związku z tym faktem, niniejsza dysertacja skupia się na zbadaniu właściwości i opracowaniu pierwszej wersji kontrolera SCS. Opisywana metoda polepsza sprawność energetyczną poprzez selektywne wygaszanie impulsów sterujących kluczami. W czasie kiedy脉sy sterujące są generowane, kontroler zapewnia warunki przełączania z zerowym napięciem. Natomiast, w czasie wygaszenia impulsów sterujących jeden z kluczy (w przypadku półmostka) pozostaje włączony w celu umożliwienia swobodnych oscylacji obwodu rezonansowego. Zmniejsza to rezystancję szeregową widzaną przez obwód rezonansowy i pozwala na wydłużenie czasu swobodnych oscylacji, co bezpośrednio przekłada się na zmniejszenie strat mocy w przetwornicy. Ważnym elementem kontrolera SCS jest właściwa synchronizacja pierwszego impulsu sterującego z prądem rezonansowym, po okresie wygaszenia. Stosując wyżej opisaną metodę, wykorzystanie elementów mocy przetwornicy jest wydajniejsze, co bezpośrednio przekłada się na poprawę parametrów przetwornicy.

Dysertacja zawiera wprowadzenie w tematykę rezonansowych przetwornic oraz opisuje wybrane najnowsze osiągnięcia w dziedzinie sterowania przetwornicami rezonansowymi. Następnie opisane są problemy związane z implementacją sterowania SCS dedykowanego dla obwodu rezonansowego LCLC. Po analizie teoretycznej skokowej odpowiedzi obwodu rezonansowego opisana jest propozycja implementacji kontrolera SCS. Otrzymany model fizyczny jest następnie weryfikowany poprzez

pomiary podstawowych parametrów zasilacza takich jak: stabilność napięcia wyjściowego, sprawność, odpowiedź na skokową zmianę obciążenia oraz zaburzenia przewodzone. Wyniki opisywanej metody sterowania SCS są porównywane z wynikami otrzymanymi przy zastosowaniu klasycznego sterowania FM.

List of Symbols

α	Steinmetz equation frequency coefficient
β	Steinmetz equation magnetic flux density coefficient
ϕ	phase shift between two bridge legs
μ_0	magnetic permeability of free space
ψ	phase shift between resonant current and fundamental component of input voltage
A	coil cross section area
B_{pk}	peak magnetic flux density
C_B	blocking capacitor
C_f	output filter capacitance
C_{GD}	transistor parasitic capacitance between gate and drain
C_P	resonant tank parallel capacitance
C_S	resonant tank series capacitance
D	duty cycle
f_o	resonant tank corner frequency
f_{op}	operating frequency
Δf_{op}	operating frequency deviation
f_r	load dependent resonant frequency
i, i_r	resonant current
$i(s)$	laplace transform for resonant current
I_{COUT}	output capacitor current
I_{load}	load output current
I_m	rectifier current fundamental component amplitude
K	Steinmetz equation material losses coefficient
K_1, K_2, K_3	PID transposed form coefficient
K_D	PID derivative coefficient
K_I	PID integral coefficient

K_p	PID proportional coefficient
L_f	output filter inductance
L_p	resonant tank parallel inductance
L_{prim}	primary winding inductance
L_{Qlimit}	quality limiter winding inductance
L_s	resonant tank series inductance
L_{sec}	secondary winding inductance
l_e	effective coil magnetic path length
n	transformer turn ratio
N	number of coil turns
P_{loss}	converter power losses
Q_L	resonant tank loaded quality factor
R_L	load resistance
R_{ON}, R_{DSON}	transistor channel resistance in ON state
T_{samp}	sampling period
V_{AB}	rectifier filter input voltage
V_{DS}	transistor drain source voltage
V_e	ferrite core effective volume
V_m	half-bridge voltage fundamental component amplitude
V_{out}	output voltage
V_{out_high}	output voltage high threshold
V_{out_low}	output voltage low threshold
V_R	rectifier voltage fundamental component
V_{Rm}	rectifier voltage fundamental component amplitude
$x_{RMS}[n]$	RMS value of a discrete signal

List of Acronyms

AD	Analog to Digital
APWM	Asymmetrical Pulse Width Modulation
BJT	Bipolar Junction Transistor
CRMS	Cyclic Root Mean Square
DC	Direct Current
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FM	Frequency Modulation
FMC	Frequency Modulation Control
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
LED	Light Emitting Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PDM	Pulse Density Modulation
PFC	Power Factor Correction
PID	Proportional-Integral-Derivative
PLL	Phase Locked Loop
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
RMS	Root Mean Square
SCS	Sequential Cycle Stealing
SCSC	Sequential Cycle Stealing Control
SMPS	Switch-Mode Power Supply
SPS	Sample per Second
SSOC	Self-Sustained Oscillation Control

ZCS

Zero Current Switching

ZVS

Zero Voltage Switching

1 Introduction

Almost all of the electric devices used nowadays need some sort of power converter for proper operation. The applications can range from consumer electronics (e.g. TV set power supplies, laptop power supplies, battery chargers) through lighting (e.g. LED lamps) to automotive (e.g. electric car battery chargers). All of these fields present a demand for better performance power converters. Higher efficiency, smaller volume, less weight, better reliability, strict EMC compliance are only several of the requirements put on a power converter design. The traditional hard-switching topologies (e.g. buck, push-pull, flyback) have limited performance due to excessive switching losses. Recent developments [1],[2],[3] try to reduce these switching by introducing quasi-resonant topologies where some degree of soft-switching can be employed. While these techniques improve the performance of hard switching converters, even better results can be achieved by employing the resonant converters. The simplest topologies for the resonant converters, i.e. series LC or parallel LC resonant converters, suffer from many drawbacks, such as wide frequency variation for the whole load range or failure at load short-circuit or open-circuit respectively. The most widely applied resonant topology is the LLC series resonant converter. While it improves the performance over the LC series resonant converter it is still prone to failure at load short-circuit. This is where the LCLC series-parallel resonant converter improves over the former. Having an embedded load short-circuit protection with self output current limiting is a desired feature in many applications. However, the LCLC series-parallel converter suffers from relatively poor efficiency at light loads. This is where an idea for changing the control method appeared. The Frequency Modulation (FM) has poor efficiency at light loads and produces high amplitude narrow EMI spikes. Additionally, the LCLC series-parallel converter can be improved with magnetic component integration techniques [4], [5], [6].

The topic of the thesis “Performance optimization of a DC-DC converter with series-parallel resonant circuit” contains theoretical analysis, state-of-art in resonant converter control methods analysis, followed by design and implementation of novel control method, Sequential Cycle Stealing (SCS), that ensures proper conditions for ZVS switching in all operating conditions. Additionally, in order to improve the energy conversion efficiency in light load conditions, the proposed method introduces selective stealing of converter switching cycles. The proposed solution shall improve resonant converter performance and reduce its size. The innovation of the thesis is the application of unique control algorithms, dedicated to resonant converters, based on selective stealing of the switching cycles on following manner. During the time when the switching impulses are generated, the ZVS conditions are ensured. During the time when switching impulses are not generated (i.e. stolen), one of the half-bridge switches stays constantly turned on, while the other is turned off. This reduces the resistance in the resonant tank and allows for longer free oscillations of the resonant tank, thus conserving energy in the converter. An important part of the SCSC is the synchronization of the first switch event (after the free oscillation period) with the current of the resonant tank. By applying such control mechanism, the power components are better utilized, which directly leads to improvement of resonant converter performance. The SCSC described above is based on control method presented in [7] and [8] owned by AGH University of Science and Technology. The research has been conducted as a part of grant 65010 – “Innowacyjny zasilacz rezonansowy dużej mocy do pojazdów hybrydowych i elektrycznych” directed by Sławomir Ligenza from Fideltronik Poland Sp. z o.o.. The research part of the project has been conducted by the author at AGH University of Science

and Technology, while the development part has taken place at Fideltronik Poland Sp. z o.o.. It should be stated that the author is both a student at AGH UST and an employee of Fideltronik Poland Sp. z o.o..

The scope of the thesis goes along worldwide research of DC-DC resonant power converters and resonant converters control methods. Aside from theoretical aspects, the presented method has high potential in application in modern DC-DC converters.

Therefore, the thesis has three objectives to fulfill:

- The proposed control method dedicated to resonant converters, based on sequential stealing of switching cycles shall improve converter energy efficiency
- The proposed control algorithm shall allow for better integration of converter functional blocks
- The SCSC applied to resonant converter shall reduce the conducted EMI emission

The dissertation is organized with eight chapters, with the first (and current) being the introduction. Chapters two and three will give the state of the art in resonant converters and resonant converter control methods. Chapter four will present the concept of the novel SCSC method. The test platform is described in chapter five followed by the description of the digital implementations of FM Control and SCSC in chapter six. The measurement results are presented in chapter seven and the dissertation concludes in chapter eight.

2 Topologies for DC-DC Resonant Power Converters

In the last couple of years the electronics industry experienced a rapid development in power electronics applications such as LED lamps power supplies (30W-1000W), battery chargers (500W – 5000W), electric motor drive systems and many more. High efficiency, lightweight, small size and low price have always been the parameters with a constant demand for improvement. In an increasing number of applications the performance of classic hard-switching converters is insufficient. Although the resonant energy conversion technique has been known since 1959 [9], it has been mainly used in specific types of applications (e.g. solid-state electronic ballasts for fluorescent lamps or high frequency inductive heating). Nowadays, the resonant converters are applied in wider areas.

In this chapter the most common resonant topologies will be discussed. Subchapter 2.1 will focus on resonant inverter topologies, followed by a brief description of most common failure causes in resonant converters in subchapter 2.2. Finally, an introduction of basic rectifier circuits will be presented in subchapter 2.3.

2.1 Resonant inverter topologies

There are several classifications for the resonant inverter topologies. The author has decided to use the element count as the main feature. Thus, there can be two element topologies (2nd order), three element topologies (3rd order), four element topologies (4th order) and higher [10]. A short description of 2nd order series loaded, 2nd order parallel loaded, 3rd order LCC, 3rd order LLC and 4th order LCLC inverters will be given in the following sections.

2.1.1 LC series loaded inverter

The circuit for the class D voltage switching series loaded resonant inverter for both half-bridge and full-bridge configurations is presented in Fig. 2.1.

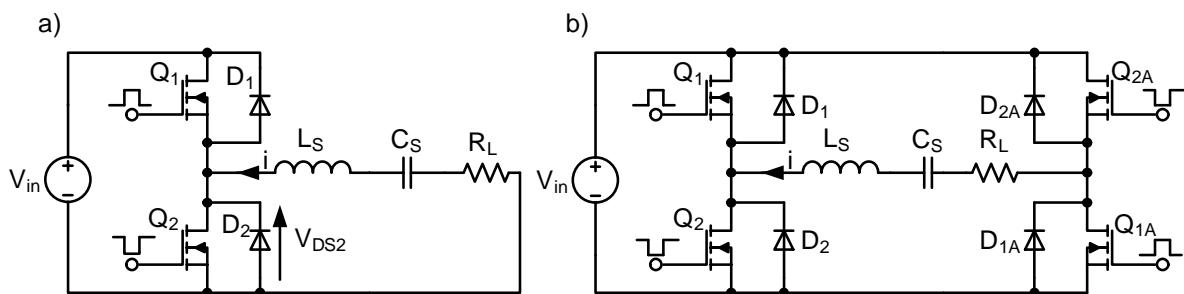


Fig. 2.1 Class D voltage switching series resonant circuit. a) Half-bridge configuration, b) Full-bridge configuration

The following analysis will be performed only for half-bridge configuration, since the behavior of the full-bridge configuration is analogous. The resonant circuit, formed by inductor L_s and capacitor C_s connected in series, is driven by a rectangular waveform, created by two bidirectional switches (Q_1, D_1 and Q_2, D_2). The load, represented by resistor R_L , is connected in series with the resonant circuit. The switches are driven by rectangular waveforms with a dead time, that usually has a fixed value.

Fig. 2.2 presents waveforms that show the operation of the resonant inverter at various switching frequencies. A square wave voltage (V_{DS2}) is driving the series resonant circuit. Assuming that the load resistance isn't too high (the quality factor is high enough), the half-bridge output current i can be approximated with a sine wave. At the resonant frequency equal to:

$$f = f_0 = \frac{1}{2\pi\sqrt{L_S C_S}}$$

the half-bridge output current is in phase with the half-bridge output voltage. In such conditions, the transistors switch at zero current which results in zero switching losses. However, many applications use varying operational frequency to control output parameters (e.g. output voltage). This can result in operation either below or above the operating frequency.

For $f < f_0$ the series resonant circuit is seen as a capacitive load for the half-bridge. In such a condition the current i flowing through the resonant circuit is ahead in phase of the fundamental component of the V_{DS2} voltage by the phase ψ , where $\psi < 0$. Because of this, the current in the switch, at instant just after turn on, is positive and is negative just before the turn off. The conduction sequence is as follows. Consider that switch Q1 is *ON* and conducts positive current. Q1 is then being turned off after a certain time after the current goes negative. At this time the anti-parallel diode D1 starts to conduct, because the switch Q2 is still turned off. When the switch Q2 is turned on, the voltage V_{DS2} starts to decrease, causing the voltage across Q1 (V_{DS1}) to increase. This turns the diode D1 off and diverts the current to Q2. The cycle finishes when Q2 turns off at negative current and the current i starts to flow through D2. A new cycle begins when Q1 turns on.

In operation below resonant frequency some undesired effects occur at turn on of each transistor. The first one is the reverse recovery of the anti-parallel diode of the opposite switch. Suppose we are in a state when Q1 is turned off and D1 conducts the current i . When transistor Q2 turns on the voltage on the D1 changes its polarity and starts to turn off the diode. However, the diode D1 turns off at high di/dt which will create a large reverse recovery current spike. This current spike will flow through the bottom transistor (which has just turned on), because the inductor in the series resonant circuit won't allow rapid current changes. These current spikes put transistors under severe stress, which can lead to transistor destruction. A second detrimental effect at transistor turn on is the discharge of the transistor output capacitance (and in class DE converters, the additional switch capacitance), which further increases the current spike. This effect occurs because the transistors are turned on at high V_{DS} voltage, which is equal to V_{IN} . Another effect to consider is the Miller's effect. Because the V_{GS} increases while the V_{DS} decreases, the transistor behaves like an inverting amplifier. Therefore, the C_{GD} will increase the transistor input capacitance significantly, which will require a higher power to drive the gate. The effects described above suggest that in applications using MOSFETs operation below resonance should be avoided.

The last region to cover is the operation above the resonant frequency. For $f > f_0$ the series resonant circuit represents an inductive load for the half-bridge. The current i flowing through the resonant circuit lags in phase with the fundamental component of the V_{DS2} voltage by the phase ψ , where $\psi > 0$. Prior to switch turn on the current flowing through a switch is negative, whereas before turn off it is positive. The current conduction sequence is as follows. Let's assume the transistor Q1 is already conducting a positive current. After the gate drive turns the transistor off, the current diverts to the bottom diode D2. The voltage V_{DS2} starts to decrease up to the value when it reaches the value

of the D2 diode forward voltage bias. Next, the transistor Q2 turns on while the current still flows through the diode D2 (i.e. the switch S2 current is negative).

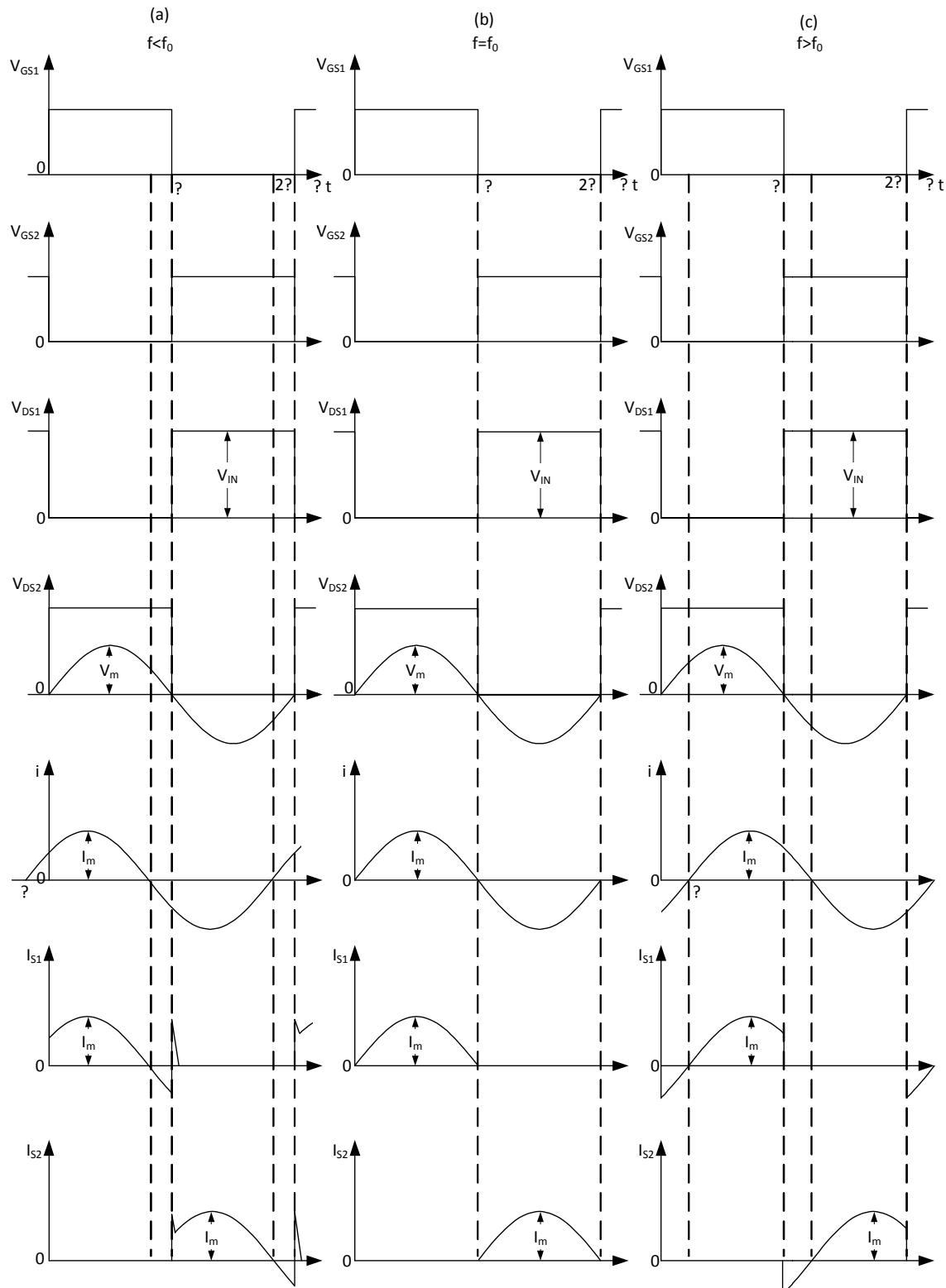


Fig. 2.2 Waveforms in half-bridge series resonant inverter for different frequencies. (a) Operation below resonance. (b) Operation at resonant frequency. (c) Operation above resonance.[10]

When Q2 turns on the resonant current i diverts to Q2 from D2. The transistor Q2 will turn off when it is still conducting positive current. After the turn off, the current is diverted to diode D1 and the voltage V_{DS2} rises to a value slightly less than the input supply voltage. A new cycle starts when the transistor Q1 turns on, while the current i was still flowing through the diode D1.

As can be seen, the transistors are turned on at nearly zero voltage (which is equal to the diode forward voltage drop). Because the V_{DS} voltage is close to zero, the Miller's effect is absent and the input capacitance is not increased. This leads to nearly zero losses at turn on for the transistors. For $f > f_0$ the turn on losses is nearly zero, but there is a turn off loss in the transistor. Both the transistor voltage and transistor current overlap during turn off, resulting in switch loss.

The behavior of the LC resonant circuit to the load change will be discussed. If the load increases towards infinity, i.e. open circuit, the resonant current i decreases to zero, which can lead to loss of zero-voltage switching and possibly can lead to damaging the switch.

On the other hand, the circuit behaves well under short circuit or near short circuit conditions. The loaded quality factor is high and the current i is nearly sinusoidal. However, care must be taken not to allow the operating frequency to go too close to the resonant frequency, because in this condition the current i will be only limited by parasitic resistances of the L_s , C_s and R_{on} of the switches. Because the quality factor is high, the resulting high amplitudes of current and voltages can lead to damaging either the switches or one of the resonant circuit components.

2.1.2 Half-bridge parallel loaded resonant converter

Fig. 2.3 shows the circuit for class D parallel loaded resonant inverter. The resonant circuit is created by L_p and C_p . A large capacitor C_B is inserted in series with R_L to prevent DC current from flowing to the load. The average voltage on C_B is $V_{IN}/2$. The two switches S_1 and S_2 create a voltage square wave that drives the parallel resonant circuit. In *ON* state the switches can conduct both positive and negative currents, while in *OFF* state the switches can only conduct negative current. Both switches are driven by non-overlapping voltage square waves i.e. the duty cycle is less than 50%.

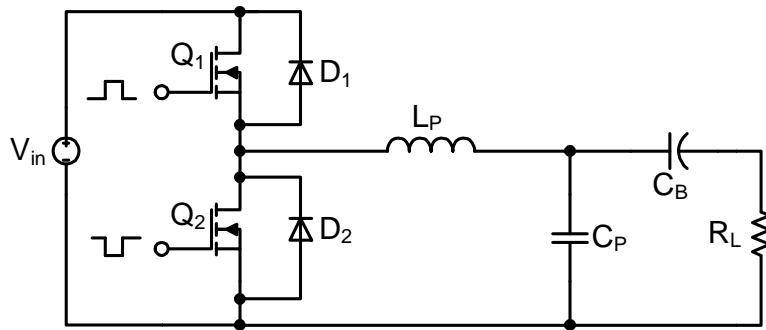


Fig. 2.3 Class D voltage switching half-bridge parallel resonant circuit

The resonant frequency equals to:

$$f_r = \frac{1}{2\pi\sqrt{L_p C_p}}.$$

Fig. 2.4 shows the current and voltage waveforms for different operating frequencies, with the assumption that the loaded quality factor is sufficiently high (e.g. $Q_L > 2.5$).

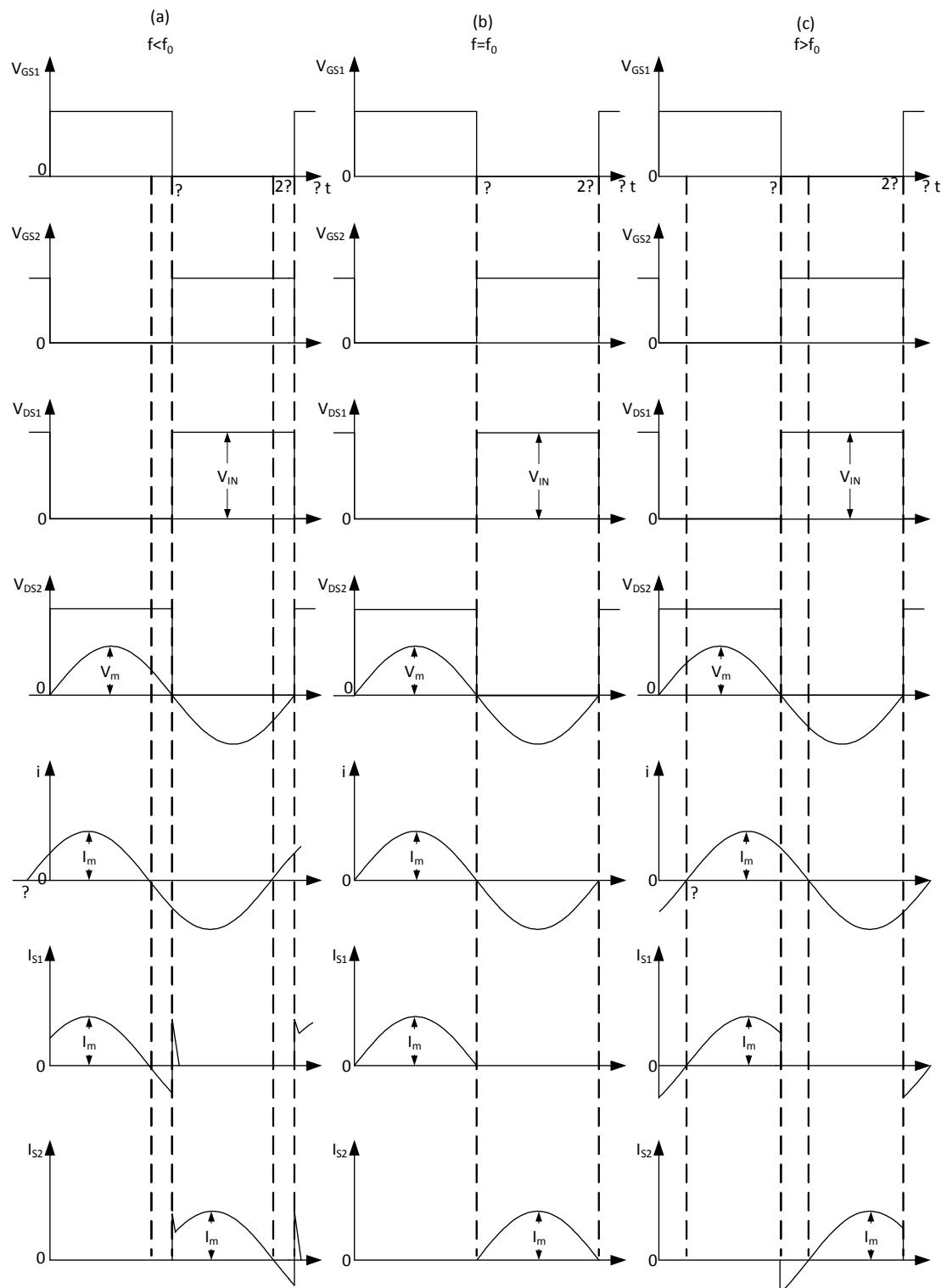


Fig. 2.4 Waveforms in half-bridge parallel resonant inverter for different frequencies. (a) Operation below resonance. (b) Operation at resonant frequency. (c) Operation above resonance.[10]

For the operating frequency $f < f_r$, the parallel resonant circuit represents a capacitive load and the phase shift between the inductor current i and the fundamental component of the voltage V_{DS2} is negative ($\psi < 0$). This mode of operation is not recommended for the same reasons described in series resonant inverter.

For $f > f_r$, the phase shift is positive ($\psi > 0$) and the resonant circuit represents an inductive load to the half-bridge. The inductor current i lags behind the fundamental component of the voltage V_{DS2} . The switches turn on while they conduct negative current and turn off when they conduct positive current. The switching sequence is as follows. Consider that the switch S_1 is conducting positive current. When the transistor Q1 turns off the voltage V_{DS1} starts to increase. This causes voltage V_{DS2} to decrease until it reaches a negative voltage sufficiently high to turn on the diode D2. The current diverts from Q1 to D2. The transistor Q2 is being turned on while the diode D2 is still conducting current (i.e. the switch S2 is conducting negative current). The current then diverts to Q2. The turn off of the transistor Q2 is analogous to the turn off of the Q1. The transistors are turned on at low V_{DS} voltage, making the turn on losses negligible. At turn off both the transistor voltage and transistor current overlap resulting in switch loss. As can be seen, the switching sequence is exactly the same as in LC series resonant converter.

The LC parallel resonant circuit load change behavior differs to series resonant circuit load change behavior. When the output resistance is decreasing towards short circuit the capacitors C_p and C_b are connected in parallel. The current in C_p is zero because $C_p \ll C_b$. The switches are loaded by the inductor L_p which limits the short circuit current (unless the inductor saturates). When the load is close to infinity the loaded quality factor is very high and the voltage across the capacitor and the inductor are sinusoidal. As the operating frequency approaches the resonant frequency, the inductor current and capacitor voltage can reach very high values, which can lead to inductor or capacitor failure because of excessive stress.

2.1.3 Half-bridge series resonant LCC converter

In previous subchapters series and parallel loaded resonant inverters have been discussed. The series-parallel resonant inverter is a hybrid between the series loaded resonant inverter and parallel loaded resonant inverter [11], [10], [12], [13]. The idea is to split the resonant capacitance into two separate capacitors. The load is connected to one of these capacitors. Fig. 2.5 presents the circuit for the class D half-bridge series resonant inverter. The resonant circuit is formed by the elements L , C_1 , C_2 , R_L . The capacitor C_1 is connected in series with inductor L , while capacitor C_2 is connected in parallel with load resistor R_L . The switches S_1 and S_2 can conduct both positive and negative currents in *ON* state and only negative current in *OFF* state. The resonant circuit is driven by a square wave voltage created by the half-bridge. The switches are driven by voltage square waves with a duty cycle less than 50%, to prevent cross conduction.

If the capacitor C_1 becomes very large the circuit will transform into parallel loaded resonant inverter. Likewise, if the capacitor C_2 is removed ($C_2 = 0$) the circuit transforms into series loaded resonant inverter.

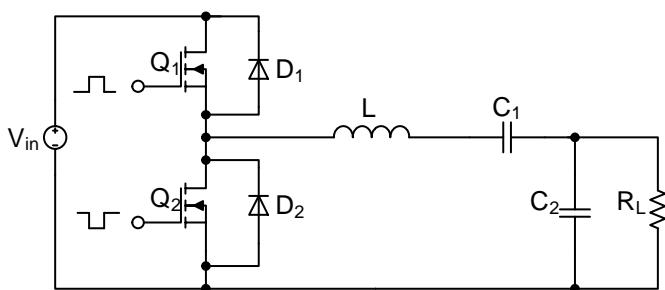


Fig. 2.5 Class D voltage switching half-bridge series-parallel LCC resonant circuit.

When the load resistance approaches zero, the capacitor C_2 is short circuited. The resonant circuit consists of L and C_1 that form a series resonant circuit. As long as the switching frequency is far enough from resonant frequency of the $L-C_1$ circuit, the converter will operate under safe conditions. Otherwise, the high voltages and currents at the $L-C_1$ resonant frequency may damage the circuit. Similarly, when load resistance increases towards infinity, the resonant circuit forms a unloaded parallel resonant circuit, where series connection of C_1 and C_2 forms the resonant capacitance. The resonant frequency is equal to the corner frequency

$$f_0 = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi} \sqrt{\frac{C_1 + C_2}{LC_1C_2}}$$

Operation at light loads ($R_L \rightarrow \infty$) at f_0 leads to excessive voltages and currents in the resonant circuit that may cause a malfunction. An example of LCC resonant tank impedance plot vs frequency is presented in Fig. 2.6.

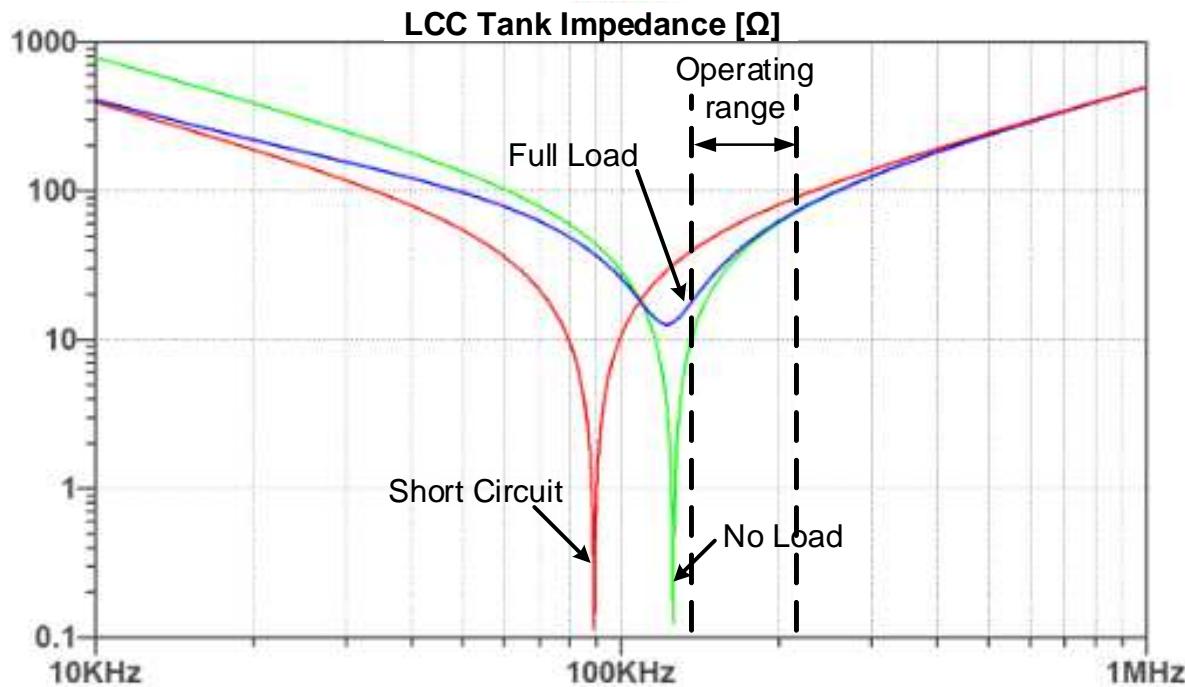


Fig. 2.6 Example of LCC resonant tank impedance-vs frequency characteristics for various load conditions

2.1.4 Half-bridge series LLC converter

Currently the most commonly applied topology for resonant converters is the LLC resonant circuit. There are a few reasons for such popularity. The main advantages are: narrow frequency band to fully cover the load variation, relatively good design procedure (many commercial companies support the LLC topology [14],[15],[16]) and the possibility of integration of the two inductors into one physical component [17][18][19], [20], [21]. As it can be seen on Fig. 2.7 the load is connected in parallel to one of the inductances. In most applications a galvanic separation between input and output is desired. If we use a transformer, then its leakage and magnetizing inductance can be used to form resonant inductances. This approach is used very commonly, because it reduced the component count, thus reducing the cost of the converter. Compared to LC series circuit, the LLC topology doesn't increase the cost (assuming that the galvanic separation is necessary), but improves the converter performance.

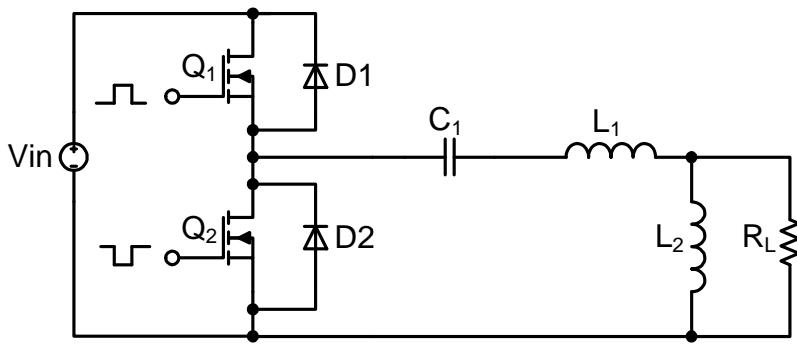


Fig. 2.7 Class D voltage switching half-bridge series LLC resonant circuit

The LLC resonant circuit has a potential disadvantage. If the load of the resonant circuit is shorted, the resonant frequency of the resonant circuit will significantly shift towards higher frequencies as can be seen on Fig. 2.8. Suppose the converter is operating at 100kHz. If a short-circuit occurs, the resonant frequency will shift to c.a. 150kHz. It means that unless the operating frequency is increased the converter can enter capacitive region operation. Additionally, the quality factor is significantly increased and even if the converter operates in inductive region, the excessive amplitudes of voltage and current can lead to critical failure of the converter if additional protection circuitry is not introduced.

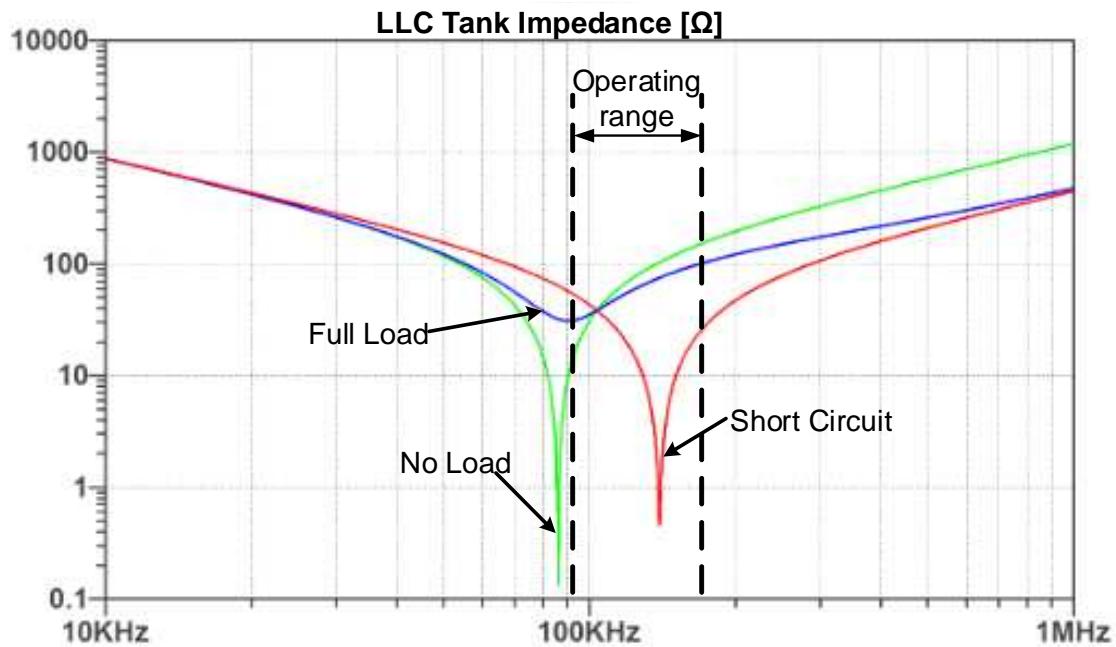


Fig. 2.8 Example of LLC resonant tank impedance-vs frequency characteristics for various load conditions

2.1.5 Half-bridge series-parallel LCLC converter

The LLC converter has one disadvantage not mentioned before. If the transformer windings have a large number of turns, the formed parasitic capacitances are added in parallel to the windings' inductance. If the transformer design is not made carefully, the parasitic capacitances will introduce additional resonant frequencies, which can lead to critical failure at certain operating conditions. This problem can be removed by the addition of a capacitor in parallel to the transformer windings, forming the LCLC resonant circuit presented in Fig. 2.9. The topology is well known, however it is difficult in design. This is the main reason for its rare applications.

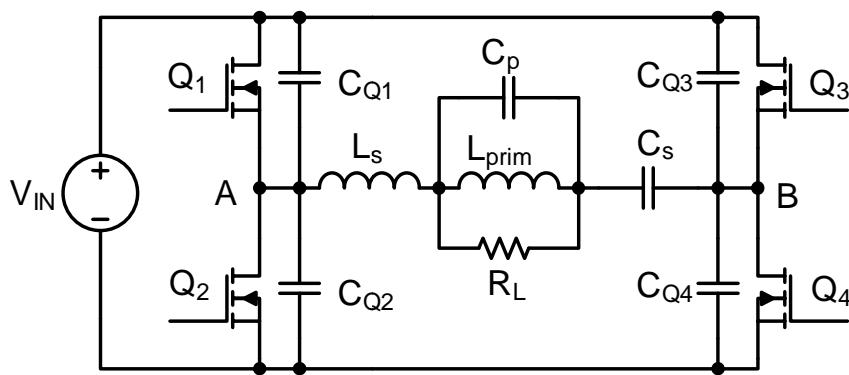


Fig. 2.9 Class DE voltage switching full-bridge series parallel LCLC resonant converter

The employed LCLC topology has several advantages [4]. If proper component values are selected, the converter will be self-protected from the load short-circuit. This is because the resonant frequency of the resonant circuit shifts towards lower frequencies when short-circuit occurs. Fig. 2.10 presents example impedance vs frequency characteristics of a LCLC resonant circuit at different load values. Suppose the converter operates at 160kHz. If short circuit suddenly occurs, we can

observe that the resonant frequency will shift to around 85kHz. The converter remains within the inductive region of operation and can operate safely.

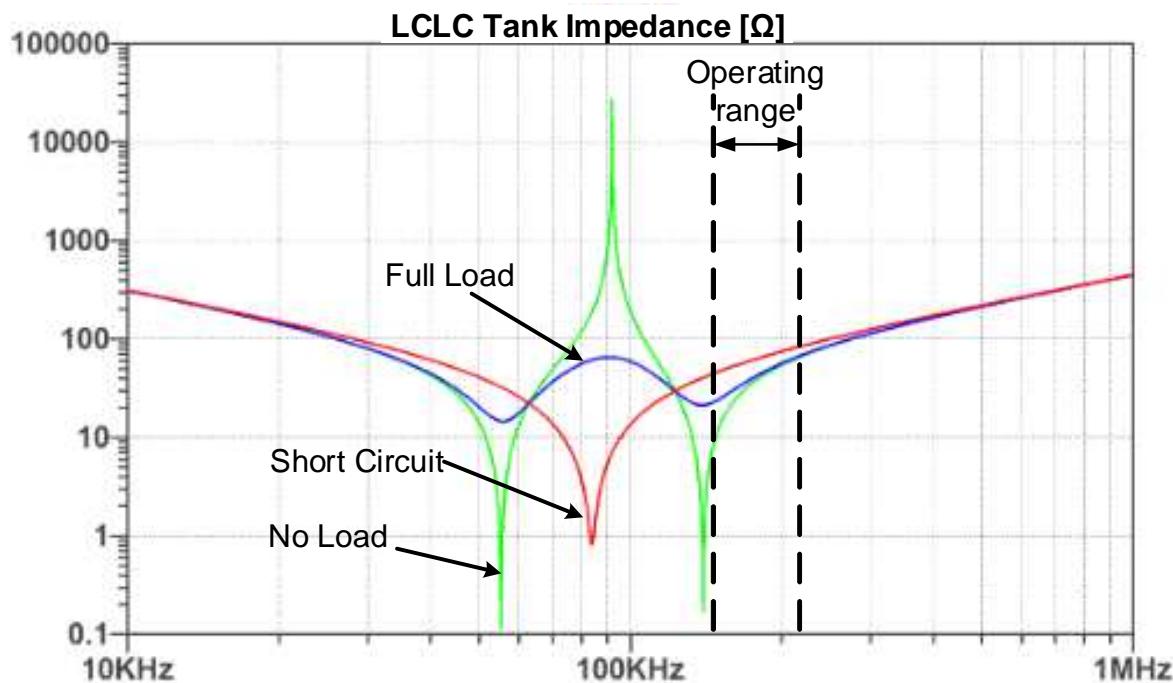


Fig. 2.10 LCLC resonant tank impedance-frequency characteristics for various load conditions

Moreover, the loaded quality factor is reduced, thus the converter will naturally limit the output current and the current in resonant circuits. An additional advantage of this topology is a narrow band for the FM to cover the whole range of the load variation (from open to short circuit). It is worth noting that there are two modes of operation for this topology. If the load resistance is higher than the maximum output power resistance (the resistance value at which the converter delivers the maximum power), the converter will regulate the desired output parameter. When the output current reaches the maximum value (induced by the resonant circuit design) it will not raise any further will stay at a constant value for load resistances below the maximum output power resistance.

2.2 Common Failure Causes in Resonant Converters

Usually the most vulnerable components in a resonant converter are the semiconductor devices (inverter and rectifier switches) and tend to fail in the first place. There are two most common mechanisms leading to failure: creation of a unwanted generator circuit and second breakdown. Should any of these phenomena occur, the switches are prone to damage in a very short time.

The generator is created by a single switch in the resonant inverter, however the second switch of the half-bridge also plays a role in this phenomenon. The generator is excited by a large current spike flowing into the drain of the MOSFET. Part of this current spike will flow into the gate through the parasitic capacitances C_{GD} of the switch. If the generation conditions are met or nearly met the transistor will start to oscillate at relatively high frequency with a high voltage applied to it. This state will inevitably destroy the switch due to exceeding the safe temperature of the device junction.

If the generator failure is not present, the high current spikes can still trigger the second breakdown mechanism. The energy from this spike can either accumulate in a single cell of the power device and lead to local thermal failure, which is followed by overall failure of the inverter, or can turn on the parasitic BJT present in the MOSFET switches yielding the same results. A more in depth analysis of this phenomenon can be found in [22], [23], [24],[25],[26]. Fig. 2.13 to Fig. 2.13 show an example of switch oscillations that will lead to component failure. Notice the degraded gate drive voltage and excessive oscillations of the V_{DS} voltage in Fig. 2.11.

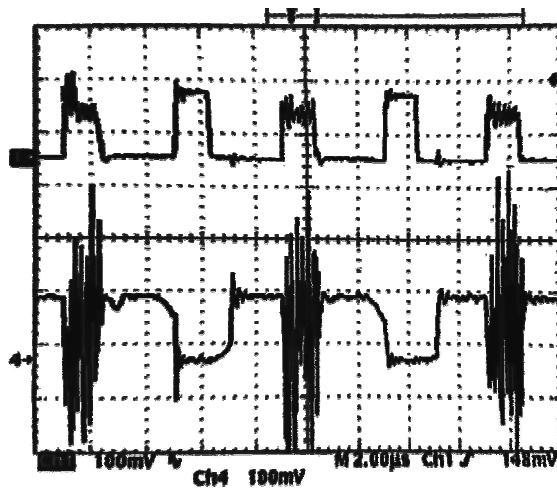


Fig. 2.11 Example of uncontrolled switch oscillations; Top waveform: gate voltage, Bottom waveform: V_{DS} voltage

Notice that the oscillations and shoot-through currents can even charge the gate and cause a turn on of the opposing switch (waveforms A and B) in Fig. 2.12.

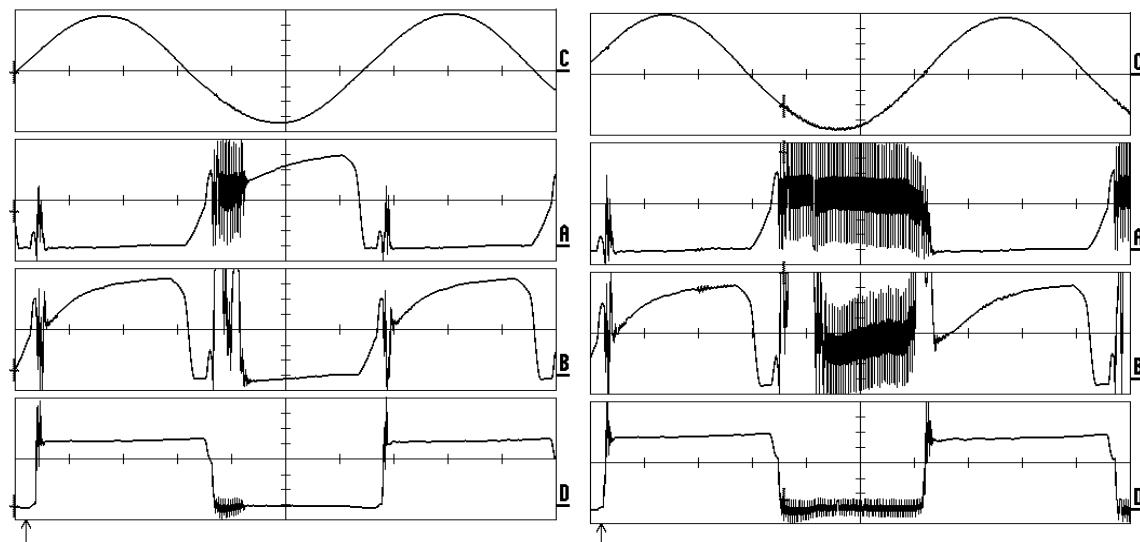


Fig. 2.12 Example of uncontrolled switch oscillations; (A,B) gate voltages, (C) resonant current, (D) V_{DS} voltage

Both, the uncontrolled oscillation and second breakdown can occur in one of the following conditions. The inverter is operating in capacitive mode or the converter is operating in the inductive region, but the energy in the resonant circuit is too small to charge/discharge the half-bridge output capacitance. Thus, when a switch turns on there are two detrimental conditions: there is still a

significant voltage across the switch and/or there is a current flow in the antiparallel diode of the opposite transistor. These two conditions will result in a very large current spike in the switch that turns on, since it has to discharge the capacitance in parallel to the switch and additionally has to turn off the diode of the opposite switch. The current spike is bigger the slower is the diode in the transistor or the larger is the total capacitance connected in parallel to the switch (i.e. transistor output capacitance or external capacitor present in class DE switching).

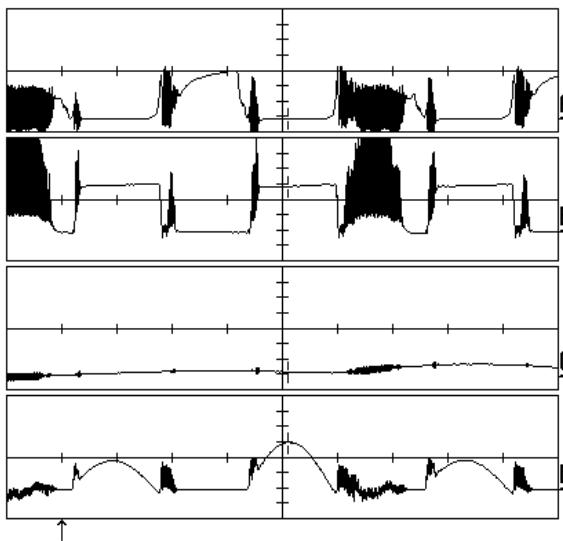


Fig. 2.13 Example of uncontrolled switch oscillations; (A) gate voltage, (B) V_{DS} voltage, (C) output current, (D) switch drain current

Other, more obvious, failure cause is exceeding the voltage and current ratings of the resonant circuit components (i.e. switches, capacitors, inductors, transformers). This failures can occur when the converter is operating in regions where the resonant tank has high quality factor (e.g. resonant frequency operation at light load)

2.3 Rectifier topologies

To create a DC-DC resonant converter a resonant inverter loaded with a high frequency rectifier is necessary. The topologies for the resonant inverters have been presented in subchapter 2.1. Here, classic topologies for voltage-driven rectifiers will be briefly discussed [10].

2.3.1 Half-wave rectifier

Fig. 2.14 presents a circuit for half-wave voltage driven rectifier. It consists of a transformer, diodes D_1 and D_2 and a second order output filter.

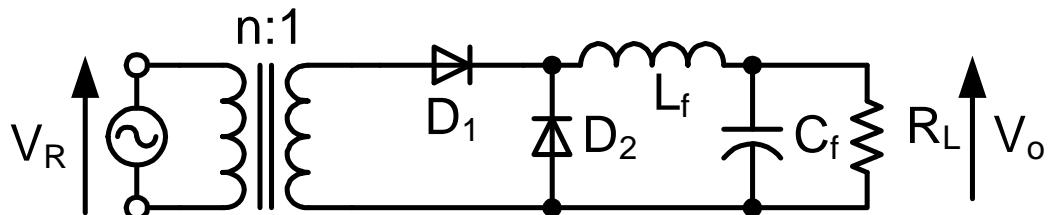


Fig. 2.14 Circuit of half-wave rectifier

The rectifier is driven by a sinusoidal voltage source. Assuming that the L_f is large enough, its ripple current is small and the inductor current is approximately equal to the output current I_o . In such conditions the output filter and the load resistance can be replaced with a current sink. Assuming the transformer is ideal, the input voltage source V_R can be reflected from the primary to the secondary side of the transformer to become V_R/n . When $V_R > 0$ the diode D_1 is on and the diode D_2 is off. When $V_R < 0$ the diode D_1 is off and the diode D_2 is on.

If the rectifier is driven by an ideal voltage source with the amplitude V_{Rm} , which is much higher than diode forward voltage drop, then the input voltage is sinusoidal can be written as:

$$V_R = V_{Rm} \sin \omega t$$

where V_{Rm} is the amplitude of V_R . The voltage at the input of the filter is $(V_{Rm} \sin \omega t)/n$ for $0 < \omega t < \pi$ and 0 for $\pi < \omega t < 2\pi$. The average voltage across the filter inductor is zero, making the voltage at the input of the filter equal to the output voltage. Thus, the output voltage can be written as:

$$V_o = \frac{1}{2\pi} \int_0^{2\pi} v_{AB} d(\omega t) = \frac{1}{2\pi} \int_0^{\pi} \frac{V_{Rm}}{n} \sin \omega t d(\omega t) = \frac{V_{Rm}}{\pi n}$$

This means, that the dc output voltage is directly proportional to the input voltage V_{Rm} . Therefore, V_o can be regulated by controlling V_{Rm} .

2.3.2 Transformer center-tapped rectifier

Fig. 2.15 shows a circuit of a transformer center tapped voltage driven rectifier. Here, we use two identical secondary windings in the transformer with rectifier diodes in series to each winding. Having two secondary windings gives us the ability to deliver energy to the output during the whole switching period. A disadvantage of this solution is that if the inductance of the two secondary windings can slightly differ between each other, which can lead to unsymmetrical load to the voltage source V_R . This will lead to non-equal current distribution between the windings and will degrade the rectifier performance. Notice that in this circuit the freewheeling diode that appeared in half wave rectifier is not necessary at all.

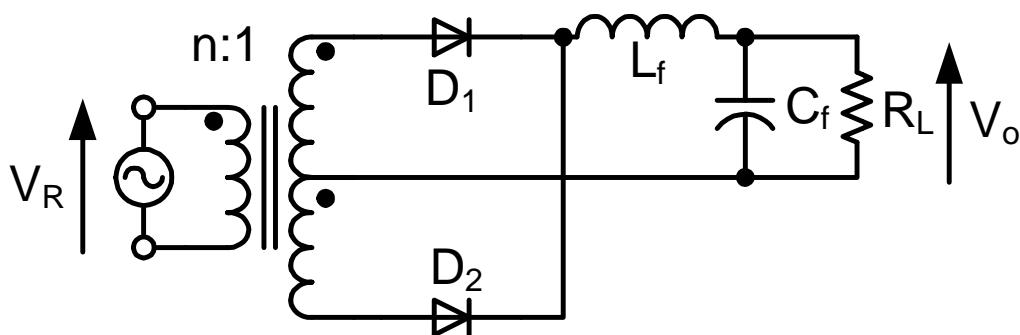


Fig. 2.15 Circuit of center-tapped rectifier

Like in half wave rectifier the average voltage across the filter inductor is zero. Thus, the dc voltage at the input of the filter is equal to the output voltage V_o , and is equal to:

$$V_o = \frac{1}{2\pi} \int_0^{2\pi} v_{AB} d(\omega t) = \frac{1}{\pi} \int_0^{\pi} v_{AB} d(\omega t) = \frac{1}{\pi} \int_0^{\pi} \frac{V_{Rm}}{n} \sin \omega t d(\omega t) = \frac{2V_{Rm}}{\pi n}$$

This means, that the dc output voltage is directly proportional to the input voltage V_{Rm} . Therefore, V_o can be regulated by controlling V_{Rm} .

2.3.3 Bridge rectifier

Fig. 2.16 presents the circuit for the bridge voltage driven rectifier. Here we use a single transformer secondary winding connected to a diode bridge. Using the rectifier bridge gives us two benefits. The energy can be delivered to the output during both halves of the switching period. Additionally, only one secondary winding is present, which simplifies the transformer design and eliminates the non-symmetrical current distribution problem present in center-tapped rectifier. However, there are two diodes in series in the conduction path, which will double the semiconductor conduction losses, resulting in lower efficiency.

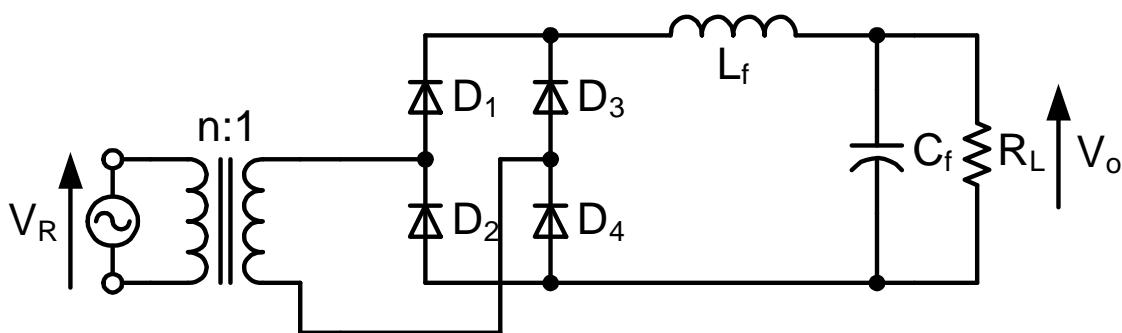


Fig. 2.16 Circuit for full bridge rectifier

Like in transformer center-tapped rectifier the average voltage across the filter inductor is zero. Thus, the dc voltage at the input of the filter is equal to the output voltage V_o and can be written as:

$$V_o = \frac{1}{2\pi} \int_0^{2\pi} v_{AB} d(\omega t) = \frac{1}{\pi} \int_0^{\pi} v_{AB} d(\omega t) = \frac{1}{\pi} \int_0^{\pi} \frac{V_{Rm}}{n} \sin \omega t d(\omega t) = \frac{2V_{Rm}}{\pi n}$$

This means, that the dc output voltage is directly proportional to the input voltage V_{Rm} . Therefore, V_o can be regulated by controlling V_{Rm} .

2.4 Summary

In the chapter most common topologies for resonant inverters and three classic topologies for voltage driven rectifiers have been introduced. The following resonant inverter topologies have been discussed: series loaded resonant inverter, parallel loaded resonant inverter, series resonant LCC and LLC inverters and series-parallel LCLC resonant inverter. The series loaded resonant inverter cannot operate safely at short circuit at the resonant frequency and has poor performance at light loads, due to high switching frequency needed for maintaining regulation. Likewise, the parallel resonant inverter cannot operate safely at light loads at the corner frequency and has poor performance at short circuit. This shows that both of these topologies have problems when the regulation must be ensured for wide load range. This problem can be solved by using more complex higher order resonant inverter topologies. Both LCC and LLC topologies improve inverter performance over the 2nd order circuits. However, the LCC topology increases the cost because of the additional resonant capacitor present in the resonant circuit, whereas the LLC topology can preserve the cost by employing integration of the resonant inductance into the transformer leakage inductance. This is one of the reasons why LLC resonant inverter is more commonly applied topology. However, the LLC resonant inverter is prone to load short-circuit failures and transformer winding parasitic capacitances can lead to unexpected behavior of the inverter. To resolve these issues, the LCLC

resonant inverter topology has been introduced. The LCLC resonant inverter topology is not sensitive to transformer winding parasitic capacitances due to external capacitor already connected parallel to transformer. Additionally, the LCLC resonant tank can be designed in such a way, that it will have intrinsic load short-circuit protection.

Next the most common failures of the resonant converters have been discussed. Not only the operation in capacitive region can destroy the inverter, but also operation with insufficient energy necessary to charge the transistor output capacitances can lead to failure of the inverter.

The chapter ends with a brief introduction to three classic voltage driven rectifier circuits. All of these circuits use a second order L_F-C_F output filter. The half wave rectifier is the simplest one (thus, is the cheapest), but also has the lowest efficiency. The transformer center-tapped has the highest efficiency, but has two transformer secondary winding, which can be difficult to design for most performance. The bridge rectifier is a compromise between the half wave and transformer center tapped rectifiers. Its efficiency is between the two other rectifiers and it uses only one transformer secondary winding. However it uses twice as much semiconductor devices, but the voltage stress is reduced by half. All of these rectifiers can be converted to synchronous rectifiers, by replacing the diodes with low R_{DSon} resistance MOSFETs, which can further improve the rectifier efficiency.

3 Control Methods for SMPS

As the demand for Switching Mode Power Supplies' (SMPS) performance and functionality increases, there is a need for more robust and flexible methods for feedback loop control. Modern power supplies often already have an on-board microcontroller dedicated to monitoring the operating parameters (e.g. output current, operating temperature) and for communication with external devices. Concurrently, applying digital control methods for SMPS has been a topic of intense research[27], [28], [29], [30], [31], [32], [33], [34], [35]. By implementing the feedback loop in a digital circuit (i.e. microcontroller or FPGA IC) we receive much more freedom in the design of the control loop. Another advantage of digital control is the reduction of space that is needed on a PCB in comparison to traditional analog control methods and the ability to easily modify and reuse the solution. Digital control can be already found in many classic hard-switching PWM power supply applications [36].

This chapter will present the state-of-the-art in power supply control techniques with resonant converters in mind. The covered methods include: Pulse Width Modulation (PWM), bridge leg Phase Shift Modulation (PSM), Pulse Density Modulation (PDM), Frequency Modulation (FM), Asymmetrical Pulse Width Modulation (APWM) and Resonant Current Phase Modulation as a supplement for other methods.

3.1 Pulse Width Modulation

One of the most widely employed control schemes in power converters is the pulse width modulation (PWM). As the name states, the regulation is achieved by variation of the pulse width that drives the switching devices, i.e. variation of the switch duty cycle. Typical waveforms for PWM are shown in Fig. 3.1.

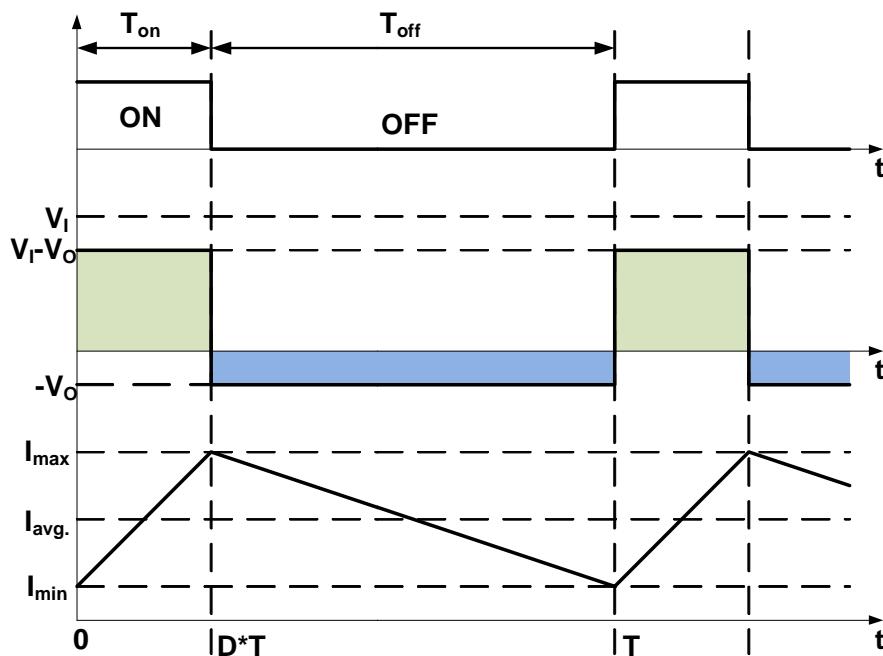


Fig. 3.1 Pulse width modulation operation waveforms

The PWM usually operates at a fixed frequency, however many systems combine frequency variation as well [37], [38]. The variable frequency can be used for spreading of the EMI spectrum, or for more advanced switching techniques (e.g. boundary or critical mode in PFC rectifiers). PWM is widely used in hard-switching converters due to the simplicity of controller design and simplicity of calculations. Unfortunately, direct PWM is not well suited for resonant converters, because soft-switching conditions are not always ensured. As presented later, this method can be modified for resonant converters.

3.2 Phase Shift Modulation

Another commonly method used is the Phase Shift Modulation. This scheme is used in bridge topologies that have at least 2 legs. For simplicity, let's consider a classic four switch bridge. The idea is to operate the two bridge legs with a phase angle shift ϕ . The maximum power is achieved when $\phi=180^\circ$, whereas minimum power is achieved when $\phi=0^\circ$.

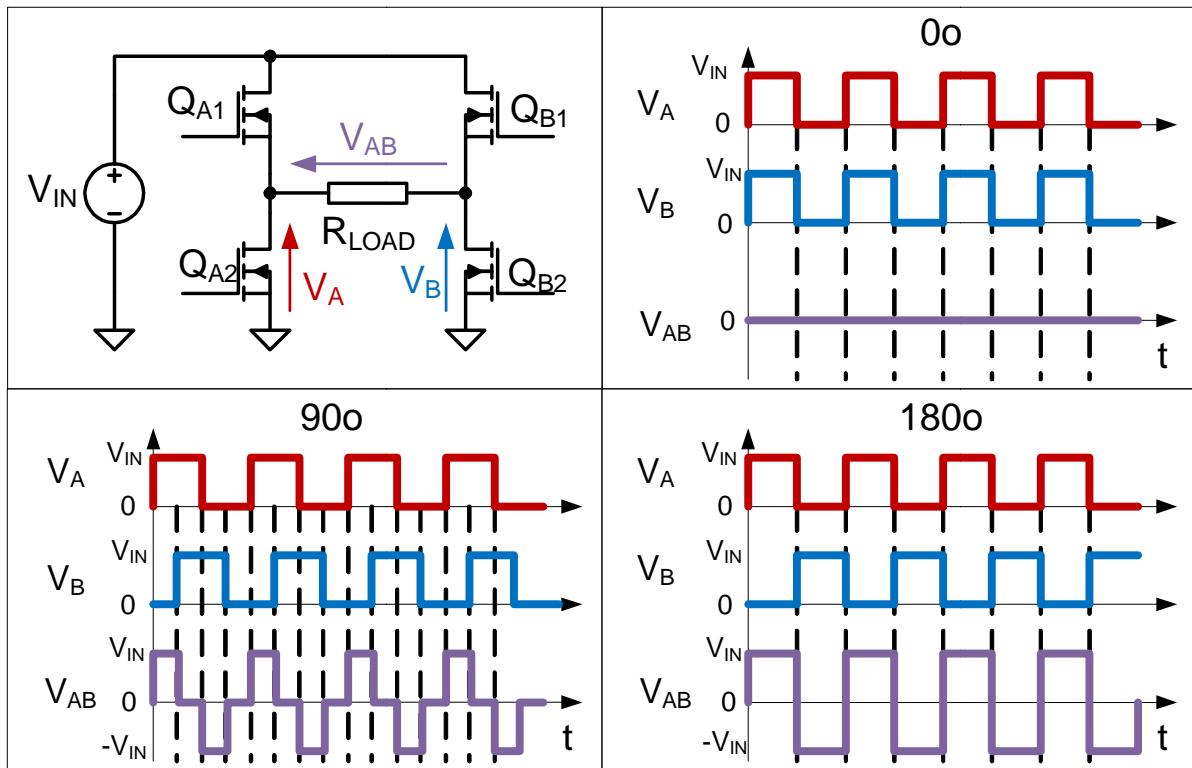


Fig. 3.2 Phase shift modulation operations waveforms

The regulation is achieved by variation of the phase angle. The method is widely used in high power hard-switching applications, because it requires at least four power switches for the primary side. With slight modifications, the phase shift modulation can be used in soft-switching converters including resonant converters [39], [40].

3.3 Burst Mode – Pulse Density Modulation

A simple and common method of regulation is the Burst Mode method, a subclass of Pulse Density Modulation (PDM)[41], [42], [43]. By skipping a switching cycle, we put on hold the transfer of the energy from the source to the load. Thus, by regulating the duty cycle of the switching time to

non-switching time the output regulation can be achieved. The method can be easily implemented using a voltage comparator with hysteresis. If the output voltage is above the threshold the pulse generation for the switches is ceased. If the output voltage drops below the threshold, pulse generations is resumed, allowing the converter to deliver energy to the output. This method will produce a higher voltage ripple at the output of the converter, compared to methods described earlier. The switching frequency of the generated pulses is often kept constant. Fig. 3.3 presents typical waveforms for Burst Mode operation

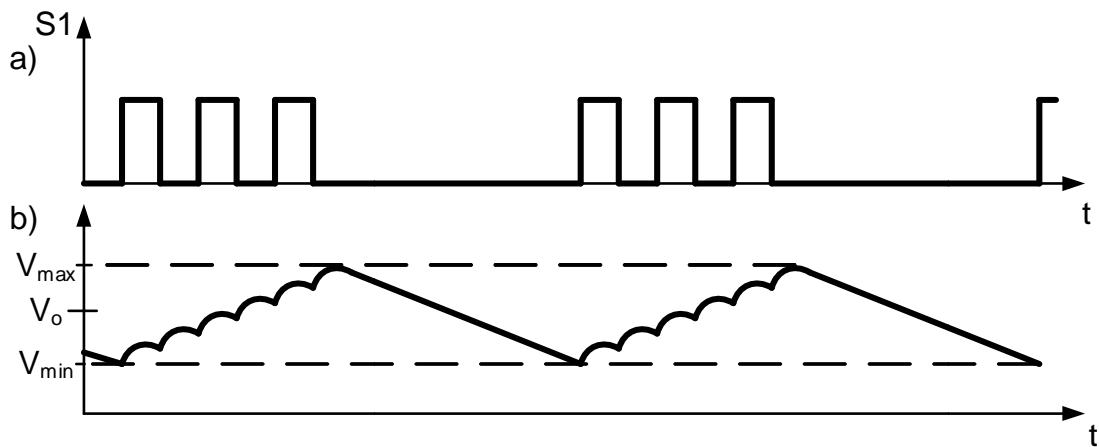


Fig. 3.3 Burst Mode operation at partial load conditions. a) Switch drive signals, b) converter output voltage

This method is often used as an addition to the PWM or FM to improve efficiency at light loads.

The PDM method is not only limited to burst mode operation. In [44], [45], [46], [47] an interesting approach, that uses the Delta-Sigma converter, is presented. A 1-bit Delta-Sigma modulator (Fig. 3.4) is used to drive the half-bridge resonant inverter switches directly. The main advantage of this method over a classic burst mode is the lack of sub-harmonics in the output voltage. Lower output voltage sub-harmonics allow to decrease the size of the output filter needed to achieve the desired ripple voltage. This method can also potentially reduce the audible sound generated by the converter.

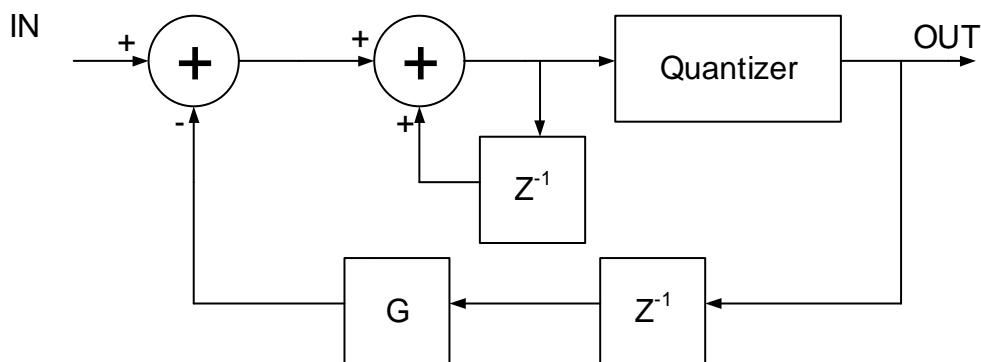


Fig. 3.4 1st order delta-sigma modulator controller [44]

Depending on the output value of the quantizer in the delta-sigma modulator the half-bridge is driven as follows. While the output is “1” the switches are driven normally. When the output is “0” the switches are off.

The Burst Mode is sometimes implemented in controllers dedicated for resonant converters. It is due to the fact that in some cases (e.g. 2nd order series loaded resonant converter) the switching frequency would have to be increased significantly to maintain regulation. The addition of Burst Mode allows for output regulation at light and no load conditions. It should be noted, that in resonant converters, the next switching cycle should start when the resonant current amplitude falls close to zero. Otherwise, the switches may be damaged if turned on when the resonant current is in wrong phase. This will present conditions similar to operation in capacitive region, which can create conditions for one of the failures described in chapter 2.3. Because of this the frequency of the Burst Mode is limited to a relatively low value (around several hundreds of Hz).

3.4 Frequency Modulation

The most common method applied in resonant converters, that allows for output regulation, is the Frequency Modulation (FM). By varying the operating frequency the amplitude of the resonant current changes according to the impedance of the resonant tank [48]. This regulates the amount of power transferred to the output. Usually a half-bridge or full-bridge is used to produce a symmetrical voltage square wave, which is fed into a resonant tank. The frequency of this voltage waveform will affect the current and voltage levels in the resonant circuit, as well as, the phase difference between the fundamental component of the voltage produced by the switches and resonant tank current. Chapter 2 has shown, that the desired operating region for resonant inverters is the region above the resonant frequency of the resonant tank. Fig. 3.5 shows the voltage transfer function for class D series-parallel LCLC resonant inverter. It can be seen that the voltage transfer function is highly nonlinear and changes with varying inverter load and operating frequency. At full load the switching frequency approaches the resonant frequency and as the load decreases the frequency rises. However, the frequency cannot rise indefinitely, because the limited performance of switches and switch drivers impose a limit for the maximum switching frequency. This means that for some resonant tank designs, the converter can lose regulation at light or no load conditions. Another problematic area is the operation near the resonant frequency. Depending on the inductive and capacitive components tolerances, the resonant frequency of the tank can vary. To avoid entering the region below resonance (i. e. capacitive load for the switches), a limit for minimum switching frequency must be set. The limit should be set in such a way, that it leaves enough of a margin for the resonant frequency variations from piece to piece and in different operating temperatures. Otherwise, if the converter can enter capacitive region operation and the switches are likely to break down.

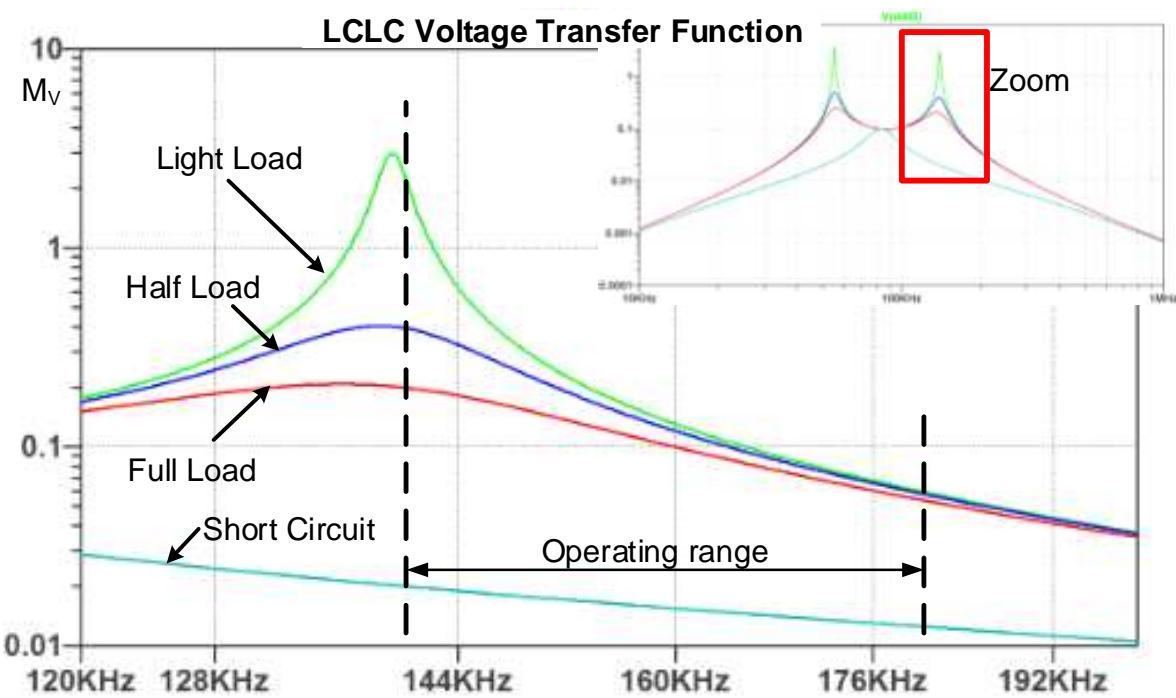


Fig. 3.5 Voltage transfer function of the resonant LCLC inverter in function of the switching frequency for different loads

The impedance of the series-parallel resonant tank vs frequency is presented in Fig. 3.6. To maintain proper switching conditions the converter should operate above the resonant frequency marked with a curve in Fig. 3.6. Another problem associated with resonant converters is the variation of the transfer function with the operating point. This makes harder to design the feedback loop because at various operating points the resonant tank gain changes, which can make the converter unstable.

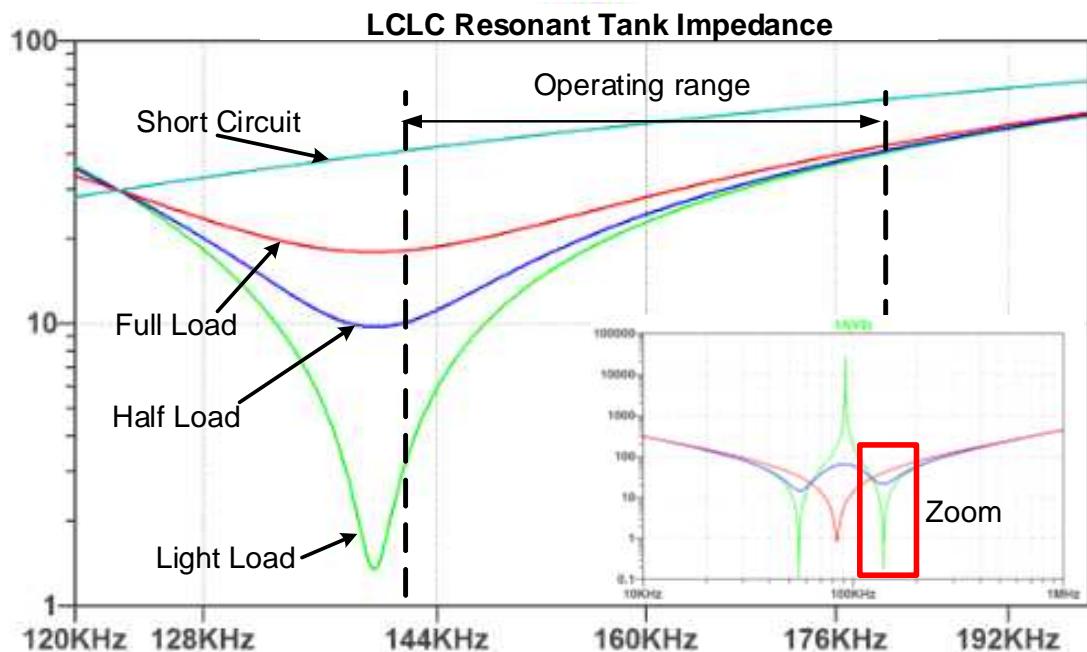


Fig. 3.6 LCLC resonant tank current magnitude in function of the switching frequency for different loads

As shown above the FM method has many drawbacks, thus there is a need for better solutions. However, one undeniable advantage of this method is its simple implementation and low cost which is why it is the most widely spread control methods for resonant converters.

3.5 Asymmetrical Pulse Width Modulation control

Another control method for the resonant converters is the Asymmetrical Pulse Width Modulation (APWM) presented in[49]. Since the efficiency of the resonant inverter drops as the switching frequency is increased, the author proposes an asymmetrical PWM control strategy. Fig. 3.7 presents the waveforms for APWM operation. The output power is regulated by regulating the ratio of the on-times of the high and low side switches.

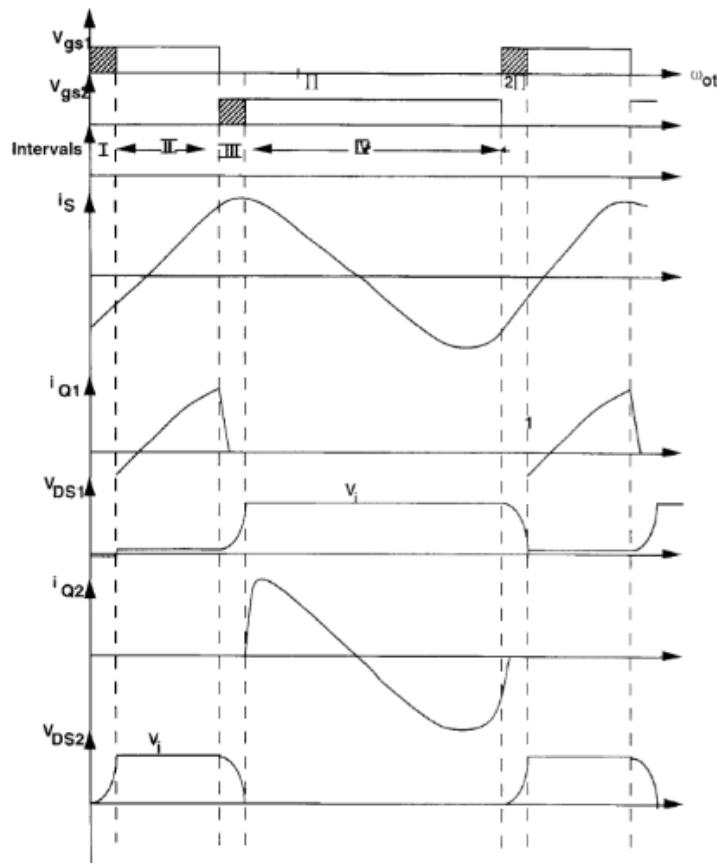


Fig. 3.7 Operating waveforms for asymmetrical PWM scheme [49]

When the high switch is being turned on for time $D T_{\text{period}}$, the low side switch will be turned on for time $(1-D)T_{\text{period}}$. This will result in change of the power delivered to the output, thus regulation can be achieved by changing the parameter D. Fig. 3.8 shows the shape of how the output voltage changes in regard to duty cycle D.

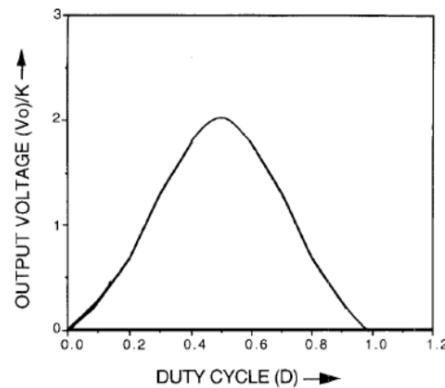


Fig. 3.8 Output voltage control for the APWM scheme [49]

It can be seen that the maximum voltage appears when $D=0.5$ (i.e. the driving signals are symmetrical). If the operating frequency is kept constant, the allowed deviation from $D=0.5$ is small, due to risk of losing ZVS conditions. In order to keep the ZVS for the whole load range, the operating frequency can be varied. In [50] the authors show a proposal of such implementation. By adding a phase locked loop (PLL), the operating frequency can be controlled with high precision by maintaining a constant phase shift between resonant current and half-bridge current.

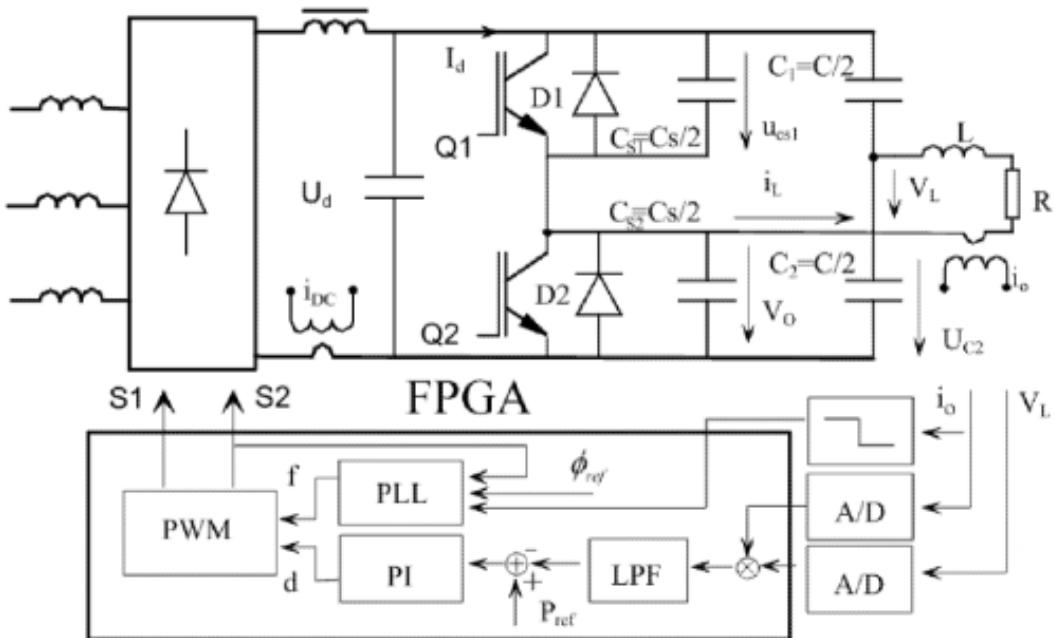


Fig. 3.9 System configuration for APWM with frequency tracking [7]

This allows to keep ZVS conditions over a wider load range than a constant frequency method. Also the switching frequency is being changed on a narrower range than in FM method.

3.6 Resonant Current Phase Control

As mentioned in previous subchapter, the phase of the resonant current related to half-bridge voltage can be regulated to ensure ZVS. It is possible to modulate only the resonant current phase to achieve output regulation, however the result will be very similar to FM. This is why the resonant

current phase modulation is rather used as a supplementing technique for ensuring the ZVS. In such applications a control loop is generally used for resonant current phase regulation in order to keep it at a constant value. By doing this, the zero-voltage switching can be ensured in most cases. However, since the phase value is being regulated to have a constant value, there is a need of an additional method for power regulation. In [40] the authors show a conjunction of resonant current phase stabilization with a full-bridge phase shift to achieve voltage regulation, called Self-Sustained Oscillation.

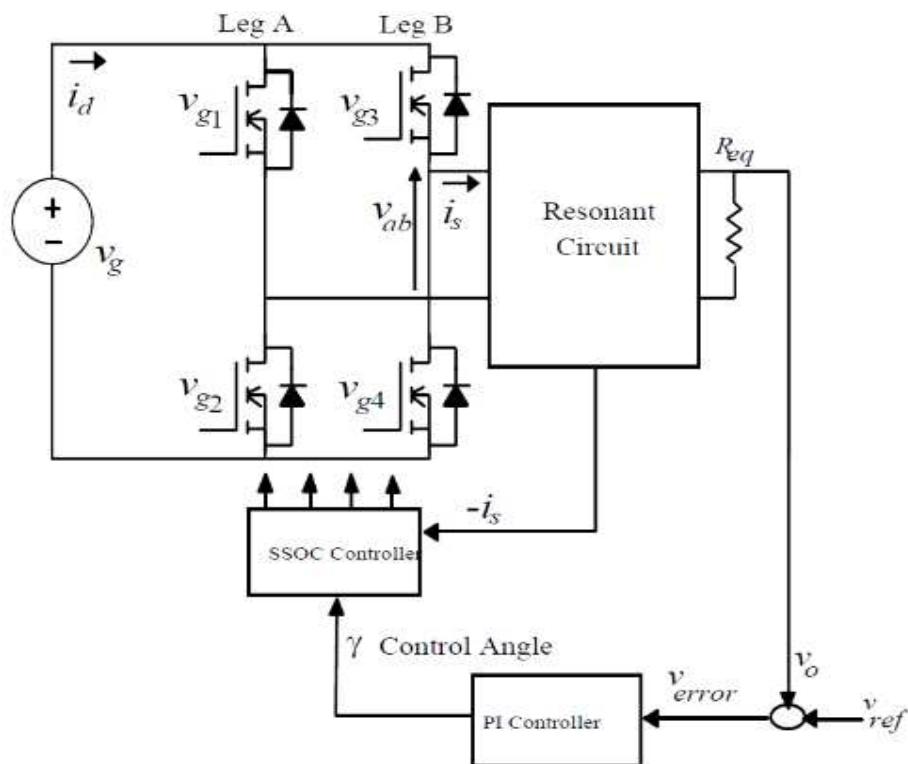


Fig. 3.10 Simplified schematic of a Self-Sustained Oscillation Controller [40]

As can be seen in Fig. 3.10 the controller consists of two control loops, one for resonant current phase stabilization and one for output voltage stabilization. The phase stabilization loop measures the time between the zero-crossing of the resonant current and the instant when one of the switches in a single bridge leg is turned off. By using this information the operating frequency is modified in order to counter any changes of the measured phase. Thus , the proper conditions for Zero-Voltage Switching can be maintained throughout the whole load range. Since the operating frequency is used to regulate the phase, another parameter must be modulated in order to maintain output power regulation. The authors proposed to use the phase shift modulation described in 3.2.

Fig. 3.11 presents the operating waveforms for the Self-Sustained Oscillation Control (SSOC) control. The i_s is the resonant current, V_{ca1} and V_{ca2} are thresholds for resonant current phase loop and bridge phase shift loop respectively, V_{ao} and V_{bo} are the output voltages of each half-bridge and V_{ab} is the voltage across the resonant circuit.

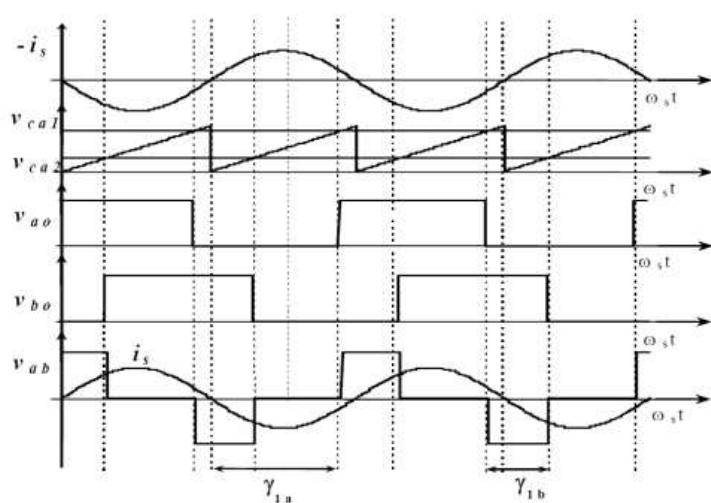


Fig. 3.11 Basic waveforms of the Self-Sustained Oscillation Controller [40]

The advantages of this kind of control are: ensuring the ZVS in whole operation range, reduced conduction losses in switches, reduced current peak values in switches and reduced switching frequency bandwidth. This features will improve the converter efficiency and reliability.

3.7 Summary

In this chapter several control methods have been discussed. The two most commonly used (PWM and phase shift modulation) cannot be directly applied to resonant converters because of the risk of losing the ZVS conditions. Thus the simplest and most broadly applied method is the FM. The controller for the FM is simple and cheap to build and doesn't need any additional measurement circuits apart from the regulated output value. However, the FM is not ideal and has its drawbacks (e.g. poor efficiency at light loads). In order to improve the resonant converter performance more advanced control methods are being researched. APWM and SSOC are the two examples of such methods. These methods ensure ZVS in the whole operating region and allow for better converter performance. This comes at a cost of additional measurement circuitry, however in applications where performance is top priority it isn't a big disadvantage.

4 Novel Control Method of Resonant Power Converter – Sequential Cycle Stealing

Recently there has been a lot of research in PDM control schemes, leading to quite interesting results [39], [51], [52], [53], [54]. However, most of the research focused mostly on second-order LC resonant circuit and in some cases third-order LLC resonant circuit. Since, the PDM control scheme has given such good results, a proposal has been made to try to apply such a method for the fourth-order LCLC resonant circuit. The proposed method is based on control method presented in [7] and [8] owned by AGH University of Science and Technology. The research has been conducted as a part of grant 65010 – “Innowacyjny zasilacz rezonansowy dużej mocy do pojazdów hybrydowych i elektrycznych” directed by Sławomir Ligenza from Fideltronik Poland Sp. z o.o. This chapter will focus on presenting the main idea of the method which is named Sequential Cycle Stealing.

4.1 Operation of the SCS Control Scheme

The main idea is to regulate the desired output parameter (e.g. voltage, current, power, etc.) by stealing (or cancelling) switching cycles of the resonant converter. The more switching cycles are stolen the less power is delivered to the resonant circuit and to the output of the converter. The main difference between this method and the others is that during periods when the converter stops switching, the last turned on switches are kept turned on. By doing so, the resonant current is allowed to pass through low resistance channel of the transistor instead through the body diode. This reduces the overall power losses and allows the resonant circuit to resonate freely for longer period of time. During free oscillations the amplitude and frequency of the resonant current is smaller than it would be with FM. This leads to lower copper losses due to reduced high frequency effects (i.e. skin effect and proximity effect) and to lower core losses due to lower amplitude of magnetic flux density (B_{pk}) and lower frequency. Usually the core losses are approximated with the Steinmetz equation:

$$P_{loss} = V_e \cdot K \cdot f^\alpha \cdot B_{pk}^\beta$$

where V_e is the effective core volume, f is the operating frequency, B_{pk} is the magnetic flux density. And K , α and β are material coefficients. Usually the α term is around 1.5 and β term is around 2.5. Thus, even small reduction in f or B_{pk} can save a lot of power. In addition to these savings, the overall switching losses (both primary and secondary side) and transistor driver losses are reduced because the average switching frequency is reduced.

The control scheme should guarantee the proper switching conditions for the transistors to avoid problems described in chapter 2.2. Fig. 4.1 presents an example of SCS operation. The drive signal V_{gate1} is applied to transistors Q_1 and Q_4 and V_{gate2} to transistors Q_2 and Q_3 . The waveform i_r represents the resonant current, while V_{out} represents the rectified output voltage (rectifier is not shown in the schematic). It should be pointed out, that during the time when the converter is switching, the frequency of the resonant circuit is different when the switching stops. This is due to the fact that during switching the resonant circuit oscillates with the forced frequency while during idle time the resonant circuit oscillates with its own resonant frequency. Additionally, the self resonant frequency varies with load, temperature, etc. In order to ensure the proper switching

conditions, especially when the switching restarts, it is necessary to measure the resonant current i_r . This gives us the information about the direction (i.e. sign) of the current as well as the instantaneous value. Thanks to this, a proper time instant can be chosen for the switch to turn on, i.e. the current in the switch is negative and its value is high enough to swing the voltage in the half-bridge (class DE switching). Otherwise, the switches may break down due to excessive currents when the ZVS conditions are lost.

The SCS operation is as follows. Suppose that the converter is switching. This means that the output voltage V_{out} is steadily rising until it reaches the upper threshold V_{out_high} . Upon crossing this threshold the converter stops switching, but keeps the switches that were turned on in on state. The resonant circuit starts to oscillate with self resonant frequency and the resonant current amplitude as well as the output voltage steadily decreases. When the output voltage falls to low threshold V_{out_low} , the converter synchronizes with the resonant current and restarts switching.

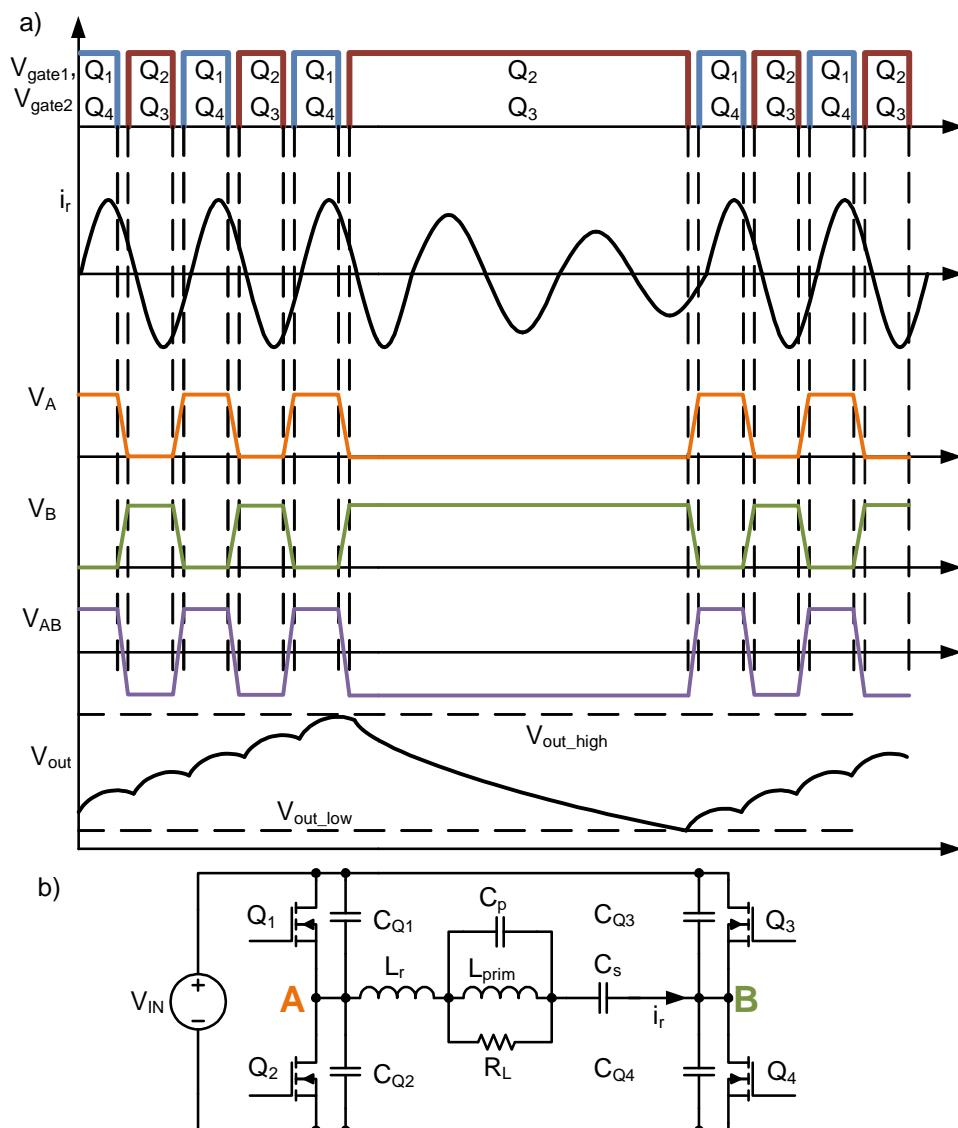


Fig. 4.1 Basic operation of the SCS in class DE full-bridge LCLC resonant converter; a) operating waveforms, b) Class DE full-bridge LCLC DC-DC resonant converter

There is a risk that during the non-switching period the resonant current amplitude will fall to a level where it is not possible to either synchronize or to fully swing the half-bridge voltage when the switching restarts. To prevent such scenario, a mechanism has been implemented to keep the resonant current above a preset level. The resonant current RMS value is observed and if it falls below a set threshold the converter will start switching until the RMS value of the resonant current rises above the threshold. The switching instances are synchronized with the resonant current to prevent improper switching conditions.

It is worth to note that it is not optimal to keep the same pair of switches turned on during the self oscillation periods. Consider a situation of a light load. The converter will be switching for time T_{ON} and will stop switching for T_{OFF} . If the same switch pair was constantly chosen for the T_{OFF} period it would conduct the resonant current for a significantly longer time than the opposite pair. This would result in higher switch temperature which results in higher conduction losses (in case of MOSFETs) and reduced reliability. To balance the conduction times, we can select the opposite switch pair each time the converter enters the T_{OFF} period. Such mechanism will balance the conduction times of the switches and reduce the switch junction operating temperature.

4.2 Step response of a series-parallel LCLC resonant circuit

In order to have a better insight in the behavior of the resonant converters, step response for the series LC circuit and series-parallel LCLC circuits will be derived. Consider a series LC resonant circuit presented in Fig. 4.2.

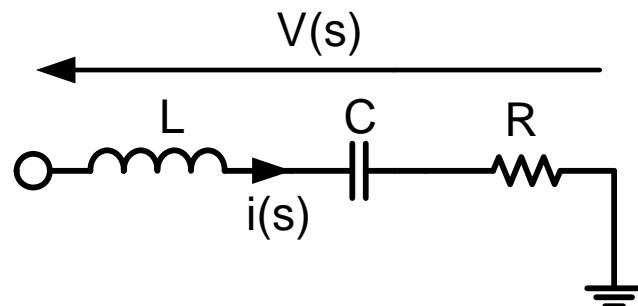


Fig. 4.2 Series resonant LC circuit

The input voltage can be written as:

$$V(s) = i(s) \cdot sL + i(s) \cdot \frac{1}{sC} + i(s)R$$

$$V(s) = i(s) \cdot \left(sL + \frac{1}{sC} + R \right)$$

Thus, the resonant current is equal to:

$$i(s) = \frac{V(s)}{\left(sL + \frac{1}{sC} + R \right)}$$

$$i(s) = \frac{V(s) \cdot sC}{\left(s^2 LC + sCR + 1 \right)}$$

Inserting the transmittance of the step function for $V(s)$, $V_{IN}(s) = \frac{1}{s}$, and assuming zero initial conditions we get:

$$i(s) = \frac{\frac{1}{s} \cdot sC}{s^2 LC + sCR + 1}$$

$$i(s) = \frac{C}{s^2 LC + sCR + 1}$$

$$i(s) = \frac{\frac{1}{L}}{s^2 + s \frac{R}{L} + \frac{1}{LC}}$$

$$i(s) = \frac{\frac{1}{L}}{s^2 + s \frac{R}{L} + \frac{R^2}{4L^2} - \frac{R^2}{4L^2} + \frac{1}{LC}}$$

$$i(s) = \frac{\frac{1}{L}}{\left(s + \frac{R}{2L} \right)^2 + \frac{1}{LC} - \frac{R^2}{4L^2}}$$

Assuming that: $\frac{1}{LC} > \frac{R^2}{4L^2}$

$$i(s) = \frac{1}{L \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}} \cdot \frac{\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}}{\left(s + \frac{R}{2L} \right)^2 + \left(\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \right)^2}$$

Knowing that $Ae^{\alpha t} \sin \omega_r t \rightarrow A \frac{\omega_r}{(s - \alpha)^2 + \omega_r^2}$

We can calculate the coefficients A, α , ω :

$$\alpha = -\frac{R}{2L}$$

$$\omega_r = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}$$

$$A = \frac{1}{\omega_r L}$$

It can be seen that as long as $\frac{1}{LC} > \frac{R^2}{4L^2}$ holds, the step response of a LC circuit has a form of fading oscillations. The resulting resonant current shape can be observed in Fig. 4.3, which is the result of SPICE simulation.

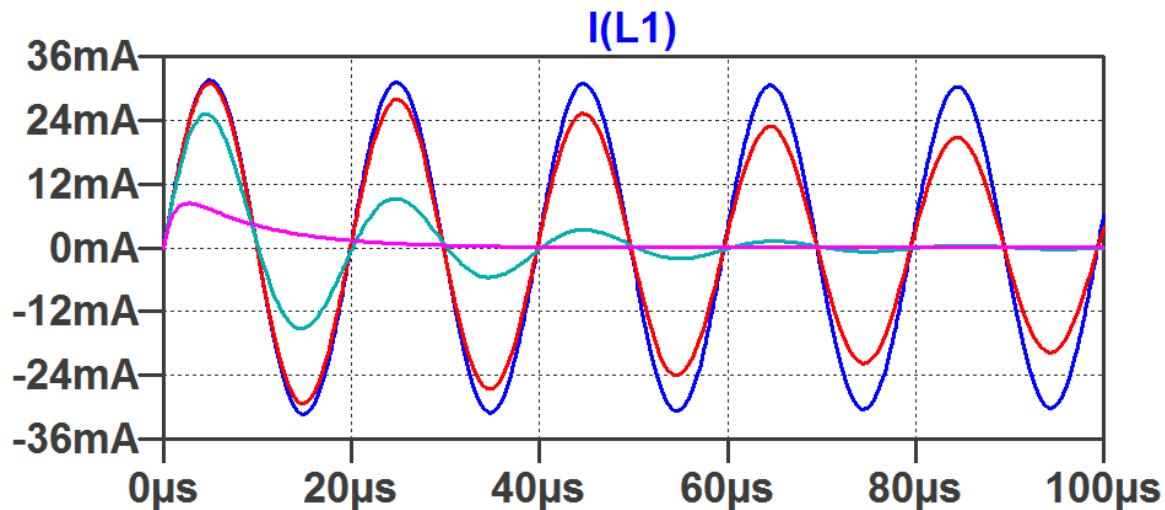


Fig. 4.3 Series loaded LC resonant tank step response for various R values

A similar analysis will be performed for the LCLC circuit which is presented in Fig. 4.4.

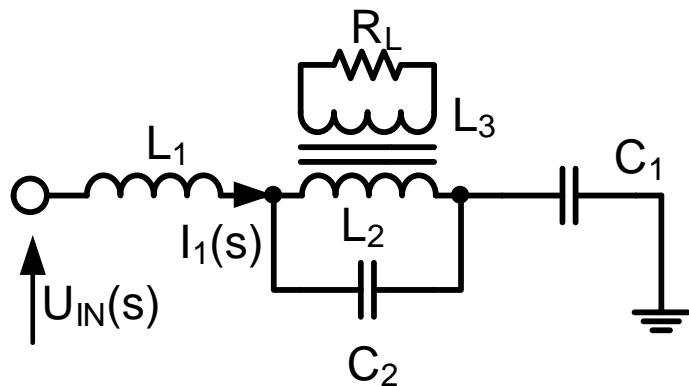


Fig. 4.4 Series-parallel LCLC resonant circuit

After calculations we can derive the following equation:

$$\begin{aligned}
 I_1(s) &= U_{IN}(s) \frac{s^4(L_2L_3C_1C_2 - M^2C_1C_2) + s^3L_2C_1C_2R_L + s^2L_3C_1 + sC_1R_L}{s^5(L_1L_2L_3C_1C_2 - L_1M^2C_1C_2) + s^4(L_1L_2C_1C_2R_L) +} = \\
 &\quad + s^3(L_1L_3C_1 + L_2L_3C_2 - M^2C_2 + L_2L_3C_1 - M^2C_1) + \\
 &\quad + s^2(L_1C_1R_L + L_2C_2R_L + L_2C_1R_L) + sL_3 + R_L \\
 &= \frac{U_{IN}(s)}{R_L} \frac{s^4(L_2L_3C_1C_2 - M^2C_1C_2) + s^3L_2C_1C_2R_L + s^2L_3C_1 + sC_1R_L}{s^5(L_1L_2L_3C_1C_2 - L_1M^2C_1C_2)(1/R_L) + s^4(L_1L_2C_1C_2) +} \\
 &\quad + s^3(L_1L_3C_1 + L_2L_3C_2 - M^2C_2 + L_2L_3C_1 - M^2C_1)(1/R_L) + \\
 &\quad + s^2(L_1C_1 + L_2C_2 + L_2C_1) + sL_3(1/R_L) + 1
 \end{aligned}$$

In order to clarify the equation we shall substitute the polynomial coefficients as:

$$a_4 = (L_2L_3C_1C_2 - M^2C_1C_2)$$

$$a_3 = L_2C_1C_2R_L$$

$$a_2 = L_3C_1$$

$$a_1 = C_1R_L$$

$$b_5 = (L_1L_2L_3C_1C_2 - L_1M^2C_1C_2)(1/R_L)$$

$$b_4 = L_1L_2C_1C_2$$

$$b_3 = (L_1L_3C_1 + L_2L_3C_2 - M^2C_2 + L_2L_3C_1 - M^2C_1)(1/R_L)$$

$$b_2 = L_1C_1 + L_2C_2 + L_2C_1 = L_1C_1 + L_2(C_2 + C_1)$$

$$b_1 = L_3(1/R_L)$$

$$b_0 = 1$$

Thus, the equation transforms into:

$$I_1(s) = \frac{U_{IN}(s)}{R_L} \frac{a_4s^4 + a_3s^3 + a_2s^2 + a_1s}{b_5s^5 + b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0}$$

To calculate the step response we substitute: $U_{IN}(s) = \frac{U}{s}$

$$I_1(s) = \frac{U}{s} \frac{a_4s^4 + a_3s^3 + a_2s^2 + a_1s}{b_5s^5 + b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0} = U \frac{a_4s^3 + a_3s^2 + a_2s^1 + a_1}{b_5s^5 + b_4s^4 + b_3s^3 + b_2s^2 + b_1s + b_0}$$

Assuming that the coupling coefficient M is equal to 1 we get:

$$M = \sqrt{L_2L_3}$$

$$a_4 = 0$$

$$a_3 = L_2 C_1 C_2 R_L$$

$$a_2 = L_3 C_1$$

$$a_1 = C_1 R_L$$

$$b_5 = 0$$

$$b_4 = L_1 L_2 C_1 C_2$$

$$b_3 = L_1 L_3 C_1 (1/R_L)$$

$$b_2 = L_1 C_1 + L_2 (C_2 + C_1)$$

$$b_1 = L_3 (1/R_L)$$

$$b_0 = 1$$

Thus, the equation reduces to:

$$I_1(s) = \frac{U}{s} \frac{a_3 s^3 + a_2 s^2 + a_1 s}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} = U \frac{a_3 s^2 + a_2 s + a_1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1}$$

As we can see in equation above, the denominator polynomial order is 4. Since, the solution for the 4th order polynomial roots is quite complex, it can be seen that it will be hard to determine the influence of the component values on the step response. We shall derive a general solution instead, assuming that the denominator polynomial roots are known. Let p_1, p_2, p_3 and p_4 be the root of the 4th order polynomial.

$$\begin{aligned} I_1(s) &= U \frac{a_3 s^2 + a_2 s + a_1}{b_4 s^4 + b_3 s^3 + b_2 s^2 + b_1 s + 1} = U \frac{L(s)}{M(s)} = U \frac{a_3 s^2 + a_2 s + a_1}{(c_2 s^2 + c_1 s + 1)(d_2 s^2 + d_1 s + 1)} = \\ &= U \frac{a_3 s^2 + a_2 s + a_1}{(s - p_1)(s - p_2)(s - p_3)(s - p_4)} = \\ &= U \left\{ \frac{R_1}{(s - p_1)} + \frac{R_2}{(s - p_2)} + \frac{R_3}{(s - p_3)} + \frac{R_4}{(s - p_4)} \right\} \end{aligned}$$

The R_1, R_2, R_3 and R_4 can be derived using the residue theorem.

$$R_i = (s - p_i) I_1(s) \Big|_{s=p_i} = (s - p_i) \frac{L(s)}{M(s)} \Big|_{s=p_i} = \frac{L(p_i)}{(p_i - p_1)(p_i - p_2) \cdots (p_i - p_n)}$$

$$R_1 = (s - p_1) I_1(s) \Big|_{s=p_1} = (s - p_1) \frac{L(s)}{M(s)} \Big|_{s=p_1} = \frac{a_3 p_1^2 + a_2 p_1 + a_1}{(p_1 - p_2)(p_1 - p_3) \cdot (p_1 - p_4)}$$

$$R_2 = (s - p_2) I_1(s) \Big|_{s=p_2} = (s - p_2) \frac{L(s)}{M(s)} \Big|_{s=p_2} = \frac{a_3 p_2^2 + a_2 p_2 + a_1}{(p_2 - p_1)(p_2 - p_3) \cdot (p_2 - p_4)}$$

$$R_3 = (s - p_3)I_1(s) \Big|_{s=p_3} = (s - p_3) \frac{L(s)}{M(s)} \Big|_{s=p_3} = \frac{a_3 p_3^2 + a_2 p_3 + a_1}{(p_3 - p_1)(p_3 - p_2) \cdot (p_3 - p_4)}$$

$$R_4 = (s - p_4)I_1(s) \Big|_{s=p_4} = (s - p_4) \frac{L(s)}{M(s)} \Big|_{s=p_4} = \frac{a_3 p_4^2 + a_2 p_4 + a_1}{(p_4 - p_1)(p_4 - p_2) \cdot (p_4 - p_3)}$$

Substituting for R_1 , R_2 , R_3 and R_4 we get:

$$I_1(s) = U \left\{ \frac{R_1}{(s - p_1)} + \frac{R_2}{(s - p_2)} + \frac{R_3}{(s - p_3)} + \frac{R_4}{(s - p_4)} \right\} = U \left\{ \begin{array}{l} \frac{a_3 p_1^2 + a_2 p_1 + a_1}{(p_1 - p_2)(p_1 - p_3) \cdot (p_1 - p_4)} \frac{1}{(s - p_1)} + \\ + \frac{a_3 p_2^2 + a_2 p_2 + a_1}{(p_2 - p_1)(p_2 - p_3) \cdot (p_2 - p_4)} \frac{1}{(s - p_2)} + \\ + \frac{a_3 p_3^2 + a_2 p_3 + a_1}{(p_3 - p_1)(p_3 - p_2) \cdot (p_3 - p_4)} \frac{1}{(s - p_3)} + \\ + \frac{a_3 p_4^2 + a_2 p_4 + a_1}{(p_4 - p_1)(p_4 - p_2) \cdot (p_4 - p_3)} \frac{1}{(s - p_4)} \end{array} \right\}$$

The step response in time domain is equal to:

$$\begin{aligned} i_1(t) &= R_1 e^{p_1 t} + R_2 e^{p_2 t} + R_3 e^{p_3 t} + R_4 e^{p_4 t} = \frac{a_3 p_1^2 + a_2 p_1 + a_1}{(p_1 - p_2)(p_1 - p_3)(p_1 - p_4)} e^{p_1 t} + \\ &+ \frac{a_3 p_2^2 + a_2 p_2 + a_1}{(p_2 - p_1)(p_2 - p_3)(p_2 - p_4)} e^{p_2 t} + \frac{a_3 p_3^2 + a_2 p_3 + a_1}{(p_3 - p_1)(p_3 - p_2)(p_3 - p_4)} e^{p_3 t} + \\ &+ \frac{a_3 p_4^2 + a_2 p_4 + a_1}{(p_4 - p_1)(p_4 - p_2)(p_4 - p_3)} e^{p_4 t} \end{aligned}$$

If p_1 , p_2 and p_3 , p_4 are conjugated respectively, they will form two pairs of conjugated poles.

$$p_2 = p_1^* \quad \text{and} \quad p_4 = p_3^*$$

$$p_1 = -p_{1\text{Re}} + j p_{1\text{Im}} \quad \text{and} \quad p_2 = p_1^* = -p_{1\text{Re}} - j p_{1\text{Im}}$$

$$p_3 = -p_{3\text{Re}} + j p_{3\text{Im}} \quad \text{and} \quad p_4 = p_3^* = -p_{3\text{Re}} - j p_{3\text{Im}}$$

The step response equation can be then written as:

$$\begin{aligned} I_1(s) &= U \frac{a_3 s^2 + a_2 s + a_1}{(c_2 s^2 + c_1 s + 1)(d_2 s^2 + d_1 s + 1)} = \\ &= U \frac{a_3 s^2 + a_2 s + a_1}{(s + p_{1\text{Re}} - j p_{1\text{Im}})(s + p_{1\text{Re}} + j p_{1\text{Im}})(s + p_{3\text{Re}} - j p_{3\text{Im}})(s + p_{3\text{Re}} + j p_{3\text{Im}})} = \\ &= U \left\{ \frac{\hat{R}_1}{(s + p_{1\text{Re}} - j p_{1\text{Im}})} + \frac{\hat{R}_2}{(s + p_{1\text{Re}} + j p_{1\text{Im}})} + \frac{\hat{R}_3}{(s + p_{3\text{Re}} - j p_{3\text{Im}})} + \frac{\hat{R}_4}{(s + p_{3\text{Re}} + j p_{3\text{Im}})} \right\} \end{aligned}$$

where:

$$\begin{aligned}
 \hat{R}_1 &= (s - p_1) I_1(s) \Big|_{s=p_1} = \frac{a_3 p_1^2 + a_2 p_1 + a_1}{(p_1 - p_2)(p_1 - p_3) \cdot (p_1 - p_4)} = \\
 &= \frac{a_3(-p_{1\text{Re}} + jp_{1\text{Im}})^2 + a_2(-p_{1\text{Re}} + jp_{1\text{Im}}) + a_1}{[-p_{1\text{Re}} + jp_{1\text{Im}} - (-p_{1\text{Re}} - jp_{1\text{Im}})](-p_{1\text{Re}} + jp_{1\text{Im}} + p_{3\text{Re}} - jp_{3\text{Im}}) \cdot (-p_{1\text{Re}} + jp_{1\text{Im}} + p_{3\text{Re}} + jp_{3\text{Im}})} = \\
 &= \frac{a_3(-p_{1\text{Re}} + jp_{1\text{Im}})^2 + a_2(-p_{1\text{Re}} + jp_{1\text{Im}}) + a_1}{j 2 p_{1\text{Im}} (-p_{1\text{Re}} + jp_{1\text{Im}} + p_{3\text{Re}} - jp_{3\text{Im}}) \cdot (-p_{1\text{Re}} + jp_{1\text{Im}} + p_{3\text{Re}} + jp_{3\text{Im}})} = |R_1| e^{j\psi_{R1}} \\
 \hat{R}_2 &= (s - p_2) I_1(s) \Big|_{s=p_2} = \frac{a_3 p_2^2 + a_2 p_2 + a_1}{(p_2 - p_1)(p_2 - p_3) \cdot (p_2 - p_4)} = \\
 &= \frac{a_3(-p_{1\text{Re}} - jp_{1\text{Im}})^2 + a_2(-p_{1\text{Re}} - jp_{1\text{Im}}) + a_1}{[-p_{1\text{Re}} - jp_{1\text{Im}} - (-p_{1\text{Re}} + jp_{1\text{Im}})](-p_{1\text{Re}} - jp_{1\text{Im}} + p_{3\text{Re}} - jp_{3\text{Im}}) \cdot (-p_{1\text{Re}} - jp_{1\text{Im}} + p_{3\text{Re}} + jp_{3\text{Im}})} = \\
 &= \frac{a_3(-p_{1\text{Re}} - jp_{1\text{Im}})^2 + a_2(-p_{1\text{Re}} - jp_{1\text{Im}}) + a_1}{-j 2 p_{1\text{Im}} (-p_{1\text{Re}} - jp_{1\text{Im}} + p_{3\text{Re}} - jp_{3\text{Im}}) \cdot (-p_{1\text{Re}} - jp_{1\text{Im}} + p_{3\text{Re}} + jp_{3\text{Im}})} = |R_1| e^{-j\psi_{R1}} \\
 \hat{R}_3 &= (s - p_3) I_1(s) \Big|_{s=p_3} = \frac{a_3 p_3^2 + a_2 p_3 + a_1}{(p_3 - p_1)(p_3 - p_2) \cdot (p_3 - p_4)} = \\
 &= \frac{a_3(-p_{3\text{Re}} + jp_{3\text{Im}})^2 + a_2(-p_{3\text{Re}} + jp_{3\text{Im}}) + a_1}{(-p_{3\text{Re}} + jp_{3\text{Im}} + p_{1\text{Re}} - jp_{1\text{Im}})(-p_{3\text{Re}} + jp_{3\text{Im}} + p_{1\text{Re}} + jp_{1\text{Im}}) \cdot (-p_{3\text{Re}} + jp_{3\text{Im}} + p_{3\text{Re}} + jp_{3\text{Im}})} = \\
 &= \frac{a_3(-p_{3\text{Re}} + jp_{3\text{Im}})^2 + a_2(-p_{3\text{Re}} + jp_{3\text{Im}}) + a_1}{j 2 p_{3\text{Im}} (-p_{3\text{Re}} + jp_{3\text{Im}} + p_{1\text{Re}} - jp_{1\text{Im}}) \cdot (-p_{3\text{Re}} + jp_{3\text{Im}} + p_{1\text{Re}} + jp_{1\text{Im}})} = |R_3| e^{j\psi_{R3}} \\
 \hat{R}_4 &= (s - p_4) I_1(s) \Big|_{s=p_4} = \frac{a_3 p_4^2 + a_2 p_4 + a_1}{(p_4 - p_1)(p_4 - p_2) \cdot (p_4 - p_3)} = \\
 &= \frac{a_3(-p_{3\text{Re}} - jp_{3\text{Im}})^2 + a_2(-p_{3\text{Re}} - jp_{3\text{Im}}) + a_1}{(-p_{3\text{Re}} - jp_{3\text{Im}} + p_{1\text{Re}} - jp_{1\text{Im}})(-p_{3\text{Re}} - jp_{3\text{Im}} + p_{1\text{Re}} + jp_{1\text{Im}}) \cdot (-p_{3\text{Re}} - jp_{3\text{Im}} + p_{3\text{Re}} - jp_{3\text{Im}})} = \\
 &= \frac{a_3(-p_{3\text{Re}} - jp_{3\text{Im}})^2 + a_2(-p_{3\text{Re}} - jp_{3\text{Im}}) + a_1}{-j 2 p_{3\text{Im}} (-p_{3\text{Re}} - jp_{3\text{Im}} + p_{1\text{Re}} - jp_{1\text{Im}}) \cdot (-p_{3\text{Re}} + jp_{3\text{Im}} + p_{1\text{Re}} + jp_{1\text{Im}})} = |R_3| e^{-j\psi_{R3}} \\
 I_1(s) &= U \left\{ \frac{\hat{R}_1}{(s + p_{1\text{Re}} - jp_{1\text{Im}})} + \frac{\hat{R}_2}{(s + p_{1\text{Re}} + jp_{1\text{Im}})} + \frac{\hat{R}_3}{(s + p_{3\text{Re}} - jp_{3\text{Im}})} + \frac{\hat{R}_4}{(s + p_{3\text{Re}} + jp_{3\text{Im}})} \right\} = \\
 &= U \left\{ \frac{|R_1| e^{j\psi_{R1}}}{(s + p_{1\text{Re}} - jp_{1\text{Im}})} + \frac{|R_1| e^{-j\psi_{R1}}}{(s + p_{1\text{Re}} + jp_{1\text{Im}})} + \frac{|R_3| e^{j\psi_{R3}}}{(s + p_{3\text{Re}} - jp_{3\text{Im}})} + \frac{|R_3| e^{-j\psi_{R3}}}{(s + p_{3\text{Re}} + jp_{3\text{Im}})} \right\}
 \end{aligned}$$

Using the inverse Laplace transform:

$$Ae^{\sigma t} \cos(\omega t + \phi) \cdot 1(t) \Leftrightarrow \frac{\frac{1}{2} A e^{j\phi}}{s - \sigma + j\omega} + \frac{\frac{1}{2} A e^{-j\phi}}{s - \sigma - j\omega}$$

$$I_1(s) = U \left\{ \frac{|R_1|e^{j\psi_{R1}}}{(s + p_{1Re} - jp_{1Im})} + \frac{|R_1|e^{-j\psi_{R1}}}{(s + p_{1Re} + jp_{1Im})} + \frac{|R_3|e^{j\psi_{R3}}}{(s + p_{3Re} - jp_{3Im})} + \frac{|R_3|e^{-j\psi_{R3}}}{(s + p_{3Re} + jp_{3Im})} \right\}$$

We get a sum of two fading oscillations:

$$i_1(t) = 2U \{ |R_1|e^{-p_{1Re}t} \cos(p_{1Im}t + \psi_{R1}) + |R_3|e^{-p_{3Re}t} \cos(p_{3Im}t + \psi_{R3}) \}$$

The resulting resonant current shape can be observed in Fig. 4.5, which is the result of SPICE simulation.

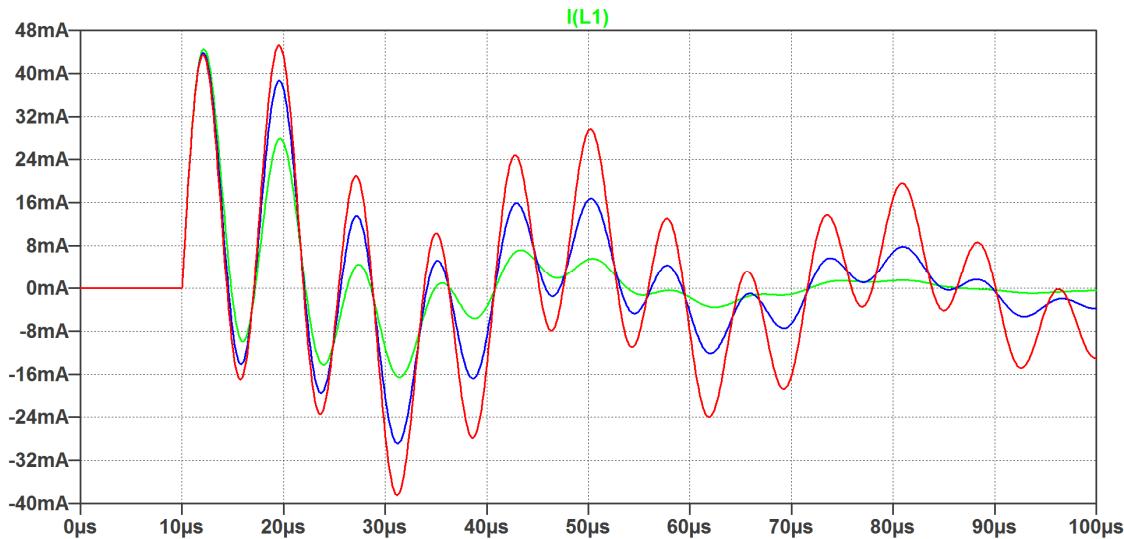


Fig. 4.5 Series-parallel LCLC resonant tank step response for various load values

It is worth noting that the resulting equation for step response of a simple RLC circuit is quite complex and only because the coefficients are grouped it is possible to understand the impact of each of the component values to the resonant circuit response. In case of the LCLC resonant tank, even if the formula for the step response was fully derived, the resulting equation would be so complex that it would be of no practical use. This suggests that a predictive control system will be hard to develop and reactive control is more preferred.

4.3 Summary

In the chapter a new concept of SCS control method has been introduced. The method improves light load efficiency by reducing the amount of switching cycles (switching losses reduction) and the average frequency and amplitude of the resonant current (copper and core loss reduction). The simplified operation is discussed and several problems have been highlighted (resonant current sustain and synchronization with resonant current). The most difficult task is proper synchronization with the resonant current since the step response is a sum of two fading oscillations. This fact is confirmed by a simplified analysis and simulation results.

5 Test Platform

In order to validate the proposed control method a test platform has been prepared. The block schematic of the test platform is presented in Fig. 5.1.

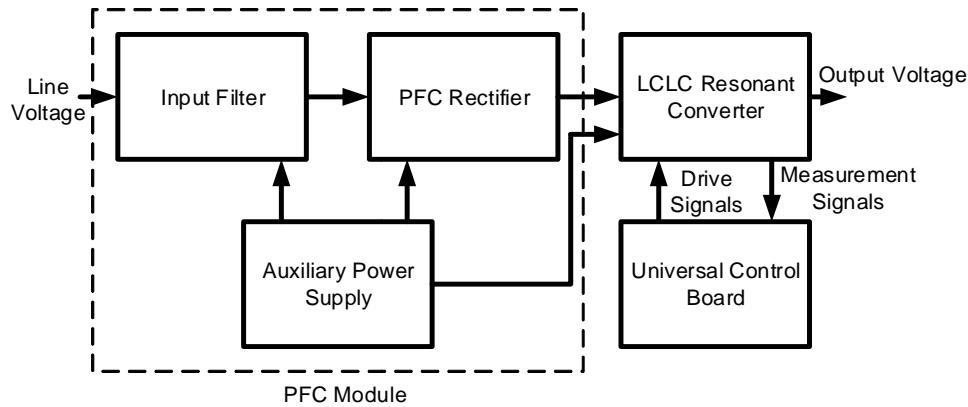


Fig. 5.1 Block schematic of the test platform

It consists of a 3kW power supply and a separate universal control board. A photograph of the test platform setup is presented in Fig. 5.2.

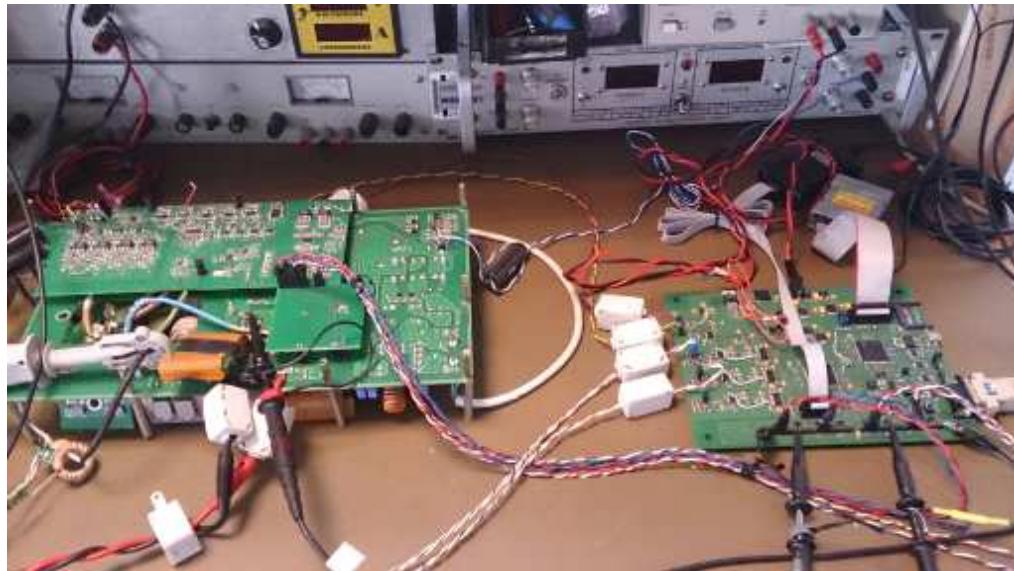


Fig. 5.2 Test platform setup

The power supply consists of a PFC rectifier (including an EMI input filter) and a DC-DC full-bridge class DE LCLC resonant converter. This chapter will briefly discuss the parameters of the test platform.

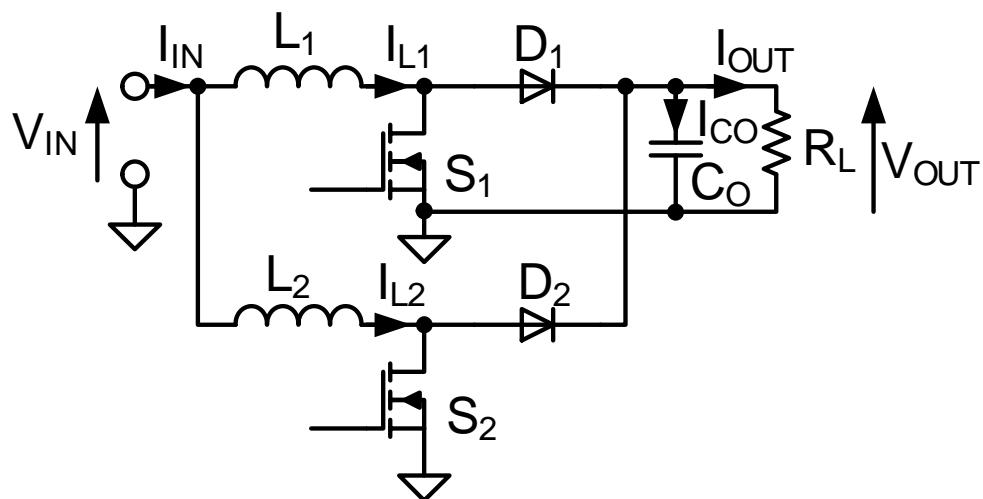
5.1 Active Power Factor Correction Module

In order to pass the current EN61000-3-2 EMC regulations and provide a wide input voltage range it is necessary to include a Power Factor Correction rectifier. Aiming for high efficiency, a two-phase interleaved topology has been chosen. The basic parameters are presented in TABLE 5.1.

TABLE 5.1 Basic parameters of the PFC rectifier

Input Voltage	85VAC-260VAC
PFC Rectifier Output Voltage	390VDC
PFC Rectifier Output Power	3000W
Switching Frequency	80kHz-120kHz
Peak Efficiency	97% (including the input filter)

The PFC rectifier is built using the Texas Instruments UCC28070 two-phase interleaved PFC controller. A simplified schematic of a two phase interleaving boost converter is presented in Fig. 5.3.


Fig. 5.3 Simplified schematic of two-phase interleaving PFC boost converter.

The interleaved boost converter is created from two classic boost converters connected in parallel and operating with a 180° phase shift. As it is shown in Fig. 5.3, the input current is a sum of two inductor currents (I_{L1} and I_{L2}). Since the two boosts operate with a 180° phase shift, the maximum of the I_{L1} is at the same time as the minimum of I_{L2} (and vice versa). If the currents are summed up, the input current ripple will be reduced in comparison to the single boost construction. The best cancellation occurs at 50% duty cycle operation. A similar behavior occurs with the output ripple current. Because of the 180° phase shift operation the output capacitor ripple current is reduced from the sum of the output currents I_{D1} , I_{D2} . An example of operating waveforms are depicted in Fig. 5.4.

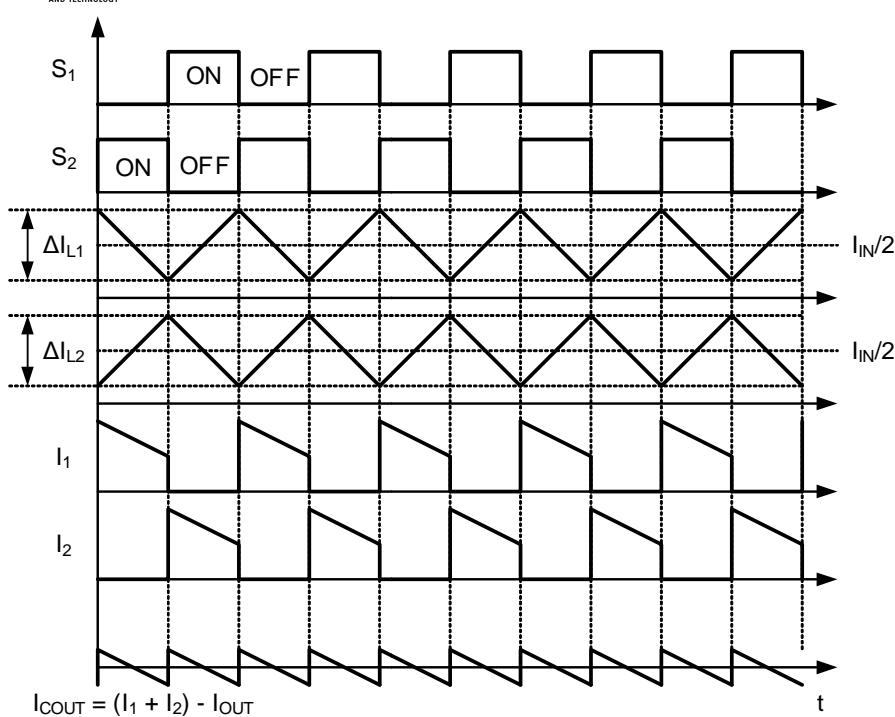


Fig. 5.4 Typical waveforms for two-phase interleaved boost converter

The above mentioned features allow to reduce the size of the input filter and output capacitor. This will improve the overall efficiency of the PFC rectifier. The results of the PFC rectifier efficiency measurements are presented in Fig. 5.5. The measurements have been performed using the Yokogawa WT3000 precision power analyzer.

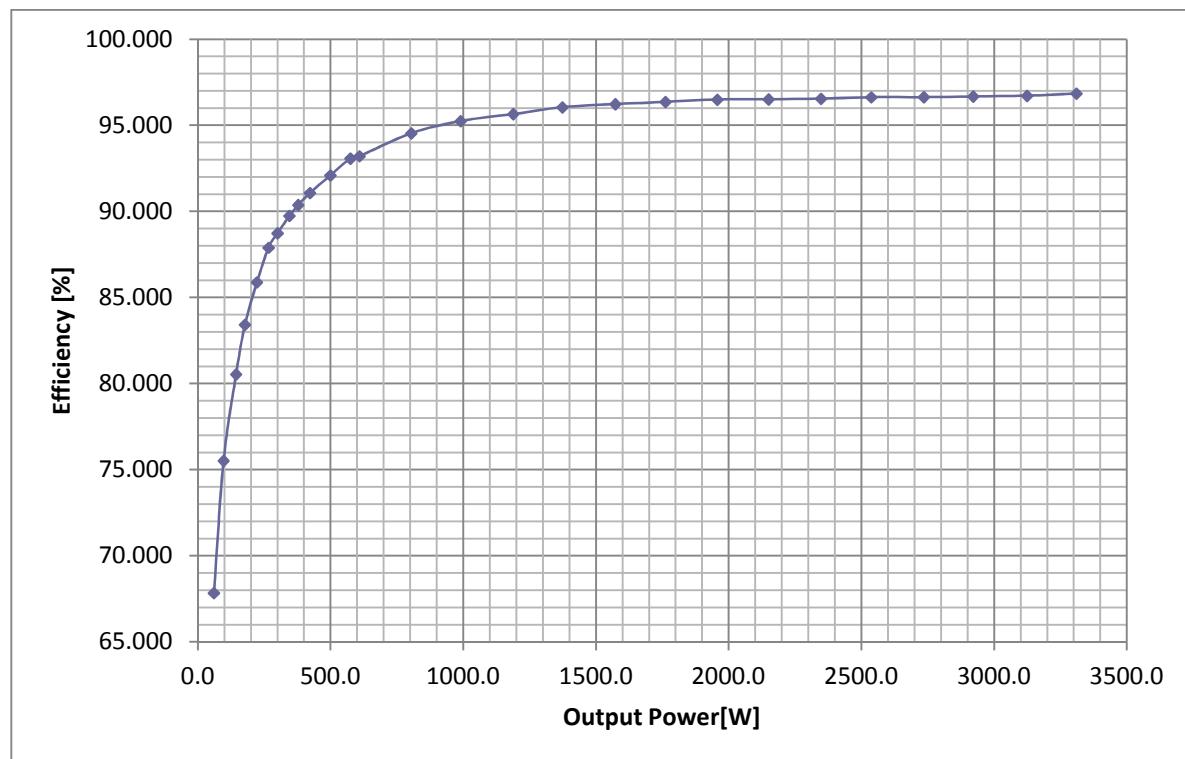


Fig. 5.5 PFC rectifier efficiency vs output power (including the input filter)

The PFC rectifier achieves 96.85% peak efficiency, including the input filter and auxiliary power supply.

5.2 LCLC Resonant DC-DC Converter

The chosen topology for the DC-DC converter is the class DE full-bridge LCLC resonant converter. The basic information is provided in TABLE 5.2 and the simplified schematic is presented in Fig. 5.6.

TABLE 5.2 Basic parameters of the DC-DC resonant converter

Input Voltage	370VDC-420VDC
Output Voltage	48VDC
Output Current	62ADC
Output Power	3000W
Switching Frequency	145kHz - 190kHz

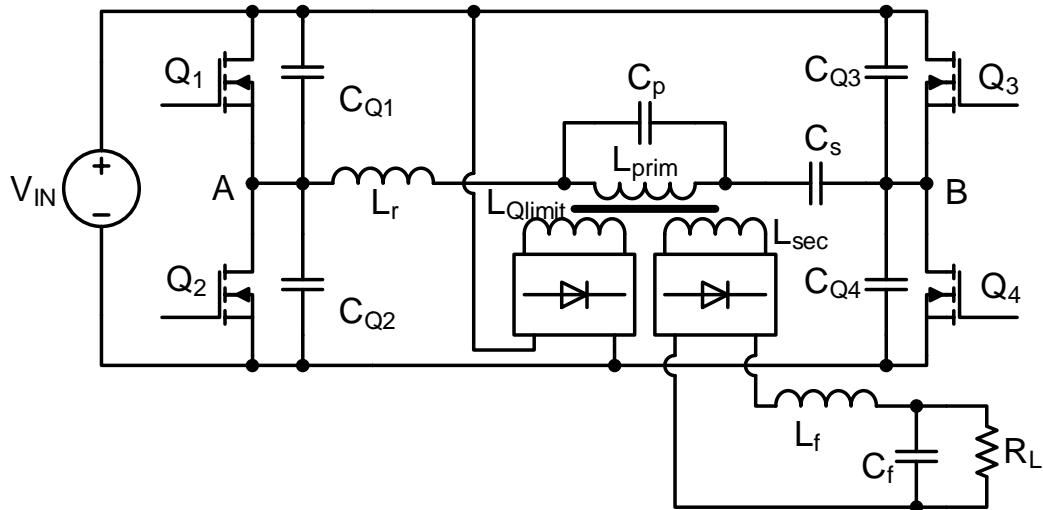


Fig. 5.6 Simplified schematic of Class DE Full-bridge LCLC resonant DC-DC converter.

The diodes $D_{Q1}, D_{Q2}, D_{Q3}, D_{Q4}$ along with the winding $L_{Q\text{limit}}$ form a protection circuit that reduced the quality factor of the resonant tank in unwanted areas of operation (e.g. light load operation with low operating frequency). The idea is, that when the voltage across $L_{Q\text{limit}}$ will be larger than the supply voltage, the diode bridge will start to conduct and the excess energy existing in the resonant tank will be returned to the supply capacitor. This ensures that the voltage across the resonant tank components will stay in the safe operating area, thus protecting the circuit.

The output stage is a center-tapped rectifier, which will help in achieving higher efficiencies and will also reduce the number of required rectifier diodes.

TABLE 5.3 Resonant converter component values

Q_1, Q_2, Q_3, Q_4	SPW35N60CFD
$C_{Q1}, C_{Q2}, C_{Q3}, C_{Q4}$	2.2nF
C_s	50nF
C_p	50nF
L_r	72uH

L_{prim}	60uH
n_{sec}	10/1
n_Q	10/6
D_{01}, D_{02}	DSA90C200HB
C_{out}	1500uF

The resonant tank components are presented in Fig. 5.7. The resonant inductors have been constructed using the Integrated Magnetic Component technique. This kind of construction helps in component size reduction and improves efficiency. A detailed description of this component can be found in [4], [5], [6]. The resonant tank inductances and capacitances are presented in Fig. 5.7.

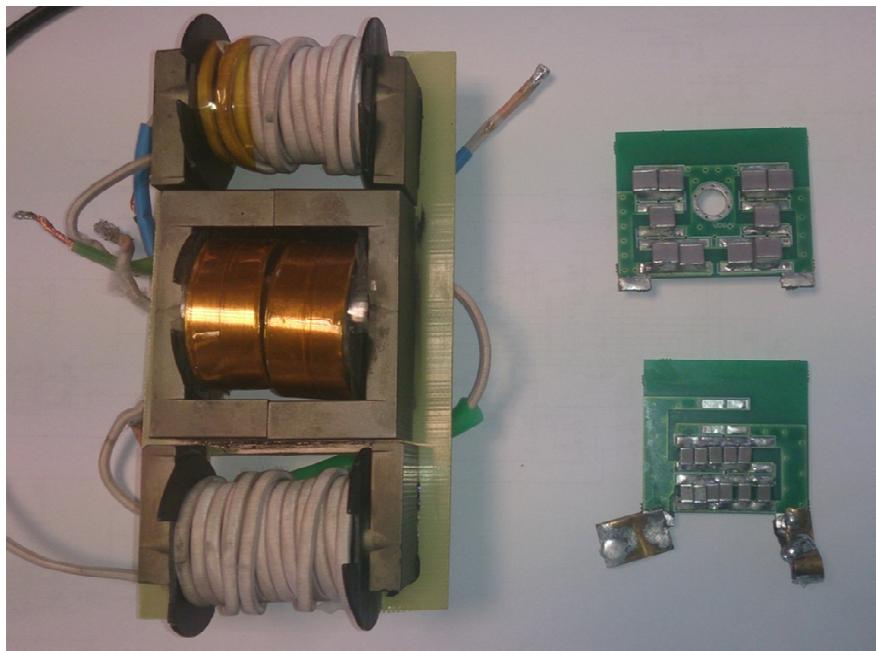


Fig. 5.7 Resonant tank inductors (left) and capacitors (right)

The simulated impedance characteristics of the built LCLC resonant tank are presented in Fig. 5.8.

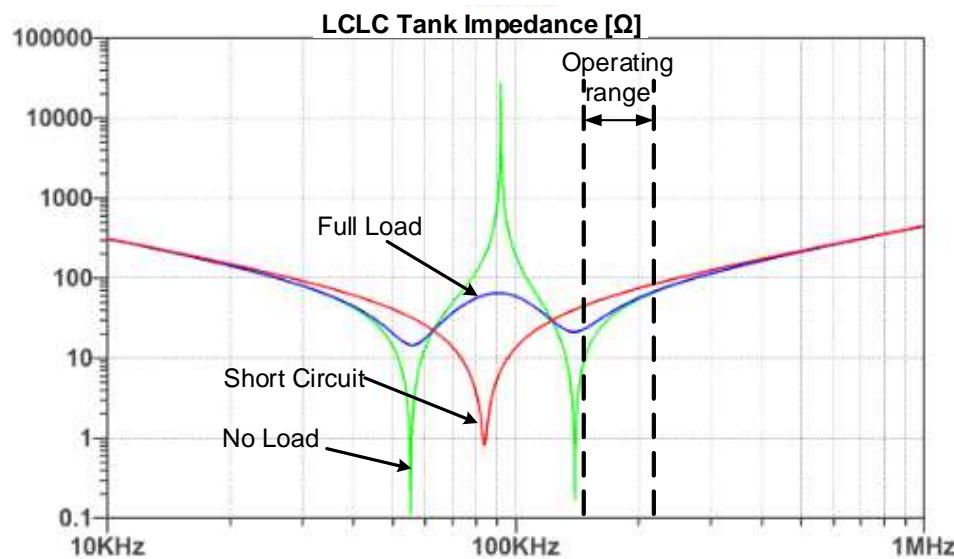


Fig. 5.8 Impedance vs frequency of LCLC resonant tank

The resulting LCLC resonant tank impedance is designed in such a way that it will reduce the resonant current during load short circuit, thus limiting the output current to a constant value. The resulting operating frequency is 144kHz to 190kHz.

5.3 Universal Control Board for Resonant Converters

In order to verify different control method proposals a universal control board has been designed and constructed. The design has been based on previous work [55], however the hardware has been modified and software has been rewritten completely. The main part of the universal control board is a Cyclone III FPGA with three ADC 12bit 40MSPS channels and two ADC 12bit 250kSPS channels. A simplified block schematic of the universal control board is presented in Fig. 5.9.

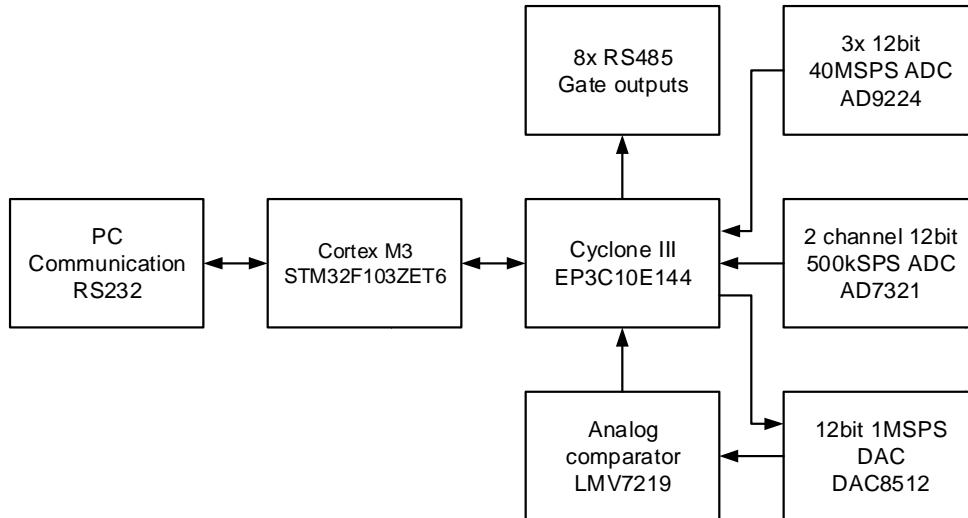


Fig. 5.9 Universal control board block schematic

In addition to these resources there are also 8 RS485 channels for transistors' gates driving signals, one 12bit DAC and one fast comparator. To make supervision and external communication easier a ARM microcontroller has been also included.

5.4 Measurement Circuits

Several parameters of the resonant converter are measured. These include: output voltage, output current, resonant current, resonant current derivative and resonant current cyclic RMS value. The measurement circuits for the mentioned parameters will be presented in this subchapter.

5.4.1 Output Parameters Measurement Circuits

The output voltage is measured using a 12bit 250kSps ADC. In order to reduce aliasing effects a second-order low pass filter is inserted at the input of the analog to digital converter. The schematic for the output voltage measurement path is presented in Fig. 5.10. The output voltage, divided by R_{D1} and R_{D2} , is fed into a 2nd order Butterworth low pass filter. The low pass filter is constructed using Sallen-Key topology.

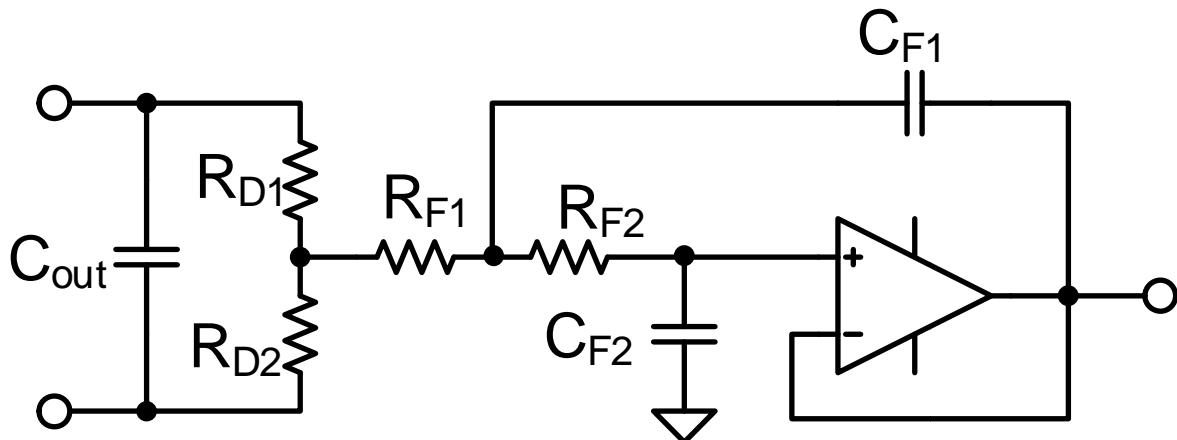


Fig. 5.10 Output voltage measurement circuit

The filter cutoff frequency has been set to around 10kHz. The measurement path AC transfer characteristic is presented in Fig. 5.11

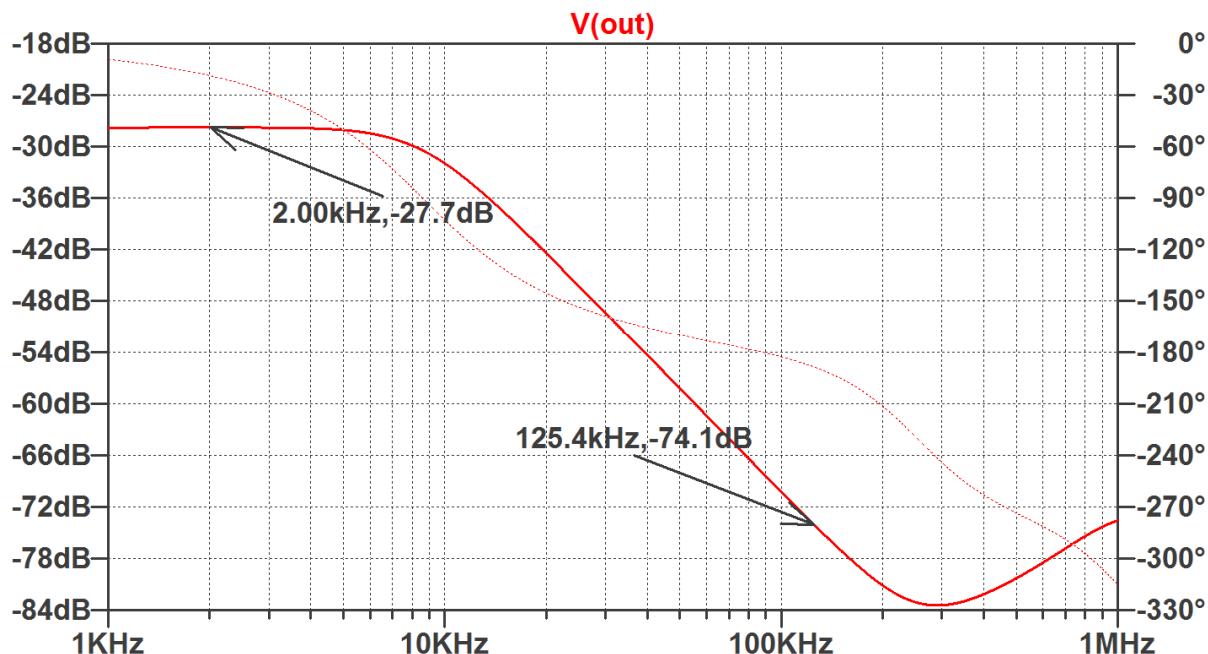


Fig. 5.11 Output voltage measurement path AC transfer characteristics vs frequency

In order to avoid aliasing for a 12bit resolution, a -74dB attenuation is needed at Nyquist frequency. The resulting component values are presented in TABLE 5.4.

TABLE 5.4 Voltage measurement component values

RD1	47kΩ
RD2	2kΩ
RF1	8.2kΩ
RF2	15kΩ
CF1	2.2nF
CF2	1nF

The output current is measured using a $R_{SH}=1\text{m}\Omega$ shunt resistor. The voltage is amplified and then fed into a 12b 250kSps ADC through identical low pass filter as in the output voltage measurement path. The schematic for the current measurement path is presented in Fig. 5.12.

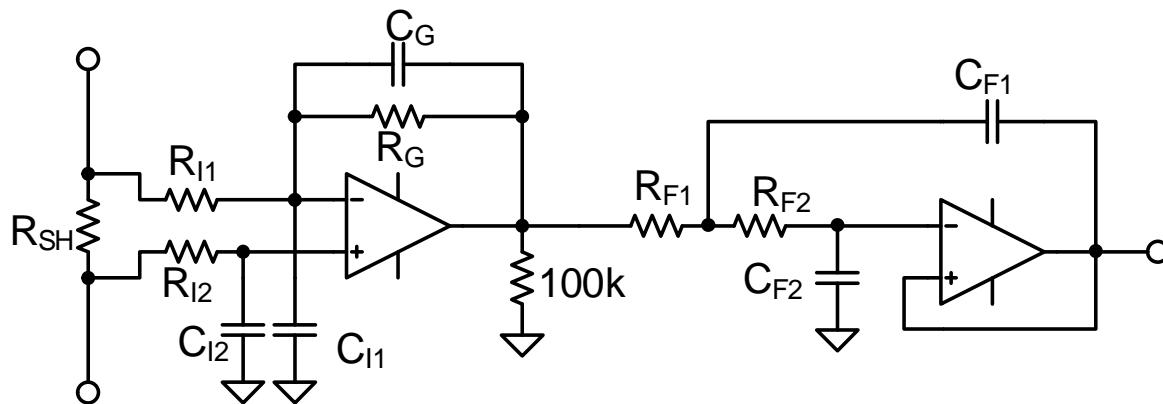


Fig. 5.12 Output current measurement circuit

The filter values are the same as in the voltage measurement track. The measurement path AC transfer characteristic is presented in Fig. 5.13.

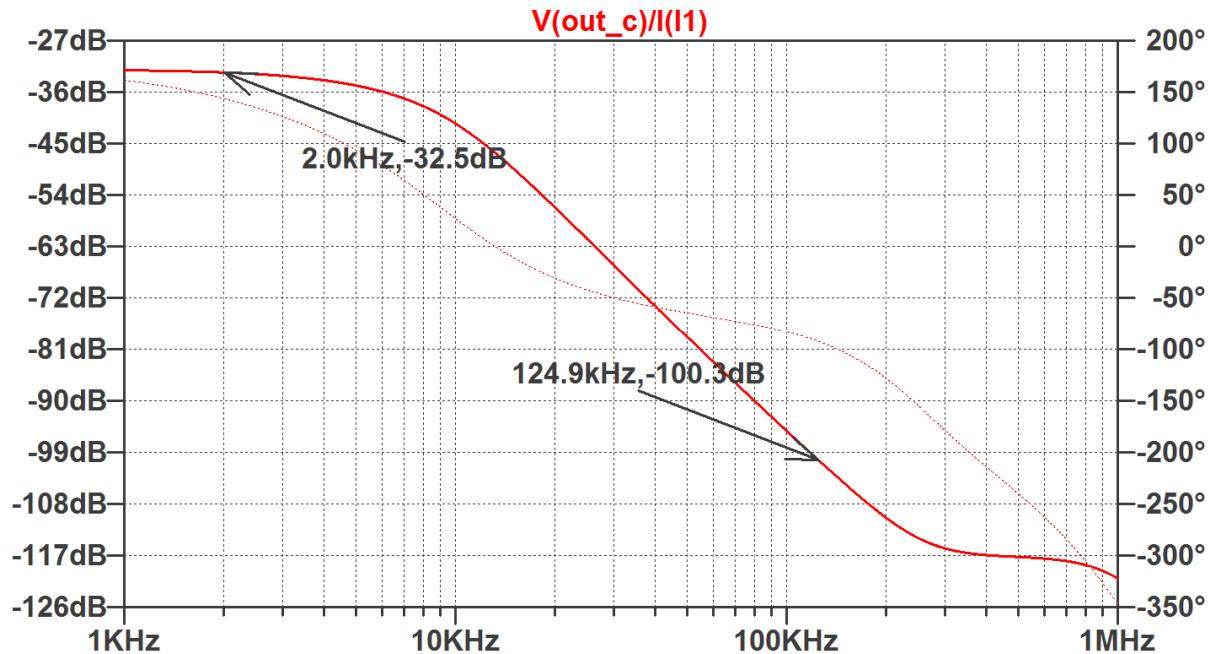


Fig. 5.13 Output current measurement path AC transfer characteristics vs frequency

Since we have information about the output voltage and output current it is possible to estimate the instantaneous output power using straight multiplication of these two values. The result bit length will be twice the length of the input values. Because of this only the most significant bits of the resulting power are stored.

5.4.2 Resonant Current Measurements

As mentioned in chapter 4.1 it is necessary to measure the instantaneous value of the resonant current. The resonant current has a quasi-sinusoidal shape and has no DC component. Because of

this, a current transformer is fitting as a measuring device. Additionally the current transformer provides the necessary isolation from high voltage existing on the primary side. The schematic for the measurement path is presented in Fig. 5.14.

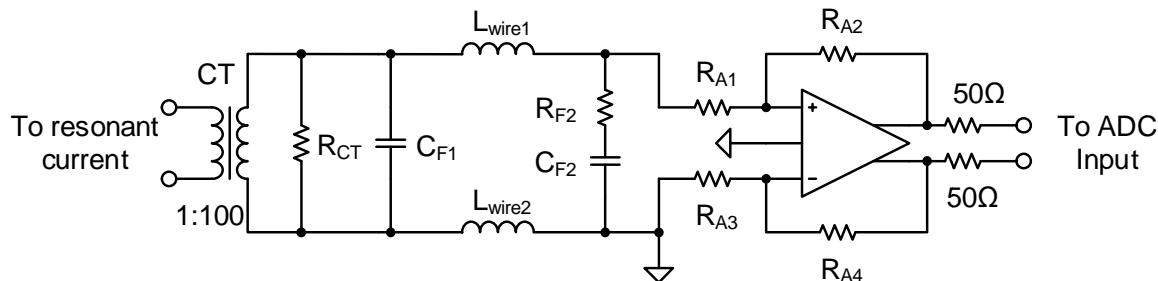


Fig. 5.14 Resonant current measurement circuit

The resonant current is sampled with a 12bit 40MSps AD converter. The cutoff frequency has been set to 10MHz in order to reduce the effects of aliasing.

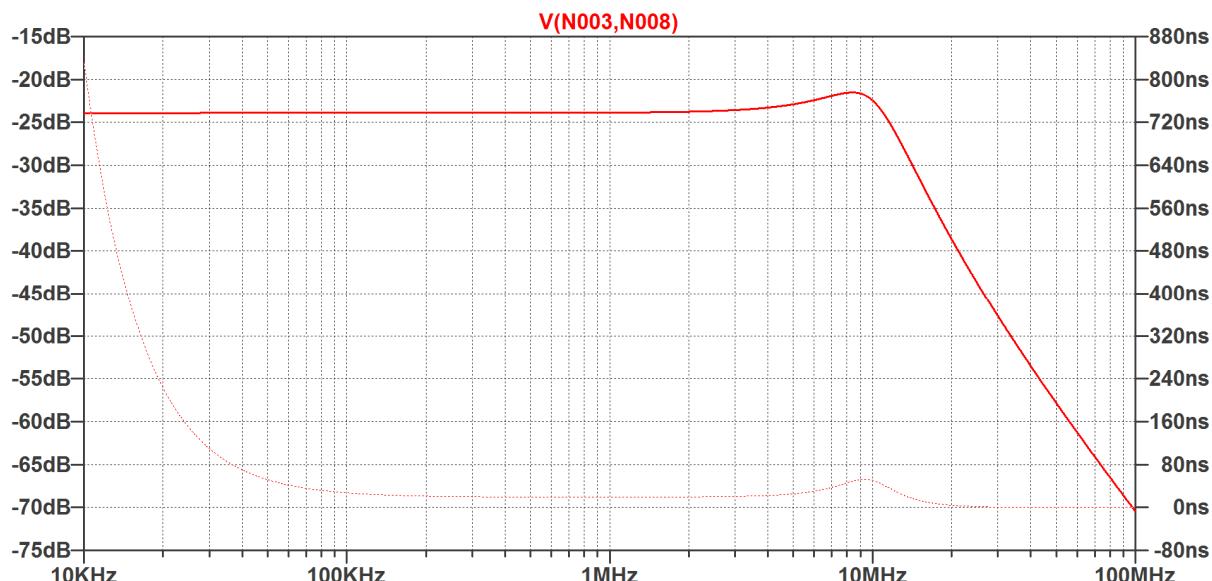


Fig. 5.15 Resonant current transfer function and group delay vs frequency

Apart from the resonant current value, the resonant current derivative is also measured. In current application it is achieved by using a custom made Rogowski coil. The voltage across the Rogowski coil terminals is proportional to the rate of change of the current flow through the inside of the coil. In other words, the voltage across the coil is proportional to the time derivative of the measured current. A photograph of the constructed Rogowski coil is shown in Fig. 5.16 and the schematic for the measurement path is shown in Fig. 5.17.



Fig. 5.16 Current transformer (left), Rogowski coil (right)

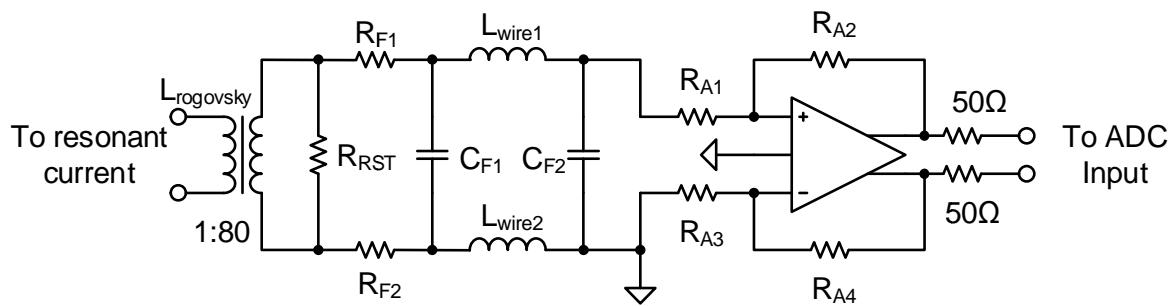


Fig. 5.17 Resonant current derivative measurement circuit

The resonant current derivative is sampled using a 12bit 40MSps AD converter. In future development, a digital approach to obtain the resonant current derivative should be considered. The transfer function and group delay of the measurement path is shown in Fig. 5.18. The circuit gives proper derivative information for signals up to around 1MHz, which should be sufficient for the used application.



Fig. 5.18 Resonant current derivative transfer function and group delay vs frequency

The voltage across the Rogowski coil terminals is given by:

$$v(t) = \frac{-AN\mu_0}{l_e} \frac{di}{dt}$$

where A is the area of one coil turn, N is the number of turns, μ_0 is the magnetic permeability, l_e is the toroidal coil effective length and i is the measured current. The constructed coil has 80 turns and for a 100kHz 1A sinusoidal input signal shall produce 10.6mV output voltage.

Another measured parameter is the CRMS value of the resonant current. This parameter is calculated directly from the sampled resonant current values. This information is used for determining whether the resonant current amplitude has fallen below acceptable value, so that proper actions can be performed (i.e. perform several switching cycles in order to increase the resonant current amplitude). The block schematic for the FPGA circuit for CRMS calculation is presented in Fig. 5.19.

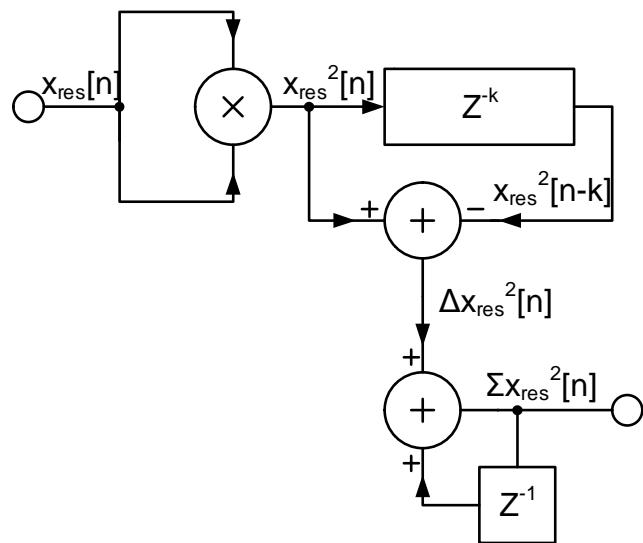


Fig. 5.19 Cyclic RMS calculation schematic

From the definition of the CRMS of a sampled function we have:

$$x_{RMS}[n] = \sqrt{\frac{1}{k} (x[n]^2 + x[n-1]^2 + \dots + x[n-k]^2)}$$

$$k \cdot x_{RMS}[n]^2 = x[n]^2 + x[n-1]^2 + \dots + x[n-k]^2$$

Also:

$$k \cdot x_{RMS}[n+1]^2 = x[n+1]^2 + x[n]^2 + \dots + x[n-k+1]^2$$

$$k \cdot x_{RMS}[n+1]^2 = x[n+1]^2 + (x[n]^2 + \dots + x[n-k+1]^2 + x[n-k]^2) - x[n-k]^2$$

$$k \cdot x_{RMS}[n+1]^2 = x[n+1]^2 + k \cdot x_{RMS}[n+1]^2 - x[n-k]^2$$

Since the CRMS value is only used for level comparison and the reference value is constant it is easier to scale the value of the reference instead of performing division by k and then the square root operation (which consumes relatively large amount of resources). Thus, we can compute the necessary information using only one multiplier, two adders and a simple shift buffer.

Apart from the CRMS value, the frequency of the resonant current is sensed. Currently this information is used only as an indicator. The frequency value is obtained by the detection of the time between the resonant current zero crossings. By having the information about the length of the half-period, the frequency can be easily computed.

There are four control signals generated from the resonant current measurements:

- Resonant Current Positive,
- Resonant Current Negative,
- Resonant Current Derivative Positive,
- Resonant Current Derivative Negative.

These signals are used for the synchronization with the resonant current. The Resonant Current Positive signal is created by comparing the resonant current values with a preset threshold. Additionally, a customizable hysteresis has been implemented to reduce ringing during the transitions. The rest of the signals are generated in the same way, with respect, that each of them has its own threshold value.

5.5 Summary

In the chapter the test platform has been presented to verify the proposed method. The test platform consists of a 3kW resonant power supply and a universal control board. The power supply consists of a EMI input filter, PFC rectifier, auxiliary power supply and a DC-DC resonant power converter. The basic parameters of the main block are presented. Since the universal control board needs some information about the state of the DC-DC resonant converter, several parameters are measured. The required parameters are: output voltage, output current, resonant current and resonant current derivative. The measurement path for each parameter is presented and briefly analyzed.

6 Digital Control Implementations

In order to verify the novel control method concept and provide a benchmark reference, two algorithms have been implemented in the FPGA, i.e.: Digital Frequency Modulation Control and Digital Sequential Cycle Stealing Control (SCSC). In the chapter the digital implementations of these two control algorithms are presented and discussed.

6.1 Digital Frequency Modulation

The analog FM control is by far most common technique used in today's resonant converters [56], [57], [58], [59], [60]. Since this method is so widely spread it feels natural to use it as a benchmark for comparison. To ensure the same operating conditions for both FM Control and SCSC, a frequency modulation controller has been implemented in the FPGA. The block schematic for this implementation is shown in Fig. 6.1.

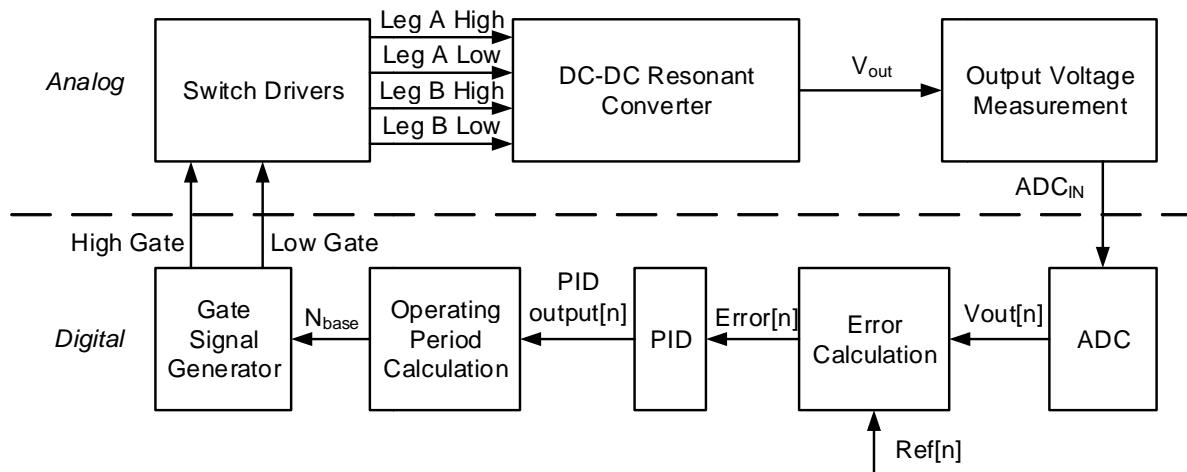


Fig. 6.1 Block schematic of FPGA Digital FM Controller

The regulated parameter is the rectified output voltage of the converter. The whole feedback loop is fully implemented in digital form. The sensed output voltage value is subtracted from a reference value in order to get the current voltage error value. The error value is being input into a PID regulator and then the new value of the operating period (represented by the number of clock cycles) is calculated from output of the PID regulator. This new period value (N_{base}) is then used by the switch gate signal generator, which will then insert the desired dead time into the gate drive signal.

The schematic of a classic PID regulator in parallel form is presented in Fig. 6.2.

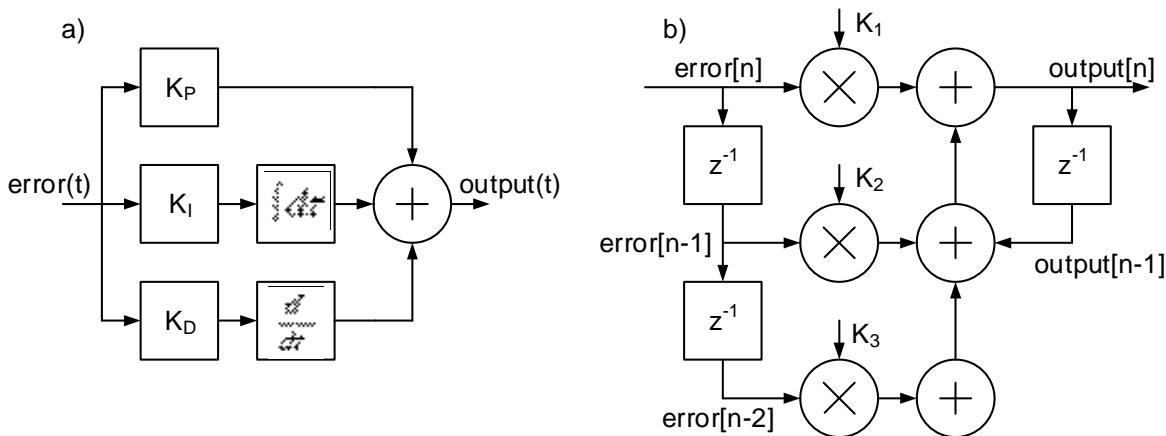


Fig. 6.2 PID regulator schematic: a) continuous time implementation, b) converted discrete time implementation

From Fig. 6.2a we can write the standard PID regulator equation in parallel form:

$$output(t) = K_P \cdot error(t) + K_I \cdot \int error(\tau) d\tau + K_D \cdot \frac{d}{dt} error(t)$$

Using the Laplace transform:

$$G(s) = K_P + \frac{K_I}{s} + sK_D$$

If we want to go to the discrete time domain we must find the equations for discrete integral and discrete derivative. The difference equation for the integral is:

$$u(n) = u(n-1) + f(n) \cdot T_{samp}$$

Moving to z domain:

$$U(z) = U(z)z^{-1} + F(z) \cdot T_{samp}$$

$$U(z)(1 - z^{-1}) = F(z) \cdot T_{samp}$$

$$U(z) = \frac{F(z) \cdot T_{samp}}{1 - z^{-1}}$$

Which yields the formula for integral in z domain. Similarly with derivative:

$$u(n) = \frac{f(n) - f(n-1)}{T_{samp}}$$

$$U(z) = \frac{F(z) - F(z)z^{-1}}{T_{samp}}$$

$$U(z) = \frac{F(z)(1-z^{-1})}{T_{\text{samp}}}$$

Yielding the formula for the derivative in z domain. Using () and () we can write the PID difference equation in z domain:

$$U(z) = \left(K_P + \frac{K_I T_{\text{samp}}}{1-z^{-1}} + \frac{K_D}{T_{\text{samp}}} (1-z^{-1}) \right) E(z)$$

$$U(z) = \left[\frac{\left(K_P + K_I T_{\text{samp}} + \frac{K_D}{T_{\text{samp}}} \right) + \left(-K_P - 2 \frac{K_D}{T_{\text{samp}}} \right) z^{-1} + \frac{K_D}{T_{\text{samp}}} z^{-2}}{1-z^{-1}} \right] E(z)$$

We can define the following coefficients

$$K_1 = K_P + K_I T_{\text{samp}} + \frac{K_D}{T_{\text{samp}}}$$

$$K_2 = -K_P - 2 \frac{K_D}{T_{\text{samp}}}$$

$$K_3 = \frac{K_D}{T_{\text{samp}}}$$

From () and () we can write:

$$U(z) = U(z)z^{-1} + K_1 E(z) + K_2 E(z)z^{-1} + K_3 E(z)z^{-2}$$

$$\text{output}(n) = \text{output}(n-1) + K_1 \text{error}(n) + K_2 \text{error}(n-1) + K_3 \text{error}(n-2)$$

The difference equation above will be used to implement the discrete time PID regulator in the FPGA. The schematic of this implementation is shown in Fig. 6.2b. The implementation prevents the regulator from overflow by incorporating the saturation arithmetic.

Since the output of the PID cannot be used directly to drive the switch gate signal generator it should be scaled first into a useful value. Usually, a resonant converter operates within a defined range of frequencies (i.e. minimum and maximum operating frequency). Also, we can observe that the resonant converter delivers more energy at lower frequencies and less energy if the operating frequency rises. Thus, it seems natural to scale the PID output in such a way, that when it reaches its minimal boundary (i.e. the output voltage is too low), the converter should operate at minimal frequency. Similarly, when the PID output is at its maximum (i.e. the output voltage is too high) the converter should operate at its maximum frequency.

The last piece of the control loop is the switch gate signal generator. It is a four state machine that represents the possible states of the switching half- or full-bridge. The states are: Active High Switch, Dead Time After High Switch, Active Low Switch and Dead Time After Low Switch. Depending on the current state, proper gate signals are driven to the switches. The state machine graph is presented in Fig. 6.3.

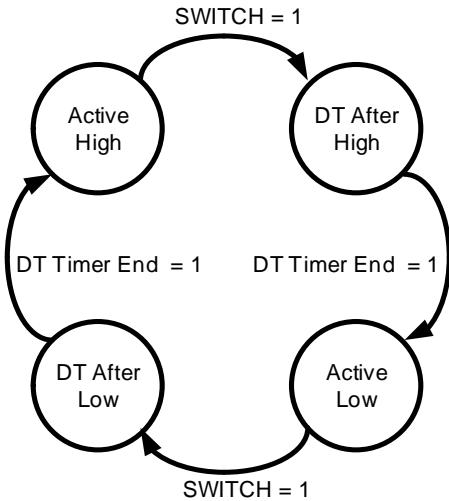


Fig. 6.3 Switch gate signal generator state machine graph

The state machine is driven by two timers. One is used for generating half of the operating period and the other for dead time generation. The operating period timer cyclically counts up to a value and when finished it sets the SWITCH signal to '1' for a single clock cycle. The state machine then transitions into one of the dead time states and concurrently the dead time counter starts. After reaching a preset dead time clock ticks the signal DT TIMER END is set to 1 for a single clock cycle. The state machine then proceeds into one of the active states. The block schematic of the complete signal generator is presented in Fig. 6.4.

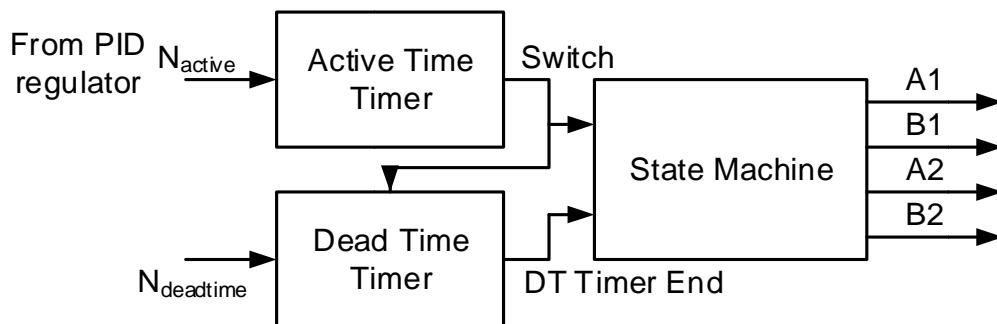


Fig. 6.4 Switch gate signal generator block schematic

The frequency resolution of such system varies with the operating frequency. For a certain generated operating frequency we can write:

$$f_{op} = \frac{1}{N_{period} T_{clk}}$$

However the generator has to generate the control signal for both switches, which means that in reality it is generating half period ticks. Hence:

$$f_{op} = \frac{1}{2N_{active}T_{clk}}$$

If we want to calculate the frequency resolution, we can write:

$$\Delta f_{op} = \frac{1}{2(N_{active}-1)T_{clk}} - \frac{1}{2N_{active}T_{clk}}$$

$$\Delta f_{op} = \frac{N_{active} - (N_{active} - 1)}{4N_{active}(N_{active} - 1)T_{clk}} \approx \frac{1}{4N_{active}^2 T_{clk}} = f_{op}^2 T_{clk}$$

In the constructed generator the $T_{clk} = 200\text{MHz}$, and the converter operating frequency range is roughly from 150kHz to 190kHz. Thus, the frequency resolution of the system changes from 112.5Hz at low frequency to 180.5Hz at high frequency. In [30] authors show that in resonant converters with digital FM there is a risk of limit cycles phenomenon occurrence. This phenomenon manifests itself as oscillations at the output of the converter (and indirectly in the resonant current amplitude level oscillations). Such oscillations can occur when the variation of the output due to the LSB change of the control is larger than the resolution of the AD converter used to measure the output value. Since the oscillations only increase the output ripple and prevents from steady operation, care should be taken when designing the control loop.

6.2 Digital SCS

In chapter 4.1 a concept for SCS has been presented. This chapter will focus on the digital implementations details. The controller consists of a comparator, SCS state machine and switch gate signal generator. A simplified schematic for the resonant power supply with digital SCS controller is presented in Fig. 6.5. The comparator is used to generate the control signal STOP. The signal is set to '1' when the output voltage exceeds the reference level and is set to '0' otherwise. When $\text{STOP} = '0'$ the converter is switching and when $\text{STOP} = '1'$ the converter ceases to switch leaving one of the switches turned on (two switches in case of full-bridge) to allow free oscillations of the resonant circuit.

There are four control signals necessary for proper controller operation. These are: ResCurPos (resonant current positive), ResCurNeg (resonant current negative), DerCurPos (resonant current derivative positive) and DerCurNeg (resonant current derivative negative). These control signals are generated by comparators with adjustable level and hysteresis. The measurement paths for these signals have been described in chapter 5.4.

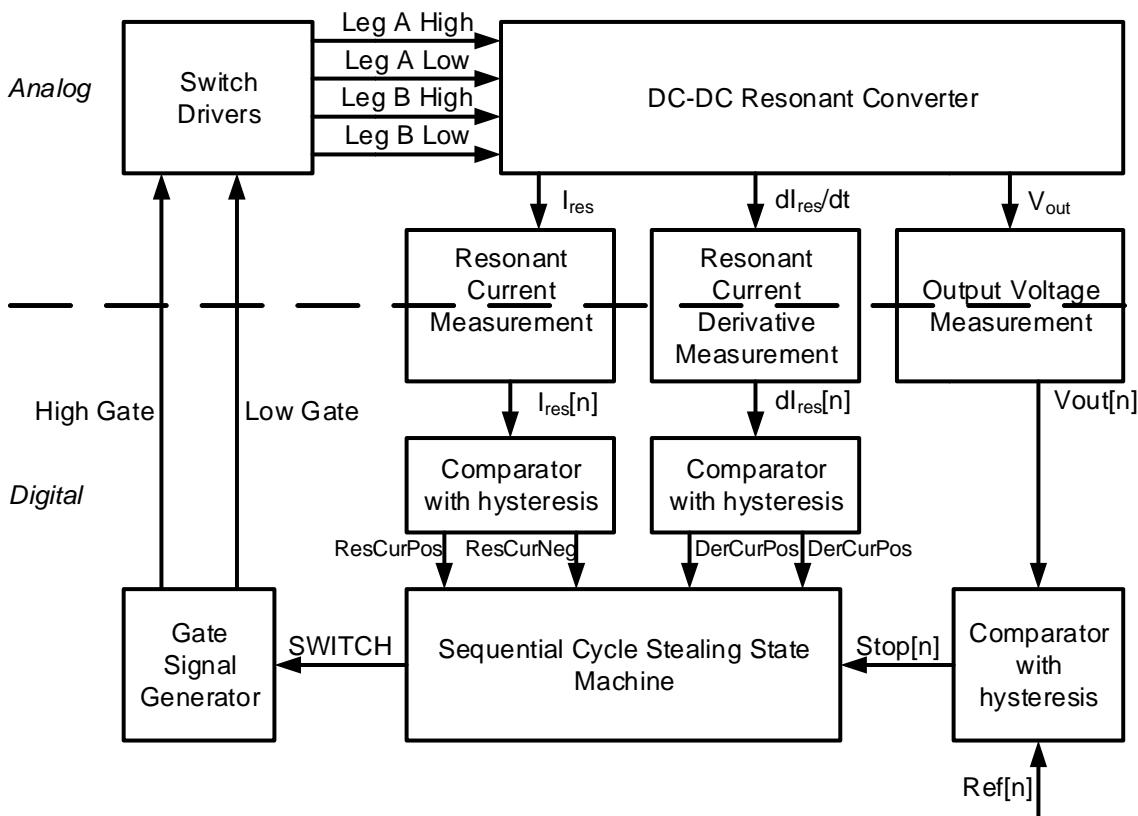


Fig. 6.5 Block schematic of FPGA Digital SCS Controller

The graph for the SCS State Machine has been presented in Fig. 6.6. There are 6 states available:

- Run,
- Stop,
- Sync,
- Restart,
- Sustain,
- Timeout.

In Run state the controller switches at a preselected constant frequency, thus delivering energy to the output. When the output voltage rises above comparator threshold the signal STOP changes to 1 and the controller enters Stop state. In this state the controller ceases to switch and one of the switches (two in case of full-bridge) is continuously turned on to allow for free oscillations in order to conserve energy. There are two possible conditions to leave this state. One is when the output voltage falls below the comparator threshold and the second is when the measures cyclic RMS value of the resonant current fall below a predefined level. In both cases the controller enters the Sync state. In this state the controller wait for proper switch conditions. Consider a half-bridge topology and a transition from low switch conduction to high switch conduction. The criteria chosen for proper soft switching in this case are as follows. The resonant current absolute value is above a preset threshold and the resonant current derivative is negative for low-high transition or is positive for high-low transition. In other words, for low-high transition the resonant current should be falling and its value should be below the negative threshold. Similarly, for high-low transition the resonant current should be rising and its value should be above positive threshold. If these conditions are met,

then the controller enters either Restart state or Sustain state (depending on the STOP signal value). In Restart state the controller can perform (depending on the settings) several synchronized switches or a preset pattern of switches. This is done in order to ensure proper switching conditions during the restart sequence. Should this sequence be omitted, some hard-switching may occur due to the nature of the step response of the LCLC resonant tank (which has been described in chapter 4.2). After the restart sequence finished the controller enters Run state and is switching constantly at a fixed frequency until STOP signal changes to 1 again. In the sustain state the controller can perform a similar pattern to this described in Restart state, however a single switch gives the best results. This is due to the fact that during Sustain state we don't want to deliver too much energy into the resonant circuit, because this will lead to overvoltage at the output of the converter at light loads. The last possible state to cover is the Timeout state. This state has been introduced in order to prevent from lockups of the converter should it fail to synchronize. In normal operation the controller shouldn't enter this state.

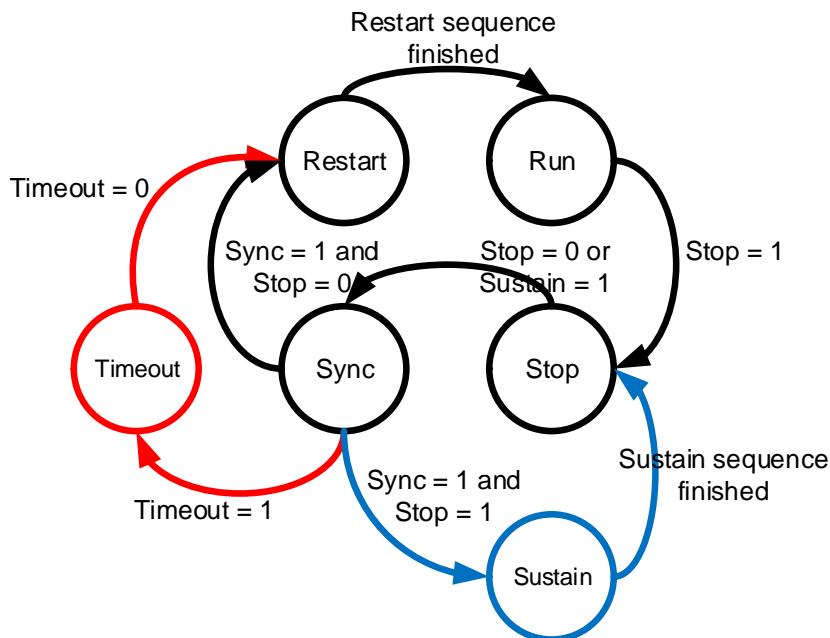


Fig. 6.6 Digital SCS State Machine

The main issue in this control scheme is the proper synchronization with the resonant current. In order to clarify this conditions exemplary operation waveforms are presented in Fig. 6.7.

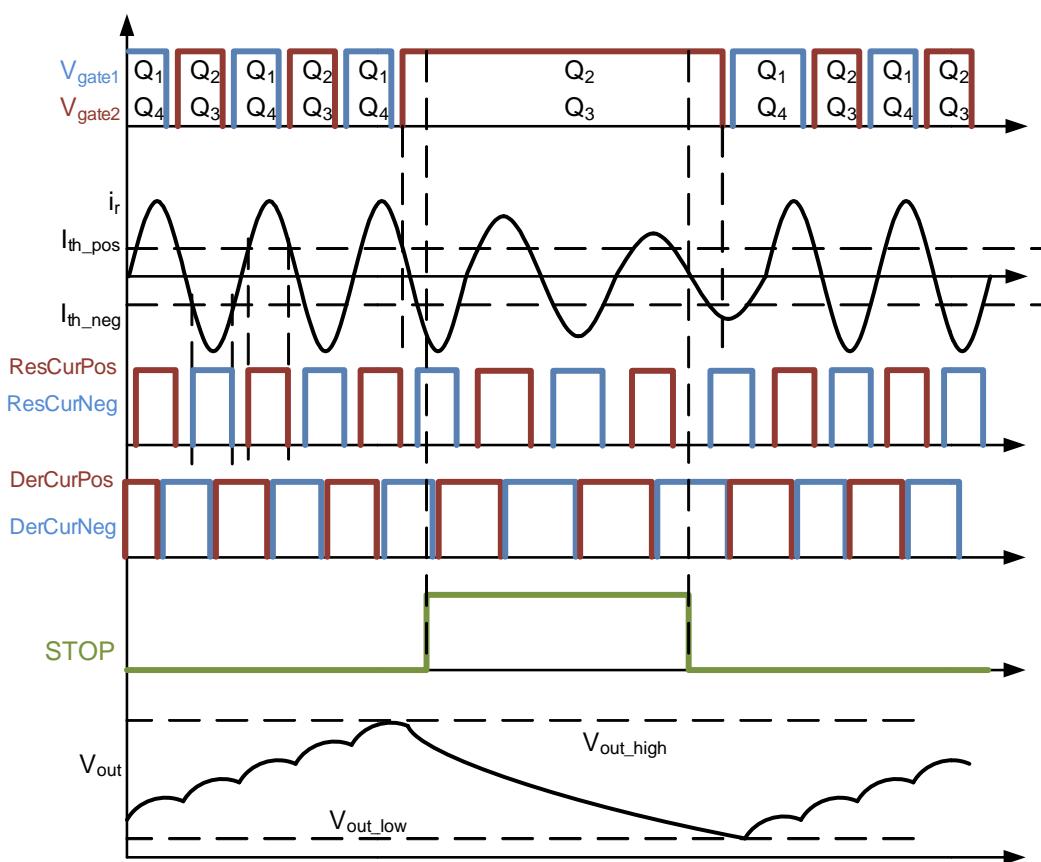


Fig. 6.7 Digital SCS Operating Waveforms

If we look closer at the instant when the signal STOP goes to 0, we can observe that the resonant current derivative is in fact negative, however the absolute value is too low. The controller waits for the absolute value of the resonant current to rise above the threshold and then performs the switch.

6.3 Summary

The digital implementations of two used control algorithms have been introduced in this chapter. The FM has been implemented for reference purposes. In order to achieve good output regulation and prevent from limit cycle oscillations the demand for the frequency resolution is quite high. Hence, the digital form of the FM requires relatively high resources in terms of clock frequency used for gate signal generation. On the other hand, the design of the control loop in digital form is pretty straightforward and enables easy modifications of the PID parameters in real time.

The second implemented control method is the SCS. The implementation details and problems associated with it have been discussed. The state machine for the control algorithm is described and individual controller blocks are described in detail. The most important mechanisms for the SCS Controller are the resonant current synchronization mechanism and the resonant current sustain mechanism. Without, the first the controller would not be able to restart switching properly, and the switches would be exposed to high current stress due to improper switching. The resonant current sustain mechanism exists to prevent the fading of the resonant current to such a value that the synchronization is no longer possible.

7 Measurements and Experimental Verification

On the base of implemented controller, which has been used to control the resonant power converter, several performance parameters have been measured. The most interesting measurements are the verification of soft switching conditions, operating waveforms, the quality of the output voltage, load change step response, the overall efficiency of the converter and the conducted electromagnetic interference. These measurements have been performed for both FM and SCS for comparison purposes. All of the measurements have been performed on the 3kW LCLC resonant converter described in chapter 5.2. To ease to localization of the measurement point a simplified schematic for the full-bridge resonant converter is presented in Fig. 7.1.

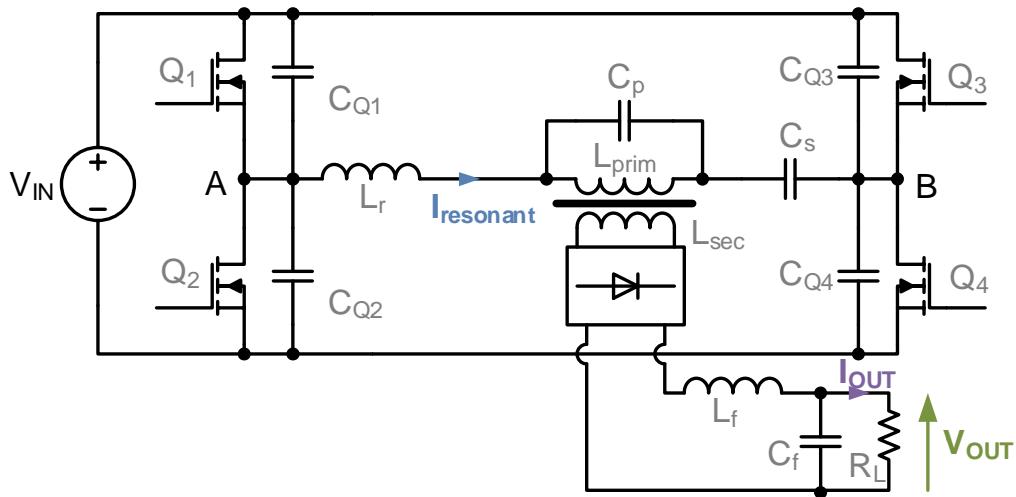


Fig. 7.1 3kW Class DE full-bridge resonant power converter

The current probe used in the following measurements has been set to 1V/1A sensitivity.

7.1 Operation Waveforms

The operation waveforms measurements have been performed at 200V DC supply voltage. This is due to the fact that a 400V improper operation would destroy the resonant converter. The developed controller is still at its preliminary stage and full reliability cannot yet be ensured. Because of this fact, the measurements have been made at a safer voltage. This limits the voltages and current to a more manageable level and the resonant converter can withstand occasional periods of improper operation. Additionally, measurements with the PFC rectifier are not preferred due to the existence of the 100Hz line ripple voltage which is clearly visible on the measurement waveforms. An additional factor is the possibility of interference with the power converter operation when connecting oscilloscope probes to sensitive areas of the circuit. Hence the 200V DC supply voltage has been chosen for the following measurements. As experience shows, the converter at 200V behaves very closely to the operation at 400V supply voltage. In order to provide similar operating conditions at 200V, the output voltage has been scaled down proportionally from 48V to 24V. The output current is also scaled down from 60A to 30A and the resulting output power reduces four times from 3000W to 750W.

The most important measurement is the verification of the soft switching conditions for the MOSFETs. No hard switching should ever occur, since as described in chapter 2.2, a single hard switching event may lead to the catastrophic failure of the converter. Fig. 7.2 to Fig. 7.6 show the rising and falling edges of leg A of the full-bridge resonant converter (point A in Fig. 7.1) in the SCS control scheme.

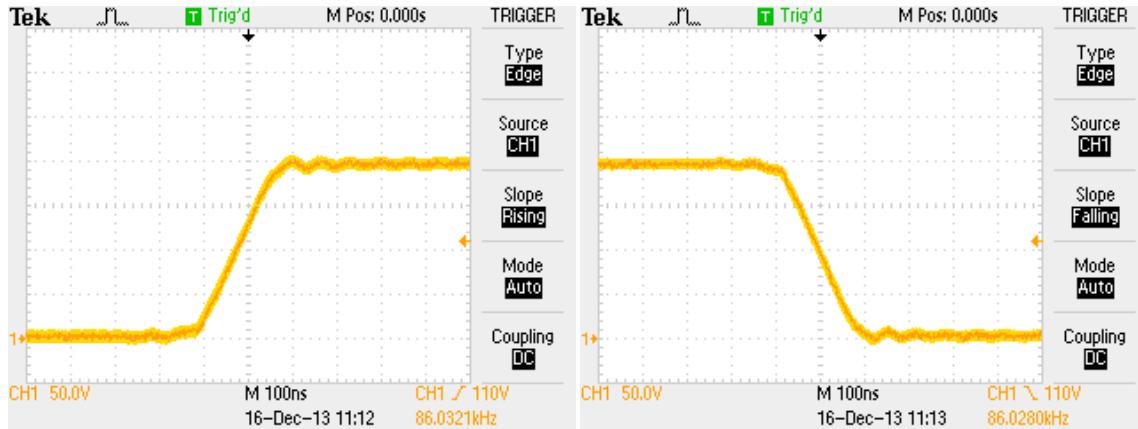


Fig. 7.2 SCS rising (left) and falling (right) edge of one of the full-bridge legs middle voltage at output conditions: $I_{load} = 0A$ (0% load), $V_{out} = 25.29V$

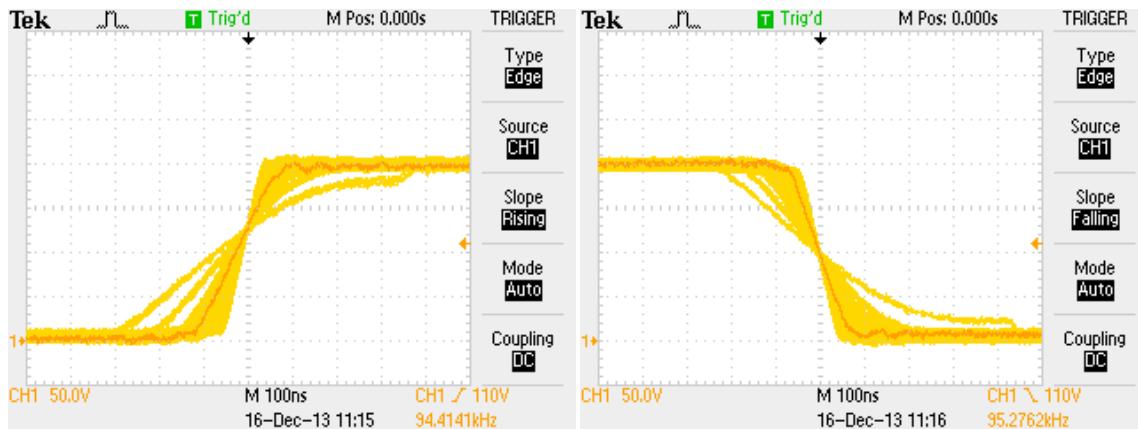


Fig. 7.3 SCS rising (left) and falling (right) edge of one of the full-bridge legs middle voltage at output conditions: $I_{load} = 7.8A$ (25% load), $V_{out} = 23.51V$

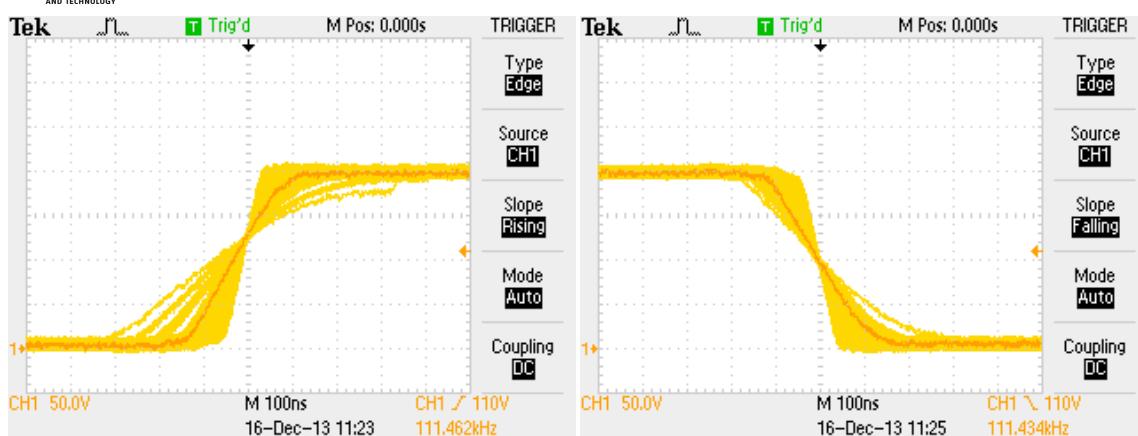


Fig. 7.4 SCS rising (left) and falling (right) edge of one of the full-bridge legs middle voltage at output conditions: $I_{load-} = 15.6A$ (50% load), $V_{out} = 23.49V$

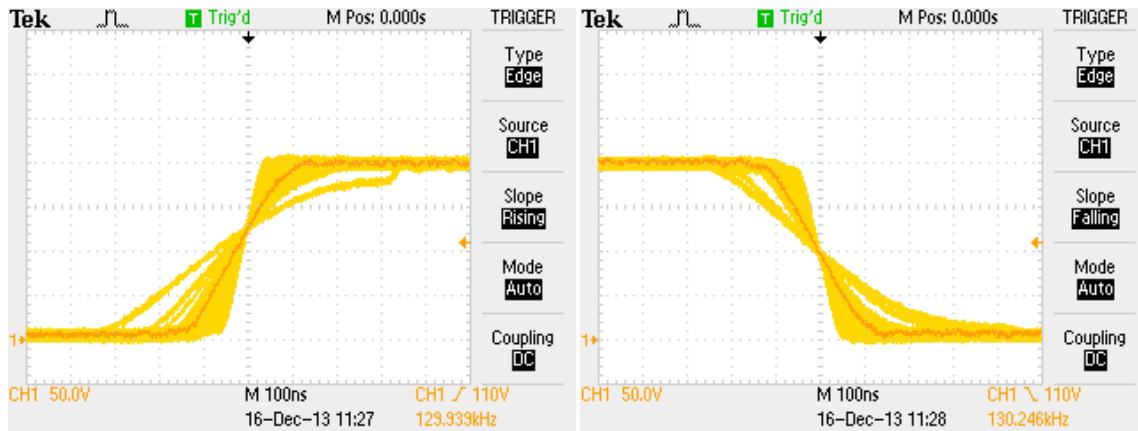


Fig. 7.5 SCS rising (left) and falling (right) edge of one of the full-bridge legs middle voltage at output conditions: $I_{load-} = 23.4A$ (75% load), $V_{out} = 23.46V$

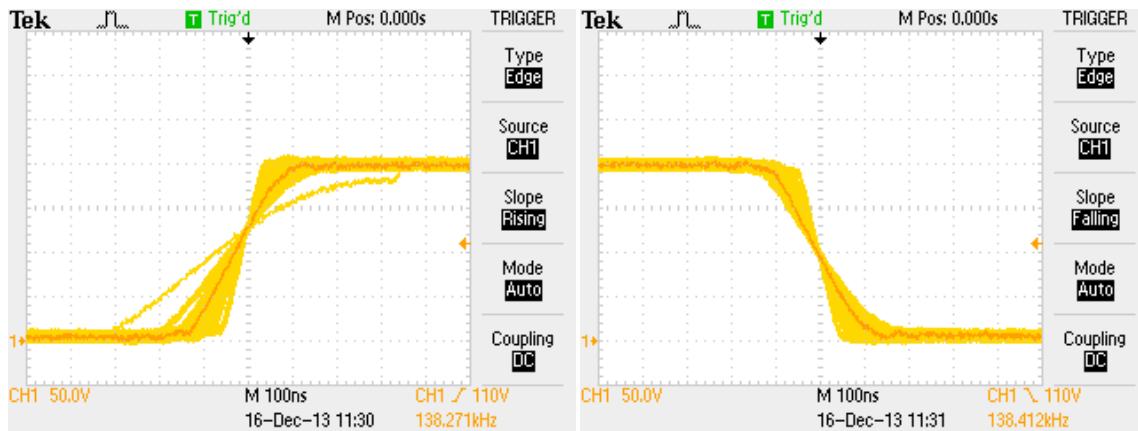


Fig. 7.6 SCS rising (left) and falling (right) edge of one of the full-bridge legs middle voltage at output conditions: $I_{load-} = 26.6A$ (85% load), $V_{out} = 23.44V$

As can be seen, the vast majority of the switching is soft switching, with the voltage across the MOSFETs fully changed. Only a small amount of switching is done with the voltage not changed to the opposite value, however these events are rare and only around 10% of the supply voltage is hard

switched. It shows that the conditions for soft switching is maintained throughout the whole operating region of the converter.

For comparison purposes the measured waveforms for the half-bridge switching in FM control scheme are also included. Fig. 7.7 to Fig. 7.11 show the rising and falling edges of leg A of the full-bridge resonant converter (point A in Fig. 7.1) in the FM control scheme.

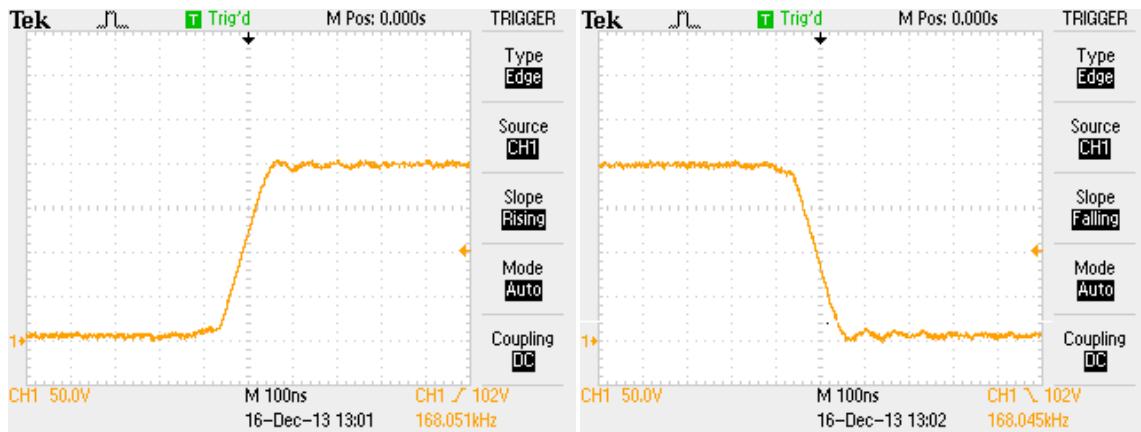


Fig. 7.7 FM rising (left) and falling (right) edge of one of the full-bridge legs middle voltage at output conditions: I-load- = 0A (0% load), Vout = 23.54V

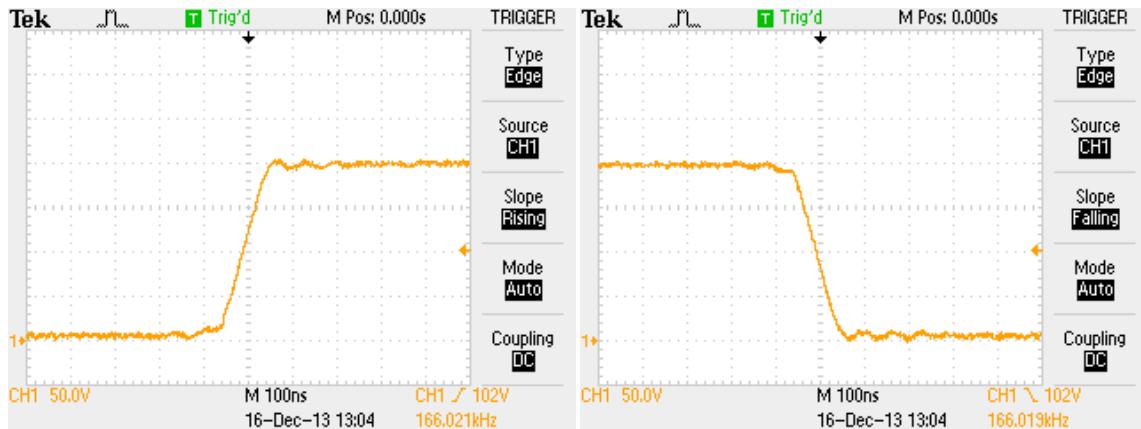
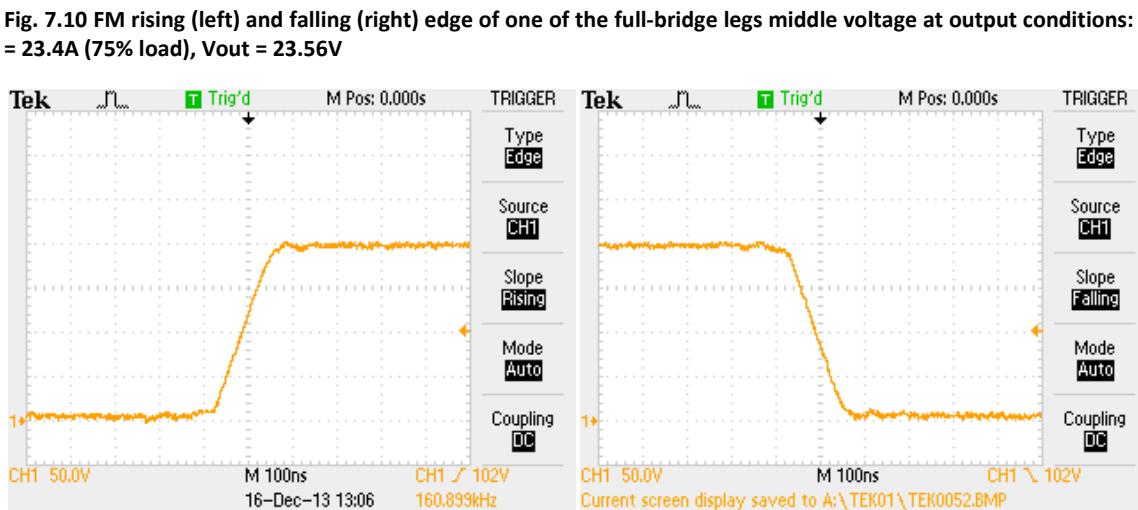
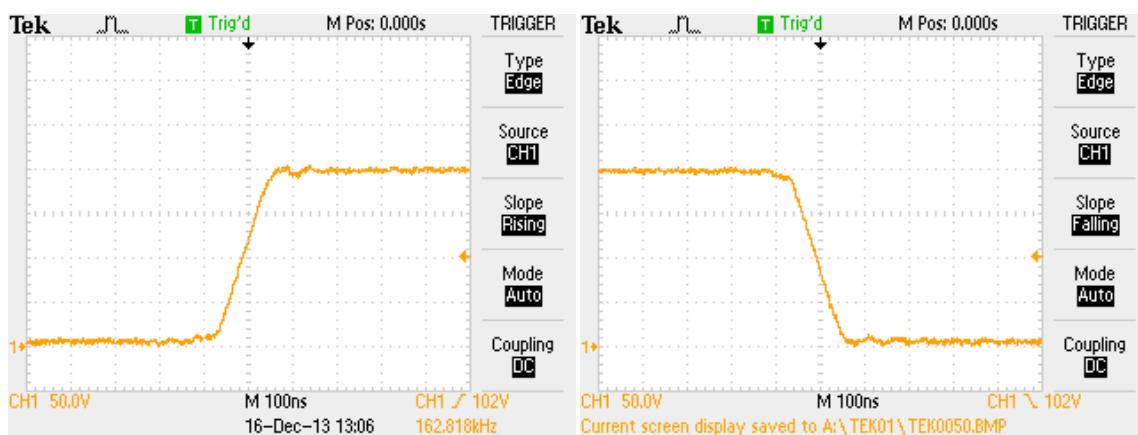
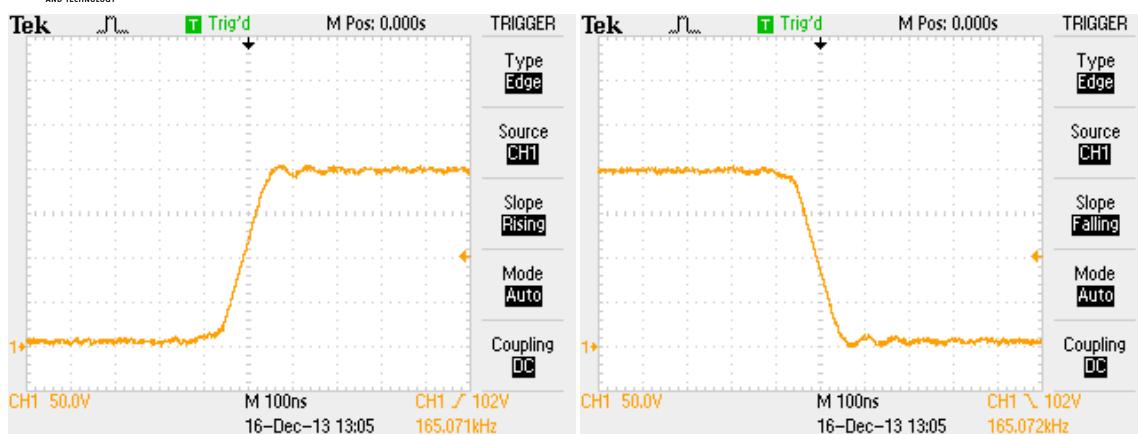


Fig. 7.8 FM rising (left) and falling (right) edge of one of the full-bridge legs middle voltage at output conditions: I-load- = 7.8A (25% load), Vout = 23.54V



As expected, in FM control scheme the MOSFETs are soft-switching as long as the converter operates in the inductive area and there is sufficient energy in the resonant circuit to charge the bridge output capacitances.

The two most interesting waveforms for converter operation in SCS control scheme are the half-bridge output voltage and the resonant current. In case of the full bridge configuration it is sufficient to measure the output voltage of only one of the full-bridge legs, since the other voltage will be complementary (assuming that the legs are symmetrical). The operating waveforms for the SCS control scheme are presented in Fig. 7.12 to Fig. 7.16. In each figure the top-left part presents a portion of the operating waveforms while the rest are zoomed in parts of it. In the first figure (Fig. 7.12) a situation with no load is presented. Since there is almost no energy flowing at the output of the converter, the only mechanism that is active is the resonant current sustain mechanism. The controller periodically performs switching in order to prevent the resonant current from falling below the desired threshold. As can be seen, the average switching frequency is at around half of the operating frequency. This is still quite a large value, and ideally this frequency (during no load) should be more around 1/10th to 1/20th of the operating frequency. However, due to the complex step response of the resonant circuit this setting proved to give acceptable results. In the future, a more complex approach to current sustain should be considered.



Fig. 7.12 SCS operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions: $I_{\text{load}} = 0\text{A}$, $V_{\text{out}} = 26.48\text{V}$

The operating waveforms for 25% load are presented in Fig. 7.13. There are a few interesting points to notice. In the top-left part an overview of the operation can be seen. The operation consists of two distinguishable states. One with lower resonant current amplitude is the period when the signal $\text{STOP} = 1$ and either no switching occurs or the resonant current sustain mechanism is working. The other is when the resonant current amplitude is larger. The signal STOP in this case is equal to 0 and the converter switches with a fixed frequency. Thus, we get “packets” of higher current amplitude interleaved with packets of lower amplitude with a frequency of around a few kilohertz.

The top-right part presents the instant of restart of the switching (STOP goes to 0). Notice that each of the switch events is soft-switched. The bottom-left part presents the instant when signal STOP goes to 1 and the converter ceases to switch.



Fig. 7.13 SCS operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions: $I_{load} = 7.8A$ (25% load), $V_{out} = 23.52V$

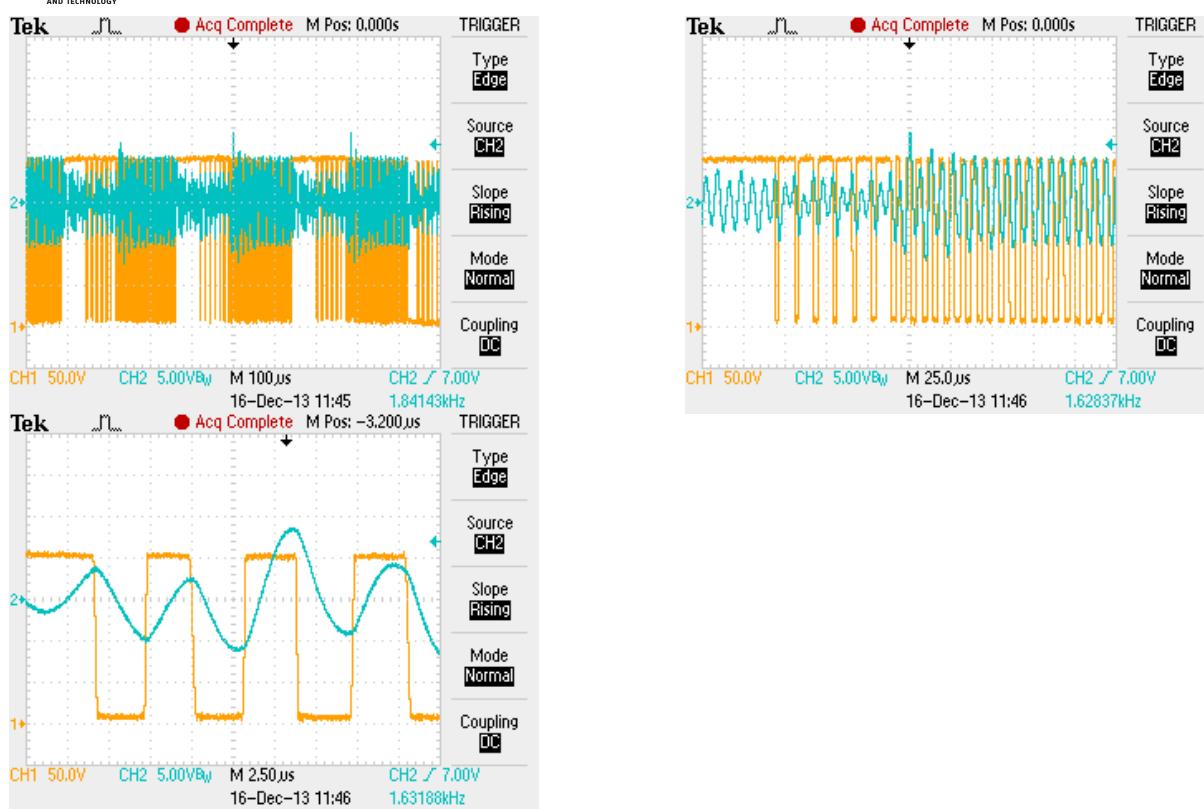


Fig. 7.14 SCS operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions: $I_{load} = 15.6A$ (50% load), $V_{out} = 23.5V$

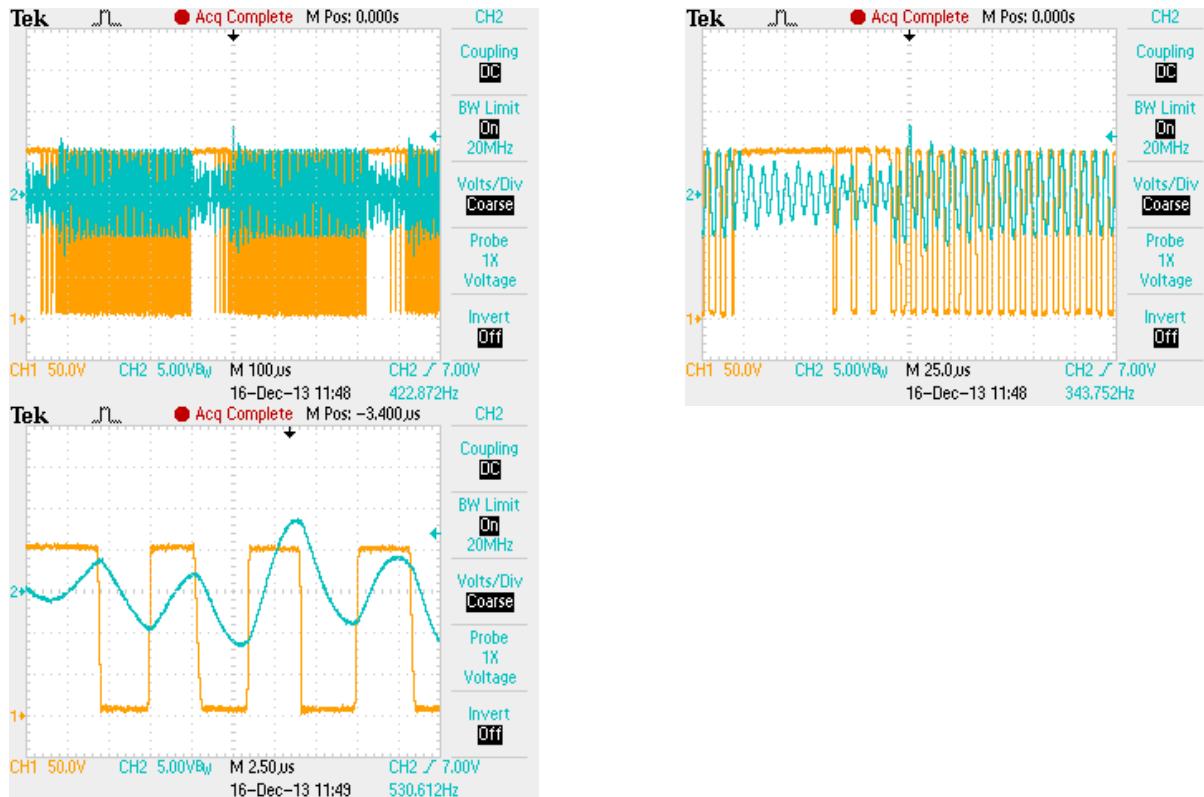


Fig. 7.15 SCS operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions: $I_{load} = 23.4A$ (75% load), $V_{out} = 23.45V$

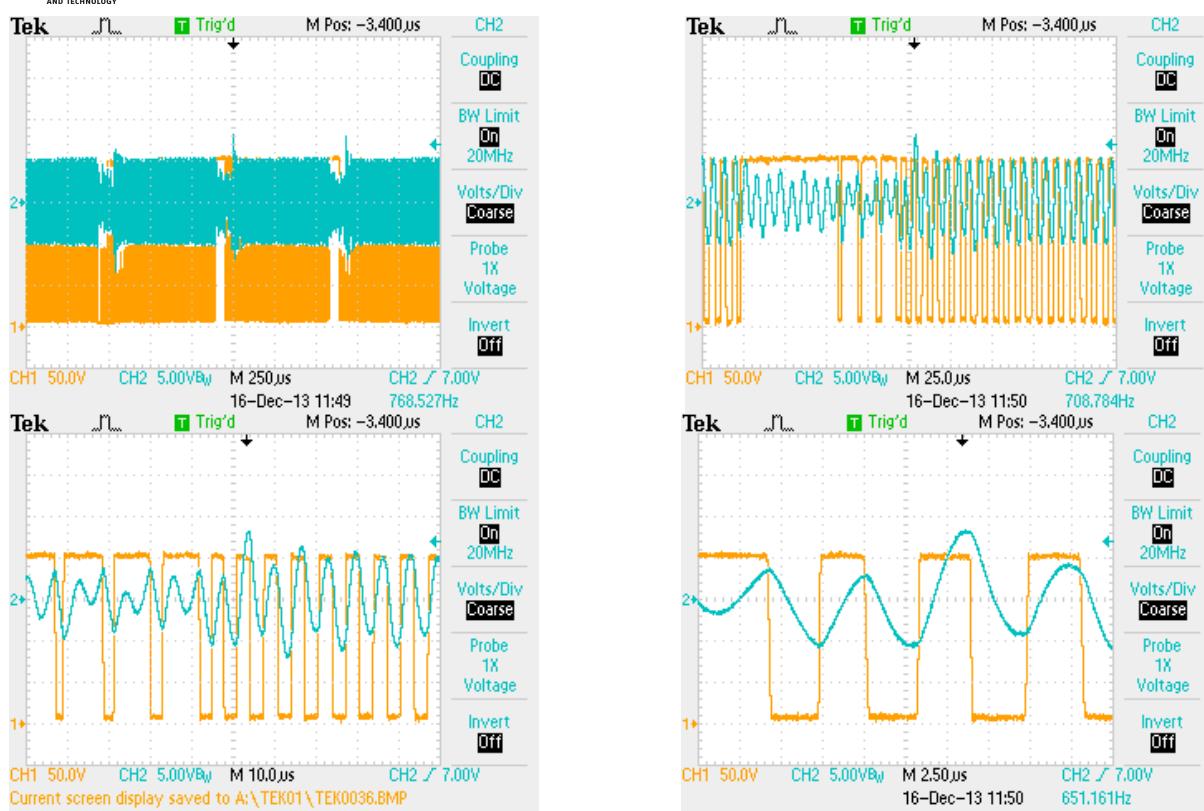


Fig. 7.16 SCS operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions:
 $I_{load} = 26.6A$ (85% load), $V_{out} = 23.44V$

As the load increases the length of the switching period increases and the average frequency of the “packets” decreases.

Again, for comparison purposes the operating waveforms for the FM control scheme are presented in Fig. 7.17 Fig. 7.21. It is worth mentioning that in LCLC resonant converter the resonant current amplitude varies only slightly with the load change.

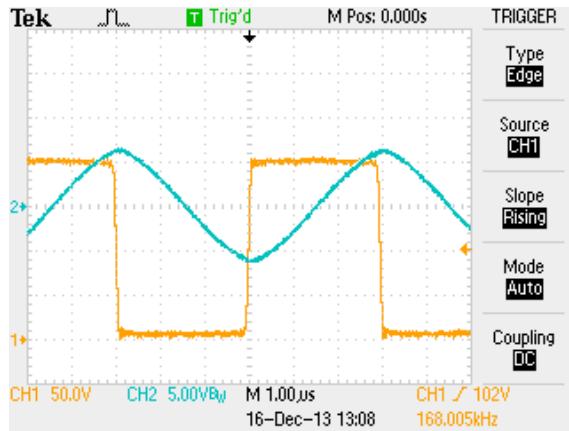


Fig. 7.17 FM operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions:
 $I_{load} = 0A$ (0% load), $V_{out} = 23.53V$

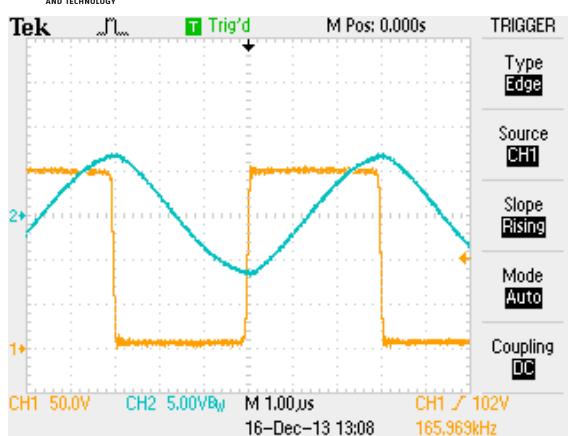


Fig. 7.18 FM operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions:
 $I_{load} = 7.8A$ (25% load), $V_{out} = 23.54V$

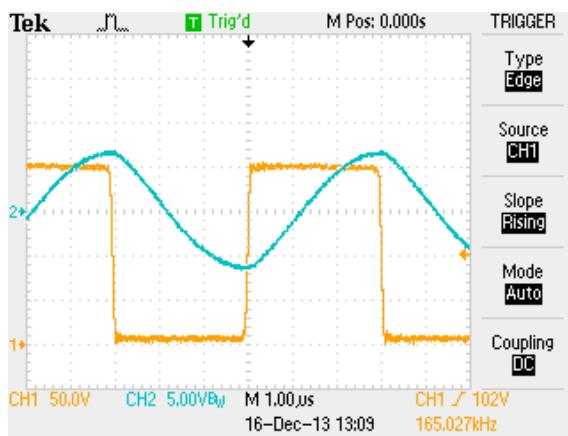


Fig. 7.19 FM operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions:
 $I_{load} = 15.6A$ (50% load), $V_{out} = 23.55V$

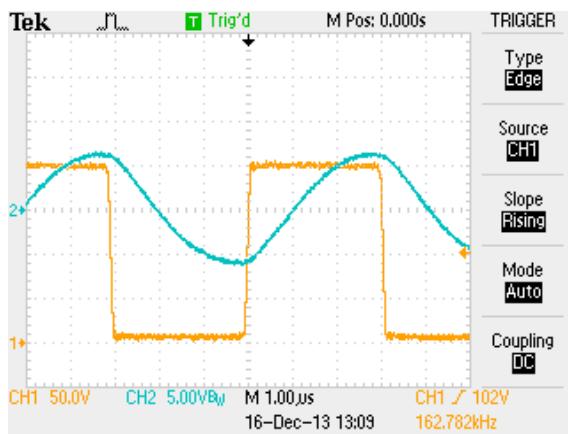


Fig. 7.20 FM operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions:
 $I_{load} = 23.4A$ (75% load), $V_{out} = 23.56V$

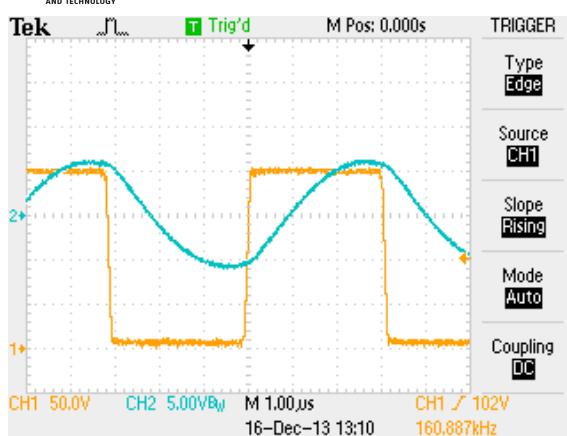


Fig. 7.21 FM operating waveforms: (1) half-bridge output voltage at point A, (2) resonant current at output conditions: $I_{load} = 26.6\text{ A}$ (85% load), $V_{out} = 23.57\text{ V}$

7.2 Output Voltage and Output Voltage Ripple

Another important parameter of any voltage power supply is the quality of the output voltage. In this chapter the measurements of the output voltage ripple for various load conditions are presented. The measured output voltage vs output power is presented in Fig. 7.22.

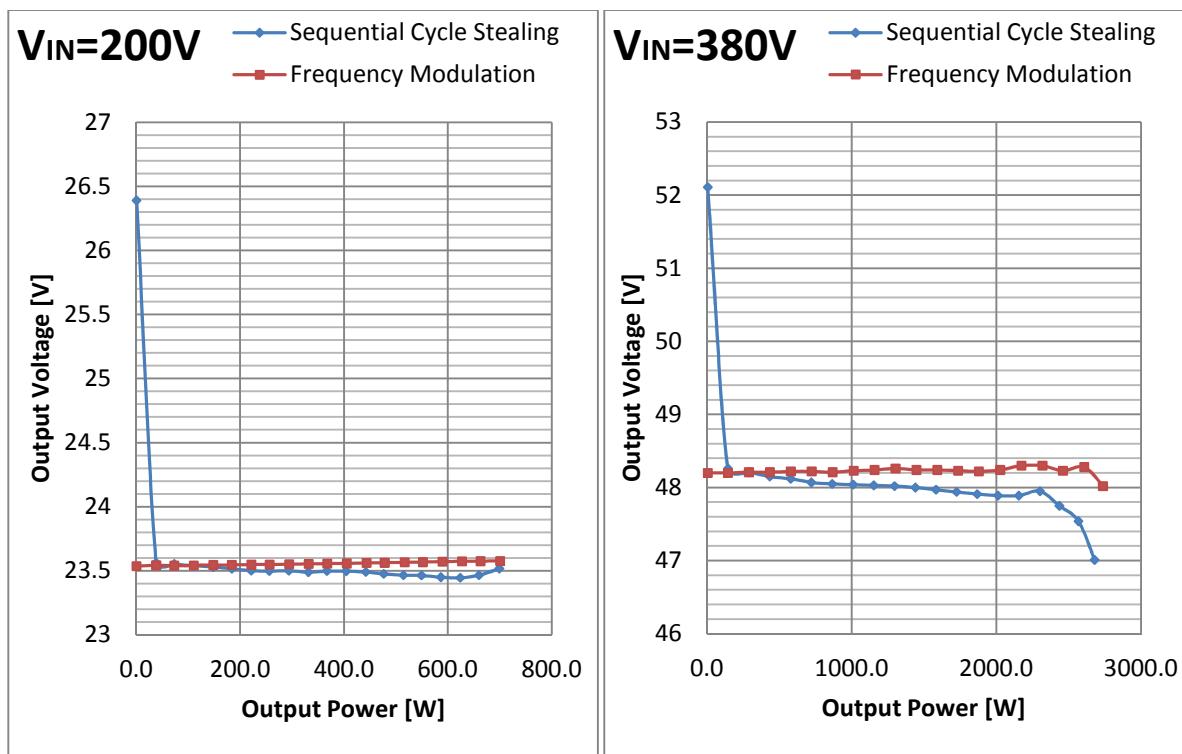
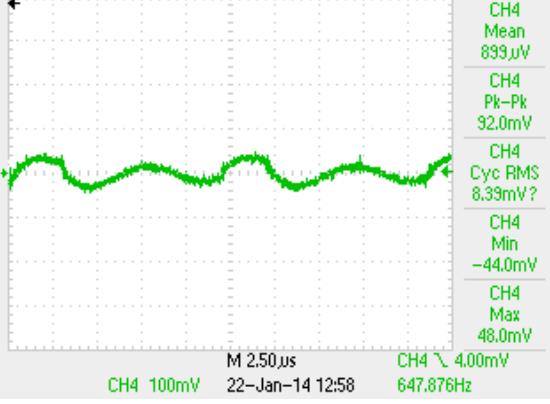
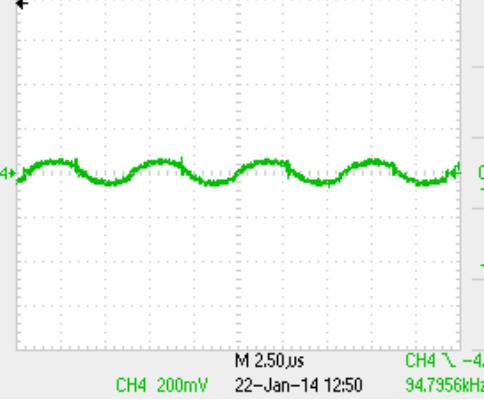
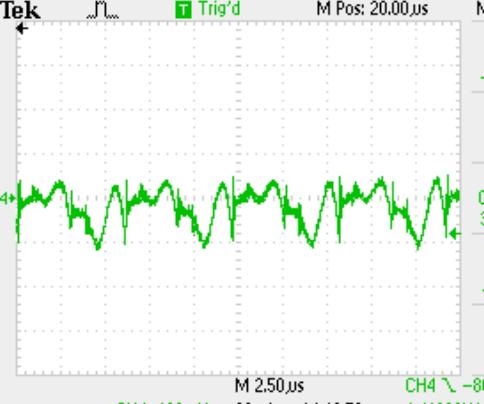
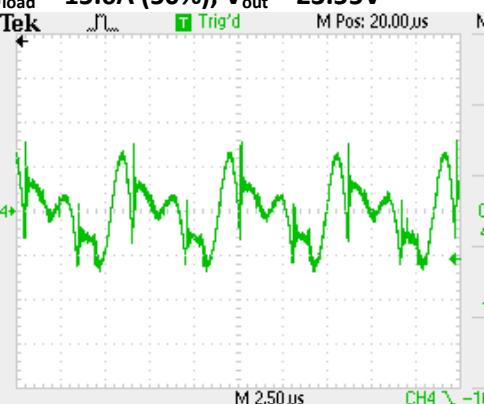
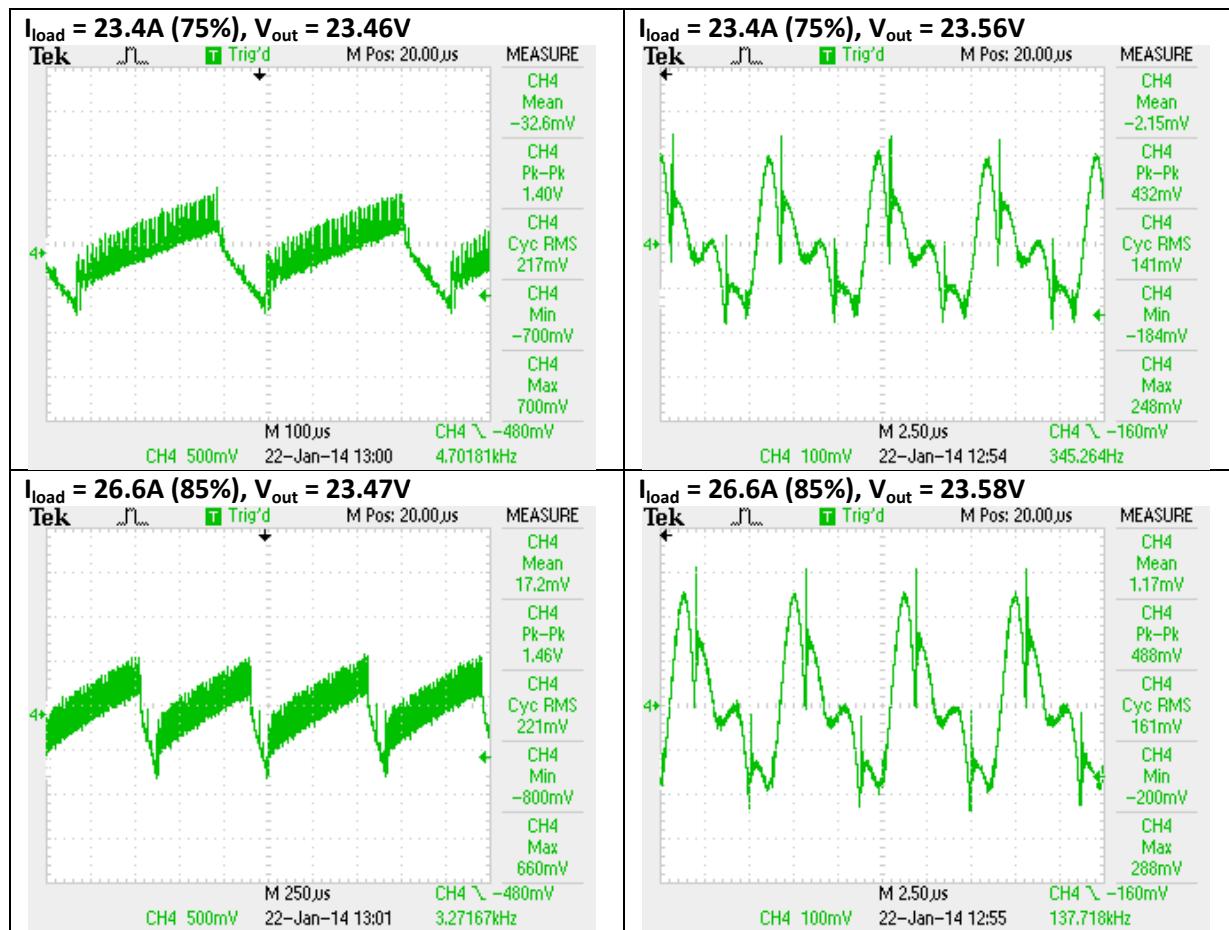


Fig. 7.22 Output voltage vs output power characteristic comparison between SCS and FM for 200V supply voltage (left) and PFC 390V supply voltage (right)

The FM maintains better regulation of the output voltage whereas the SCS suffers from a steady voltage drop with increasing output power. TABLE 7.1 contains the results for both SCS and FM control schemes.

TABLE 7.1 Output voltage ripple measurement results

Sequential Cycle Stealing	Frequency Modulation
<p>I_{load} = 0A (0%), V_{out} = 25.33V</p> <p>Tek M Pos: 20.00μs MEASURE</p>  <p>CH4 Mean 899μV CH4 Pk-Pk 92.0mV CH4 Cyc RMS 8.39mV? CH4 Min -44.0mV CH4 Max 48.0mV</p> <p>M 2.50μs CH4 ~ 4.00mV</p> <p>CH4 100mV 22-Jan-14 12:58 647.876kHz</p>	<p>I_{load} = 0A (0%), V_{out} = 23.54V</p> <p>Tek M Pos: 20.00μs MEASURE</p>  <p>CH4 Mean 4.92mV CH4 Pk-Pk 136mV CH4 Cyc RMS 14.1mV? CH4 Min -64.0mV CH4 Max 72.0mV</p> <p>M 2.50μs CH4 ~ -4.00mV</p> <p>CH4 200mV 22-Jan-14 12:50 94.7956kHz</p>
<p>I_{load} = 7.8A (25%), V_{out} = 23.51V</p> <p>Tek M Pos: 20.00μs MEASURE</p>  <p>CH4 Mean -10.5mV CH4 Pk-Pk 1.10V CH4 Cyc RMS 171mV CH4 Min -360mV CH4 Max 740mV</p> <p>M 100μs CH4 ~ -220mV</p> <p>CH4 500mV 22-Jan-14 12:59 4.55368kHz</p>	<p>I_{load} = 7.8A (25%), V_{out} = 23.54V</p> <p>Tek M Pos: 20.00μs MEASURE</p>  <p>CH4 Mean -15.3mV CH4 Pk-Pk 172mV CH4 Cyc RMS 35.0mV? CH4 Min -112mV CH4 Max 60.0mV</p> <p>M 2.50μs CH4 ~ -80.0mV</p> <p>CH4 100mV 22-Jan-14 12:52 1.41269kHz</p>
<p>I_{load} = 15.6A (50%), V_{out} = 23.50V</p> <p>Tek M Pos: 20.00μs MEASURE</p>  <p>CH4 Mean 11.2mV CH4 Pk-Pk 1.20V CH4 Cyc RMS 192mV CH4 Min -500mV CH4 Max 700mV</p> <p>M 100μs CH4 ~ -380mV</p> <p>CH4 500mV 22-Jan-14 12:59 2.12703kHz</p>	<p>I_{load} = 15.6A (50%), V_{out} = 23.55V</p> <p>Tek M Pos: 20.00μs MEASURE</p>  <p>CH4 Mean -380μV CH4 Pk-Pk 304mV CH4 Cyc RMS 46.2mV? CH4 Min -136mV CH4 Max 168mV</p> <p>M 2.50μs CH4 ~ -108mV</p> <p>CH4 100mV 22-Jan-14 12:53 209.274Hz</p>



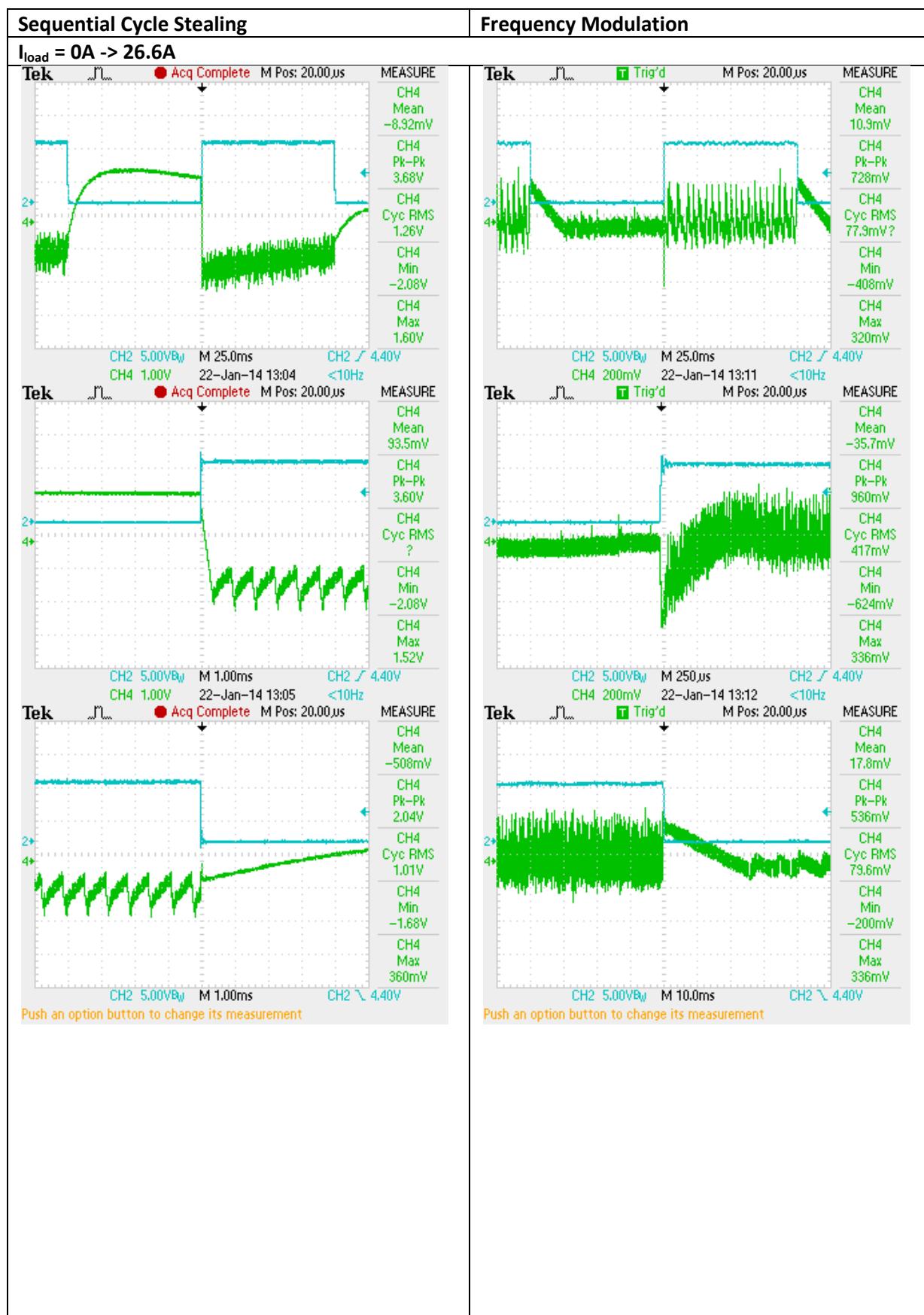
As can be seen from the measurement results the SCS control results in around 4 times higher ripple voltage. This is a drawback of this method, however the output ripple voltage could be reduced by modifying the settings for the control scheme or by applying more advanced techniques for determining the STOP signal. Currently, the STOP signal is obtained by a simple comparison of the output voltage with a reference value. It is then natural that the control scheme inherits the features of systems controlled by comparator.

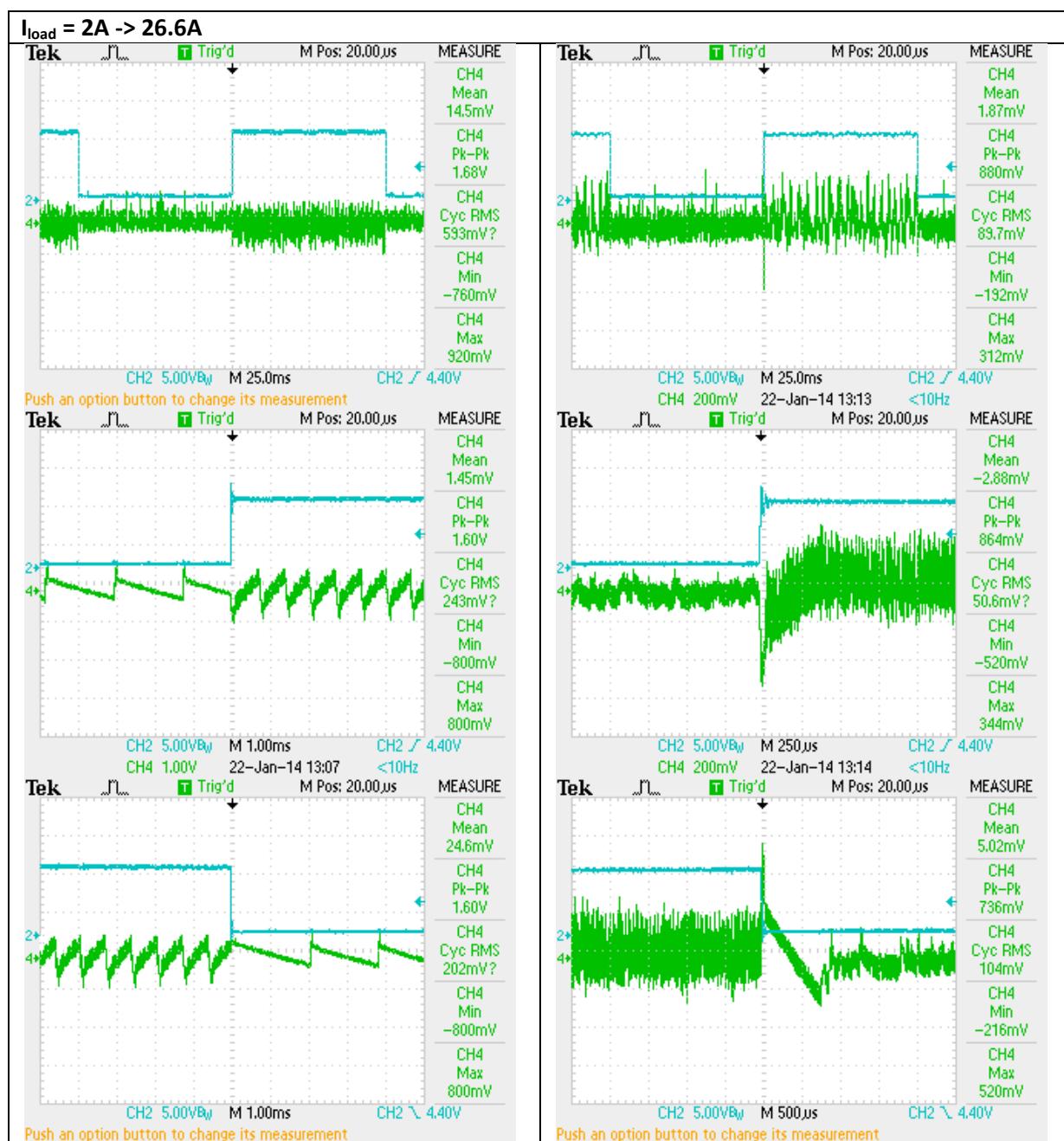
7.3 Load Step Response

An interesting topic is the load step output voltage response of the power converter. Hence, the measurement for two cases have been made. These are 0%-85% load step and 6%-85%. The two conditions have been necessary in order to show the proper operation of the SCS controller and highlight a problem that is connected with the resonant current mechanism. At no load, due to the resonant current sustain mechanism, the output voltage is c.a. 3V higher than the desired voltage. This lead to skewed step response results and is the reason for the 6%-85% measurements. The measurement results of the output voltage load step response for both cases and for SCS and FM control schemes are presented in TABLE 7.2

The first figure row gives the overview of the step response while the next two rows are zoomed in views of the load rising and falling edges.

TABLE 7.2 Output voltage load step response measurement results. (2) output current, (4) output voltage





As can be seen from the measurement results, the step response of the SCS control scheme is rather poor for the 0%-85% load change conditions. This is due to the facts mentioned above. If the load step conditions are changed to 6%-85%, the behavior improves significantly. The effects of the load step change do not influence the level of the output voltage and only the shape of the output voltage ripple is changing. With the digital implementation of the FM it is possible to achieve fast load step responses, but the main advantage of the FM is its lower ripple voltage.

7.4 Efficiency

One of the most important parameter is the efficiency of the power converter. This parameter has been measured in two conditions. One has been with the PFC rectifier omitted and the DC-DC converter supplied form 200V DC power supply and the second has been with the PFC rectifier supplied from 230V AC line and the DC-DC converter supplied with 390V directly from the PFC

rectifier output. Both measurements include the supply of the auxiliary power supply necessary for the MOSFET drivers and other components, but exclude the power drawn by the Universal Control Board. In case of the 200V supply voltage the measurement of both input and output power has been made with the Yokogawa WT3000 precision power analyzer, while the case with PFC rectifier supply voltage the input power has been measured with the Yokogawa WT 3000 and the output power has been measured using a voltage meter and current meter.

7.4.1 Efficiency measurements for 200V supply voltage

Since the supply voltage is scaled down from 400V to 200V the output values should also be scaled down by the factor of 2. Hence the output voltage is scaled down to 24V from 48V and the output current is scaled down to 30A from 60A. TABLE 7.3 and TABLE 7.4 contain the measurement results for SCS and FM control schemes respectively.

TABLE 7.3 SCS efficiency measurement results for various loads

V _{in} [V]	I _{in} [A]	V _{out} [V]	I _{out} [A]	P _{in} [W]	P _{out} [W]	P _{loss} [W]	Eff [%]
201.69	0.123	26.39	0.02	24.8	0.4	24.4	1.8
201.66	0.358	23.56	1.62	72.2	38.3	33.9	53.0
201.63	0.523	23.55	3.11	105.5	73.2	32.2	69.4
201.60	0.726	23.54	4.71	146.4	110.9	35.5	75.8
201.57	0.935	23.53	6.31	188.5	148.5	40.0	78.8
201.54	1.126	23.51	7.82	226.9	184.0	43.0	81.1
201.51	1.331	23.50	9.42	268.2	221.4	46.8	82.6
201.48	1.522	23.49	10.91	306.7	256.3	50.3	83.6
201.45	1.727	23.50	12.51	347.9	293.9	54.0	84.5
201.42	1.931	23.49	14.11	388.9	331.3	57.6	85.2
201.39	2.124	23.49	15.62	427.8	367.1	60.6	85.8
201.36	2.328	23.49	17.22	468.8	404.6	64.1	86.3
201.33	2.530	23.49	18.82	509.4	442.1	67.3	86.8
201.30	2.717	23.47	20.31	546.9	476.7	70.2	87.2
201.27	2.927	23.46	21.93	589.1	514.7	74.4	87.4
201.24	3.116	23.46	23.42	627.1	549.5	77.6	87.6
201.21	3.319	23.45	25.02	667.8	586.6	81.1	87.8
201.18	3.524	23.44	26.62	709.0	624.1	84.8	88.0
201.15	3.719	23.46	28.13	748.1	660.0	88.0	88.2
201.12	3.934	23.51	29.73	791.2	699.2	92.0	88.4

TABLE 7.4 FM efficiency measurement results for various loads

V _{in} [V]	I _{in} [A]	V _{out} [V]	I _{out} [A]	P _{in} [W]	P _{out} [W]	P _{loss} [W]	Eff [%]
201.68	0.208	23.53	0.02	41.9	0.4	41.5	1.0
201.64	0.418	23.54	1.62	84.3	38.1	46.1	45.3
201.62	0.604	23.5	3.11	121.8	73.1	48.6	60.1
201.59	0.803	23.54	4.71	161.9	110.8	51.0	68.5
201.55	1.003	23.54	6.31	202.2	148.4	53.7	73.4
201.53	1.191	23.54	7.82	240.0	184.1	55.9	76.7
201.50	1.390	23.54	9.42	280.1	221.7	58.3	79.2
201.47	1.576	23.54	10.91	317.5	256.8	60.7	80.9
201.44	1.775	23.55	12.51	357.6	294.5	63.0	82.4
201.41	1.975	23.55	14.11	397.8	332.2	65.6	83.5
201.38	2.165	23.55	15.62	436.0	368.0	68.0	84.4

201.35	2.366	23.55	17.22	476.4	405.6	70.7	85.2
201.32	2.567	23.56	18.82	516.8	443.4	73.3	85.8
201.29	2.754	23.56	20.31	554.4	478.4	75.9	86.3
201.26	2.960	23.56	21.94	595.7	516.9	78.8	86.8
201.24	3.149	23.56	23.42	633.7	551.9	81.7	87.1
201.21	3.352	23.57	25.02	674.5	589.7	84.7	87.4
201.18	3.556	23.57	26.62	715.4	627.5	87.8	87.7
201.15	3.740	23.57	28.13	752.3	663.1	89.1	88.2
201.12	3.937	23.57	29.73	791.8	701.0	90.8	88.5

The comparison between the SCS and FM power losses and efficiencies is presented in Fig. 7.23

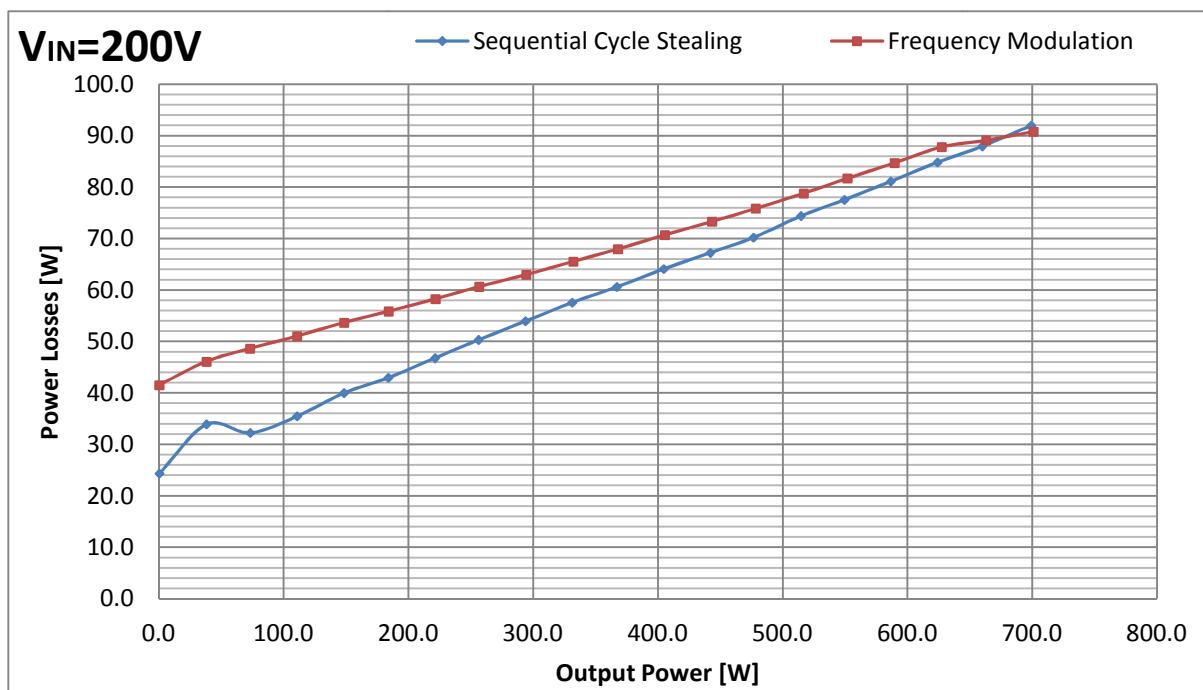


Fig. 7.23 Power losses vs output power characteristic comparison between SCS and FM

It can be seen that for light loads the power losses are almost two time smaller for SCS than for FM. The power losses gain decreases as the output power approaches full power, where the losses are somewhat equal. This is expected, since at full power the duty cycle for “packet” length is 100%, thus the waveforms between SCS and FM are identical.

The efficiency characteristic vs output power for both control schemes is presented in Fig. 7.24. The SCS improves the efficiency significantly to around 50% of output power. This is a desired feature because one of the main disadvantages of the FM control is poor efficiency at light loads. Applying SCS gives noticeable results in this region.

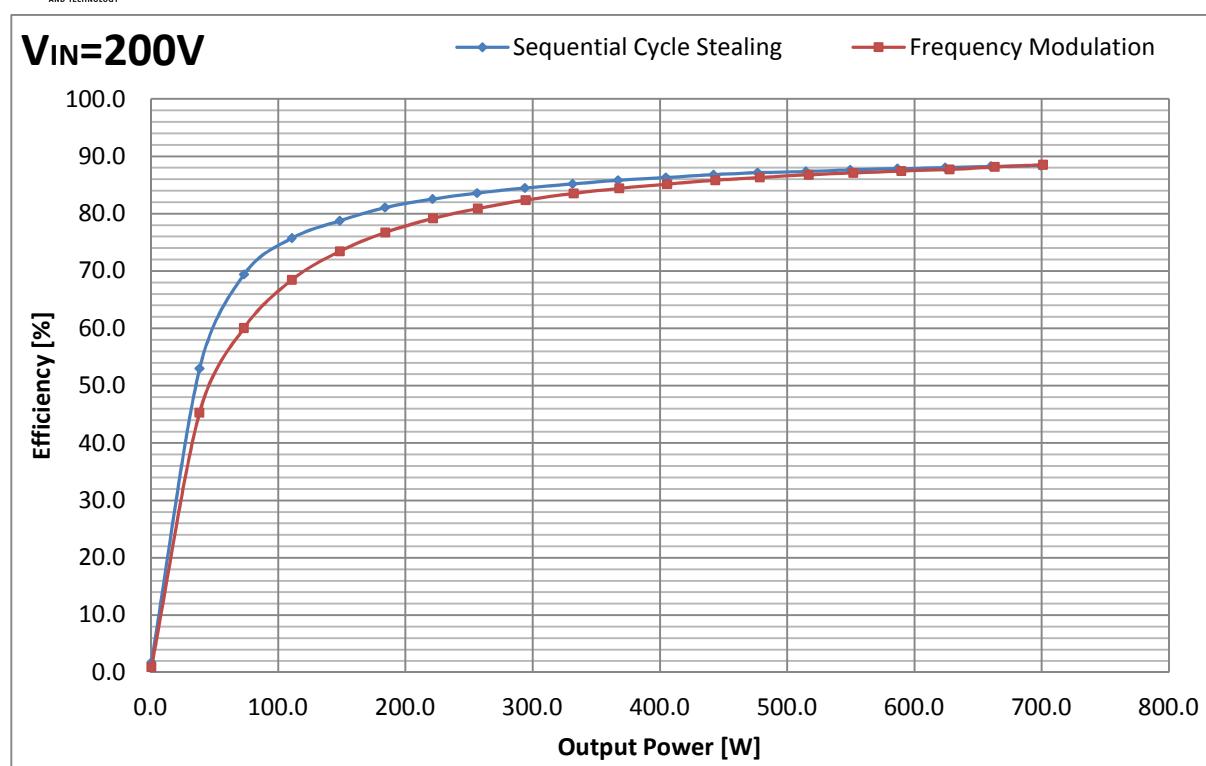


Fig. 7.24 Efficiency vs output power characteristic comparison between SCS (blue) and FM (green) control schemes. The efficiency of whole power supply is presented

7.4.2 Efficiency measurements for 390V supply voltage from PFC rectifier

Most of the high power converters operate with a PFC rectifier circuit. To verify proper operation with this circuit efficiencies have been measured and the results are presented in TABLE 7.5 and TABLE 7.6 for SCS and FM control schemes respectively.

TABLE 7.5 SCS efficiency measurement results for various loads

V _{in} [V]	I _{in} [A]	V _{out} [V]	I _{out} [A]	P _{in} [W]	P _{out} [W]	P _{loss} [W]	Eff [%]
227.05	0.56	52.11	0.10	95.0	5.2	89.8	5.5
227.32	1.17	48.26	3.01	250.0	145.3	104.7	58.1
225.12	1.92	48.21	6.01	417.0	289.7	127.3	69.5
225.36	2.64	48.15	9.01	580.0	433.8	146.2	74.8
225.20	3.36	48.12	12.01	741.0	577.9	163.1	78.0
224.26	4.09	48.07	15.00	902.0	721.1	181.0	79.9
223.08	4.83	48.05	18.01	1063.0	865.4	197.6	81.4
224.49	5.52	48.04	21.01	1223.0	1009.3	213.7	82.5
223.45	6.26	48.03	24.00	1384.0	1152.7	231.3	83.3
223.69	6.96	48.02	27.00	1543.0	1296.5	246.5	84.0
222.53	7.72	48.00	29.99	1704.0	1439.8	264.2	84.5
221.27	8.48	47.97	32.99	1864.0	1582.6	281.3	84.9
221.75	9.17	47.94	35.98	2021.0	1724.8	296.1	85.3
220.40	9.93	47.91	38.98	2177.0	1867.5	309.5	85.8
220.32	10.65	47.89	42.00	2336.0	2011.3	324.6	86.1
220.71	11.37	47.89	45.00	2493.0	2155.0	338.0	86.4

219.81	12.12	47.95	48.00	2664.0	2301.6	362.4	86.4
218.77	12.86	47.75	51.00	2804.0	2435.2	368.8	86.8
219.41	13.44	47.54	54.00	2940.0	2567.1	372.8	87.3
217.40	14.15	47.01	56.99	3069.0	2679.1	389.9	87.3

TABLE 7.6 FM efficiency measurement results for various loads

V _{in} [V]	I _{in} [A]	V _{out} [V]	I _{out} [A]	P _{in} [W]	P _{out} [W]	P _{loss} [W]	Eff [%]
227.44	0.92	48.20	0.10	192.3	4.8	187.5	2.5
227.57	1.63	48.20	3.01	356.0	145.0	210.9	40.8
226.66	2.34	48.21	6.01	514.0	289.7	224.3	56.4
225.64	3.05	48.21	9.01	671.0	434.3	236.6	64.7
226.11	3.71	48.22	12.01	824.0	579.1	244.9	70.3
225.26	4.41	48.22	15.00	978.0	723.3	254.7	74.0
223.12	5.15	48.21	18.01	1133.0	868.2	264.7	76.6
224.98	5.79	48.23	21.01	1287.0	1013.3	273.7	78.7
223.85	6.51	48.24	24.00	1442.0	1157.7	284.2	80.3
222.99	7.23	48.26	27.00	1597.0	1303.0	294.0	81.6
222.97	7.91	48.24	29.99	1751.0	1447.0	304.0	82.6
223.05	8.61	48.24	32.99	1907.0	1591.5	315.4	83.5
222.09	9.35	48.23	35.98	2064.0	1735.3	328.7	84.1
220.93	10.10	48.22	38.98	2220.0	1879.6	340.4	84.7
219.96	10.88	48.24	42.00	2374.0	2026.0	347.9	85.3
220.23	11.54	48.30	45.00	2532.0	2173.5	358.5	85.8
219.18	12.31	48.30	48.00	2689.0	2318.4	370.6	86.2
219.19	13.02	48.23	51.00	2844.0	2459.7	384.3	86.5
218.18	13.78	48.28	54.00	2996.0	2607.1	388.9	87.0
217.90	14.39	48.02	56.99	3128.0	2736.6	391.3	87.5

The comparison between the SCS and FM power losses and efficiencies is presented in Fig. 7.25.

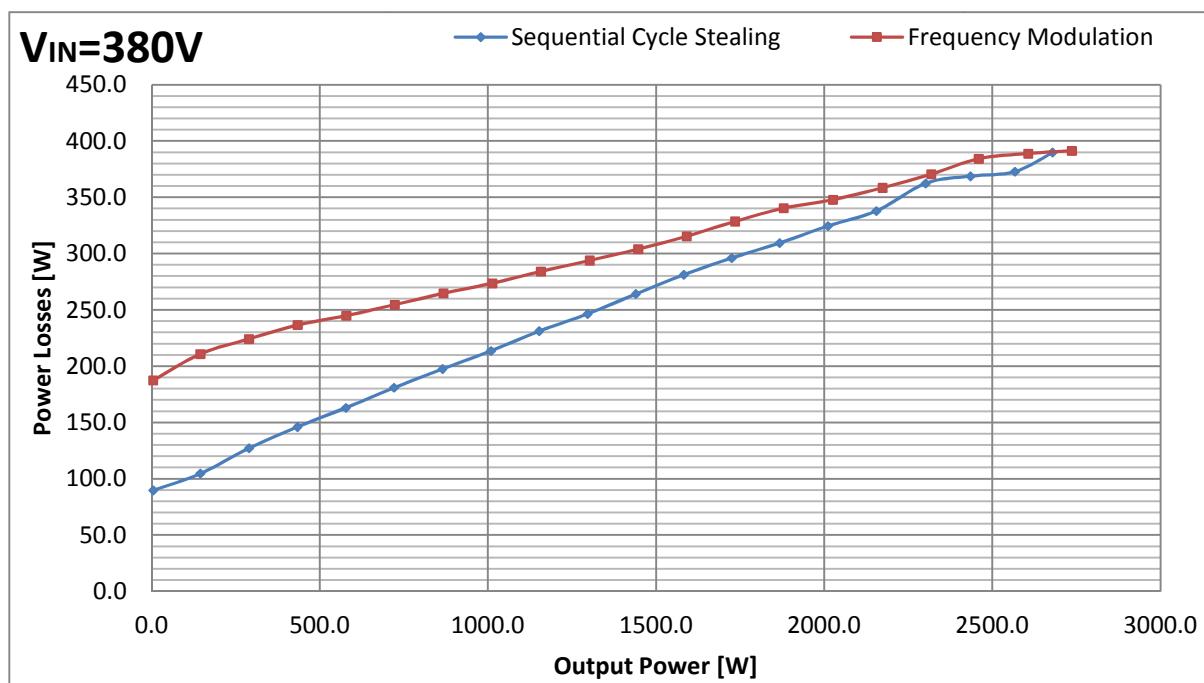


Fig. 7.25 Power losses vs output power characteristic comparison between SCS and FM

Similarly as for 200V supply voltage, the power losses for SCS are c.a. 2 times smaller than for FM. In our case the power saved at light load is around 100W.

The efficiency characteristic vs output power for both control schemes is presented in Fig. 7.26.

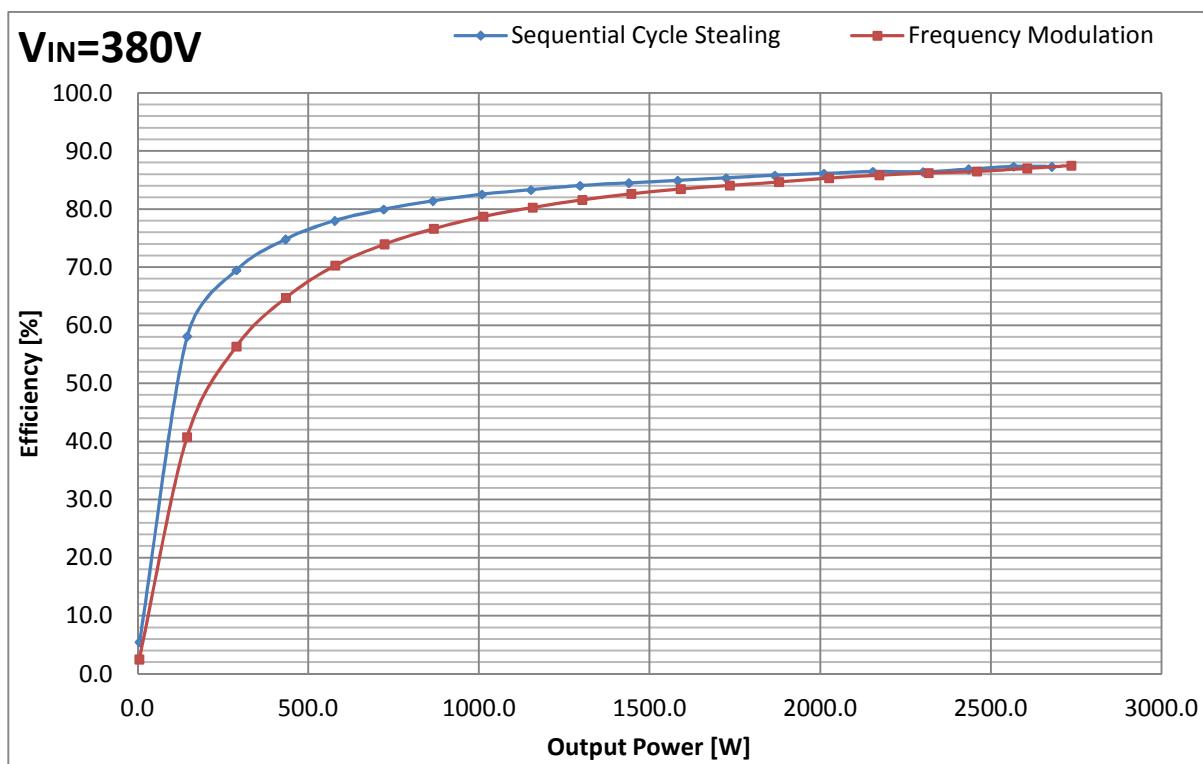


Fig. 7.26 Efficiency vs output power characteristic comparison between SCS (blue) and FM (green) control schemes. The efficiency of whole power supply is presented.

Again, the SCS improves the efficiency significantly to around 50% of output power. In case of higher supply voltage the efficiency improvement is even higher and reaches 18% at 150W output power.

7.5 Conducted EMI measurements

The power supplies connected to 230V line voltage must pass the necessary EMC regulations. The strictness of these regulations vary with the application but the measurement of conducted EMI should give an overview of the control methods performance. The measurements have been made at 30% load with the supply from 230V line voltage. Both the PFC rectifier and DC-DC resonant converter have been operating. A EMI filter is provided on the power supply PCB, however the filter has not been optimized. Thus, at higher frequency region several resonances can be seen, that are the result of the unoptimized input filter. A method for filter optimization has been presented in [61]. The measurement results are presented in Fig. 7.27 and Fig. 7.28 for SCS and FM respectively.

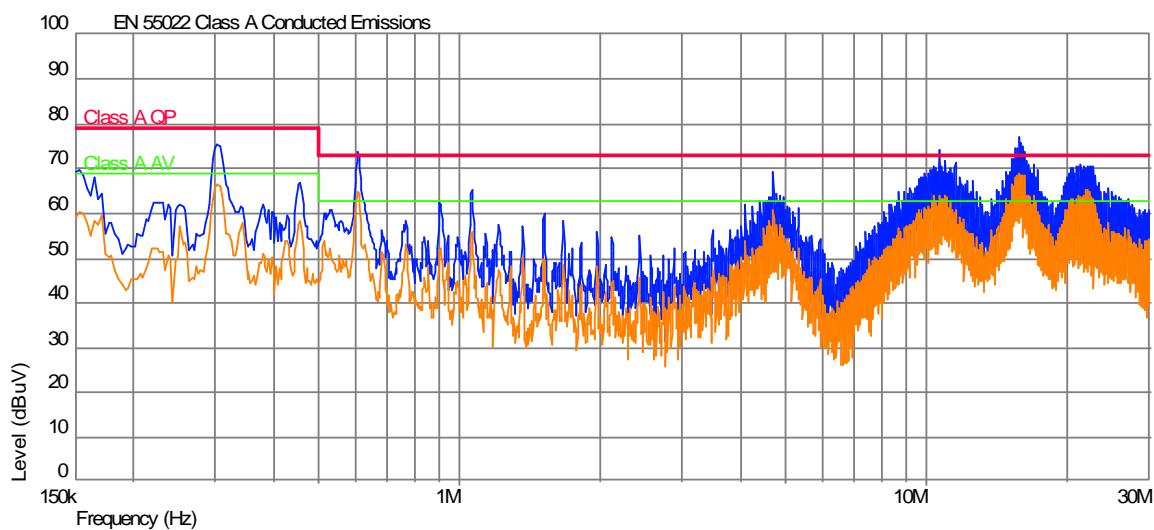


Fig. 7.27 SCS conducted EMI measurement results

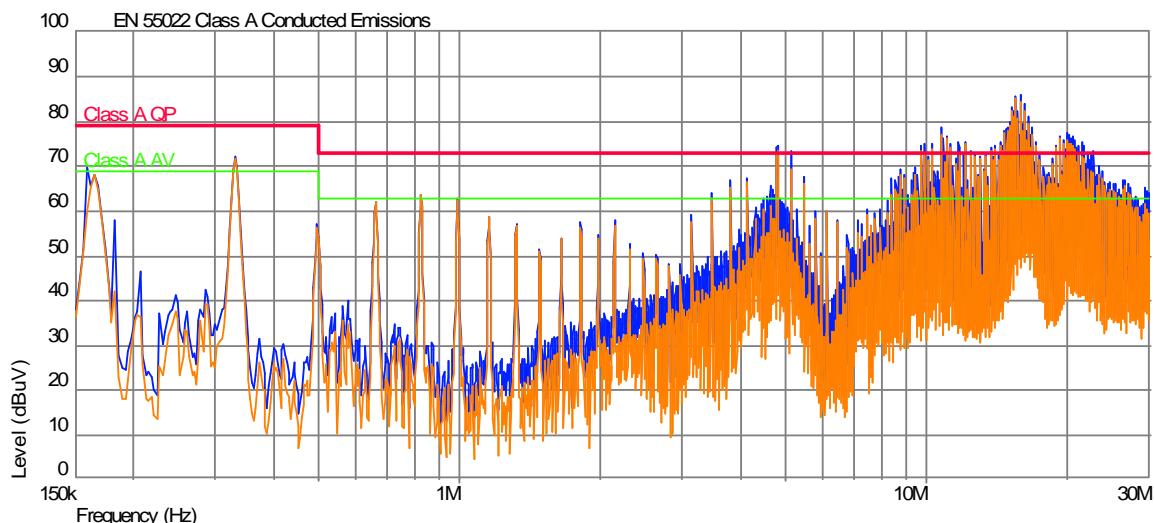


Fig. 7.28 FM conducted EMI measurements

Notice, that SCS has slightly higher peak levels for frequencies below 1MHz, but much lower peak levels for frequencies above 4MHz. Additionally, the average level is more evenly spread for the SCS for frequencies below 1MHz. This is an improvement, because it is easier to construct a filter for frequencies below several MHz than for several tens of MHz.

7.6 Summary

The chapter contains the measurement results of the prototype power supply parameters. The results compare the performance in areas such as output voltage regulation and ripple, step responses, efficiency and conducted EMI emission. Additionally, the operating waveforms are presented, to verify proper switching conditions. The preliminary version of the SCS give promising

results. The switches operate in ZVS conditions and only a small fraction of switching is not ideal. The SCS control give significant improvement in efficiency at less than 40% load area and the level of the conducted EMI emission is lower than in FM control. However, the FM control gives better results in terms of output voltage ripple level and output voltage regulation. Both control methods give similar results in case of load step response.

8 Conclusion

The thesis has been focused on finding a control method which would improve the performance of resonant power converters, with series-parallel LCLC resonant converter as the main application. However, to derive a control method, it is necessary to understand the nature of the resonant converters, which behave differently from classic hard switching converters. Several, most common resonant converter types have been presented along with a less common but attractive series-parallel LCLC resonant converter. Since the resonant converters are prone to failures when operated not properly, a brief discussion about most common failure causes has been included.

The next topic covers various control methods employed in today's applications. Classic PWM methods are briefly discussed along with more advanced methods (like Asymmetrical PWM) dedicated to resonant converters. However most of the methods suffer from either low efficiency at low loads, or operate strictly in a narrow frequency band, which can lead to problems with meeting the EMC regulations.

Thus, the next topic introduces the concept of a novel control method – Sequential Cycle Stealing. The method is based on Pulse Density Modulation. In current version the converter is switching when the output voltage is above a desired threshold and ceases to switch otherwise. The critical part of the control method is the proper synchronization with the resonant current in order to prevent improper switching without ZVS. In order to have better insight in LCLC resonant converter behavior, a generalized analysis of the step response of the LCLC resonant tank has been performed. It has shown that the prediction of the behavior of the resonant tank is not trivial and the best approach for synchronization algorithm would be a real time measurements and reactions instead of predictions. Thanks to reduced average switching frequency, the control method can reduce power losses in areas such as switching losses (especially the output rectifier), ferrite core losses and copper losses.

In order to verify the proposed SCS control method, a test platform has been built. The platform consists of a 3kW full bridge LCLC resonant power converter with a PFC rectifier. Additionally, a universal control board can be attached to allow for easy algorithm implementations and testing. Two digital algorithms have been implemented: FM and SCS. The details of the implementations are described for both algorithms.

The measurement results show that the stated initial objectives are fulfilled. The digital implementation of the control algorithm achieves one of the objectives. The converter operating with SCS can gain up to 14% increase in efficiency at light loads, and still have 1% better efficiency up to around 85% of the load. Additionally, the conducted EMI emission is lower and easier to filter than in FM Control. The step response of both control methods is quite similar and the only field where the SCS loses to FM is the output voltage regulation and ripple. During measurements of the resonant converter with SCSC a problem has been discovered. While the converter operated with SCS, audible noise from inductive components has been observed. This is the direct result of the shape of the STOP signal that controls the switching of the converter. The resulting period of the STOP signal is around 300 μ s (c.a. 3.3kHz) which is well within the audible band. However, the current version is a preliminary design and there is still space to improve the performance of the SCS. One

idea is to replace the output voltage comparator with a Sigma-Delta converter. This can potentially spread the “switching packets” resulting in smaller output ripple. Additionally, this should also reduce the level of the generated audible noise. Another field for improvement is the resonant current sustain algorithm and the synchronization algorithm. The improvement in these areas should reduce the resonant current amplitude during the stop periods, what results in further improving efficiency. A separate topic for further research is finding the minimal resolution and sampling frequency requirements for proper algorithm operation.

Summarizing, all thesis objectives, which have been to develop a digital control method that would improve the performance and EMI emissions of the series-parallel LCLC resonant converter, have been successfully fulfilled.

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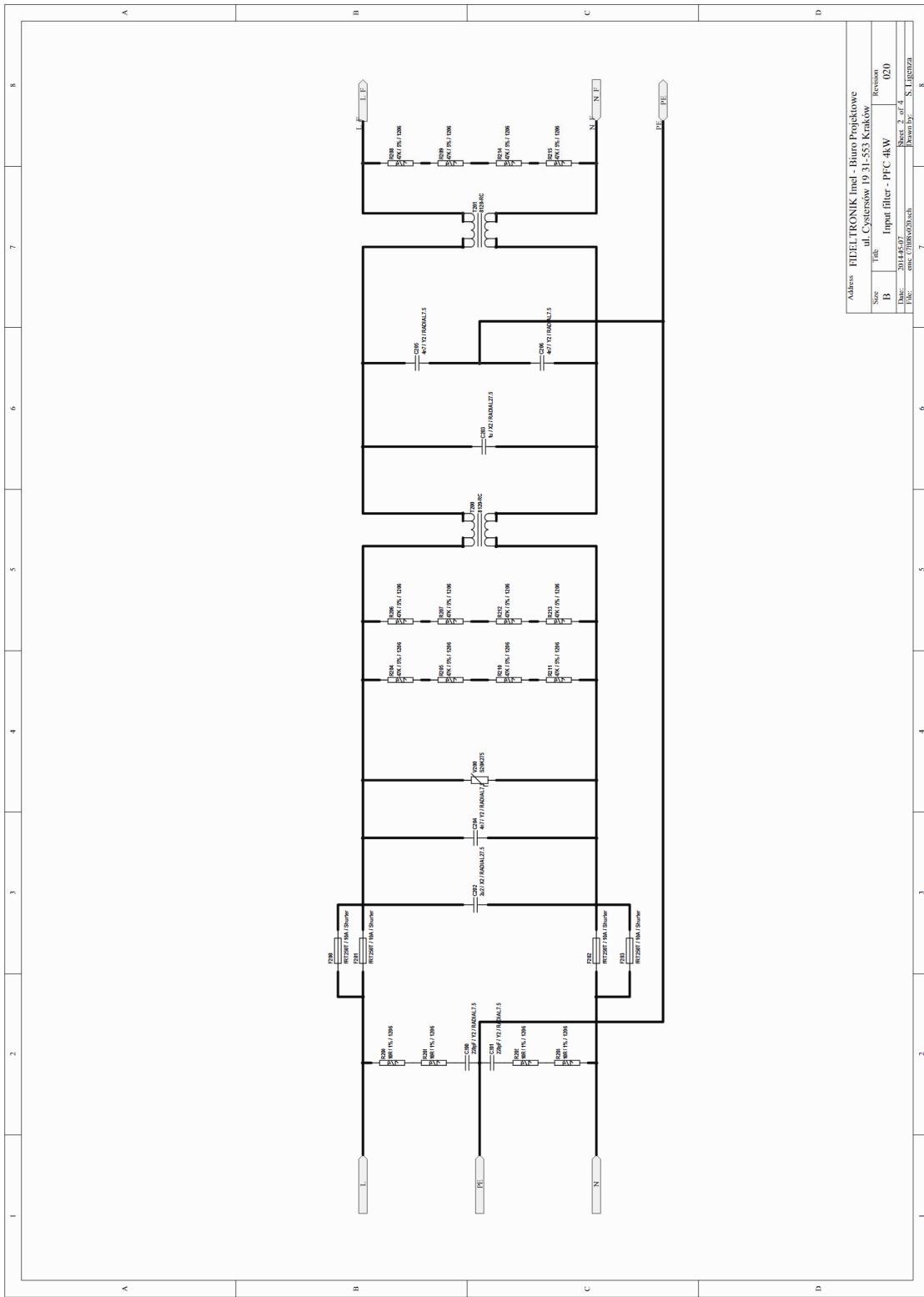
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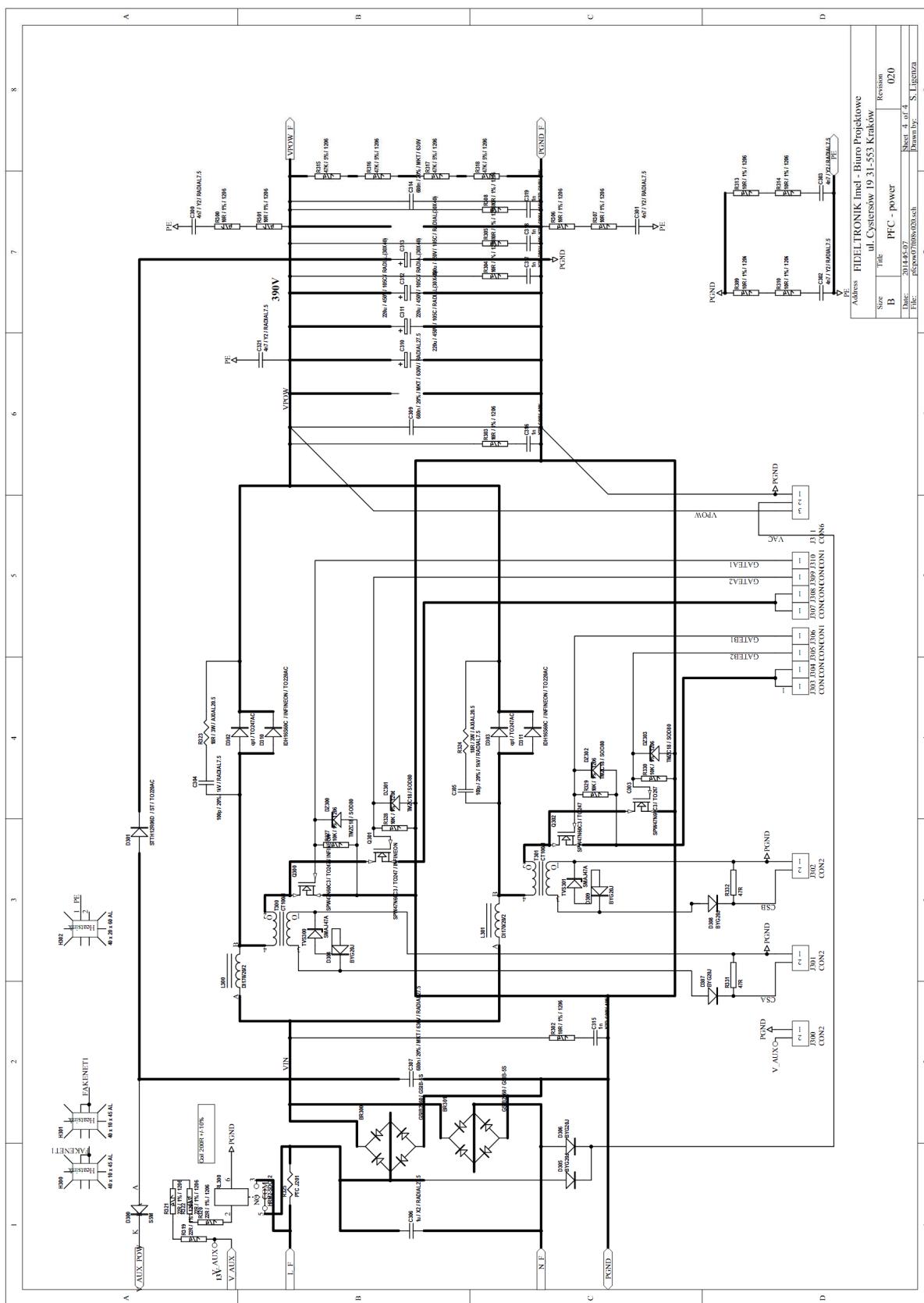
10 Appendix A - Schematics

The appendix contains most important schematics of the constructed prototype.

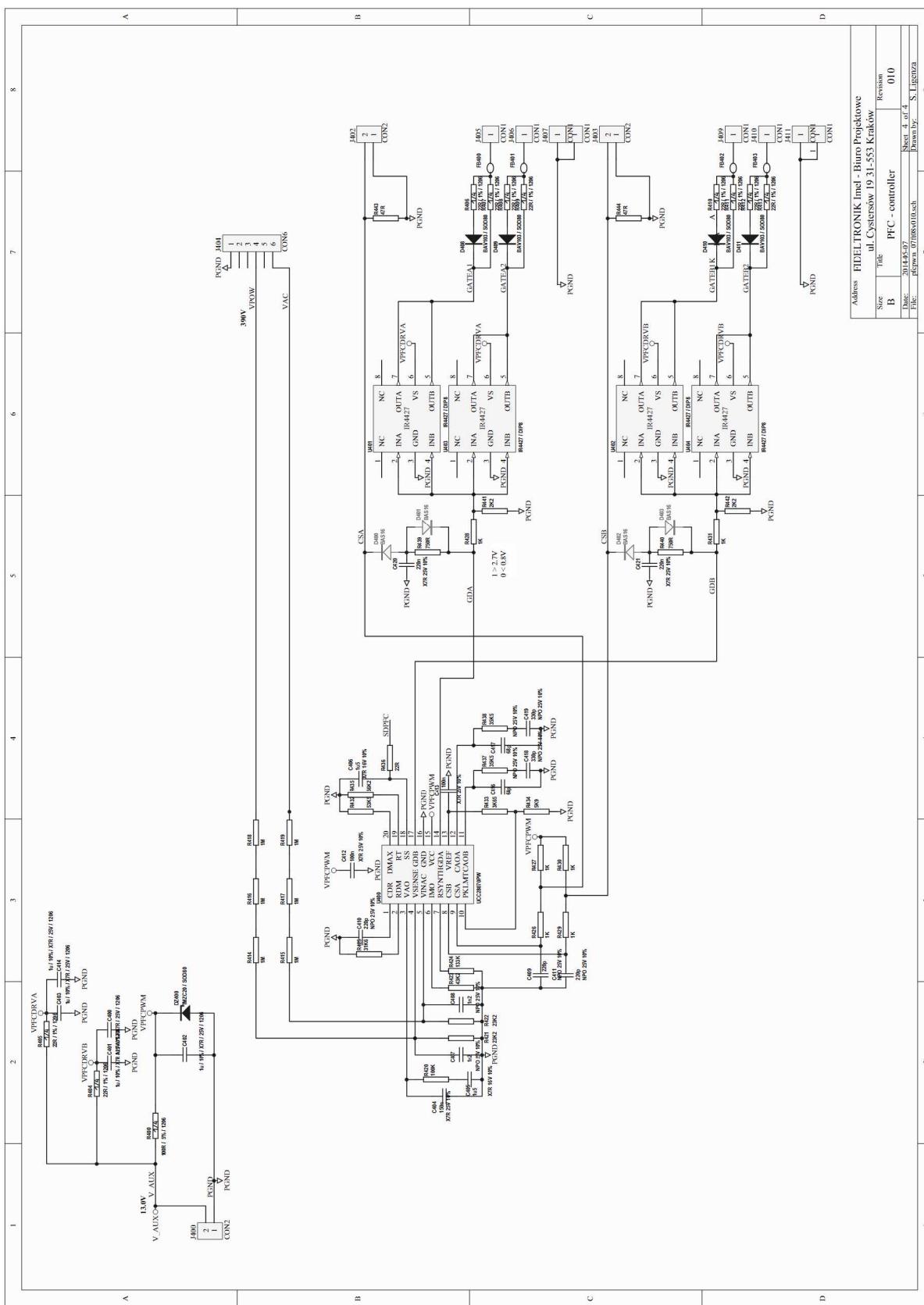
10.1 PFC Module Schematics



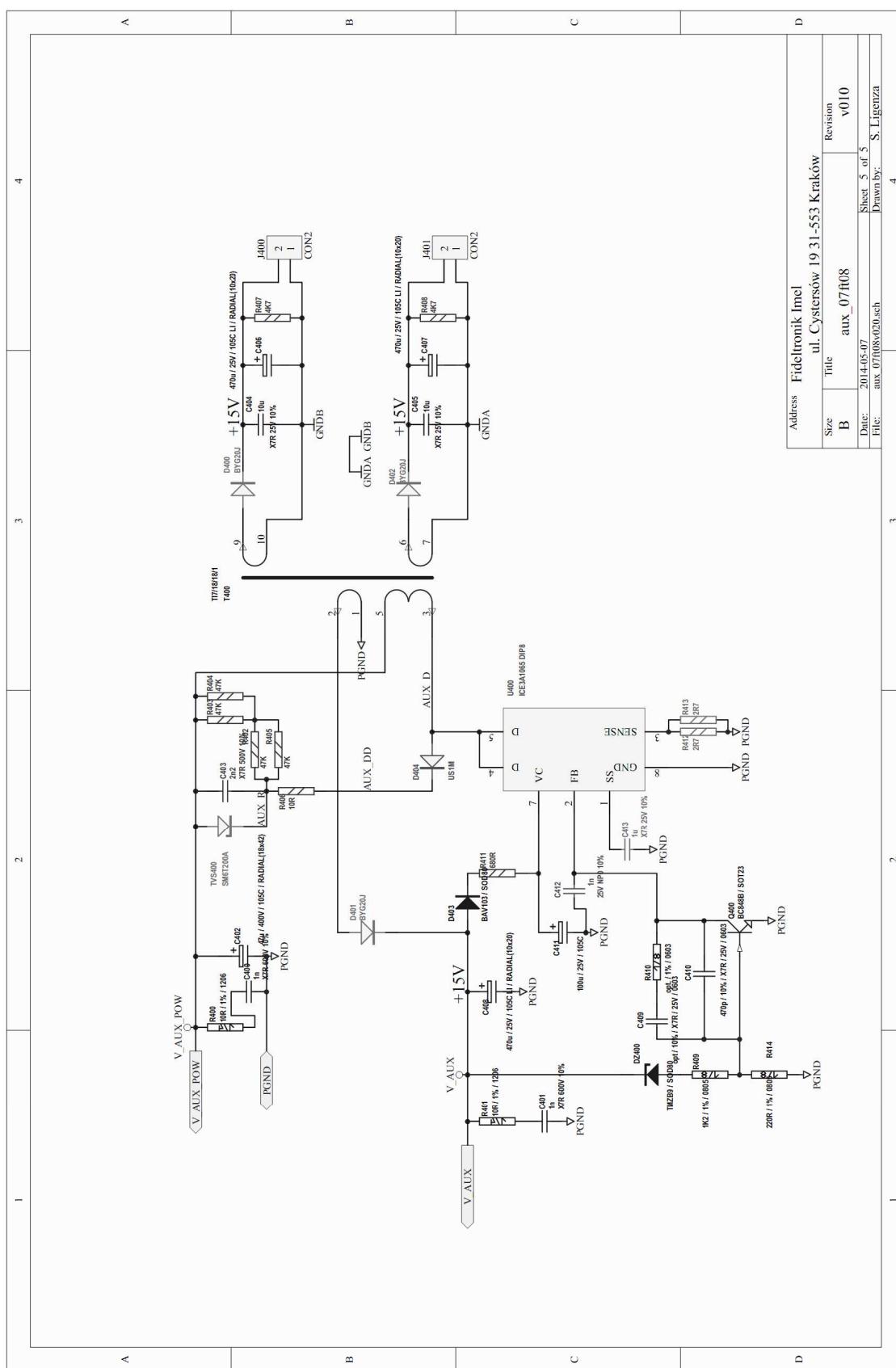
10. Appendix A

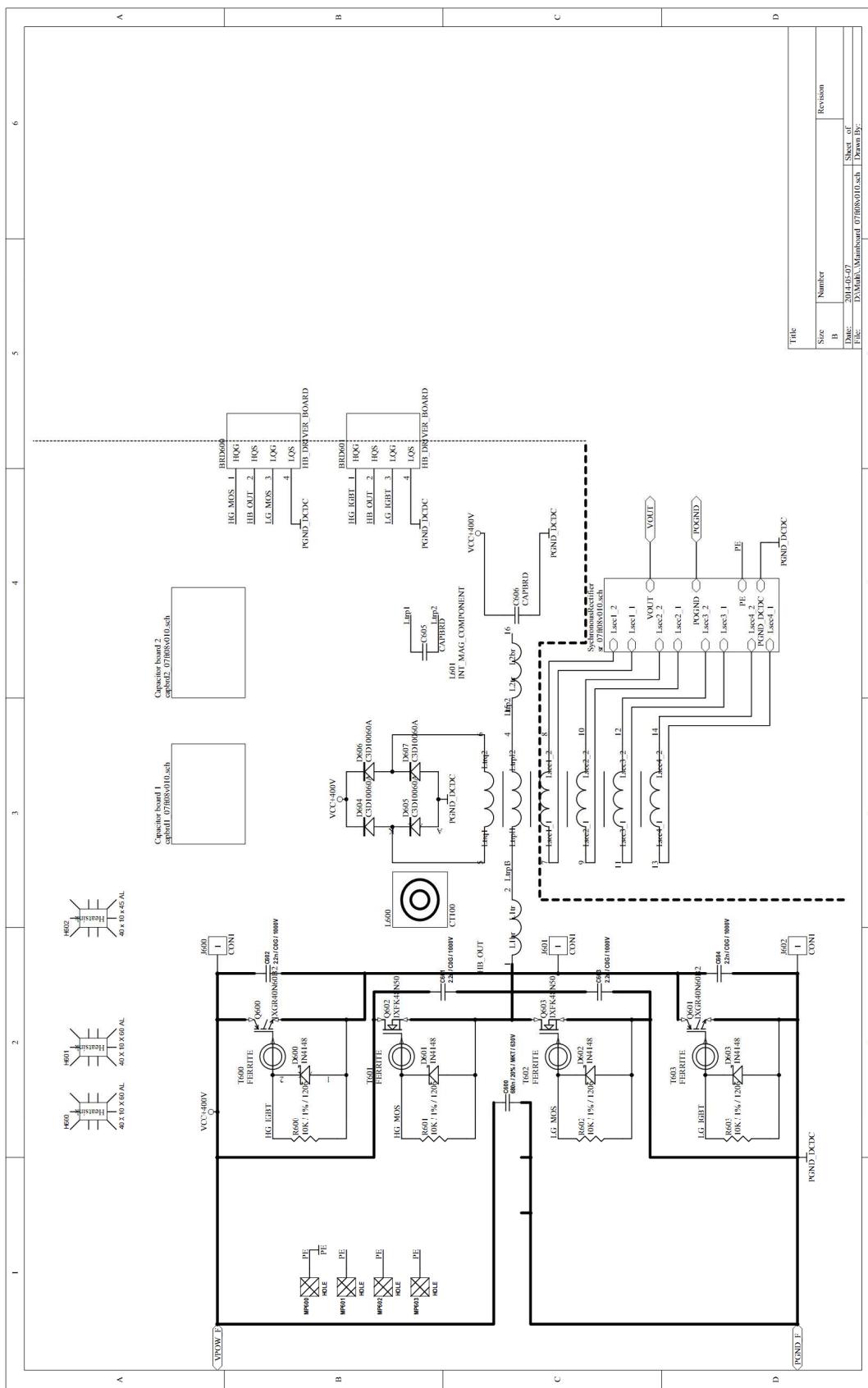


10. Appendix A

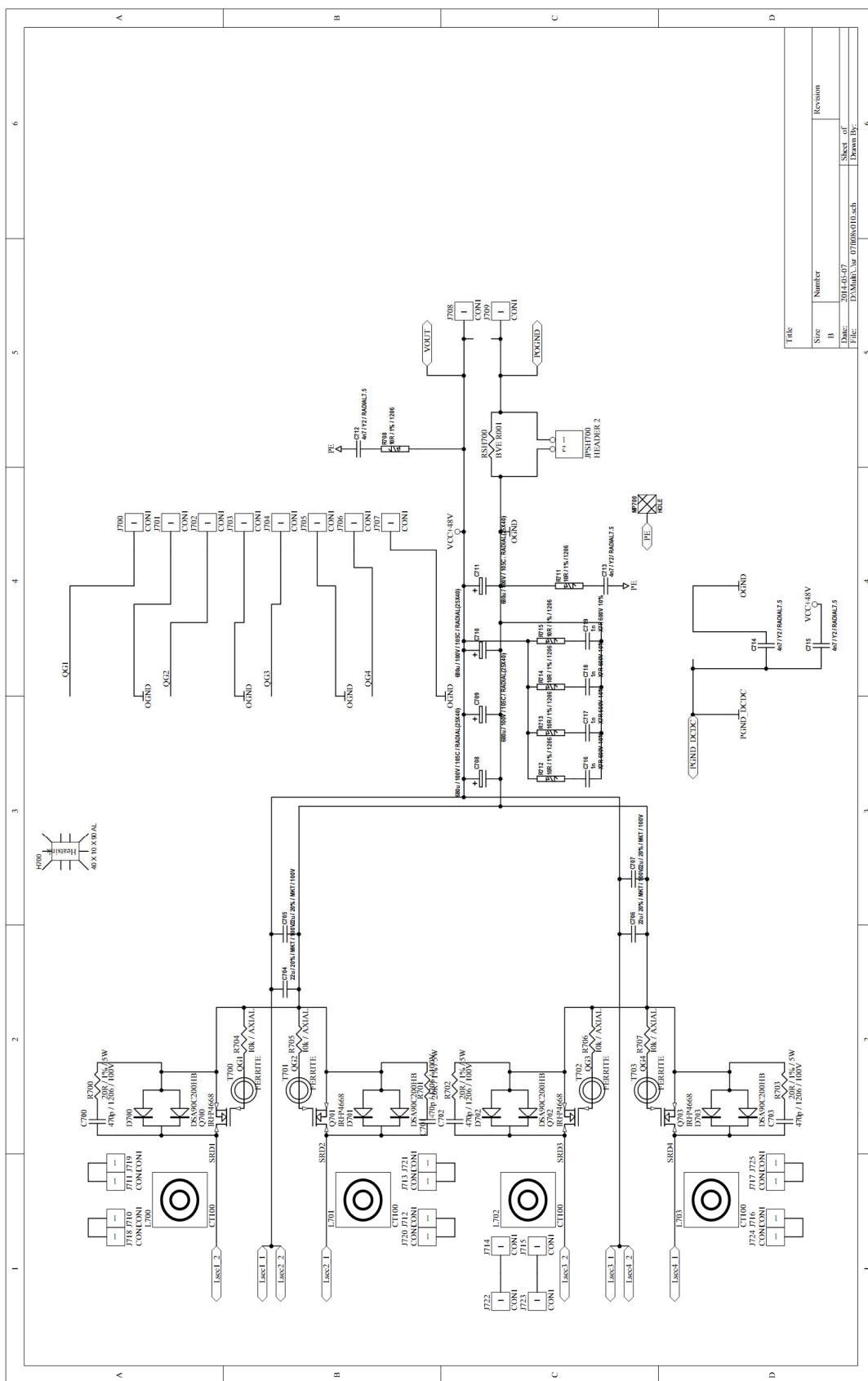


10. Appendix A

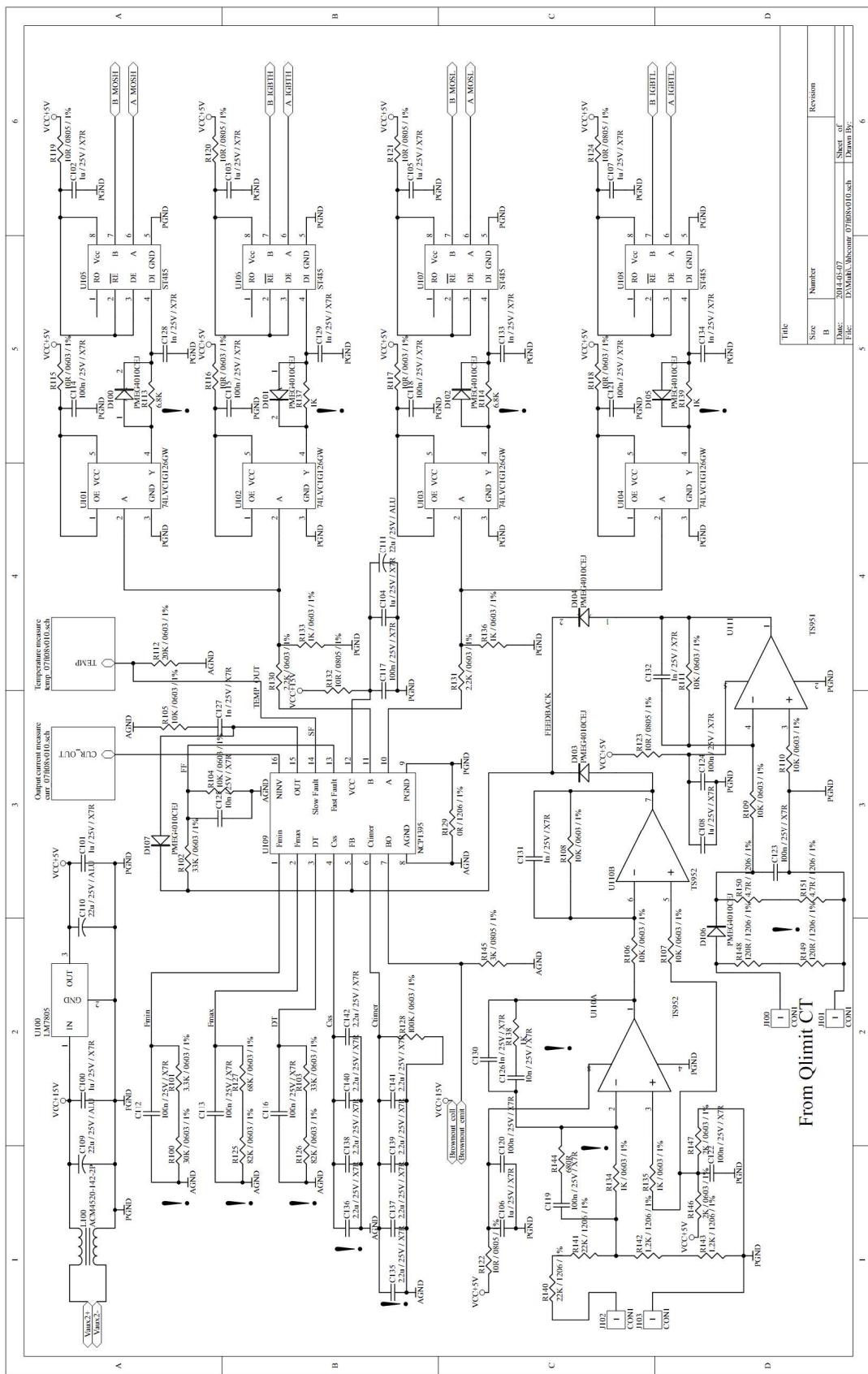


10.2
LCLC Resonant Converter Schematics


10. Appendix A

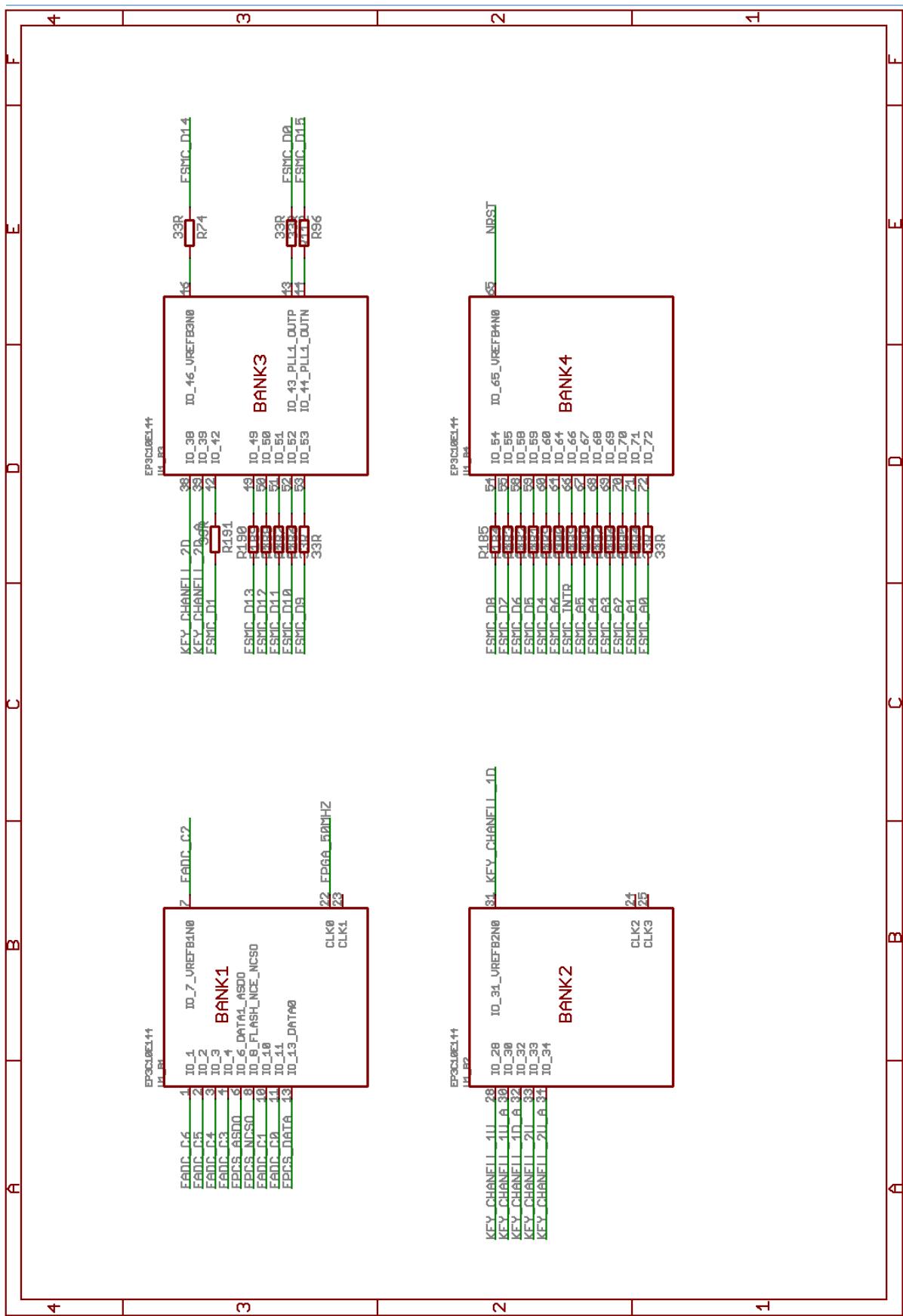


10. Appendix A

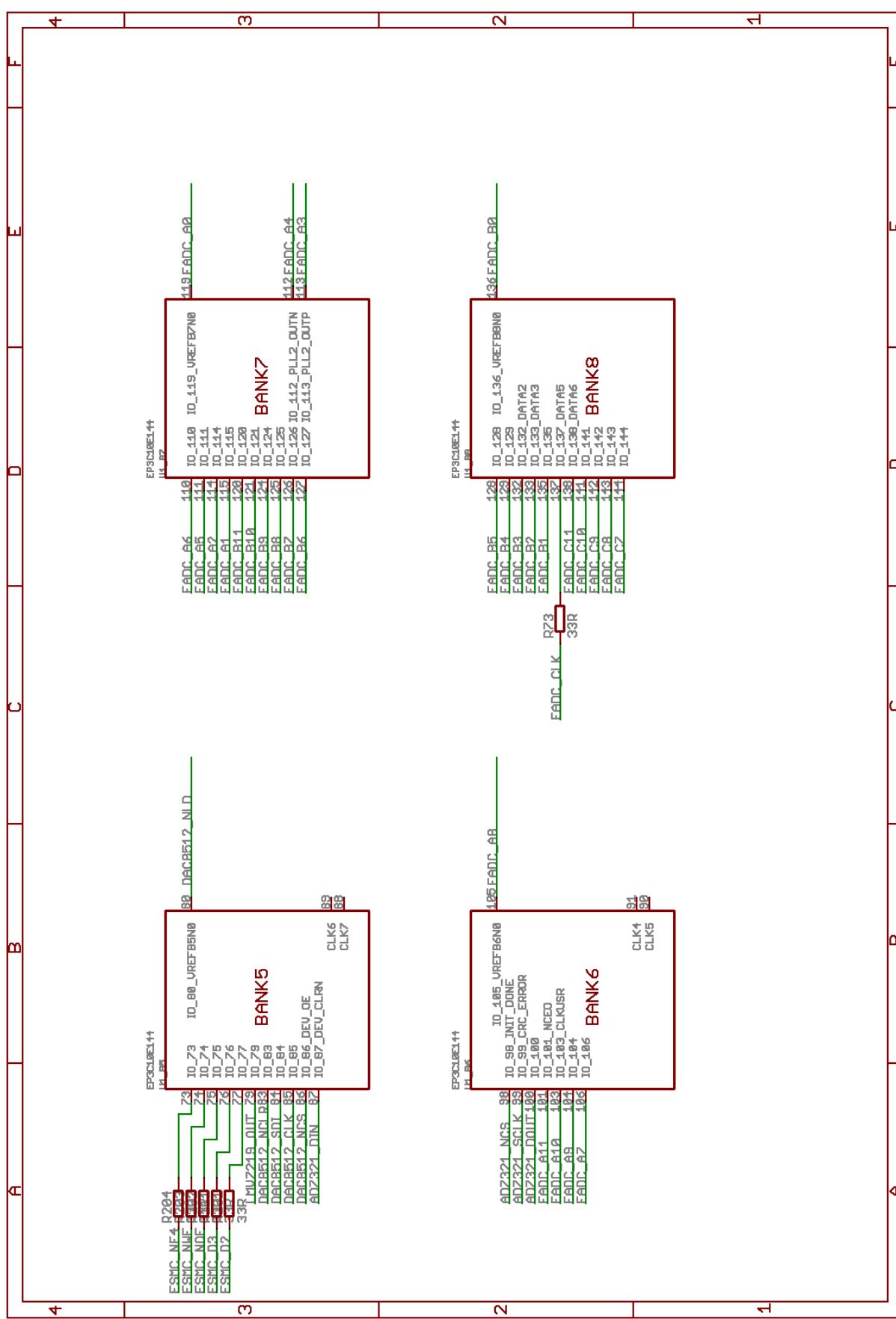


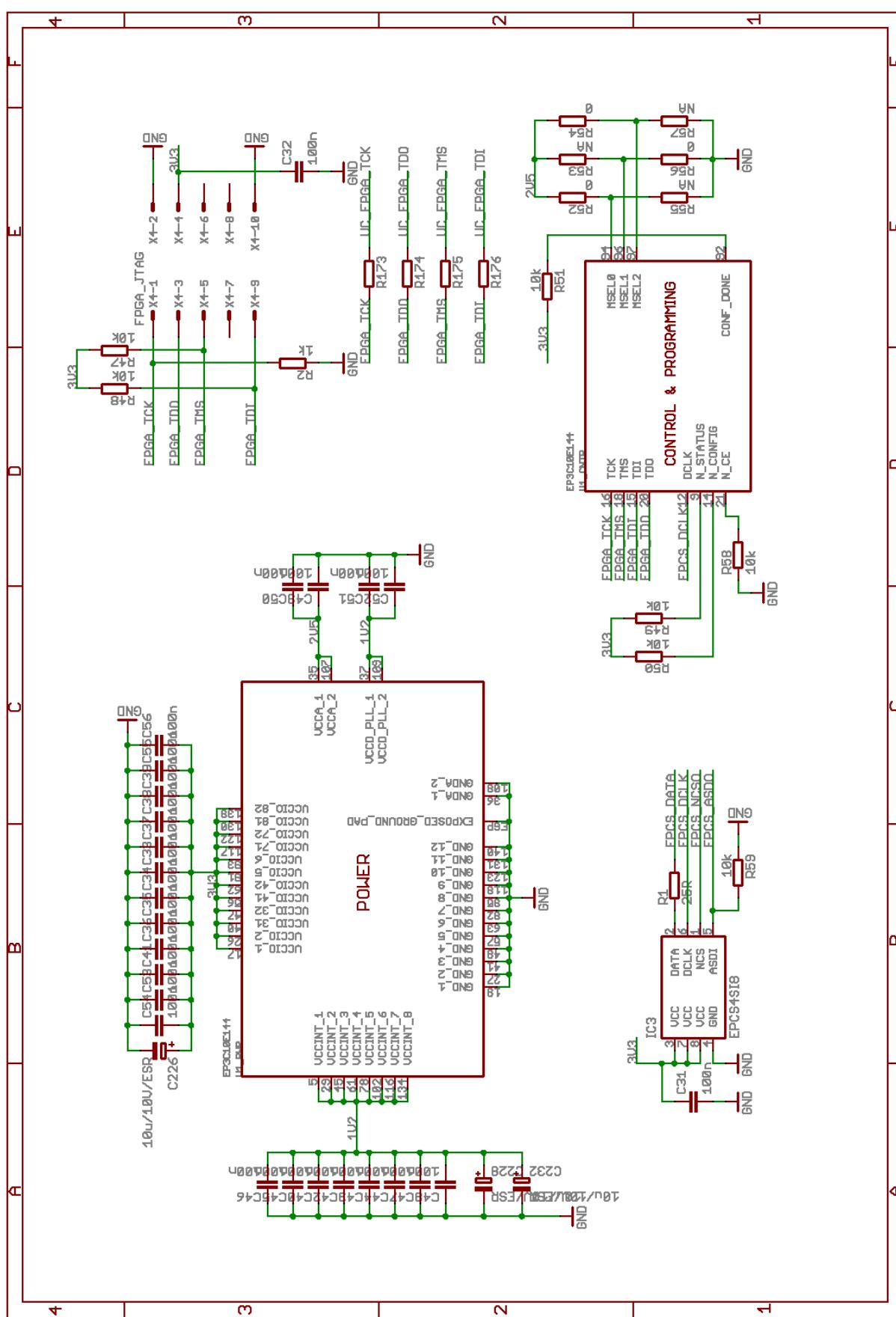
10. Appendix A

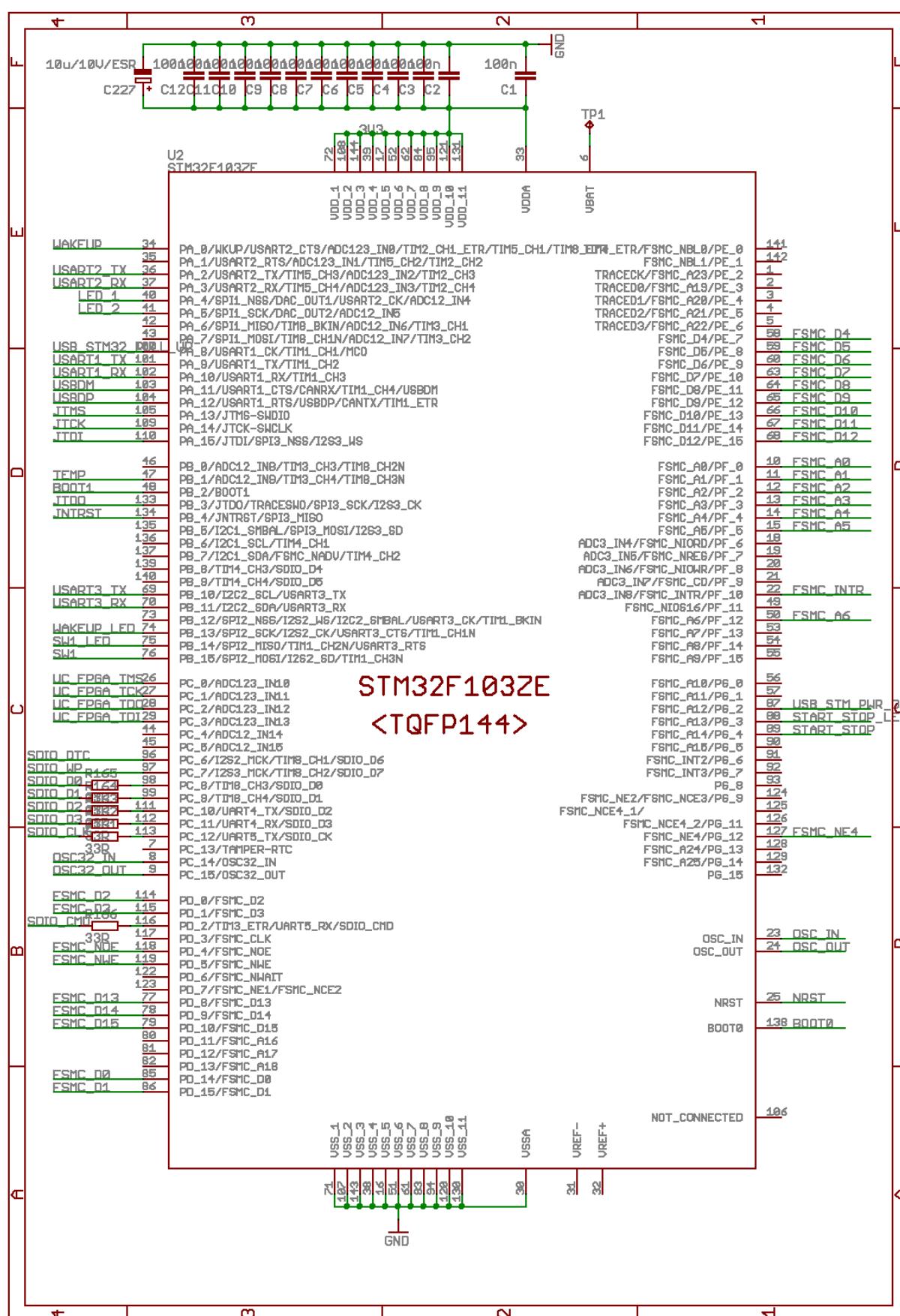
10.3 Control Board Schematics

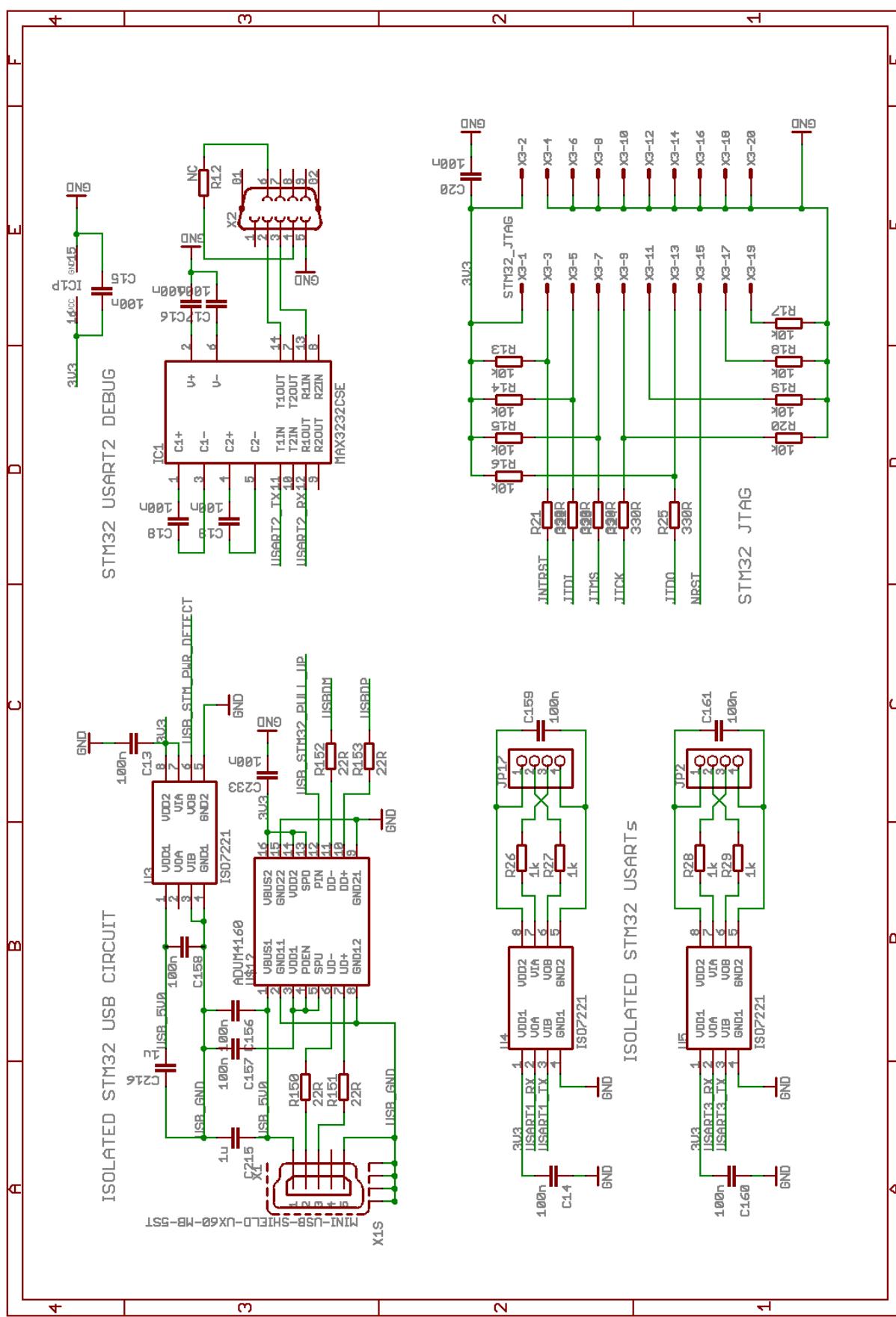


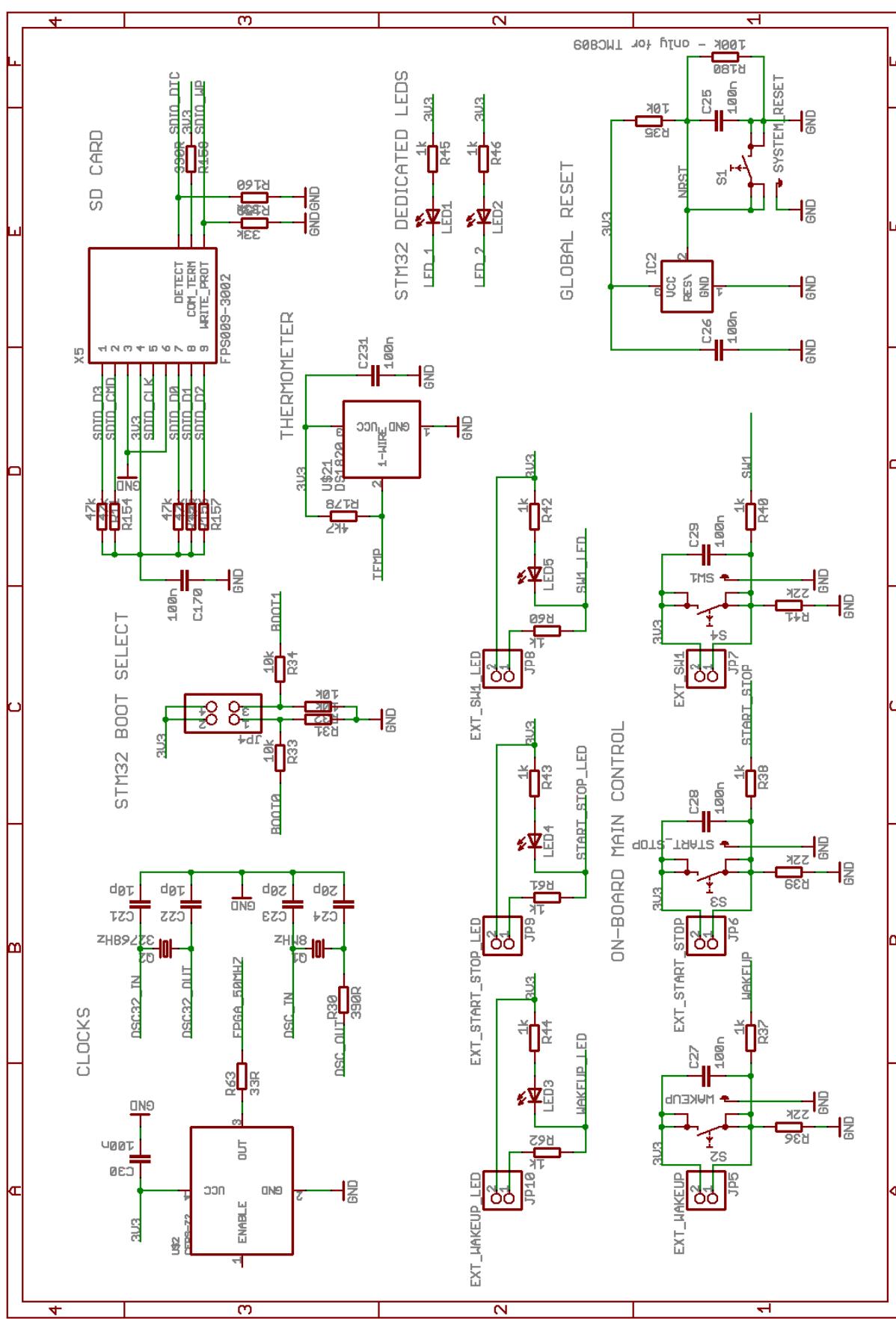
10. Appendix A



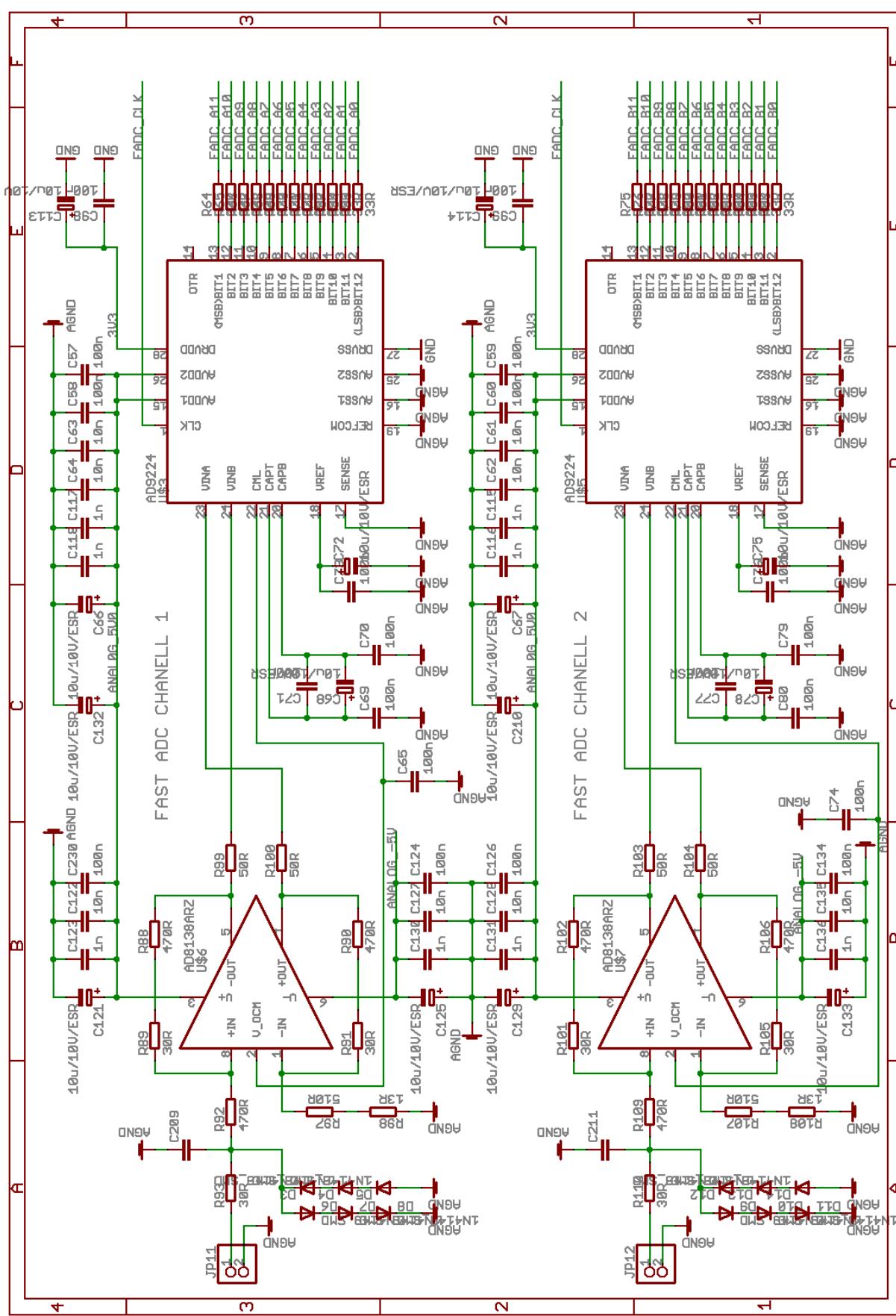


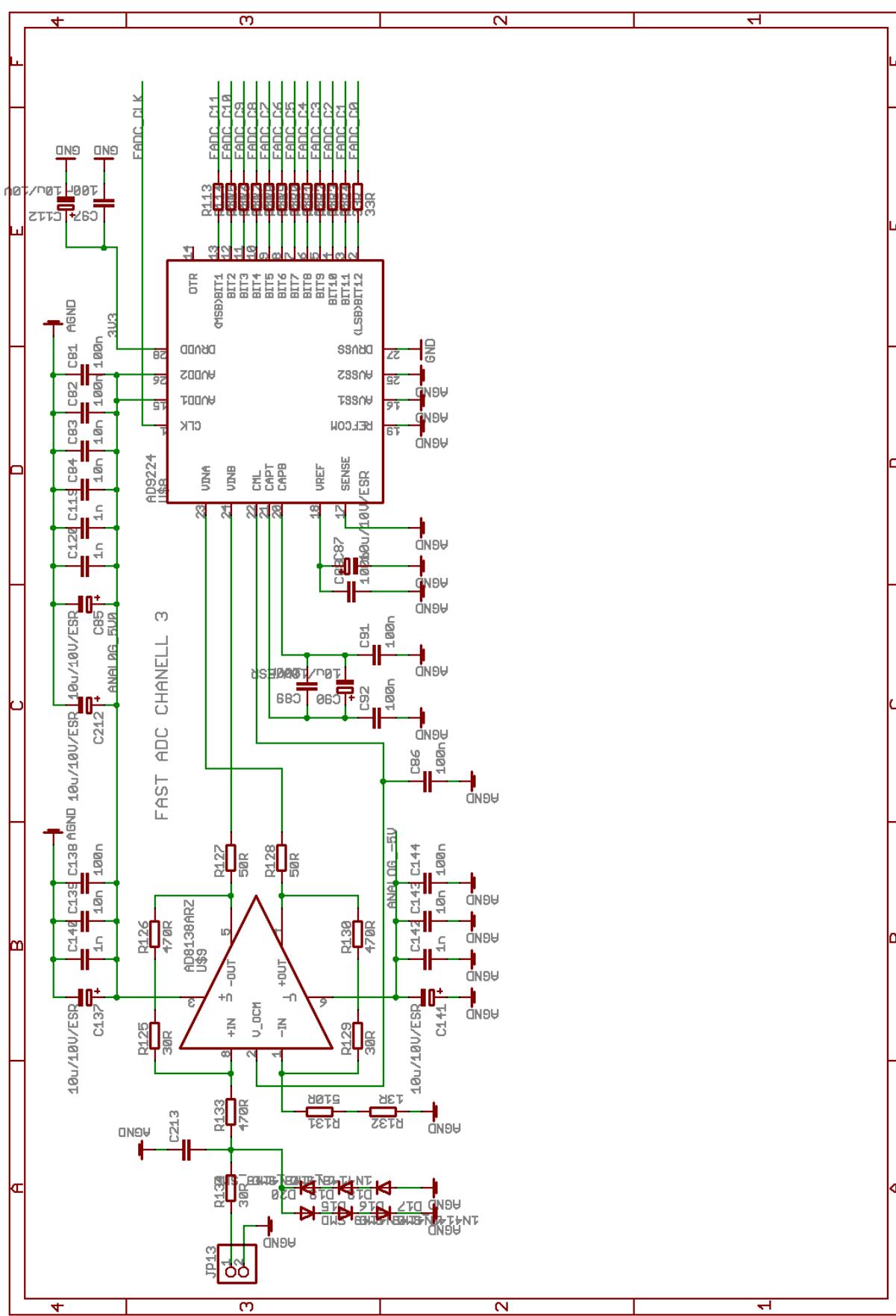


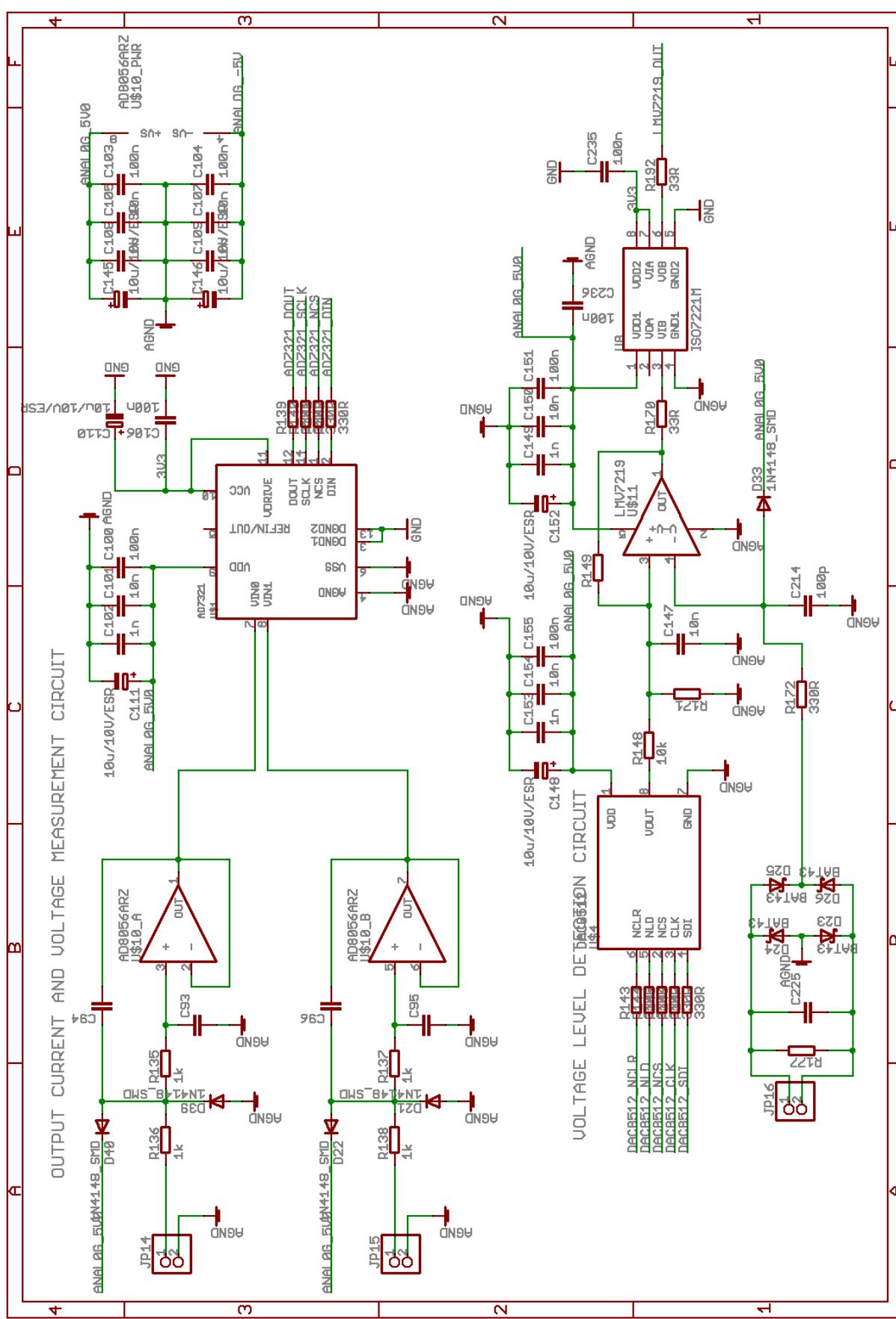




10. Appendix A







10. Appendix A

