ZT3220F, ZT3221F, ZT3222F, ZT3223F, ZT3232F, ZT1385F

Low Power +3V to +5.5V, 1000kbps RS232 Transceivers

Features

- Meets EIA/TIA-232F and CCITT V.28/V.24 specifications for V_{CC} at +3.3V ±10% and +5V ±10%
- Low Quiescent Current: 0.5mA typ., 1mA max.
- Low Shutdown Current (where applicable): 1µA typical, 10µA max.
- Guaranteed High Data Rate 1000kbps
- Proprietary Switch-Capacitor Regulated Voltage Converters (patent pending)
- Proprietary AUTOGREEN Power Saving (patent pending)
- Latch-up Free
- ESD Protection for RS-232 I/O's
  - ±15kV Human Body Model (HBM)
  - ±15kV EN61000-4-2 Air Gap Discharge
  - ±8kV EN61000-4-2 Contact Discharge
- Drop-in Replacements for MAX3220E, SP3220E, MAX3221E, ICL3221E, MAX3222E, ICL3222E, SP3222EU, MAX3223E, ICL3223E, SP3223EU, MAX3232E, ICL3232E, SP3232EU, LT1385 and SP385E
- Standard Data Rate at 250kbps Available on ZT32xxE Series

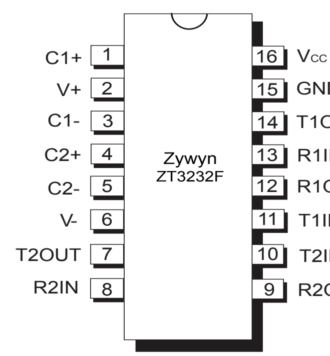
General Description

The ZT32xxF series devices are 3V powered EIA/TIA-232 and V.28/V.24 communication interfaces with low power requirements. They consist of two line drivers, two line receivers and the proprietary switch-capacitor regulated voltage converters. The ZT3220F has a 1Tx and 1Rx configuration. These devices operate from a single 3V to 5.5V power supply at the guaranteed data rate of 1000k bits/sec with enhanced electrostatic discharge (ESD) protection in all RS232 I/O pins exceeding ±15kV EN61000-4-2 Air Gap Discharge and ±8kV EN61000-4-2 Contact Discharge.

The ZT3221F and ZT3223F features the AUTOGREEN (patent pending) proprietary function which automatically powers down the on-chip regulated voltage converters and driver circuits when an RS-232 cable is disconnected from the host interface or when a connected peripheral device is turned off.

Applications

- Battery-Powered And Hand-Held Applications
- Notebooks, Subnotebooks, and Palmtops
- Industrial and Embedded PCs
- Data Cables for Cell Phones and PDAs
- Terminal Adapters and POS terminals
- Peripherals interface
- Routers and HUBs



Product Selection Guide

Part Number	Power Supply	RS232 Drivers	RS232 Receivers	Data Rate (kbps)	15KV ESD IEC1000 4-2	Receiver Enable	SHUTDOWN Enable	AUTOGREEN Function	Number of Pins	Package Type
ZT3220F	+3V to +5.5V	1	1	1000	RS232 I/O	YES	YES	NO	16	SSOP, TSSOP, WSOIC
ZT3221F	+3V to +5.5V	1	1	1000	RS232 I/O	YES	YES	YES	16	SSOP, TSSOP
ZT3222F	+3V to +5.5V	2	2	1000	RS232 I/O	YES	YES	NO	18, 20	18-WSOIC 20-SSOP, 20-TSSOP,
ZT3232F	+3V to +5.5V	2	2	1000	RS232 I/O	NO	NO	NO	16	NSOIC, WSOIC, SSOP, TSSOP, QFN
ZT3223F	+3V to +5.5V	2	2	1000	RS232 I/O	YES	YES	YES	20	SSOP, TSSOP
ZT1385F	+3V to +5.5V	2	2	1000	RS232 I/O	NO	YES	NO	18, 20	18-WSOIC, 20-SSOP

Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Power Supply, (V_{CC})..−0.3V to +6.0V
V+.. −0.3V to +7.0V
V−+0.3V to −7.0V
|V+| + |V-| .... +13.0V
I_{CC} (DC V_{CC} or GND current)..±100mA
Input Voltages
TxIN,$\overline{\text{GREEN}}$, $\overline{\text{SHUTDOWN}}$, $\overline{\text{EN}}$......................................−0.3V to +6.0V
RxIN ....±25V

Output Voltages

TxOUT .... ±15V
RxOUT, $\overline{\text{IDLE}}$ ....–0.3V to (V_{CC} +0.3V)
Short-Circuit Duration
TxOUT .... Continuous
Operating Temperature ....−40°C to +85°C
Storage Temperature ....−65°C to +150°C

Power Dissipation Per Package
16-pin SSOP (derate 7.20mW/°C above +70°C)................584mW
16-pin nSOIC (derate 10.00mW/°C above +70°C)............720mW
16-pin WSOIC (derate 10.10mW/°C above +70°C) 787mW
16-pin TSSOP (derate 6.80mW/°C above +70°C).............556mW
16-pin PDIP (derate 11.20mW/°C above +70°C) 896mW
16-pin QFN (derate 24.00mW/°C above +70°C) 2000mW
18-pin PDIP (derate 12.60mW/°C above +70°C) 962mW
18-pin WSOIC (derate 11.10mW/°C above +70°C) 850mW
20-pin PDIP (derate 12.80mW/°C above +70°C) 976mW
20-pin SSOP (derate 8.10mW/°C above +70°C)................647mW

Storage Considerations

Storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 168 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for 12 hours at 125°C in order to remove moisture prior to soldering. Zywyn ships product in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH. The MSL of this product is 3.

Electrical Characteristics

Unless otherwise stated, V_{CC} = +3.0V to +5.0V, $T_A = T_{min}$ to T_{max}, C1 to C4 = 0.1µF, typical values apply at V_{CC} = +3.3V or +5.0V and T_A = 25°C.

Parameter	Condition	Min	Typ	Max	Units
TTL Logic Input	T_1IN, T_2IN, $\overline{GREEN}$, $\overline{SHUTDOWN}$, $\overline{EN}$				
TTL Logic Output	R_1OUT, R_2OUT, $\overline{IDLE}$				
RS-232 Input	R_1IN, R_2IN				
RS-232 Output	T_1OUT, T_2OUT				
Charge Pump Pin	C_1P, C_1N, C_2P, C_2N				
Power Pin	V_{CC}, V_{GND}, V_{DD}, V_{SS}				
Charge Pump Caps	C_1P, C_1N, C_2P, C_2N	0.1	0.1	1	µF
Temp 0°C to +70°C	Commercial Grade	0	+25	+70	°C
Temp –40°C to +85°C	Industrial Grade	–40	+25	+85	°C
V_{CC} Voltage Range	V_{CC} = +5.0V Supply	4.5	5	5.5	V
	V_{CC} = +3.3V Supply	3	3.3	3.6	V
Supply Current	TTL Inputs = V_{CC}/GND, RS-232 Input = float, V_{CC} = 3.3V (For ZT3220F, ZT3222F, ZT3232F and ZT1385F)		0.5	1	mA
Supply Current, AUTOGREEN Disabled	$\overline{GREEN}$ = V_{CC}, (For ZT3221F and ZT3223F); $\overline{SHUTDOWN}$ = V_{CC}, (For ZT3221F, ZT3222F, ZT1385F and ZT3223F), TTL Inputs = V_{CC}/GND, RS-232 Input = float, V_{CC} = 3.3V		0.5	1	mA
Supply Current, AUTOGREEN Enabled	$\overline{GREEN}$ = GND, (For ZT3221F and ZT3223F); $\overline{SHUTDOWN}$ = V_{CC}, (For ZT3221F, ZT3222F, ZT1385F and ZT3223F), TTL Inputs = V_{CC}/GND, RS-232 Input = float, V_{CC} = 3.3V		1	10	µA
Supply Current, SHUTDOWN Enabled	$\overline{GREEN}$ = V_{CC}/GND, (For ZT3221F and ZT3223F); $\overline{SHUTDOWN}$ = GND, (For ZT3221F, ZT3222F, ZT1385F and ZT3223F), TTL Inputs = V_{CC}/GND, RS-232 Inputs = float, V_{CC} = 3.3V		1	10	µA
TTL LOGIC Input					
Input Threshold Low				0.8	V
Input Threshold High	V_{CC} = +5.0V Supply	2.4			V
Input Threshold High	V_{CC} = +3.3V Supply	2			V
Input Hysteresis			0.5		V
Input Leakage Current	$V_{IN} = V_{CC}$ and GND, TIN, $\overline{EN}$, $\overline{GREEN}$, $\overline{SHUTDOWN}$		±0.01	±1	µA
Input Leakage Current	$V_{IN} = V_{CC}$ and GND, TIN (For ZT1385F)		50	200	µA
TTL LOGIC Output					
Output Voltage Low	I_{OUT} = 1.6mA			0.4	V
Output Voltage High	I_{OUT} = –1.0mA	V_{CC}–0.6	V_{CC}–0.1		V
Output Leakage Current	Receiver Outputs Disabled, $V_{OUT} = V_{CC}$ or GND, $\overline{SHUTDOWN}$ = GND, $\overline{EN}$ = V_{CC}		±0.05	±10	µA
Receiver Input					
Input Voltage Range	$T_A = T_{min} - T_{max}$	–25		+25	V
Input Threshold Low	T_A = 25°C, V_{CC} = 5.0V	0.8	1.5		V
	T_A = 25°C, V_{CC} = 3.3V	0.6	1.2		V
Input Threshold High	V = 25°C			2.4	V
Input Hysteresis	T_A = 25°C		0.5		V
Input Resistance	V_{IN} = ±25V, T_A = 25°C	3		7	kΩ
Transmitter Output					
Output Voltage Swing	R_L = 3kΩ, All Outputs are loaded	±5			V
Output Resistance	$V_{CC} = V_{DD} = V_{SS}$ = GND, V_{OUT} = ±2V	300			Ω
Output Short-Circuit Current	V_{OUT} = GND			±60	mA
Output Leakage Current	Transmitter Disabled, V_{OUT} = ±12V		±5		µA
Parameter	Condition	Min	Typ	Max	Units
Timing Characteristics					

Maximum Data Rate Refers to Figure 1 and 2.	$R_L = 3k\Omega$, $C_L = 250pF$, One Transmitter Switching, $T_A = 25°C$	1,000			kbps
Transition-Region Slew Rate	$R_L = 3\sim7k\Omega$, $C_L = 150pF$ to 250pF, One Transmitter Switching, $T_A = 25°C$, Measured from +3V to –3V or –3V to +3V		60		V/µs
Receiver Propagation t_{PLH} Receiver Propagation t_{PHL} Receiver Skew Receiver Output Enable Time Receiver Output Disable Time	$C_L = 150pF$ $C_L = 150pF$ $t_{PHL} - t_{PLH}$ For ZT3220F, ZT3221F, ZT3222F, ZT3223F only For ZT3220F, ZT3221F, ZT3222F, ZT3223F only		0.15 0.15 50 0.2 0.2		µs µs ns µs µs
AUTOGREEN Timing Receiver Input to $\overline{\text{IDLE}}$ Output High Receiver Input to $\overline{\text{IDLE}}$ Output Low Power Save Mode to Transmitter Enabled	 For ZT3221F and ZT3223F only For ZT3221F and ZT3223F only For ZT3221F and ZT3223F only		 1 30 100		 µs µs µs
ESD Tolerance ESD HBM EN61000-4-2 Contact Discharge EN61000-4-2 Air Gap Discharge	 RS-232 Inputs and Outputs RS-232 Inputs and Outputs RS-232 Inputs and Outputs		 ±15 ±8 ±15		 kV kV kV

Product Cross Reference

Part Number	Pin-to-Pin Cross MAXIM	Pin-to-Pin Cross Intersil	Pin-to-Pin Cross TI	Pin-to-Pin Cross ST-M	Pin-to-Pin Cross EXAR
ZT3220F	n/a	n/a	SNx5C3220	n/a	SP3220U
ZT3221F	n/a	n/a	SNx5C3221	n/a	n/a
ZT3222F	n/a	n/a	SNx5C3222	n/a	SP3222U
ZT3232F	n/a	n/a	SNx5C3232	n/a	SP3232U
ZT3223F	MAX3225E	n/a	SNx5C3223	n/a	SP3223U

Pin Description

Pin Numbers								Name	Description
ZT3220F	ZT3221F	ZT3222F		ZT3232F	ZT1385F		ZT3223F		
16 Pins	16 Pins	18 Pins	20 Pins	16 Pins	18 Pins	20 Pins	20 Pins		
1	1	1	1	–	–	–	1	$\overline{EN}$	Receiver Enable. Logic low for Normal operation. Logic high to force the receiver outputs into high impedance state
2	2	2	2	1	2	2	2	C1+	Positive terminal of the boostrapped voltage switch capacitor
3	3	3	3	2	3	3	3	V+	Regulated +5.4V output generated by the voltage converter
4	4	4	4	3	4	4	4	C1-	Negative terminal of the boostrapped voltage switch capacitor
5	5	5	5	4	5	5	5	C2+	Positive terminal of the inverted voltage switch capacitor
7	7	7	7	6	7	7	7	V-	Regulated –5.7V output generated by the voltage converter
6 ed	6	6	6	5	6	6	6	C2-	Negative terminal of the invert- voltage switch capacitor
8	8	14	16	13	14	16	16	R1 IN	First RS232 receiver input
–	–	9	9	8	9	9	9	R2 IN	Second RS232 receiver input
9	9	13	15	12	13	15	15	R1 OUT	First TTL/CMOS receiver output
–	–	10	10	9	10	12	10	R2 OUT	Second TTL/CMOS receiver output
11	11	12	13	11	12	14	13	T1 IN	First TTL/CMOS transmitter input
–	–	11	12	10	11	13	12	T2 IN	Second TTL/CMOS transmitter input
13	13	15	17	14	15	17	17	T1 OUT	First RS232 transmitter output
–	–	8	8	7	8	8	8	T2 OUT	Second RS232 transmitter output
–	10	–	–	–	–	–	11	$\overline{IDLE}$	TTL/CMOS output indicating AUTOGREEN or SHUTDOWN status
16	16	18	20	–	18	20	20	$\overline{SHUTDOWN}$	Shutdown control. A logic LOW to disable drivers and voltage converter
–	12	–	–	–	–	–	14	$\overline{GREEN}$	A logic HIGH to override AUTO-GREEN circuitry keeping transmitters ON. (SHUTDOWN must be HIGH)
14	14	16	18	15	16	18	18	GND	Ground
15	15	17	19	16	17	19	19	V_{CC}	+3V to +5.5V Supply Voltage
10, 12	–	–	11, 14	–	1	1, 10, 11	–	NC	No connect

Pin Description

ZT3232LFEQ (5x5 16-QFN Package)

Pin Number	Pin Name	Pin Function
1	C1-	Negative terminal of the boostrapped voltage switch capacitor
2	C2+	Positive terminal of the inverted voltage switch capacitor
3	C2-	Negative terminal of the boostrapped voltage switch capacitor .
4	V-	Regulated –5.7V output generated by the voltage converter
5	T2OUT	Second RS232 transmitter output
6	R2IN	Second RS232 receiver input.
7	R2OUT	Second TTL/CMOS receiver output.
8	T2IN	Second TTL/CMOS transmitter input.
9	T1IN	First TTL/CMOS transmitter input
10	R1OUT	First TTL/CMOS receiver output.
11	R1IN	First RS232 receiver input.
12	T1OUT	First RS232 transmitter output
13	GND	Ground.
14	VCC	+3V to +5.5V Supply Voltage
15	C1+	Positive terminal of the boostrapped voltage switch capacitor
16	V+	Regulated +5.4V output generated by the voltage onverter

Circuit Description

Proprietary Switch-Capacitor Regulated Voltage Converter

Different from other suppliers, Zywyn uses a patent pending switch-capacitor voltage-controlled source and sink current generators design to provide powerful bipolar voltages to maintain compliant EIA/RS232 levels regardless of power supply fluctuations. The design consists of an internal regulated oscillator, a two phase clock cycling, regulated complementary MOS switches, fast switching diode and switch capacitors.

The switch capacitor bi-directional current generators operate with Zywyn's proprietary smartly regulated complementary MOS switches and fast switching diode from its proprietary high voltage process technology. The efficiency of these bi-directional current generators is well over 70%. The switching frequency is generated by an internal oscillator and regulated by the current loads. The switch capacitor pump design delivers higher negative bucked voltage than the positive boosted voltage to achieve a balanced voltage controlled source and sink current generators resulting a balanced bipolar voltage supplies to the chip.

With its unique proprietary design technique, Zywyn's interface product series provide a better power efficient, stable and compliant EIA/RS232 levels with superior low power consumption.

Controlled Power-Down

The ZT3220F, ZT3221F, ZT3222F and ZT3223F have a low-power shutdown mode controlled by the SHUTDOWN pin. During shutdown the driver output and the switch-capacitor regulated voltage converter are disabled with the supply current falls to less than 1μA.

The ZT3221F and ZT3223F use Zywyn's patent pending AUTOGREEN circuitry to set/reset latches, which enable the circuit shutdown function when a RS232 cable is disconnected or when the peripheral is turned off and reduce the power supply drain to a 1μA supply current. Otherwise, when a RS232 cable is connected or when the peripheral is turned on, the devices will automatically become active again.

ESD Immunity

Electro-Static Discharge (ESD) is an important factor when implementing a serial port into a system. In some applications, it is crucial that the ESD protection for the system must meet a certain tolerance level. Since RS232 transceiver devices are exposed to the outside world, there are many environmental factors that can effect the serial port and even subject it to transients that could potentially damage the transceiver itself.

The RS232 transceiver is usually routed from the serial port connector to the transceiver IC through the metal trace on the printed circuit board. This trace will have some small amount of resistance that will add some protection in terms of limiting transient current to the IC. However for added voltage protection, transient voltage suppressors (TVS) or tranzorbs, which are back-to-back diode arrays clamp, are usually necessary to protect the serial port circuity.

To further reduce cost within their system, more engineers are requiring higher ESD tolerances from the transceiver ICs themselves without having to add costly TVS circuitry. Zywyn's RS232 transceivers includes built-in transient voltage suppression where external ESD circuitry is not necessary to meet the MIL-STD-883, Method 3015, Human Body Model and the EN61000-4-2 Air/Contact Discharge tests.

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This test is intended to simulate the human body's potential to store electrostatic energy and discharge it to an integrated circuit upon close proximity or contact. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

EN61000-4-2 is used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. EN61000-4-2 specifies that the system is required to withstand an amount of static electricity when ESD is applied to exposed metal points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins.

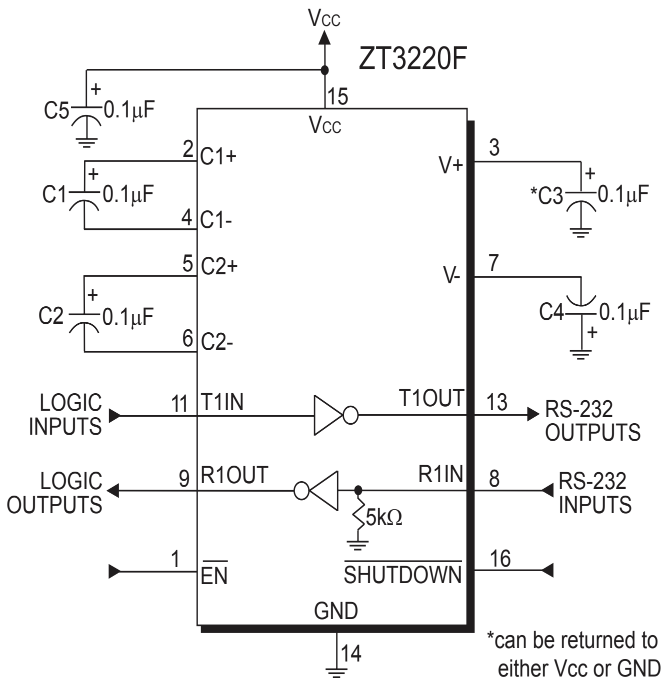
There are two methods within EN61000-4-2, the Air Discharge method and the Contact Discharge method. With the Air Discharge Method, an ESD voltage is applied to the equipment under test through air, which simulates an electrically charged person ready to connect a cable onto the rear of the system and the high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc inconsistencies.

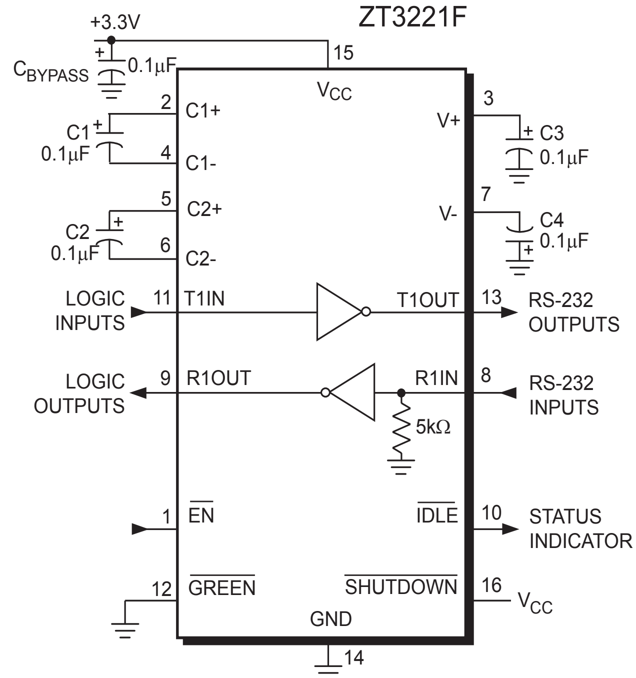
Zywyn's RS232 transceivers meets and exceeds the minimum criteria for EN61000-4-2 with ±15kV for Air Gap Discharge and ±8kV for Contact Discharge.

Operation Status	$\overline{\text{GREEN}}$	$\overline{\text{SHUTDOWN}}$	$\overline{\text{EN}}$	Signal at R_XIN	$\overline{\text{IDLE}}$	T_XOUT	R_XOUT
Shutdown	don’t care	0	0	present	1	tri-state	active
	don’t care	0	0	not present	0	tri-state	active
	don’t’ care	0	1	present	1	tri-state	tri-state
	don’t’ care	0	1	not present	0	tri-state	tri-state
Normal without $\overline{\text{GREEN}}$	1	1	0	present	1	active	active
	1	1	0	not present	0	active	active
	1	1	1	present	1	active	tri-state
	1	1	1	not present	0	active	tri-state
Normal with $\overline{\text{GREEN}}$	0	1	0	present	1	active	active
	0	1	0	not present	0	tri-state	tri-state
	0	1	1	present	1	active	tri-state
	0	1	1	not present	0	tri-state	tri-state

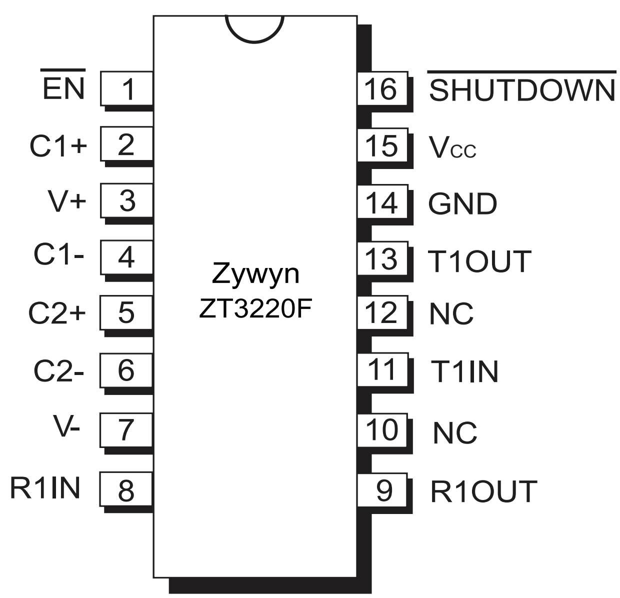
Table 1. ZT32xxF Truth Table

Typical Application Circuits

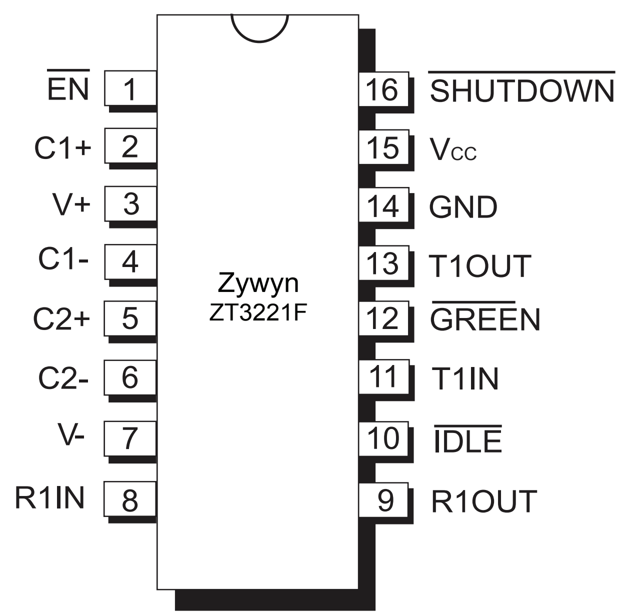




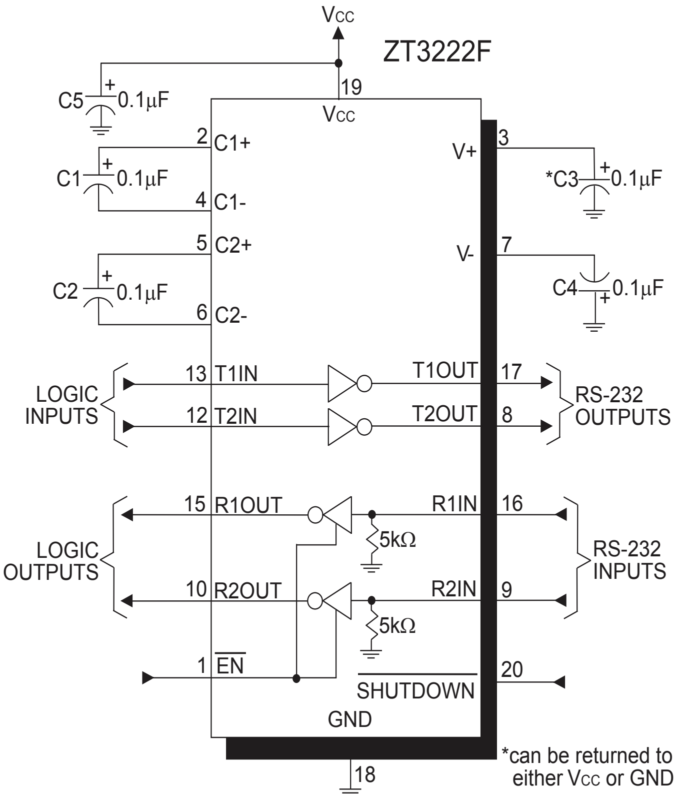
16-pin SSOP/TSSOP/WSOIC



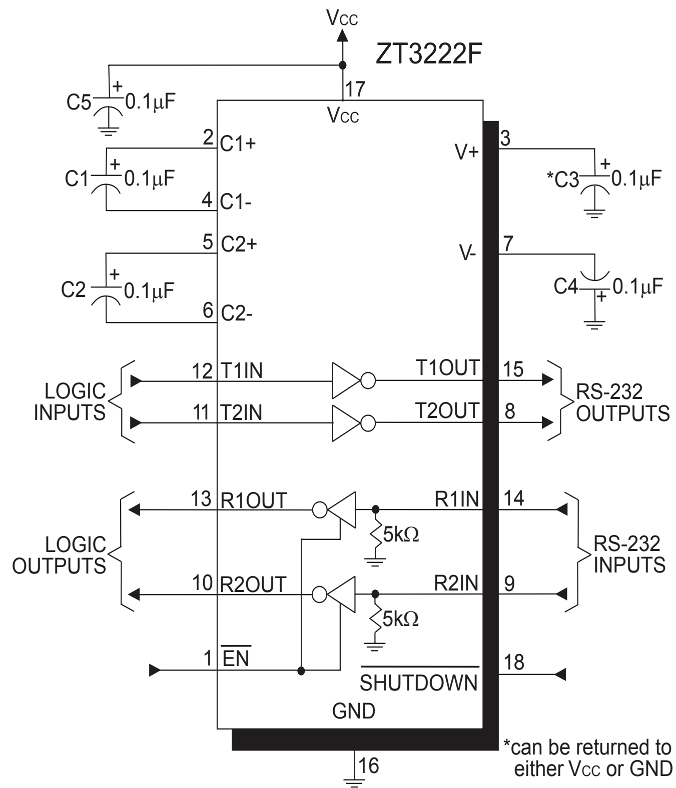
16-pin SSOP/TSSOP



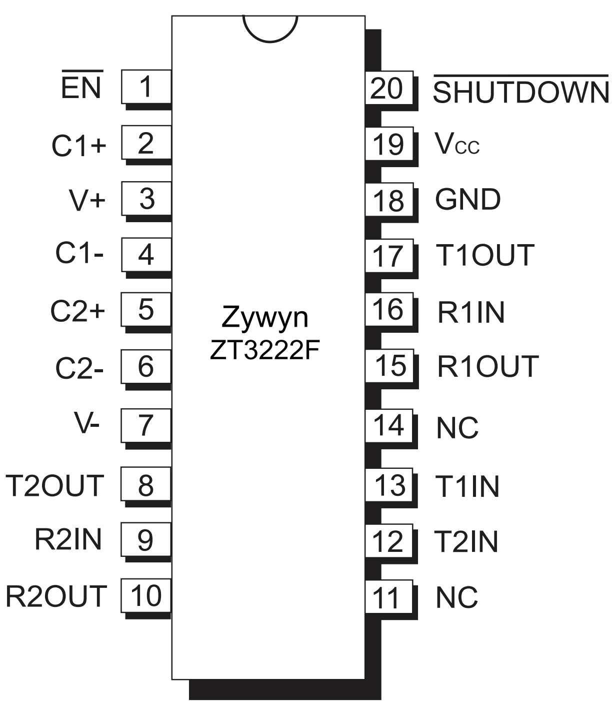
Typical Application Circuits

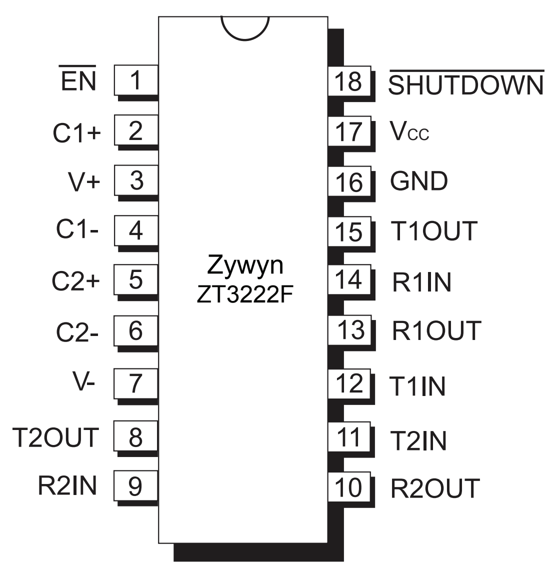


20-Pin SSOP/TSSOP

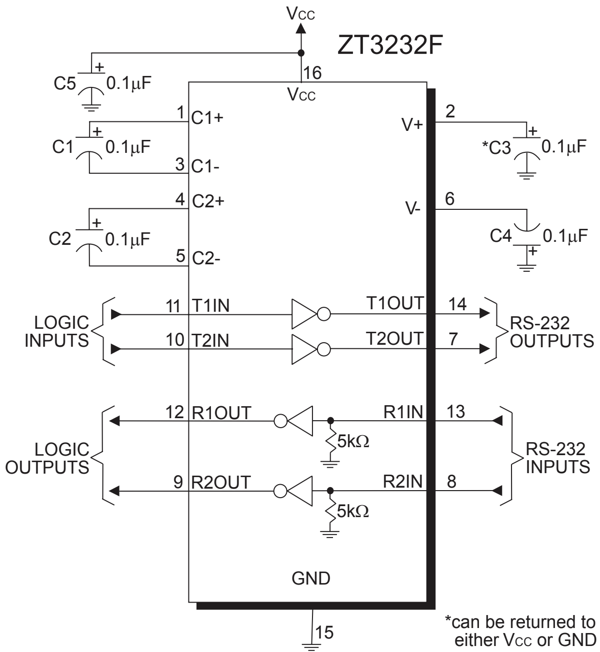


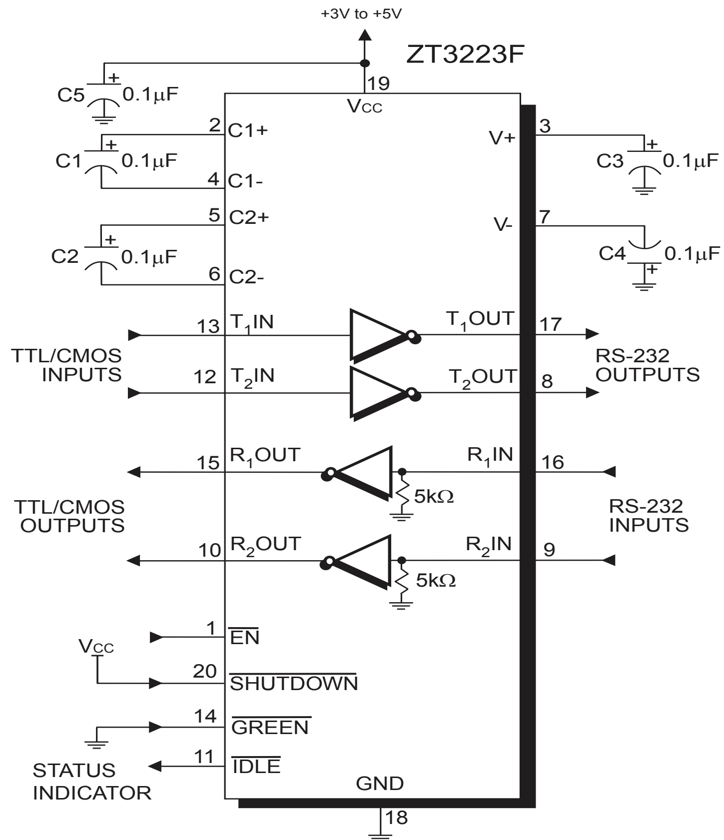
18-Pin PDIP/WSOIC



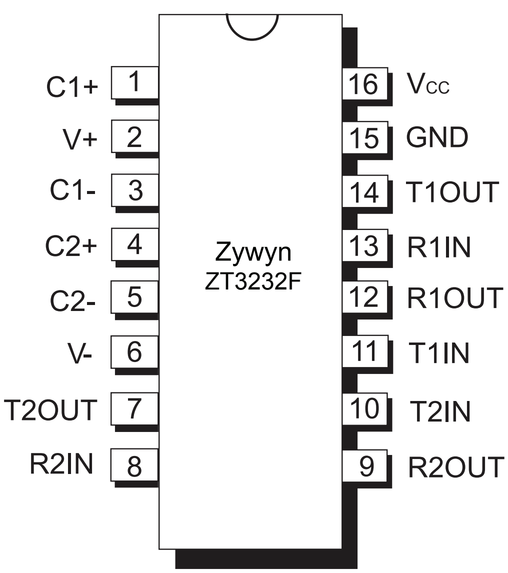


Typical Application Circuits

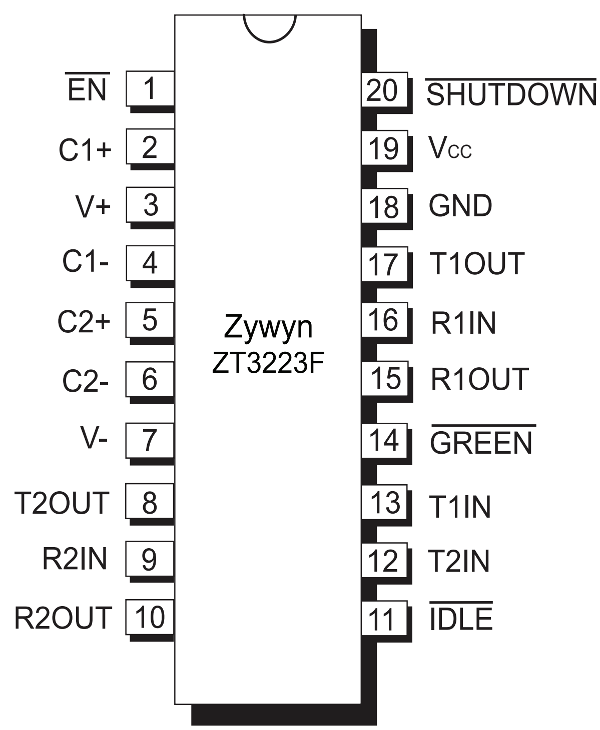




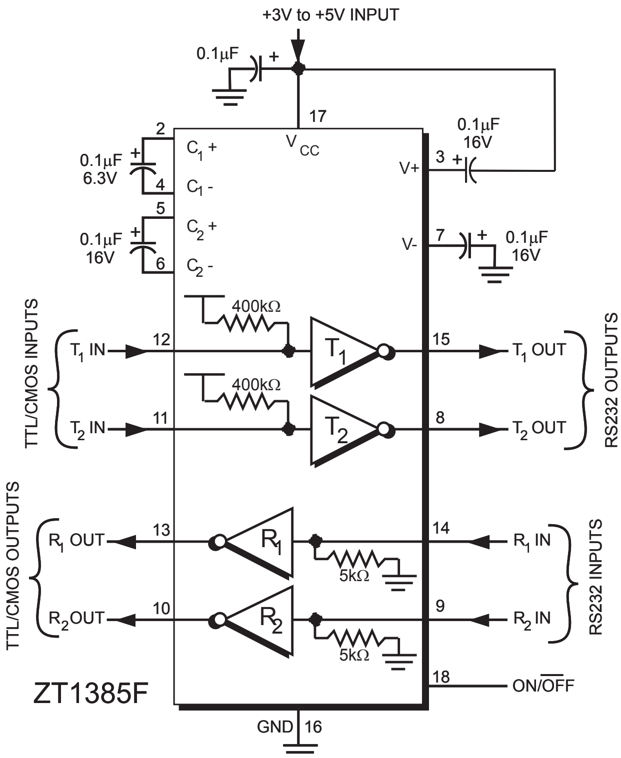
16-Pin PDIP/SSOP/SOIC/TSSOP/WSOIC



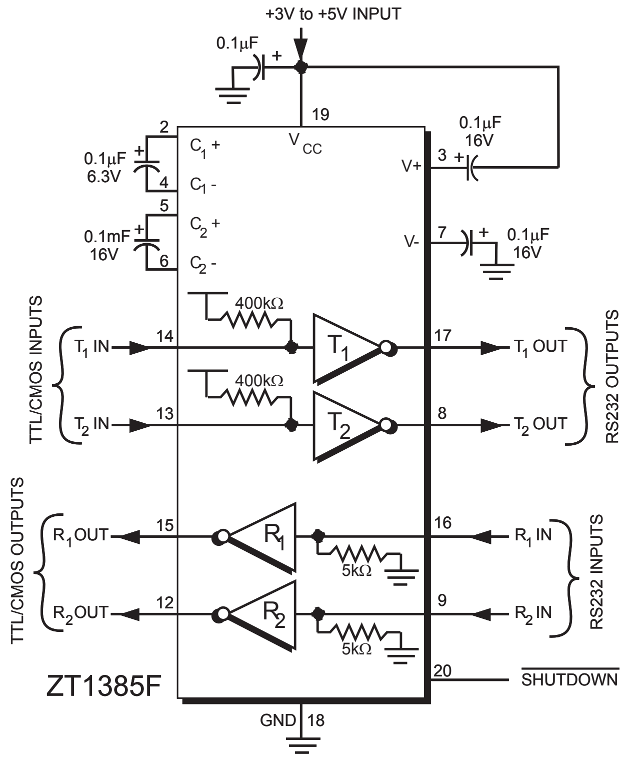
20-Pin PDIP/SSOP/TSSOP



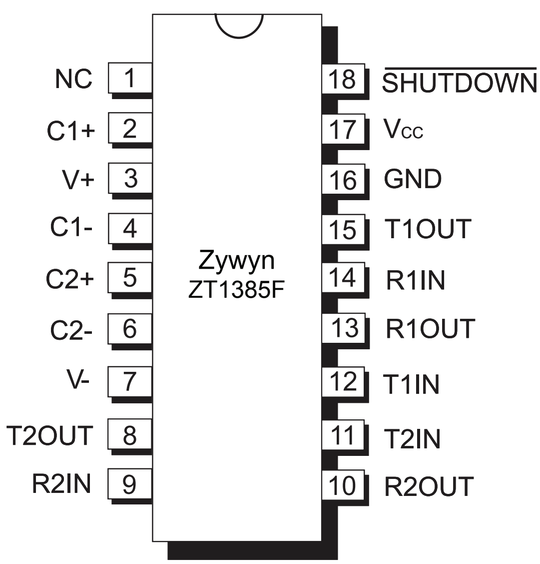
Typical Application Circuits

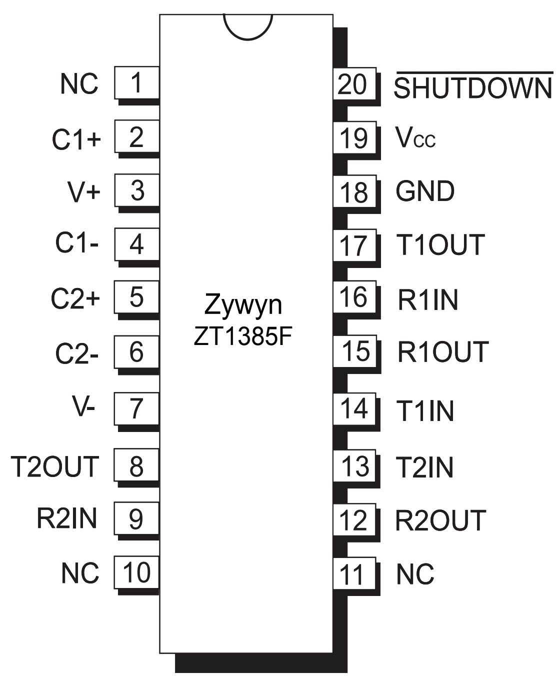


18-pin WSOIC

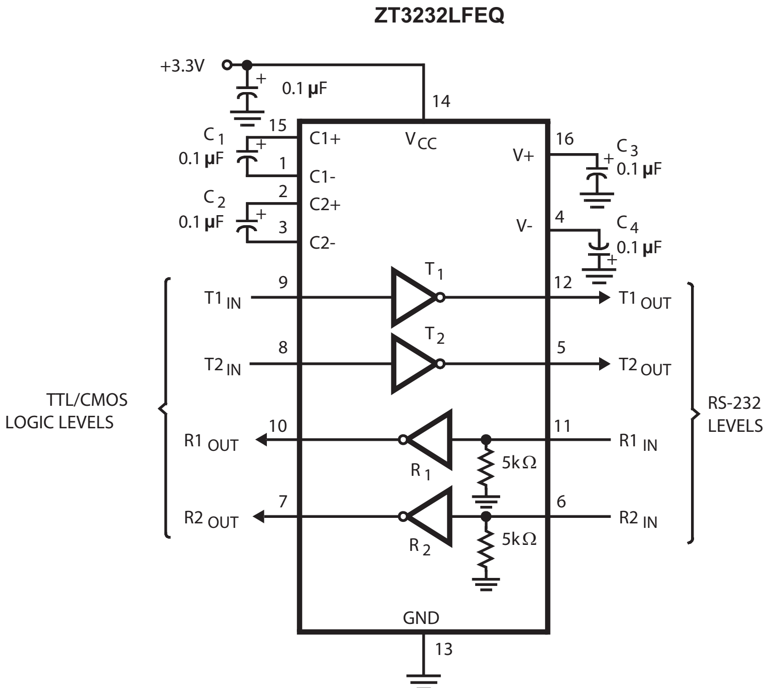


20-pin SSOP

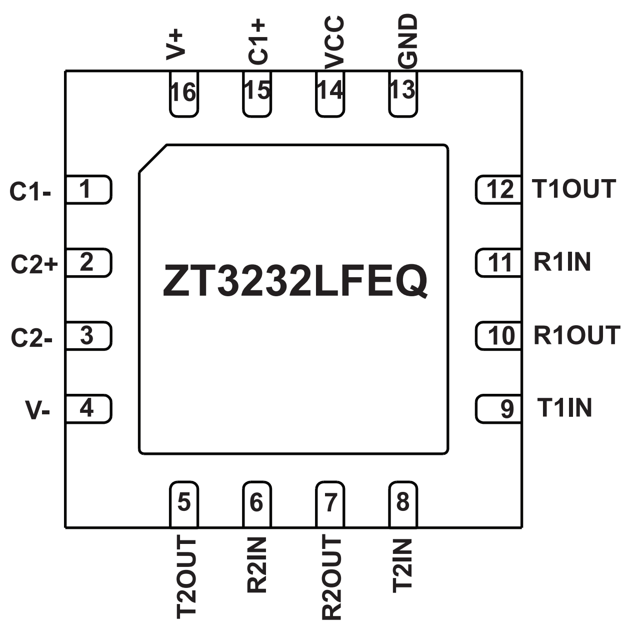




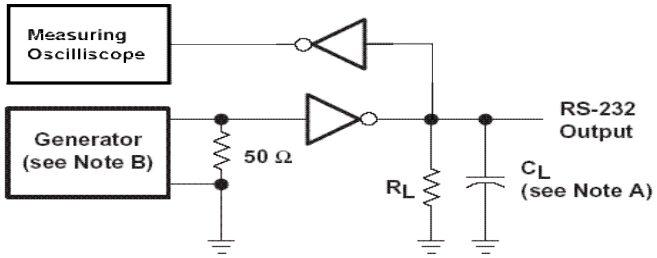
Typical Application Circuits



16-pin QFN



Typical Test Circuits



TEST CIRCUIT

Maximum Data Rate Test Circuit

Notes:

A. R_L = 3kΩ , C_L = 250pF, T_A = 25°C,

One Driver Switching.

B. The pulse generator had the following characteristics:

PRR = 1000 kbps, Zo = 50Ω, 50% duty cycle,

T_r & $T_f \leq$ 10ns.

C. $\overline{\text{SHUTDOWN}}$ = V_{CC} when applicable.

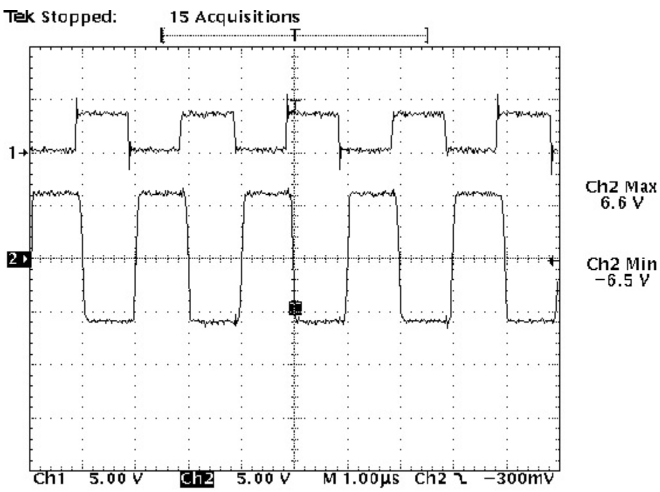


Figure 1. ZT32xxF TxIN to TxOut (no load) at 1Mbps waveform

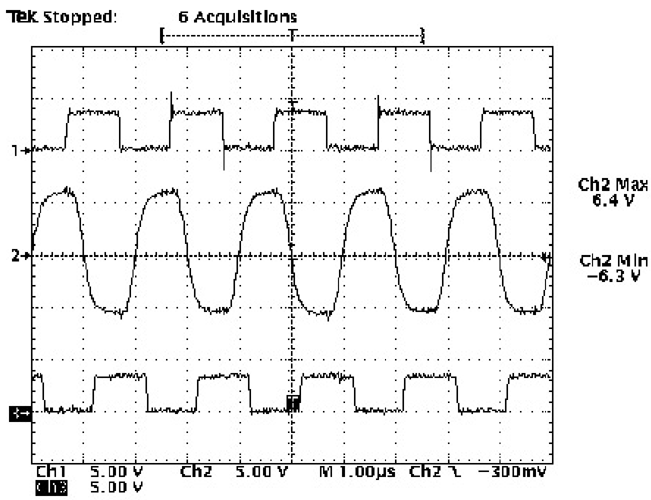


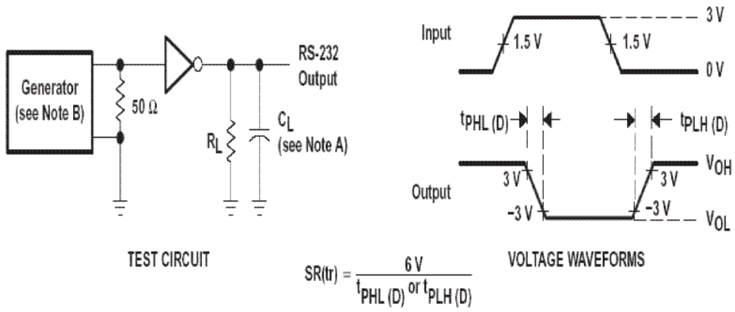
Figure 2. ZT32xxF TxIN to TxOut to RxOut (loopback to Rx with 250pF load) at 1Mbps waveform

RS232 Signal Characteristics

Figure 1 shows the normal RS232 transceiver function with a TTL/CMOS signal applied to the input on channel 1 and the resultant RS232 output shown on channel 2. This figure shows a typical RS232 line driver output without loading. In other words, this is the open circuit RS232 output voltage. The charge pump voltage converter efficiently converts the necessary voltage for the driver's output transistors so that the RS232 output is close to the ideal rail voltage of 6.6V.

Figure 2 shows the RS232 transceiver function using the TTL/CMOS input on channel 1 while showing the RS232 output on channel 2. This figure shows the RS232 signal while the output is loaded with 3kohms and 250pF. The resistive load is the receiver's input impedance as the driver's output is looped back to the receiver's input. The resultant output on channel 3 is the receiver's TTL/CMOS output. While loaded with a typical RS232 load, the driver's output level only drops 0.2V from its open circuit voltage while running at 1Mbps. The RS-232 output on channel 2 also shows good signal integrity while at the high data rates, which allows the receiver to process the signal will minimum skew and delay. Zywyn's low-drop driver circuitry working with its efficient voltage regulator allows superior line driving capability with the bonus of ±15kV ESD immunity.

Typical Test Circuits



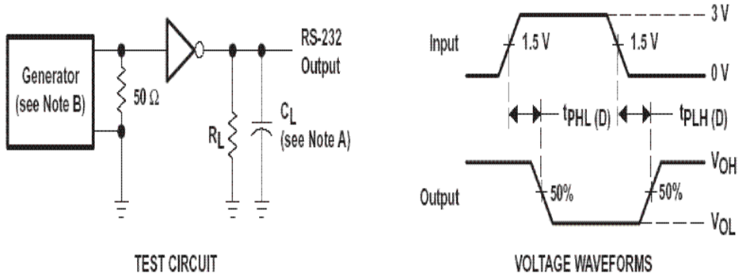
Driver Transition-Region Slew Rate Test Circuit

Notes:

A. R_L = 3k~7kΩ , C_L = 150pF to 250pF,
One Driver Switching, T_A = 25°C,
Measured from +3V to -3V or -3V to +3V.

B. The pulse generator had the following characteristics:
PRR = 1000 kbps, Zo = 50Ω, 50% duty cycle,
T_r & $T_f \leq$ 10ns.

C. $\overline{\text{SHUTDOWN}}$ = V_{CC} when applicable.



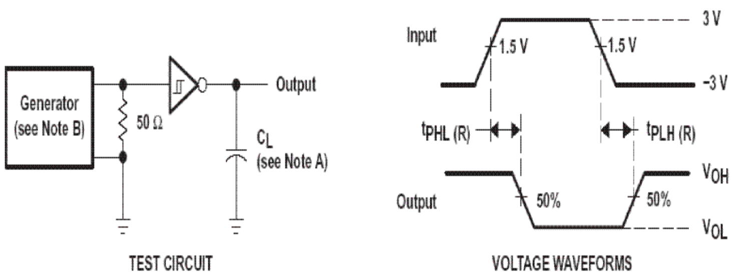
Driver Propagation (t_{PHL} & t_{PLH}) Test Circuit

Notes:

A. All drivers loaded with R_L = 3kΩ , C_L = 1000pF.

B. The pulse generator had the following characteristics:
PRR = 1000 kbps, Zo = 50Ω, 50% duty cycle,
T_r & $T_f \leq$ 10ns.

C. $\overline{\text{SHUTDOWN}}$ = V_{CC} when applicable.



Receiver Propagation Delay Times Test Circuit

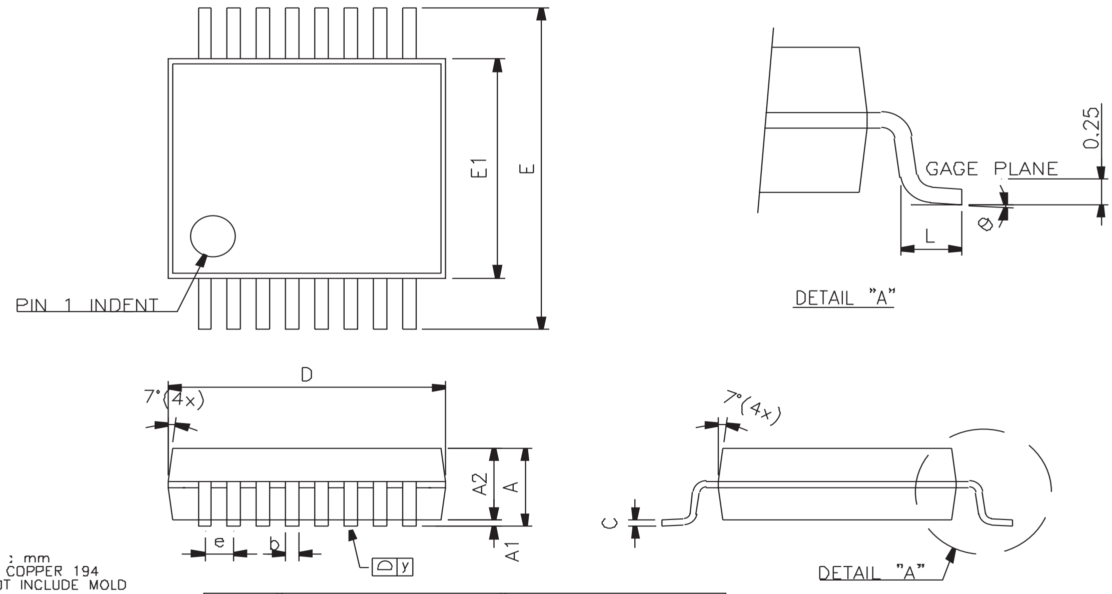
Notes:

A. C_L = 150pF, including probe and jig capacitance.

B. The pulse generator had the following characteristics:
PRR = 1000 kbps, Zo = 50Ω, 50% duty cycle,
T_r & $T_f \leq$ 10ns.

C. $\overline{\text{SHUTDOWN}}$ = V_{CC} when applicable.

Package Information



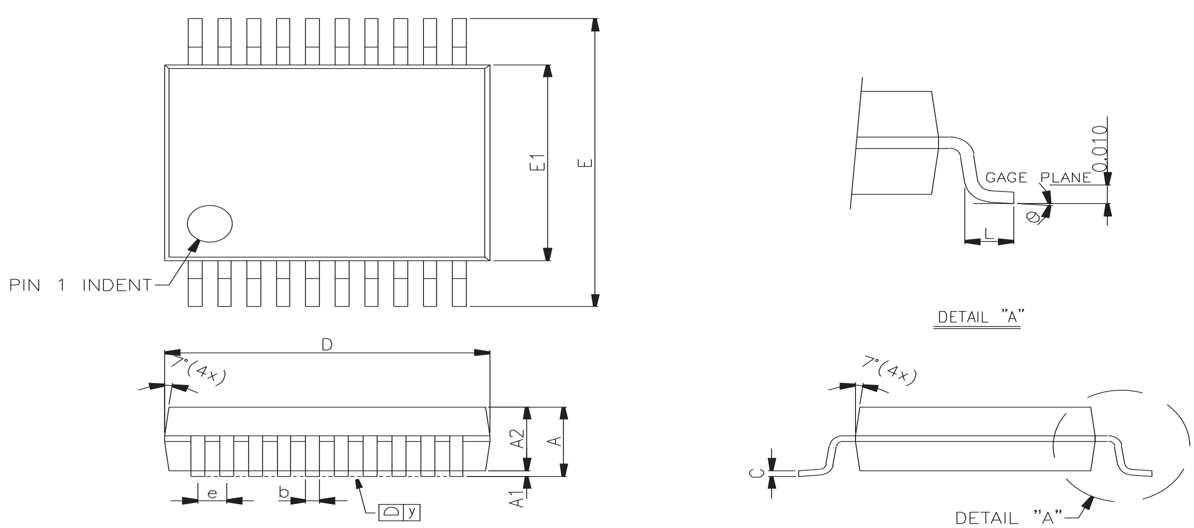
NOTE :

1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MO-150AC

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	2.00	—	—	0.079
A1	0.05	—	0.15	0.002	—	0.006
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	0.30	0.38	0.0086	0.012	0.015
C	0.09	0.15	0.25	0.0035	0.006	0.0098
D	5.90	6.20	6.50	0.232	0.244	0.256
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.022	0.030	0.037
θ	0°	4°	8°	0°	4°	8°
y	—	—	0.10	—	—	0.004

16-pin SSOP

CUSTOMER :		ZYWYN CORPORATION		
APPROVED BY	DATE	TITLE: 16L SSOP PACKAGE OUTLINE DRAWING (BODY SIZE: 5.3mm)		
DRAW BY: Jasmin Liu	01/25/'02			
CHECK BY: Edward Yang	01/25/'02			
APPROVAL: Jack Tu	01/25/'02	DWG. NO. PO-SSOP-016		REV. 0
APPROVAL: Jack Tu	01/25/'02	UNIT : mm	SCALE : 12/1	SHEET 1 OF 1



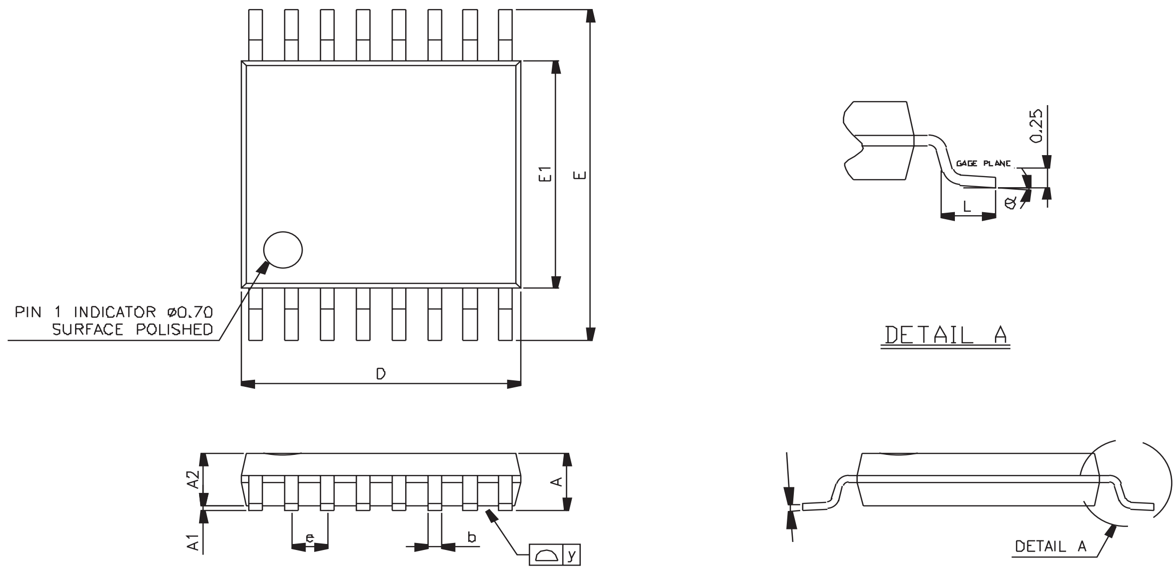
NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MO-150

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	—	1.75	—	—	0.069	—
b	0.22	0.30	0.38	0.0086	0.012	0.015
C	0.13	0.15	0.20	0.0051	0.006	0.0079
D	7.08	7.20	7.34	0.279	0.284	0.289
E	7.40	7.80	8.20	0.291	0.307	0.323
E1	5.00	5.30	5.60	0.197	0.209	0.220
e	—	0.65	—	—	0.0256	—
L	0.56	0.75	0.97	0.022	0.030	0.037
θ	—	4°	8°	—	4°	8°
y	—	—	0.076	—	—	0.003

20-pin SSOP

CUSTOMER :		ZYWYN CORPORATION		
APPROVED BY	DATE	TITLE: 20L MEDIUM FINE PITCH STANDARD SMALL OUTLINE PACKAGE DRAWING		
DRAW BY: Monica Chen	09/29/'99			
CHECK BY: Leo Chen	12/01/'99			
APPROVAL: Paul Lee	12/01/'99	DWG. NO. PO-SSOP-010		REV. 0
APPROVAL: Jack Tu	12/01/'99	UNIT : INCH	SCALE : 12/1	SHEET 1 OF 1



NOTE :

1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : OLIN C7025/EFTEC 64T
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE ; ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	1.10	1.20	0.041	0.043	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	——	1.00	1.05	——	0.039	0.041
b	0.20	0.25	0.28	0.008	0.010	0.011
C	——	0.127	——	——	0.005	——
D	4.90	5.075	5.10	0.193	0.1998	0.200⚠
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.170	0.173	0.177
e	——	0.65	——	——	0.026	——
L	0.50	0.60	0.70	0.020	0.024	0.028
y	——	——	0.076	——	——	0.003
θ	0°	4°	8°	0°	4°	8°

16-pin TSSOP

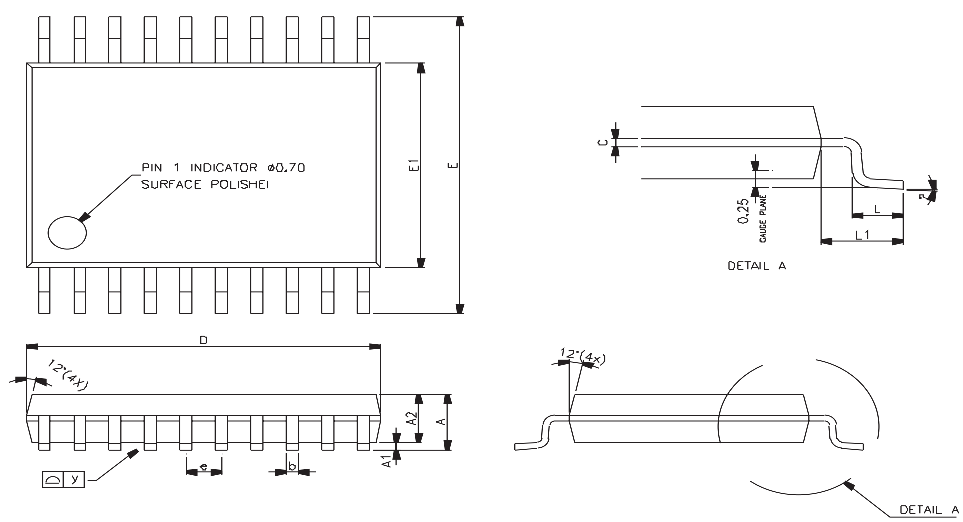
CUSTOMER ; ZYWYN CORPORATION

APPROVED BY	DATE
DRAW BY: Monica Chen	06/01/'00
CHECK BY: Leo Chen	06/17/'00
APPROVAL: Paul Lau	06/17/'00
APPROVAL: Jack Tu	06/18/'00

TITLE: 16L TSSOP PACKAGE OUTLINE DRAWING

DWG. NO. PO-TSSOP-002 REV. 1

UNIT : mm SCALE : 15/1 SHEET 1 OF 1



NOTE :

1. CONTROLLING DIMENSION : mm
2. LEAD FRAME MATERIAL : OLIN C7025/EFTEC 64T
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE. ⚠2
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE ; ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	——	——	1.20	——	——	0.047
A1	0.05	——	0.15	0.002	——	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	——	0.30	0.007	——	0.012
C	0.09	——	0.20	0.0035	——	0.008
D	6.40	6.50	6.60	0.252	0.256	0.260
E	——	6.40	——	——	0.252	——
E1	4.30	4.40	4.50	0.170	0.173	0.177
e	——	0.65	——	——	0.026	——
L	0.45	0.60	0.75	0.0177	0.024	0.0295
L1	——	1.00	——	——	0.039	——
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

20-pin TSSOP

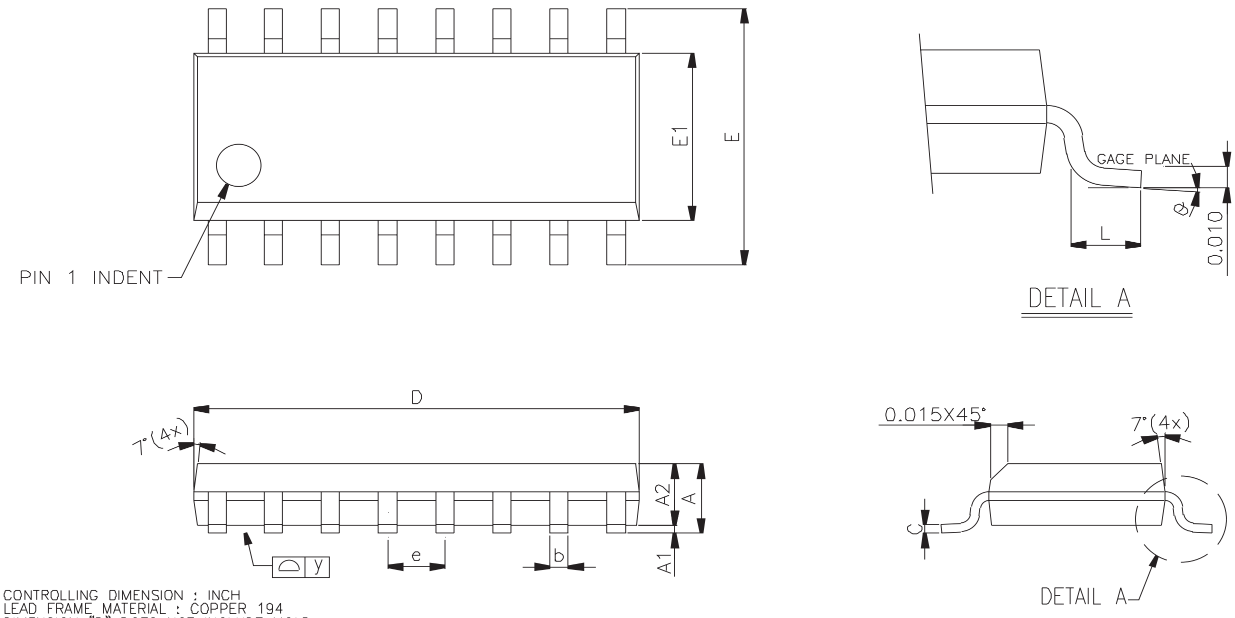
CUSTOMER : ZYWYN CORPORATION

APPROVED BY	DATE
DRAW BY: Rex Wang	09/11/'02
CHECK BY: SanWin Lin	09/12/'02
APPROVAL: Parker Chen	09/13/'02
APPROVAL: Andy Yang	09/13/'02

TITLE: 20L TSSOP PACKAGE OUTLINE DRAWING (4.4mm)

DWG. NO. PO-TSSOP-008 REV. 2

UNIT : mm SCALE : 15/1 SHEET 1 OF 1



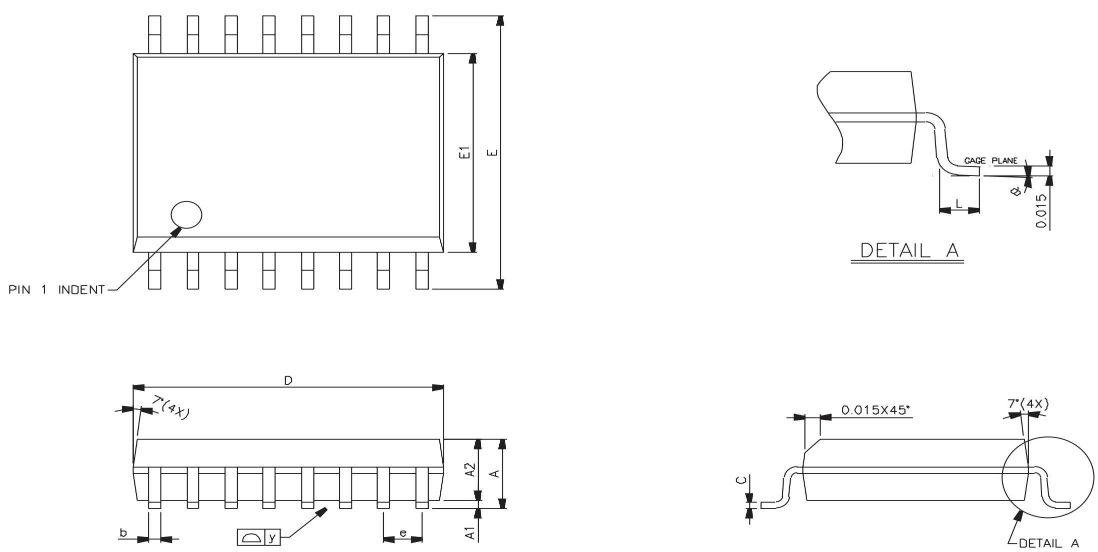
NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-012

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

16-pin nSOIC

CUSTOMER :		ZYWYN CORPORATION		
APPROVED BY	DATE	TITLE: 16L SMALL OUTLINE PACKAGE DRAWING(0.150")		
DRAW BY: Monica Chen	11/09/99			
CHECK BY: Leo Chen	11/10/99			
APPROVAL: Paul Leu	11/10/99	DWG. NO. PO-SOP-003		REV. 0
APPROVAL: Jack Ju	11/11/99	UNIT : INCH	SCALE : 12/1	SHEET 1 OF 1



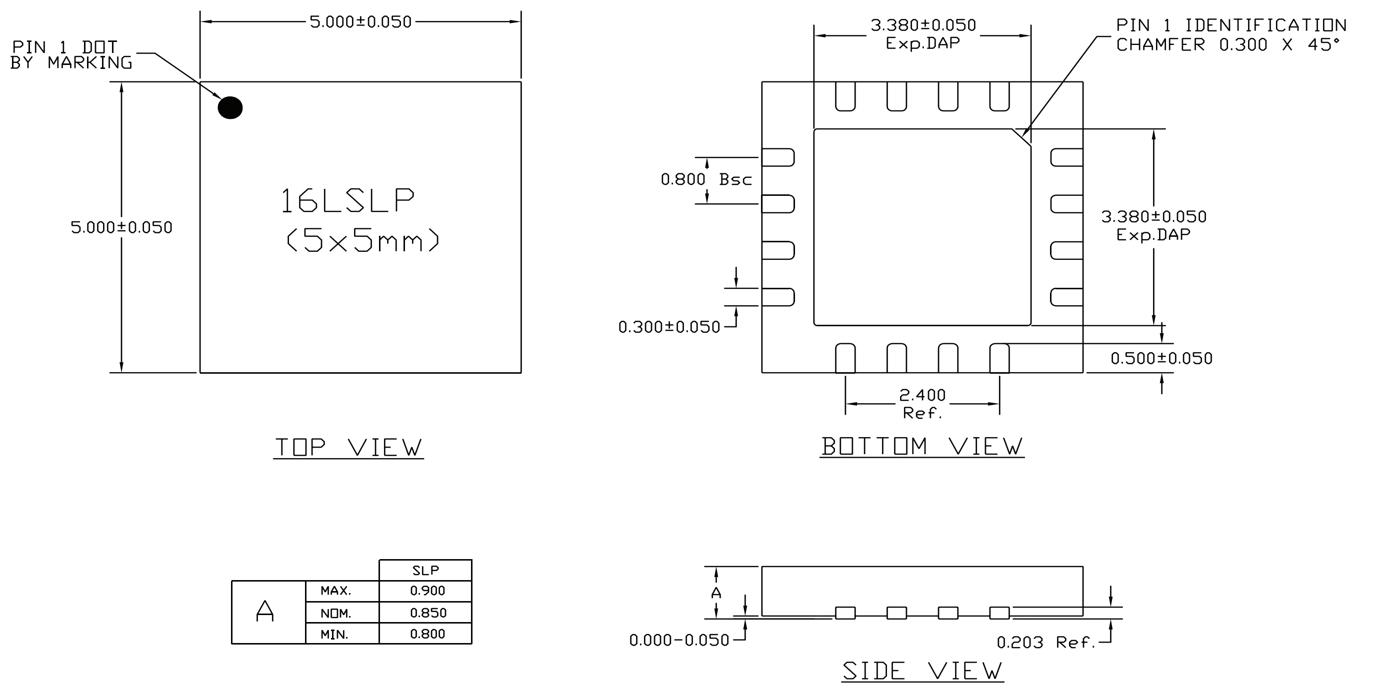
NOTE :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194
3. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm] TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5. TOLERANCE : ±0.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6. OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7. REFERENCE DOCUMENT : JEDEC SPEC MS-013

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	——	0.30	0.004	——	0.012
A2	——	2.31	——	——	0.091	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	10.08	10.31	10.49	0.397	0.406	0.413
E	10.01	10.31	10.64	0.394	0.406	0.419
E1	7.39	7.49	7.59	0.291	0.295	0.299
e	——	1.27	——	——	0.050	——
L	0.38	0.81	1.27	0.015	0.032	0.050
y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

16-pin wSOIC

CUSTOMER :		ZYWYN CORPORATION		
APPROVED BY	DATE	TITLE: 16L WIDE BODY SMALL OUTLINE PACKAGE DRAWING		
DRAW BY: Monica Chen	10/28/99			
CHECK BY: Leo Chen	11/01/99			
APPROVAL: Paul Leu	11/02/99	DWG. NO. PO-SOP-004		REV. 0
APPROVAL: Jack Ju	11/02/99	UNIT : INCH	SCALE : 8/1	SHEET 1 OF 1



		SLP
A	MAX.	0.900
	NOM.	0.850
	MIN.	0.800

REV.	DESCRIPTION	DATE	BY	APPD

TOLERANCES
REFER TO SPECIFICATION ABOVE

UNIT: MM | SCALE: NTS | SYMBOL

DESIGNED: BEN ONG	DATE:
APPD: ANDREW TAN	DATE:
APPD: CW CHAI	DATE:
APPD: GC TAN	DATE:
APPD: YC CHOO	DATE:
DWG. NO: PO-16(SLP)5x5-3.38x3.38	REV.: 00

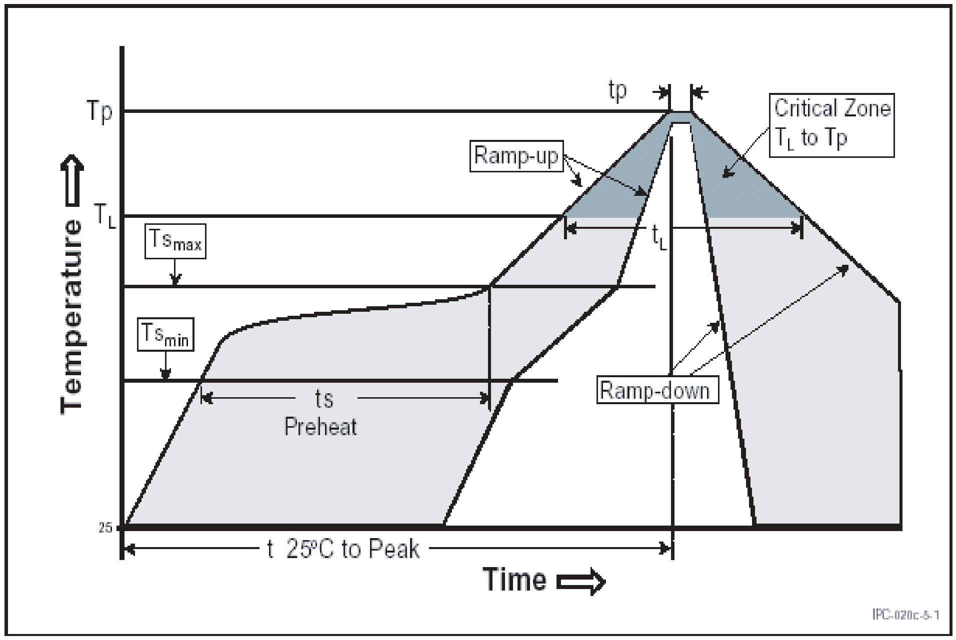
ZYWYN CORPORATION

16L (SLP) 5x5 mm
(PACKAGE OUTLINE)

SHEET NO : 1 OF 1.

Green Package SMD IR Reflow Profile Information

IR Reflow Profile Conditions



Profile Feature	JESD Sn-Pb Eutectic Assembly	JESD Pb-free Assembly
Average Ramp-Up Rate (T_{Smax} to T_P)	3°C/seconds max.	3°C/seconds max.
Pre-heat - Temperature Min (T_{Smin}) - Temperature Max (T_{Smax}) - Time (T_{Smin} to t_{Smax})	100°C 150°C 60~120 seconds	150°C 200°C 60~180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60~150 seconds	217°C 60~150 seconds
Peak/Classification Temperature (T_P)	235°C+5/-0°C	255°C+5/-0°C
Time within 5°C of actual Peak Temperature (t_P)	10~30 seconds	20~40 seconds
Ramp-Down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

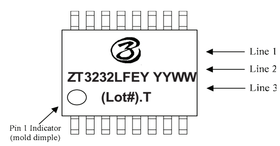
Zywyn Green Packages are Pb-free and RoHS compliance.

Ordering Information

Part Number	Temperature Range	Package Type
ZT3220LFEA	-40°C to +85°C	16-pin SSOP
ZT3220LFET	-40°C to +85°C	16-pin WSOIC
ZT3220LFEY	-40°C to +85°C	16-pin TSSOP
ZT3221LFEA	-40°C to +85°C	16-pin SSOP
ZT3221LFEY	-40°C to +85°C	16-pin TSSOP
ZT3222LFEA	-40°C to +85°C	20-pin SSOP
ZT3222LFET	-40°C to +85°C	18-pin WSOIC
ZT3222LFEY	-40°C to +85°C	20-pin TSSOP
ZT3223LFEA	-40°C to +85°C	20-pin SSOP
ZT3223LFEY	-40°C to +85°C	20-pin TSSOP
ZT3232LFEA	-40°C to +85°C	16-pin SSOP
ZT3232LFEN	-40°C to +85°C	16-pin nSOIC
ZT3232LFET	-40°C to +85°C	16-pin WSOIC
ZT3232LFEY	-40°C to +85°C	16-pin TSSOP
ZT3232LFEQ	-40°C to +85°C	16-pin QFN
ZT1385LFEA	-40°C to +85°C	20-pin SSOP
ZT1385LFET	-40°C to +85°C	18-pin WSOIC

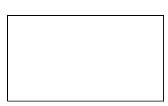
Please contact the factory for pricing and availabiliy on Tape-and-Reel options.

TOPSIDE MARK INSTRUCTIONS:



Line 1: Zywyn (logo)
Line 2: Zywyn Part Number "ZT3232LFEY", Space " ", Date Code (Prod Year & Week)
Line 3: Lot #, dot and Country ".T"
Note: Pin # 1 " △" Indicator Required if no mold dimple

BOTTOMSIDE MARK INSTRUCTIONS:



No backside marking

Zywyn Corporation
Headquarters and Sales Office
1270 Oakmead Parkway, Suite 201 • Sunnyvale, CA 94085 • Tel: (408) 733-3225 • Fax: (408) 733-3206
Email: sales@zywyn.com • www.zywyn.com