

國立臺灣科技大學
電機工程系

博士學位論文

學號: D10007202

應用於升壓電力轉換之新型台科大多倍壓電路

A Novel Taiwan Tech Voltage Multiplier for Step-Up
Power Conversion Applications



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中華民國 一百零四年 八月三十一日



博士學位論文指導教授推薦書



D10007202

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104 年 07 月 07 日



博士學位考試委員審定書



D10007202

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中華民國 104 年 07 月 07 日

中文摘要

藉由合併兩個傳統的 Cockcroft-Walton 半波多倍壓整流電路，本論文提出一個新型之台科大多倍壓整流電路。結合傳統雙電感電流饋入式轉換器，得以使用較低應力的半導體元件及較低的變壓器匝數比，實現所需的電壓增益。此外，電路更因具有輸出電壓漣波抵消機制，可以使用較小容值之聚丙烯(PP)電容取代大容值的電解電容，達成電壓漣波規格，進而提高整體轉換器的可靠度。

對高輸出電壓應用之輸出電壓漣波與輸出電壓降規格的性能，所提出之電路有顯度的降低，可以使用更多級的倍壓模組與更低應力的元件，滿足規格之輸出電壓。上列之特性顯示，本論文提出之多倍壓整流電路適合在如再生能源發電系統需求或是高電壓應用的醫療設備之高頻、高效率、高輸出電壓及高可靠度的電力轉換應用。



本論文以雙電桿電流饋入式架構為一次側電路，搭配所提出之台科大倍壓整流電路與台科大多倍壓整流電路，分別在第二章及第三章進行理論分析與相關公式的推導，並且以輸入電壓 24-36V 輸出 380V/380W 之規格設計，分別完成實作電路。進而以相同規格實驗之傳統 Cockcroft-Walton 六倍壓電路及對稱式六倍壓電路，比較其電路特性。

關鍵字：電流饋入式轉換器、高電壓增益轉換率、台科大倍壓整流電路、台科大多倍壓整流電路。

Abstract

By combining two Cockcroft-Walton half-wave voltage multiplier rectifiers, a novel Taiwan Tech voltage multiplier rectifier is proposed in this dissertation. Applying it to a widely used dual-inductor current-fed converters, low voltage rating devices with low turns-ratio transformer can be used to achieve the required high voltage gain. Moreover, output voltage ripple is significantly reduced due to its built-in output voltage ripple cancellation mechanism. Consequently, small capacitance film capacitors can be used instead of high voltage-rating electrolytic capacitors. Thus, the reliability of the power converter can be enhanced.

Furthermore, the proposed has significantly reduction in two key issues, voltage drop and voltage ripple, for high output voltage applications. Thus, more stages voltage multiplier with lower voltage-rating components can be applied to meet the same output voltage specification. These features make the proposed voltage multiplier rectifier desirable for high frequency, high efficiency, high output-voltage, and high reliability power applications, such as the sustainable energy source power system or some high voltage medical instrument power conversion applications.

In addition to operation principle, theoretical analysis, and design considerations, a dual-inductor current-fed converter with Taiwan Tech voltage doubler rectifier and a dual-inductor current-fed boost converter with six-fold Taiwan Tech voltage multiplier rectifier as examples are described in Chapter 2 and Chapter 3, respectively. Three six-fold dual-inductor current-fed converters with a Cockcroft-Walton voltage multiplier rectifier, with a symmetrical Cockcroft-Walton voltage multiplier rectifier,

and with a Taiwan Tech voltage multiplier rectifier, have been implemented with same 100 kHz, 24~36V input, 380V/380W output specifications. Also the performance comparisons among these circuits are made.

Keywords: current-fed boost converter, high voltage gain, Taiwan Tech voltage doubler rectifier, Taiwan Tech voltage multiplier rectifier.



Acknowledgement

With sincere appreciation in my heart, I would like to thank my advisor, Dr. Ching-Shan Leu for his guidance, encouragement and support throughout my graduate studies. It was an invaluable learning experience to be one of his students. From him I have learned not only in the knowledge of the power electronics, but also the ability of independent research and the attitude toward research. It is going to benefit me for the rest of my life.

I would like to thank all my oral defense committee members, Prof. Huang-Jen Chiu, Prof. Chung-Ming Young, Prof. Ray-Lee Lin, Prof. Jiann-Fuh Chen, Prof. Yaow-Ming Chen, Prof. Tsai-Fu Wu, Dr. Yu-Kang Lo, and Dr. C. Y. Lin for their valuable suggestions and comments. Their kind supports and guidance have been of great value in this study.

Also, I would like to thank all the members of the Power Conversion Lab (PCL), Mr. Ming-Hui Li, Mr. Sin-Jhu Chen, Mr. Shun-Yuan Wu, Mr. Shih-Che Lan, Mr. Sheng-Min Chiu, Mr. Shiang-Kai Huang, Mr. Soung-Poul Yeh, Mr. Ren-Ming Hsu, Mr. Wen-Cheng Hsu, Mr. Wei-Teng Lin, Mr. Chia-Wei Lee, Mr. Cheng-Kai Huang, Mr. Chih-Chung Chen, Mr. En-Fu Foeng, Mr. Cheng-Chia Liu, Mr. Hsin-Yu Huang, Mr. Kai-Shiang Syu, Mr. Quang Trong Nha, Mr. Jyun-Yi Yan, Mr. Yi-Hsiang Huang, Mr. Li-Tang Wu, Mr. Wei-Liang Kung, Mr. Chang-Chieh Lo Mr. Chang-Hang Hsieh, Mr. Joseph Yang, and Mr. Yu-Yao Peng, and Mr. Ting-Yu Chou. I want to thank them for

all their help, stimulating suggestions, and encouragement. They helped me in all the time of research for and writing of this dissertation.

Moreover, I would like to thank my best friends who have helped me a lot during my study process. Mr. Matt Su, Miss. I-Nung Chiu, Miss. Yian Chen, Mr. Kuan-Hung Lo, Mr. Wei Zhang, Mr. Chia-His Chang, and Miss. Yi-Ying Chiang. Without their encouragement, I wouldn't get through all the pain and darkness.

There are some people who have made a difference in my life. You may never realize how much your existence means to me. I can't list all your names but you know who you are.

Most of all, my heartfelt appreciation goes toward my dear family, Chiu-Kuei Huang, Mei-Lin Yang, Pin-Chen Huang and Xin-Yi Yang, with their unconditional love, support, understanding and encouragement for all of my endeavors.



To my family



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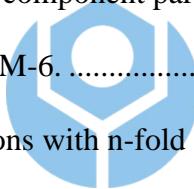
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Chapter 1 Introduction

1.1 Background and motivation

A step-up power conversion technique is demanding more and more in recent years for many industry applications such as uninterrupted power supplies (UPS), distributed photovoltaic power generation systems (PV), and fuel cell energy conversion systems [1]-[3]. To reach high voltage gain, a conventional boost converter is widely used for non-isolated applications. In practice, however, it suffers from high voltage stress on the main switch. Thus, a high-voltage rating switch has to be used and its high on-resistance, $R_{DS(on)}$, results in higher conduction losses. Moreover, serious reverse recovery problems are thus generated on the power device under extremely high duty cycle and the voltage gain declines due to its circuit parasitic components as shown in Fig. 1-1 [4]. Consequently, the conventional boost converter would not be acceptable for realizing high step-up voltage gain ($V_O \geq 5 \cdot V_{in}$) along with high efficiency.

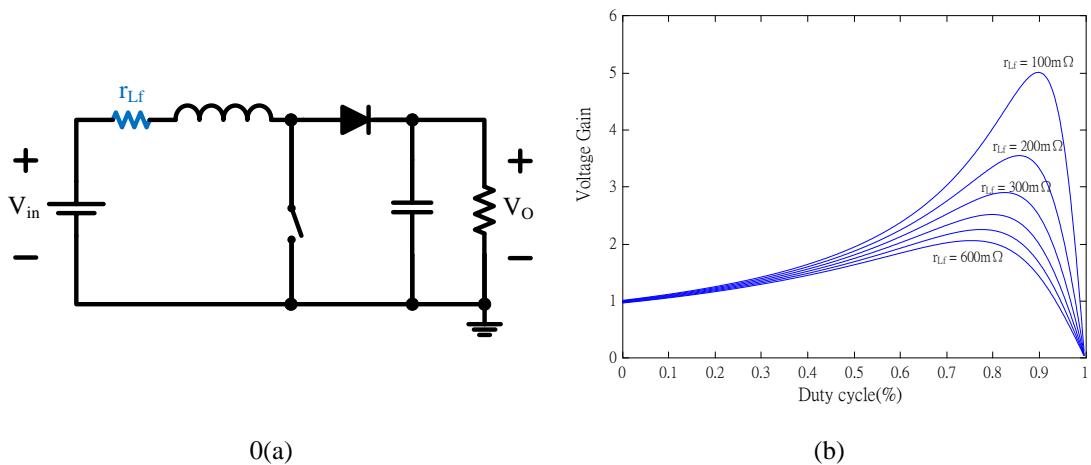


Fig. 1-1. (a) Circuit diagram of boost converter and (b) voltage gain with r_{Lf} as a running parameter.

One of the approaches to obtain high voltage gain has been proposed by cascading either conventional boost converters or employing a modified cascaded boost [5]-[7]. However, there is a significant drawback of the cascading configuration that high voltage stress on switches and passive components. Consequently, it is not possible to employ lower voltage-rating switches resulting in poor efficiency.

To surpass such limitations, a transformer or a coupled inductor is employed to achieve high voltage gain. Without requiring high values of duty cycle or multiple cascaded stages, voltage gain can be obtained by introducing the turns-ratio of the transformer. In addition to provide galvanic isolation, the voltage rating of active semiconductors is reduced to improve the converter efficiency. Moreover, by utilizing the magnetizing inductor and leakage inductance of transformer, soft switching can be achieved in power switching devices [8].



To achieve high efficiency and high power density performance, several operational characteristics of an isolated topology must be investigated for its utilization in high output voltage applications. These are:

- 1) Constant high switching frequency, allowing to choose the optimum switching frequency with reducing the reactive elements, such as inductors, filter capacitors and the power transformer;
- 2) Soft-commutation in the power switches, avoiding an efficiency reduction due to the increment of the switching frequency;
- 3) Incorporation of the intrinsic elements of the circuit in the converter operation, like

the switch capacitance, the leakage inductance and the equivalent capacitance of the high-voltage transformer, thus avoiding the dissipation of the energy stored in these elements;

- 4) A step-up output characteristic, reducing transformer turns-ratio and minimizing the effects of the transformer equivalent capacitance referred to the transformer primary side;
- 5) Good load regulation and operation with a large input voltage variation;

Considering the above characteristics as criteria for choosing the isolated converters, several topologies were proposed in literature [9]-[16]. These can be classified into voltage-fed and current-fed configurations. For instance, a conventional voltage-fed full-bridge converter is shown in Fig. 1-2. It is characterized as buck-derived isolated converter. High turns-ratio of transformer is required to meet high step-up voltage gain demand and thus the parasitic capacitance and leakage inductance of transformer are introduced resulting in making worse the converter performance. For instance, the secondary winding leakage inductance and the parasitic capacitance of the rectifier diodes cause undesirable voltage spikes which can damage power semiconductor devices. In addition, the construction of the transformer with high turns-ratio leads to high insulation requirement and larger number of the secondary winding. Thus the transformer is bulky and expensive.

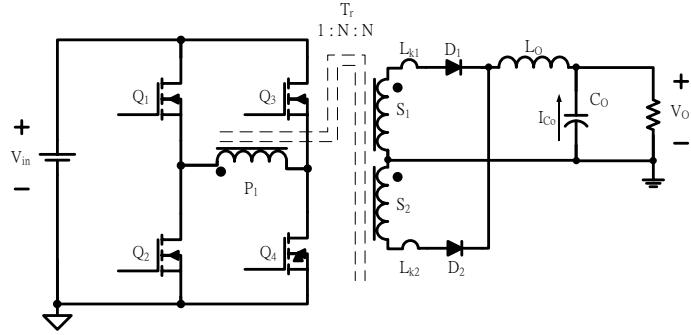


Fig. 1-2. Circuit diagram of conventional voltage-fed full-bridge converter.

On the contrary, the current-fed isolated boost converter is characterized as a boost-derived converter as shown in Fig. 1-3. Because part of the voltage gain can be provided by the input inductor, the overall voltage gain can be obtained with a comparatively low turns-ratio transformer. Without output filter inductor, the rectifier diode's blocking voltage is reduced as compared with voltage-fed configuration topologies.

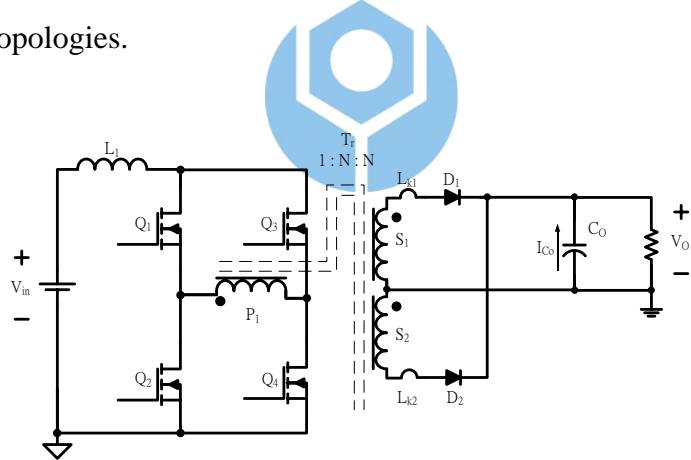


Fig. 1-3. Circuit diagram of conventional current-fed full-bridge converter.

Accordingly, the current-fed configuration is more suitable for step-up power conversion applications. Several current-fed converter topologies with clamping circuit have been proposed to provide high voltage gain and alleviate voltage and current spikes. Among them, two current-fed isolated boost converters, single inductor isolated boost converter [14] and dual-inductor isolated boost converter [15],

[16], are widely used for high output voltage applications as shown in Fig. 1-4 and Fig. 1-5, respectively.

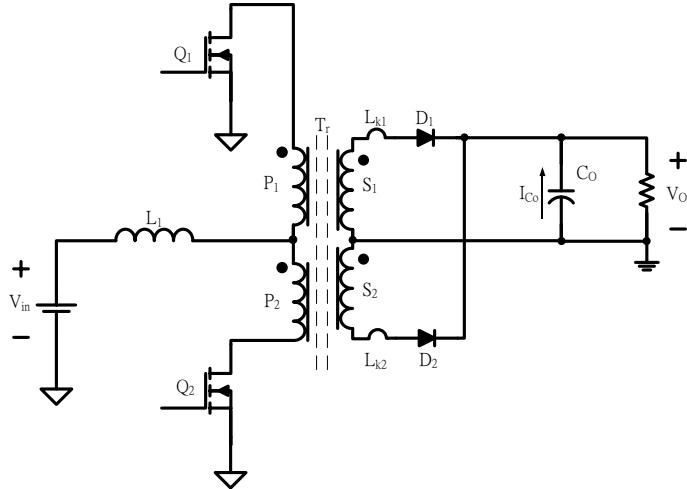


Fig. 1-4. Circuit diagram of current-fed single inductor boost converter.

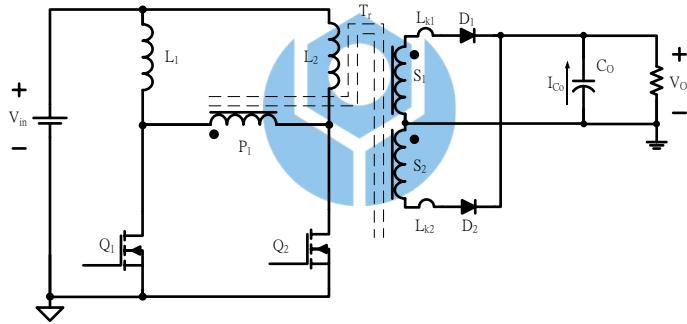


Fig. 1-5. Circuit diagram of current-fed dual-inductor boost converter.

In addition, the input current of dual-inductor boost converter is evenly distributed. Thus, two input inductors are more effectively utilized with a smaller volume. To obtain the same voltage gain, moreover, a smaller turns-ratio of a transformer can be used in a dual-inductor boost converter than that of a single inductor boost converter. Thus, a comparatively low voltage stress on the MOSFETs can be used and this results in reduced conduction loss [17]. In addition,

the transformer and inductors copper losses are also reduced due to lower RMS current. Consequently, the converter efficiency can be improved.

To enhance converter performance, the secondary rectifier stage is investigated. The circuit diagram and key waveforms of a dual-inductor current-fed boost converter using conventional central-tapped rectification-filter circuit are shown in Fig. 1-6(a) and Fig. 1-6(b), respectively. The rectifier diode's blocking voltage is two times of output voltage and suffers from voltage spikes caused by the transformer secondary leakage inductance and the diode parasitic capacitance. Moreover, it has a high output capacitor current ripple due to the lack of the output inductor. Consequently, a turn-off snubber circuit and a larger number of the output capacitor are needed. These components degrade converter efficiency and power density performance.

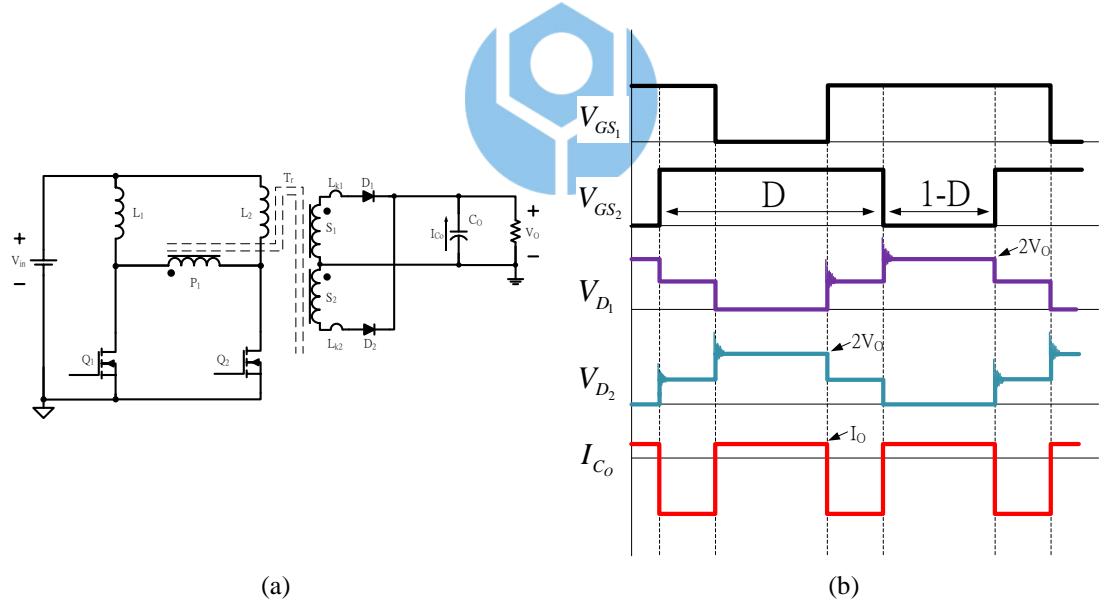


Fig. 1-6. (a) Circuit diagram and (b) key waveforms of conventional central-tapped rectification.

On the contrary, a voltage doubler rectifier derived from two conventional half-wave rectifiers can be employed instead as shown in Fig. 1-7(a) [18]-[21]. Without adding snubber circuits, the voltage waveforms of the diodes are clamped to

output voltage and free from voltage spikes as shown in Fig. 1-7(b). The comparatively low voltage-rating diodes accompanied with low forward drop can thus be used and this results in reducing the conduction loss and improving the efficiency. Moreover, two times voltage gain is provided by the voltage doubler rectifier. The turns-ratio of the transformer is thus reduced to minimize the side effect caused by the parasitic capacitance and leakage inductance. An active-clamp circuit can also be included to overcome the effect of high voltage spikes on the main switches and to recycle the leakage energy as well.

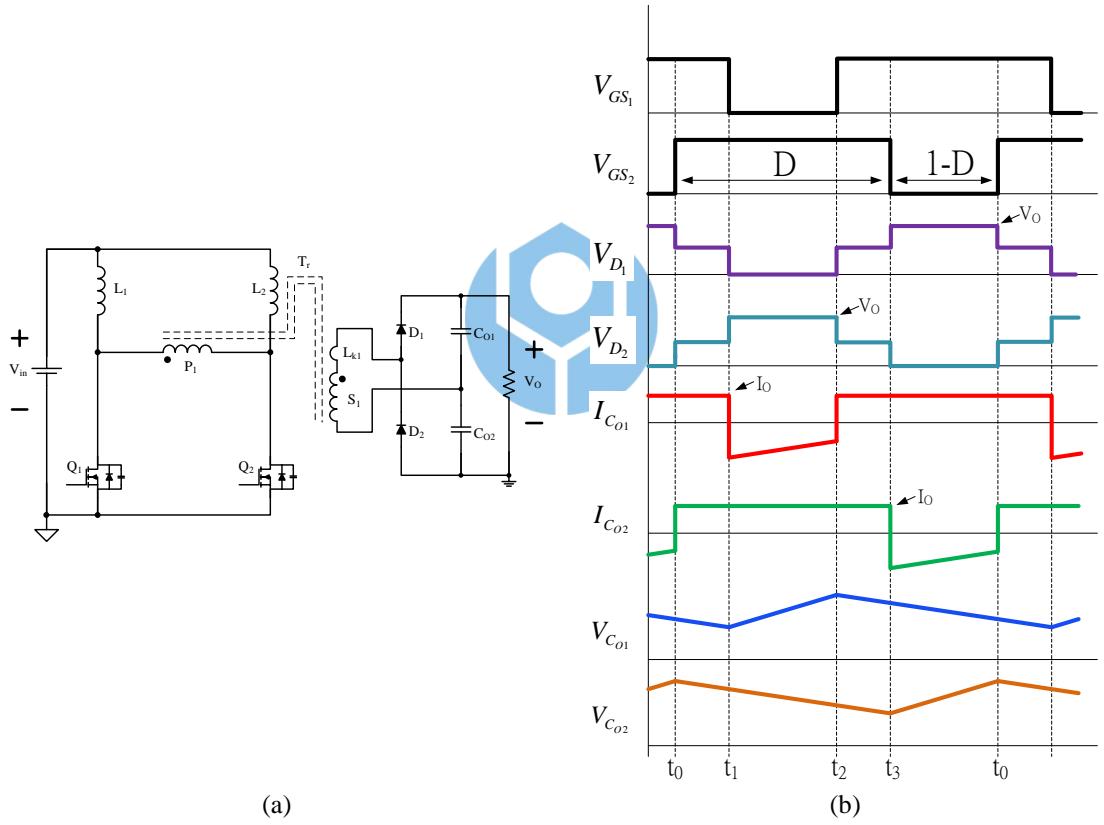


Fig. 1-7. (a) Circuit diagram and (b) key waveforms of conventional voltage doubler rectification.

However, the conventional voltage doubler rectifier still has a high output capacitor current ripple due to lacking of output inductor. High current ripple makes high ESR dissipation resulting in capacitors lifetime degradation. Consequently, large number of high voltage-rating aluminum electrolytic capacitor is generally

paralleled to deal with this current ripple issue [22]. In addition to having bulky volume and heavy weight, the aluminum capacitor becomes the prime factor of reliability degradation of the power converter due to the temperature rising induced by the internal heating generated from current ripple [23]. Therefore, a voltage doubler rectifier having reduced capacitor's current ripple and smaller output voltage ripple is preferred instead. However, it is not fully explored yet and it becomes one of the motivations of this research. To achieve this goal, a novel Taiwan Tech voltage doubler rectifier (TTVD) is proposed which is also derived from two conventional half-wave rectifiers as shown in Fig. 1-8 [24].

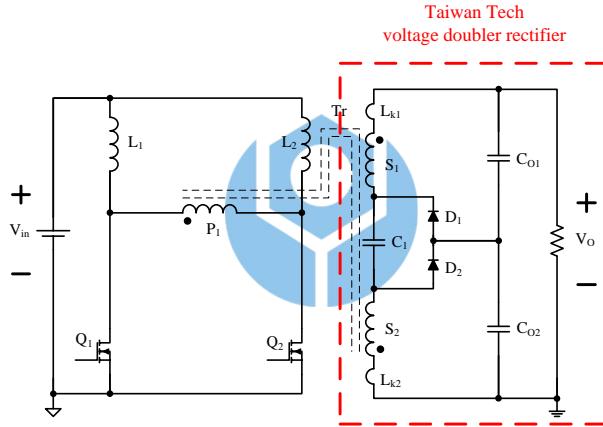


Fig. 1-8. Proposed circuit diagram of Taiwan Tech voltage doubler rectifier.

Furthermore, there are many different applications where the use of higher than several thousands of volt level dc output voltage is demanded, such as X-ray systems, electron microscopes, and lasers systems, etc. [25]-[31]. As shown in Fig. 1-9, high output voltage can be achieved by using a comparatively high turns-ratio of transformer. However, to obtain a high voltage gain through a high turns-ratio transformer is undesirable because it has large parasitic capacitance and leakage inductance. The parasitic elements lead to current or voltage spikes on power

devices to increase loss and noise. Moreover, the rectifier diodes and output capacitors suffer from high voltage stress resulting in increasing the conduction loss and the volume of capacitors. Thus, the efficiency and power density performance are degraded.

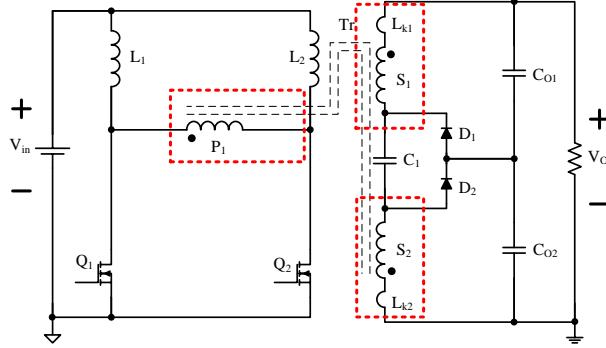


Fig. 1-9. Step-up circuit for high output voltage by using high turns-ratio of transformer.

To alleviate the effect of parasitic elements on power converters, two approaches have been proposed. One of the solutions is series-connected the multi-stage voltage multiplier rectifier modules by using a multi-winding of transformer secondary. For instance, a four-stage series-connected voltage doubler rectifier modules converter is shown in Fig. 1-10. Consequently, one-fourth turns-ratio of transformer is applied to reduce the parasitic capacitance and leakage inductance. The voltage-ratings of the rectifier diodes and output capacitors are thus reduced to $V_o/4$ and $V_o/8$, respectively. However, by using a multi-winding of transformer complicates the design and construction of the transformer.

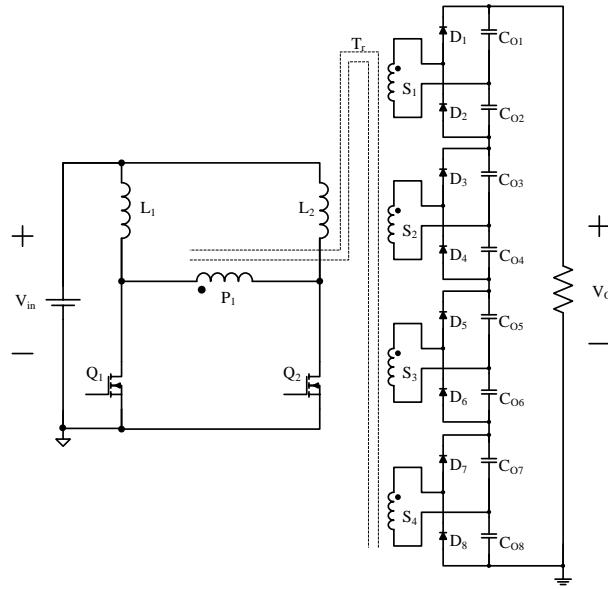


Fig. 1-10. Four-stage series-connected rectifier-modules of transformer configuration.

The other approach is to use the voltage multiplier rectifier on the secondary side of the transformer. It allows higher voltages to be created from a low voltage power source without a need for an expensive high voltage transformer [18]-[19]. For example, a six-fold Cockcroft-Walton voltage multiplier rectifier is applied as shown in Fig. 1-11. Consequently, one-third of turns-ratio of a transformer is applied to reduce the parasitic capacitance and leakage inductance. The voltage stresses on the rectifier diodes are thus reduced to $V_o/3$. On the other hand, the voltage-rating of the output capacitor, C_1 , is reduced to $V_o/6$ and the others output capacitors, C_2-C_6 , are reduced to $V_o/3$, respectively. However, it can only supply low currents to a high-resistance ($+100k\Omega$) load because the generated output voltage quickly drops-off as load current increases.

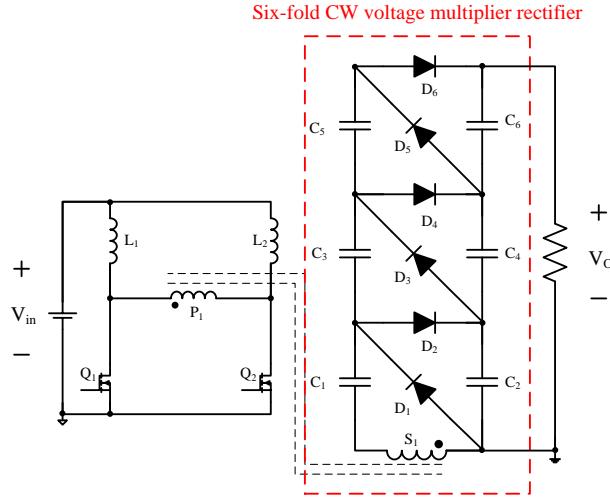


Fig. 1-11. Six-fold CW voltage multiplier rectifier

Therefore, a voltage multiplier rectifier having low voltage drop for high output voltage applications is preferred. However, it is not fully explored yet [29], [31] and it becomes another motivation of this research. To achieve this goal, a novel Taiwan Tech voltage multiplier rectifier (TTVM) is thus proposed as shown in Fig. 1-12 [32].

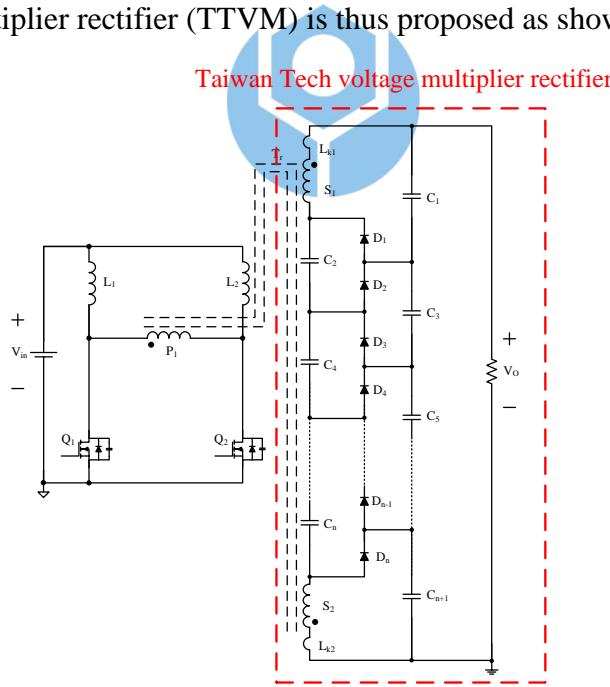


Fig. 1-12. Taiwan Tech voltage multiplier rectifier (TTVM).

1.2 Objectives of dissertation

To achieve the aforementioned goals, a Taiwan Tech voltage doubler rectifier (TTVD) and a Taiwan Tech voltage multiplier rectifier (TTVM) are proposed in this dissertation.

Five objectives are listed below:

1. To reduce the voltage stress on rectifier diodes and output capacitor;
2. To reduce the output voltage ripple with small capacitance;
3. To reduce the output capacitor current ripple to improve converter reliability;
4. To obtain high step-up voltage conversion gain from voltage multiplier rectifier, thus small turns-ratio of transformer can be applied;
5. To reduce the output voltage drop of voltage multiplier rectifier as load current increased.

1.3 Organization of dissertation

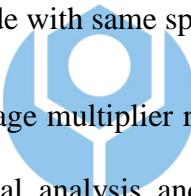
By applying the proposed TTVD and TTVM to replace the conventional voltage doubler rectifier and voltage multiplier rectifier, a dual-inductor current-fed boost converter with Taiwan Tech voltage doubler rectifier (DB-TTVD) and a dual-inductor current-fed boost converter with Taiwan Tech voltage multiplier rectifier (DB-TTVM) are presented as two examples for the sustainable energy sources power conversion applications and higher than several thousands of volt output voltage applications,

respectively.

This dissertation consists of four chapters organized as follows:

Chapter 1: To describe the background, motivation and the objectives of this dissertation.

Chapter 2: By employing a novel voltage doubler rectifier, a dual-inductor current-fed boost converter with Taiwan Tech voltage doubler rectifier (DB-TTVD) is proposed in this chapter. The operation principle, theoretical analysis, design considerations, and experimental results are presented. Moreover, the characteristic comparison between conventional full-wave voltage doubler rectifier and Taiwan Tech voltage doubler rectifier is made with same specification.



Chapter 3: The Taiwan Tech voltage multiplier rectifier (TTVM) is proposed in this chapter. The theoretical analysis and circuit characteristic comparison with conventional CW voltage multiplier rectifier are described. To demonstrate the feasibility of TTVM, a dual-inductor current-fed boost converter with six-fold TTVM (DB-TTVM-6) is implemented and tested as an example to demonstrate the feasibility of the proposed TTVM in this chapter.

Chapter 4: To summarize this dissertation and to propose several future researches.

Chapter 2 Dual-Inductor Current-Fed Boost converter with Taiwan Tech Voltage Doubler Rectifier (DB-TTVD)

2.1 Introduction

In renewable energy power generation systems, the input source generally produces low voltage level such as photovoltaic cell and fuel cell. The step-up voltage conversion is required to provide output voltage demand in power converter. The boost converter is widely used configuration due to simplify circuit construction. However, the step-up voltage gain is restricted to parasitic components as described in previous chapter. To obtain high step-up voltage gain, a high voltage transformer and voltage doubler rectifier can be applied.



The conventional voltage doubler rectifier is shown in Fig. 2-1. According to Section 1.1, it has several advantages, such as lower voltage stress on the diodes, free of voltage spikes, reduced voltage ripple, and higher voltage gain over the central-tapped rectifier for high output-voltage power conversion applications. However, the output capacitors suffer from high current ripple due to the lack of an output inductor. In addition, the ESR of the output capacitor introduces power dissipation and makes capacitor lifetime degradation. Consequently, a large number of output filter capacitors are required to deal with the voltage ripple and ESR dissipation. In general, high voltage rating aluminum electrolytic capacitors are widely used due to its low cost and high capacitance performance. It becomes the reliability issue of concern.

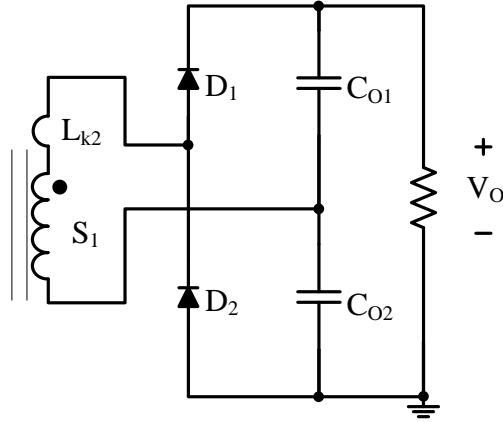


Fig. 2-1. Circuit diagram of conventional full-wave voltage doubler rectifier.

To enhance the reliability performance, film capacitor is thus preferred. However, it suffers from degrading the power density performance due to small capacitance. To provide a comprehensive solution, the conventional half-wave voltage doubler rectifier is thus re-examined. As illustrated in Fig. 2-2(a) is the circuit diagram of a conventional half-wave voltage doubler rectifier. By inverting the diode polarity, a modified half-wave voltage doubler rectifier can be obtained with opposite voltage potential as shown in Fig. 2-2(b).

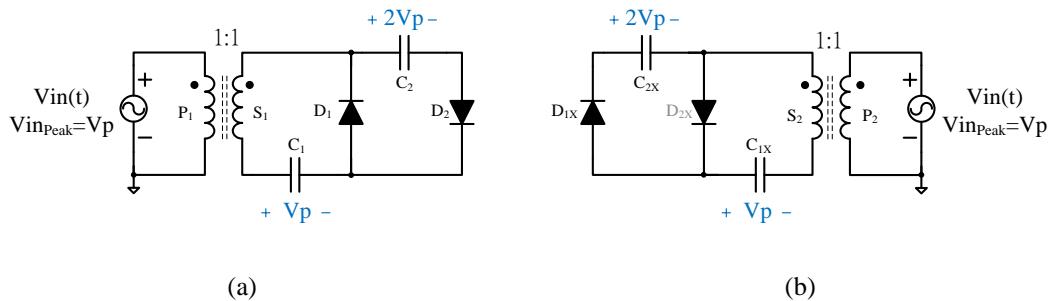


Fig. 2-2. Circuit diagrams of (a) conventional and (b) modified half-wave voltage doubler rectifier.

Circuit operations of these two voltage doubler rectifiers during positive half cycle and negative half cycle are illustrated in Fig. 2-3(a) and Fig. 2-3(b), respectively. As shown in Fig. 2-3(a), rectifier diodes, D_2 and D_{2X} , are turned-on due to the forward biased by their individual input source. Capacitors, C_2 and C_{1X} are respectively

charged by the input source via $C_2(-)$ - D_2 - C_1 - S_1 - $C_2(+)$ and $C_{1X}(-)$ - S_2 - D_{2X} - $C_{1X}(+)$, respectively. On the other hand, rectifier diodes, D_1 and D_{1X} are turned-on as shown in Fig. 2-3(b). Capacitors, C_1 and C_{2X} are charged by the input source via $C_1(-)$ - D_1 - S_1 - $C_1(+)$ and $C_{1X}(+)$ - D_{1X} - C_{2X} - S_2 - $C_{1X}(-)$, respectively. It can be seen that the components in each pair, D_1 - D_{1X} , C_2 - C_{2X} and D_2 - D_{2X} performs the same function as its count part. In addition, the capacitors, C_2 and C_{2X} have same voltage level and polarity. Consequently, the equivalent circuit can be obtained by merging both half-wave voltage doubler rectifier circuits into one and a novel Taiwan Tech voltage doubler rectifier (TTVD) is proposed as shown in Fig. 2-3(c).

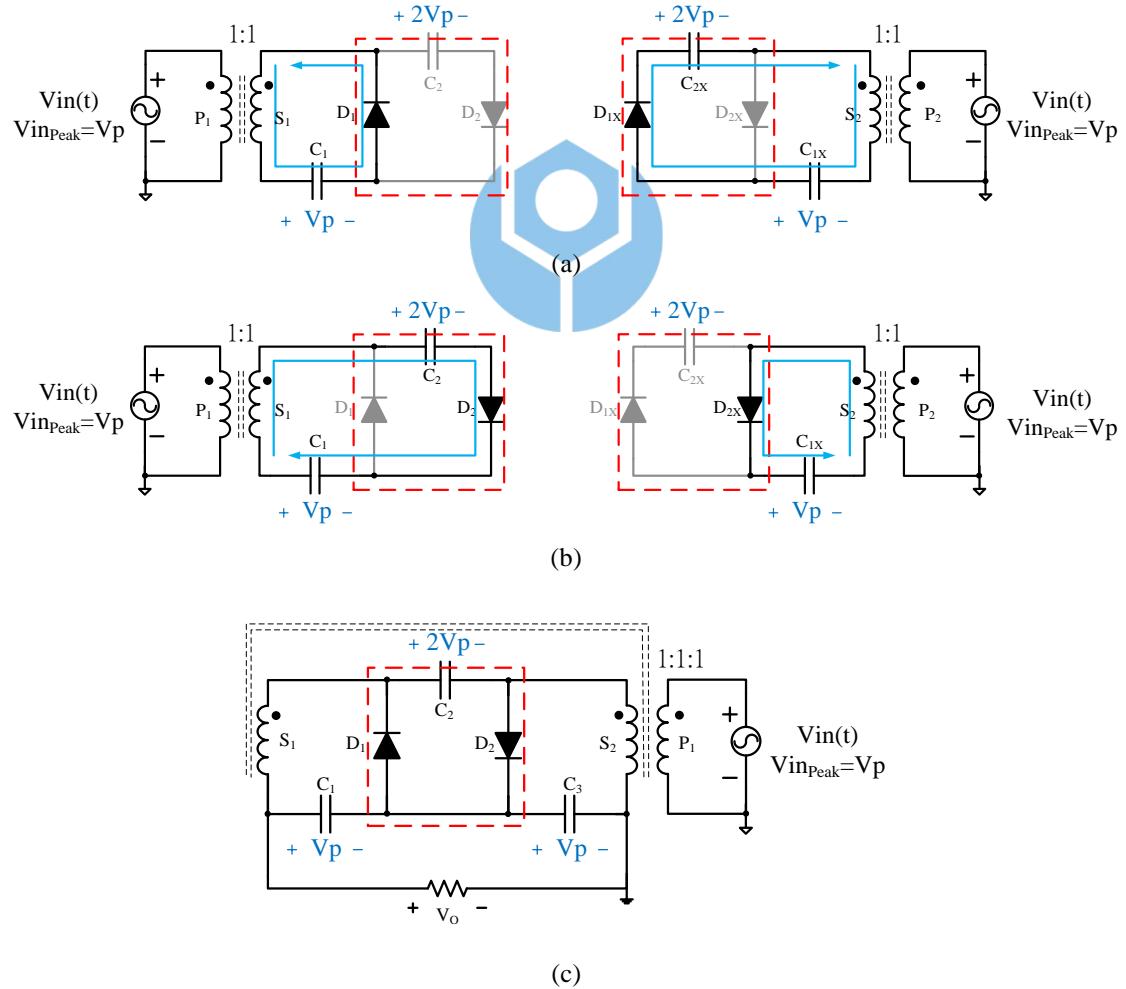


Fig. 2-3. (a) (b) Evolution of proposed rectifier and (c) proposed Taiwan Tech voltage doubler rectifier.

To integrate the proposed voltage doubler rectifier with an isolated boost converter, a dual-inductor current-fed boost converter with Taiwan Tech voltage doubler rectifier (DB-TTVD) is presented as shown in Fig. 2-4.

In Sections 2.2 and 2.3, the operational principle and circuit analysis of DB-TTVD are described. Also, the characteristics comparison between the proposed circuit and the conventional voltage doubler rectifier are discussed in Section 2.4. The hardware implementation is presented to demonstrate its feasibility in Section 2.5 and Section 2.6, the design processes of DB-TTVD are described with 100 kHz, 24~36V input range and 380V/1A output power operating conditions. The summary of this chapter is given in Section 2.7.

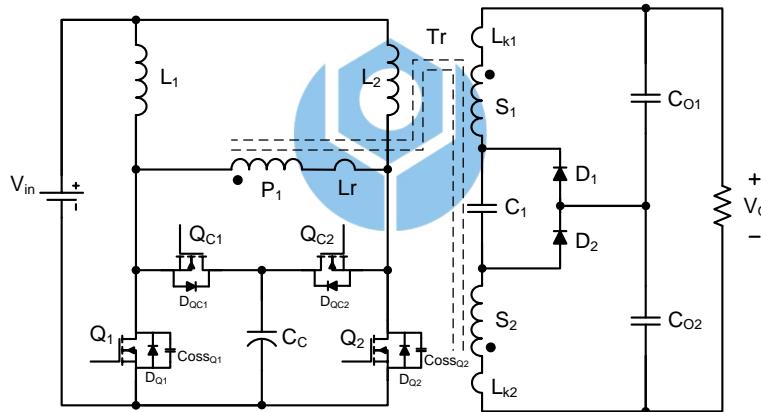


Fig. 2-4. Circuit diagram of DB-TTVD.

2.2 Operation Principle

A dual-inductor current-fed boost converter with Taiwan Tech voltage doubler rectifier (DB-TTVD) is illustrated in Fig. 2-4. It comprises two input inductors, L_1 and L_2 , one transformer, T_r , two main switches, Q_1 and Q_2 , two clamping switches, Q_{C1} and Q_{C2} , and two clamping capacitors, C_C and C_1 , two output capacitors C_{O1} and C_{O2} , and two rectifier diodes D_1 and D_2 . The transformer consists of one primary winding

P_1 and two identical secondary windings S_1 and S_2 , with the $1:n:n$ turns-ratio. L_r , L_{k1} and L_{k2} are represented as the leakage inductor of P_1 , S_1 and S_2 , respectively. D_{Q1} , D_{QC1} , D_{Q2} , D_{QC2} , $Coss_{Q1}$, and $Coss_{Q2}$ are represented as the body-diode and output capacitance of their respective switches. The key waveforms of the proposed DB-TTVD are shown in Fig. 2-5.

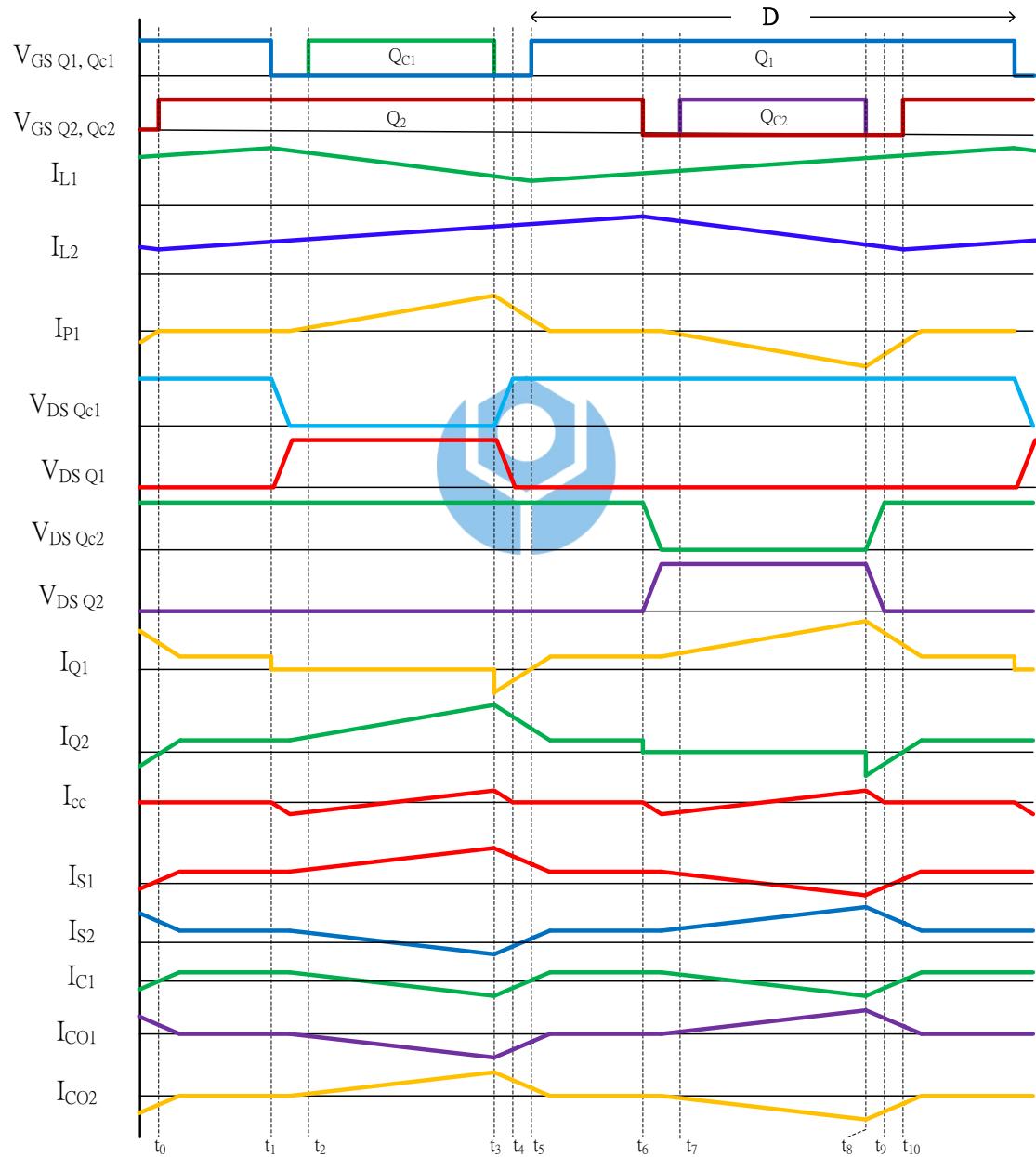


Fig. 2-5. Key waveforms of DB-TTVD.

To simplify the analysis, all diodes are assumed to be ideal. The clamping capacitor, C_1 , and output capacitors, C_{O1} and C_{O2} , are assumed to be sufficiently large so that the voltage across these capacitors are constant and equal to V_O and $1/2V_O$, respectively. Two input inductors L_1 and L_2 are assumed to be sufficiently large as two current sources. Two leakage inductances of secondary windings, L_{k1} and L_{k2} , are assumed to be equal. There are ten operating stages within one switching cycle during the steady-state operation. Due to the analogous circuit operation, only first five stages are described as follows.

Stage 1 [t_0-t_1]:

Before t_1 , main switches Q_1 and Q_2 are turned on, and clamping switches Q_{C1} and Q_{C2} are turned off. As shown in Fig. 2-6, the voltage across the transformer is thus shorted and the current of two input inductors increases linearly. Without forward bias, both diodes D_1 and D_2 are turned off and clamped to $V_O/2$. The average voltage across C_1 is equal to output voltage. The output current is the sum of the current through output capacitors and clamping capacitor as shown:

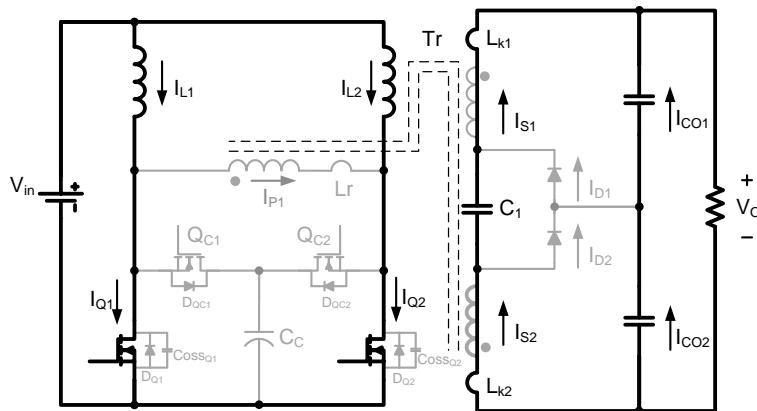


Fig. 2-6. Operating stage of DB-TTVD during $[t_0-t_1]$ time interval.

Stage 2 [t_1-t_2]:

At t_1 , the main switch Q_1 is turned off by the control signal. As shown in Fig. 2-7, the parasitic capacitor of main switch, C_{ossQ1} , is charged by the current through input inductor, L_1 . The voltage across parasitic capacitor of main switch, V_{cossQ1} , is linearly increased and clamped to the V_{Cc} due to turning-on of the D_{Qc1} . The voltage across the primary winding is the sum of the input voltage and the voltage across L_1 . Thus, the rectifier diode D_1 is turned on due to its forward bias. Consequently, input power energy are transferred from primary winding to both of the secondary windings to charge output capacitor C_{O1} and clamping capacitor C_1 via $S_1(+)-C_{O1}-D_1-S_1(-)$ and $S_2(+)-C_{O2}-D_1-C_1-S_2(-)$, respectively. Also, the voltage across D_2 is clamped to V_{C1} due to the turning on of the D_1 .

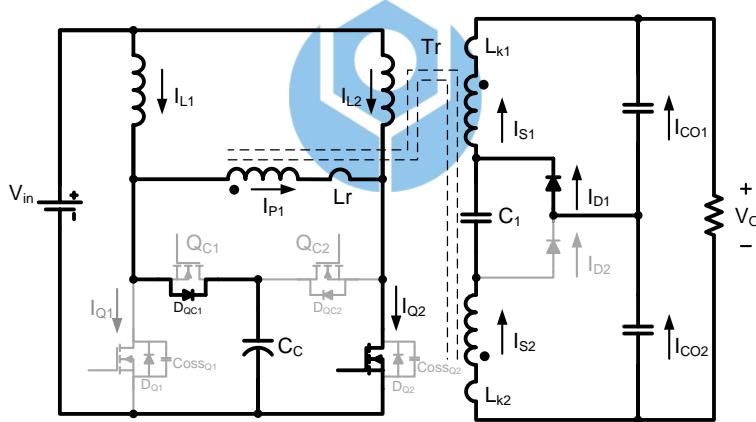


Fig. 2-7. Operating stage of DB-TTVD during $[t_1-t_2]$ time interval.

Stage 3 [t_2-t_3]:

At t_2 , the clamping switch Q_{C1} is turned on by the control signal to achieve the zero voltage turned-on (ZVS). As shown in Fig. 2-8, the energy stored in clamping capacitor C_C can be released to the secondary windings via transformer due to the turning-on of clamping switch during this time interval.

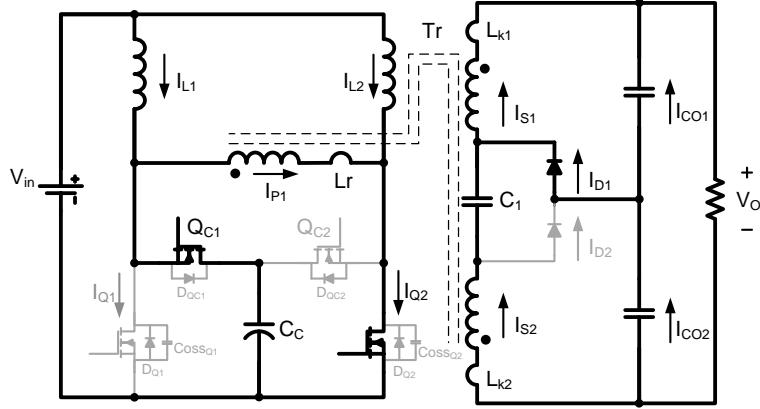


Fig. 2-8. Operating stage of DB-TTVD during $[t_2-t_3]$ time interval.

Stage 4 $[t_3-t_4]$:

As shown in Fig. 2-9, the clamping switch is turned off by the control signal at t_3 . The parasitic capacitor of main switch, C_{ossQ1} , is discharged by the leakage inductor current via $P_1(-)$ - L_r - C_{ossQ1} - $P_1(+)$. To ensure that voltage across parasitic capacitor of main switch, C_{ossQ1} , declines to zero, the energy which stores in leakage inductor has to be sufficiently large as shown in Eq. (2-1), where the discharging time of parasitic capacitor of main switch is calculated as follows.

$$L_r \cdot I_{L_{r_{peak}}}^2 \gg C_{ossQ_1} \cdot V_{DSQ_1}^2 \quad (2-1)$$

$$D_{deadtime} \cdot T_s > \frac{C_{ossQ_1} \cdot V_{DSQ_1}}{I_{L_{r_{peak}}}} \quad (2-2)$$

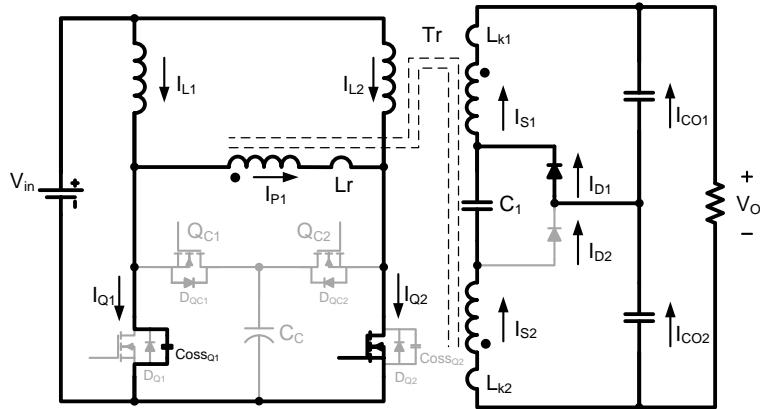


Fig. 2-9. Operating stage of DB-TTVD during $[t_3-t_4]$ time interval.

Stage 5 [t₄-t₅]:

At t₄, the voltage across main switch Q₁ is clamped to zero due to turning-on of the body diode. The voltage across leakage inductor, L_r, is equal to the voltage of transformer primary winding as shown in Fig. 2-10. Thus, the current through transformer primary winding decreased linearly with the slope which depended on the leakage inductance, L_r. The main switch, Q₁, can be turned on at this time interval to achieve ZVS operation.

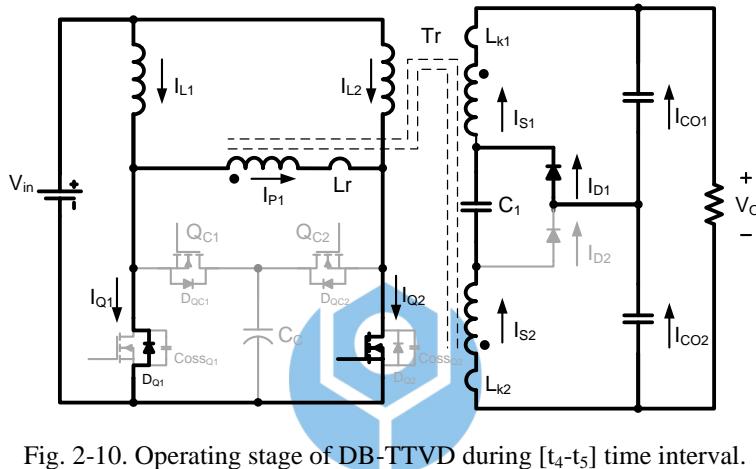


Fig. 2-10. Operating stage of DB-TTVD during [t₄-t₅] time interval.

After t₅, the operation that in [t₅-t₆] is identical to Stage 1[t₀-t₁]. The operations of the following stages during another half period are analogous.

2.3 Circuit analysis

2.3.1 Voltage gain

By applying volt-second balance of input inductor, L₁, the voltage gain is derived as follows.

$$V_{in} \cdot DT_s + (V_{in} - V_{Cc}) \cdot (1-D)T_s = 0 \quad (2-3)$$

During main switch turned off, the voltage across transformer primary winding is equal to that of clamping capacitor, C_C , as shown in Eq. (2-4)

$$V_{Cc} = \frac{V_o}{2N} \quad (2-4)$$

Thus, the voltage gain of proposed circuit is calculated as follows.

$$\frac{V_o}{V_{in}} = \frac{2N}{1-D} \quad (2-5)$$

The converter is operated in continuous conduction mode (CCM).

2.3.2 ZVS operation of switches, Q_1 , Q_2 , Q_{C1} , and Q_{C2}

The four switches of proposed converter can achieve zero voltage switching operation to reduce the switching loss. The main switches and clamping switches have different ZVS conditions. The equivalent circuit diagrams of main switches and clamping switches during switching transient are illustrated as Fig. 2-11. As shown in Fig. 2-11(a), when main switches turned off the current through parasitic capacitor of clamping switch is provided by the input inductor. Therefore, the clamping switches, Q_{C1} and Q_{C2} , are easily to be achieved ZVS operation. On the other hand, the ZVS conditions of main switches are depended on the leakage inductor, L_r , as shown in Fig. 2-11(b). Thus, the design of leakage inductance, L_r , will directly limit the ZVS condition of main switches.

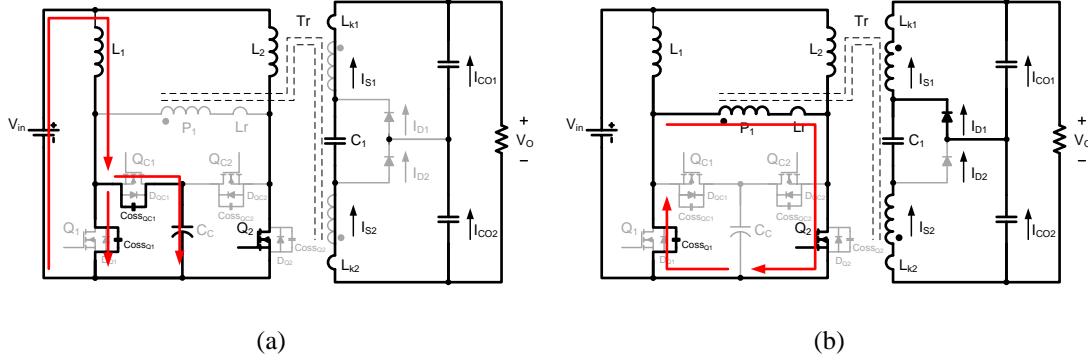


Fig. 2-11. Circuit operation during (a) [t₁-t₂] and (b) [t₄-t₅] time interval.

Therefore, the leakage inductor has to provide enough energy to discharge the parasitic capacitor of main switches Q₁ and Q₂. The equation has to be met as follows.

$$L_r \cdot I_{L_{r_{peak}}}^2 \gg C_{ossQ_1} \cdot V_{DSQ_1}^2 \quad (2-6)$$

2.3.3 Output capacitor current analysis

For simply illustrating the current of output capacitors, all waveforms are shown that converter operated with ideal components and without active clamp circuit. From previous descriptions, the proposed rectifier can be generalized to two phases, T_{charge} and T_{transfer}, within half of the switching cycle as illustrated in Fig. 2-12. The time intervals are given as Eq. (2-7) and Eq. (2-8).

$$T_{charge} = (D - \frac{1}{2}) \cdot T_s \quad (2-7)$$

$$T_{transfer} = (1 - D) \cdot T_s \quad (2-8)$$

During T_{transfer} time interval, the energy is transferred to secondary side via transformer. The current ripple through the output capacitor is equal to the transformer secondary winding as shown in Fig. 2-12(a) and Fig. 2-12(b), respectively.

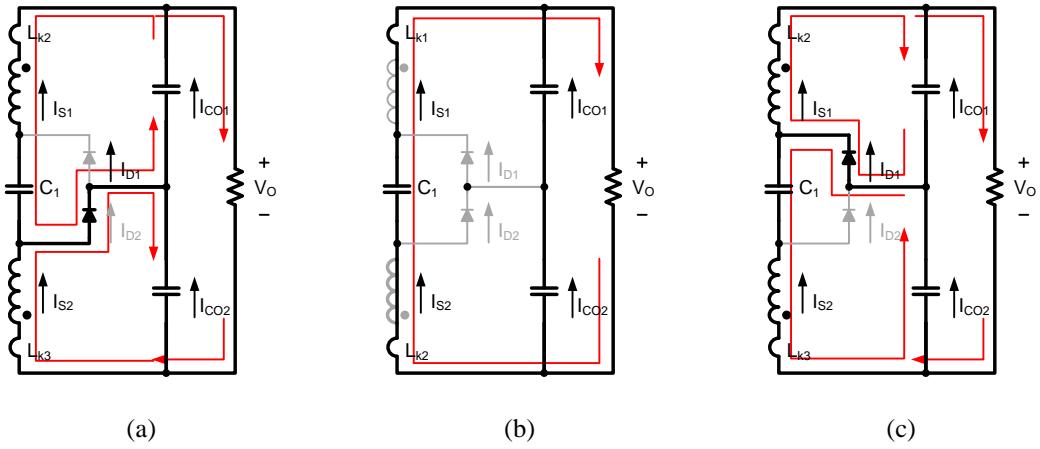


Fig. 2-12. Operational models of DB-TTVD during (a) the switch Q₂ turn off, (b) the switch Q₂ turn on, (c) the switch Q₁ turn off.

The primary side can be considered as a constant current source in current-fed converter. The equivalent diagram is illustrated as Fig. 2-13.

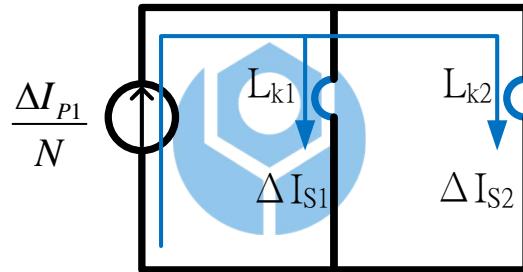


Fig. 2-13. Current ripple distribution of transformer secondary windings.

Therefore, the current ripple is distributed to transformer secondary windings and the ratio is depending on leakage inductance of transformer. The current ripple of the secondary windings is calculated as (2-10) and (2-11).

$$\frac{\Delta I_{S_1}}{\Delta I_{S_2}} = \frac{L_{k_2}}{L_{k_1}} \quad (2-9)$$

$$\Delta I_{S_i} = \frac{L_{k_2}}{L_{k_1} + L_{k_2}} \times \frac{\Delta I_{P_1}}{N} \quad (2-10)$$

$$\Delta I_{S_2} = \frac{L_{k_1}}{L_{k_1} + L_{k_2}} \times \frac{\Delta I_{P_1}}{N} \quad (2-11)$$

Several key current waveforms are thus illustrated in Fig. 2-14 to investigate the output capacitor current.

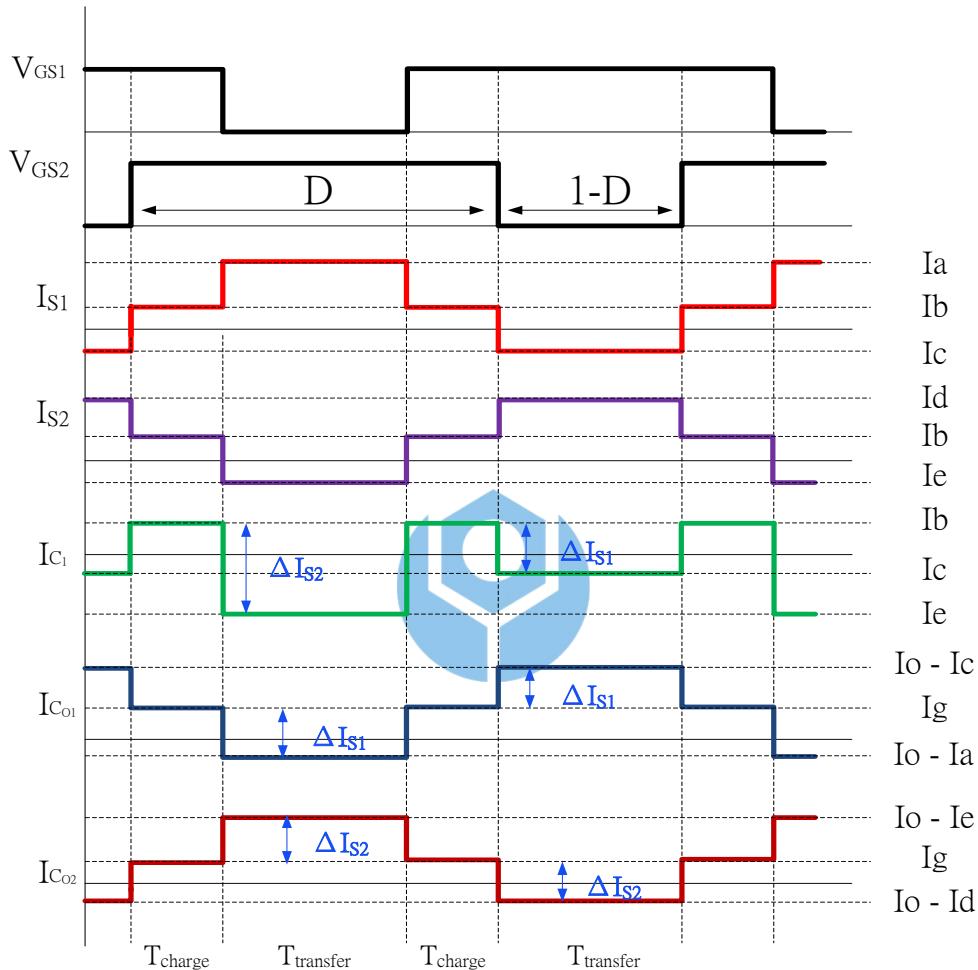


Fig. 2-14. Key current waveforms of transformer secondary windings and capacitors.

Accordingly, the Eq. (2-12) and Eq. (2-13) have to be met and the current ripple of the transformer secondary windings is shown as Eq. (2-17) and Eq. (2-18).

$$I_{S1} + I_{Co1} = I_o \quad (2-12)$$

$$I_{S2} + I_{Co2} = I_o \quad (2-13)$$

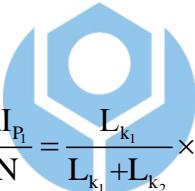
Applying the Amp-Second balance of the clamping capacitor C_1 and Eq. (2-10) and Eq. (2-11), the current through capacitor during T_{charge} is calculated as expressed in Eq. (2-14) to Eq. (2-19):

$$\int_0^{T_s} I_{C_1}(t) \cdot dt = 0 \quad (2-14)$$

$$I_b \times \left(D - \frac{1}{2} \right) T_s + I_e \times (1-D) T_s + I_g \times \left(D - \frac{1}{2} \right) T_s + I_c \times (1-D) T_s = 0 \quad (2-15)$$

$$I_b \times \left(D - \frac{1}{2} \right) T_s + (I_b - \Delta I_{S_2}) \times (1-D) T_s + I_g \times \left(D - \frac{1}{2} \right) T_s + (I_b - \Delta I_{S_1}) \times (1-D) T_s = 0 \quad (2-16)$$

$$\Delta I_{S_1} = \frac{L_{k_2}}{L_{k_1} + L_{k_2}} \times \frac{\Delta I_{P_1}}{N} = \frac{L_{k_2}}{L_{k_1} + L_{k_2}} \times \frac{I_o}{1-D} \quad (2-17)$$



$$\Delta I_{S_2} = \frac{L_{k_1}}{L_{k_1} + L_{k_2}} \times \frac{\Delta I_{P_1}}{N} = \frac{L_{k_1}}{L_{k_1} + L_{k_2}} \times \frac{I_o}{1-D} \quad (2-18)$$

$$I_b = I_o \quad (2-19)$$

Therefore, the current through output capacitors during T_{charge} is equal to zero as shown:

$$I_g = 0, I_{C_{O_{1,2}}} = 0, \text{ during } [t_0 - t_1] \text{ and } [t_2 - t_3] \quad (2-20)$$

Due to the help of clamping capacitor C_1 and the leakage inductors of the transformer secondary L_{k1} and L_{k2} , the current through the output capacitors C_{O1} and C_{O2} are nearly zero during T_{charge} time intervals and the current ripple of the output capacitors during the transient time are reduced.

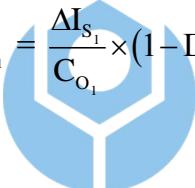
2.3.4 Output voltage ripple cancellation

Several key current and voltage waveforms are shown in Fig. 2-15. During T_{transfer} time interval, C_{O1} and C_{O2} are respectively charged and discharged. On the other hand, the current through both output capacitors are nearly zero during T_{charge} time interval referring to section 2.3.3.

Therefore, the output voltage ripple is calculated as Eq. (2-21).

$$\Delta V_O = \left| \Delta V_{C_{O_1}} - \Delta V_{C_{O_2}} \right| \quad (2-21)$$

The voltage ripple of each capacitor is calculated as Eq. (2-22) and Eq. (2-23).



$$\Delta V_{C_{O_1}} = \frac{\Delta I_{S_1}}{C_{O_1}} \times (1-D)T_s \quad (2-22)$$

$$\Delta V_{C_{O_2}} = \frac{\Delta I_{S_2}}{C_{O_2}} \times (1-D)T_s \quad (2-23)$$

As expressed in Eq. (2-9), the current ripple distribution is depended on the transformer secondary leakage inductance.

Consequently, the output voltage ripple is derived as Eq. (2-24)

$$\Delta V_O = \left| \frac{1}{C_O} \left(\frac{L_{k_2} - L_{k_1}}{L_{k_1} + L_{k_2}} \right) \cdot \frac{\Delta I_p}{N} \cdot (1-D)T_s \right| \quad (2-24)$$

Accordingly, the smaller difference between L_{k1} and L_{k2} is, the smaller output

voltage ripple will be. If $L_{k1}=L_{k2}$, zero output voltage ripple can be achieved no matter what condition operated.

Thus, the output capacitor current waveforms are symmetrical and opposite to each other resulting in achieving output ripple cancellation as shown.

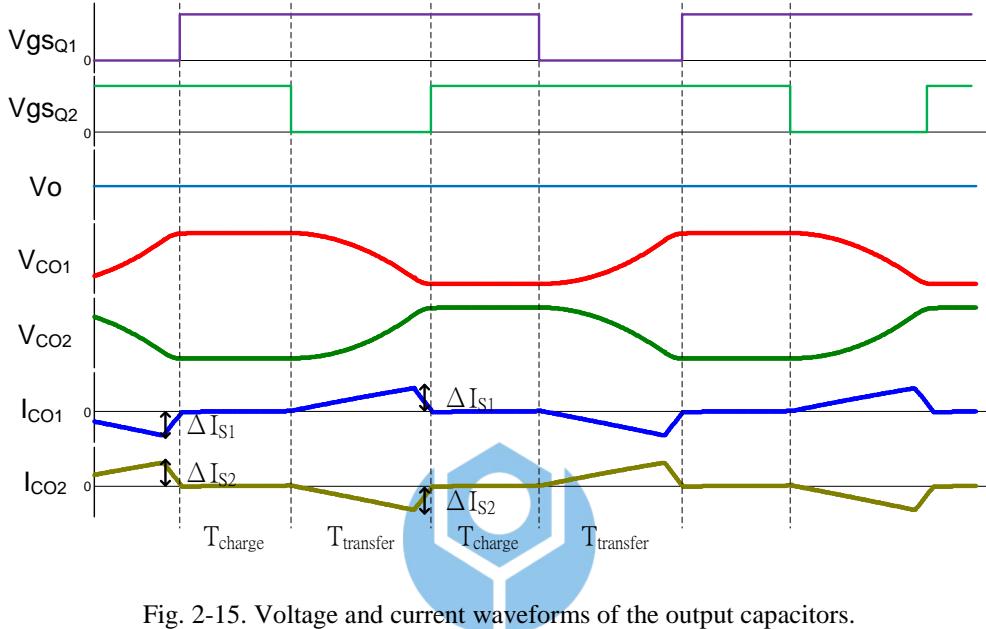


Fig. 2-15. Voltage and current waveforms of the output capacitors.

Voltage ripple caused by equivalent series resistor (ESR):

The equivalent series resistor (ESR) is one of the capacitor parasitic elements. It will cause additional voltage ripple on capacitor as current through capacitors. Thus, the voltage ripple caused by the ESR is expressed as:

$$\Delta V_{ESR} = \Delta I_{Co} \times R_{ESR} \quad (2-25)$$

As previously described, the current ripple of output capacitor, ΔI_{Co} , is equal to the current ripple of transformer secondary winding, ΔI_S . Accordingly, if $\Delta I_{S1} = \Delta I_{S2}$ is established with identical capacitor's ESR, the voltage ripple on each capacitor's ESR, ΔV_{ESR} , will be cancelled by each other as shown in Fig. 2-16.

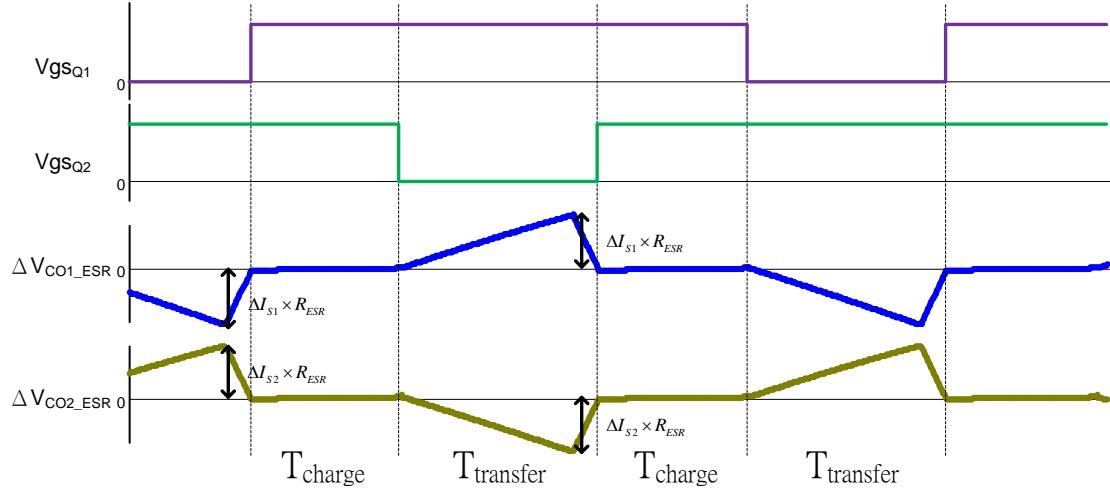


Fig. 2-16. Voltage ripple waveforms of the capacitor's ESR.

Accordingly, the smallest output voltage ripple can be obtained and the output capacitance can be reduced.

2.4 Comparisons between DB-TTVD and conventional full-wave voltage doubler rectifier (CVD)

The circuit diagrams of the dual-inductor current-fed boost converter with conventional voltage doubler rectifier (DB-CVD) and the proposed DB-TTVD are shown in Fig. 2-17 (a) and Fig. 2-17 (b), respectively. To highlight the advantages of the proposed TTVD over that of the CVD, the transformer secondary current, output capacitor current and output voltage ripple will be investigated and simulated for characteristic comparison in this section. The simulated specifications of two converters are given in Table 2-1.

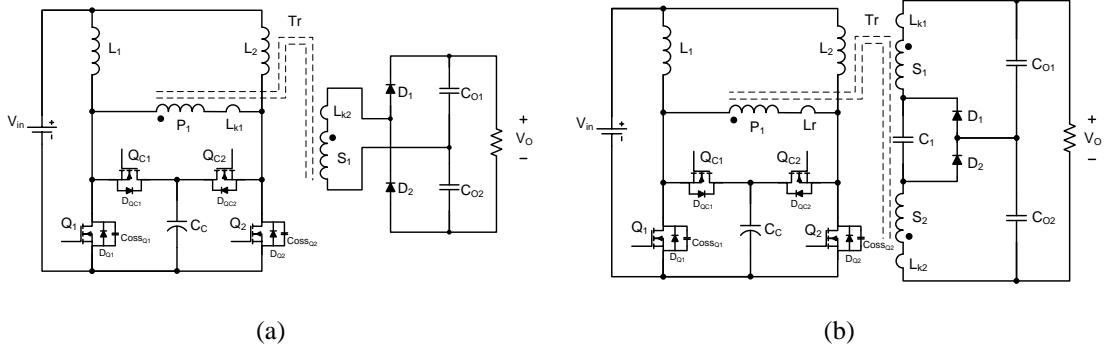


Fig. 2-17. Circuit diagrams of (a) DB-CVD and (b) DB-TTVD.

Table 2-1. Specifications of DB-CVD and DB-TTVD.

	DB-CVD	DB-TTVD
Input Voltage, V_{in}	24~36 V	
Output Voltage, V_O		380 V
Maximum Load Current, $I_{O, \text{max}}$		1 A
Maximum Load Power, $P_{O, \text{max}}$		380 W
Switching frequency, f_s		100 kHz
Turns-ratio of transformer, N	1:2	1:2:2
Leakage inductance of primary inductor, L_r		2.5 μH

2.4.1 Currents of transformer secondary windings

The current waveforms of transformer secondary windings in DB-TTVD and DB-CVD are illustrated in Fig. 2-18(a) and Fig. 2-18(b), respectively. As shown in Fig. 2-18(a), during the T_{transfer} time interval, the current is distributed to two windings in proposed circuit. On the contrary, there is only one secondary winding to suffer from current ripple in DB-CVD as shown in Fig. 2-18(b). Therefore, DB-TTVD has

smaller current ripple of transformer secondary windings than DB-CVD has so that the RMS current of transformer secondary windings is much smaller.

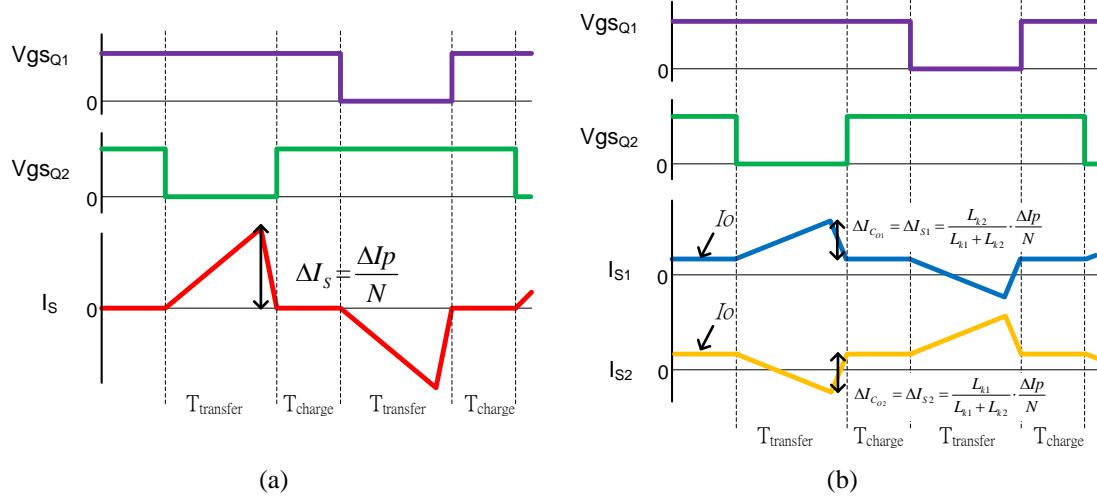


Fig. 2-18. Current waveforms of transformer secondary windings comparison between (a) DB-CVD and (b) DB-TTVD.

The worst case of the largest current ripple on transformer secondary windings is occurred in low-line ($V_{in}=24V$) operating condition. Thus, the RMS current of transformer secondary windings comparison between DB-CVD and DB-TTVD is made under low-line ($V_{in}=24V$) and different load current operating conditions as shown in Fig. 2-19. It assumes that the leakage inductances of transformer secondary windings are identical in DB-TTVD. The difference between DB-CVD and DB-TTVD increases as the load current increases. As shown, the RMS current of transformer secondary windings in DB-TTVD has 41.2% reduction than DB-CVD under low-line ($V_{in}=24V$) full-load ($I_O=1A$) operation conditions. The conduction loss of transformer secondary windings is thus reduced.

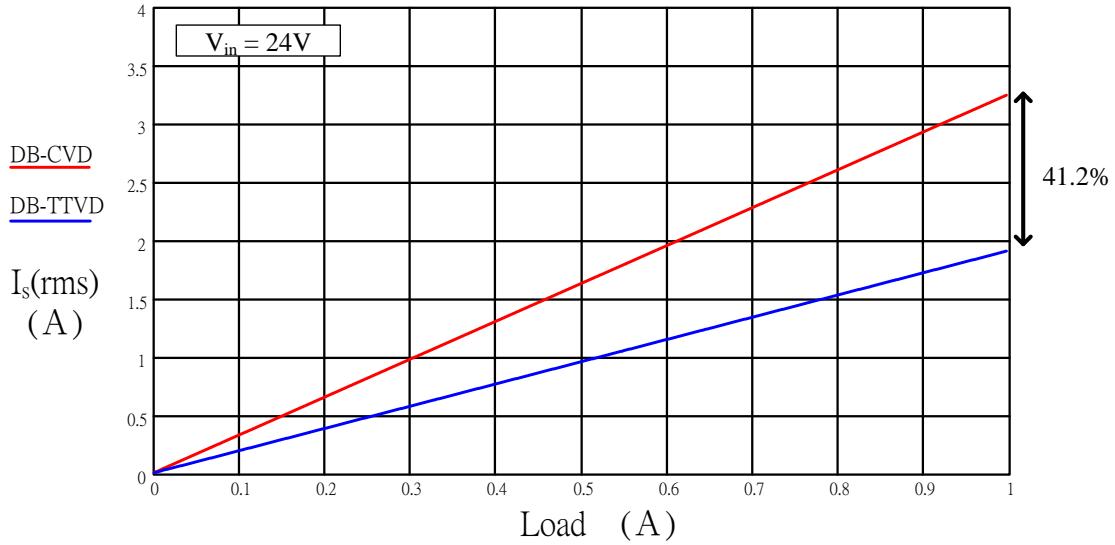


Fig. 2-19. RMS current of transformer secondary winding comparison between DB-CVD and DB-TTVD under ($V_{in}=24V$) with different load condition.

2.4.2 Current of output capacitors

The current waveforms of output capacitors in DB-CVD and DB-TTVD are shown in Fig. 2-20(a) and Fig. 2-20(b), respectively. As shown, during $T_{transfer}$ time interval, the current ripple of the output capacitors is equal to transformer secondary winding in DB-CVD and DB-TTVD. However, in DB-TTVD, the current ripple is distributed to two output capacitors and depended on the leakage inductance of transformer secondary as calculated in Eq. (2-17) and Eq. (2-18), respectively. On the contrary, in DB-CVD, during one of the capacitor is charging, the other has to supply the load current as shown in Fig. 2-20(a). Thus, the output capacitors have to suffer from all current ripple of transformer secondary. Consequently, DB-TTVD has smaller output capacitor current ripple during the $T_{transfer}$ time interval.

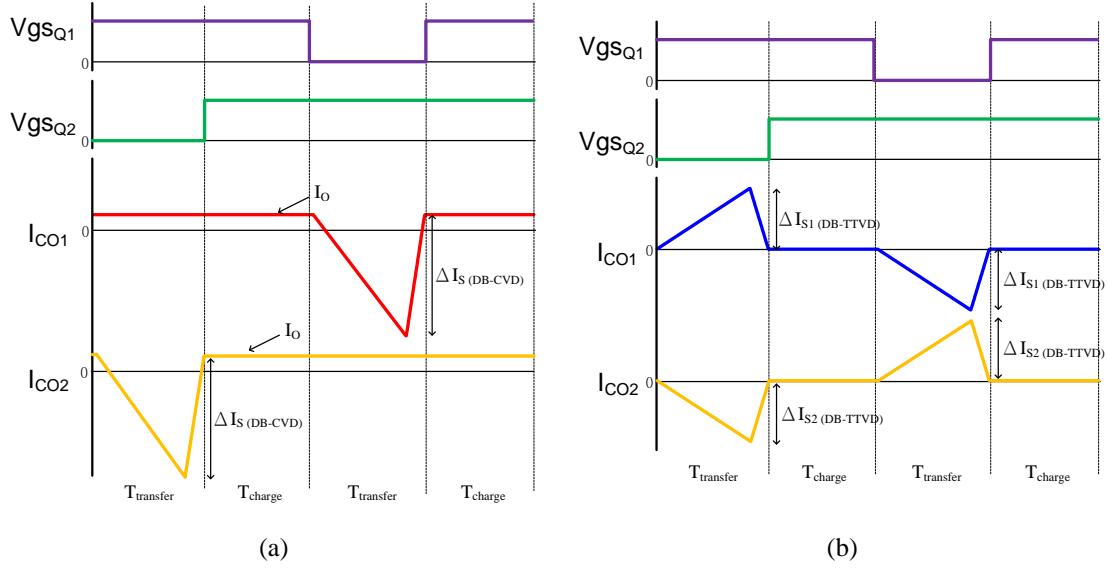


Fig. 2-20. Current waveforms of output capacitors comparison between (a) DB-CVD and (b) DB-TTVD.

The worst case of the largest current ripple on output capacitor is occurred in low-line ($V_{in}=24V$) operating condition. Thus, the RMS current of output capacitor comparison between DB-CVD and DB-TTVD is made under low-line ($V_{in}=24V$) and different load current operating conditions as shown in Fig. 2-21. Where, it assumes that the leakage inductance of transformer secondary windings is identical in DB-TTVD. The difference between DB-CVD and DB-TTVD increases as the load current increases. As shown, the RMS current of output capacitor in DB-TTVD has also 21.4% reduction than DB-CVD under low-line ($V_{in}=24V$) full-load ($I_o=1A$) operation conditions. The smaller RMS current and current ripple reduces the ESR dissipation of the output capacitors.

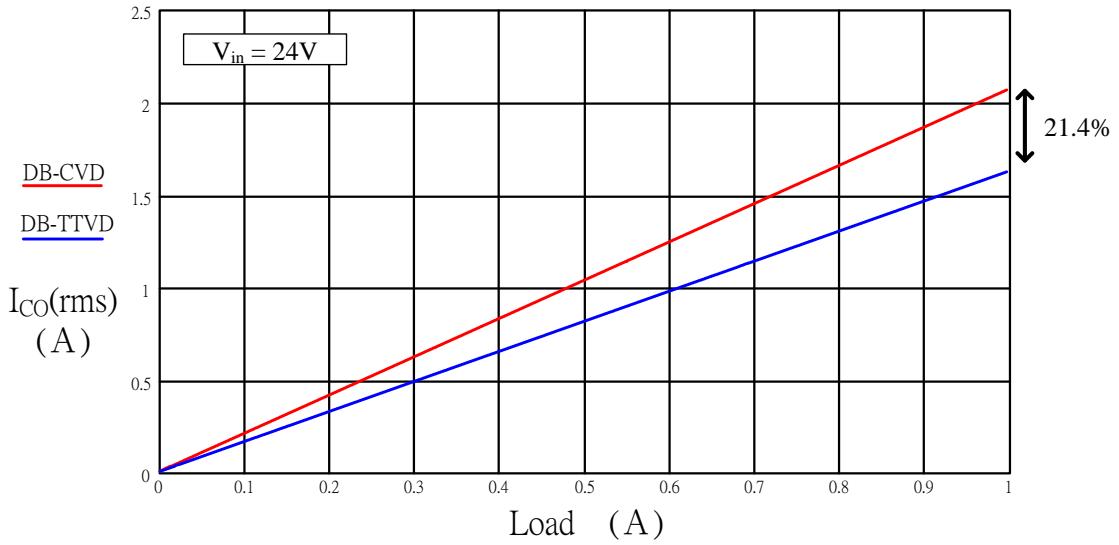


Fig. 2-21. RMS current of output capacitors comparison between DB-CVD and DB-TTVD under low-line ($V_{in}=24V$) with different load condition.

2.4.3 Output voltage ripple

Several key voltage and current waveforms of DB-CVD and DB-TTVD are illustrated in Fig. 2-22(a) and Fig. 2-22(b), respectively. As shown in Fig. 2-22(a), the voltage waveforms across the ESR of the output capacitors, ΔV_{CO1_ESR} and ΔV_{CO2_ESR} are 180° phase-shifted to each other. Consequently, the sum of voltage ripple from the ESR of output capacitors is a non-zero shape as shown. It can be concluded that part of the output voltage ripple are contributed by the voltage across the ESR of the output capacitor. On the other hand, the output voltage ripple caused by the ESR can be cancelled by each other in DB-TTVD as shown in Fig. 2-22(b). As a result, the output voltage ripple is near zero due to its built-in voltage cancellation mechanism.

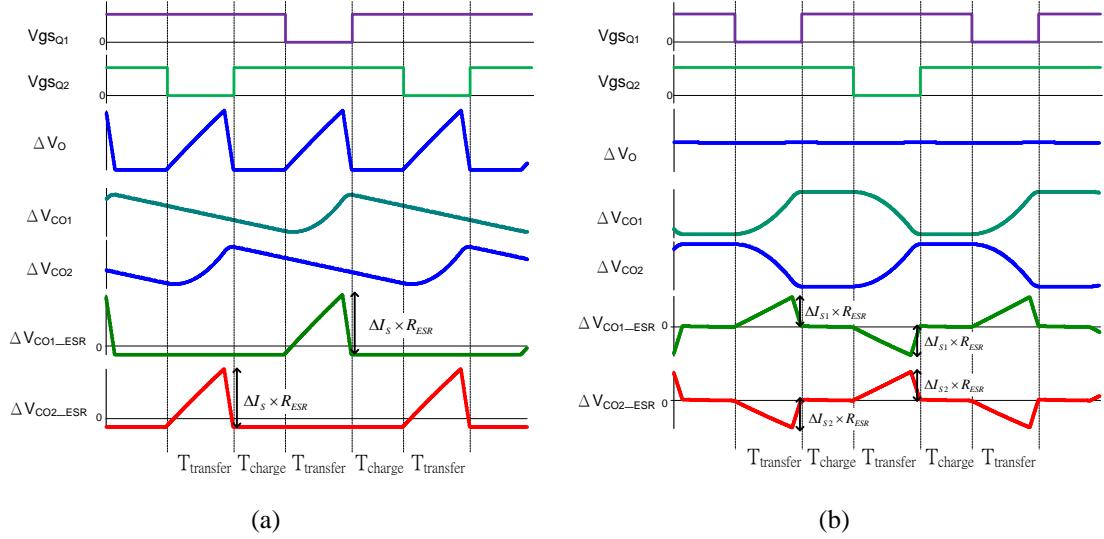


Fig. 2-22. Output voltage ripple comparison between (a) DB-CVD and (b) DB-TTVD.

The output voltage ripple of DB-CVD and DB-TTVD are calculated as follows.

$$\text{DB-CVD} \quad \Delta V_O = \left| \frac{I_O}{C_O} \times (2D-1) \right| T_s \quad (2-26)$$

$$\text{DB-TTVD} \quad \Delta V_O = \left| \frac{1}{C_O} \left(\frac{L_{k_2} - L_{k_1}}{L_{k_1} + L_{k_2}} \right) \cdot \frac{\Delta I_P}{N} \cdot (1-D) T_s \right| \quad (2-27)$$

The smallest output voltage ripple can be achieved when the $L_{k1}=L_{k2}$ condition is met. Therefore, smaller output capacitance can be designed to meet the voltage ripple specification in DB-TTVD. Moreover, it also has reduced current ripple leading to decreasing capacitor equivalent series resistance (ESR) power dissipations. Consequently, the number of the output capacitors can be minimized greatly. These two features make the non-electrolytic capacitor can be used to replace the aluminum electrolytic capacitors and the converter reliability is much upgraded.

2.5 Hardware implementation

The design procedures of DB-TTVD with 100 kHz, 24~36V input range and 380V/1A output are described in this section. The selections of several key components such as input inductors, L_1 and L_2 , power MOSFETs, rectifier diodes, D_1 and D_2 , clamping capacitor, C_1 , output capacitors, C_{O1} and C_{O2} , and transformer parameters including leakage inductances, L_t , L_{k1} and L_{k2} , and turns-ratio, 1:n:n, are provided as follows.

Table 2-2. Specifications of DB-TTVD.

	DB-TTVD
Input Voltage, V_{in}	24~36 V
Output Voltage, V_o	380 V
Maximum Load Current, $I_{o, \max}$	1 A
Maximum Load Power, $P_{o, \max}$	380 W
Switching frequency, f_s	100 kHz

2.5.1 Turns-ratio of transformer (N) and duty cycle (D)

The voltage gain is limited in the current-fed converters due to the input inductor ohmic losses. The transfer function can be derived as:

$$\frac{V_o}{V_{in}} = \frac{2N}{(1-D)} \cdot \frac{1}{1 + \frac{2N^2}{(1-D)^2} \cdot \frac{r_f}{R_o}} \quad (2-28)$$

where r_f is the ESR of the input inductor.

The gain curve with different duty cycle and ESR of the input inductor is illustrated as Fig. 2-23.

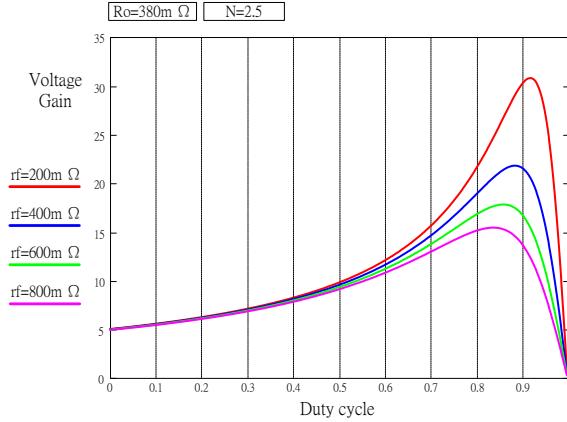


Fig. 2-23. Voltage gain of DB-TTVD with different duty cycle and input inductor ESR.

As shown in Fig. 2-23, the duty cycle maximum is near 0.85 in the proposed circuit. According to the specifications as shown in Table 2-2, the maximum voltage gain is calculated to be 15.833 ($V_O/V_{in,min}=380V/24V$) at low-line operating condition. On the other hand, the minimum gain is equal to 10.556 ($V_O/V_{in,max}=380V/36V$) at the high-line operating condition. As shown in Fig. 2-24(a), the voltage gain is illustrated with four different turns-ratio of transformer. The higher turns-ratio has lower duty cycle operating point and wide operating range. However, the duty cycle determines the voltage rating of switching MOSFETs as illustrated in Fig. 2-24(b). The voltage stress on switches is increase as following duty cycle increase. The higher voltage rating results in higher turn-on resistance of MOSFETs. In general, the boost converter best efficiency can be achieved with 50% duty cycle operating condition. However, the turns-ratio of transformer increase as following duty cycle decrease. Moreover, the leakage inductor plays an important role in the proposed circuit. To reduce the parasitic inductance and conform to the criteria, the interleaving construction is preferred. Therefore, the turns-ratio of the transformer is set to 1:2:2 ($n=2$) and the maximum of duty cycle is set to 80% for better switching MOSFETs selection.

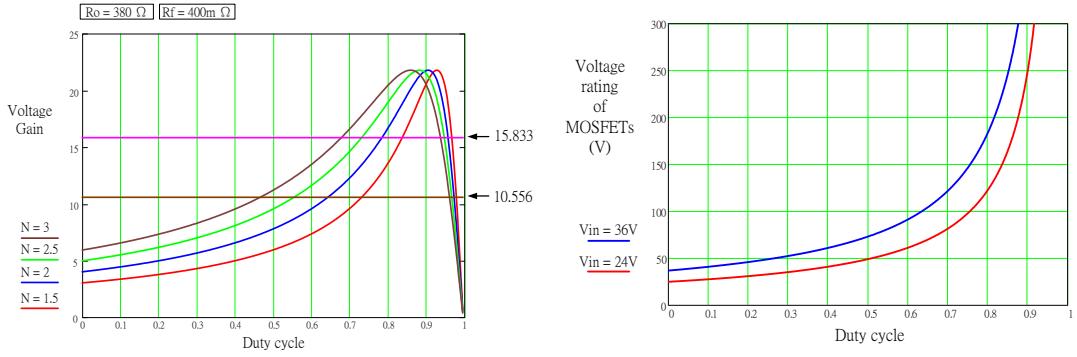


Fig. 2-24. (a)Voltage gain of DB-TTVD with different turns-ratio N and (b)voltage rating of MOSFETs with different various duty cycle operating conditions

2.5.2 Leakage inductance (L_r) for ZVS operation

The leakage inductor of transformer primary side determines the ZVS operation of main switches. The leakage inductor has to provide sufficiently large energy to discharge the parasitic capacitor of main switches Q_1 and Q_2 . The minimum leakage inductance is calculated as follows.



$$L_r \cdot I_{L_{rpeak}}^2 \gg Coss_{Q_1} \cdot V_{DS_{Q_1}}^2 \quad (2-29)$$

During main switch turned-off, the energy transfers to secondary side via transformer. The voltage across transformer primary winding has voltage drop due to leakage inductor of transformer. Thus, the leakage inductor will influence on the voltage gain of converter. The voltage and current waveforms of leakage inductor are shown in Fig. 2-25. The reset time of leakage inductor, $D_r T_s$, is calculated by applying the volt-second balance of leakage inductor as shown in Eq. (2-30) and Eq. (2-31).

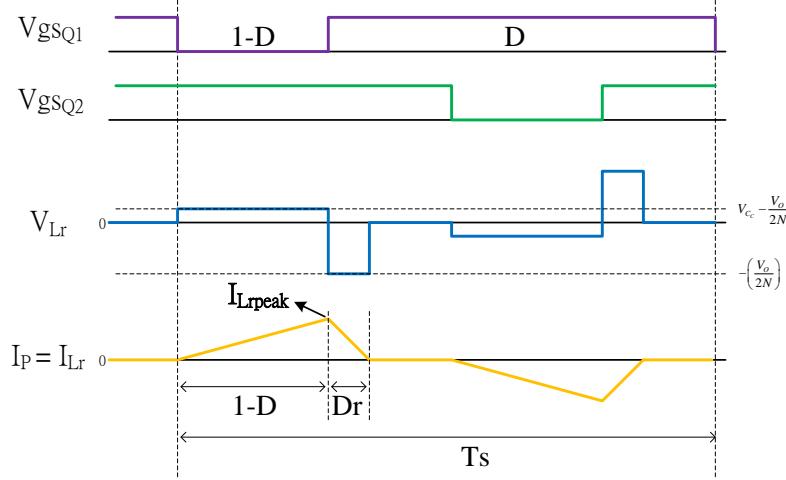


Fig. 2-25. Current waveform of transformer primary winding.

$$\left(V_{cc} - \frac{V_o}{2N} \right) \cdot (1 - D) T_s = \frac{V_o}{2N} \cdot D_r T_s \quad (2-30)$$

$$D_r = \frac{2N}{V_o} \cdot V_{cc} - (1 - D) \quad (2-31)$$

The average current of transformer primary winding is equal to that of the load current reflected to primary side. Therefore, the voltage gain is derived as shown in Eq. (2-34).

$$\frac{I_{L_{peak}} \cdot ((1 - D) + D_r) T_s}{2} \cdot \frac{1}{T_s} \cdot \frac{1}{N} = I_o = \frac{V_o}{R_o} \quad (2-32)$$

$$I_{L_{peak}} = \frac{V_{cc} - \frac{V_o}{2N}}{L_r} \cdot (1 - D) T_s \quad (2-33)$$

$$\frac{V_o}{V_{in}} = \sqrt{\left[\frac{R_o \cdot T_s}{L_r} \cdot \left(\frac{1 - D}{4N} \right) \right]^2 + \frac{R_o \cdot T_s}{L_r} - \frac{R_o \cdot T_s}{L_r} \cdot \frac{(1 - D)}{4N}} \quad (2-34)$$

The voltage gain ratio with different leakage inductance under full load condition is shown in Fig. 2-26. The maximum voltage gain requirement is given under

low-line operating condition ($V_O/V_{in}=15.833$). As shown, the maximum duty cycle operating point is increased as the leakage inductance increases. Large leakage inductance makes main switches easier to achieve zero voltage turned-on. However, referring to Fig. 2-24(b), the higher voltage rating of MOSFETs is required resulting in more conduction loss. Finally, the leakage inductance is set to $2.5\mu H$. For more convenient hardware components design consideration, an additional inductor is series-connected with leakage inductor of transformer primary side to get the required equivalent inductance.

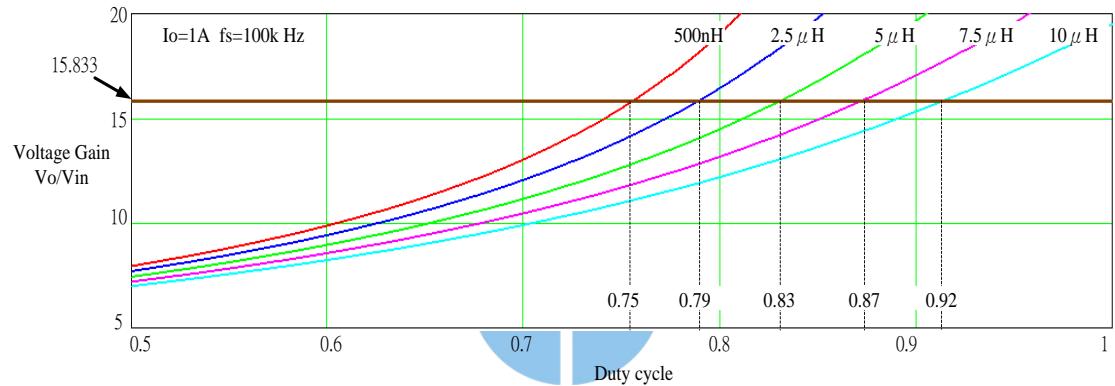


Fig. 2-26. Voltage gain of DB-TTVD with different leakage inductance.

2.5.3 Clamping capacitor (C_C) for ZVS operation

For zero voltage turned-on of the main switches, the value of clamping capacitor, C_C , depends on the clamping switch on-time duration at high line such that one-half of the resonant period is larger than the $[t_2-t_3]$ or $[t_7-t_8]$ time interval.

Since the leakage inductance is defined, the clamping capacitor is calculated as follows.

$$\pi\sqrt{L_r \cdot C_C} \geq (1 - D_{min})T_s \quad (2-35)$$

$$C_C \geq \frac{(1-D_{\min})^2}{f_s^2 \pi^2 L_r} \quad (2-36)$$

Thus, the clamping capacitor, C_C , is set to $8.2\mu F$.

2.5.4 Input inductors (L_1 and L_2)

The proposed circuit operated in the CCM mode. Therefore, the average current of the input current and the current ripple of the input inductor should satisfy the following equation.

$$I_{L_{1,2,\text{avg}}} > \frac{\Delta I_{L_{1,2}}}{2} \quad (2-37)$$

The minimum inductance is calculated under high-line ($V_{in}=36V$) and light load ($I_o=0.1A$) operating condition as:



$$L_{1,2} > \frac{V_{in}}{I_{in}} \cdot D \cdot T_s = 190.7 \mu H \quad (2-38)$$

Besides, the input current ripple can be calculated as:

$$\Delta I_{in} = \frac{V_{in}}{L_1} \cdot D \cdot T_s - \frac{V_{in}}{L_2} \cdot (1-D) \cdot T_s \quad (2-39)$$

Finally, the inductance value of input inductors L_1 and L_2 are set to $320\mu H$ and $315\mu H$, respectively.

2.5.5 Output capacitors (C_{o1} and C_{o2})

The designs of the output capacitors are depend on the output voltage ripple

cancellation. Reference to Section 2.3, the smallest output voltage ripple occurs under same current ripple of the transformer secondary windings and same output capacitor device conditions. As the Section 2.3 mention before, the leakage inductance plays a key role in proposed circuit. The leakage inductance has designed identically by the interleaved transformer layer arrangement. For the purpose of conformity to the same ESR condition, the output capacitors capacitance is selected to identically.

In addition, the average voltage across output capacitors is half of the output voltage. During the T_{transfer} time interval, output capacitance is designed to avoid voltage discharge down to zero. Thus the minimum capacitance is calculated as:

$$C_{o_{\min}} > \frac{\Delta I_p}{2 \cdot N \cdot V_o} \cdot (1 - D) \cdot T_s \quad (2-40)$$



Due to the output voltage cancellation mechanism, the small capacitance of output capacitors can be applied. Such as polypropylene film capacitor can be used to handle the voltage ripple. As a result, the output capacitors are used $1\mu\text{F}$.

2.5.6 Clamping capacitor (C_1)

During both main switches turned off time interval as shown in Fig. 2-27(a), the output load is supplied by clamping capacitor, leakage inductors of transformer secondary side and output capacitors. The equivalent circuit of secondary rectifier during this time interval is illustrated as Fig. 2-27(b). As shown, the output load is considered as a constant current, I_o . In addition, L_{eq} is the sum of leakage inductance and C_{eq} is equal to two series-connected output capacitors, respectively.

The equivalent circuit during this time interval becomes a CLC resonant network to supply the load demand.

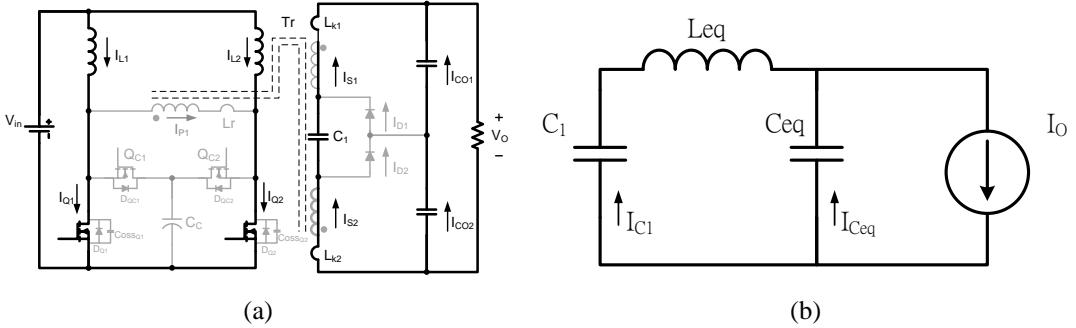


Fig. 2-27. (a) Operating stage of DB-TTVD during both main switches turned on and (b) the secondary side equivalent circuit diagram.

The resonant current of clamping capacitor, \$I_{C1}\$, and resonant frequency is calculated as follows.

$$I_{C_1}(t) = I_o \cdot \frac{C_1}{C_1 + C_{eq}} + (I_{C_1}(t_0) - I_o) \cos(\omega_0 \cdot t) + \frac{V_{C_1}(t_0) - V_{C_2}(t_0)}{Z_0} \sin(\omega_0 \cdot t) \quad (2-41)$$

$$Leq = L_{k_1} + L_{k_2} \quad (2-42)$$

$$C_{eq} = \frac{C_{o_1} \cdot C_{o_2}}{C_{o_1} + C_{o_2}} \quad (2-43)$$

$$\omega_0 = \frac{1}{\sqrt{L_{eq} \cdot \frac{C_1 \cdot C_{eq}}{C_1 + C_{eq}}}} \quad (2-44)$$

$$f_0 = \frac{1}{2\pi \sqrt{L_{eq} \cdot \frac{C_1 \cdot C_{eq}}{C_1 + C_{eq}}}} \quad (2-45)$$

$$Z_0 = \sqrt{\frac{L_{eq}}{\frac{C_1 \cdot C_{eq}}{C_1 + C_{eq}}}} \quad (2-46)$$

As a result of the small capacitance is applied in DB-TTVD, the selection of clamping capacitor and output capacitors are become a significant parameter to decide the resonant frequency. To obtain good output voltage ripple cancellation mechanism, the half of resonant period large than $[t_0-t_1]$ time duration is preferred as shown in Fig. 2-28. Otherwise, it makes output equivalent capacitor, C_{eq} , obtain additional energy power from clamping capacitor or provide extra energy power to catch up on the load demand. Consequently, it influences the output voltage ripple performance. Finally, the value of the clamping capacitor, C_1 , is set to $4.7\mu F$.

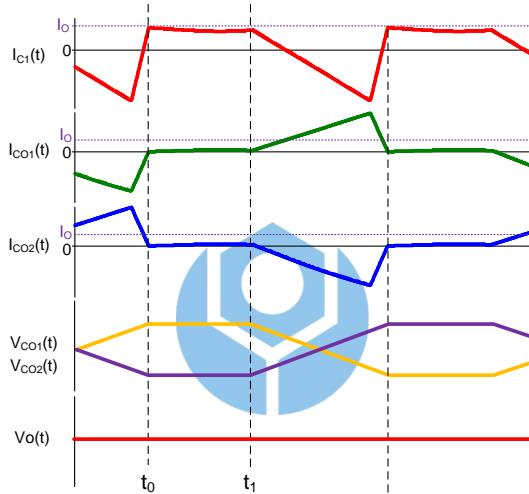


Fig. 2-28. Expected current and voltage waveforms of clamping capacitor and output capacitors.

2.5.7 Rectifier diodes (D_1 and D_2)

The selection of the rectifier diodes depend on the voltage stress, the forward voltage drop and the reverse recovery current. The maximum voltage stress of the rectifier diode occurs under one of the switches turned off and it equal to the output voltage V_O . Moreover, the lower forward voltage drops the lower conduction loss. To concern about the reverse recovery current, the Silicon Carbide Schottky diode is preferred. Accordingly, the C3D10065 is used and the specification is shown as follows.

Table 2-3. Key parameters of C3D10065.

Parameter	Value
Reverse blocking voltage, V_R	650 V
Average forward current, $I_{F(AVG)}$	10 A
Forward voltage, V_F	1.5 V
Reverse current, I_R	12 μ A

2.5.8 Switches (Q_1 , Q_2 , Q_{C1} and Q_{C2})

The selection of the switches MOSFETs depend on the voltage stress and the static Drain-to-Source On-Resistance ($R_{DS(ON)}$). The voltage stress of four switches is equal to the voltage of clamping capacitor, C_C , and shows as follows.

$$V_{C_c} = \frac{V_{in}}{1-D} \quad (2-47)$$

The maximum voltage stress of the switches occurs under low-line and full-load operating conditions which is 115V ($D_{max}=0.79$). Accordingly, the PSMN020-150W is used and its specification is shown as follows.

Table 2-4. Key parameters of PSMN020-150W.

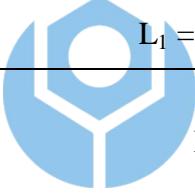
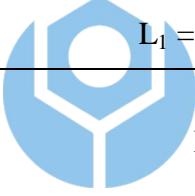
Parameter	Value
Drain-source voltage, V_{DSS}	150 V
Continuous drain current, $I_{D,max}$	73 A
Drain-source on-state resistance, $R_{DS(on)}$	20 m Ω
Output capacitance, C_{oss}	810 pF

2.6 Experiment results of DB-TTVD

To demonstrate the feasibility and highlight the advantages of the proposed rectifier, two hardware circuits (DB-TTVD and DB-CVD) operating with same

specification are both implemented and compared. The specifications and main component parameters between these two circuits are listed in Table 2-5.

Table 2-5. Specifications and main component parameters of DB-CVD and DB-TTVD.

	DB-CVD	DB-TTVD
Input Voltage, V_{in}	24~36 V	
Output Voltage, V_O	380 V	
Maximum Load Current, $I_{O, max}$	1 A	
Maximum Load Power, $P_{O, max}$	380 W	
Switching frequency, f_s	100 kHz	
Transformer	Leakage inductance $L_{k1} = 0.455 \mu H$, $L_{k2} = 0.423 \mu H$ Turns-ratio $P_1:S_1:S_2 = 1:2:2$	
Input inductor, L_1, L_2	 $L_1 = 320 \mu H$, $L_2 = 315 \mu H$	
Main Switches, Q_1, Q_2 Active clamping switches Q_{c1}, Q_{c2}	 PSMN020-150W	
Active clamping capacitor, C_c	8.2 μF	
Inductor, L_r	2.5 μH	
Rectifier diodes, D_1, D_2	C3D10065	
Clamping capacitor, C_1	N/A	4.7 $\mu F/450 V$
Output filter capacitors, C_{O1}, C_{O2}	360 $\mu F/420 V$ (3 parallel) E-cap	1 $\mu F/450 V$ PP-cap

As shown in Fig. 2-29 to Fig. 2-32, the voltage across the main switches and clamping switches Q_1, Q_2, Q_{c1} and Q_{c2} are clamped to the voltage of active clamping capacitor ($V_{in}/1-D$). All switches are turned on with ZVS operation under low-line ($V_{in}=24V$, 140W-380W) and high-line ($V_{in}=36V$, 210W-380W) operating conditions.

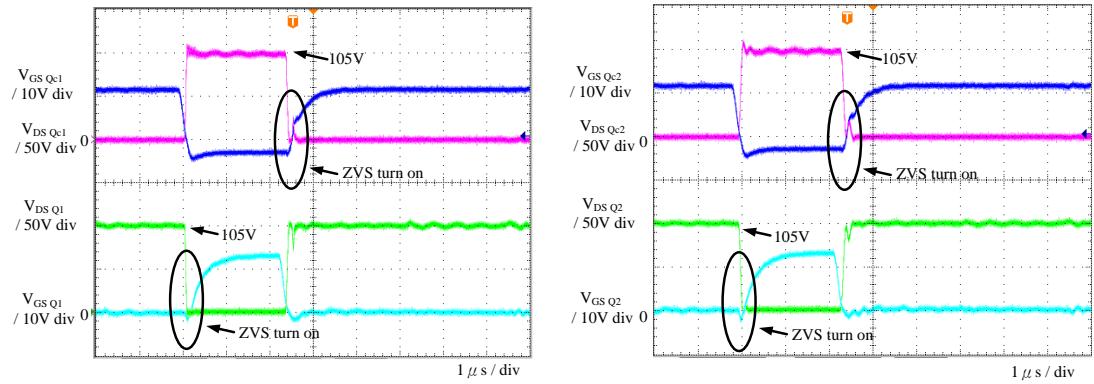


Fig. 2-29. ZVS operation waveforms of all switches under $V_{in} = 24V/140W$ operating condition.

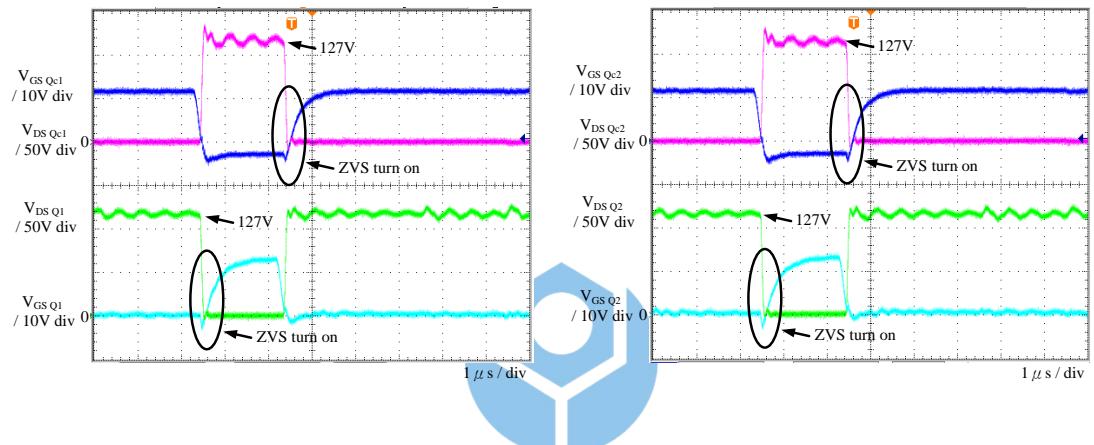


Fig. 2-30. ZVS operation waveforms of all switches under $V_{in} = 24V/380W$ operating condition.

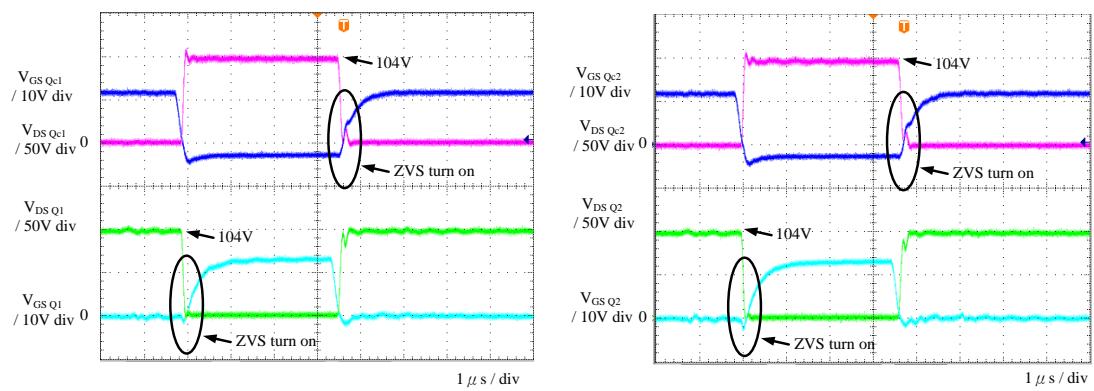


Fig. 2-31. ZVS operation waveforms of all switches under $V_{in} = 36V/210W$ operating condition.

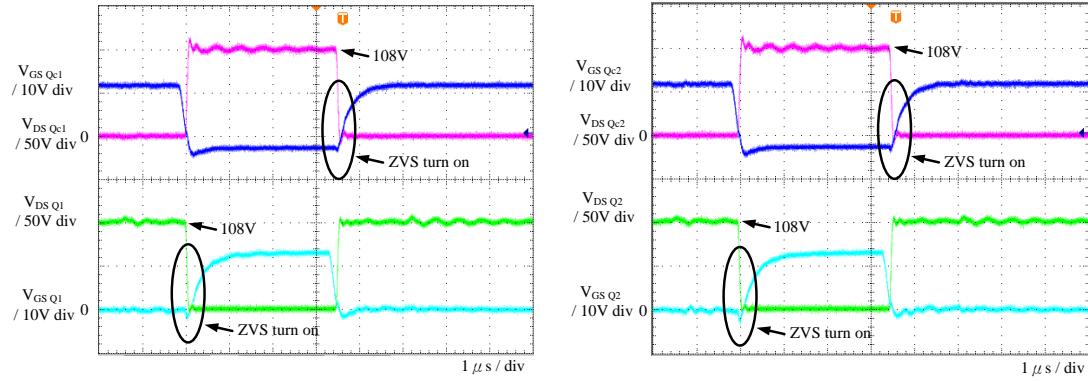


Fig. 2-32. ZVS operation waveforms of all switches under $V_{in} = 36V/380W$ operating condition.

The current waveforms of two transformer secondary windings are shown in Fig. 2-33. During both main switches turned-on time interval, the output current via transformer secondary windings and clamping capacitor to provide required energy. While one of the main switches turned-off, the current ripple is distributed to two transformer secondary windings and depended on the leakage inductance of transformer.

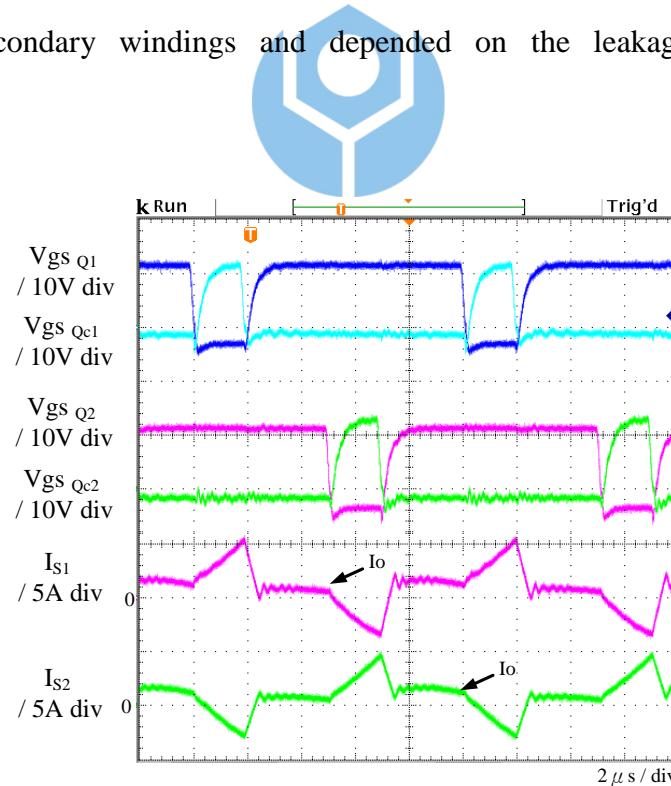


Fig. 2-33. Current waveforms of transformer secondary windings under low-line and full-load operating conditions.

As shown in Fig. 2-34(a) and Fig. 2-34(b), the voltage ripple and current waveforms of output capacitors have symmetrical and inverse waveform. During both main switches turned-on time interval, clamping capacitor provide the output power thus the current through output capacitors is nearly zero as shown.

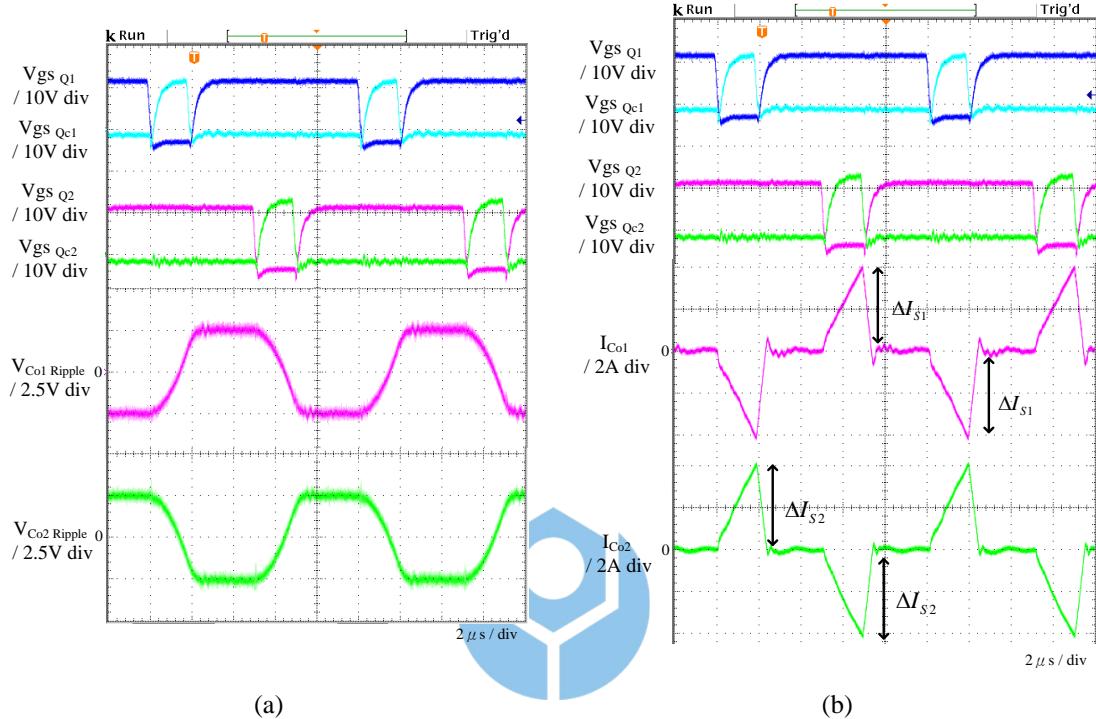


Fig. 2-34. (a)Voltage ripple waveforms and (b) current waveforms of output capacitors under low-line and full-load operating conditions.

The output voltage ripple cancellation mechanism is shown in Fig. 2-35. According to current waveform performance, the voltage ripple of two output capacitors have symmetric and inverse characteristic to minimum the output voltage ripple by applying three film capacitor ($4.7\mu F$ and $1\mu F*2$).

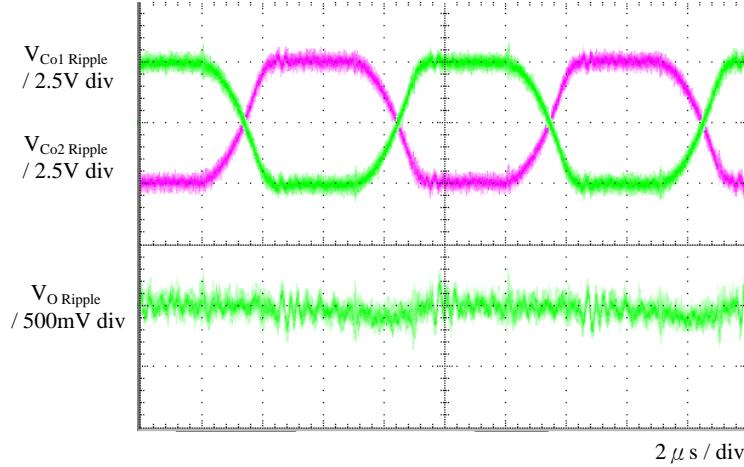


Fig. 2-35. Voltage ripple waveforms on output capacitors and output voltage under low-line and full-load operating conditions.

The measured efficiency of the presented converter with different input voltage and load conditions is shown in Fig. 2-36. A maximum efficiency, 95.17%, is obtained at high-line and 90% load conditions. Because the conduction loss is dominant of the total losses, low input voltage has lower conversion efficiency.

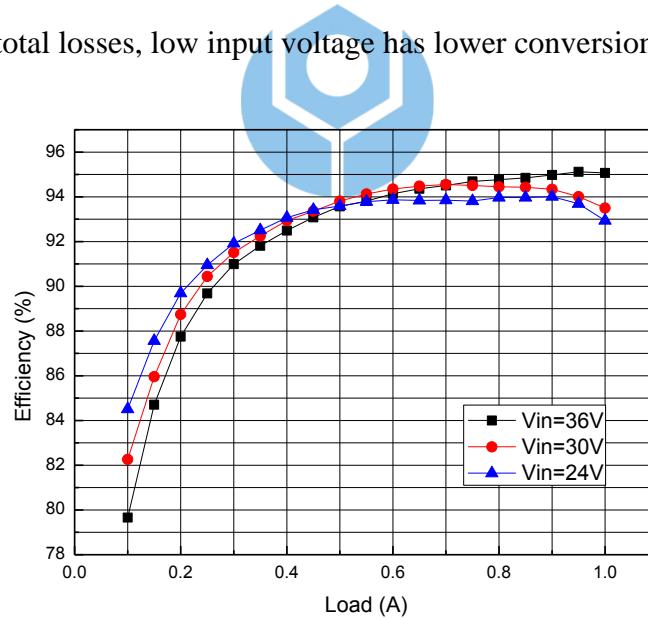


Fig. 2-36. Measured efficiency of DB-TTVD power stage.

2.7 Experiment results comparison between DB-CVD and DB-TTVD

The hardware performance comparison between DB-TTVD and DB-CVD is made under low-line ($V_{in}=24V$) and full-load (380W) operation conditions.

2.7.1 Current of transformer secondary windings

As shown in Fig. 2-37, the current of transformer secondary distribute to two windings in DB-TTVD resulting in the 33% RMS current reduction of transformer secondary winding.

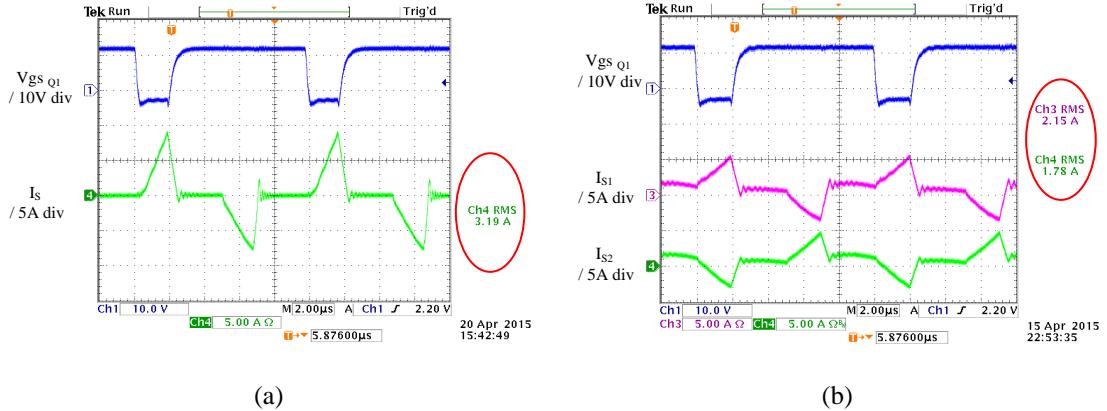


Fig. 2-37. Current waveforms of transformer secondary windings comparison between (a) DB-CVD and (b) DB-TTVD.

2.7.2 Output capacitors

As shown in Fig. 2-38, the RMS current of output capacitors is reduced. It is easy to perceive the contrast between the current ripple distribution and opposite waveforms of proposed rectifier and conventional voltage doubler rectifier.

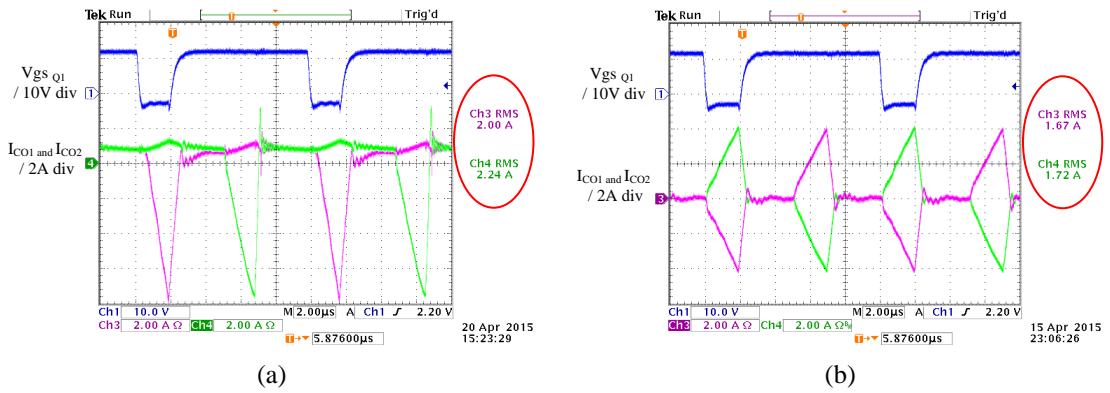


Fig. 2-38. Current waveforms of output capacitors comparison between (a) DB-CVD and (b) DB-TTVD.

Accordingly to the current waveforms, the proposed voltage doubler rectifier has better voltage ripple cancel effect than conventional voltage doubler rectifier. The voltage waveforms of output capacitors are shown in Fig. 2-39.

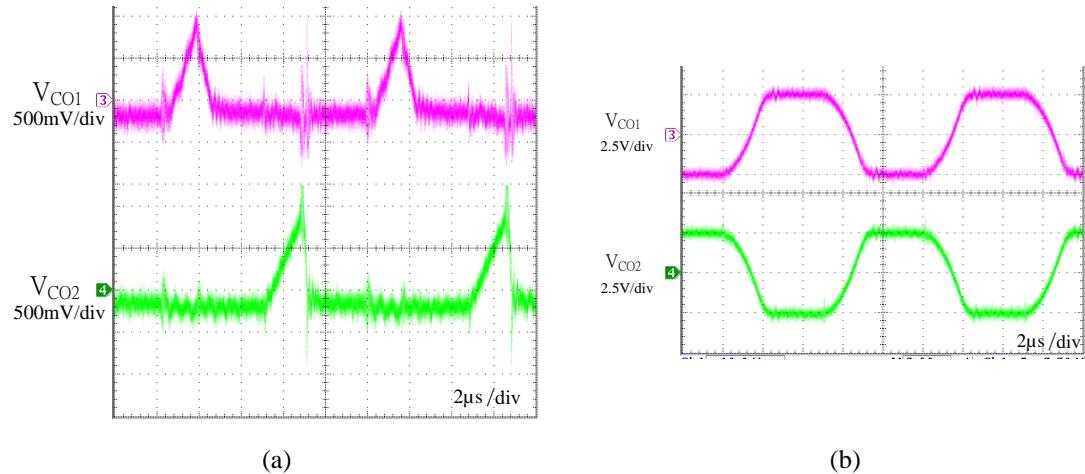


Fig. 2-39. Voltage ripple waveforms of output capacitors comparison (a)DB-CVD and (b)DB-TTVD.

Moreover, three 120 μ F/420 V aluminum electrolytic capacitors are parallel to decrease the ESR effects of capacitors of each output capacitor in the DB-CVD. On the other hand, only two 1 μ F/450V film capacitors are used in DB-TTVD. The volume of capacitors is shown in Fig. 2-40 and the ESR of output capacitors is shown in Table 2-6.

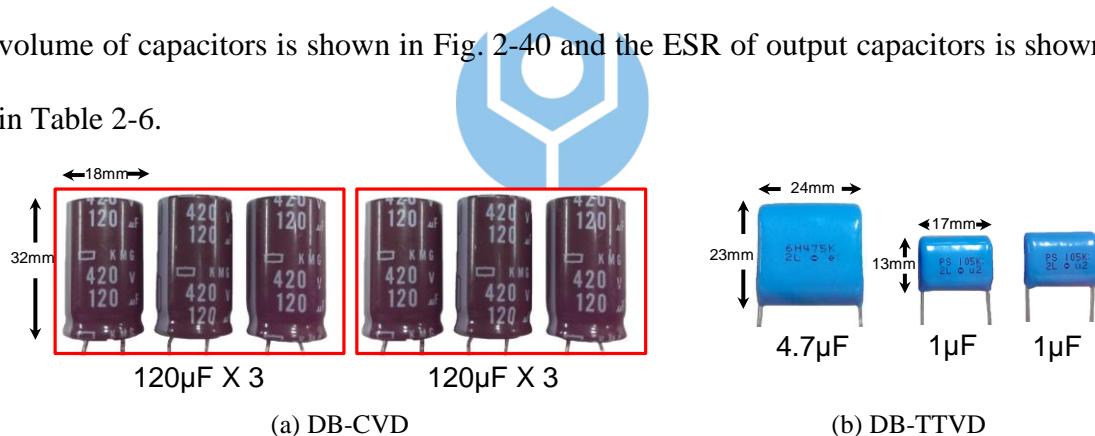


Fig. 2-40. Volume comparison of using capacitors between DB-CVD and DB-TTVD.

Table 2-6. Output capacitors specifications of DB-CVD and DB-TTVD.

	DB-CVD	DB-TTVD	
Type	Aluminum electrolytic capacitor	Polypropylene film capacitor	
Voltage rating	420V	450 V	450 V
Capacitance	120 μ F	4.7 μ F	1 μ F
R _{ESR}	388mΩ	45 mΩ	64 mΩ

2.7.3 Output voltage ripple

By using different capacitance and material of the output capacitors between DB-CVD and DB-TTVD, the voltage ripple performance comparison is made. As shown in Fig. 2-41, voltage ripple waveforms are captured. DB-CVD has to use two large capacitance of output capacitors is required to approach the proposed rectifier voltage ripple specification.

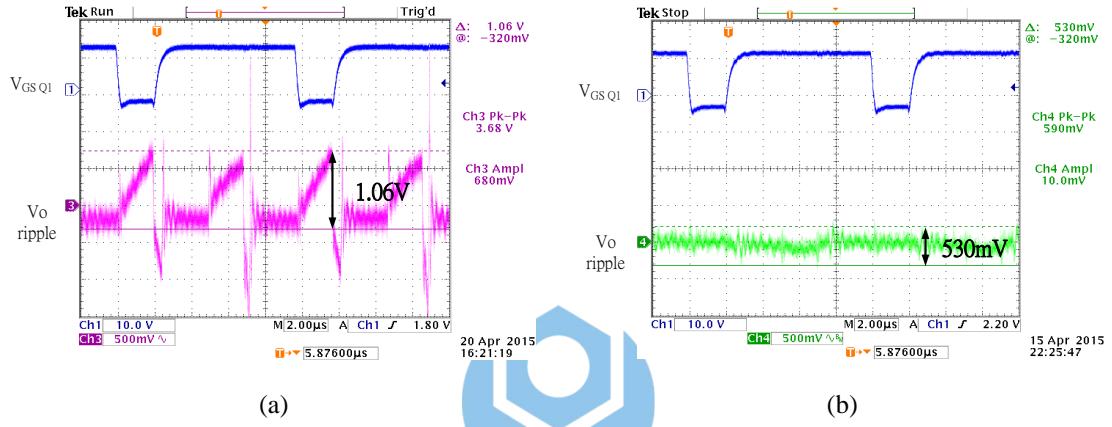


Fig. 2-41. Output voltage ripple comparison between (a) DB-CVD and (b) DB-TTVD.

2.7.4 Efficiency

Finally, the measured efficiency comparison between DB-CVD and DB-TTVD is made. As shown in Fig. 2-42, the switching loss of power devices dominates the efficiency while both converters operated in light load condition. Because no matter how output power is, the power devices suffer from high voltage stress in current-fed configuration. As load current increased the conduction loss start to dominate the efficiency. Thus, while converters operated under high-line ($V_{in}=36V$) condition have better efficiency than low-line ($V_{in}=24V$) condition. In DB-CVD, large capacitance of aluminum electrolytic capacitor is applied to deal with the output

voltage ripple. As a result, the E-cap has higher ESR of capacitors as shown in Table 2-6 and higher RMS current through output capacitors, DB-CVD has more ESR dissipation. Thus, DB-TTVD has 3.36% efficiency improvements under low-line and full-load operation conditions.

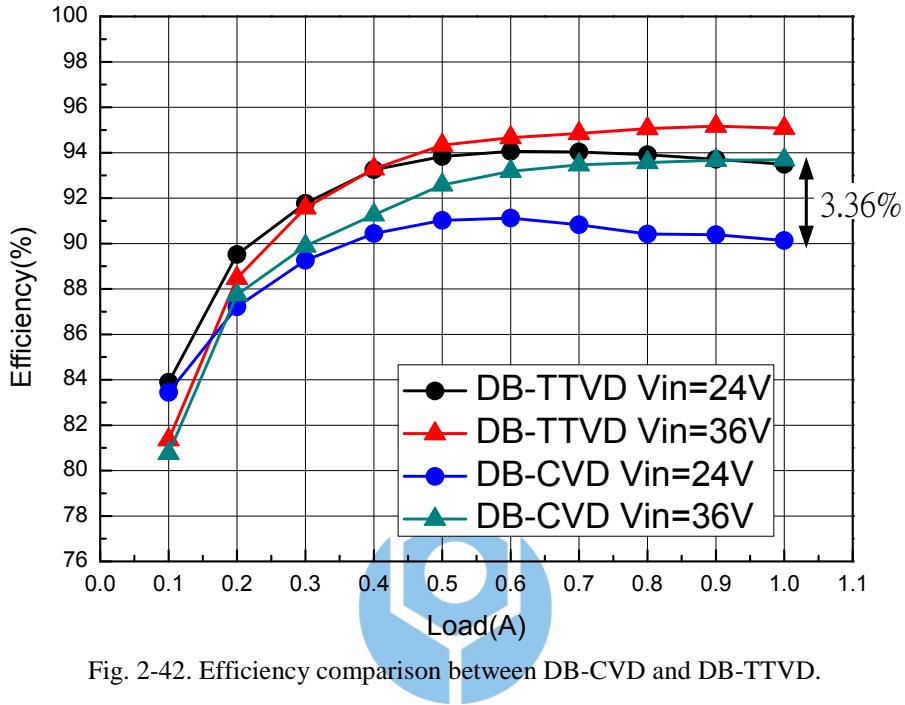


Fig. 2-42. Efficiency comparison between DB-CVD and DB-TTVD.

2.8 Summary

By applying the proposed voltage doubler rectifier to replace a current-fed power converter, a current-fed push-pull boost converter with voltage doubler rectifier (DB-TTVD) is presented in this chapter. In addition to the analysis and design, the hardware of DB-CVD and DB-TTVD are implemented and tested for comparison. By employing the voltage doubler rectifier technique, the required voltage gain, 15.833($=380V/24V$), is obtained with a smaller transformer turns-ratio 1:2:2. Therefore, the leakage inductance of the secondary windings, S_1 and S_2 , are smaller

(0.45 μ H and 0.43 μ H). Due to the help of the clamping capacitor, the leakage energies are absorbed and recycled. As a result, the secondary rectifier diodes are free of spikes and each voltage stress is clamped to output voltage (380V).

Compared with the conventional voltage doubler rectifier, the proposed circuit has less RMS value of the current and current ripple on the output capacitors, thus reduce the ESR dissipation and minimize the number of the capacitors. Furthermore, less current ripple benefits the power stage reduced EMI noise generation. Due to the output voltage ripple cancellation mechanism, the capacitance of the capacitor can be minimized. Therefore, the film capacitor can be used instead. Consequently, an increase in lifetime and reliability of the power converter can be achieved.

Therefore, higher efficiency, power density and reliability with the film capacitor can be achieved and make the proposed converter suitable for high frequency high efficiency high output voltage applications.



Chapter 3 Taiwan Tech Voltage Multiplier Rectifier

3.1 Introduction

In Chapter 2, the Taiwan Tech voltage doubler rectifier (TTVD) is proposed. In addition to having output voltage ripple cancellation mechanism to minimize the output filter capacitor, double voltage gain can be provided. However, there are many different applications where the use of higher than several thousands of volt level dc output voltage is demanded, such as X-ray systems, electron microscopes, and lasers systems, etc. [25]-[31]. Employing the proposed TTVD, consequently, the required is difficult to obtain unless a comparatively high turns-ratio of transformer has to be used instead. However, a high voltage transformer introduces large parasitic capacitance and leakage inductance. These parasitic elements lead current or voltage spikes on power devices. Moreover, the rectifier diodes and output capacitors suffer from high voltage stress resulting in increasing the conduction loss and the volume of capacitors. Thus, the efficiency and power density performance are degraded.



Referring to Fig. 1-10 and Fig. 1-11, two approaches have been proposed to alleviate the effect of parasitic elements on power converters. The first approach is series-connected multiple voltage doubler rectifier modules with a multiple secondary-winding of transformer. Although the voltage stress on the output capacitor and rectifier diode can be reduced, it complicates the construction of a high-voltage transformer. The second approach is to use a voltage multiplier rectifier on the secondary side of the transformer. It allows higher output voltages to

be created from a low voltage power source without using an expensive high voltage transformer.

Therefore, the turns-ratio of transformer and the voltage rating of rectifier diodes and capacitors can be significantly reduced. The original voltage multiplier circuit was Cockcroft-Walton half-wave voltage multiplier rectifier (CWVM) as shown in Fig. 3-1. To focus on the CWVM operation, the turns-ratio of transformer is set to 1:1. It comprises with several multiplier stages. Each multiplier stage includes one diode and one capacitor. However, the CWVM suffers from high output voltage drop and output voltage ripple for high output voltage applications [28]. To overcome these problems, a symmetrical voltage multiplier rectifier (SVM) was developed by Heilpern in 1954 by adding an additional column of capacitors and a stack of rectifiers as shown in Fig. 3-2 [29]. The voltage drop and output voltage ripple can be reduced. However, the component count is almost twice compared with CWVM. In addition to having high voltage gain with low transformer turns-ratio, low voltage stress on the rectifier diodes and minimum component counts, consequently, a voltage multiplier rectifier having low output voltage drop and output voltage ripple is preferred. However, it is not fully explored yet.

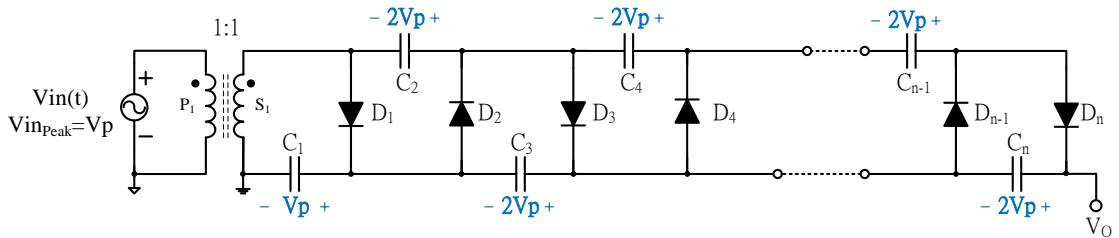


Fig. 3-1. Conventional Cockcroft-Walton voltage multiplier rectifier (CWVM).

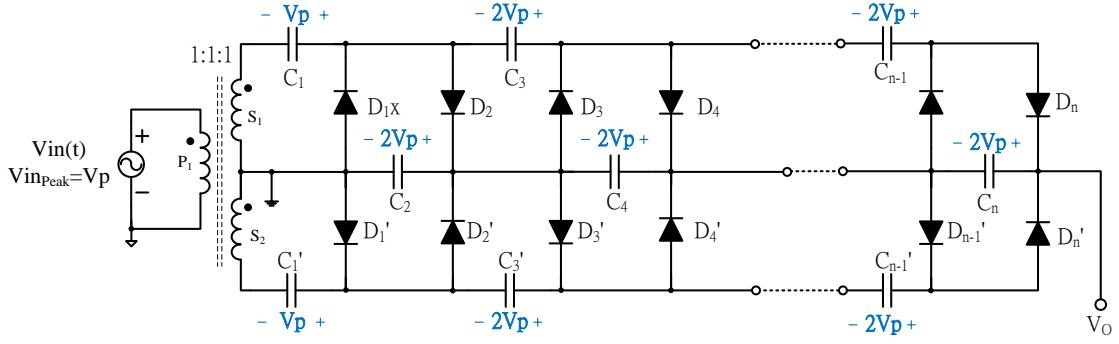


Fig. 3-2. Circuit diagram of symmetrical voltage multiplier rectifier (SVM).

A CWVM based voltage multiplier, Taiwan Tech voltage multiplier (TTVM), is thus proposed to provide a comprehensive solution for high output voltage applications.

The same concept to derive the TTVD can be applied to the evolution of the proposed TTVM. As shown in Fig. 3-3(a) is the conventional CW half-wave voltage multiplier rectifier with m -fold ($m > 2$). A modified CW half-wave voltage multiplier rectifier with n -fold ($n > 2$) can be introduced by inverting diode's polarity as illustrated in Fig. 3-3(b). The corresponding capacitor and diode, ($C_m - C_n$, $D_m - D_{n-1}$ and $D_{m-1} - D_n$) have identical operating sequence and same voltage level. Therefore, two voltage multiplier circuits can be merged via the overlap of the dotted diode-capacitor-diode cell. A novel Taiwan Tech voltage multiplier rectifier (TTVM) with multiple stages is proposed as shown in Fig. 3-4.

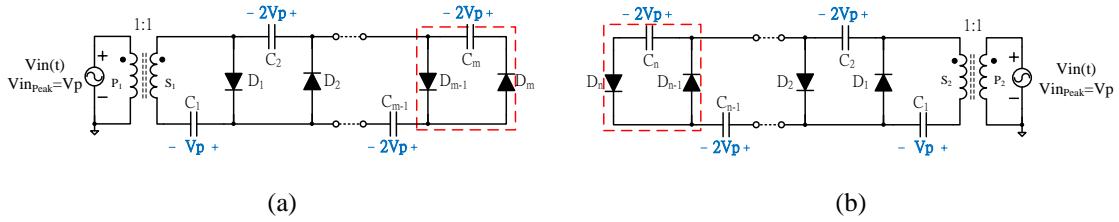


Fig. 3-3. Circuit diagrams of (a) m -fold and (b) n -fold CW half-wave voltage multiplier rectifiers.

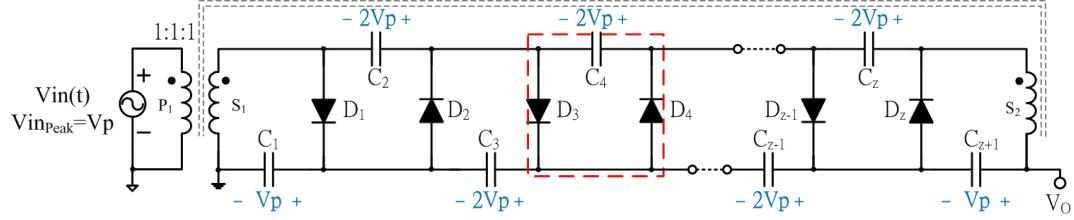


Fig. 3-4. Circuit diagram of TTVM.

To demonstrate the feasibility, a dual-inductor current-fed boost converter with six-fold TTVM (DB-TTVM-6) is presented as an example as shown in Fig. 3-5.

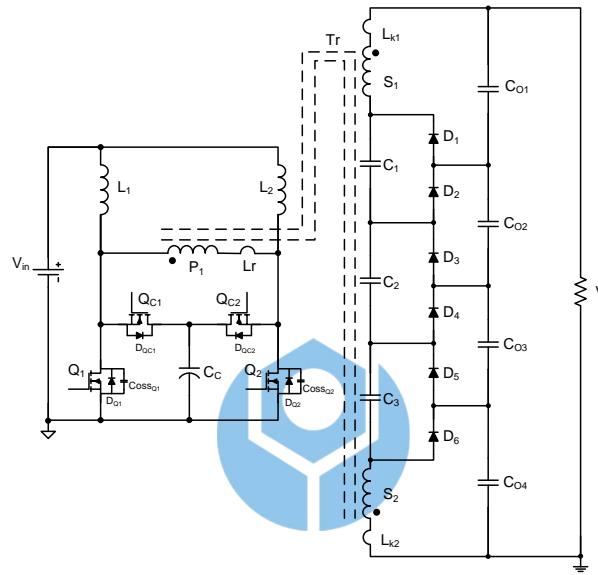


Fig. 3-5. Circuit diagram of DB-TTVM-6.

In Section 3.2, the operational analysis of the Taiwan Tech voltage multiplier is described. Also, the characteristics of TTVM will be compared with the CWVM and SVM in Sections 3.3. In Section 3.4, a six-fold TTVM is applied to a dual-inductor current-fed boost converter as an application example. Moreover, three dual-inductor current-fed boost converters with six-fold CWVM and SVM, and TTVM rectifier circuits are also implemented and compared. These hardware are implemented with 100 kHz, 24~36V input range and 380V/1A output power operating conditions. The summary of this chapter is given in Section 3.5.

3.2 Operation principle

The circuit diagram of the proposed n-stage TTVM is shown in Fig. 3-6. Each stage consists of a series diode-capacitor module. An additional filter capacitor and transformer secondary winding are connected to the last stage as shown. Therefore, it consists of two transformer secondary windings, n rectifier diodes and $n+1$ filter capacitors. Compared to the CWVM, TTVM has one additional filter capacitor, C_{n+1} , and one secondary winding, S_2 . Two half-wave rectification filter sub-circuits are formed by $S_1-D_1-C_1$ and $S_2-D_{n+1}-C_{n+1}$. Both capacitors, C_1 and C_{n+1} , are thus charged to the peak voltage across secondary winding (V_p). On the other hand, the rest $n-1$ filter capacitors are charged to twice peak voltage across secondary winding ($2V_p$). Therefore, the voltage gain of an n-stage TTVM is presented as $V_o=nV_p$.

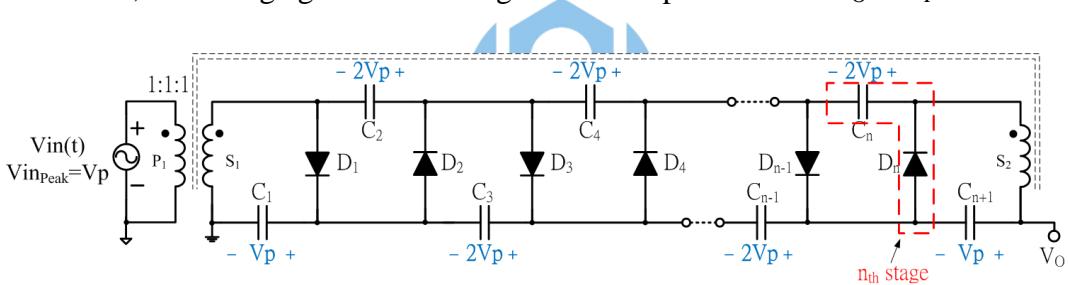


Fig. 3-6. Circuit diagram of n-fold TTVM.

Accordingly, Taiwan Tech voltage doubler rectifier is the lowest level of TTVM ($n=2$) as shown in Fig. 3-7.

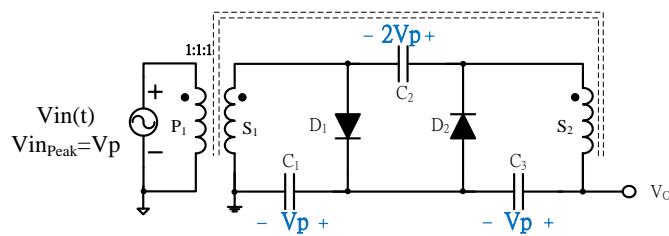


Fig. 3-7. The lowest level of TTVM ($n=2$ and $V_o=2V_p$).

Several n-stage TTVMs, such as three-fold, four-fold, five-fold, and six-fold, are

illustrated as examples and shown in Fig. 3-8 to Fig. 3-11, respectively.

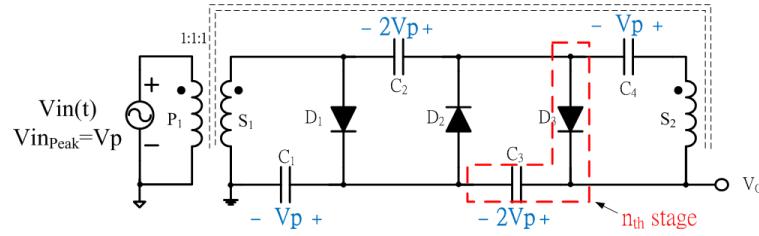


Fig. 3-8. Circuit diagram of three-fold TTVM ($n=3$ and $V_o=3V_p$).

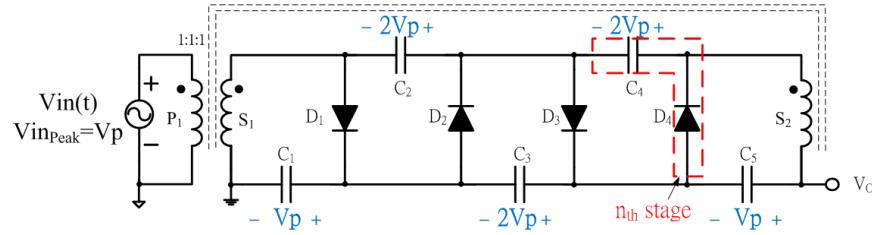


Fig. 3-9. Circuit diagram of four-fold TTVM ($n=4$ and $V_o=4V_p$).

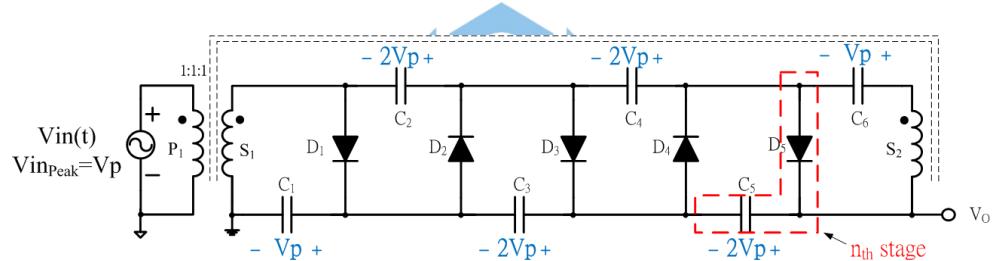


Fig. 3-10. Circuit diagram of five-fold TTVM ($n=5$ and $V_o=5V_p$).

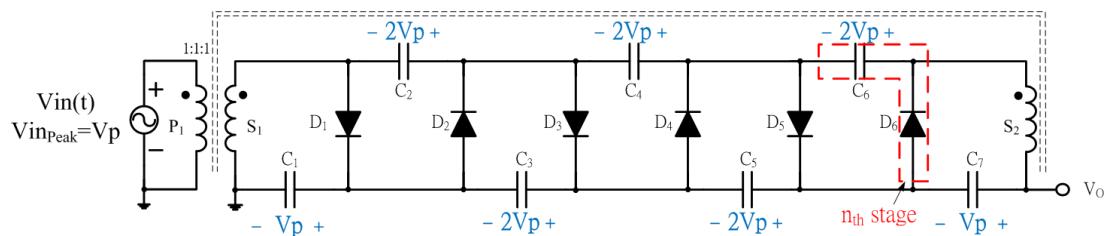


Fig. 3-11. Circuit diagram of six-fold TTVM ($n=6$ and $V_o=6V_p$).

Two converter's performances, output voltage drop and output voltage ripple, are two key issues of concern for high output voltage power conversion applications. Channel 1, Channel 2, and Channel 3 in the Fig. 3-12 are the definition of the output

voltage drop, voltage ripple, and sinusoidal power source, respectively. The output voltage is equal to the sum of voltage across each output capacitor which is nV_p under no-load operating condition. On the contrary, the voltage drop (ΔV_o) and voltage ripple (δV_o) occurs under different load current operating conditions and it will be worse as the stage increased.

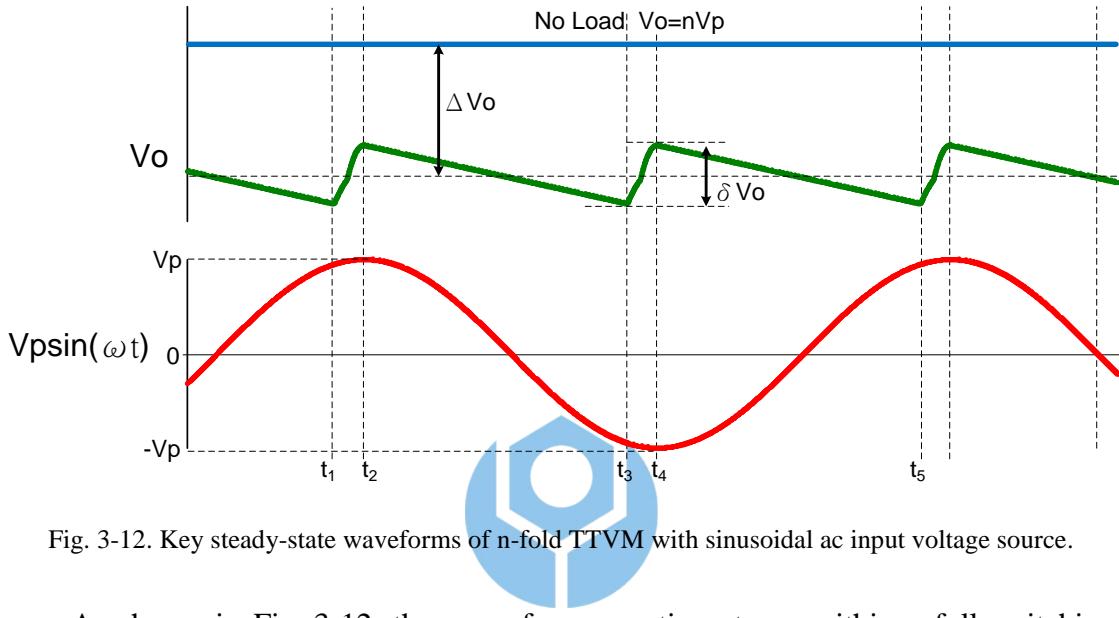


Fig. 3-12. Key steady-state waveforms of n-fold TTVM with sinusoidal ac input voltage source.

As shown in Fig. 3-12, there are four operating stages within a full switching cycle and each equivalent circuit is illustrated and described as follows.

Stage 1 [t_1-t_2]:

Before t_1 , the filter capacitors provided energy to supply load current. At t_1 , the rectifier diodes are turned on due to forwarded bias. As shown in Fig. 3-13, the filter capacitor, C_1 , is charged to the peak of input voltage due to turning-on rectifier diode, D_1 . The rectifier diode, D_3 , is conducted when the $V_{C1}+V_{C3}$ is equal to the sum of filter capacitor C_2 and input voltage ($V_{C2}+V_{in}(t)$). Therefore, the filter capacitor, C_3 , is charged by input voltage and filter capacitor, C_2 , where V_{C3} is equal to V_{C2} . On the other hand, another side of transformer secondary winding, S_2 has similar

operation. The filter capacitors, C_{n+1} and C_{n-1} , are discharged by another transformer winding, S_2 , through rectifier diodes D_{n-1} and D_{n-3} , respectively. Therefore, the same column of filter capacitors are charged and discharged simultaneously to achieve output voltage ripple reduction.

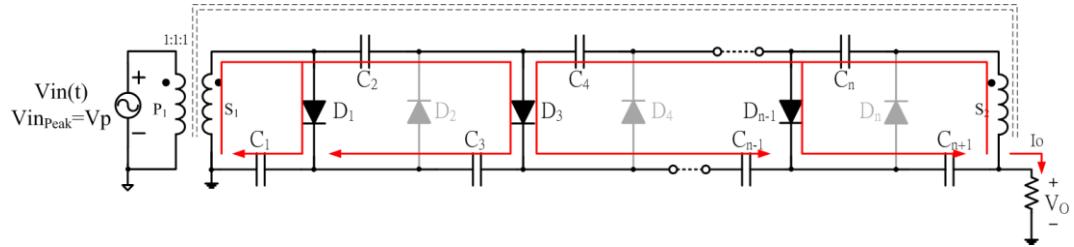


Fig. 3-13. Equivalent circuit of TTVM during charging stage $[t_1-t_2]$.

Stage 2 [t_2-t_3]:

After t_2 , the input voltage is decreased under the peak value. The voltage of filter capacitors is higher than input voltage thus the rectifier diodes are turned off without being forwarded bias as shown in Fig. 3-14. The load current is provided by filter capacitors through two series-connected capacitors loop, $S_1-C_2-C_4-\dots-C_n-S_2$ and $C_1-C_3-C_5-\dots-C_{n-1}-C_{n+1}$, respectively. Because the current through output capacitors is distributed into two loops, the output voltage ripple is reduced.

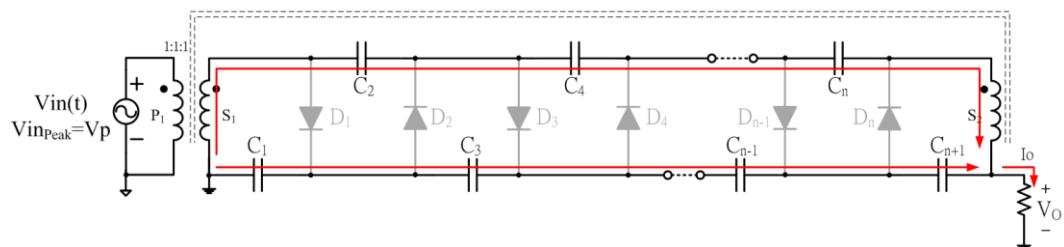


Fig. 3-14. Equivalent circuit of TTVM during discharging stage $[t_2-t_3]$.

Stage 3 [t_3-t_4]:

As shown in Fig. 3-15, the operation is similar as stage 1. The even-number rectifier diodes, $D_2, D_4, D_6, \dots, D_n$, are conducted due to being forwarded bias. Therefore, the same column of filter capacitors are charged and discharged simultaneously to achieve output voltage ripple reduction.

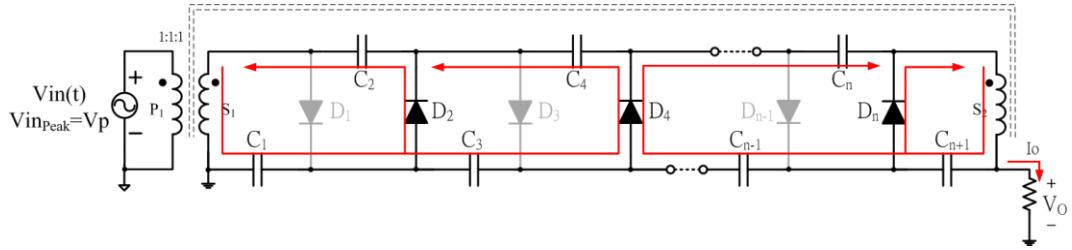


Fig. 3-15. Equivalent circuit of TTVM during charging stage [t_3-t_4].

Stage 4 [t_4-t_5]:

After t_4 , the operation that in $[t_4-t_5]$ is identical to Stage 1 [t_2-t_3]. The load current is provided by two series-connected filter capacitors. After stage 4, a completely cycle is achieved.

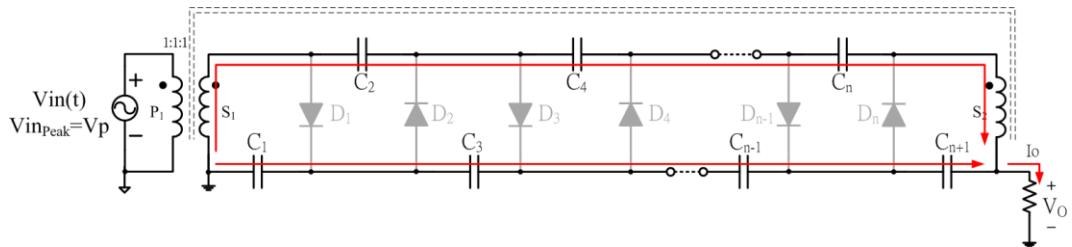


Fig. 3-16. Equivalent circuit of TTVM during charging stage [t_4-t_5].

3.2.1 Output voltage ripple

The circuit diagram of a two-fold TTVM is shown in Fig. 3-17. Instead of having output voltage ripple reduction property of a two-fold CWVM, moreover, it has output voltage ripple cancellation mechanism. Therefore, the required output

voltage ripple specification can be achieved by using small output filter capacitors.

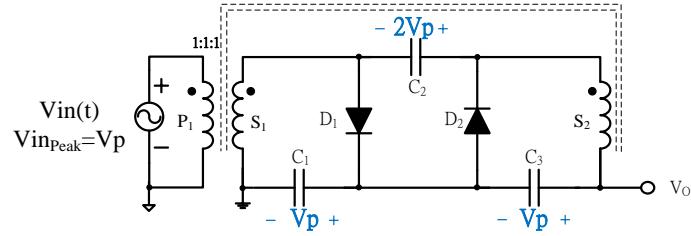
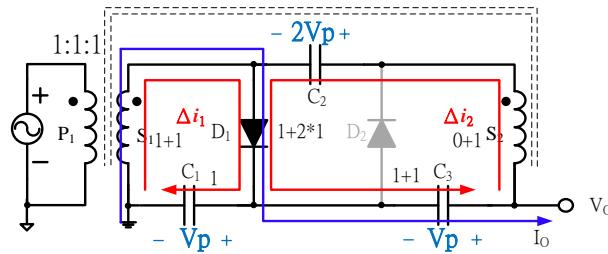


Fig. 3-17. Circuit diagram of two-fold TTVM.

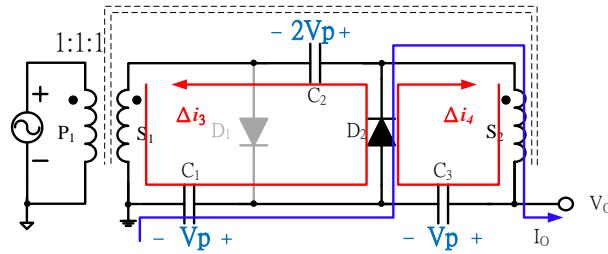
The operating equivalent circuits of a two-fold TTVM during rectifier diodes, D_1 and D_2 conducted are alternatively illustrated as shown in Fig. 3-18 (a) and Fig. 3-18 (b), respectively. As shown, the current is distributed via two transformer secondary windings to charge or discharge output capacitors, C_1 and C_3 , with same current ripple. Accordingly, the voltage ripple on capacitors, C_1 and C_3 , can be calculated as Eq. (3-1) expressed.

$$I \cdot t = C \cdot \Delta V \quad (3-1)$$

Since two output capacitors, C_1 and C_3 , are charged and discharged simultaneously by same value of current as shown in Fig. 3-19(a). Thus, the output voltage ripple can be eliminated to achieve the output voltage ripple cancellation mechanism as shown in Fig. 3-19(b).



(a)



(b)

Fig. 3-18. Circuit operation of two-fold TTVM during two charging stages (a) and (b).

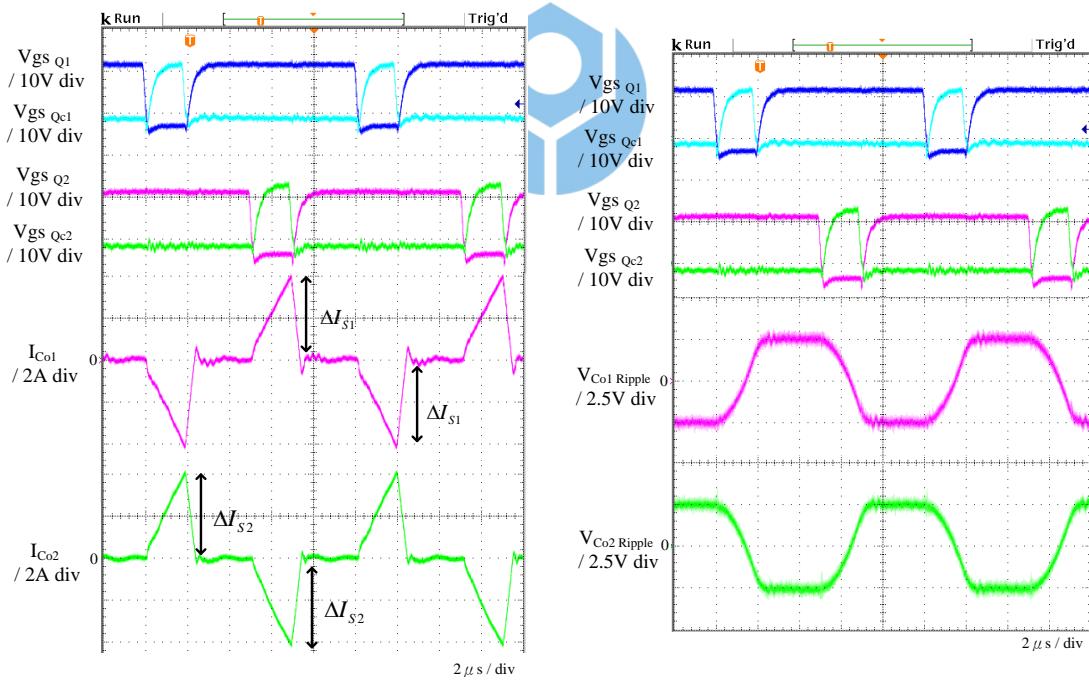


Fig. 3-19. (a) Current waveforms and (b) voltage ripple waveforms of output capacitors under low-line and full-load operating conditions.

To achieve output voltage cancellation mechanism, two operating conditions are summarized as.

1. The number of output capacitors has to be even.
2. Identical current flows through each output capacitor.

Referring to Fig. 3-8, Fig. 3-9, Fig. 3-10, and Fig. 3-11, accordingly, several multiple-stage TTVMs are investigated. Among them, three-fold, four-fold, and five-fold TTVM cannot satisfy above two operating conditions simultaneously. Instead of output voltage ripple cancellation, these are able to achieve the output voltage ripple reduction only. On the contrary, six-fold TTVM can meet the above two operating conditions, therefore, the output voltage ripple cancellation can be performed. To achieve output voltage ripple cancellation, consequently, a general rule can be applied if $(2+k*4)$ -fold TTVM is selected.



3.3 Characteristic comparison among three voltage multiplier rectifiers

Several characteristic comparisons among CWVM, SVM and TTVM are described in this section including voltage drop, voltage ripple, the voltage rating of components and component counts. The circuit diagrams of CWVM, SVM, and TTVM are shown as Fig. 3-20 to Fig. 3-22, respectively. As shown in Fig. 3-20, n-fold CWVM consists of one transformer secondary winding and n-stage series diode-capacitor modules. The voltage gain of CWVM is equal to nV_P under no-load operating condition.

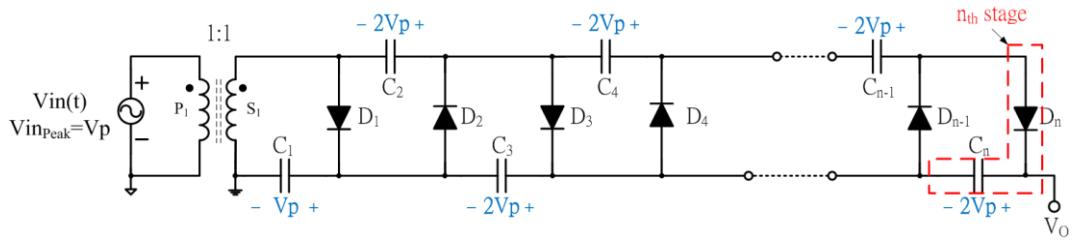


Fig. 3-20. Circuit diagram of n-fold CWVM.

The circuit diagram of n-fold SVM is shown in Fig. 3-21. It consists of two transformer secondary windings and an additional symmetrical half-wave voltage multiplier rectifier. It can be considered as two CWVM paralleled with series-connected capacitors, $C_2, C_4 \dots C_n$ in common. Therefore, the voltage ripple and voltage drop are both smaller than these of CWVM due to two transformer secondary windings operated in parallel [29]. The voltage gain is equal to nV_p where n is an even number.

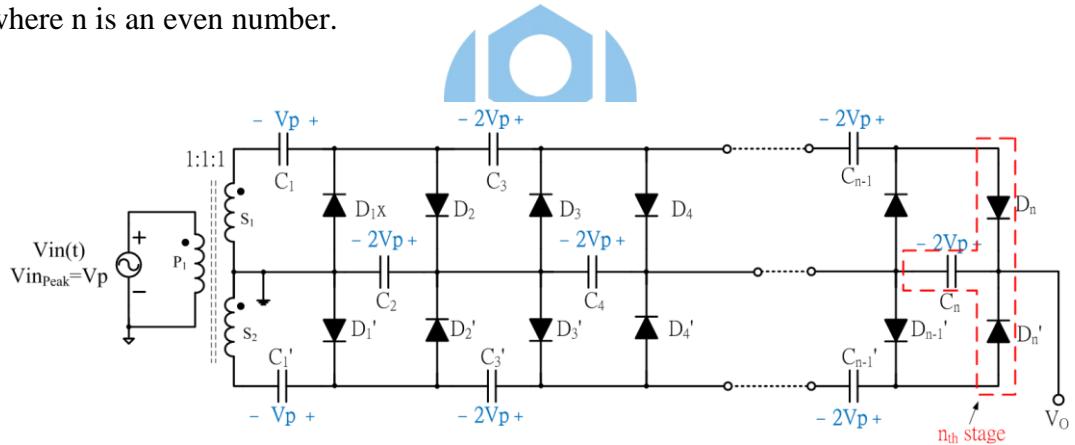


Fig. 3-21. Circuit diagram of n-fold SVM.

The circuit diagram of n-fold TTVM is illustrated as shown in Fig. 3-22. It consists of two transformer secondary windings and several n-stage series diode-capacitor modules. Compared to CWVM, it has one additional capacitor and two transformer secondary winding. It can be considered as two CWVMs operated in parallel. Therefore, the voltage ripple and voltage drop is smaller than CWVM.

The voltage gain is equal to nV_p .

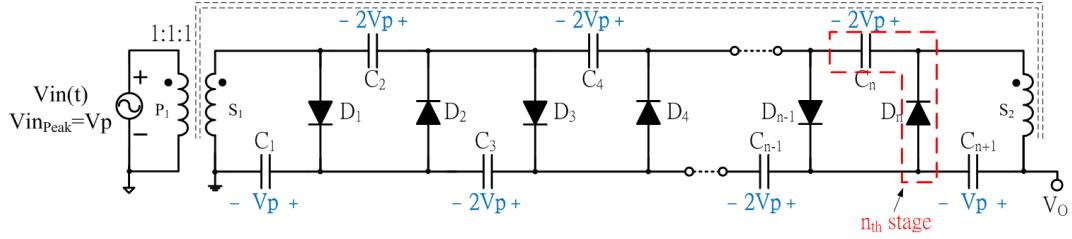


Fig. 3-22. Circuit diagram of n-fold TTVM.

The voltage drop and voltage ripple of CWVM, SVM and TTVM comparisons are made by using SIMPLIS simulation program with same operating conditions; 500V input sinusoidal voltage source with 50 kHz frequency and 0.1mA to 1mA load conditions. The filter capacitances are set to 1nF.

The voltage drop verse output load condition with multiple-stage as running parameter of CWVM and SVM are obtained as shown in Fig. 3-23(a) and Fig. 3-23(b), respectively. Compared to CWVM, SVM has smaller voltage drop due to having two transformer secondary windings operated in parallel.

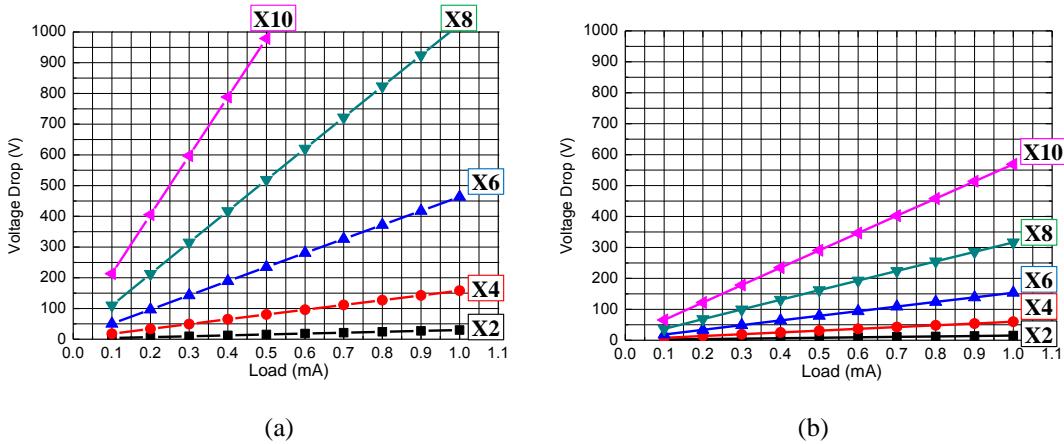


Fig. 3-23. Vltage drop comparison between (a) CWVM and (b) SVM.

Moreover, the voltage ripple verse output load condition with multiple-stage as running parameter of CWVM and SVM are obtained and shown in Fig. 3-24(a) and

Fig. 3-24(b), respectively. As shown, the voltage ripple is greatly reduced in SVM due to the paralleled configuration.

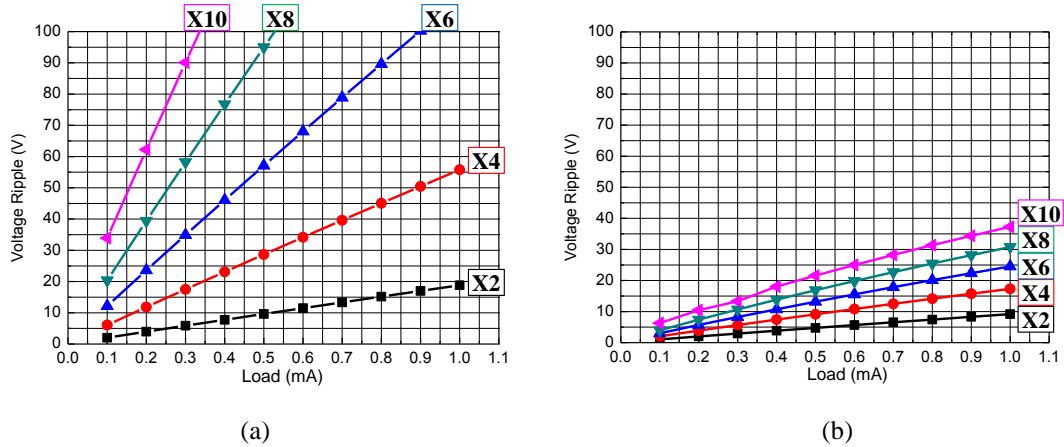


Fig. 3-24. Voltage ripple comparison between (a) CWVM and (b) SVM.

The voltage drop verse output load condition with multiple-stage as running parameter of SVM and TTVM are obtained and shown in Fig. 3-25 (a) and Fig. 3-25 (b), respectively. Because both circuits have two transformer secondary windings to provide output capacitors energy, consequently, the voltage drop of SVM compared with TTVM is barely identical as shown.

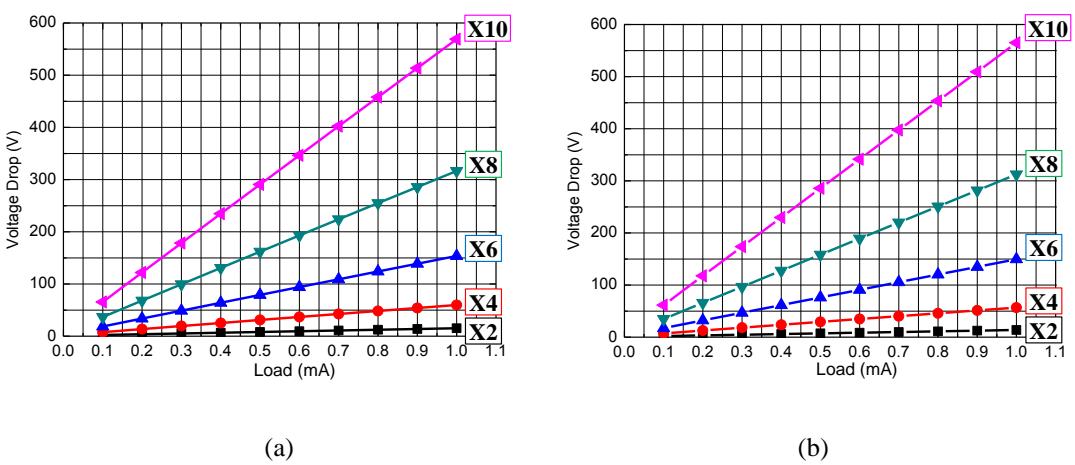


Fig. 3-25. Vltage drop comparison between (a) SVM and (b) TTVM.

The voltage ripple versus output load condition with multiple-stage as running parameter of SVM and TTVM are obtained and shown in Fig. 3-26 (a) and Fig. 3-26 (b), respectively. The proposed TTVM has output voltage ripple reduction or cancellation mechanism. As a result, the voltage ripple of TTVM is significant reduced as shown.

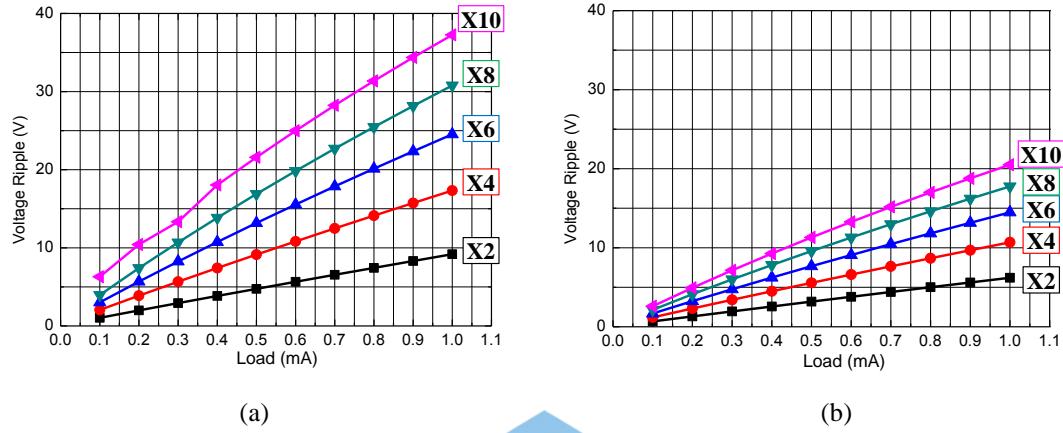


Fig. 3-26. Voltage ripple comparison between (a) SVM and (b) TTVM.

The characteristic comparisons among n-fold CWVM, SVM and TTVM are summarized and listed in Table 3-1. The parameters include voltage gain, voltage rating of components, component count, voltage drop, voltage ripple, and transformer voltage insulation requirement.

Table 3-1. Characteristic comparison with n-fold voltage multiplier rectifiers.

	CWVM	SVM	TTVM
Output voltage	nV_p		
Voltage rating of diode	$\frac{2V_o}{n}$		
Maximum voltage rating of capacitor	$\frac{2V_o}{n}$		
Voltage drop @X6, $I_o=1\text{mA}$	463.283 V	153.611 V	149.55 V
Voltage ripple @X6, $I_o=1\text{mA}$	110.832 V	24.526 V	14.476 V
Number of diode	n	2n	n
Number of capacitor	n	$\frac{3}{2}n$	n+1
Number of transformer secondary winding	1	2	2
Transformer insulation requirement	Low	Low	High

Where V_p is the peak voltage of transformer secondary winding.

*Data obtained under $V_{in}=500\text{V}$, $C=1\text{nF}$, and $V_o=3000\text{V}$ operating condition.

It can be read from Table 3-1, the same voltage rating of rectifier diodes and filter capacitors can be applied for all three circuits. The voltage drop and voltage ripple performances are improved by using two transformer secondary windings in TTVM. Compared to CWVM, an additional filter capacitor and transformer secondary winding are required in TTVM. Accordingly, it can reach same output voltage specification with more stages while voltage drop and ripple performances are maintained. As a result, a small turns-ratio transformer can be used to alleviate the side effect induced by parasitic components of high voltage transformer. However, the transformer has to provide high voltage insulation requirement because one of the

transformer secondary windings is directly connected to the high output voltage terminal.

As shown in Fig. 3-27, three six-fold voltage multiplier rectifiers, CWVM, SVM and TTVM, are simulated under start-up operating condition. The simulation is running with 50 kHz 500V sinusoidal input, 1mA load, and 1nF filter capacitances operating condition. Because SVM and TTVM used two transformer secondary windings, the output voltage can be quickly reached. As shown, TTVM is the fastest to reach steady-state output voltage within 1ms.

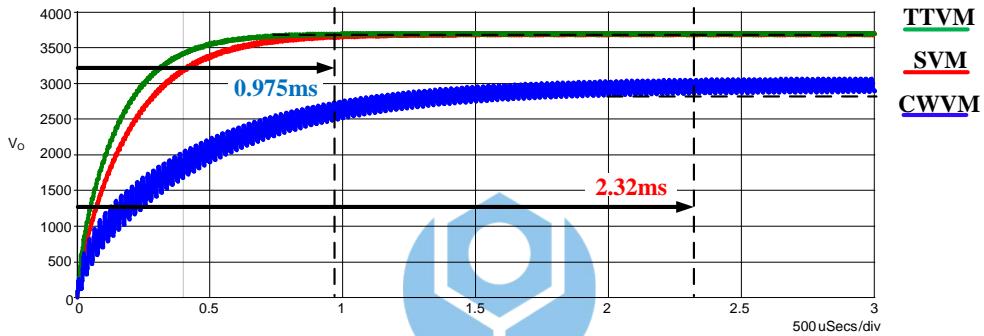


Fig. 3-27. Output voltage waveforms of TTVM and CWVM operated with start-up operating conditions.

3.4 Dual-inductor current-fed boost converter with six-fold Taiwan Tech voltage multiplier rectifier (DB-TTVM-6)

One of the design considerations for high output voltage applications is to reduce the parasitic components induced by high turns-ratio of transformer. Two major approaches are using voltage multiplier rectifier or series-connected voltage doubler modules of transformer secondary. The first approach is using Cockcroft-Walton rectifier as an example, the number of stages is restricted by the high voltage drop and output voltage ripple performance. The second approach is applied to alleviate these

values. As shown in Fig. 3-28(a) and Fig. 3-29(a), for example, three two-fold CWVM modules connected in series can respectively reduce the voltage drop and voltage ripple from 463V to 90V and 110V to 55V under 1mA load operating condition.

Compared to CWVM, the proposed TTVM has greatly reduced the voltage drop and output voltage ripple as shown in Fig. 3-28(b) and Fig. 3-29(b), respectively. For example, six-fold TTVM has 150V voltage drop and 15V voltage ripple under 1mA load operating condition. With simply transformer construction, the six-fold TTVM is recommended to be an alternative solution.

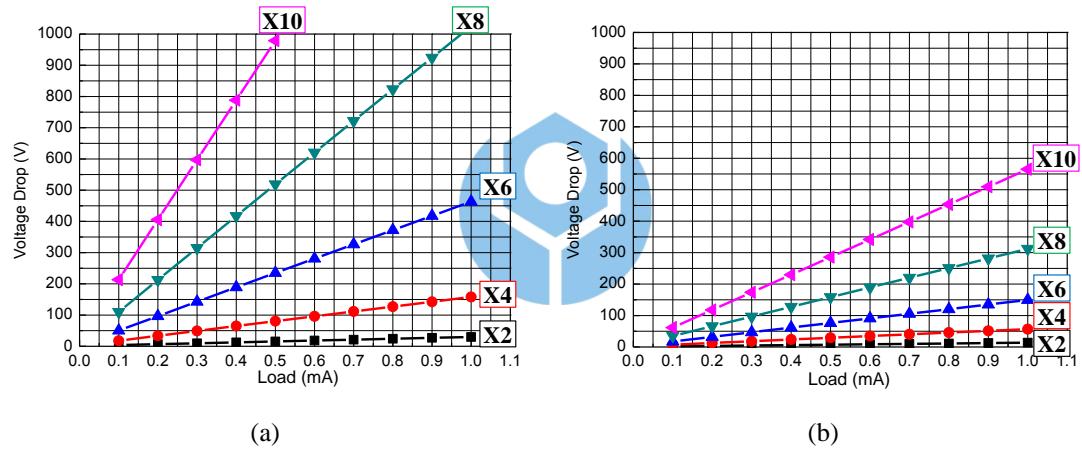


Fig. 3-28. Output voltage ripple comparison between (a) CWVM and (b) TTVM.

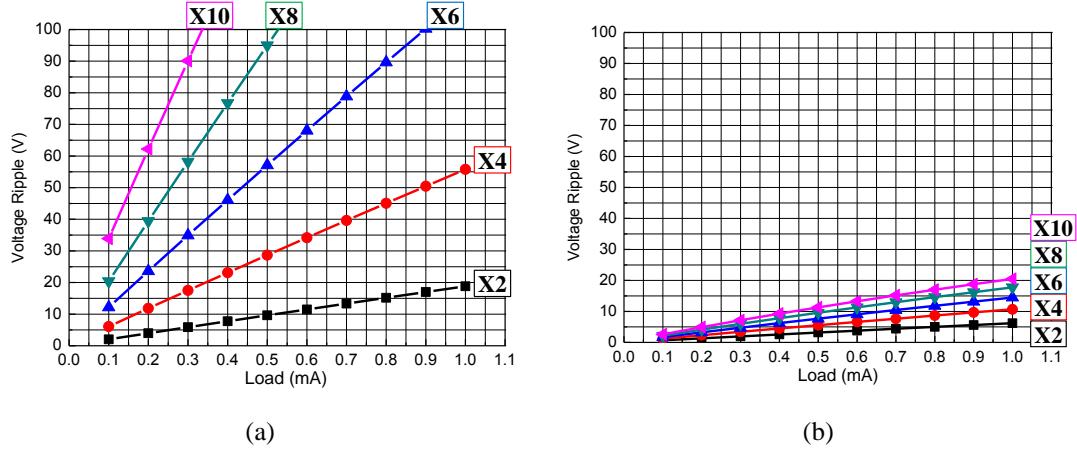


Fig. 3-29. Voltage drop comparison between (a) CWVM and (b) TTVM.

To demonstrate the feasibility, three dual-inductor current-fed boost converters with different six-fold voltage multiplier rectifiers (CWVM, SVM, and TTVM) are implemented and compared. The circuit diagrams of three converters are illustrated as shown from Fig. 3-30 to Fig. 3-32, respectively. As shown in Fig. 3-30, a dual-inductor current-fed boost converter with six-fold Cockcroft-Walton voltage multiplier rectifier (DB-CWVM-6) is presented. The converter consists of six rectifier diodes, six filter capacitors and dual-inductor current-fed boost configuration with active clamp circuit.

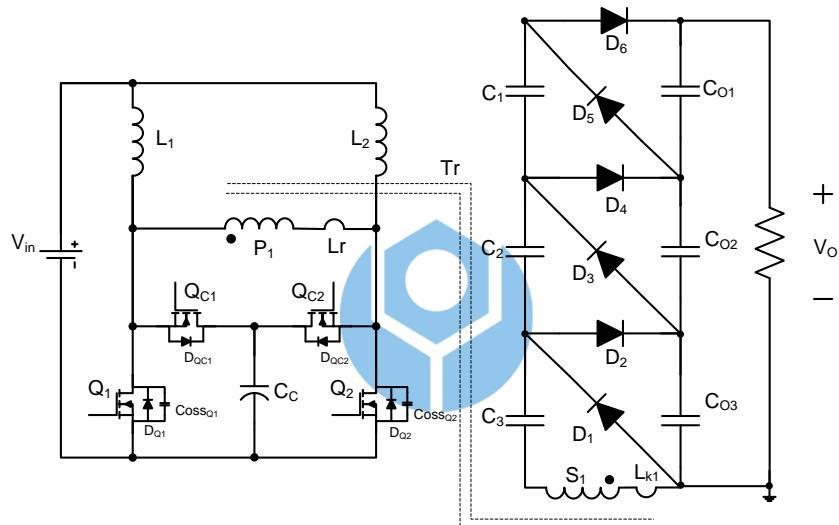


Fig. 3-30. Circuit diagram of DB-CWVM-6.

As shown in Fig. 3-31, a dual-inductor current-fed boost converter with six-fold symmetrical Cockcroft-Walton voltage multiplier rectifier (DB-SVM-6) is presented. The converter consists of two transformer secondary windings and approximately twice component counts of rectifier compared to the DB-CWVM-6.

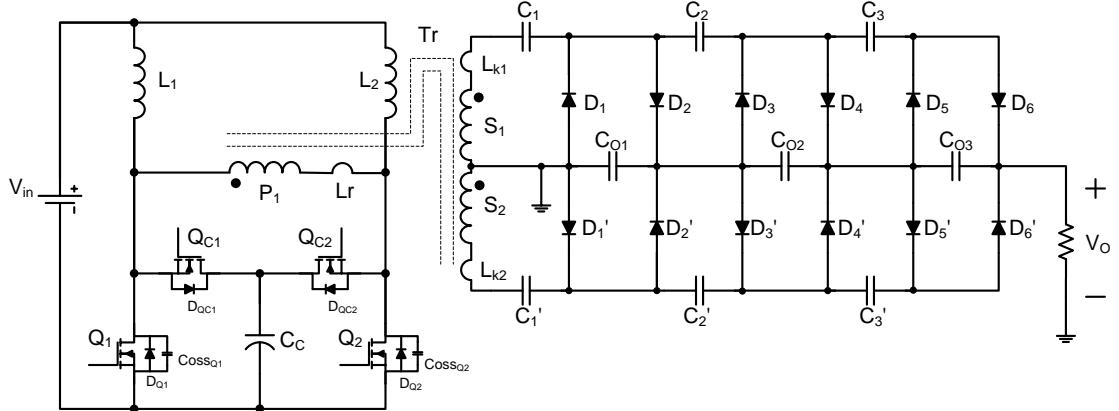


Fig. 3-31. Circuit diagram of DB-SVM-6.

As shown in Fig. 3-32, a dual-inductor current-fed boost converter with six-fold Taiwan Tech voltage multiplier rectifier (DB-TTVM-6) is presented. It is also required an additional transformer secondary winding. However, the secondary rectifier of DB-TTVM-6 only consists of six rectifier diodes and seven filter capacitors compared to the DB-SVM-6.

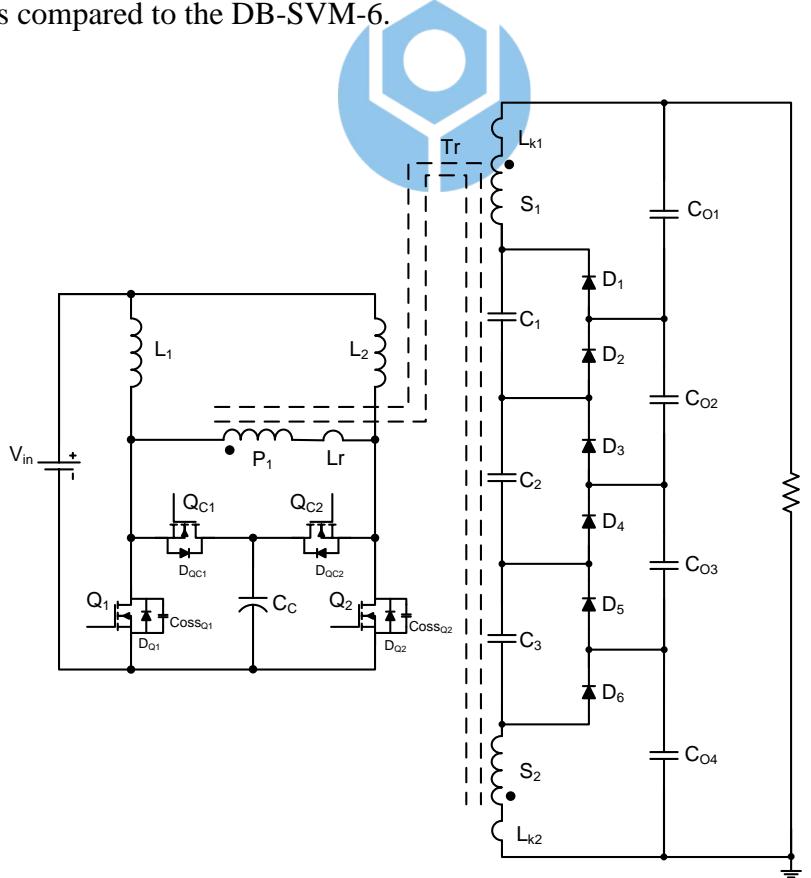
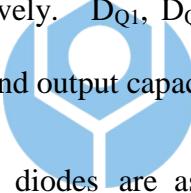


Fig. 3-32. Circuit diagram of DB-TTVM-6.

3.4.1 Operation principle

The operation principle of CWVM and SVM can be referred to the other publications [20], [29]. A dual-inductor current-fed boost converter with six-fold Taiwan Tech voltage multiplier rectifier (DB-TTVM-6) is illustrated in Fig. 3-32. It comprises two input inductors, L_1 and L_2 , one transformer, T_r , two main switches, Q_1 and Q_2 , the active clamp circuit with two clamping switches, Q_{C1} and Q_{C2} , and one clamping capacitor, C_C , the clamping capacitors, C_1 , C_2 , C_3 , four output capacitors C_{O1} , C_{O2} , C_{O3} and C_{O4} , six series-connected diodes D_1 , D_2 , D_3 , D_4 , D_5 and D_6 . The transformer consists of one primary winding P_1 and two identical secondary windings S_1 and S_2 , with the $1:n:n$ turns-ratio. L_r , L_{k1} and L_{k2} are represented as the leakage inductors of P_1 , S_1 and S_2 , respectively. D_{Q1} , D_{QC1} , D_{Q2} , D_{QC2} , $Coss_{Q1}$, and $Coss_{Q2}$ are represented as the body-diode and output capacitance of their respective switches.



To simplify the analysis, all diodes are assumed to be ideal, the clamping capacitors and output capacitors are assumed to be sufficiently large that the voltage across these capacitors is constant. Two input inductors L_1 and L_2 are assumed to be sufficiently large as two current sources. Two leakage inductances of secondary windings, L_{k1} and L_{k2} , assumed to be identical.

Although the circuit can be operated with full duty cycle range, the operation principle will be described with less than 50% duty cycle operation. There are six stages within one switching cycle during the steady-state operation. Due to the analogous circuit operation, only first three stages are described as follows.

Stage 1:

In stage 1, the main switch Q_1 is turned on by the control signal. The voltage on input inductor, L_1 , is equal to input voltage. Therefore, the current through inductor, L_1 , increased linearly. Because of the turning-off main switch, Q_2 , the voltage across the primary winding is the sum of the input voltage and the voltage across L_1 . Thus, the rectifier diodes, D_2 , D_4 and D_6 , are turned on due to its forwarded bias. Consequently, input power energy is transferred from primary winding to both of the secondary windings to charge output capacitors and clamping capacitors. The clamping capacitors C_1 and C_2 are charged by transformer winding S_1 through $S_1(-)-C_1-D_2-C_{O1}-S_1(+)$ and $S_1(-)-C_1-C_2-D_4-C_{O1}-C_{O2}-S_1(+)$, respectively. Also, the output capacitors C_{O3} and C_{O4} are charged by transformer winding S_2 through $S_2(-)-D_6-C_{O4}-S_2(+)$ and $S_2(-)-C_3-D_4-C_{O3}-C_{O4}-S_2(+)$, respectively. The voltage across D_1 , D_3 and D_5 is clamped to $V_o/3$ due to the turning on of the D_2 , D_4 and D_6 . Moreover, the energy stored in clamping capacitor C_C can be released to the secondary windings via transformer due to the turning-on of clamping switch during this time interval.

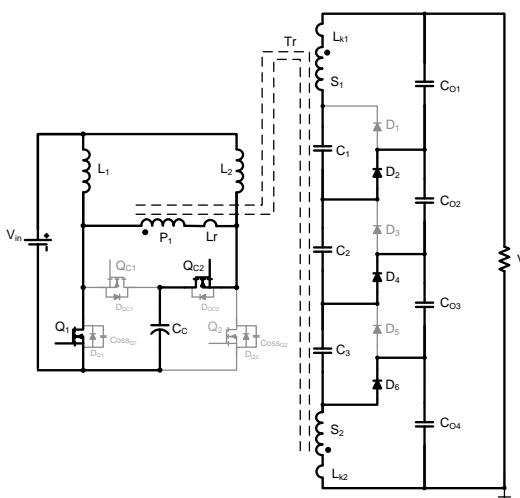


Fig. 3-33. Stage 1 of DB-TTVM-6.

Stage 2:

As shown in Fig. 3-34, the main switch Q_1 is turned off by the control signal. The parasitic capacitor of main switch, C_{ossQ1} , is charged by the current through input inductor, L_1 . The voltage across parasitic capacitor of main switch, V_{cossQ1} , is linearly increased and clamped to the V_{Cc} due to turning-on of the D_{Qc1} . The voltage across the primary winding is equal to the leakage inductor of transformer primary winding, L_r . Thus, the current through the rectifier diodes, D_2 , D_4 and D_6 , are decreased linearly until zero.

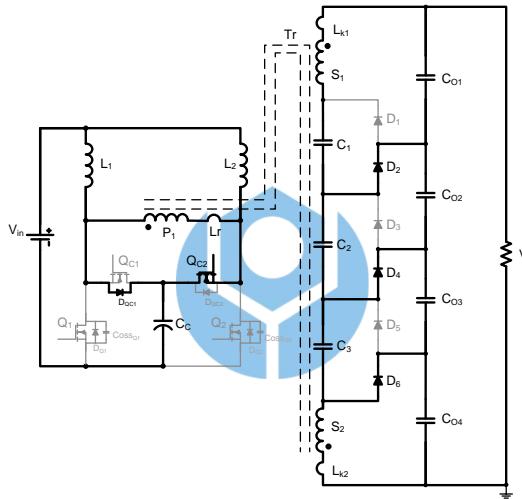


Fig. 3-34. Stage 2 of DB-TTVM-6.

Stage 3:

As shown in Fig. 3-35, the clamping switch Q_{C1} is turned on by the control signal to achieve the zero voltage turned-on (ZVS). The voltage across the transformer is thus shorted and the current of two input inductors decreases linearly. Without forward bias, both diodes D_1 - D_6 are turned off and clamped to $V_o/6$, respectively. The output current is the sum of the current through output capacitors and clamping capacitors as shown:

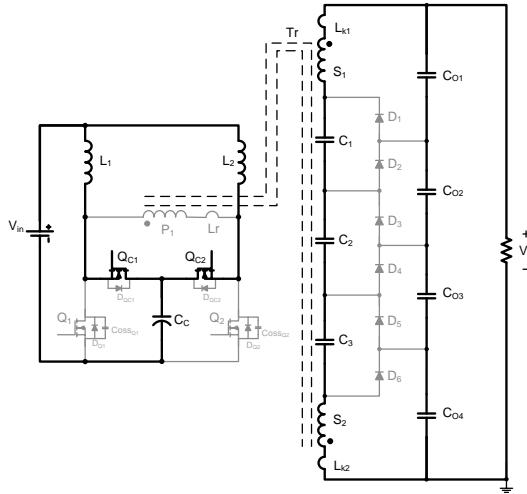


Fig. 3-35. Stage 3 of DB-TTVM-6.

Due to the similar operational behavior, the analogous stages are omitted.

3.4.2 Experiment Results of DB-TTVM-6

To demonstrate the feasibility and highlight the advantages of the proposed rectifier, three hardware circuits (DB-CWVM-6, DB-SVM-6 and DB-TTVM-6) operating with same specification are implemented and compared. Because the operating principle is analogous to the DB-TTVD, the design consideration of DB-TTVM-6 can be referred to Section 2.5. The specifications and main component parameters of DB-TTVM-6 are listed in Table 3-2.

Table 3-2. Specifications and main component parameters of DB-TTVM-6.

	DB-TTVM-6
Input Voltage, V_{in}	24~36 V
Output Voltage, V_O	380 V
Maximum Load Current, $I_{O, max}$	1 A
Maximum Load Power, $P_{O, max}$	380 W
Switching frequency, f_s	100 kHz
Transformer	Leakage inductance $L_{k1} = 0.156 \mu H, L_{k2} = 0.179 \mu H$ Turns-ratio $P_1:S_1:S_2 = 1 : 1.1 : 1.1$
Input inductor, L_1, L_2	$L_1 = 421 \mu H, L_2 = 315 \mu H$
Main Switches, Q_1, Q_2 Active clamping switches Q_{c1}, Q_{c2}	FDP047AN08A0
Active clamping capacitor, C_c	8.2 μF
Rectifier diodes $D_1, D_2, D_3, D_4, D_5, D_6$	MBR40250
Output filter capacitors $C_1, C_2, C_3, C_{O1}, C_{O2}, C_{O3}, C_{O4}$	8.2 $\mu F/450 V$ PP-cap

As shown in Fig. 3-36, the voltage across Q_1, Q_2, Q_{c1} and Q_{c2} are all clamped to the clamping capacitor, C_c which is $V_o/6.6\sim 58V$, respectively. Because the six-fold provide additional voltage gain, the low turns-ratio transformer can be applied. Therefore, the voltage rating of rectifier components is reduced. The operating duty cycle is over 50% when DB-TTVM-6 operated in low-line ($V_{in}=24V$) operating condition. On the contrary, the operating duty cycle is under 50% when

circuit operated in high-line ($V_{in}=36V$) operating condition.

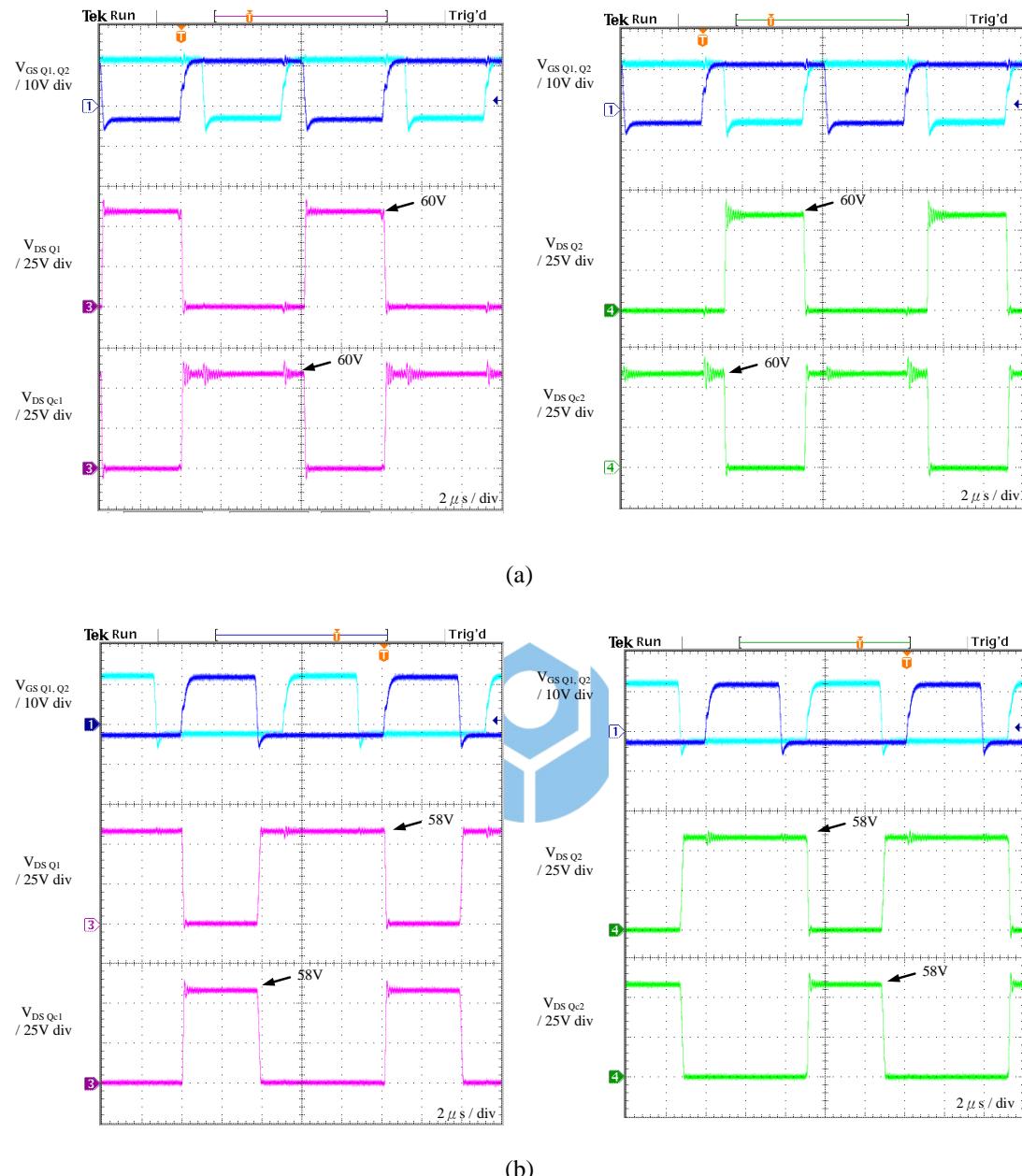


Fig. 3-36. Voltage waveforms of main switch and clamping switch under (a) low-line full-load ($V_{in}=24V$ $I_o=1A$) and (b) high-line light-load ($V_{in}=36V$ $I_o=0.1A$) operating conditions.

As shown in Fig. 3-37, the voltage stress of each rectifier diodes is identical and all clamped to $V_o/3$, 126V.

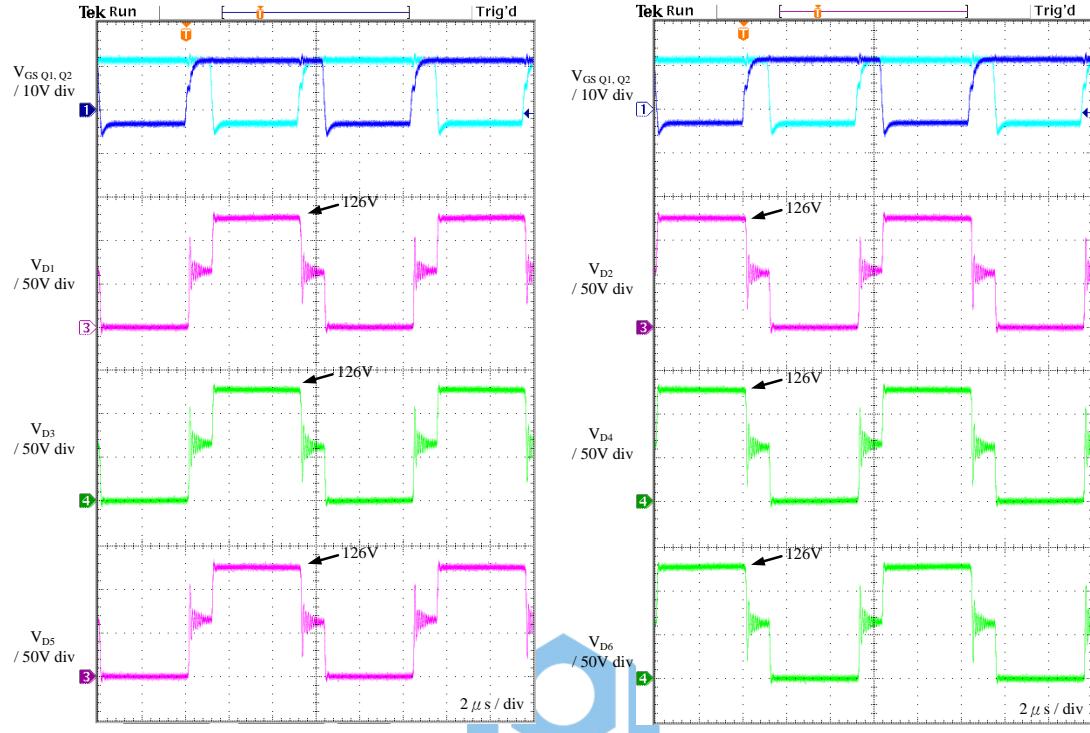


Fig. 3-37. Voltage waveforms of rectifier diodes under low-line and full-load operating conditions.

As shown in Fig. 3-38, the voltage of output capacitors, C_{O2} and C_{O3} , is evenly distributed to $V_o/3=126V$ which is two-time of the peak voltage of transformer secondary windings. The voltage of output capacitors, C_{O1} and C_{O4} is equal to $V_o/6=63V$ which is equal to the peak voltage of transformer secondary windings.

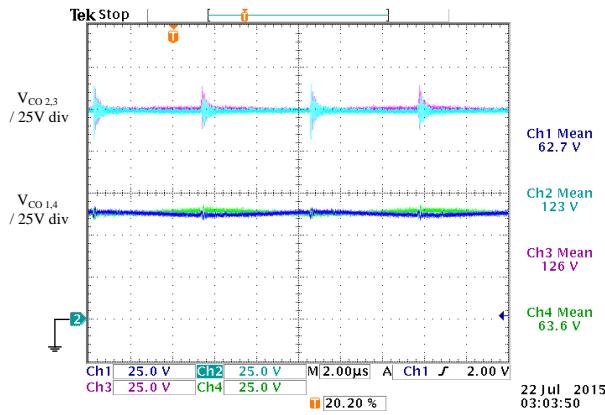


Fig. 3-38. Voltage waveforms of output capacitors.

As shown in Fig. 3-39, the current waveforms of output capacitors, $C_{O1}-C_{O4}$ and $C_{O2}-C_{O3}$, are inverse to each other. During both main switches Q_1 and Q_2 are turned on time interval, clamping capacitors, C_1 , C_2 , and C_3 , provides the output power. Thus, the current through output capacitors is nearly zero.

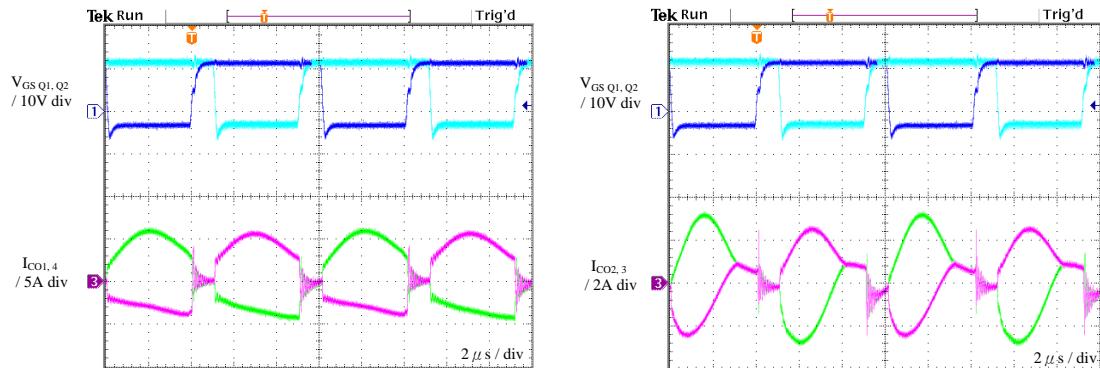


Fig. 3-39. Current waveforms of output capacitors under low-line and full-load operating conditions.

As shown in Fig. 3-40, the voltage ripple waveforms of output capacitors, $C_{O1}-C_{O4}$, and $C_{O2}-C_{O3}$ are upside down symmetrical to each other. The output capacitors are charged and discharged simultaneously to reduce the output voltage ripple. The output voltage ripple reduction can be achieved. Furthermore, the six-fold TTVM have even number of output capacitors and identical voltage ripple. Thus, the output voltage ripple cancellation mechanism is achieved to minimum the value as shown.

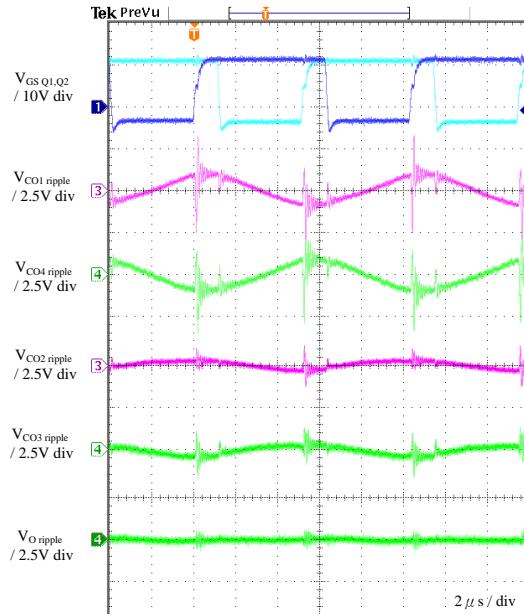


Fig. 3-40. Voltage ripple waveforms of output capacitors and output load under low-line and full-load operating conditions.

The measured efficiency of the presented converter with different input voltage and load conditions is shown in Fig. 3-41. A maximum efficiency, 95.51%, is obtained at low-line and 60% load conditions. In general practice, the best efficiency operating point of boost configuration is occurred at 50% duty cycle operating condition. The operating duty cycle is under 50% when the proposed circuit is operated under normal-line ($V_{in}=30V$) and high-line ($V_{in}=36V$) operating conditions.

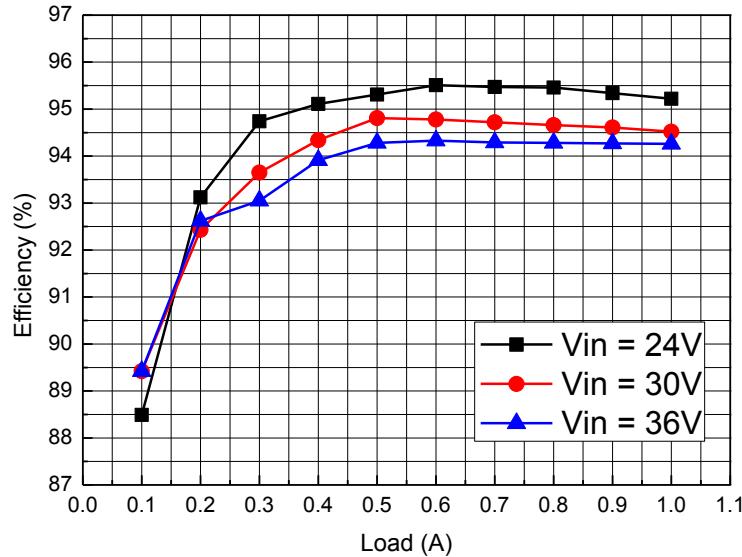


Fig. 3-41. Measured efficiency of DB-TTVM-6 power stage.

3.4.3 Experiment result comparisons among DB-CWVM-6, DB-SVM-6, and DB-TTVM-6

The voltage ripple and efficiency comparisons among DB-CWVM-6, DB-SVM-6, and DB-TTVM-6 are made under low-line ($V_{in}=24V$) and full-load (380W) operation conditions. The specifications and main parameters of three converters are shown as Table 3-3.

Table 3-3. Specifications and main component parameters of DB-CWVM-6, DB-SVM-6, and DB-TTVM-6.

	DB-CWVM-6	DB-SVM-6	DB-TTVM-6
Input Voltage, V_{in}	24~36 V		
Output Voltage, V_o		380 V	
Maximum Load Current, $I_{O, max}$		1 A	
Maximum Load Power, $P_{O, max}$		380 W	
Switching frequency, f_s		100 kHz	
Transformer	Leakage inductance $L_{k1} = 0.156 \mu H$, $L_{k2} = 0.179 \mu H$ Turns-ratio $P_1:S_1:S_2 = 1 : 1.1 : 1.1$		
Input inductor, L_1, L_2		$L_1 = 421 \mu H$, $L_2 = 315 \mu H$	
Main Switches, Q_1, Q_2 Active clamping switches Q_{c1}, Q_{c2}		FDP047AN08A0	
Active clamping capacitor, C_c		8.2 μF	
Rectifier diodes $n =$ number of components		MBR40250	
	$n = 6$	$n = 12$	$n = 6$
Output filter capacitors $n =$ number of components	8.2 $\mu F/450 V$ PP-cap		
	$n = 6$	$n = 9$	$n = 7$

As shown in Fig. 3-42 to Fig. 3-44, the output voltage ripple waveforms of three converters are captured, respectively. The voltage ripple of three circuits are 7.3V, 0.25V, and 0.1V, respectively.

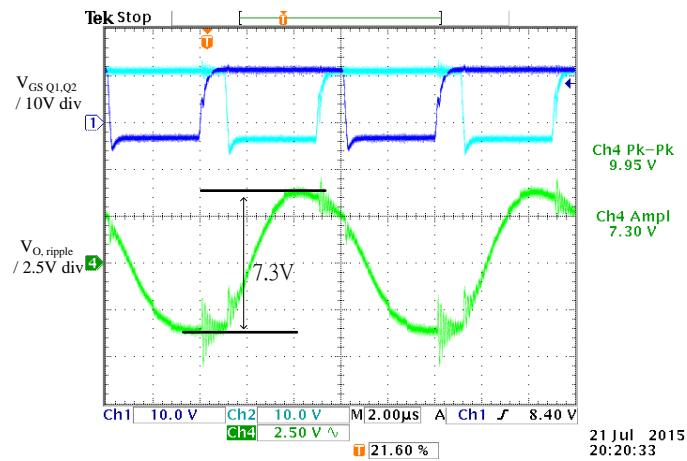


Fig. 3-42. Output voltage ripple waveform of DB-CWVM-6.

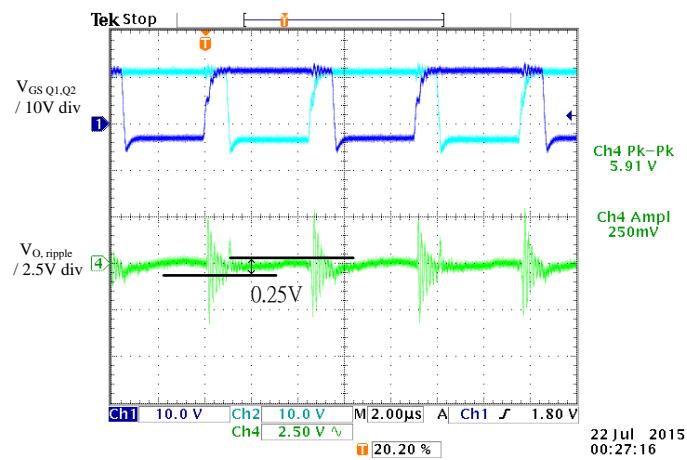


Fig. 3-43. Output voltage ripple waveform of DB-SVM-6.

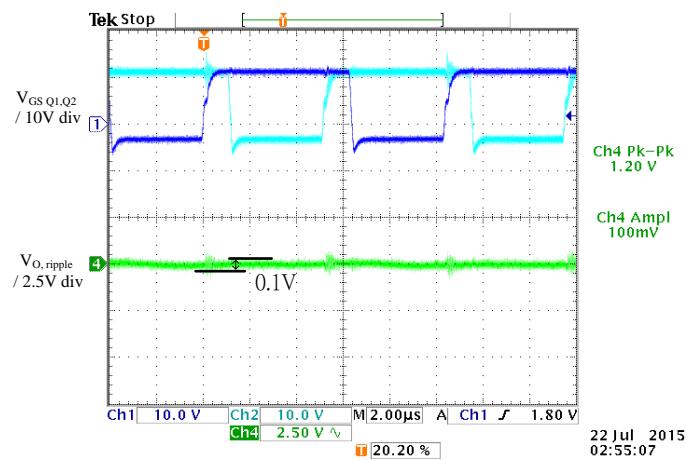


Fig. 3-44. Output voltage ripple waveform of DB-TTVM-6.

The efficiency comparison among DB-CWVM-6, DB-SVM-6 and DB-TTVM-6 is made under low-line operating condition ($V_{in} = 24V$) as shown in Fig. 3-45. The DB-TTVM-6 has higher efficiency performance than DB-CWVM-6 and DB-SVM-6. Because CWVM has the largest voltage drop, the efficiency is the worst.

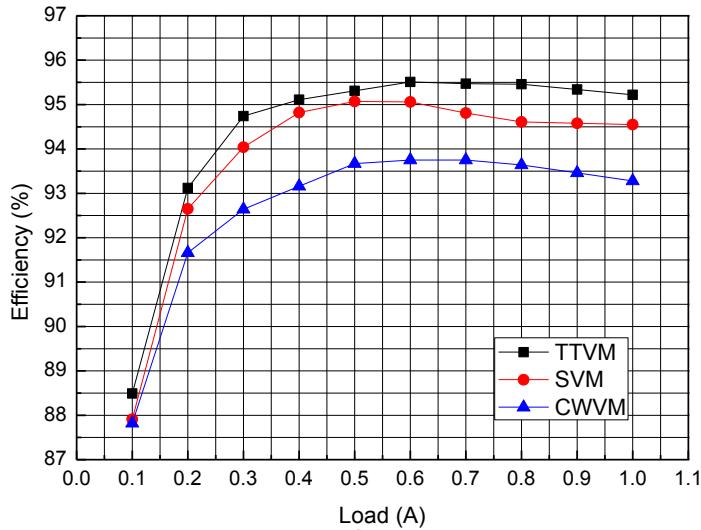
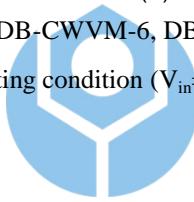


Fig. 3-45. Efficiency comparison among DB-CWVM-6, DB-SVM-6 and DB-TTVM-6 under low-line operating condition ($V_{in}=24V$).



3.5 Summary

A novel voltage multiplier rectifier, Taiwan Tech voltage multiplier rectifier (TTVM), is proposed in this section. Three voltage multiplier rectifiers (CWVM, SVM, and TTVM) are investigated and compared. TTVM has greatly reduced the output voltage ripple and voltage drop compared with CWVM under same operating conditions. Because, TTVM has built-in output voltage ripple cancellation/reduction mechanism, the capacitance of multiplier can be reduced. SVM and TTVM have two transformer secondary windings to reduce the output voltage ripple and voltage drop. However, the TTVM can be achieved same output voltage ripple specification with less component counts.

Three circuits of DB-CWVM-6, DB-SVM-6, and DB-TTVM-6 are implemented with 100 kHz, 24~36V input range and 380V/1A output specification. The output voltage ripple of three circuits is measured as 7.3V (DB-CWVM-6), 0.25V (DB-SVM-6), and 0.1V (DB-TTVM-6), respectively. The maximum efficiency of three circuits is 93.75% (DB-CWVM-6), 95.07% (DB-SVM-6), and 95.51% (DB-TTVM-6), respectively. These data verify the description in this Chapter.



Chapter 4 Conclusions and future research

4.1 Conclusions

DB-TTVD and DB-CVD have been implemented and compared for sustainable energy power system applications. The proposed TTVD has the output voltage ripple cancellation mechanism and the current ripple reduction of output capacitors. Therefore, the output capacitances can be minimized. Consequently, large capacitance of aluminum electrolytic capacitors can be replaced with small capacitance of polypropylene film capacitors.

A TTVM has also been presented in this dissertation. The characteristics comparisons among n-fold CWVM, SVM and TTVM are summarized and listed in Table 4-1. The characteristics include voltage gain, voltage rating of components, component count, voltage drop, voltage ripple, and transformer voltage insulation requirement. By using an additional transformer secondary winding and filter capacitor, TTVM has less voltage drop, voltage ripple and start-up time than these of CWVM at the cost of using a high voltage insulation transformer. In addition, the output voltage ripple cancellation mechanism can be achieved with $(2+k*4)$ -fold TTVM.

Table 4-1. Characteristic comparisons with n-fold voltage multiplier rectifiers.

	CWVM	SVM	TTVM
Output voltage	nV_p		
Voltage rating of diode	$\frac{2V_o}{n}$		
Maximum voltage rating of capacitor	$\frac{2V_o}{n}$		
Voltage drop* @X6, $I_o=1\text{mA}$	463.283 V	153.611 V	149.55 V
Voltage ripple* @X6, $I_o=1\text{mA}$	110.832 V	24.526 V	14.476 V
Number of diode	n	2n	n
Number of capacitor	n	$\frac{3}{2}n$	n+1
Number of transformer secondary winding	1	2	2
Transformer insulation requirement	Low	Low	High

Where V_p is the peak voltage of transformer secondary winding.

*Data obtained under $V_{in}=500\text{V}$, $C=1\text{nF}$, and $V_o=3000\text{V}$ operating condition.

DB-CWVM-6, DB-SVM-6 and DB-TTVM-6 have been implemented under same specifications. Among them, the voltage ripple and efficiency performance are compared. Referring to Fig. 3-42, Fig. 3-43, and Fig. 3-44, voltage ripple of three circuits are 7.3V (DB-CWVM-6), 0.25V (DB-SVM-6), and 0.1V (DB-TTVM-6), respectively. On the other hand, DB-TTVM-6 has the highest efficiency under full-load operating conditions referred to Fig. 3-45. The maximum efficiency of three circuits is 93.75% (DB-CWVM-6), 95.07% (DB-SVM-6), and 95.51% (DB-TTVM-6), respectively.

4.2 Future Research

To solve the high voltage insulation of transformer problem, two transformer secondary windings can be implemented with two individual transformers. Therefore, it is easier to design the transformer construction.

To realize the parameters, such as filter capacitance, load current, operating frequency, parasitic of components influence the output voltage ripple and voltage drop of TTVM, it can be further investigated and calculated.

This dissertation proposes a novel Taiwan Tech voltage multiplier rectifier circuits that can be applied to any other converters, such as single-inductor current-fed boost converter, full-bridge current-fed boost converter, and LLC converter as shown in Fig. 4-1 to Fig. 4-6, respectively. The different voltage gain can be achieved by using different number of stages and comparative small voltage-rating components.

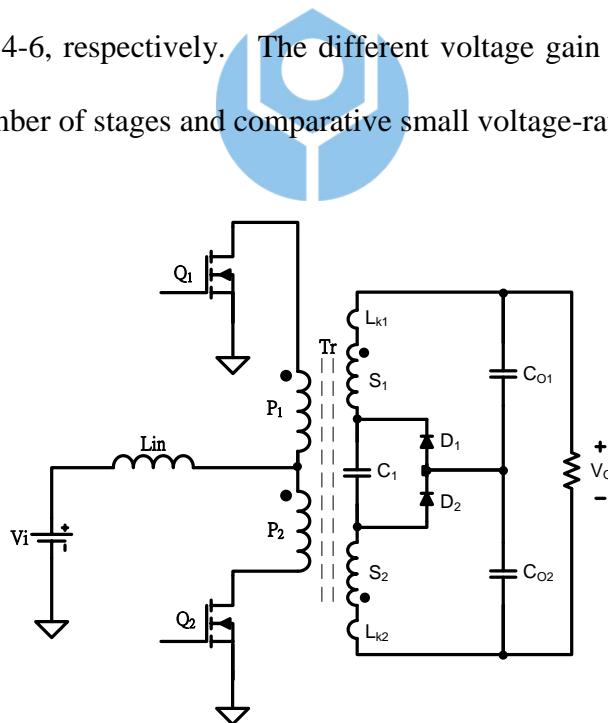


Fig. 4-1. Circuit diagram of single-inductor current-fed boost converter with TTVD.

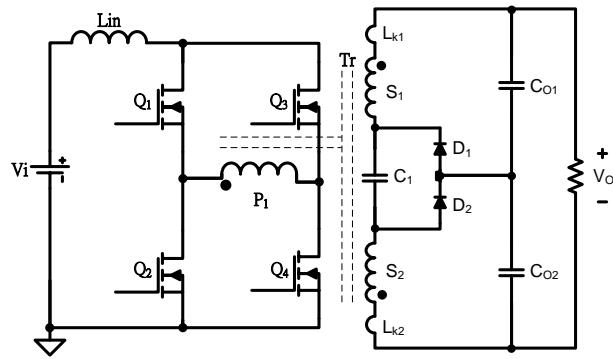


Fig. 4-2. Circuit diagram of full-bridge current-fed boost converter with TTVD.

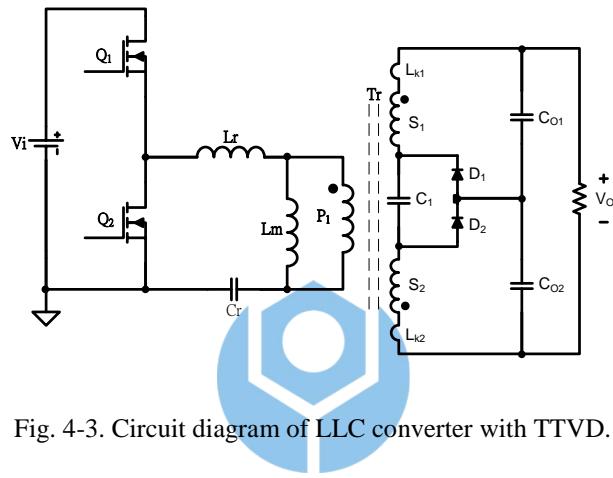


Fig. 4-3. Circuit diagram of LLC converter with TTVD.

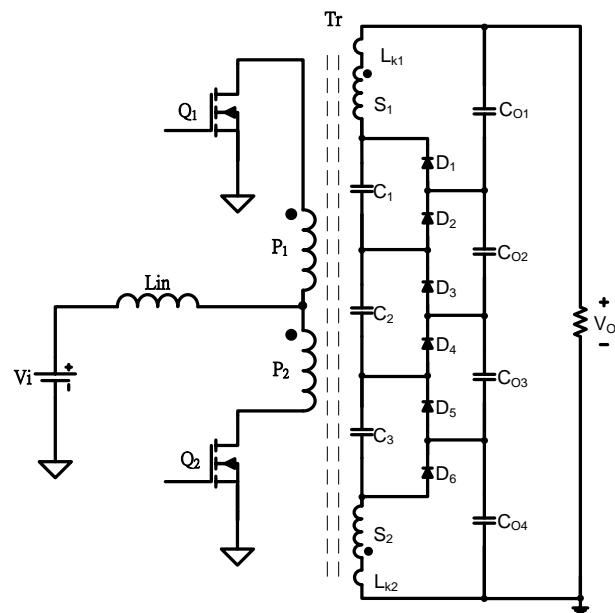


Fig. 4-4. Circuit diagram of single-inductor current-fed boost converter with TTVM-6.

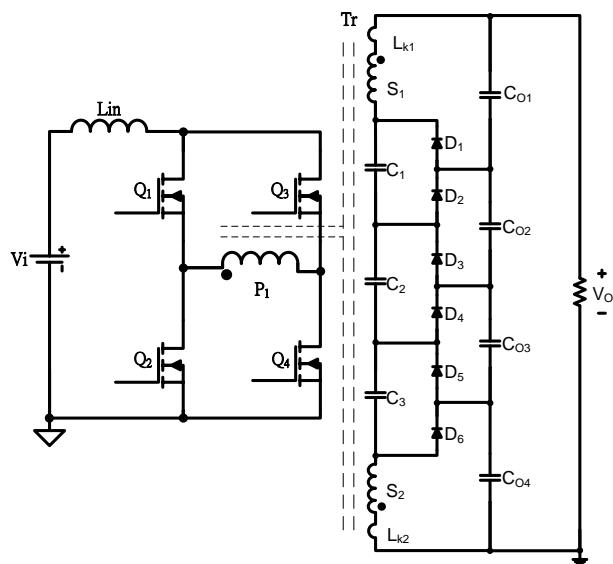


Fig. 4-5. Circuit diagram of full-bridge current-fed boost converter with TTVM-6.

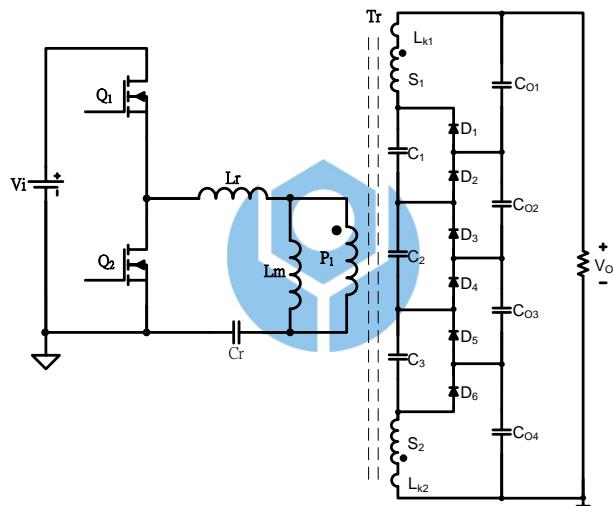


Fig. 4-6. Circuit diagram of LLC converter with TTVM-6.

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