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Output Impedance in PWM Buck Converter

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ABSTRACT

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In this paper, a method is presented to design a minimum order compensator for a PWM buck converter with voltage-mode control that will reduce the closed-loop output impedance to match a specific transfer function. The transfer function for the compensator is rigorously developed. It is shown that a third-order compensator is sufficient to achieve a closed-loop output impedance represented by a first-order transfer function. The method is applied to an example, in which the hardware of the dc-dc converter is realized and tested to verify compliance to system requirements.

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1 Research Motivation

1.1 Introduction

The requirements for the dc-dc converter continue to become more stringent as load voltages decrease and load current demands increase. The converter must be able to maintain its output voltage within an ever tightening tolerance, while responding to ever increasing load step sizes. Many attempts have been made to improve the dynamic response of PWM buck converters to a step change in load current [1]-[8]. Ljumbomi Varga presented a method to synthesis a zero-impedance converter [9]. This method requires both a positive current feedback and a negative voltage feedback for synthesis as well as a current sensing device. Richard Redl presented a method to achieve near-optimum dynamic regulation by combining feed-forward of the output current and input voltage with current-mode control (CMC) [10]. A common method used in industry to control the output impedance is to use many output filter capacitors placed in parallel to reduce the equivalent series resistance (ESR) [11]-[17]. In this approach, the feedback compensator is designed to provide the loop gain and phase margin for stability and the peak closed-loop output impedance is achieved through proper selection of low ESR output capacitors.

The objective of this paper is to consider how to reduce the output impedance in the PWM buck converter with voltage-mode control (VMC) without requiring low ESR output capacitors. VMC offers a cost and size advantage over the CMC method of

converter control. The selection of low ESR capacitors is limited, and increasing the number of capacitors to meet the transient requirement is not a suitable solution in many applications because of size and cost issues.

This paper accomplishes the task of deriving the transfer function of the feedback compensator in order to achieve a specific closed-loop output impedance. The methodology shows how to reduce the output impedance using a combination of compensator gain and the ESR of the output capacitor. The specific closed-loop output impedance is represented by a first-order transfer function with a "high-pass" frequency response for which the gain and bandwidth are established to comply with a given set of converter requirements using the critical bandwidth concept previously published [18]. To derive the transfer function of the compensator, the PWM switches are replaced by a linear small-signal model. The results show that a third-order compensator is sufficient to achieve the closed-loop output impedance. Additional tests are rigorously developed to determine if the order of the compensator can be further reduced. The compensator design method is demonstrated via simulation and hardware experiments.

1.2 The Buck Converter Circuit

The circuit diagram of an open-loop PWM buck converter is shown in Fig. 1.1. There is one input, the duty cycle of the PWM signal, which includes the sum of a fixed or dc component and a varying or ac component expressed as $d_T = D_T + d_t$. There are two disturbances, the input voltage, $v_I = V_I + v_i$, and the output current, $i_O = I_O + i_o$ where both consist of the sum of dc and ac components. There are two outputs, voltage, $v_O = V_O + v_o$, and inductor current, $i_L = I_L + i_l$, each having a dc and ac component. The inductor, L, has a parasitic dc resistance r_L, and the capacitor, C, has a parasitic dc resistance r_C.

The switches are a MOSFET and a diode. The switches will be replaced by a linear model and open-loop transfer functions will be provided to design a PWM buck converter.

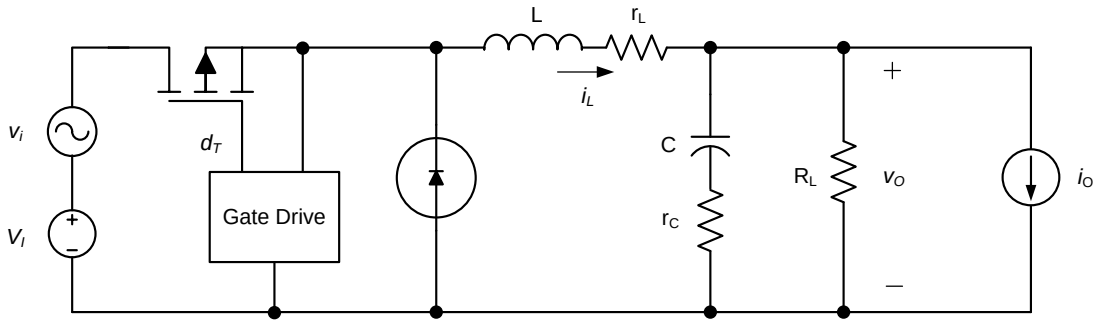

Figure 1.1: Open-loop Buck Converter

The buck converter is a step down type of converter in which the output voltage is always lower than the input voltage. It is one of the most fundamental topologies and common switching power supply configurations. Its operation is like this [19]. When the switch is turned on (closed), the input voltage is applied to the inductor, and power is delivered to the load, R_L. When the switch is turned off (opened) the voltage across the inductor reverses and the free-wheeling diode becomes forward biased. This allows the energy stored in the inductor to be delivered to the output where the continuous current is then smoothed by the output filter capacitor, *C*. Typical waveforms for a buck converter are shown in Fig. 1.2. Neglecting circuit losses, the steady-state average voltage across the inductor is zero. The basic dc equation of the buck converter is given by

$$M_{vdc} = \frac{V_O}{V_I} = D \tag{1.1}$$

where *D* is the MOSFET switching duty cycle.

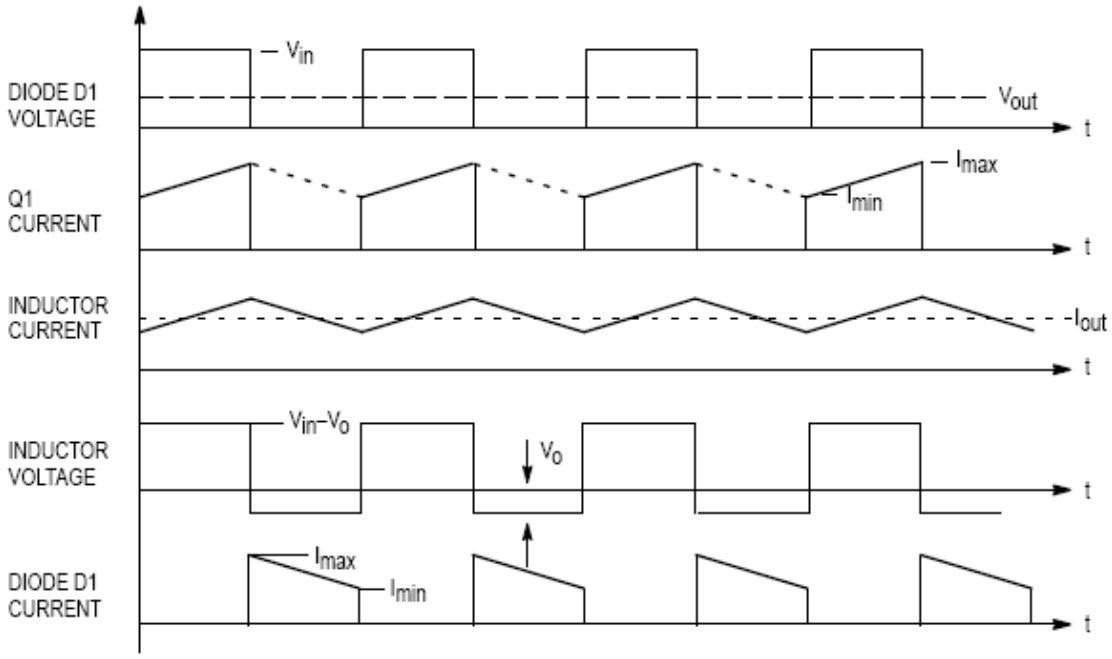

Figure 1.2: PWM Buck Converter waveforms

The closed-loop PWM buck converter with voltage feedback control circuitry is shown in Fig. 3. Output voltage regulation is controlled by varying the duty cycle of the switch by the PWM modulator through voltage feedback. In Fig. 1.3, the output voltage is fed through a voltage divider network, β, to produce the feedback voltage, v_f, which is equal to the dc reference voltage, v_{REF}, when the disturbances are equal to zero. The difference between the feedback voltage and the reference voltage is the error voltage, v_e. The error amplifier conditions the loop gain to achieve the desired frequency and dynamic response for the closed-loop system. A method to design the compensator to achieve a specific frequency response will be derived. The modulator compares the output from the compensator, v_c, to a ramp waveform to produce a PWM signal with a duty cycle which is proportional to the error, v_c. The frequency of the ramp waveform, f_s, determines the frequency of the PWM signal which controls the switch.

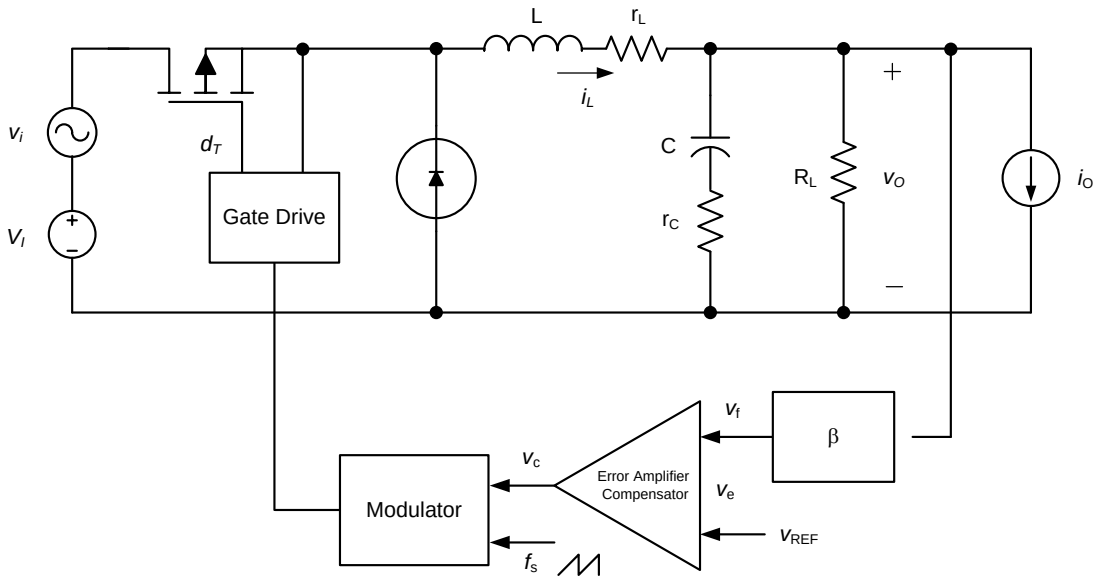

Figure 1.3: Buck Converter with Voltage Feedback Control

The compensator typically includes an integrator to achieve a desired phase margin for the loop gain. At high frequency, the compensator produces a loop gain which has a negligible gain and hence little effect on the closed-loop response. The thesis will derive a compensator that can affect the high frequency response as required to achieve design specifications for a dc-dc converter.

1.3 Dissertation Objectives

The objectives of this thesis are to provide a compensator design method that improves the output impedance of the closed-loop PWM buck converter with voltage mode control. It will be shown that a third-order compensator is sufficient to achieve a critically damped response of the output voltage to a step change in load current. A set of tests are derived to provide the designer a straight-forward way to determine if the order of the compensator can be further reduced. A relationship will be provided between the coefficients of the compensator transfer function and critical aspects of dc-dc converter specifications including bandwidth and output voltage tolerance. A gain parameter is

provided which gives the designer control over the magnitude of the output impedance and hence the size of the voltage spike due to a step change in load current. This provides an alternative to adding low ESR capacitors to the buck converter. The range for the transfer function coefficients are derived which consider the limitations of the linear small-signal model for the switches, synthesis limitations, and assurance of a critically damped dynamic response.

1.4 Outline of Dissertation

Chapter 2 presents a literature search which focuses on how industry engineers design a compensator for a PWM Buck Converter to comply with a given set of requirements. The industry approach is demonstrated using Intel's Voltage Regulator Module specifications. The relevant transfer functions for the open and closed-loop systems are presented. In addition, the step response of the output voltage to a step change in input voltage and load current are shown to verify the design complies with the system requirements.

Chapter 2 begins with the introduction of the linear model for the switches. The converter is a highly non-linear system which includes a transistor operating as a switch to control the output voltage. Using the linear model for the transistor and diode, the open-loop transfer functions are developed for the output filter of the power stage, the control-to-output voltage, the input-to-output voltage, input impedance, and output impedance. Specifications for a real world dc-dc converter are used to give the reader insight of typical frequency and time response characteristics of an open-loop converter. The open-loop step response of the output voltage to a step change in input voltage, duty cycle, and load current are presented.

Next, the closed-loop transfer functions for the input-to-output voltage and output impedance are presented. It is shown that the loop gain attenuates the closed-loop transfer function at low frequency, but typically has little effect at high frequency. As a result, the loop gain plays a very important part in the closed-loop system response. The loop gain is highly dependent on the compensator. A step-by-step method for compensator design commonly used by industry engineers is presented using real-world requirements for a dc-dc converter. In this method, the engineer selects one of three different compensator topologies depending on the required phase margin of the closed-loop system and the actual phase margin of the uncompensated loop gain. The gain, poles, and zeros of the compensator are then arranged to achieve the required phase margin. The transfer functions and their frequency response are presented. In addition, the response of the output voltage to a step change in input voltage and load current are presented for the closed-loop buck converter.

Chapter 3 presents an alternative approach to design a PWM Buck Converter with Voltage Mode Control (VMC). The first step is to design the power stage for the converter and determine the open-loop output impedance of the converter. The next step is to determine a transfer function for the closed-loop output impedance that ensures the output voltage stays within its specified tolerance when exposed to the maximum step change in load. A first order, critically damped transfer function is chosen as the model for the closed-loop output impedance. The transfer function for the compensator is derived. It is shown that a third order compensator is sufficient to achieve a critically damped response to a step change in load. A set of tests are derived that can be used to determine if the order of the compensator can be further reduced.

In Chapter 4 the method presented in Chapter 3 is applied to a real world dc-dc converter. Simulation results are presented to verify compliance to the real-world requirements. A second example is presented in Chapter 5. In this example, the hardware for the buck converter is designed, simulated, and tested to verify compliance to stated requirements.

Chapter 6 provides a summary and conclusion for the thesis.

2 Common Industry Approach to Buck Converter Design

2.1 Introduction

This chapter presents the most common method used by industry to design a PWM Buck Converter with Voltage Mode Control. The method employs a linear small-signal model in place of the non-linear switching elements to enable classical control theory. The method relies on designing the loop gain to achieve the phase margin. A limited set of compensator topologies are used to achieve the required phase margin. The output impedance is determined by the ESR of the output capacitor. To meet stringent requirements, many parallel capacitors may be required to achieve the ESR necessary to keep the output voltage of the dc-dc converter within its tolerance band when exposed to a fast large step change in load current. The Intel VRM 9.1 requirements are used as a design example.

2.2 Small-Signal Model of PWM Buck Converter

The common method to design a closed-loop feedback system is to apply linear control theory. Linear control theory is well developed and provides valuable tools for studying the dynamic performance of a converter. Typical control aspects of interest are frequency response, transient response, and stability. However, the PWM Buck Converter is not a linear system since it contains a MOSFET and diode operating as switches. Therefore, a linear model is required in order to apply linear control theory.

In this research, the circuit-averaging method is applied to create a linear circuit model of the MOSFET and diode [20]. This model includes parasitic aspects of the switching devices according to

$$r = D_{nom} r_{DS} + (1 - D_{nom}) R_F + r_L \tag{2.1}$$

where r_{DS} is the MOSFET drain to source resistance, R_F is the forward resistance of the diode, r_L is the equivalent series resistance (ESR) of the inductor, and D_{nom} is the nominal duty cycle of the switch. Fig. 2.1 shows the PWM buck converter with VMC with the linear model employed.

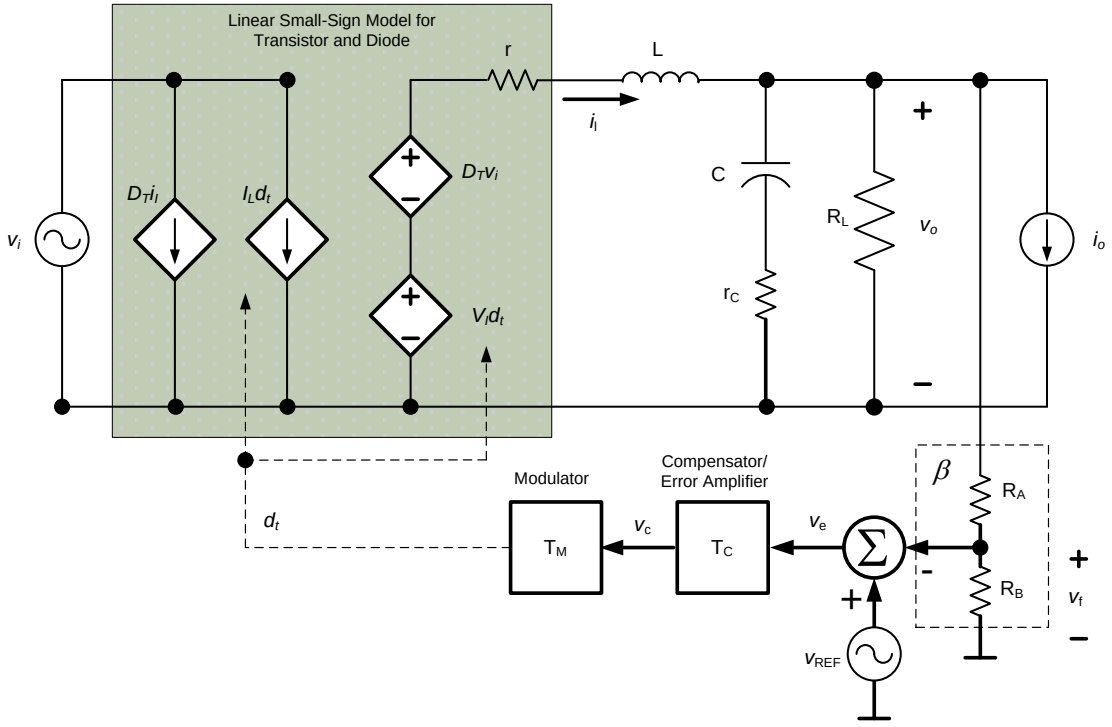

Figure 2.1: Linear small-signal model of PWM Buck Converter with VMC

The various transfer functions that characterize the converter are necessary to facilitate the use of control theory. Fig. 2.2 shows a fundamental block of the converter, the output filter of the power stage. The transfer function of the output filter, G_{psf}, in the

s-domain is developed in (2.2)-(2.14). The transfer function is near unity at low frequency, provided the load resistance is significantly larger than the parasitic resistance, *r*. The transfer function has a zero due to the ESR of the capacitor (2.11), and two poles according to (2.12). The resonant frequency is expressed in (2.13). The damping coefficient (2.14) includes the parasitic elements of the components; therefore, they should not be ignored when characterizing the buck converter.

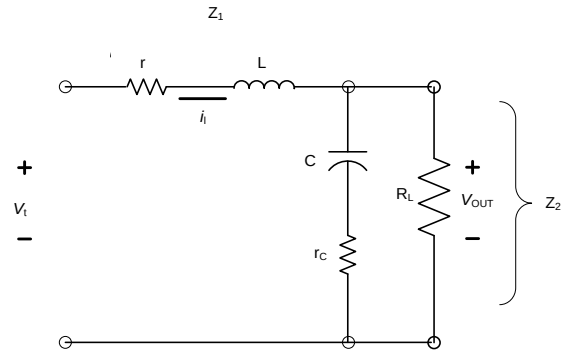

Figure 2.2: Buck Converter output filter with *r*

$$G_{psf}(s) \equiv \frac{v_o(s)}{v_t(s)}\Big|_{v_i = i_o = d = 0} = \frac{Z_2}{Z_1 + Z_2} \tag{2.2}$$

$$Z_1 = r + Ls \tag{2.3}$$

$$Z_2 = R_L \,\|\left(\frac{1}{sC} + r_C\right) = \frac{R_L(1 + r_C sC)}{1 + sC(R_L + r_C)} \tag{2.4}$$

$$G_{psf}(s) = \frac{\dfrac{R_L(1 + r_C sC)}{1 + sC(R_L + r_C)}}{r + Ls + \dfrac{R_L(1 + r_C sC)}{1 + sC(R_L + r_C)}} \tag{2.5}$$

$$G_{psf}(s) = \frac{R_L(1 + r_C sC)}{s^2 LC(R_L + r_C) + s\left[C(R_L r_C + R_L r + r_C r) + L\right] + (R_L + r)} \tag{2.6}$$

$$G_{psf}(s) = \frac{R_L r_C}{L(R_L + r_C)} \frac{s + \frac{1}{Cr_C}}{s^2 + s\left(\frac{\left[C(R_L r_C + R_L r + r_C r) + L\right]}{LC(R_L + r_C)}\right) + \frac{R_L + r}{LC(R_L + r_C)}} \quad (2.7)$$

$$G_{psf}(0) = \frac{R_L}{R_L + r} \approx 1 \quad R_L << r \quad (2.8)$$

$$G_{psf}(s) = G_{psfx} \frac{s + \omega_Z}{s^2 + 2\xi\omega_O s + \omega_O^2} \quad (2.9)$$

$$G_{psfx} = \frac{R_L r_C}{L(R_L + r_C)} \quad (2.10)$$

$$\omega_z = -\frac{1}{Cr_C} \quad (2.11)$$

$$\omega_{p_1}, \omega_{p_2} = -\omega_O\xi \pm \omega_O\sqrt{\xi^2 - 1} = -\omega_O\xi \pm j\omega_O\sqrt{1 - \xi^2} \quad (2.12)$$

$$\omega_O = \sqrt{\frac{R_L + r}{LC(R_L + r_C)}} \quad (2.13)$$

$$\xi = \frac{L + C\left[R_L(r_C + r) + r_C r\right]}{2\sqrt{LC(R_L + r_C)(R_L + r)}} \quad (2.14)$$

The control-to-output transfer function, also called the duty cycle-to-output voltage transfer function, is expressed by (2.15)-(2.16). The low frequency value of the transfer function is approximately equal to the nominal input voltage (2.17). The open-loop input-to-output transfer function, also called the line-to-output transfer function, or the audio susceptibility is given by (2.18)-(2.19). The low frequency value of the transfer function is approximately equal to the nominal duty cycle (2.20). The transfer functions for T_P and M_V both have the same poles, zeros, and phase as the transfer function of the output filter, G_{psf}.

$$T_P(s) \equiv \frac{v_o(s)}{d(s)}\Big|_{v_i = i_o = 0} = V_I G_{psf}(s) = T_{px}\frac{s + \omega_Z}{s^2 + 2\xi\omega_O s + \omega_O^2} \tag{2.15}$$

$$T_{px} = V_I G_{psfx} = \frac{V_I R_L r_C}{L(R_L + r_C)} \tag{2.16}$$

$$T_p(0) = V_I \frac{R_L}{R_L + r} \approx V_I \quad R_L << r \tag{2.17}$$

$$M_V(s) \equiv \frac{v_o(s)}{v_i(s)}\Big|_{d = i_o = 0} = DG_{psf}(s) = M_{vx}\frac{s + \omega_Z}{s^2 + 2\xi\omega_O s + \omega_O^2} \tag{2.18}$$

$$M_{vx} = DG_{psfx} = \frac{DR_L r_C}{L(R_L + r_C)} \tag{2.19}$$

$$M_v(0) = D\frac{R_L}{R_L + r} \approx D \quad R_L << r \tag{2.20}$$

The transfer function for the open-loop input impedance is given by (2.21)-(2.23) [20]. The low frequency value of the open-loop input impedance is given by (2.24). The input impedance increases at +20 dB/decade at frequencies above ω_o.

$$Z_i(s) \equiv \frac{v_i(s)}{i_i(s)}\Big|_{d = i_o = 0} = Z_{ix}\frac{s^2 + 2\xi\omega_O s + \omega_O^2}{s + \omega_{cr}} \tag{2.21}$$

$$\omega_{cr} = -\frac{1}{C(R_L + r_C)} \tag{2.22}$$

$$Z_{ix} = \frac{L}{D^2} \tag{2.23}$$

$$Z_i(0) = \frac{R_L + r}{D^2} \approx \frac{R_L}{D^2} \qquad R_L << r \tag{2.24}$$

To find the output impedance for the open-loop converter, one can apply a test voltage source v_t across the load resistance R_L and determine the current i_t forced by test voltage. The ratio of the voltage, v_t, to the current, i_t, is equal to the output impedance

Z_O. Fig. 2.3 shows the schematic used to derive the open-loop output impedance of the converter. The transfer function for the open-loop output impedance is derived in (2.25)-(2.34). The low frequency value of the open-loop output impedance is approximately r (2.33), and the high frequency value can be approximated by r_C (2.34) when R_L is much greater than r and r_C. Note the output impedance has the same poles as the output filter of the buck converter.

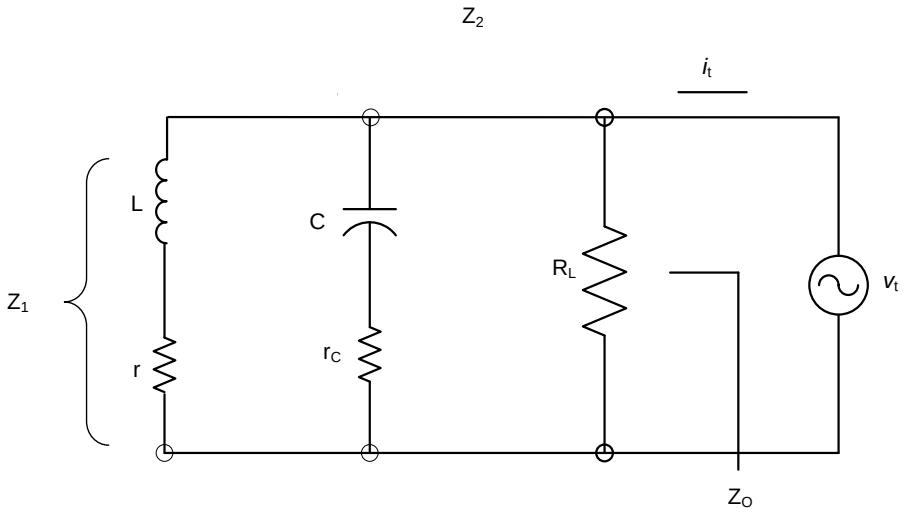

Figure 2.3: Small-signal model of the PWM converter for the derivation of the open-loop output impedance, Z_O

$$Z_o(s) \equiv -\frac{v_t(s)}{i_t(s)}\Big|_{v_i=d=i_o=0} = Z_1(s) \| Z_2(s) \tag{2.25}$$

$$Z_1(s) = Ls + r \tag{2.26}$$

$$Z_2(s) = \left(\frac{1}{sC} + r_C\right) \Big\| R_L = \frac{R(sCr_C + 1)}{C(R + r_C) + 1} \tag{2.27}$$

$$Z_o(s) = \frac{Rr_C\left[s^2 + \left(\frac{L + Cr_C r}{LCr_C}\right)s + \left(\frac{r}{LCr_C}\right)\right]}{(R + r_C)\left[s^2 + \left(\frac{L + rC(R + r_C) + RCr_C}{LC(R + r_C)}\right)s + \left(\frac{R + r}{LC(R + r_C)}\right)\right]} \tag{2.28}$$

$$Z_o(s) = \frac{Rr_C\left(s + \frac{1}{Cr_C}\right)\left(s + \frac{r}{L}\right)}{(R + r_C)\left[s^2 + \left(\frac{L + rC(R + r_C) + RCr_C}{LC(R + r_C)}\right)s + \left(\frac{R + r}{LC(R + r_C)}\right)\right]} \tag{2.29}$$

$$Z_o(s) = LG_{psf}(s)(s + \omega_{rl}) = Z_{ox}\frac{(s + \omega_z)(s + \omega_{rl})}{s^2 + 2\xi\omega_O s + \omega_O^2} \tag{2.30}$$

$$Z_{ox} = LG_{psfx} = \frac{R_L r_C}{R_L + r_C} \tag{2.31}$$

$$\omega_{rl} = -\frac{r}{L} \tag{2.32}$$

$$Z_o(0) = \frac{R_L r}{R_L + r} \approx r \quad r << R_L \tag{2.33}$$

$$Z_o(\infty) = \frac{R_L r_C}{R_L + r_C} \approx r_C \quad r_C << R_L \tag{2.34}$$

As an example, consider the requirements for the Intel microprocessor given in Table 2.1 [21]. A design procedure based on [22] is as follows. The maximum and minimum values for the output power are expressed by (2.35) and (2.36) and the minimum and maximum values for the load resistance (2.37) and (2.38). The minimum and maximum values of the dc voltage transfer function are given by (2.39) and (2.40) and the range for the duty cycle is given by (2.41) and (2.42).

$$P_{O(\max)} = V_{O(\max)} I_{O(\max)} = 1.491 \times 10 = 14.91\ \text{W} \tag{2.35}$$

$$P_{O(\min)} = V_{O(\min)} I_{O(\min)} = 1.461 \times 0.5 = 0.73\ \text{W} \tag{2.36}$$

$$R_{L(\max)} = \frac{V_{O(\max)}}{I_{O(\min)}} = \frac{1.491}{0.5} = 2.982\ \Omega \tag{2.37}$$

$$R_{L(\min)} = \frac{V_{O(\min)}}{I_{O(\max)}} = \frac{1.461}{10} = 0.146\ \Omega \tag{2.38}$$

$$M_{VDC(\max)} = \frac{V_{O(\max)}}{V_{I(\min)}} = \frac{1.491}{11.04} = 0.135 \tag{2.39}$$

$$M_{VDC(\min)} = \frac{V_{O(\min)}}{V_{I(\max)}} = \frac{1.461}{12.60} = 0.116 \tag{2.40}$$

$$D_{(\max)} = \frac{M_{VDC(\max)}}{\eta} = \frac{0.135}{0.7} = 0.193 \tag{2.41}$$

$$D_{(\min)} = \frac{M_{VDC(\min)}}{\eta} = \frac{0.116}{0.7} = 0.166 \tag{2.42}$$

Parameter	Max	Nominal	Min
Input Voltage, V_I (V)	12.60	12.00	11.04
Output Voltage, V_O (V)	1.491	1.476	1.461
Output Current, I_O (A)	10		0.5
Output Current Slew Rate, I_O (A/μs)			50
Switching frequency, f_S (Hz)			200
Ripple Voltage (%)	1		
Efficiency, η (%)			70

Table 2.1: Buck Converter Specifications

The minimum inductance that is required to maintain the converter in Continuous Conduction Mode (CCM) is expressed by (2.43). The inductor selected to comply with (2.43) is given by (2.44). The dc resistance of the inductor is (2.45). The maximum inductor ripple current is expressed by (2.46). The ripple voltage is given by (2.47). The maximum ESR of the filter capacitor to comply with the ripple voltage specification is given by (2.48). Before selecting the ESR, the designer must also consider the maximum step size of load current, and choose the ESR so the product of the maximum step change

in load does not cause the output voltage to exceed the voltage specification as expressed in (2.49). The minimum value of the filter capacitance at which the ripple voltage is determined by the ripple voltage across the ESR is expressed by (2.50). Choose the capacitance of the output filter to be (2.51) to comply with (2.50). To achieve the required ESR and minimum capacitance, the design will require 7 capacitors on the output filter, which will equate to the total output capacitance and ESR expressed by (2.52).

$$L_{(\min)} = \frac{R_{L(\max)}\left(1 - D_{(\min)}\right)}{2 f_S} = \frac{2.982\left(1 - 0.166\right)}{2\left(200 \times 10^3\right)} = 6.2\ \mu\text{H} \tag{2.43}$$

$$L = 13\ \mu\text{H} / 9\ \text{m}\Omega / 11.4\ \text{A} \tag{2.44}$$

$$r_L = 9\ \text{m}\Omega \tag{2.45}$$

$$\Delta i_{L(\max)} = \frac{V_{O(\max)}\left(1 - D_{(\min)}\right)}{f_S L} = \frac{1.491\left(1 - 0.166\right)}{\left(200 \times 10^3\right)\left(13 \times 10^{-6}\right)} = 0.478\ \text{A} \tag{2.46}$$

$$V_r = \frac{V_{O(\max)}}{100} = \frac{1.491}{100} = 0.01491\ \text{V} \tag{2.47}$$

$$r_{C(\max)} = \frac{V_r}{\Delta i_{L(\max)}} = \frac{0.01491}{0.478} = 31.12\ \text{m}\Omega \tag{2.48}$$

$$r_{C(\max)} = \frac{\Delta v_O}{\Delta i_O} = \frac{V_{nom} - V_{\min}}{i_{L(\max)} - i_{L(\min)}} = \frac{\left(1.476 - 1.461\right)}{\left(10 - 0.5\right)} = 1.579\ \text{m}\Omega \tag{2.49}$$

$$C_{(\min)} = \max\left\{\frac{D_{(\max)}}{2 f_S r_C}, \frac{1 - D_{(\min)}}{2 f_S r_C}\right\} = \max\left\{305\ \mu\text{F}, 1320\ \mu\text{F}\right\} = 1320\ \mu\text{F} \tag{2.50}$$

$$C = 470\ \mu\text{F} / 0.01\,\Omega / 4\ \text{V} \tag{2.51}$$

$$C = 3290\ \mu\text{F} / 1.4\ \text{m}\Omega / 4\ \text{V} \tag{2.52}$$

The power MOSFET and diode voltage and current stresses are (2.53) and (2.54). An International Rectifier IRF7475 power MOSFET is selected which has the characteristics given in (2.55)-(2.59). The diode was chosen to be an IRF85HFR which has the characteristics given in (2.60)-(2.63).

$$V_{SM(\max)} = V_{DM(\max)} = 1.491 \text{ V} \tag{2.53}$$

$$I_{SM(\max)} = I_{DM(\max)} = I_{O(\max)} + \frac{\Delta i_{L(\max)}}{2} = 10 + \frac{0.478}{2} = 10.239 \text{ A} \tag{2.54}$$

$$V_{DSS} = 12 \text{ V} \tag{2.55}$$

$$I_{SM} = 11 \text{ A} \tag{2.56}$$

$$r_{DS(ON)} = 0.015\ \Omega \tag{2.57}$$

$$Q_g = 19 \text{ nC} \tag{2.58}$$

$$C_O = 1310 \text{ pF} \tag{2.59}$$

$$I_{DM} = 40 \text{ A} \tag{2.60}$$

$$V_{DM} = 15 \text{ V} \tag{2.61}$$

$$V_F = 0.39 \text{ V} \tag{2.62}$$

$$R_F = 0.0\,15\ \Omega \tag{2.63}$$

The power losses and the efficiency are calculated at full load, and maximum input voltage which corresponds to the minimum duty cycle. The conduction power loss in the MOSFET is calculated by (2.64), and the switching loss is determined by (2.65). The total power loss in the MOSFET is (2.66).

$$P_{rDS} = D_{\min} r_{DS} I_{O(\max)}^2 = 0.166 \times 0.015 \times 10^2 = 0.249 \text{ W} \tag{2.64}$$

$$P_{SW} = f_S C_O V_{I(\max)}^2 = \left(200 \times 10^3\right)\left(1310 \times 10^{-12}\right) \times 12.6^2 = 0.042 \text{ W} \tag{2.65}$$

$$P_{FET} = P_{rDS} + \frac{P_{SW}}{2} = 0.249 + \frac{0.042}{2} = 0.270 \text{ W} \tag{2.66}$$

The diode loss due to the forward voltage is determined by (2.67) and the diode loss due to the forward resistance is (2.68). The total conduction loss due to the power diode is (2.69).

$$P_{VF} = (1 - D_{\min}) V_F I_{O(\max)} = (1 - 0.166) \times 0.39 \times 10 = 3.253 \text{ W} \tag{2.67}$$

$$P_{RF} = (1 - D_{\min}) R_F I_{O(\max)}^2 = (1 - 0.166) \times 0.015 \times 10^2 = 1.251 \text{ W} \tag{2.68}$$

$$P_D = P_{VF} + P_{RF} = 3.253 + 1.251 = 4.504 \text{ W} \tag{2.69}$$

The power loss in the inductor ESR is given by (2.70). The power loss in the capacitor ESR is expressed by (2.71). The total power loss due to the MOSFET, diode, inductor, and capacitor is (2.72), and the efficiency of the converter at full load is expressed by (2.73).

$$P_{rL} = r_L I_{O(\max)}^2 = (9 \times 10^{-3}) \times 10^2 = 0.90 \text{ W} \tag{2.70}$$

$$P_{rC} = \frac{r_C (\Delta i_{L(\max)})^2}{12} = \frac{0.0014 \times 0.478^2}{12} = 0.027 \text{ mW} \tag{2.71}$$

$$P_{LS} = P_{rDS} + P_{SW} + P_D + P_{rL} + P_{rC} = 5.695 \text{ W} \tag{2.72}$$

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{1.491 \times 10}{1.491 \times 10 + 5.695} = \frac{14.91}{14.91 + 5.695} = 72.36\,\% \tag{2.73}$$

Table 2.2 provides a summary of the circuit components and parameters for the PWM Buck Converter to comply with the requirements of Table 2.1. The value of *r* was determined using (2.2).

Parameter	Value	Unit
L	13	µH
r_L	0.009	Ω
C	3290	µF
r_C	0.0014	Ω
r_{DS}	0.015	Ω
R_F	0.015	Ω
V_F	0.39	V
Dnom	0.180	NA
r	0.024	Ω

Table 2.2: Buck Converter components

The transfer function of the output filter for the buck converter is given by (2.74). Fig. 2.4 and Fig. 2.5 provide the frequency response of the output filter. The transfer function has an attenuation of (2.75), a pair of complex poles at (2.76), and a zero at (2.77). The damping ratio is (2.78). The frequency response rolls off at -20 dB/decade at high frequency with a phase shift of -90º.

$$G_{psf}(s) = \frac{106.7\left(s + 2.17\times10^{5}\right)}{s^{2} + 4.015\times10^{3}\,s + 2.697\times10^{7}} \tag{2.74}$$

$$G_{psf}(0) = 0.8587 = -1.32 \text{ dB} \tag{2.75}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{R_L + r}{LC\left(R_L + r_C\right)}} = 826.47 \text{ Hz} \tag{2.76}$$

$$f_z = \frac{1}{2\pi C r_C} = 3.45\times10^{4} \text{ Hz} \tag{2.77}$$

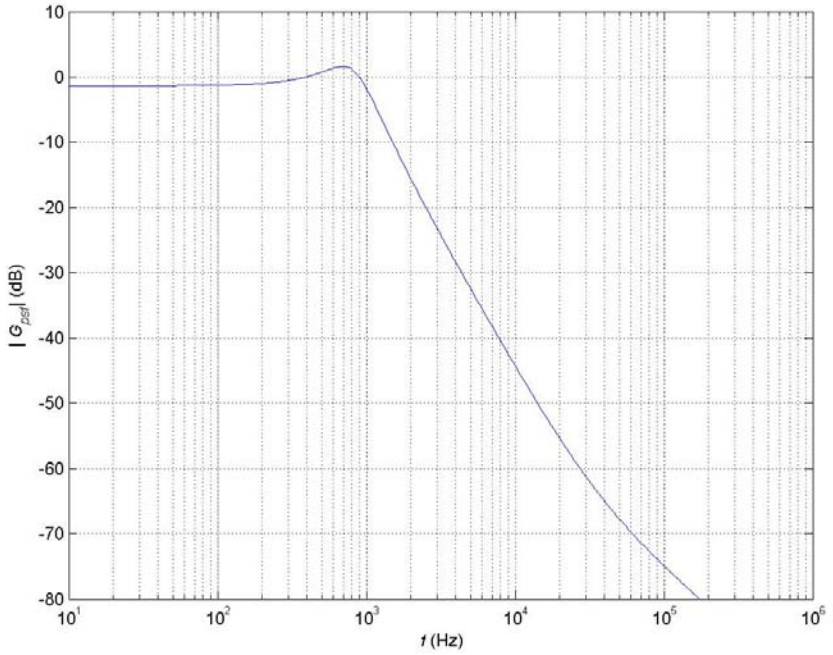

Figure 2.4: Magnitude of the output filter, G_{psf}, with R_L = 0.146 Ω, and r = 0.024 Ω

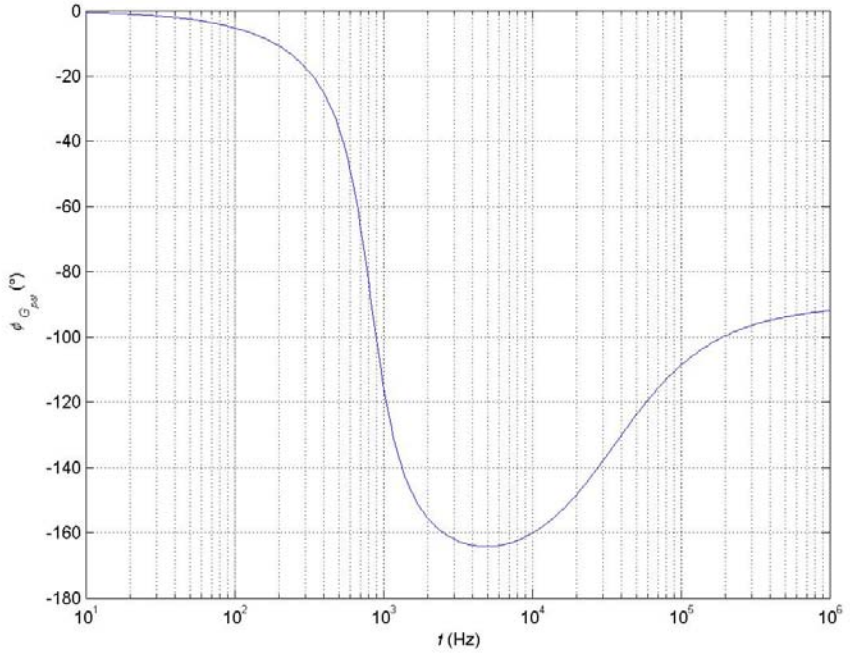

Figure 2.5: Phase of the output filter, G_{psf}, with R_L = 0.146 Ω and r = 0.024 Ω

$$\xi = 0.3866 \tag{2.78}$$

The duty cycle-to-output transfer function is expressed by (2.79). The transfer function has the same zero, poles, and damping ratio as the output filter. The dc gain is given by (2.80). Fig. 2.6 provides the magnitude response of the transfer function. The phase response is identical to that of the output filter.

$$T_P(s) = \frac{1280\left(s + 2.171\times10^5\right)}{s^2 + 4.015\times10^3 s + 2.697\times10^7} \tag{2.79}$$

$$T_p(0) = 10.30 \text{ V} = 20.25 \text{ dBV} \tag{2.80}$$

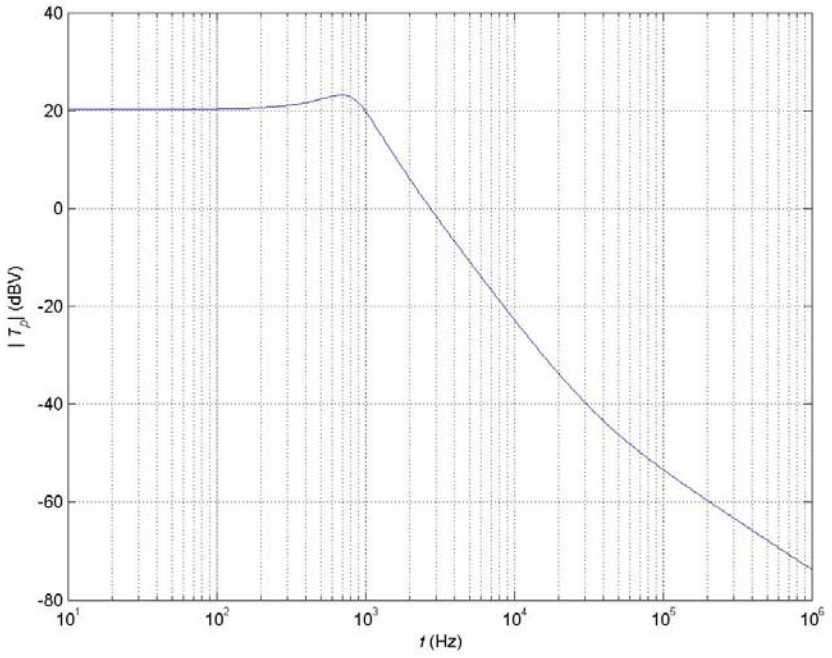

Figure 2.6: Magnitude response of the control-to-output transfer function, T_p, with V_I = 12 V, R_L = 0.146, and r = 0.024 Ω

The input to output transfer function is (2.81). Once again, the transfer function has the same zero, poles, and damping ratio as the output filter. The dc gain is given by (2.82). Fig. 2.7 provides the magnitude response of the transfer function. The phase response is identical to that of the output filter.

$$M_v(s) = \frac{19.2\left(s + 2.171\times10^5\right)}{s^2 + 4.015\times10^3 s + 2.697\times10^7} \tag{2.81}$$

$$M_v(0) = 0.1548 = -16.20 \text{ dB} \tag{2.82}$$

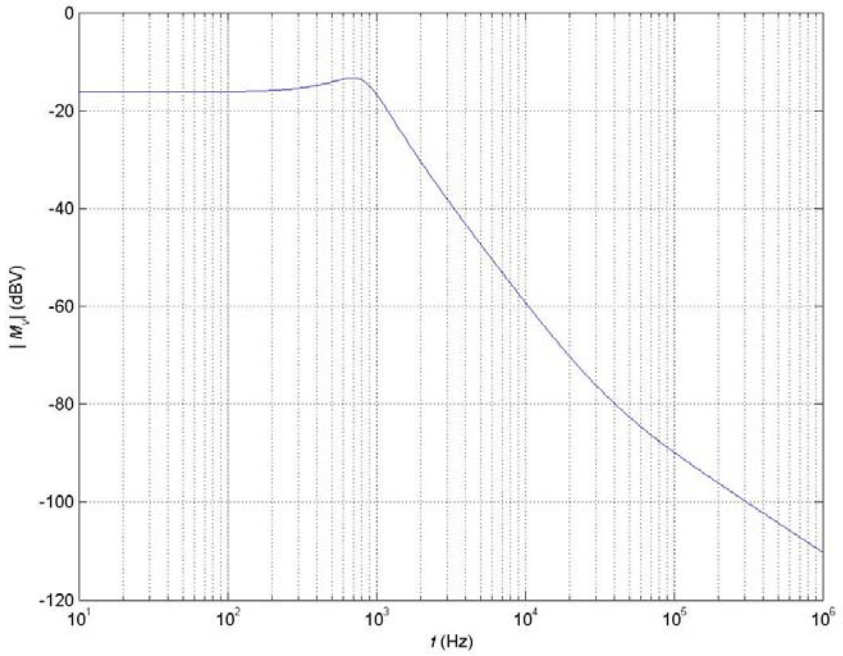

Figure 2.7: Magnitude response of the input-to-output transfer function, M_v, with R_L = 0.146 Ω, r = 0.024 Ω and D = 0.180

Equation (2.83) provides the transfer function of the open-loop input impedance. It has a pair of complex zeros at the same frequency at which the output filter had a pair of complex poles. The transfer function has a pole at (2.84). The dc input impedance is given by (2.85). Figures 2.8 through Fig. 2.10 provide the magnitude and phase response of the input impedance. The input impedance increases at +20 dB/decade at high frequency.

$$Z_i(s) = \frac{4.012\times10^{-4}\left(s^2 + 4.015\times10^3 s + 2.697\times10^7\right)}{s + 2.062\times10^3} \tag{2.83}$$

$$f_{cr} = \frac{1}{2\pi C\left(R_L + r_C\right)} = 328 \text{ Hz} \tag{2.84}$$

$$Z_i(0) = 5.24\ \Omega = 14.38\ \text{dB}\Omega \tag{2.85}$$

The transfer function of the open-loop output impedance for the given example is expressed by (2.86). Fig. 2.11 through Fig. 2.13 provides the frequency response of the output impedance. The output impedance has the same poles as the output filter, with zeros at (2.87) and (2.88). The dc output impedance is given by (2.89) and the resistance at high frequency is given by (2.90), which is approximately equal to r_C.

$$Z_o(s) = \frac{1.387 \times 10^{-3}\left(s^2 + 2.189 \times 10^5 s + 4.007 \times 10^8\right)}{s^2 + 4.015 \times 10^3 s + 2.697 \times 10^7} \tag{2.86}$$

$$f_z = \frac{1}{2\pi C r_C} = 3.386x10^4\ \text{Hz} \tag{2.87}$$

$$f_{rl} = \frac{r}{2\pi L} = 294.43\ \text{Hz} \tag{2.88}$$

$$Z_o(0) = 0.02\ \Omega = -33.98\ \text{dB}\Omega \tag{2.89}$$

$$Z_o(\infty) = 0.0014\ \Omega = -57.07\ \text{dB}\Omega \tag{2.90}$$

Now consider the response of the output voltage to a step change in input voltage. Suppose there is a step change in the input voltage of magnitude ΔV_I at a time $t = 0$ for fixed duty cycle and load resistance. The total input voltage is given by input (2.91), where $u(t)$ is the unit step function, ΔV_I is the size of the step change in voltage, and $V_I(0^-)$ is the steady state input voltage (dc) before the step change in voltage. The step change in voltage expressed in the s-domain is (2.92). The output voltage in the s-domain is expressed by (2.93), and the output voltage in the time domain is obtained using the inverse Laplace transform (2.94). The output voltage is equal to the initial output voltage plus the change due to the step input.

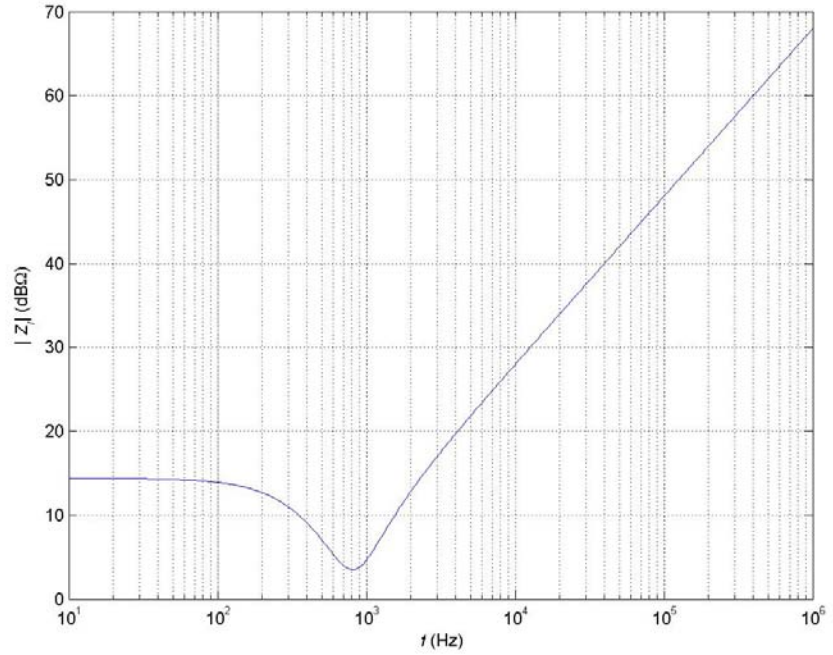

Figure 2.8: Magnitude of open-loop input impedance, Z_i, with R_L = 0.146 Ω, D = 0.180, and r = 0.024 Ω

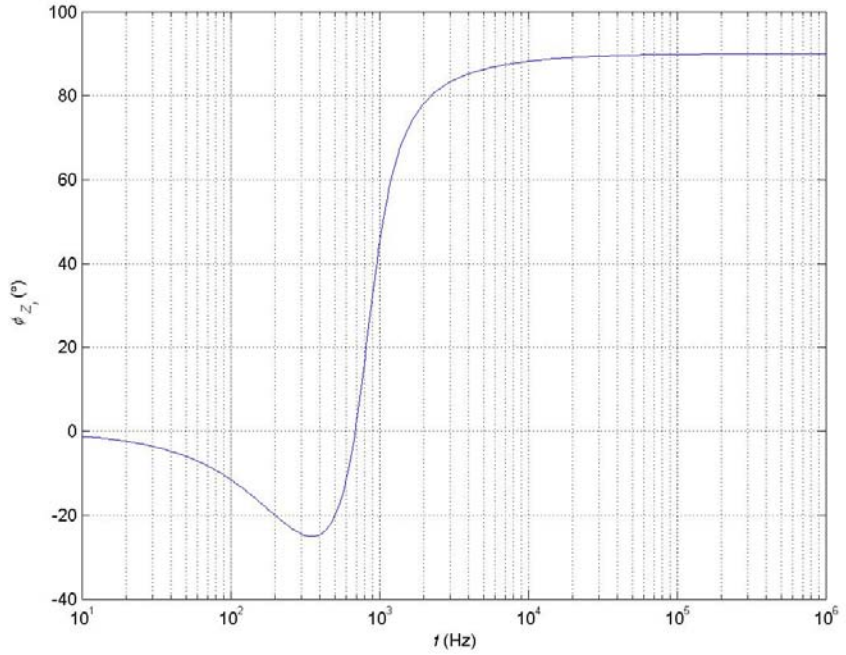

Figure 2.9: Phase of open-loop input impedance, Z_i, with R_L = 0.146 Ω, D = 0.180, and r = 0.024 Ω

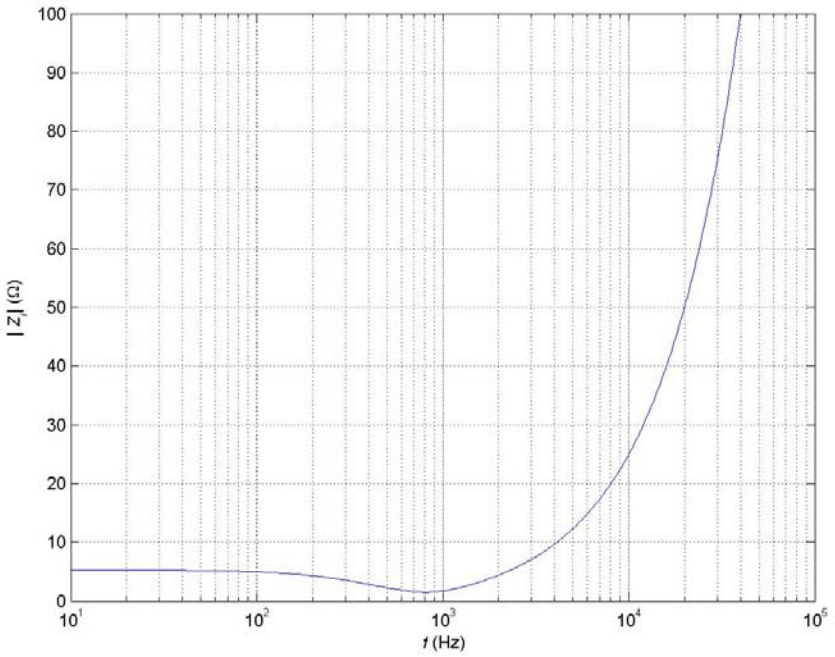

Figure 2.10: Magnitude of open-loop input impedance, Z_i, with R_L = 0.146 Ω, D = 0.180, and r = 0.024 Ω

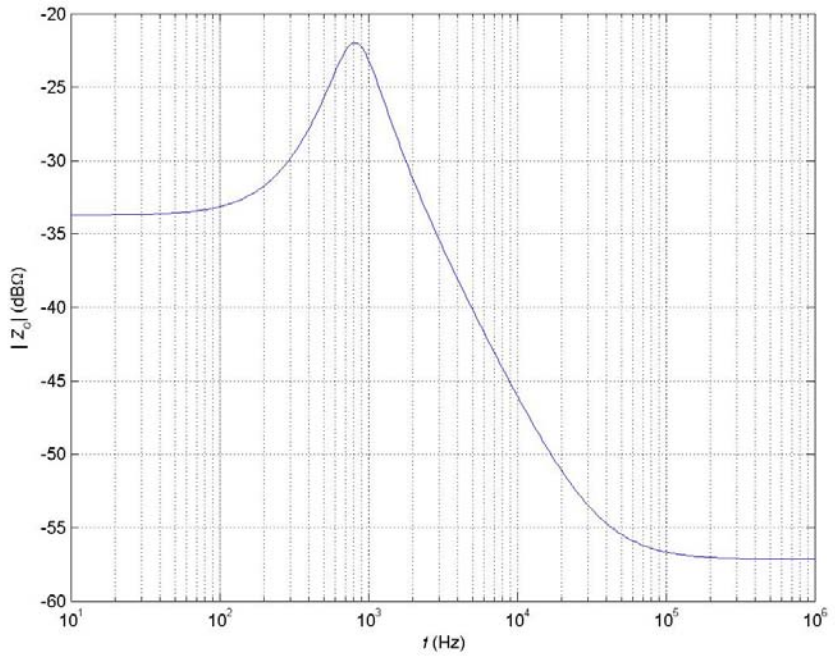

Figure 2.11: Magnitude of open-loop output impedance, Z_o, with R_L = 0.146 Ω, and r = 0.024 Ω

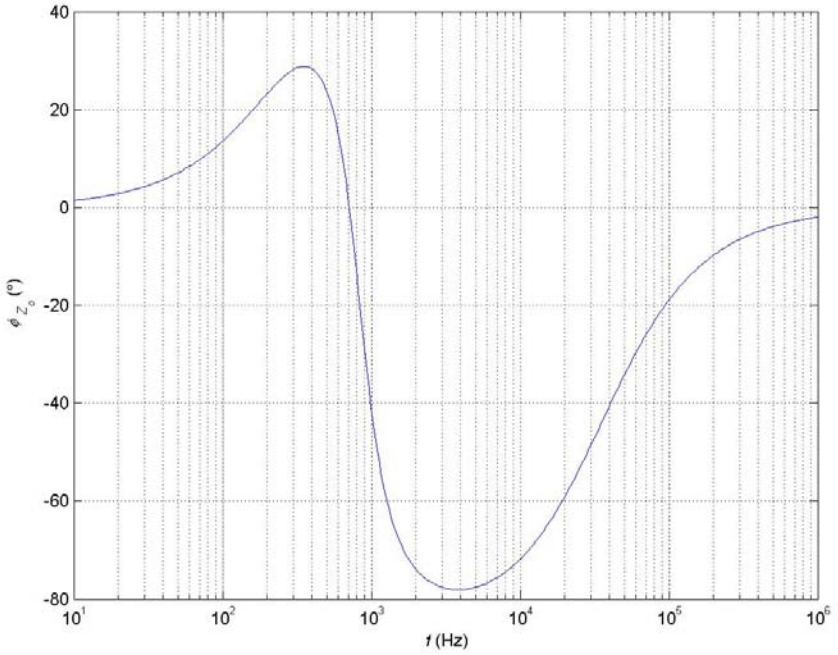

Figure 2.12: Phase of open-loop output impedance, Z_o, with R_L = 0.146 Ω, and r = 0.024 Ω

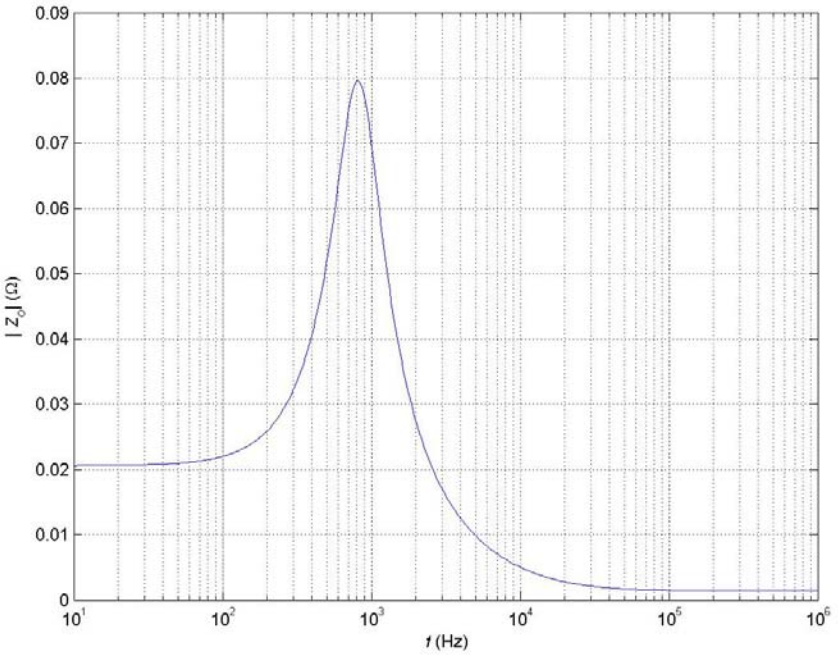

Figure 2.13: Magnitude of open-loop output impedance, Z_o, with R_L = 0.146 Ω, and r = 0.024 Ω

$$v_I(t) = V_I(0^-) + \Delta V_I u(t) \tag{2.91}$$

$$v_i(s) = \frac{\Delta V_I}{s} \tag{2.92}$$

$$v_o(s) = M_v(s) v_i(s) = M_v(s) \frac{\Delta V_I}{s} \tag{2.93}$$

$$v_o(t) = \mathcal{L}^{-1}\{v_o(s)\} = v_O(0^-) + v_o(t) \tag{2.94}$$

The open-loop step response of the output voltage to a 0.6 V change in input voltage (12.0 V to 12.6 V) is shown in Fig. 2.14. The output voltage starts at the nominal voltage than rises to a peak of 1.594 V before settling at 1.569 V around 2.5 ms. The open-loop step response of the output voltage to a 0.1 change in duty cycle is shown in Fig. 2.15.

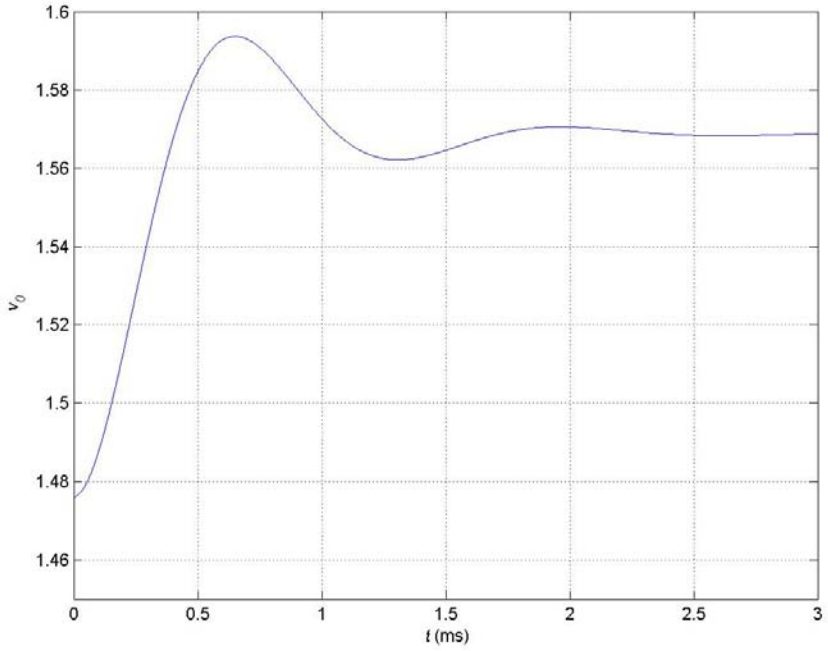

Figure 2.14: Open-loop step response of output voltage, v_O, to a change in input voltage from 12.0 to 12.6 V with R_L = 0.146 Ω, and D = 0.180

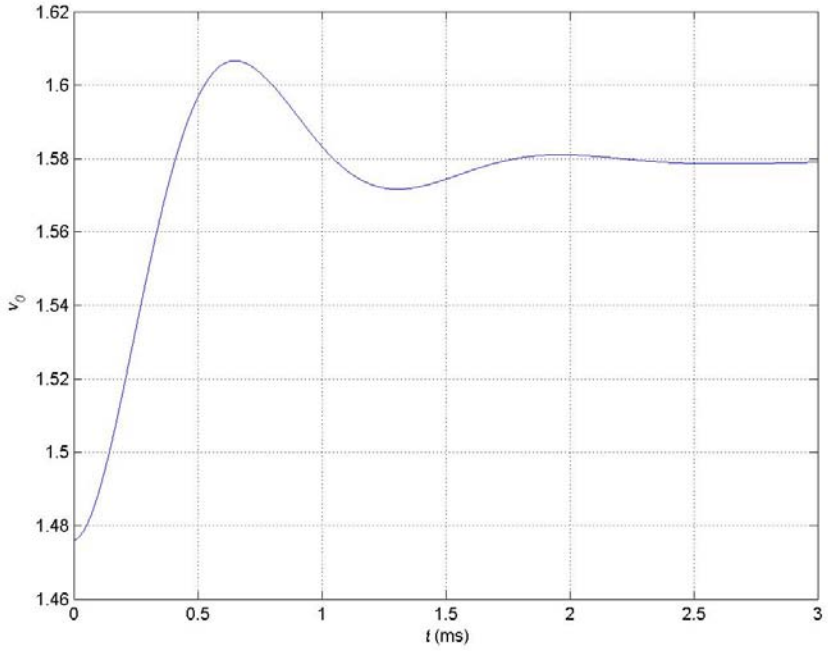

Figure 2.15: Open-loop step response of output voltage, v_O, to a step change in duty cycle from 0.180 to 0.190 with V_I = 12 V, and R_L = 0.146 Ω

The output voltage starts at the nominal voltage than rises to a peak of 1.607 V before settling at 1.579 V around 2.5 ms.

The open-loop step response of the output voltage to a 9.5 A change in load current is presented in Fig. 2.16. The output voltage initially drops from the nominal voltage of 1.476 V to 1.463 V due to the product of the current step and r_C which is -0.0133 V. The output voltage falls to a minimum value of 1.014 V before settling at 1.279 V around 2.5 ms. Each step response showed the open-loop system does not stay within the specified tolerance of the output voltage.

This section introduced a small-signal linear model for the highly nonlinear PWM Buck Converter. The transfer functions for the various components of the open-loop system were provided along with a typical example to provide some insight of the

frequency response and the dynamic behavior of the open-loop system. The time responses showed the open-loop system is incapable of maintaining a constant output

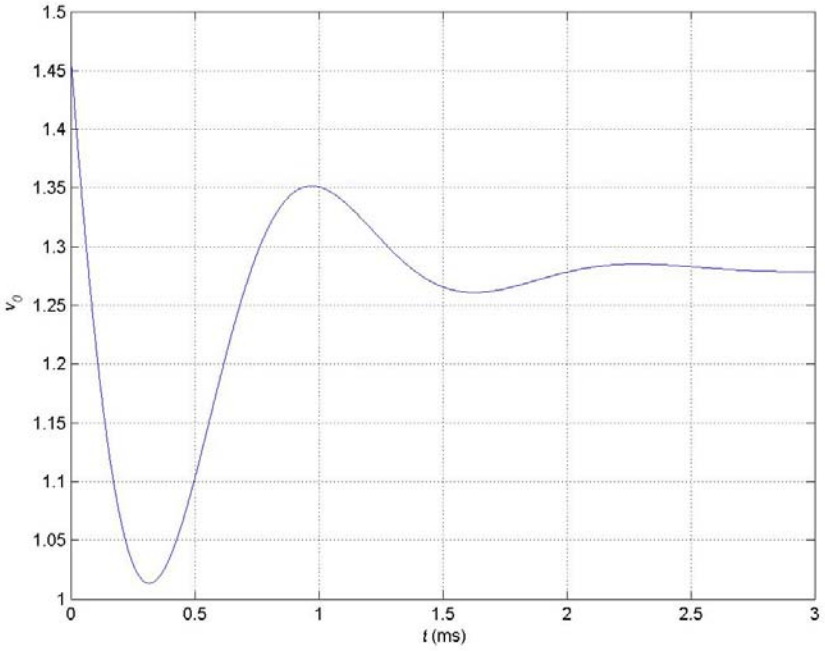

Figure 2.16: Open-loop step response of output voltage, v_O, to a step change in the load current from 0.5 to 10 A with V_I = 12 V, and D = 0.180

voltage when a disturbance is introduced. A closed-loop system can improve the responsiveness or rejection of a disturbance and maintain the desired output voltage within a tight tolerance. The next section presents a common industry method for designing the closed-loop system.

2.3 Classical Control Theory for Compensator Design

In classical control theory, the closed-loop system stability is determined by the gain and phase margin. The designer makes a bode plot of the loop gain and adjusts the gain, poles, and zeros of the compensator to achieve the gain and phase margin that makes the closed-loop system response comply with the system requirements. Fig. 2.17 shows a block diagram of the PWM Buck converter. In the figure, the loop gain is expressed by

(2.95), where T_C is the compensator (2.96), T_m is the transfer function of the pulse-width modulator (2.97), and β is the voltage transfer function of the feedback network (2.98). In the figure, v_f represents the ac feedback signal and v_e represents the ac error signal. The figure shows the converter is a multivariable system with three inputs, v_{ref}, v_i, and i_o which are considered to be disturbances. Applying superposition, one obtains the ac component of the output voltage (2.99) [22].

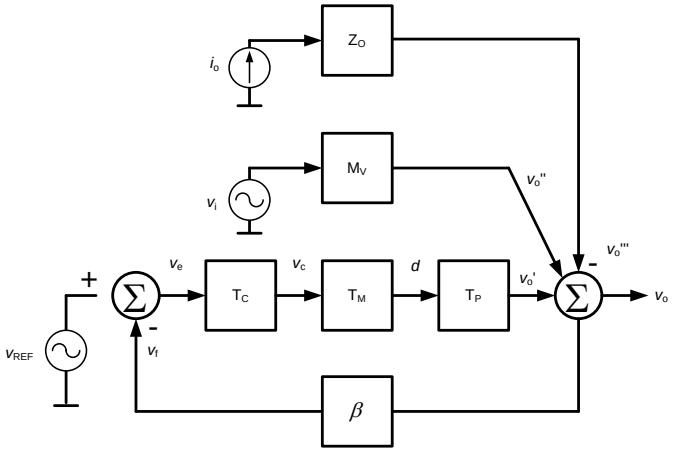

Figure 2.17: Block diagram of PWM Buck Converter using linear small-signal model

$$T(s) \equiv \frac{v_f(s)}{v_e(s)}\Big|_{v_i = i_o = 0} = T_C(s) T_M T_P(s) \beta \tag{2.95}$$

$$T_C(s) \equiv \frac{v_c(s)}{v_e(s)} \tag{2.96}$$

$$T_M \equiv \frac{d}{v_c} = \frac{1}{V_{TM}} \tag{2.97}$$

$$\beta = \frac{R_B}{R_A + R_B} \tag{2.98}$$

$$v_o(s) = \frac{M_v(s)}{1 + T(s)} v_i(s) + \frac{A(s)}{1 + T(s)} v_{ref}(s) + \frac{Z_o(s)}{1 + T(s)} i_o(s) \tag{2.99}$$

The closed-loop transfer functions relating the output voltage to the three input sources are expressed by (2.100)-(2.103) [22]. The transfer functions show that negative feedback reduces the closed-loop audio susceptibility, susceptibility to reference voltage change, and the output impedance by a factor of (1 + |*T*|). Typically the loop gain decreases with increasing frequency, reducing its effect on high frequency to the point where the open and closed-loop frequency responses become identical.

$$M_{vcl}(s) = \frac{M_v(s)}{1 + T(s)} \tag{2.100}$$

$$A_{cl}(s) = \frac{A(s)}{1 + T(s)} \tag{2.101}$$

$$Z_{ocl}(s) = \frac{Z_o(s)}{1 + T(s)} \tag{2.102}$$

$$A(s) \equiv \frac{v_o'(s)}{v_e(s)} = T_C(s) T_M T_P(s) \tag{2.103}$$

There are two types of compensators that are typically used by industry electrical engineers to stabilize the converter [11]. These compensators are referred to as Type-II and Type-III networks due to the shape of their bode plot. The transfer function for a Type-II compensator is given by (2.104). The Bode plot of the Type-II compensator is provided in Fig. 2.18. Type-II compensation gets its name from the fact that the Bode magnitude plot has two diagonal slopes [11]. It can be seen that the Type-II compensator extends the bandwidth without increasing the loop phase. Therefore this compensation method may be used if the phase margin of the open loop system is greater than the desired loop phase margin at the desired crossover frequency. It should be mentioned that if the phase margin of the loop gain exceeds the requirement by 90º, then a simple

integrator with a gain may be used as the compensator. This is a Type-I compensation network.

$$T_{C-II}(s) = \frac{sA_1 + 1}{s(sA_2 + 1)} \tag{2.104}$$

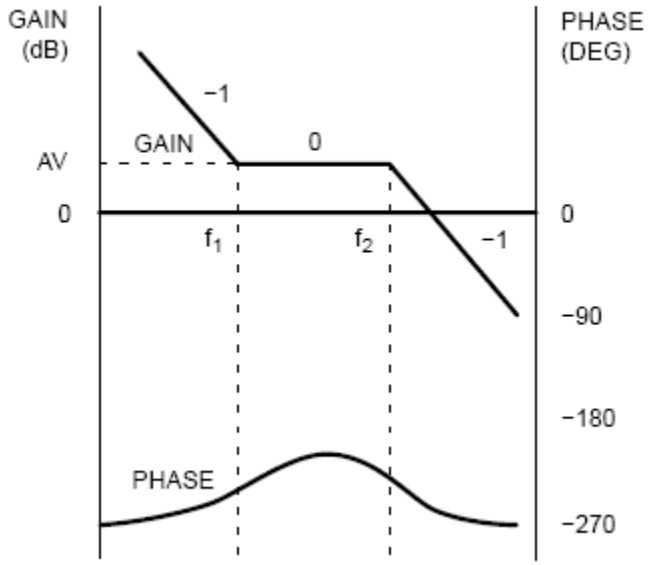

Figure 2.18: Type-II compensator frequency response

The transfer function for a Type-III compensator is given by (2.105). The Bode plot of the Type-III compensator is provided in Fig. 2.19. Type-III compensation gets its name from the fact that the Bode magnitude plot has three diagonal slopes [11]. It can be seen that the Type-III compensator extends the bandwidth and increases the loop phase. Therefore this compensation method may be used if the phase margin of the open loop system is less than the closed loop phase margin at the desired crossover frequency.

$$T_{C-III}(s) = \frac{(sA_1 + 1)(sA_2 + 1)}{s(sA_3 + 1)(sA_4 + 1)} \tag{2.105}$$

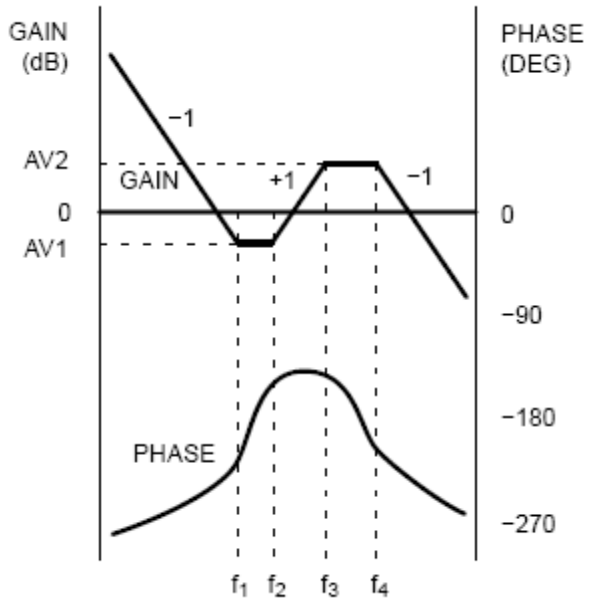

Figure 2.19: Type-III compensator frequency response

The following steps are the general guide used by industry to select and design the compensator for the converter. The output impedance is set by the ESR of the output capacitance. The focus is to design the loop gain to provide a specific phase margin. Prior to these steps, the ESR of the output capacitor needs to be selected so the spike due to a step change in load does not cause the output voltage to exceed its specifications.

1. Plot the loop gain without the compensator.
2. Select the type of compensator through analysis of the phase margin at the desired crossover frequency.
3. Design the transfer function of the compensator.
4. Plot the loop gain with the compensator to confirm proper phase margin is achieved.
5. Simulate the closed-loop response to verify compliance with requirements.

These steps should be iterated until a suitable solution is reached. As a rule of thumb, the phase margin is typically 45º to 90º, however 52º is preferable at the desired crossover frequency which is typically $1/5^{th}$ to $1/10^{th}$ the switching frequency [11].

To demonstrate the method, consider the design example using the requirements stated in Table 2.3. These are the same requirements expressed in Table 2.1 with the added requirement for bandwidth and phase margin. Therefore, the components selected in the previous section are sufficient to satisfy the requirements.

Parameter	Max	Nominal	Min
Input Voltage, V_I (V)	12.60	12.00	11.04
Output Voltage, V_O (V)	1.491	1.476	1.461
Output Current, I_O (A)	10	5.25	0.5
Output Current Slew Rate, I_O (A/μs)			50
Switching frequency, f_S (A)	198	200	202
Ripple Voltage (%)	1		0
Efficiency, η (%)			70
Loop BW (kHz)			60
Loop Phase Margin (Deg)			52

Table 2.3: PWM Buck Converter specifications

To complete the closed loop design, the values of the reference voltage, voltage divider, and modulator gain need to be selected. The reference voltage should be about half the value of the output voltage, therefore, select a reference voltage of 0.8 V. The voltage divider is determined by (2.106). The modulator signal will be created by comparing the compensator output voltage to the voltage of a saw-tooth waveform. If the

error voltage is above the reference voltage, the modulator will decrease the duty cycle of the modulator output, and if the error voltage is less than the reference voltage, the modulator will increase the duty cycle of the modulator output. The modulator gain is determined using (2.107) and (2.108), where V_{Tm} is the magnitude of the saw-tooth waveform. Pick T_m to be 0.2. The cross-over frequency is set to 60 kHz in order to be greater than the critical frequency, f_C, (2.109).

$$\beta = \frac{v_{REF}}{v_{O(nom)}} = \frac{0.8}{1.476} = 0.5420 \tag{2.106}$$

$$V_{Tm} \approx \frac{v_{REF}}{D_{nom}} = \frac{0.8}{0.1802} = 4.43 \text{ V} \tag{2.107}$$

$$T_m = \frac{1}{5} = 0.2 \text{ V}^{-1} \tag{2.108}$$

$$f_C = \frac{1}{4r_C C} = \frac{1}{4 \times 0.0014 \times \left(3200 \times 10^{-6}\right)} = 55.80 \times 10^3 \text{ Hz} \tag{2.109}$$

The frequency response of the loop gain without compensation, T_{WOC}, is shown in Fig. 2.20 and Fig. 2.21. The phase margin at the cross-over frequency is measured to be 60.6º. Since the phase margin meets the requirement, the Type-II compensator will be applied. The transfer function of the compensator, T_C, is given by (2.110). The zero was set at a frequency of 1/15th that of the cross-over frequency, and the pole was set at 15x the cross-over frequency. The gain was set in order to make the loop gain equal to 0 dB at the cross-over frequency. Fig. 2.22 and Fig. 2.23 provide the frequency response of the Type-II compensator. The frequency response of the loop gain is shown in Fig. 2.24 and Fig. 2.25. The loop gain has a phase margin of 53º, which complies with the given requirements.

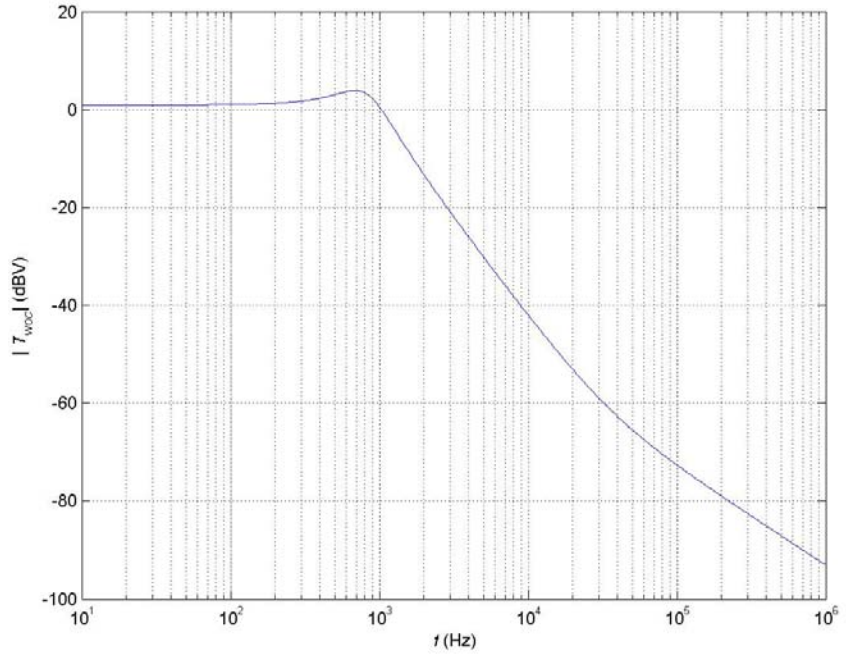

Figure 2.20: Magnitude of loop gain without compensation with V_I = 12 V and R_L = 0.146 Ω

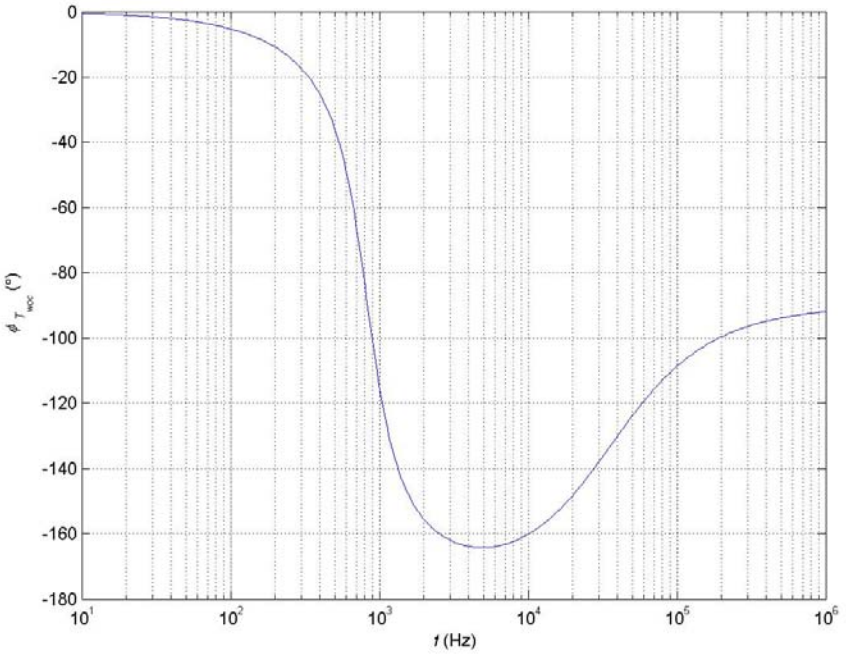

Figure 2.21: Phase of loop gain without compensation with V_I = 12 V and R_L = 0.146 Ω

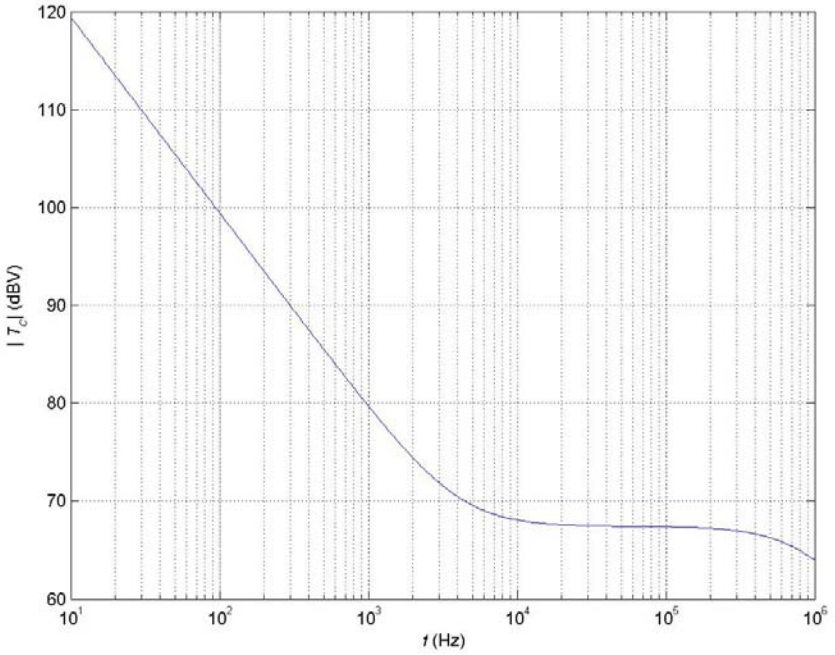

Figure 2.22: Magnitude of the compensator, T_c

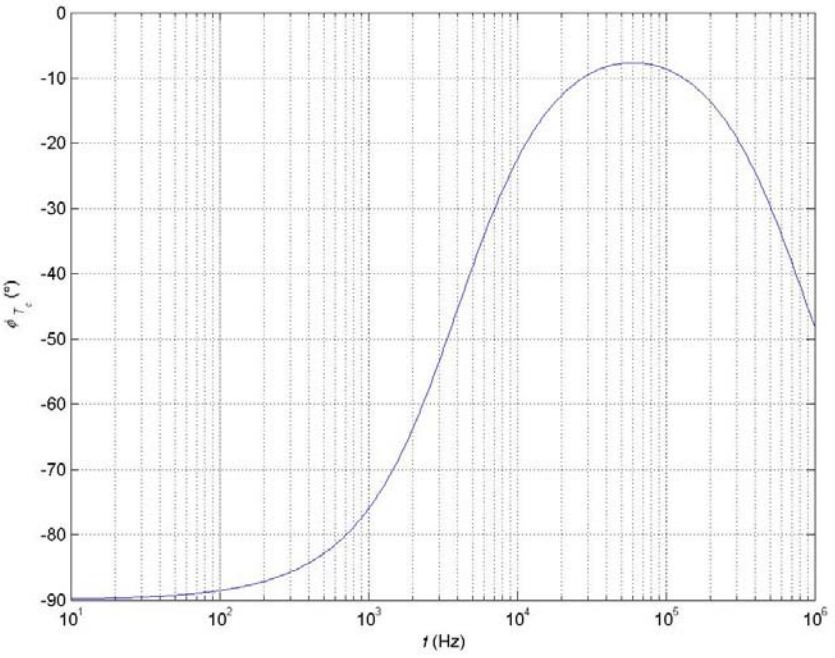

Figure 2.23: Phase of the compensator, T_c

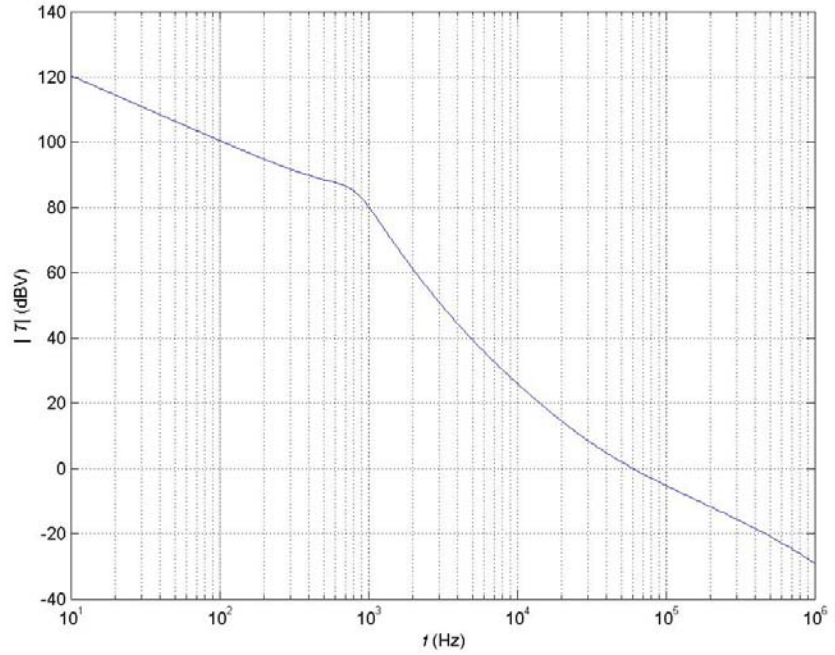

Figure 2.24: Magnitude of loop gain with compensator for V_I = 12 V and R_L = 0.146 Ω

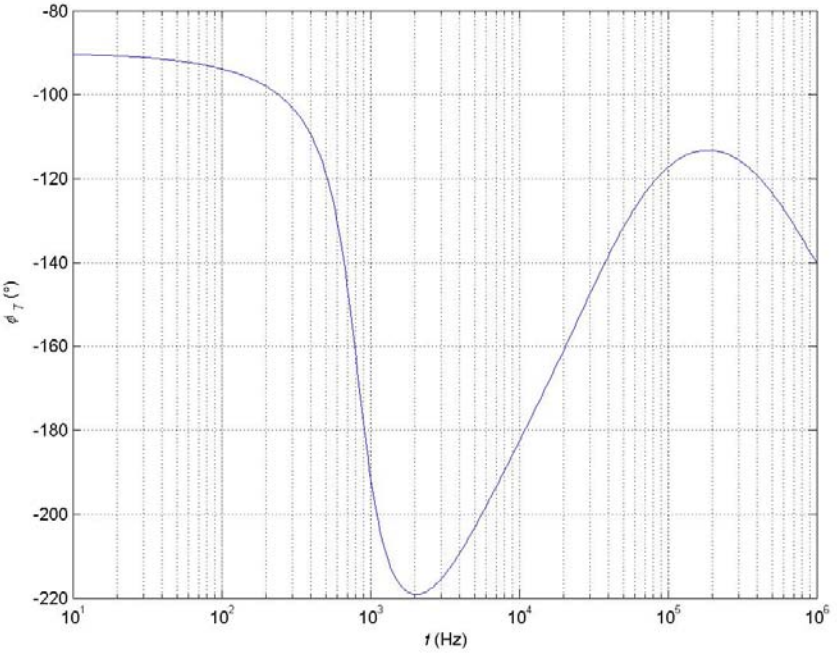

Figure 2.25: Phase of loop gain with compensator for V_I = 12 V and R_L = 0.146 Ω

$$T_C(s) \equiv \frac{1.329 \times 10^{10}\left(s + 2.51 \times 10^{4}\right)}{s\left(s + 5.655 \times 10^{6}\right)} \tag{2.110}$$

Fig. 2.26 and Fig. 2.27 show the frequency response of the closed-loop input-to-output transfer function of the Buck converter. Comparing this response to that of the open-loop shown in Fig. 2.14, shows the loop gain has a large affect at low frequency and an insignificant effect at high frequency where the frequency response is the same as the open-loop response.

Fig. 2.28 through Fig. 2.30 provide the frequency response of the closed-loop output impedance. The loop gain has little effect at high frequency, but significantly reduces the output impedance at low frequency. An ideal voltage source is a circuit element where the voltage across it is independent of the current through it. The output impedance of an ideal voltage source is zero; it is able to supply or absorb any amount of current. The frequency response shows that the loop gain helps to make the Buck converter behave like an ideal voltage source at low frequency.

The step response of the closed-loop Buck converter to a 0.6 V disturbance is presented in Fig. 2.31. The output voltage stays within the required tolerance during the disturbance and returns to the nominal output voltage after 0.2 ms.

Fig. 2.32 provides the response of the output voltage due to a step change in load current. After an initial deviation due to r_C, the response returns to the nominal output voltage after approximately 0.05 ms. Note that since the system bandwidth is greater than the critical frequency, the voltage does not deviate more than the initial spike due to r_C. The closed-loop response to a step change in load complies with the requirements of the output voltage to confirm compliance with the design specifications.

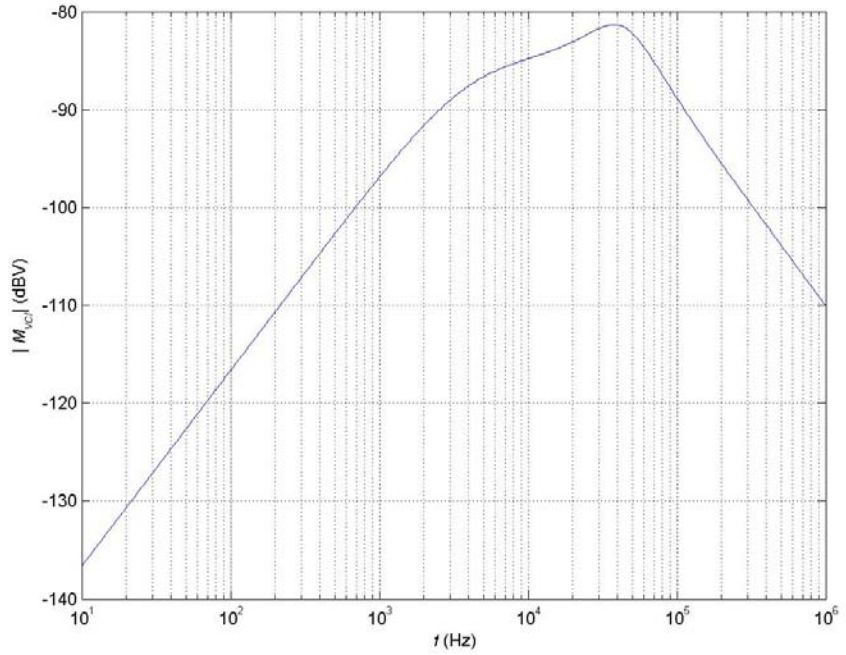

Figure 2.26: Magnitude of compensated closed-loop input-to-output transfer function, M_{vcl}, of the converter with R_L = 0.1463 Ω

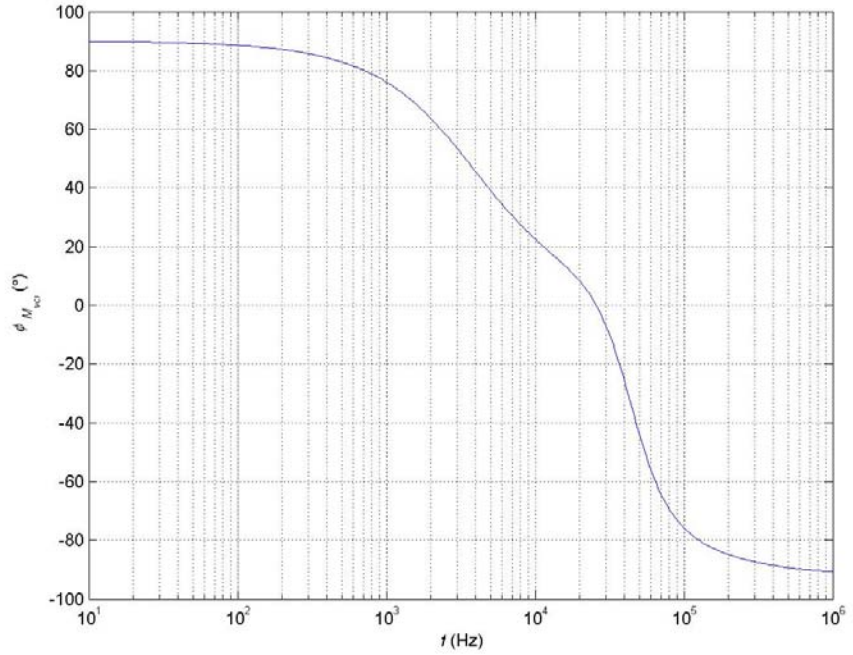

Figure 2.27: Phase of compensated closed-loop input-to-output transfer function, M_{vcl}, of the converter with R_L = 0.146 Ω

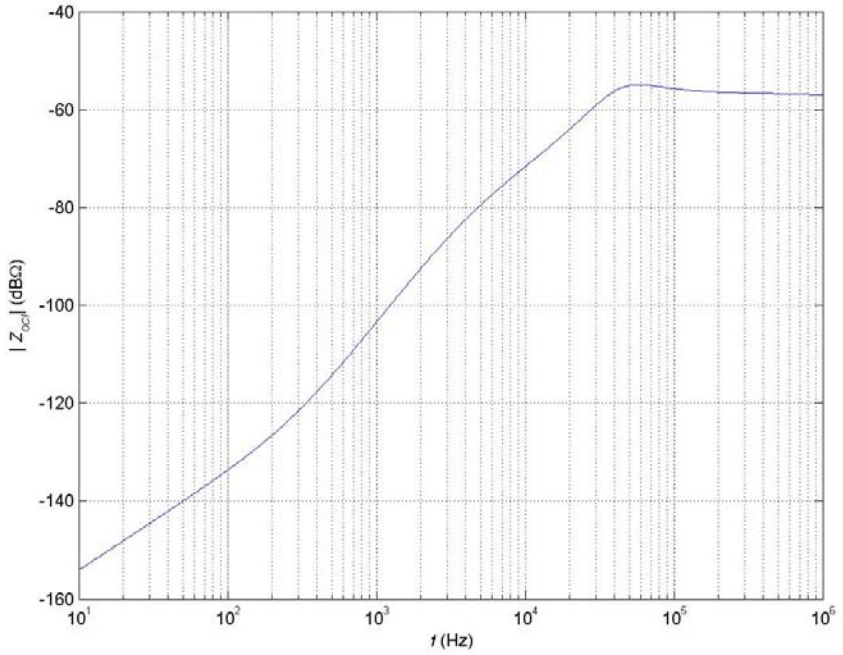

Figure 2.28: Magnitude of compensated closed-loop output impedance, Z_{ocl}, with R_L = 0.146 Ω

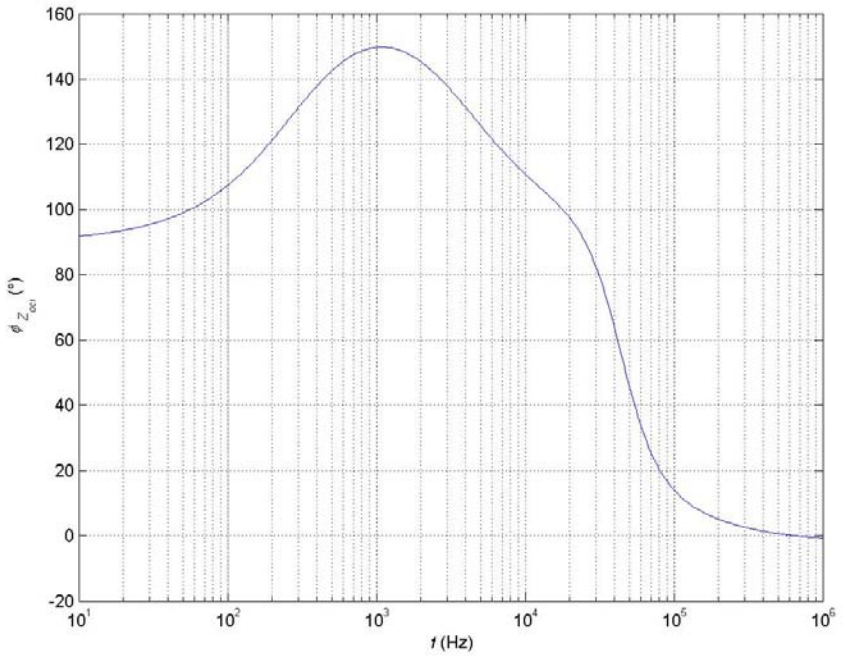

Figure 2.29: Magnitude of compensated closed-loop output impedance, Z_{ocl}, with R_L = 0.146 Ω

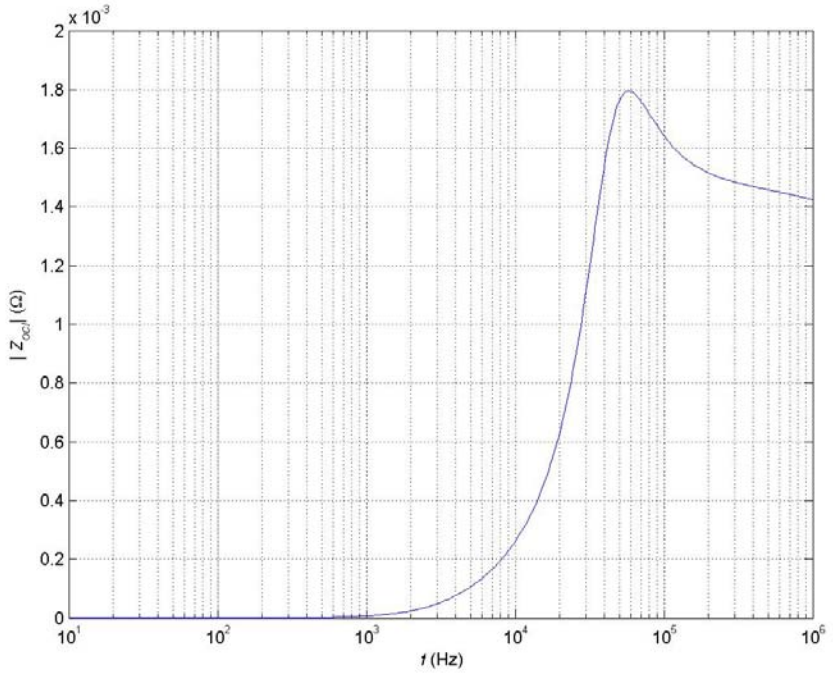

Figure 2.30: Magnitude of compensated closed-loop output impedance, Z_{ocl}, with R_L = 0.146 Ω

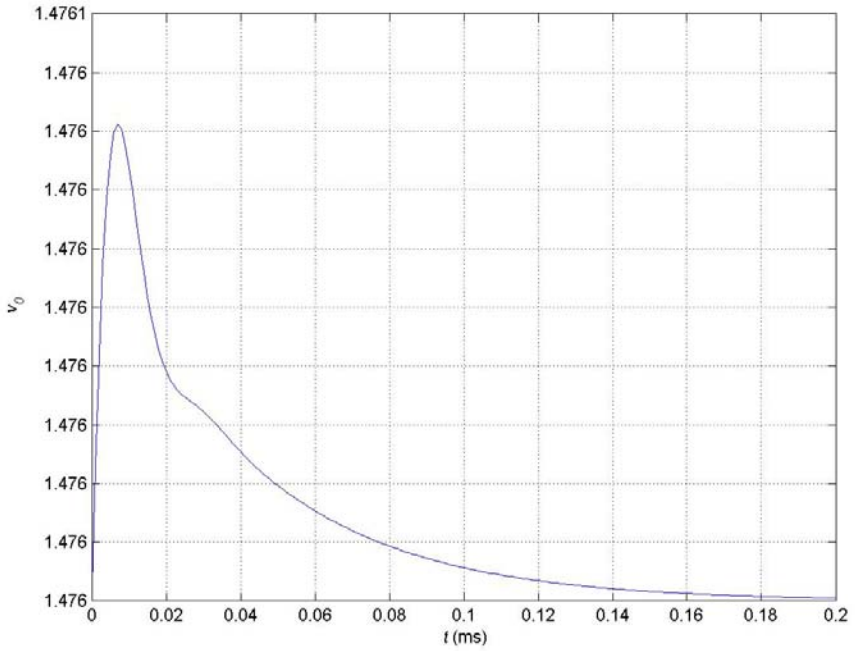

Figure 2.31: Closed-loop step response of v_o to a step change in input voltage from 12 to 12.6 *V* for the closed-loop converter with R_L = 0.146 Ω

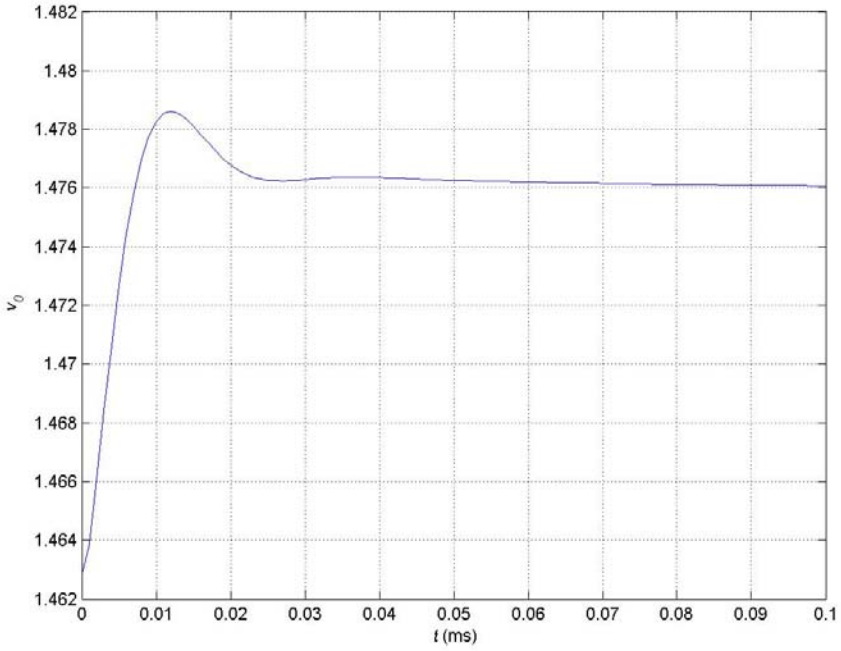

Figure 2.32: Closed-loop step response of v_o to a step change in the load current from 0.5 to 9.5 A for the closed-loop converter with V_I = 12 V and R_L = 0.146 Ω

If the phase margin of the loop gain without the compensator was less than the requirement, a Type-III compensator would have been applied to the design example. The Type-III compensator typically has a pair of complex zeros placed to eliminate the complex poles in the output filter of the power stage, G_{psf}. In this way, the compensator provides a notch that will eliminate the resonant peak. The compensator gain will be determined to achieve 0 dB at the cross over frequency.

This section presented the method of compensator design that is well known in industry. The method is useful; however, there is not a clear relationship between the phase margin and the requirements. The required phase margin is achieved through design iteration until the closed-loop system requirements are achieved through simulation. The output impedance is set by the ESR of the output capacitor. If low ESR

is required to comply with requirements, many parallel capacitors may be required. This solution can be expensive and use a lot of space on the circuit board.

Chatper 3 presents an alternative method to determine the loop gain in order to improve the response of the Buck converter to a change in load current.

3 An Alternate Method to Achieve the Desired Output Impedance

3.1 Introduction

The literature search presented in Chapter 2 showed the method commonly used in industry to design a PWM Buck converter. The non-linear elements were converted to a linear small-signal model to enable classical control theory to design the closed-loop system. Using the presented method, the design engineer uses a toolbox of compensator topologies, not knowing with certainty if the lowest cost solution has been selected. In addition, the designed does not know with certainty the loop gain that is required to achieve the closed-loop system requirements. The designer targets a phase margin based on experience, and iterates to either an acceptable solution or the best solution with minimal components. In addition, the closed-loop requirements are loosely tied to the phase margin at the cross-over frequency.

In the proposed method which will be presented in this chapter and demonstrated with examples in Chapters 4 and 5, the designer begins with the desired closed-loop frequency response and applies mathematics to determine the required loop gain. Then, knowing the loop gain, the designer can easily determine the exact compensator that achieves the design requirements. The resulting compensator, when included in the loop gain, will create the desired closed-loop frequency response that will make the closed-loop system satisfy the requirements of the dc-dc converter.

3.2 Proposed Approach to Determine Loop Gain and Compensator

The closed-loop output impedance is related to the loop gain, *T*, in the s-domain as given by (3.1). The terms of the output impedance, Z_{ocl}, can be rearranged to solve for the loop gain in terms of the open and closed-loop output impedance (3.2)-(3.4). The end goal here is to determine how to design a compensator that will achieve the closed-loop requirements. Given the loop gain, *T*, as expressed by (3.4), the compensator, T_C, can be determined by (3.5)-(3.6).

$$Z_{ocl}(s) = \frac{Z_o(s)}{1 + T(s)} \tag{3.1}$$

$$T(s) = \frac{Z_o(s)}{Z_{ocl}(s)} - 1 \tag{3.2}$$

$$T(s) = \frac{Z_o(s) - Z_{ocl}(s)}{Z_{ocl}(s)} \tag{3.3}$$

$$T(s) = T_C(s) T_M T_P(s) \beta \tag{3.4}$$

$$T_C(s) = \frac{Z_o(s) - Z_{ocl}(s)}{Z_{ocl}(s) T_M T_P(s) \beta} \tag{3.5}$$

$$T_C(s) = \frac{V_{TM}}{\beta}\left[\frac{Z_o(s) - Z_{ocl}(s)}{Z_{ocl}(s) T_P(s)}\right] \tag{3.6}$$

Now, let Z_{ocld} be the desired transfer function for the closed-loop output impedance whose time domain response to a step change in load satisfies a given set of requirements for the converter. So, to determine the compensator, replace Z_{ocl} in (3.6) with Z_{ocld} as shown in (3.7). Ideally Z_{ocld} would be zero across the frequency bandwidth. However, since that would require an infinite loop gain, it is not practical for synthesis. This approach is not limited by the designer's selection of the desired transfer function for the

closed-loop output impedance. The transfer function chosen for the desired closed-loop output impedance is chosen because it provides an acceptable frequency and time response and it results in a compensator that can be easily synthesized as will be shown in the design examples. It is therefore unnecessary to choose a more complicated or higher order transfer function. The gain, order, and coefficients of Z_{ocld} are therefore chosen and verified by the designer to comply with the requirements for the output impedance of the closed-loop system (3.8). The value of K_Z needs to be determined so the spike in the output voltage due to a step change in load current does not exceed the specification for the output voltage as given by (3.9). The range for K_Z is given in (3.10). It must be greater than zero for practical synthesis.

$$T_C(s) = \frac{V_{TM}}{\beta}\left[\frac{Z_o(s) - Z_{ocld}(s)}{Z_{ocld}(s)T_P(s)}\right] \tag{3.7}$$

$$Z_{ocld}(s) = \frac{K_Z r_C s}{s + \omega_{Zocld}} \tag{3.8}$$

$$K_Z r_C \le \frac{\Delta v_O}{\Delta i_O} \tag{3.9}$$

$$0 < K_Z \le \frac{\Delta v_O}{r_C \Delta i_O} \tag{3.10}$$

Now consider the range for the bandwidth of the closed-loop output impedance, ω_{Zocld}. K. Yao, Y. Meng, and F. Lee provided a relationship between the bandwidth of the closed-loop system and the transient response [18]. They showed that in order to limit the response to a step change in load current to the product of r_C and Δi, the bandwidth must be greater than the critical frequency, $f_{critical}$. The relationship is given in (3.11) and (3.12). The frequency at which the loop gain is 0 dB is the cross over

frequency, f_C. With a low bandwidth design, the maximum transient voltage is reached at some point after the load step change. This means that the control of the power stage determines the value of the transient voltage spike. When the bandwidth is higher than the critical frequency, the maximum transient voltage always occurs at the same time as the load step change. The upper limit of the bandwidth is limited by the validity of the model which is below ½ of the MOSFET switching frequency, f_S [22]. Using the given relationships, the resulting valid range for ω_{Zocld} is expressed by (3.14).

$$\left|V_{pk}\right| = \begin{cases} \dfrac{1+\left(4r_C C f_C\right)^2}{8Cf}\Delta I & f_C < f_{critical} \\ r_C \Delta I & f_C \geq f_{critical} \end{cases} \tag{3.11}$$

$$f_{critical} = \frac{1}{4r_C C} \tag{3.12}$$

$$f_{critical} \leq f_{Zocld} < \frac{f_S}{2} \tag{3.13}$$

$$2\pi f_{critical} \leq \omega_{Zocld} < \pi f_S \tag{3.14}$$

Substituting the equation for Z_{ocld}, Z_O, T_P, into (3.7) yields (3.15). The terms of (3.15) are rearranged and simplified with a substitution for the parallel resistance of R_L and r_C in (3.16) through (3.17). The general form of the compensator transfer function is expressed by (3.23), with the gain and coefficients given by (3.24)-(3.28).

$$T_C(s) = \frac{V_{TM}}{\beta}\left[\frac{\dfrac{R_L r_C}{R_L + r_C}\dfrac{(s+\omega_z)(s+\omega_{rl})}{s^2 + 2\xi\omega_O s + \omega_O^2} - \dfrac{K_Z r_C s}{s+\omega_{Zocld}}}{\dfrac{K_Z r_C s}{s+\omega_{Zocld}}\left[\dfrac{V_I R_L r_C}{L(R_L + r_C)}\dfrac{s+\omega_Z}{s^2 + 2\xi\omega_O s + \omega_O^2}\right]}\right] \tag{3.15}$$

$$T_C(s)=\frac{V_{TM}}{\beta}\left[\frac{\left(\frac{R_L r_C}{R_L+r_C}\right)(s+\omega_Z)(s+\omega_{rl})(s+\omega_{Zocld})-K_Z r_C s\left(s^2+2\xi\omega_o s+\omega_o^2\right)}{\left(\frac{K_Z r_C^2 V_I R_L}{L(R_L+r_C)}\right)s(s+\omega_Z)}\right] \tag{3.16}$$

$$T_C(s)=\frac{V_{TM}L}{\beta V_I}\left[\frac{\left(\frac{R_L r_C}{R_L+r_C}\right)\begin{bmatrix}s^3+s^2(\omega_Z+\omega_{rl}+\omega_{Zocld})+\\ s(\omega_Z\omega_{rl}+\omega_{Zocld}\omega_Z+\omega_{Zocld}\omega_{rl})\\ +\omega_Z\omega_{rl}\omega_{Zocld}\end{bmatrix}-K_Z r_C s\begin{pmatrix}s^2\\ +2\xi\omega_o s\\ +\omega_o^2\end{pmatrix}}{K_Z r_C\left(\frac{R_L r_C}{R_L+r_C}\right)s(s+\omega_Z)}\right] \tag{3.17}$$

$$T_C(s)=\frac{V_{TM}L}{\beta V_I}\left[\frac{\begin{bmatrix}s^3+s^2(\omega_Z+\omega_{rl}+\omega_{Zocld})+\\ s(\omega_Z\omega_{rl}+\omega_{Zocld}\omega_Z+\omega_{Zocld}\omega_{rl})\\ +\omega_Z\omega_{rl}\omega_{Zocld}\end{bmatrix}-K_Z r_C\left(\frac{R_L+r_C}{R_L r_C}\right)s\begin{pmatrix}s^2\\ +2\xi\omega_o s\\ +\omega_o^2\end{pmatrix}}{K_Z r_C s(s+\omega_Z)}\right] \tag{3.18}$$

$$R=\frac{R_L r_C}{R_L+r_C} \tag{3.19}$$

$$T_C(s)=\frac{V_{TM}L}{\beta V_I}\left[\frac{\begin{bmatrix}s^3+s^2(\omega_Z+\omega_{rl}+\omega_{Zocld})+\\ s(\omega_Z\omega_{rl}+\omega_{Zocld}\omega_Z+\omega_{Zocld}\omega_{rl})\\ +\omega_Z\omega_{rl}\omega_{Zocld}\end{bmatrix}-\frac{K_Z r_C}{R}s\left(s^2+2\xi\omega_o s+\omega_o^2\right)}{K_Z r_C s(s+\omega_Z)}\right] \tag{3.20}$$

$$T_C(s)=\frac{V_{TM}L}{\beta V_I}\left[\frac{\begin{bmatrix}s^3\left(1-\frac{K_Z r_C}{R}\right)+s^2\left(\omega_Z+\omega_{rl}+\omega_{Zocld}-2\frac{K_Z r_C}{R}\xi\omega_o\right)+\\ s\left(\omega_Z\omega_{rl}+\omega_{Zocld}\omega_Z+\omega_{Zocld}\omega_{rl}-\frac{K_Z r_C}{R}\omega_o^2\right)+\omega_Z\omega_{rl}\omega_{Zocld}\end{bmatrix}}{K_Z r_C s(s+\omega_Z)}\right] \tag{3.21}$$

$$T_C(s)=\frac{V_{TM}L\omega_{rl}\omega_{Zocld}}{\beta V_I K_Z r_C}\frac{\left[\begin{array}{l} s^3\left(\dfrac{1-\dfrac{K_Z r_C}{R}}{\omega_Z\omega_{rl}\omega_{Zocld}}\right) \\ +s^2\left(\dfrac{\omega_Z+\omega_{rl}+\omega_{Zocld}-2\dfrac{K_Z r_C}{R}\xi\omega_o}{\omega_Z\omega_{rl}\omega_{Zocld}}\right)+ \\ s\left(\dfrac{\omega_Z\omega_{rl}+\omega_{Zocld}\omega_Z+\omega_{Zocld}\omega_{rl}-\dfrac{K_Z r_C}{R}\omega_o^2}{\omega_Z\omega_{rl}\omega_{Zocld}}\right)+1 \end{array}\right]}{s\left(\dfrac{s}{\omega_Z}+1\right)} \tag{3.22}$$

$$T_C(s)=T_{CX}\left[\frac{c_3 s^3+c_2 s^2+c_1 s+1}{d_2 s^2+s}\right] \tag{3.23}$$

$$T_{CX}=\frac{V_{TM}L\omega_{rl}\omega_{Zocld}}{\beta V_I K_Z r_C} \tag{3.24}$$

$$c_3=\left(\frac{1-\dfrac{K_Z r_C}{R}}{\omega_Z\omega_{rl}\omega_{Zocld}}\right) \tag{3.25}$$

$$c_2=\left(\frac{\omega_Z+\omega_{rl}+\omega_{Zocld}-2\dfrac{K_Z r_C}{R}\xi\omega_o}{\omega_Z\omega_{rl}\omega_{Zocld}}\right) \tag{3.26}$$

$$c_1=\left(\frac{\omega_Z\omega_{rl}+\omega_{Zocld}\omega_Z+\omega_{Zocld}\omega_{rl}-\dfrac{K_Z r_C}{R}\omega_o^2}{\omega_Z\omega_{rl}\omega_{Zocld}}\right) \tag{3.27}$$

$$d_2=\frac{1}{\omega_Z} \tag{3.28}$$

This derivation shows that the desired closed-loop output impedance, as defined by (3.8) can be achieved with a third-order compensator. However, (3.23) is not a proper transfer function. As a result, the high frequency magnitude is unbounded and the transfer function is not realizable as a real circuit. For practical reasons, it must be determined if variables K_Z and ω_{Zocld} can selected in a way to elimate at least one of the coefficients in the numerator of the compensator transfer function. The following will present tests which can be applied to determine how to select the variables to make *Tc* a proper or stictly proper transfer function.

3.2.1 ***Coefficient elimination Test* I.**

It is clear from (3.25) that coefficient c_3, can be eliminated by setting K_Z equal to R/r_C provided the value of K_Z satisfies (3.10). Using this value for K_Z, further order reduction may be achieved if a ω_{ocld} can be found that makes coefficient c_2 or c_1 equal to zero. First consider c_2. Set c_2 equal to zero, substitution of K_Z equal to R/r_C into (3.26) yields (3.29). Solve (3.29) for ω_{Zocld} to determine the value of ω_{Zocld} that makes c_2 equal to zero which is expressed in (3.30). If ω_{Zocld} determined by (3.30) complies with (3.14), then it can be used to eliminate coefficient c_2.

$$0 = \omega_Z + \omega_{rl} + \omega_{Zocld} - \frac{2}{R}\left(\frac{R}{r_C}\right) r_C \xi \omega_0 \tag{3.29}$$

$$\omega_{Zocld} = 2\xi\omega_0 - \omega_Z - \omega_{rl} \tag{3.30}$$

In the same way, one can determine if a value of ω_{Zocld} can be found that makes c_1 equal to zero. Set c_1 equal to zero, substituting K_Z equal to R/r_C yields (3.31). Solve (3.31) for ω_{Zocld} to determine the value of ω_{Zocld} that makes c_1 equal to zero (3.32). If

ω_{Zocld} determined by (3.32) complies with (3.14), then it can be used to eliminate coefficient c_1. Table 3.1 provides the equations which are used to determine if c_3, c_2, or c_1 can be eliminated.

$$0 = \omega_Z \omega_{rl} + \omega_Z \omega_{Zocld} + \omega_{Zocld} \omega_{rl} - \frac{1}{R}\left(\frac{R}{r_C}\right) r_C \omega_0^2 \tag{3.31}$$

$$\omega_{Zocld} = \frac{\omega_0^2 - \omega_Z \omega_{rl}}{\omega_Z + \omega_{rl}} \tag{3.32}$$

Coefficient	K_Z	ω_{Zocld}
c_3=0 *if* $\rightarrow$	$0 < K_Z = \frac{R}{r_C} \le \frac{\Delta v_O}{r_C \Delta i_O}$	NA
c_2=0 *if* $\rightarrow$	$0 < K_Z = \frac{R}{r_C} \le \frac{\Delta v_O}{r_C \Delta i_O}$	$2\pi f_{critical} \le \omega_{Zocld} = 2\xi\omega_0 - \omega_Z - \omega_{rl} < \pi f_S$
c_1=0 *if* $\rightarrow$	$0 < K_Z = \frac{R}{r_C} \le \frac{\Delta v_O}{r_C \Delta i_O}$	$2\pi f_{critical} \le \omega_{Zocld} = \frac{\omega_0^2 - \omega_Z \omega_{rl}}{\omega_Z + \omega_{rl}} < \pi f_S$

Table 3.1: Test I to determine if c_3, c_2, or c_1 can be eliminated

3.2.2 ***Coefficient elimination Test* II.**

An alternate approach to eliminate coefficients c_2 and c_1 is to solve equations (3.26) and (3.27) simultaneously for K_Z and ω_{Zocld}. The solution is as follows. Set equations (3.26) and (3.27) equal to zero and eliminate the denominator terms as shown in (3.33) and (3.34). Solve (3.33) for K_Z as expressed by (3.35). Substitute K_Z from (3.35) into (3.34) as expressed by (3.36). Solve (3.36) for ω_{Zocld} yields (3.37). Table 3.2 provides the equations which are used to determine if c_2 and c_1 can be eliminated.

$$0 = \omega_Z + \omega_{rl} + \omega_{Zocld} - 2\frac{K_Z r_C}{R}\xi\omega_o \tag{3.33}$$

$$0 = \omega_Z \omega_{rl} + \omega_{Zocld} \omega_Z + \omega_{Zocld} \omega_{rl} - \frac{K_Z r_C}{R} \omega_o^2 \tag{3.34}$$

$$K_Z = \frac{R\left(\omega_Z + \omega_{rl} + \omega_{Zocld}\right)}{2 r_C \xi \omega_o} \tag{3.35}$$

$$0 = \omega_Z \omega_{rl} + \omega_{Zocld} \omega_Z + \omega_{Zocld} \omega_{rl} - \frac{r_C}{R} \frac{R\left(\omega_Z + \omega_{rl} + \omega_{Zocld}\right)}{2 r_C \xi \omega_o} \omega_o^2 \tag{3.36}$$

$$\omega_{Zocld} = \frac{\omega_o\left(\omega_Z + \omega_{rl}\right) - 2\xi \omega_Z \omega_{rl}}{2\xi\left(\omega_Z + \omega_{rl}\right) - \omega_o} \tag{3.37}$$

Coefficient	K_Z	ω_{Zocld}
$c_2 = c_1 = 0$ *if* $\rightarrow$	$0 < K_Z = \frac{R\left(\omega_Z + \omega_{rl} + \omega_{Zocld}\right)}{2 r_C \xi \omega_o} \le \frac{\Delta v_O}{r_C \Delta i}$	$2\pi f_{critical} \le \omega_{Zocld} = \frac{\omega_o\left(\omega_Z + \omega_{rl}\right) - 2\xi \omega_Z \omega_{rl}}{2\xi\left(\omega_Z + \omega_{rl}\right) - \omega_o} < \pi f_S$

Table 3.2: Test II to determine if c_2 or c_1 can be eliminated

As previously stated, at least one coefficient must be eliminated in order to create a realizable compensator transfer function. Consider once again the allowable range for K_Z as given by (3.38). Substitute $K_Z = R/r_C$ into (3.38) yields (3.39), and cancelling the common r_C term in the denominator yields (3.40). Substitute R into (3.40) yields (3.41). Equation (3.41) can be re-written as expressed in (3.42). Equation (3.43) is used to select r_C so the voltage spike due to a step change in load current does not exceed the output voltage requirement of the dc-dc converter. This equation can always be made valid through selection of r_C. Equation (3.44) is also always valid. Combining (3.43) and (3.44) proves that (3.42) can always be made valid through proper selection of r_C. This shows that a K_Z can always be selected to eliminate c_3 through proper selection of r_C.

$$0 < K_Z \le \frac{\Delta v_O}{r_C \Delta i_O} \tag{3.38}$$

$$0 < \frac{R}{r_C} \leq \frac{\Delta v_O}{r_C \Delta i_O} \tag{3.39}$$

$$0 < R \leq \frac{\Delta v_O}{\Delta i_O} \tag{3.40}$$

$$0 < \frac{R_L r_C}{R_L + r_C} \leq \frac{\Delta v_O}{\Delta i_O} \tag{3.41}$$

$$0 < \left[\frac{R_L}{R_L + r_C} \right] r_C \leq \frac{\Delta v_O}{\Delta i_O} \tag{3.42}$$

$$0 < r_C \leq \frac{\Delta v_O}{\Delta i_O} \tag{3.43}$$

$$0 < \frac{R_L}{R_L + r_C} \leq 1 \tag{3.44}$$

$$0 < \left[\frac{R_L}{R_L + r_C} \right] r_C \leq r_C \tag{3.45}$$

3.3 Summary of methodology

In summary, the steps in this alternative approach to design a Buck Converter to achieve the desired output impedance are as follows. These steps should be iterated until a suitable solution is reached.

1. Design the power stage and determine the transfer function of the open-loop output impedance, Z_o.
2. Determine the allowable range for K_Z and ω_{Zocld}.
3. Determine the minimal order transfer function for the compensator, and set the final values for K_Z and ω_{Zocld} for the transfer function of the desired closed-loop output impedance.
4. Simulate the closed-loop response to verify compliance to design requirements.

5. Design the compensation network. Select the component values and verify compliance to closed-loop system requirements through simulation and hardware synthesis.

Two design examples using this method are presented in the following two chapters. In Chapter 4, the design method is used to design a converter which complies with the VRM9.1 specifications presented in Chapter 2. This will offer a contrast to common industry design method presented in that chapter.

In Chapter 5, the method will be applied to comply with the requirements of a military aircraft standard for dc power supply. In this example, a complete hardware design will be presented. The hardware is simulated with PSPICE. The hardware is synthesized, and the actual hardware is tested to verify compliance with the military specifications.

4 Design for the Intel VRM9.1 Voltage Regulator Module

4.1 Introduction

In Chapter 2, a PWM Buck Converter was designed using the linear-small signal model for the switch which included the diode and parasitic effects. The industry methodology was used to determine the compensator to enable the converter to comply with the Intel VRM9.1 specifications. The design required an ESR of the output capacitor to be no greater than 0.0015 Ω in order to keep the voltage spike within tolerance during a step change in load current. The size of the output capacitor was determined to be no greater than 2775 μF. Since no single capacitor could be found with those characteristics, a combination of 7 parallel 470 μF capacitors with an ESR of 0.01 Ω was used in the design.

The method presented in Chapter 3 can be used to determine an alternate compensator that does not require multiple output capacitors to comply with the converter requirements. The multiple capacitors were required in order to achieve the ESR and hence output impedance that will prevent the output voltage from deviating beyond its specified tolerance in response to the maximum step change in load. Using the method presented in Chapter 3, the output impedance will not be determined solely by the ESR of the output capacitance, but also by the compensator through proper selection of K_Z.

4.2 Design

Consider once again the buck converter specifications for the Intel VRM9.1 voltage regulator module presented in Table 2.1. Using the inductor value selected in Chapter 2, begin a redesign with the output capacitor. The maximum inductor ripple current is expressed by (4.1). The ripple voltage is given by (4.2). The maximum ESR of the filter capacitor to comply with the ripple voltage specification is given by (4.3). The minimum value of the filter capacitance at which the ripple voltage is determined by the ripple voltage across the ESR is expressed by (4.4). Choose the capacitance of the output filter to be (4.6). To achieve the required ESR and minimum capacitance as given by (4.3), the design will use 1 output capacitor, and rely on further reduction in output impedance through proper selection of K_Z as shown in Chapter 3. Basically, the effective ESR will be equal to the product of the ESR of the output capacitor and K_Z. Table 4.1 lists the components that will be used in the design.

$$\Delta i_{L(\max)} = \frac{V_{O(\max)}\left(1 - D_{(\min)}\right)}{f_S L} = \frac{1.491\left(1 - 0.166\right)}{\left(200 \times 10^3\right)\left(13 \times 10^{-6}\right)} = 0.478 \text{ A} \tag{4.1}$$

$$V_r = \frac{V_{O(\max)}}{100} = \frac{1.491}{100} = 0.01491 \text{ V} \tag{4.2}$$

$$r_{C(\max)} = \frac{V_r}{\Delta i_{L(\max)}} = \frac{0.01491}{0.478} = 0.031\,\Omega \tag{4.3}$$

$$C_{(\min)} = \max\left\{\frac{D_{(\max)}}{2 f_S r_C}, \frac{1 - D_{(\min)}}{2 f_S r_C}\right\} \tag{4.4}$$

$$C_{(\min)} = \max\left\{15.56\ \mu\text{F}, 67.26\ \mu\text{F}\right\} = 67.25\ \mu\text{F} \tag{4.5}$$

$$C = 470\ \mu\text{F} / 0.01\,\Omega / 4\text{ V} \tag{4.6}$$

Parameter	Value	Unit
L	13	µH
r_L	0.009	Ω
C	470	µF
r_C	0.01	Ω
r_{DS}	0.015	Ω
R_F	0.015	Ω
V_F	0.39	V
Dnom	0.180	NA
r	0.024	Ω

Table 4.1: Buck converter component values

With the components selected, the design continues using the steps outlined in Chapter 3.3. The first step is to determine the open-loop output impedance. This transfer function was defined in (2.86). The second step is to determine the range of acceptable values for K_Z and ω_{Zocld}. The range for K_Z and ω_{Zocld} is given by (4.8) and (4.9), respectively.

$$K_Z r_C \le \frac{V_{nom} - V_{\min}}{i_{L(\max)} - i_{L(\min)}} = \frac{(1.476 - 1.461)}{(10 - 0.5)} = 0.0015\,\Omega \tag{4.7}$$

$$0 < K_Z \le \frac{V_{nom} - V_{\min}}{r_C\left(i_{L(\max)} - i_{L(\min)}\right)} = \frac{(1.476 - 1.461)}{0.01(10 - 0.5)} = \frac{0.0015}{0.01} = 0.158 \tag{4.8}$$

$$2\pi f_{critical} \le \omega_{Zocld} < \pi f_S \tag{4.9}$$

$$\frac{\pi}{2r_C C} \le \omega_{Zocld} < \pi f_S \tag{4.10}$$

$$\frac{\pi}{2\times 0.01\times\left(470\times 10^{-6}\right)} \le \omega_{Zocld} < \pi\left(200\times 10^{3}\right) \tag{4.11}$$

$$334\times 10^{3}\ {}^{\text{rad}}\!/_{\text{sec}} \le \omega_{Zocld} < 628\times 10^{3}\ {}^{\text{rad}}\!/_{\text{sec}} \tag{4.12}$$

The next step is to determine if any of the coefficients of the compensator transfer function, T_C, can be eliminated using Table 3.1 and Table 3.2. Coefficient c_3 can be eliminated by selecting K_Z to be equal to R/r_C. The calculations are provided by (4.13). Since this result does not comply with (4.8), coefficient c_3 cannot be eliminated.

$$\frac{R}{r_C} = \frac{R_L}{R_L + r_C} = \frac{0.146}{\left(0.146 + 0.01\right)} = 0.935 \tag{4.13}$$

Now consider if coefficients c_2 and c_1 can be eliminated by using the equations presented in Table 3.2. The calculations are completed in (4.14) and (4.15). The results indicate that neither c_2 nor c_1 can be eliminated.

$$\omega_{Zocld} = \frac{\omega_o\left(\omega_Z + \omega_{rl}\right) - 2\xi\omega_Z\omega_{rl}}{2\xi\left(\omega_Z + \omega_{rl}\right) - \omega_o} = 9671.9\ {}^{\text{rad}}\!/_{\text{sec}} \tag{4.14}$$

$$K_Z = \frac{R\left(\omega_Z + \omega_{rl} + \omega_{Zocld}\right)}{2r_C\xi\omega_o} = 12.95 \tag{4.15}$$

It has been shown that none of the coefficients of the compensator transfer function can be eliminated. However, at least one of the numerator coefficients of the transfer function must be eliminated in order to make the transfer function proper, and realizable. Choose r_C = 0.0015 Ω to comply with (4.7). This changes the range of K_Z to that shown in (4.17). Equation (4.18) shows that selecting $K_Z = R/r_C$ is valid. As a result, coefficient c_3 is eliminated and the transfer function of the compensator is proper. Select $_{Zocld}$ to be 60 kHz.

$$0 < r_C \le \frac{\Delta v_O}{\Delta i_O} = 0.0015 \tag{4.16}$$

$$0 < K_Z \le \frac{V_{nom} - V_{\min}}{r_C\left(i_{L(\max)} - i_{L(\min)}\right)} = \frac{\left(1.476 - 1.461\right)}{0.0015\left(10 - 0.5\right)} = \frac{0.0015}{0.0015} = 1 \tag{4.17}$$

$$\frac{R}{r_C} = \frac{R_L}{R_L + r_C} = \frac{0.146}{\left(0.146 + 0.0015\right)} = 0.98 \tag{4.18}$$

$$\omega_{Zocld} = 2\pi f_{Zocld} = 2\pi\left(60 \times 10^3\right)^{\text{rad}/\text{sec}} \tag{4.19}$$

The next step is to determine the transfer function of the compensator using (3.23) with gain and coefficients defined by (3.24) – (3.28). The transfer function terms are given by (4.20)-(4.24). The frequency response of the compensator is shown in Fig. 4-1 and Fig. 4-2.

$$T_{CX} = \frac{V_{TM} L \omega_{rl} \omega_{Zocld}}{\beta V_I K_Z r_C} = 4.685 \times 10^6 \tag{4.20}$$

$$c_2 = \left(\frac{\omega_Z + \omega_{rl} + \omega_{Zocld} - 2\dfrac{K_Z r_C}{R}\xi\omega_o}{\omega_Z \omega_{rl} \omega_{Zocld}} \right) = 1.804 \times 10^{-9} \tag{4.21}$$

$$c_1 = \left(\frac{\omega_Z \omega_{rl} + \omega_{Zocld}\omega_Z + \omega_{Zocld}\omega_{rl} - \dfrac{K_Z r_C}{R}\omega_o^2}{\omega_Z \omega_{rl} \omega_{Zocld}} \right) = 5.448 \times 10^{-4} \tag{4.22}$$

$$d_2 = \frac{1}{\omega_Z} = 7.05 \times 10^{-7} \tag{4.23}$$

$$T_C(s) = 4.685 \times 10^6 \left[\frac{1.804 \times 10^{-9} s^2 + 5.448 \times 10^{-4} s + 1}{7.05 \times 10^{-7} s^2 + s} \right] \tag{4.24}$$

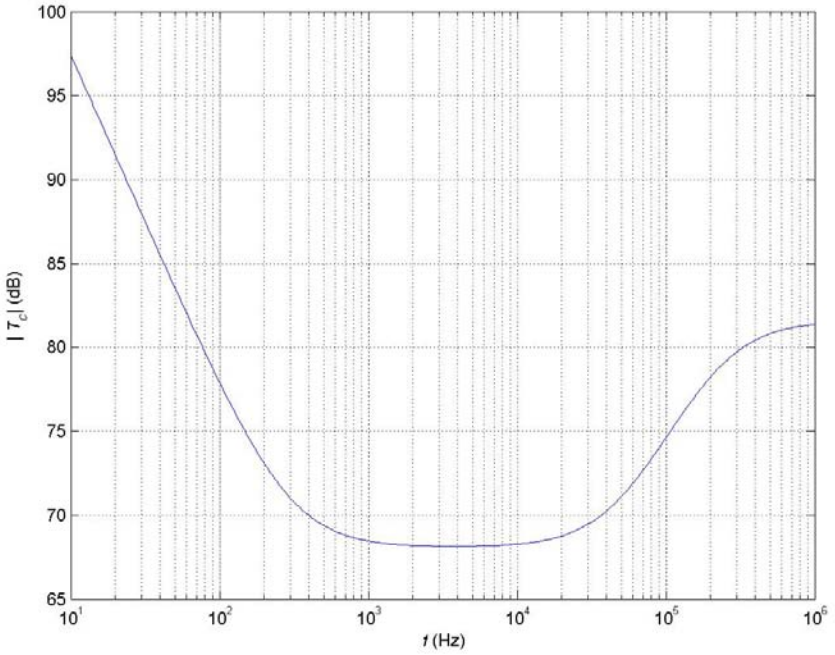

Figure 4.1: Magnitude of compensator, T_c

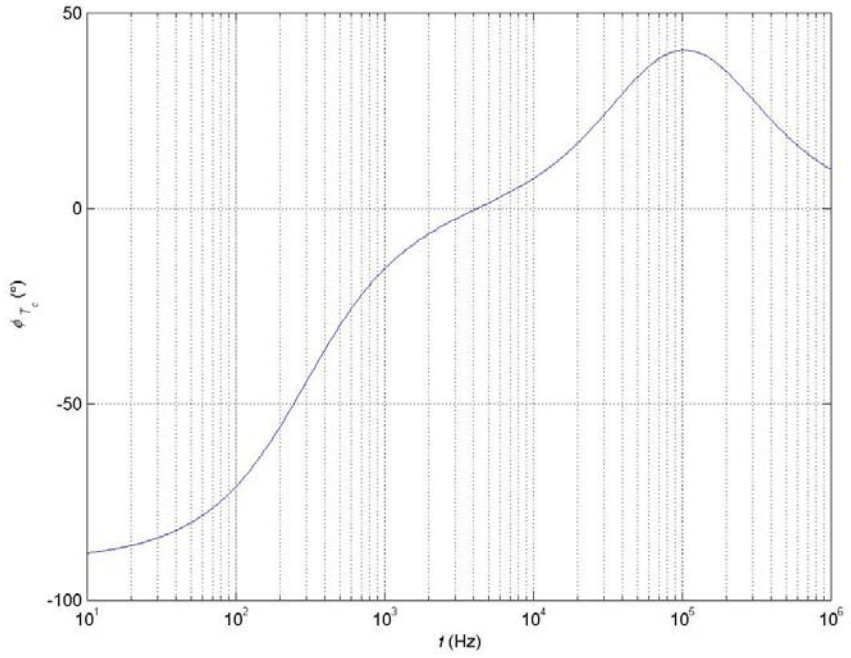

Figure 4.2: Phase of the compensator, T_c

The frequency response of the loop gain is presented in Fig. 4.3 – 4.4. The loop cross over frequency is 288 kHz, and the phase margin is 81º. Figs 4.5 – 4.7 provide a comparison between the closed-loop output impedance achieved with the compensator, T_C, and the desired closed-loop output impedance. As can be seen, there is very good agreement between the designed and desired closed-loop output impedances. Fig. 4.8 compares the open and closed-loop output impedance. The figure shows the compensator caused the resonant due to the parallel LC network to be eliminated and the bandwidth of the closed-loop output impedance to be increased.

The step response of the output voltage to a step change in load is presented in Fig. 4.9. The maximum spike occurs at the initial step change in load. The maximum peak is 1.462 V which is within tolerance of the output voltage. The step response of the output voltage to a step change in input voltage is shown in Fig. 4.10. The output voltage stays well within the tolerance and therefore complies with the given specifications.

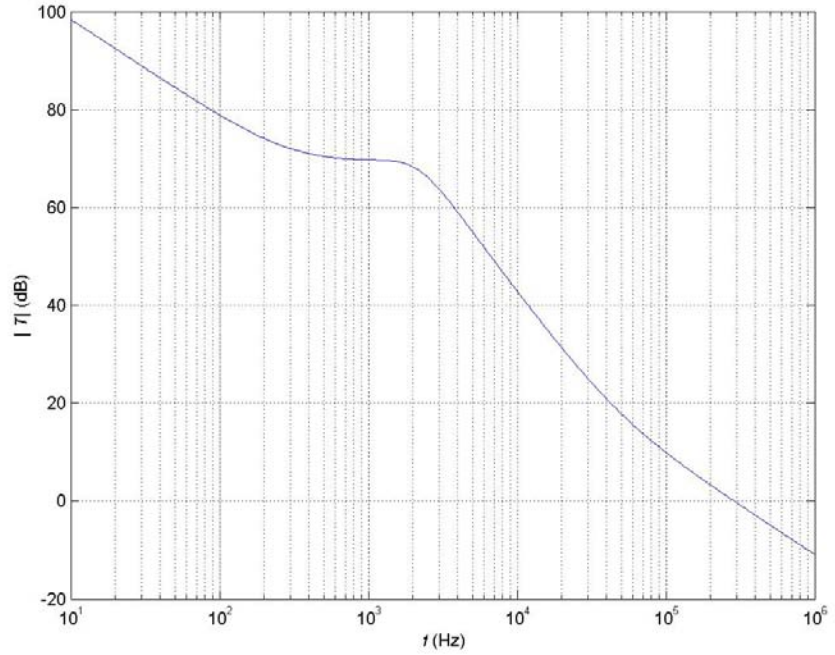

Figure 4.3: Loop gain with compensator

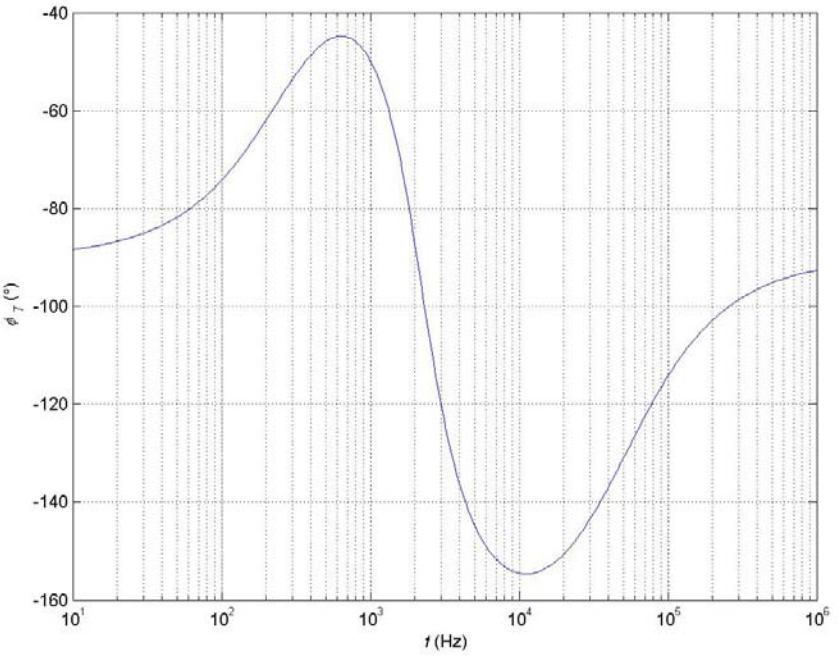

Figure 4.4: Phase of compensated loop gain

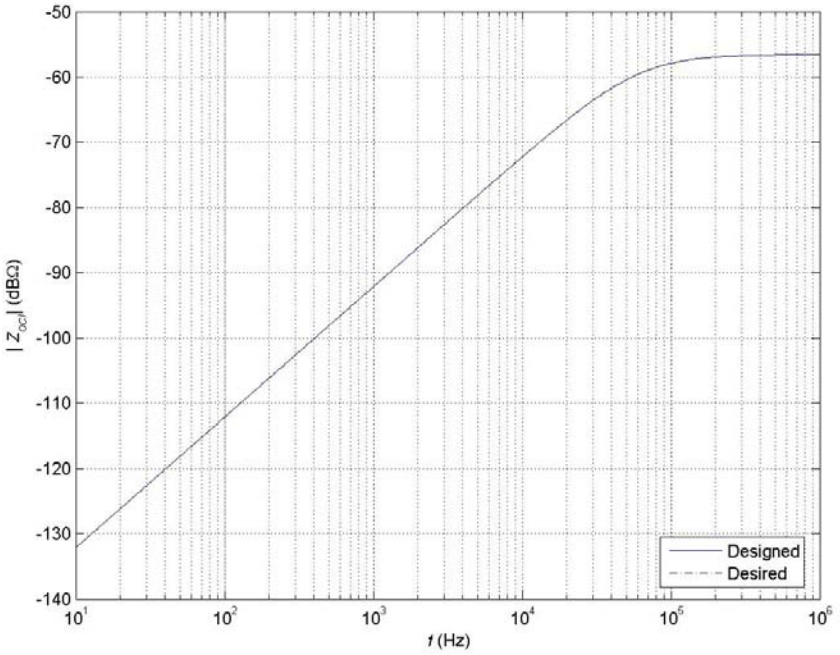

Figure 4.5: Magnitude of closed-loop output impedance

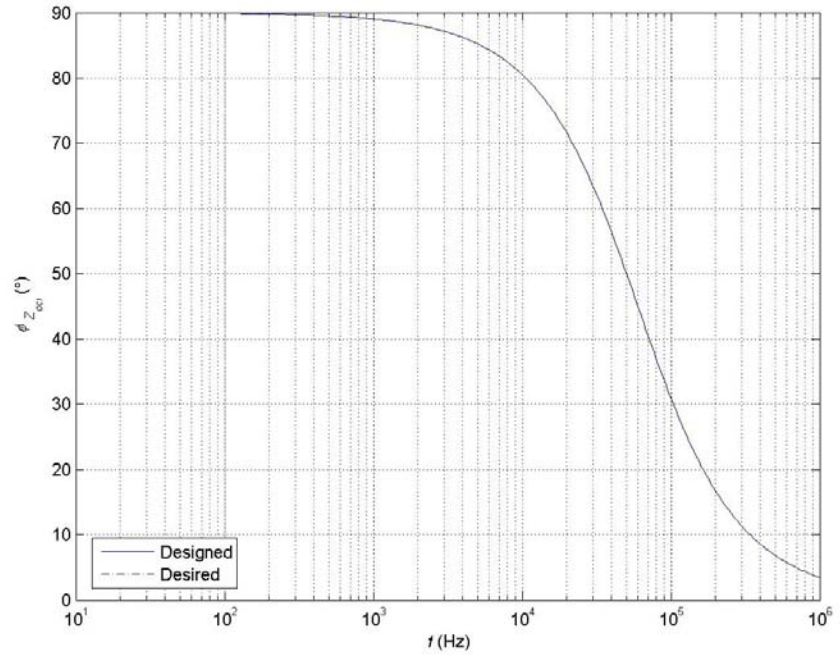

Figure 4.6: Phase of closed-loop output impedance

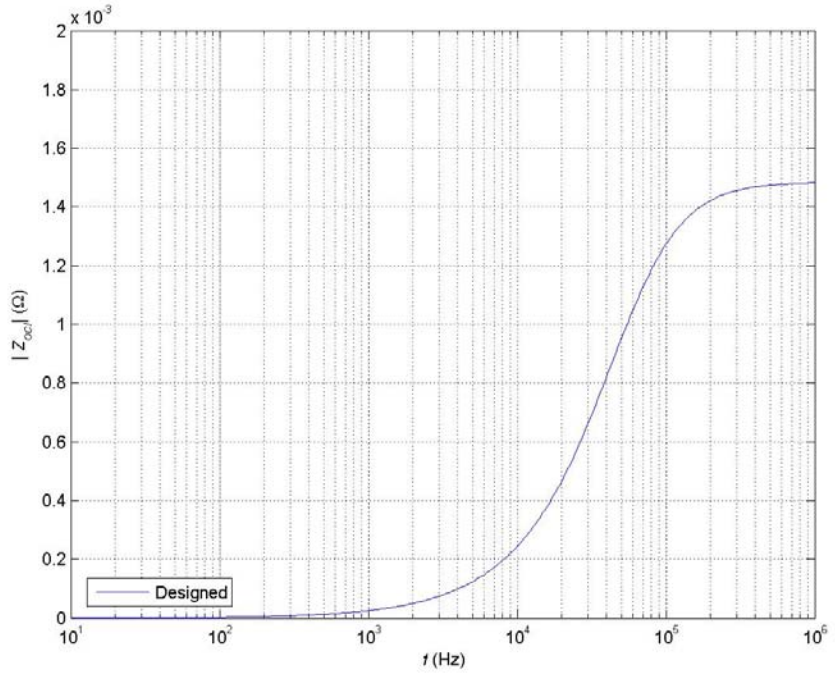

Figure 4.7: Magnitude of closed-loop output impedance

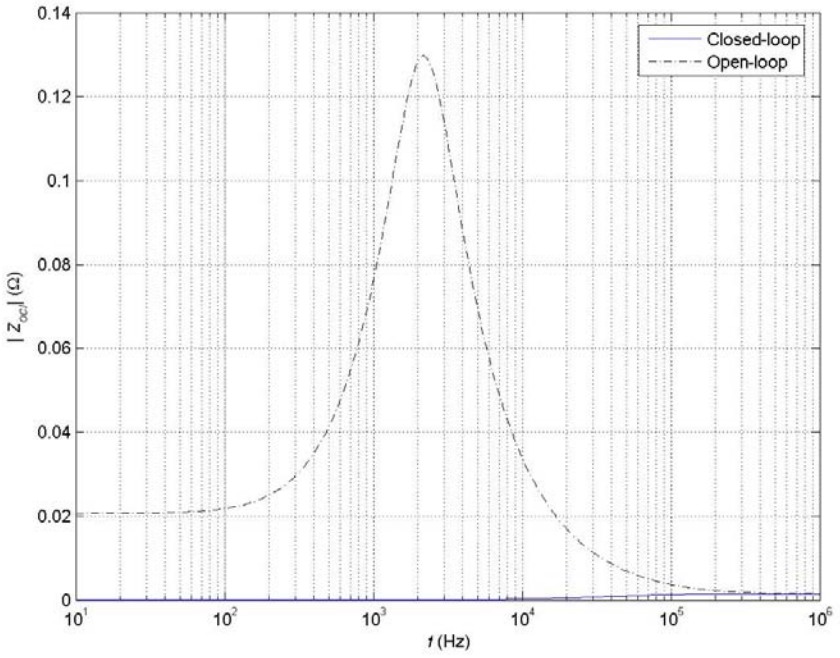

Figure 4.8: Magnitude of open and closed-loop output impedance

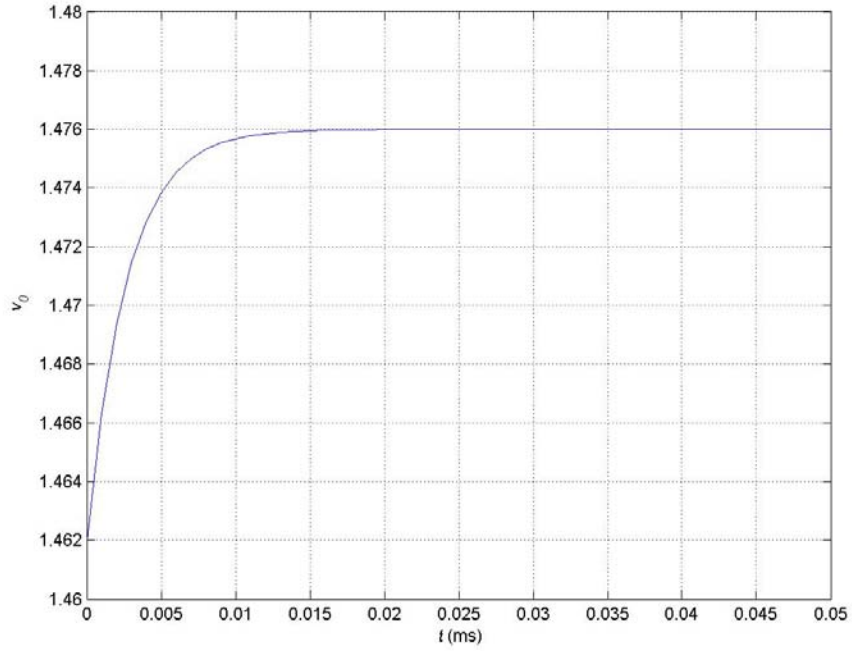

Figure 4.9: Step response of vo to a step change in the load current from 0.5 to 10 A for the closed-loop converter with V_I = 12 V and R_L = 0.146 Ω

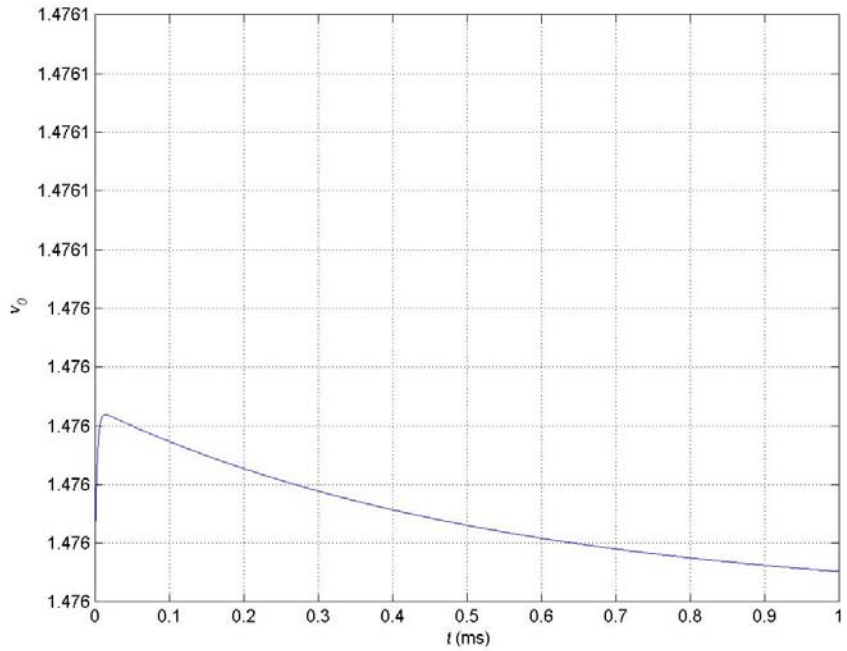

Figure 4.10: Step response of vo to a step change in input voltage from 12 to 12.6 V for the closed-loop converter with R_L = 10.3 Ω

5 Design for the Aircraft Electric Power Regulator MIL-STD-704F

5.1 Introduction

This chapter applies the method presented in Chapter 3 to design a dc-dc converter for an aircraft dc-dc converter in accordance with the requirements stated in MIL-STD-704F. The aircraft electric power system consists of a main power source, emergency power source, power conversion circuits, control and protection devices, and an interconnection network (wires, cables, connectors, etc.). The main power is derived from aircraft generators driven by the aircraft propulsion engines. Emergency power is derived from batteries, engine bleed air, independent auxiliary power units, ram air driven generators, or hydraulic generators.

There are both AC and DC conversion circuits. The AC system provides electrical power using the single-phase or three-phase wire connected ground neutral systems. The voltage waveform is a sine wave with a nominal voltage of 115 volts and a nominal frequency of 400 Hz. The DC conversion system provides power using direct current, two-wire or negative ground return system having a nominal voltage of 28 V or 270 V. This chapter presents the design of a single dc converter for the 28 V supply system. The dc-dc converter serves the purpose of down converting the 28 V supply to 14 V for analog circuits on board the aircraft. The converter must be capable of withstanding input voltage and load disturbances without allowing the output voltage to exceed the

requirements stated in the military standard. This chapter presents the design, circuit simulation, hardware realization, and hardware verification testing.

Table 5.1 summarizes the dc-dc converter specifications stated in MIL-STD-704F. The input voltage to the converter is nominally 28 V with a ±4 V tolerance. The converter is designed to supply a nominal output voltage of 14 V, and allows a tolerance of ±1 V due to input voltage and load disturbances. The single dc converter must be capable of supplying as much as 0.90 A at full load and a light load of 0.50 A. The ripple of the output voltage is to be no greater than 1.5 V.

Parameter	Max	Nominal	Min
Input Voltage, V_I (V)	32.0	28.0	24.0
Output Voltage, V_O (V)	15.0	14.0	13.0
Output Current, I_O (A)	0.90	0.70	0.50
Ripple Voltage, V_r (V)	0.2		0
Response Time (1% of V_O) (ms)	0.02		

Table 5.1: MIL-STD-704F dc-dc converter specifications

5.2 Power stage design

This section presents the design and simulation of the power stage for the 28 V dc buck converter using the methods presented in [22]. The range for the power supplied by the converter is determined using the limits for the output voltage and current given in the specification as determined by (5.1) and (5.2). Likewise, the limits for the load resistance are determined by (5.3) and (5.4). The dc transfer function for the PWM Buck Converter is simply the dc output voltage divided by the dc input voltage. The range for the dc transfer functions are given by (5.5) and (5.6). The efficiency of a PWM Buck Converter

is typically around 90%. Using the assumed efficiency, the duty cycle limits required to maintain the output voltage when considering the range of the input voltage is expressed by (5.7) through (5.9). The nominal duty cycle of the PWM signal is 0.573. A PWM frequency, f_S, of 100 kHz is typical for Buck Converters of this nature and will be adequate for this design.

$$P_{O(\max)} = V_{O(\max)} I_{O(\max)} = 32 \times 0.9 = 28.80 \text{ W} \tag{5.1}$$

$$P_{O(\min)} = V_{O(\min)} I_{O(\min)} = 24 \times 0.50 = 12.00 \text{ W} \tag{5.2}$$

$$R_{L(\max)} = \frac{V_{O(\max)}}{I_{O(\min)}} = \frac{15.0}{0.50} = 30.0\ \Omega \tag{5.3}$$

$$R_{L(\min)} = \frac{V_{O(\min)}}{I_{O(\max)}} = \frac{13.0}{0.90} = 14.4\ \Omega \tag{5.4}$$

$$M_{VDC(\max)} = \frac{V_{O(\max)}}{V_{I(\min)}} = \frac{15}{24} = 0.625 \tag{5.5}$$

$$M_{VDC(\min)} = \frac{V_{O(\min)}}{V_{I(\max)}} = \frac{13}{32} = 0.406 \tag{5.6}$$

$$D_{(\max)} = \frac{M_{VDC(\max)}}{\eta} = \frac{0.625}{0.90} = 0.694 \tag{5.7}$$

$$D_{(\min)} = \frac{M_{VDC(\min)}}{\eta} = \frac{0.406}{0.90} = 0.451 \tag{5.8}$$

$$D_{(nom)} = \frac{D_{(\max)} + D_{(\max)}}{2} = 0.573 \tag{5.9}$$

The parameters for the inductor and output capacitor of the power stage will now be determined. The minimum inductance that is required to maintain the converter in Continuous Conduction Mode (CCM) is expressed by (5.10). A 330 µH toroid inductor was chosen for the design. The inductance and dc resistance of the inductor both vary

with frequency. Using test equipment at the AFRL Propulsion Lab at WPAFB, the inductance and dc resistance was measured to be 364.56 μH and 0.3 Ω. The relevant characteristics of the inductor are expressed by (5.11). The maximum ripple current is expressed using the measured value for the inductance as determined by (5.12).

$$L_{(\min)} = \frac{R_{L(\max)}\left(1 - D_{(\min)}\right)}{2 f_S} = \frac{30.0(1 - 0.451)}{2\left(100 \times 10^3\right)} = 82.35\ \mu\text{H} \tag{5.10}$$

$$L = 364.56\ \mu\text{H} / 0.3\ \Omega / 4.9\ \text{A} \tag{5.11}$$

$$\Delta i_{L(\max)} = \frac{V_{O(\max)}\left(1 - D_{(\min)}\right)}{f_S L} = \frac{15.0(1 - 0.451)}{\left(100 \times 10^3\right)\left(364.56 \times 10^{-6}\right)} = 0.225\ \text{A} \tag{5.12}$$

If the filter capacitor is large enough, the ripple voltage is equal to the product of the capacitor ESR and the ripple current. As a result, the ESR must be limited so the product does not allow the output voltage to exceed its specification due to the maximum step change in load current. The maximum value of the ESR is determined by (5.13). The minimum value of the filter capacitance at which the ripple voltage is determined by the ripple voltage across the ESR is expressed by (5.14). A 47 μF aluminum electrolytic capacitor was chosen for the design. The characteristics of the capacitor at the PWM frequency were measured to be 42.56 μF and 0.7 Ω as shown in (5.15).

$$r_{C(\max)} = \min\left\{\frac{V_r}{\Delta i_{L(\max)}}, \frac{V_{nom} - V_{\min}}{i_{O(\max)} - i_{O(\min)}}\right\} = 0.67\ \Omega \tag{5.13}$$

$$r_{C(\max)} = \min\left\{\frac{0.20}{0.225}, \frac{1.0}{(0.90 - 0.50)}\right\} = 0.89\ \Omega \tag{5.13}$$

$$C_{(\min)} = \max\left\{\frac{D_{(\max)}}{2 f_S r_C}, \frac{1 - D_{(\min)}}{2 f_S r_C}\right\} \tag{5.14}$$

$$C_{(\min)} = \max\left\{\frac{0.694}{2(100\times10^{3})(0.7)}, \frac{1-0.451}{2(100\times10^{3})(0.7)}\right\} \tag{5.14}$$

$$C_{(\min)} = \max\{4.96\ \mu\text{F}, 3.92\ \mu\text{F}\} = 4.96\ \mu\text{F} \tag{5.14}$$

$$C = 42.56\ \mu\text{F} / 0.7\ \Omega / 200\ \text{V} \tag{5.15}$$

The parameters for the switch and diode are required to complete the design of the power stage. The voltage and current stresses for the devices are given by (5.16) and (5.17) respectively. An International Rectifier IRF530 power MOSFET was selected for the design. The relevant characteristics for the switch are given by (5.18) through (5.20). An On Semiconductor MUR820 power rectifier was selected. The relevant characteristics of the power diode in regards to this design are given by (5.21) through (5.24). Table 5.2 provides a summary of the component parameters of the design.

$$V_{SM(\max)} = V_{DM(\max)} = 15\ \text{V} \tag{5.16}$$

$$I_{SM(\max)} = I_{DM(\max)} = I_{O(\max)} + \frac{\Delta i_{L(\max)}}{2} = 1.4 + \frac{0.225}{2} = 1.5125\ \text{A} \tag{5.17}$$

$$V_{DSS} = 100\ \text{V} \tag{5.18}$$

$$I_{SM} = 16\ \text{A} \tag{5.19}$$

$$r_{DS(ON)} = 0.4\ \Omega \tag{5.20}$$

$$I_{DM} = 16\ \text{A} \tag{5.21}$$

$$V_{DM} = 200\ \text{V} \tag{5.22}$$

$$V_{F} = 0.7\ \text{V} \tag{5.23}$$

$$R_{F} = 0.1\ \Omega \tag{5.24}$$

Parameter	Value	Unit
L	364.56	µH
r_L	0.3	Ω
C	42.546	µF
r_C	0.7	Ω
R_{Lmin}	14.4	Ω
r_{DS}	0.012	Ω
R_F	0.05	Ω
V_F	0.79	V
Dnom	0.573	NA
r	0.57	Ω

Table 5.2: Buck Converter components

Fig. 5.1 shows the schematic of the power stage using the parameters of the selected components. The value of *r* was determined using the parasitic parameters of the inductor, switch, and diode in accordance with (5.25). The schematic includes the annotated nodes to be used in the PSPICE simulation.

$$r = D_{nom} r_{DS} + (1 - D_{nom}) R_F + r_L \tag{5.25}$$

$$r = 0.573 \times 0.4 + (1 - 0.573)(0.1) + 0.3 = 0.57\ \Omega \tag{5.25}$$

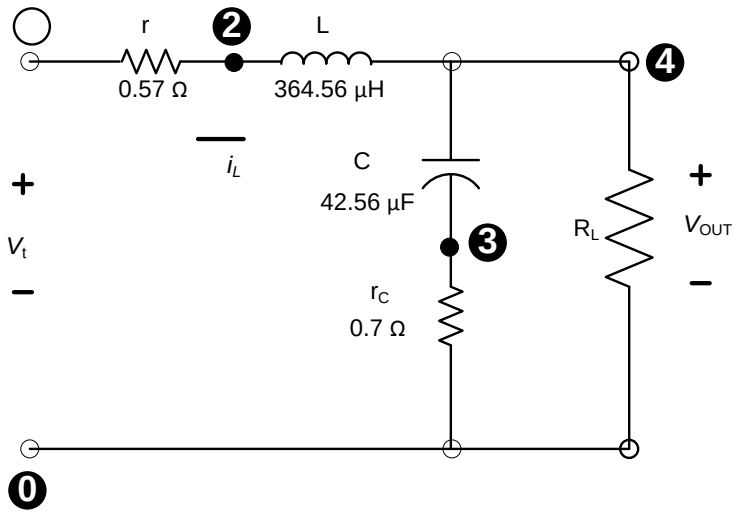

Figure 5.1: Schematic of power stage of Buck Converter

The transfer function for the power stage is given by (5.26). Fig. 5.2 and Fig. 5.3 provide the frequency response of the power stage with R_L = 14.4 Ω, which is the measured value for the load resistor used in the design. Selected points from the PSPICE simulation are included in the frequency response plots, showing it is in good agreement with the analytical results obtained through Matlab. The power stage filter has a dc value of 0.962, a resonance at 1309 Hz, and a zero at 5344 Hz. The power stage has a damping factor of 0.313. The peak value of the power stage is 4.375 dB.

$$G_{psf}(s) = \frac{1937\left(s + 3.358 \times 10^4\right)}{s^2 + 5154s + 6.764 \times 10^7} \tag{5.26}$$

$$G_{psf}(0) = 0.962 = -0.34 \text{ dB} \tag{5.27}$$

$$f_o = 1309 \text{ Hz} \tag{5.28}$$

$$f_z = 5344 \text{ Hz} \tag{5.29}$$

$$\xi = 0.313 \tag{5.30}$$

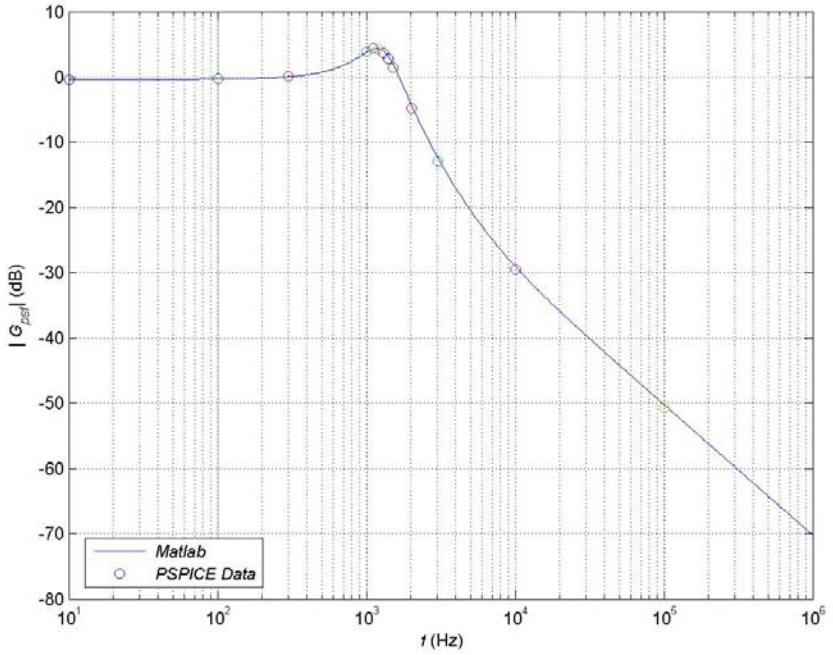

Figure 5.2: Magnitude response of power stage, G_{psf}, with R_L = 14.4 Ω

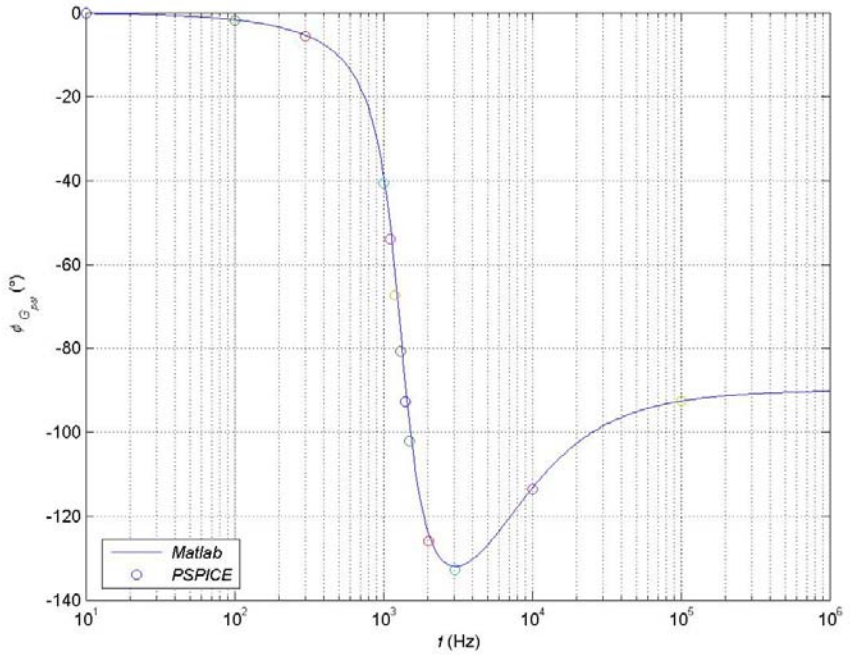

Figure 5.3: Phase response of the power stage, G_{psf}, with R_L = 14.4 Ω

To complete this section on the design of the power stage, the transfer functions for the duty cycle-to-output voltage, input voltage-to-output voltage, and output impedance will be provided. The transfer function for the duty cycle-to-output voltage for the nominal input voltage is provided in (5.31). The dc value of the transfer function is 28.60 dBV. The transfer function of the input voltage-to-output voltage with the nominal duty cycle is expressed in (5.33). The magnitude response of both transfer functions is offset from the response of the power stage by a constant factor. The phase response of both transfer functions is identical to that of the power stage presented in Fig. 5.3.

$$T_P(s) \equiv \frac{v_o(s)}{d(s)}\Big|_{v_i = i_o = 0} = V_{I(nom)} G_{psf}(s) = \frac{5.425 \times 10^4 \left(s + 3.358 \times 10^4\right)}{s^2 + 5154s + 6.764 \times 10^7} \tag{5.31}$$

$$T_p(0) = 26.93 \text{ V} = 28.60 \text{ dBV} \tag{5.32}$$

$$M_V(s) \equiv \frac{v_o(s)}{v_i(s)}\Big|_{d = i_o = 0} = D_{nom} G_{psf}(s) = \frac{1109\left(s + 3.358 \times 10^4\right)}{s^2 + 5154s + 6.764 \times 10^7} \tag{5.33}$$

$$M_v(0) = 0.551 = -5.18 \text{ dB} \tag{5.34}$$

Fig. 5.4 provides the schematic to determine the open-loop output impedance. The schematic includes the annotated nodes to be used in the PSPICE simulation. The transfer function for the open-loop output impedance, Z_O, with a load of 14.4 Ω is expressed by (5.35). The frequency response of the open-loop output impedance is shown in Fig. 5.5 and Fig. 5.6. The results show the PSPICE model is in very good agreement with the analytical results achieved through Matlab. The value of r and r_C are close approximations for the output impedance at low and high frequency as expressed by (5.36) and (5.37) respectively. The impedance has a peak of 4.57 Ω (5.38). Note the output impedance has the same poles as the power stage.

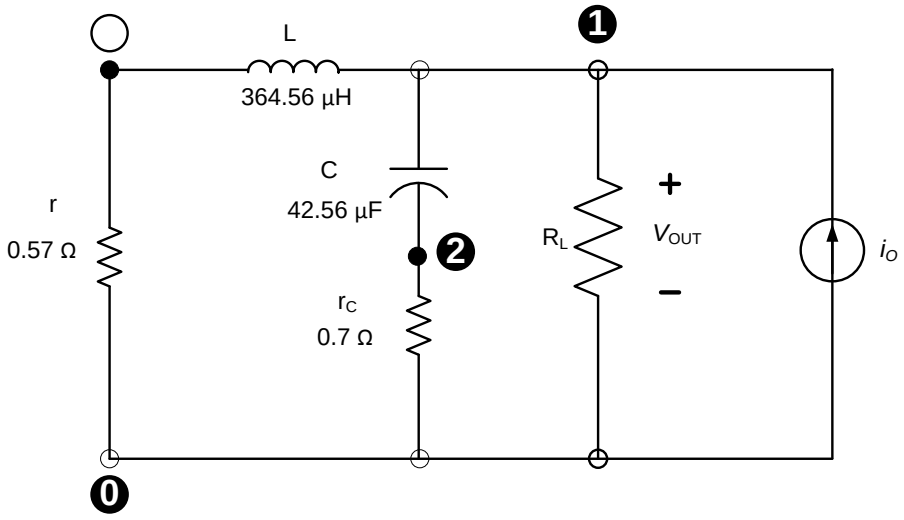

Figure 5.4: Schematic to determine open-loop output impedance

$$Z_o(s) \equiv -\frac{v_o(s)}{i_o(s)}\Big|_{v_i=d} = \frac{0.6675\left(s^2 + 3.524\times10^4\, s + 5.573\times10^7\right)}{s^2 + 5154s + 6.764\times10^7} \tag{5.35}$$

$$Z_o(0) = 0.55\ \Omega = -5.19\ \text{dB}\Omega \approx r \tag{5.36}$$

$$Z_o(\infty) = 0.67 = -3.48\ \text{dB}\Omega \approx r_C \tag{5.37}$$

$$Z_{o(peak)} = 4.57\ \Omega = 13.20\ \text{dB}\Omega \tag{5.38}$$

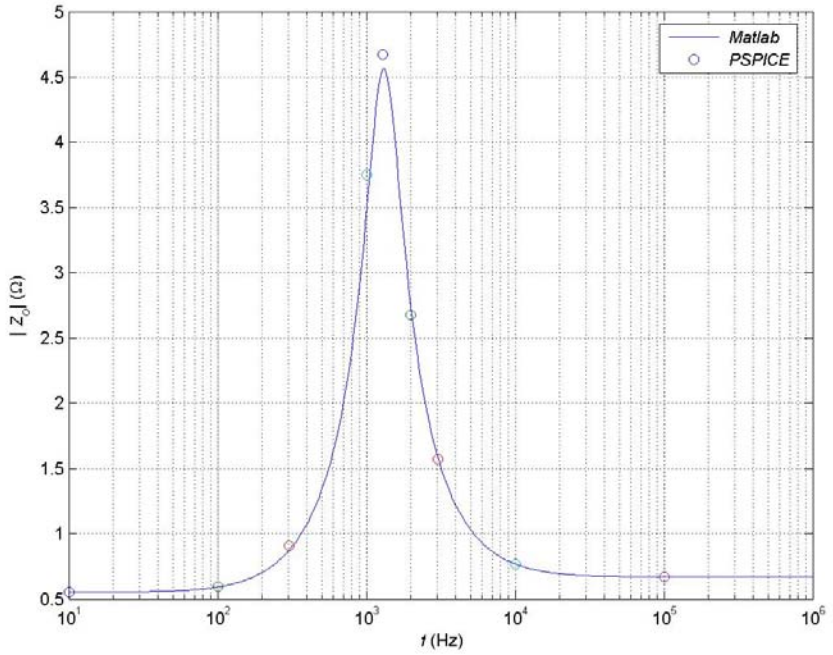

Figure 5.5: Magnitude of the open-loop output impedance, Z_O, with R_L = 14.4 Ω

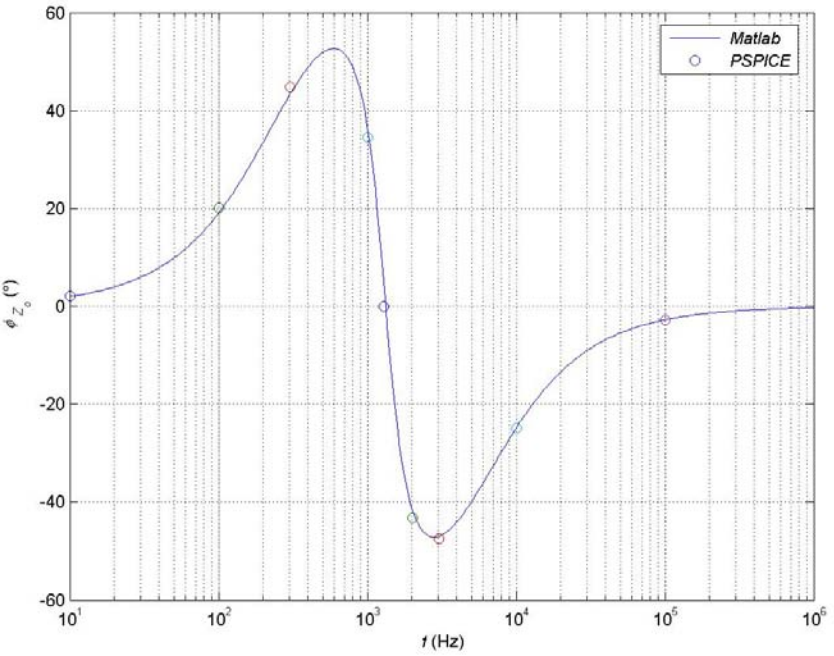

Figure 5.6: Phase of the open-loop output impedance, Z_O, with R_L = 14.4 Ω

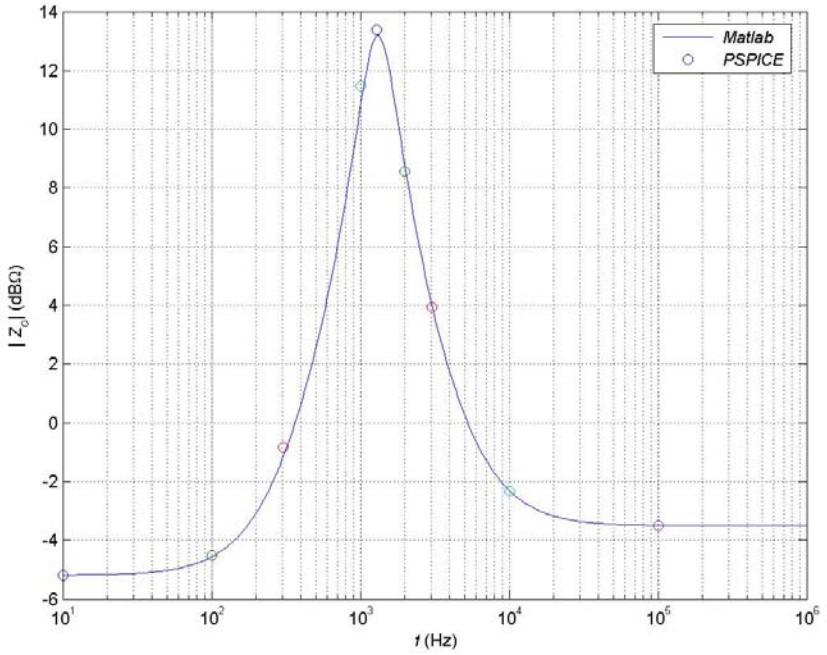

Figure 5.7: Magnitude of the open-loop output impedance, Z_O, with R_L = 14.4 Ω

5.3 Closed-loop design

With the power stage design complete, and the open-loop output impedance determined, the next step in the closed-loop design is to determine the allowable range for the parameters K_Z and ω_{Zocld}. The range for K_Z and ω_{Zocld} is given by (5.40) and (5.44), respectively.

$$0 < K_Z r_C \le \frac{V_{nom} - V_{\min}}{i_{L(\max)} - i_{L(\min)}} = \frac{(14.0 - 13.0)}{(0.9 - 0.5)} = 2.5 \tag{5.39}$$

$$0 < K_Z \le \frac{V_{nom} - V_{\min}}{r_C\left(i_{L(\max)} - i_{L(\min)}\right)} = \frac{(14.0 - 13.0)}{0.7(0.9 - 0.5)} = 3.57 \tag{5.40}$$

$$2\pi f_{critical} \le \omega_{Zocld} < \pi f_S \tag{5.41}$$

$$\frac{\pi}{2r_C C} \le \omega_{Zocld} < \pi f_S \tag{5.42}$$

$$\frac{\pi}{2\times 0.7\times\left(42.56\times 10^{-6}\right)} \le \omega_{Zocld} < \pi\left(100\times 10^{3}\right) \tag{5.43}$$

$$5.27\times 10^{4}\ {}^{\text{rad}}\!/_{\text{sec}} \le \omega_{Zocld} < 3.14\times 10^{5}\ {}^{\text{rad}}\!/_{\text{sec}} \tag{5.44}$$

The next step is to determine if some of the coefficients of the compensator transfer function, T_C, can be eliminated using Table 3.1 and Table 3.2. Coefficient c_3 can be eliminated by selecting K_Z to be equal to R/r_C expressed by (5.45). Since this result complies with the allowable range for K_Z as given by (5.40), we can eliminate coefficient c_3. Using this value for K_Z, coefficient c_2 can be eliminated if the result of (5.46) falls within the allowable range for ω_{Zocld}. The result shows that an allowable ω_{Zocld} cannot be found to eliminate c_2. In the same way, coefficient c_1 cannot be eliminated because the result of (5.47) is not within the allowable range for ω_{Zocld}.

$$\frac{R}{r_C} = \frac{R_{L(\min)}}{R_{L(\min)} + r_C} = \frac{14.4}{\left(14.4 + 0.7\right)} = 0.95 \tag{5.45}$$

$$\omega_{Zocld} = 2\xi\omega_0 - \omega_Z - \omega_{rl} = -3.0083\times 10^{4}\ {}^{\text{rad}}\!/_{\text{sec}} \tag{5.46}$$

$$\omega_{Zocld} = \frac{\omega_0^2 - \omega_Z\omega_{rl}}{\left(\omega_Z + \omega_{rl}\right)} = 337\ {}^{\text{rad}}\!/_{\text{sec}} \tag{5.47}$$

Now consider if coefficients c_2 and c_1 can be eliminated by using the equations presented in Table 3.2. The calculations are completed in (5.48) and (5.49). The results indicate that neither c_2 nor c_1 can be eliminated.

$$\omega_{Zocld} = \frac{\omega_o\left(\omega_Z + \omega_{rl}\right) - 2\xi\omega_Z\omega_{rl}}{2\xi\left(\omega_Z + \omega_{rl}\right) - \omega_o} = 1.8392\times 10^{4}\ {}^{\text{rad}}\!/_{\text{sec}} \tag{5.48}$$

$$K_Z = \frac{R\left(\omega_Z + \omega_{rl} + \omega_{Zocld}\right)}{2r_C\xi\omega_o} = 9.92 \tag{5.49}$$

It has been shown that only coefficient c_3 can be eliminated by choosing K_Z equal to R/r_C (5.50). Set ω_{Zocld} to the value which is well above the critical frequency as given by (5.51). Therefore, the transfer function of the desired closed-loop output impedance, Z_{ocld}, is expressed by (5.52).

$$K_Z = 0.95 \tag{5.50}$$

$$\omega_{Zocld} = 2\pi\left(20\times10^3\right) = 1.2566\times10^5 \ {}^{\text{rad}}\!/_{\text{sec}} \tag{5.51}$$

$$Z_{ocld}(s) = \frac{\left(\frac{R}{r_C}\right)r_C s}{s+\omega_{Zocld}} = \frac{Rs}{s+\omega_{Zocld}} = \frac{(0.6675)s}{s+1.2566\times10^5} \tag{5.52}$$

To complete the closed loop design, the values of the reference voltage, voltage divider, and modulator gain need to be selected. The reference voltage should be about half the value of the output voltage, therefore, select a reference voltage of 5 V. The voltage divider, β, is determined by (5.53). The modulator signal will be created by comparing the compensator output voltage to the voltage of a saw-tooth waveform. If the error voltage is above the reference voltage, the modulator will decrease the duty cycle of the modulator output, and if the error voltage is less than the reference voltage, the modulator will increase the duty cycle of the modulator output. The modulator gain is determined using (5.54) and (5.55), where V_{Tm} is the magnitude of the saw-tooth waveform.

$$\beta = \frac{v_{REF}}{v_{O(nom)}} = \frac{5}{14} = 0.357 \tag{5.53}$$

$$V_{Tm} \approx \frac{v_{REF}}{D_{nom}} = \frac{5}{0.573} = 8.72 \text{ V} \tag{5.54}$$

$$T_m = \frac{1}{10} = 0.1\ \mathrm{V}^{-1} \tag{5.55}$$

The next step is to determine the transfer function of the compensator using equations (3.23)-(3.28) developed in Chapter 3. Since K_Z has been set to eliminate c_3, the general form of the transfer function will be as expressed by (5.56). Solving for the coefficients yields the transfer function (5.62).

$$T_C(s) = T_{CX}\left[\frac{c_2 s^2 + c_1 s + 1}{d_2 s^2 + s}\right] \tag{5.56}$$

$$T_{CX} = \frac{V_{TM} L \omega_{rl} \omega_{Zocld}}{\beta V_I K_Z r_C} = 1.0766 \times 10^5 \tag{5.57}$$

$$c_2 = \left(\frac{\omega_Z + \omega_{rl} + \omega_{Zocld} - 2\frac{K_Z r_C}{R}\xi\omega_o}{\omega_Z \omega_{rl} \omega_{Zocld}}\right) = 2.224 \times 10^{-8} \tag{5.58}$$

$$c_1 = \left(\frac{\omega_Z \omega_{rl} + \omega_{Zocld}\omega_Z + \omega_{Zocld}\omega_{rl} - \frac{K_Z r_C}{R}\omega_o^2}{\omega_Z \omega_{rl} \omega_{Zocld}}\right) = 6.3057 \times 10^{-4} \tag{5.59}$$

$$d_2 = \frac{1}{\omega_Z} = 2.9782 \times 10^{-5} \tag{5.60}$$

$$T_C(s) = 1.0766 \times 10^5\left[\frac{\left(2.224 \times 10^{-8}\right)s^2 + \left(6.3057 \times 10^{-4}\right)s + 1}{\left(2.9782 \times 10^{-5}\right)s^2 + s}\right] \tag{5.61}$$

$$T_C(s) = 80.4\left[\frac{(s+1687)(s+26671)}{s(s+33579)}\right] \tag{5.62}$$

The transfer function of the compensator may be realized using the active filter shown in Fig. 5.8. Using the ideal op-amp assumptions that in the feedback configuration the plus and minus input have the same potential and draw no current, the

general form of the transfer function for the active filter can be shown to be (5.63). The impedances, Z_1, and Z_2, can by expressed be simplified to (5.64) and (5.65), which yields the transfer function for the compensator as (5.66).

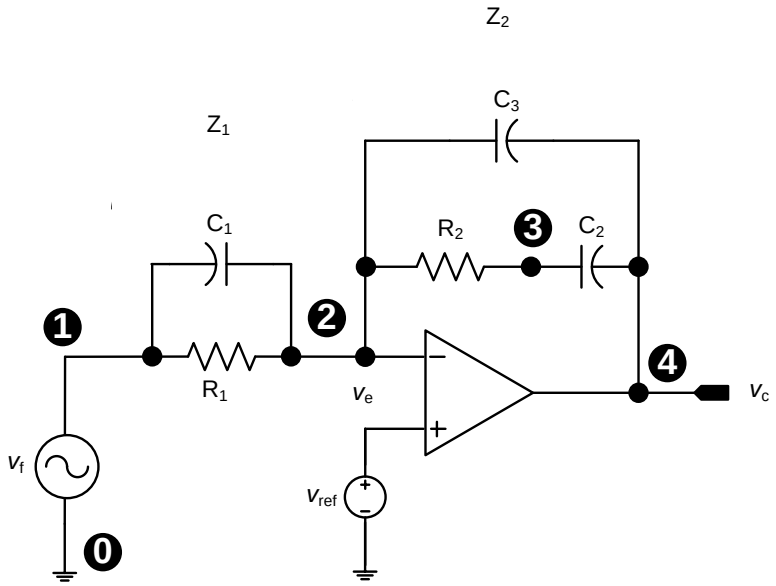

Figure 5.8: Compensator circuit with PSICE nodes

$$T_C(s) = \frac{v_C(s)}{v_f(s)} = -\frac{Z_2(s)}{Z_1(s)} \tag{5.63}$$

$$Z_2(s) = \left(R_2 + \frac{1}{sC_2} \right) \Bigg\| \frac{1}{sC_3} = \frac{1}{sC_3} \frac{s + \dfrac{1}{R_2 C_2}}{s\left[s + \dfrac{C_2 + C_3}{R_2 C_2 C_3} \right]} \tag{5.64}$$

$$Z_1(s) = R_1 \| \frac{1}{sC_1} = \frac{1}{C_1} \frac{1}{s + \dfrac{1}{R_1 C_1}} \tag{5.65}$$

$$T_C(s) = -\frac{C_1}{C_3} \frac{\left(s + \dfrac{1}{R_1 C_1} \right)\left(s + \dfrac{1}{R_2 C_2} \right)}{s\left[s + \dfrac{C_2 + C_3}{R_2 C_2 C_3} \right]} \tag{5.66}$$

To realize the compensator, the component values need to be determined. Standard values will be used for capacitors and resistors. Begin with component selection by picking R_2 to be 10 kΩ. C_2 can then be determined using (5.67). Pick C_2 to be 3.9 nF. Capacitor C_3 is determined using (5.69). Select C_3 to be 12 nF. The value of C_1 is calculated by (5.70). Pick C_1 to be 1.0 µF. R_1 is determined using the selected value of C_1 and the zero, ω_{Z1}, as given by (5.71). Select R_1 to be 620 Ω. The selected parameters are summarized in Table 5.3.

$$C_2 = \frac{1}{R_2 \omega_{z2}} = \frac{1}{10000 \times 26671} = 3.75 \times 10^{-9} \text{ F} \tag{5.67}$$

$$\omega_p = \frac{C_2 + C_3}{R_2 C_2 C_3} \tag{5.68}$$

$$C_3 = \frac{C_2}{\left(\omega_p R_2 C_2 - 1\right)} = \frac{3.9x10^{-9}}{33579 \times 10000 \times \left(3.9 \times 10^{-9}\right) - 1} = 12.6 \times 10^{-9} \text{ F} \tag{5.69}$$

$$C_1 = T_{CX} C_3 = (80)\left(12 \times 10^{-9}\right) = 0.96 \times 10^{-6} \text{ F} \tag{5.70}$$

$$R_1 = \frac{1}{\omega_{Z1} C_1} = \frac{1}{(1687)\left(1.2 \times 10^{-6}\right)} = 493\,\Omega \tag{5.71}$$

Parameter	Value	Unit
C_1	1.0	µF
C_2	3.9	nF
C_3	12	nF
R_1	620	Ω
R_2	10	kΩ

Table 5.3: Compensator components

The frequency response of the compensator is presented in Fig. 5.9 and Fig. 5.10. A comparison is provided between the analytical results achieved using Matlab, and the circuit simulation using PSPICE shows very good agreement. The deviation at high frequency can be decreased by choosing an op-amp with a high gain-bandwidth product. The single pole op-amp was used to realize the compensator in PSPICE. The code is shown in the appendix.

Fig. 5.11 shows the closed-loop buck converter with the linear small-signal model employed for the switch and diode. To determine the frequency response of the output impedance, the input voltage signal and reference voltage is set to zero. Fig. 5.12 shows the schematic used to determine the closed-loop output impedance. The source is the load current, i_O. The output impedance is measured by measuring the steady-state output voltage divided by the load current. The op-amp buffer circuit was inserted between the voltage divider and the compensator to ensure the load of the feedback network does not affect the load applied to the converter. The frequency response of the closed-loop output impedance is presented in Fig. 5.13 through Fig. 5.15. The analytical results are in very good agreement with the results of the hardware simulation.

Fig. 5.16 shows the schematic of the closed-loop buck converter that will be used to measure the step response of the output voltage, v_O, to a step change in load current, i_O. The step response is shown in Fig. 5.17. The response shows the output voltage complies with the specifications given in the military standard as designed. The PSPICE model with the compensator circuit is in good agreement with the analytical results. In the next section, hardware will be realized and tested to verify the expected results.

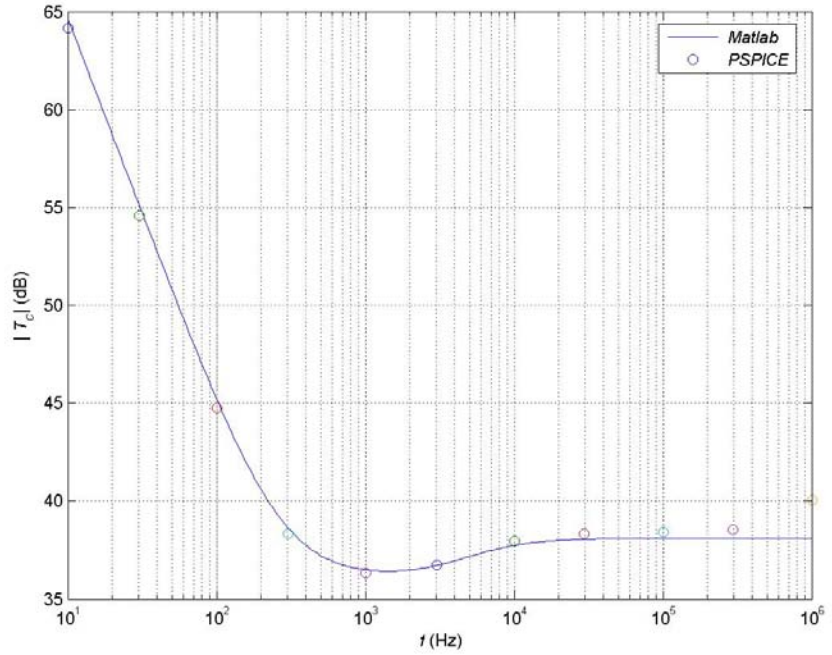

Figure 5.9: Magnitude of Compensator, T_C

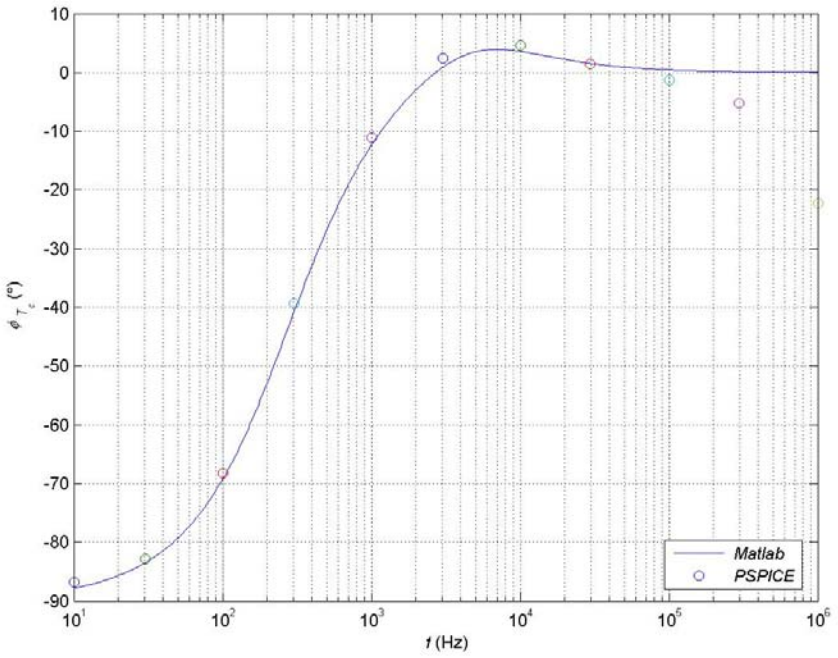

Figure 5.10: Phase of compensator, T_C

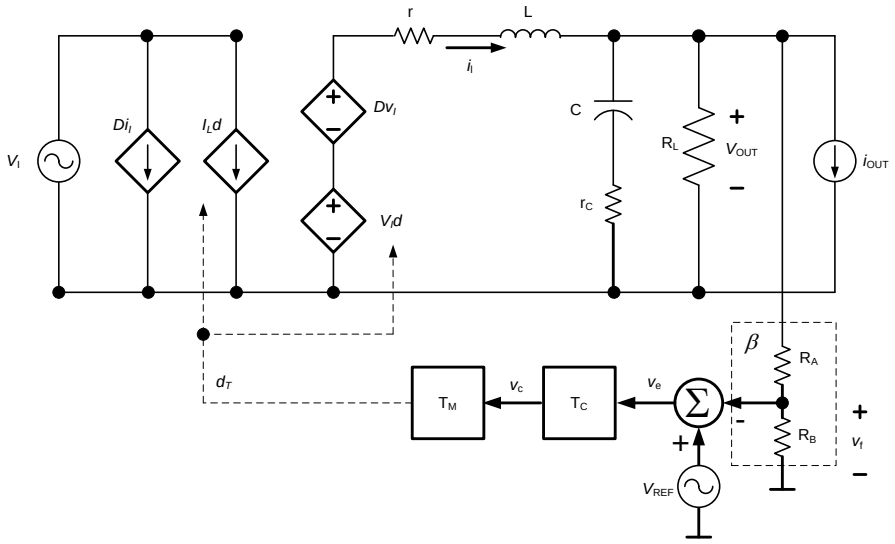

Figure 5.11: Linear small-signal model of PWM Buck Converter with VMC

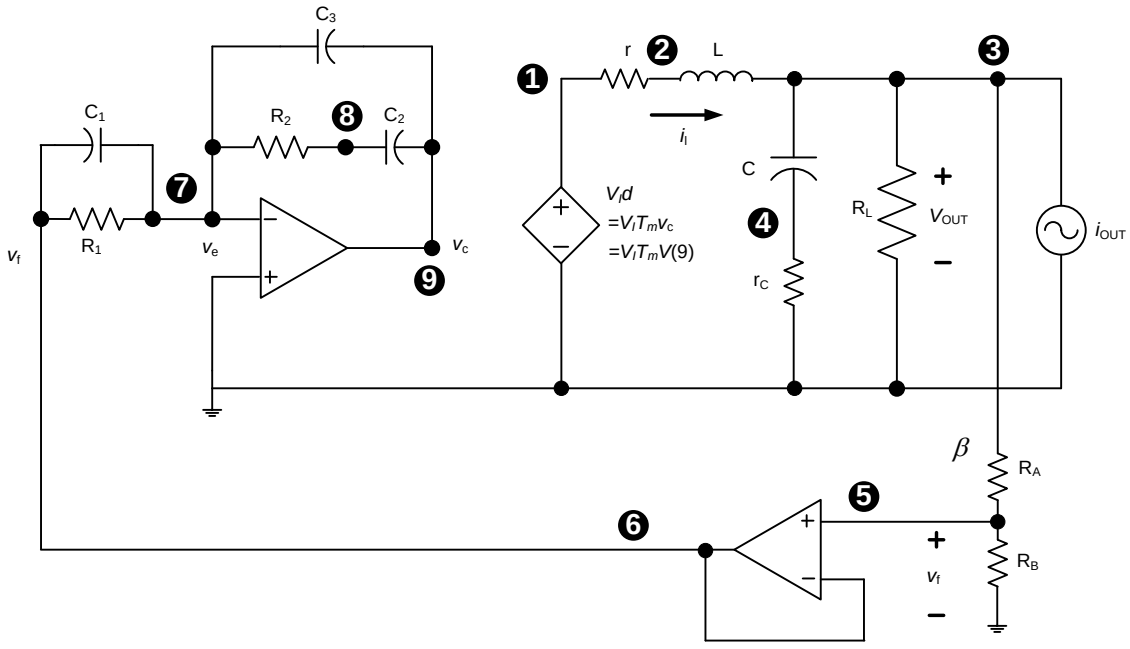

Figure 5.12: Schematic of Buck Converter to measure closed-loop output impedance

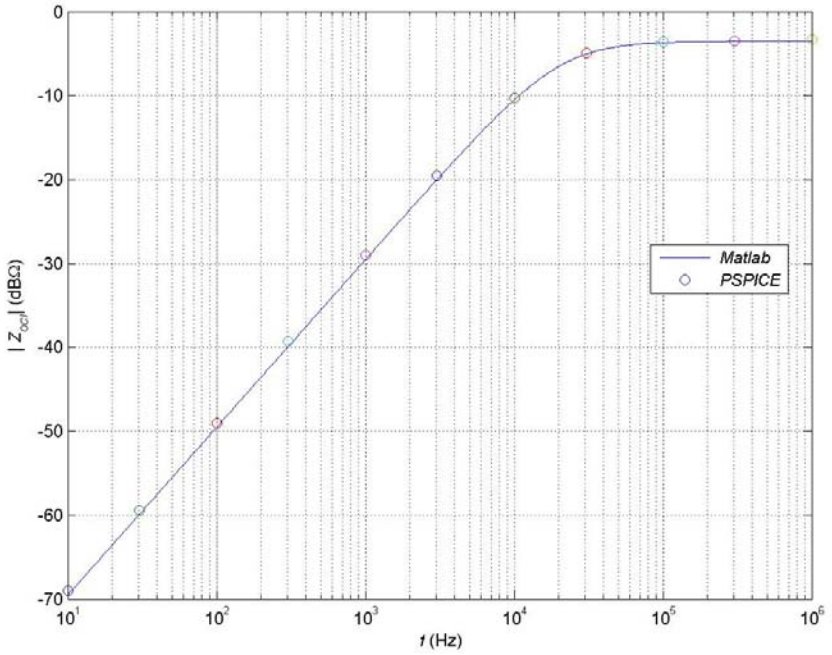

Figure 5.13: Magnitude of closed-loop output impedance with compensator

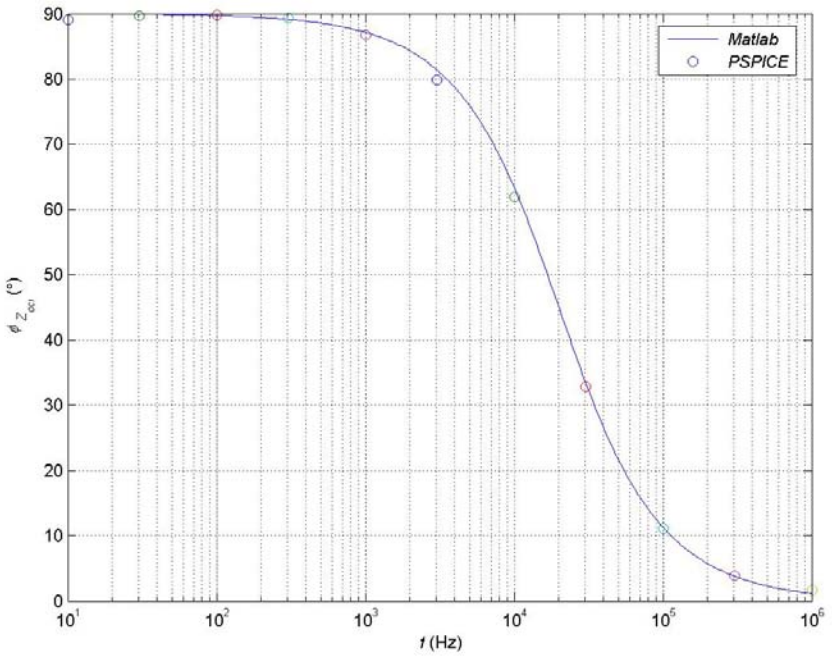

Figure 5.14: Phase of closed-loop output impedance with compensator

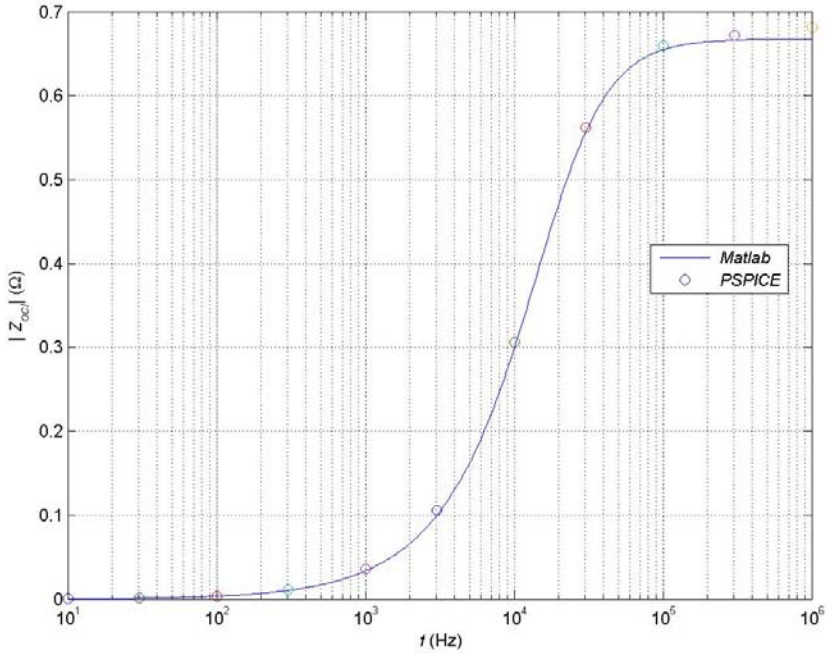

Figure 5.15: Magnitude of closed-loop output impedance with compensator

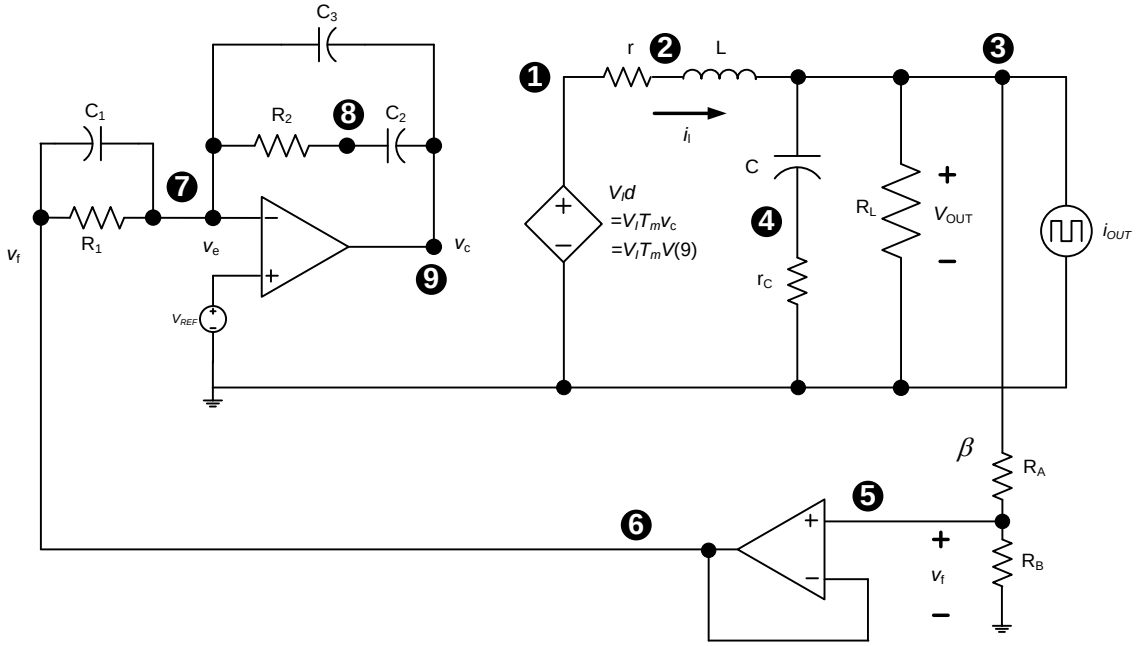

Figure 5.16: Schematic of Buck Converter to measure closed-loop response to step change in load current

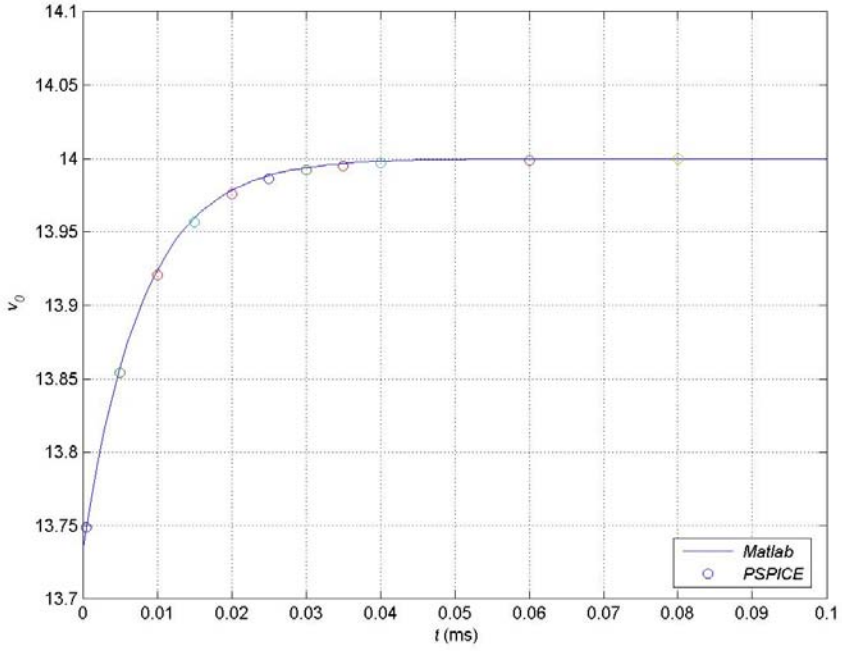

Figure 5.17: Response of closed-loop Buck Converter to a step change in load current, i_O, from 0.5 to 0.9 A

5.4 Hardware realization and testing

A Buck Converter to comply with the MIL-STD-704F requirements presented in the last section was synthesized to further demonstrate the design methodology. The circuit consists of a buck converter, voltage divider, error amplifier (compensator), pulse-width modulator, and a MOSFET driver. The circuit consists of an International Rectifier IRF530 power MOSFET, an International Rectifier MUR820 power diode, and an output filter comprised of a toroid inductor, electrolytic capacitor, and load resistor. The input voltage is supplied by a power supply. The inductor was measured to have an inductance of 364 µH and an ESR of 0.3 Ω at the operating frequency and the capacitor was measured to have a capacitance of 42.5 µF and an ESR of 0.7 Ω at the operating

frequency. The voltage divider used a 10 kΩ potentiometer adjusted to provide 5 V when the input is 14 V. As a result, β = 0.35.

The error amplifier or compensator was realized using a Linear Technology LT1222 operational amplifier. This operational amplifier was chosen to meet the high gain-bandwidth product required to properly realize the desired transfer function of the compensator. A dc reference voltage of 5 V is supplied by a LM regulator. The operational amplifier as well as the rest of the ICs used a V_{CC} = 15 V supplied by an LM regulator.

The pulse-width modulator is comprised of a Texas Instrument TLE2074 comparator and a saw-tooth voltage generator as shown in Fig. 5-18 and Fig. 5-19. The saw-tooth generator is comprised of an ST Microelectronics 2N3904 NPN transistor driven by a 100 kHz pulse supplied by a Texas Instrument TLC555 configured as an astable, an LF356N operational amplifier, a capacitor C_C = 6.4 nF, and a resistance R_C = 15 kΩ, resulting in $\tau_C = R_C C_C$ = 96 μs, and $\mu = T/\tau_C$ = 100/96 = 0.104. The output of the saw-tooth generator is a 0 to 10 V ramp with a frequency of 100 kHz. The PWM signal is determined by comparing the output of the error amplifier to the saw-tooth signal.

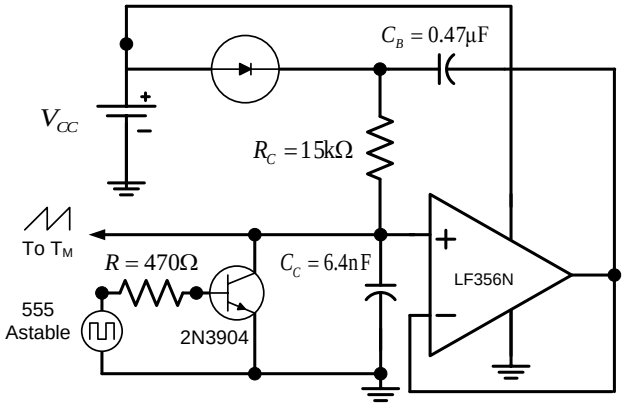

Figure 5.18: Saw-tooth Generator Circuit

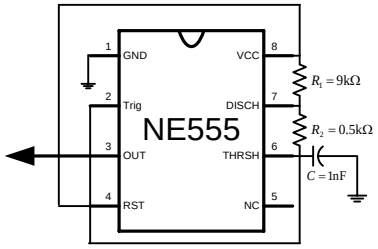

Figure 5.19: Astable circuit used to trigger saw-tooth generator

An International Rectifier IR2110E driver was used to drive the MOSFET with the PWM signal. A 1N4001 diode, and two capacitors, C_{D1} = 0.1 µF and C_{D2} = 1 µF were used to configure the driver as shown in Fig. 5-20.

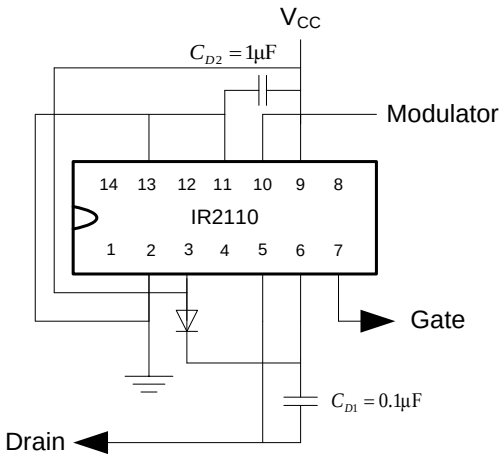

Figure 5.20: MOSFET drive circuit

The following instruments were used to develop and test the PWM Buck Converter:

- Topward 6302A Dual Power Supply
- Tektronix CFG280 Function Generator
- Tektronix TDS420A Oscilloscope

5.4.1 *Characterization of Power Stage*.

The power stage was characterized by measuring the dc transfer function, efficiency, and frequency response of the output filter. The dc transfer function was measured over the range of input and output voltages shown in Table 5-4. The resistors were chosen to be near the minimum and maximum load values. The results show the efficiency is near 95 % which is better than the estimated value of 90%. The nominal duty cycle is 0.525.

$R_L(\Omega)$	$V_I(V)$	$V_O(V)$	D	M_{VDC}	η
24.6	24.0	15.0	0.648	0.625	0.965
24.6	28.0	14.0	0.524	0.500	0.954
24.6	32.0	13.0	0.428	0.410	0.958
16.4	24.0	15.0	0.654	0.625	0.956
16.4	28.0	14.0	0.526	0.500	0.951
16.4	32.0	13.0	0.434	0.411	0.948

Table 5.4: DC Transfer Function and Efficiency

The frequency response of the output filter was measured for comparison to the analytical results. The input voltage was applied at the input to the inductor and the output voltage was measured across the 16.4 Ω load resistor. The frequency response of the magnitude and phase is shown in Fig. 5-21 and Fig. 5-22. The data points measured from the actual hardware are in good agreement with the theoretical results achieved with Matlab.

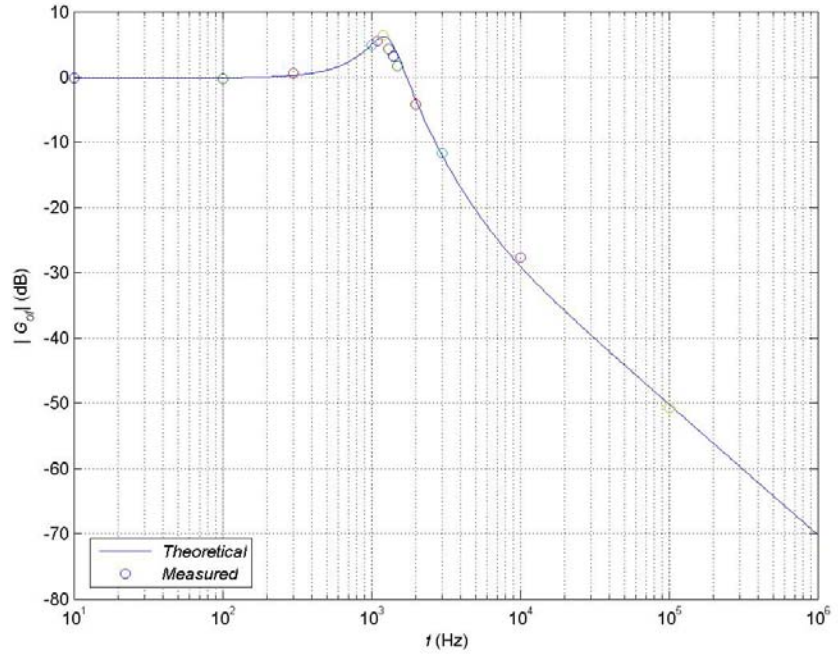

Figure 5.21: Magnitude response of Output Filter with R_L = 16.4 Ω

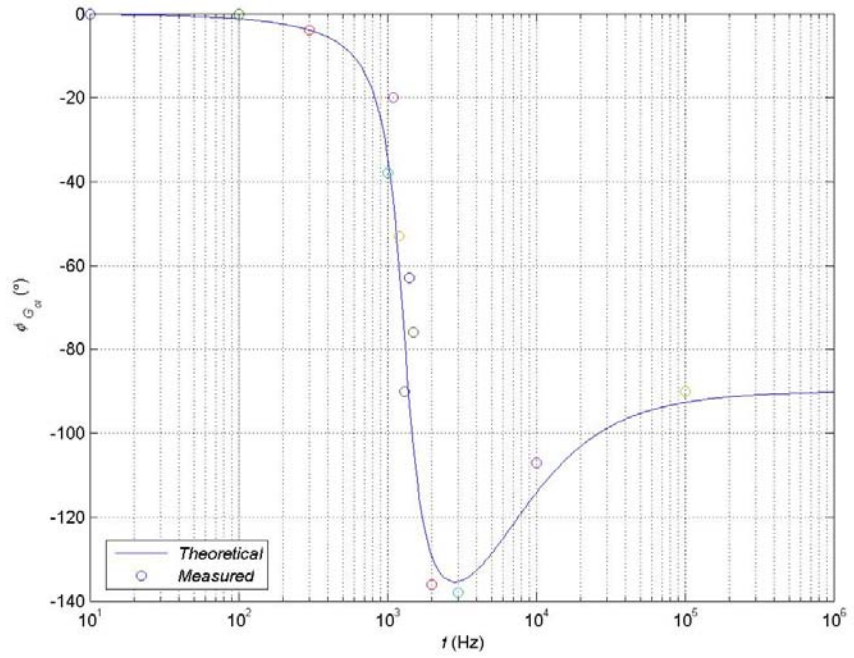

Figure 5.22: Phase Response of Output Filter with R_L = 16.4 Ω

5.4.2 *Open-loop Output Impedance.*

Fig. 5.23 shows the circuit that is used to measure the frequency response of the open-loop output impedance as well as the step response of the output voltage to a step change in load. In Fig. 5.23, a current sink circuit is connected to the output of the buck converter. The input voltage, V_I, is set to the nominal input voltage, 28 V. A fixed error voltage is applied to the comparator in order to generate a PWM with the nominal duty cycle. The output voltage from the open-loop converter is the nominal output voltage, 14V. This voltage is the drain voltage for the current sink MOSFET. The gate voltage is biased to keep the current sink MOSFET in saturation. A 1 Ω resistor is applied from source to ground serving as the output current sense resistor. To measure the frequency response, a small signal is applied to the gate, and the output impedance is equal to the signal measured across the output resistor, R_L, divided by the amplitude of the output current. The step response is measured by applying a step input as the gate signal while measuring the output voltage.

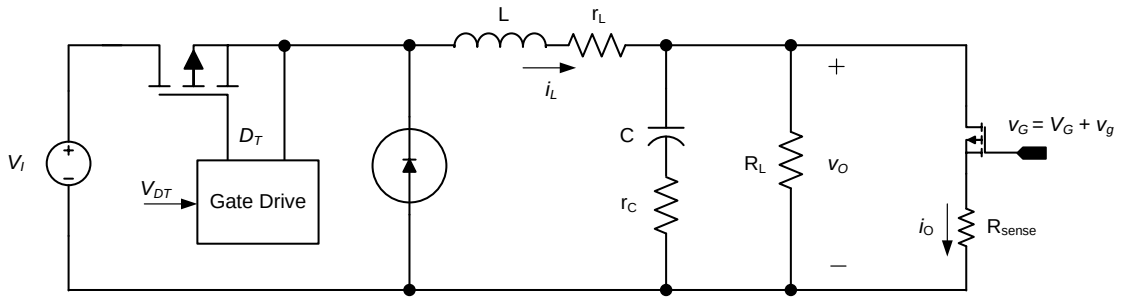

Figure 5.23: Open-loop Buck Converter with Current Sink to measure output impedance

Fig. 5.24 through Fig. 5.26 shows the frequency response of the open-loop output impedance at nominal input voltage, nominal duty cycle, and maximum load. The measured results are in good agreement with the analytical results.

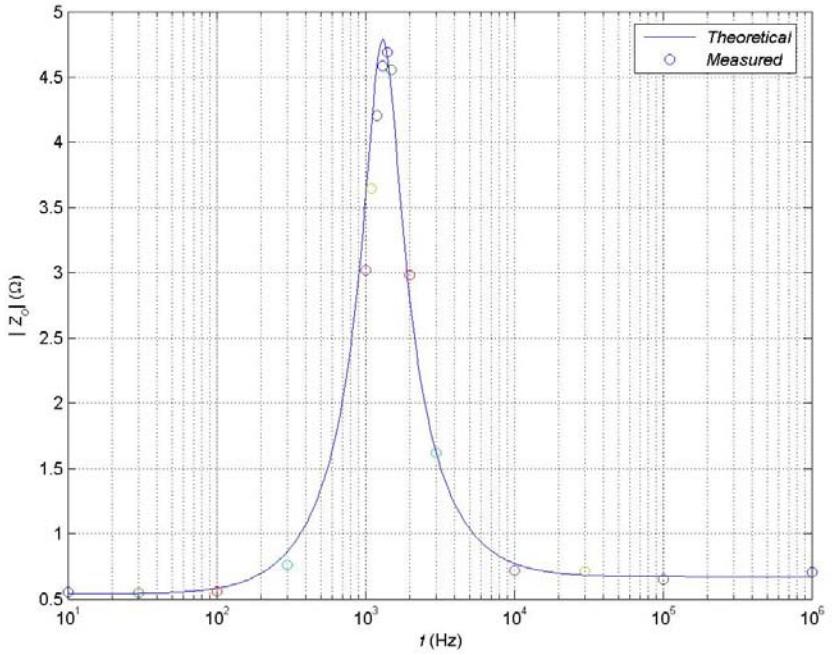

Figure 5.24: Magnitude of open-loop output impedance at V_I = 28 V, D_T = 0.525, and R_L = 16.4 Ω

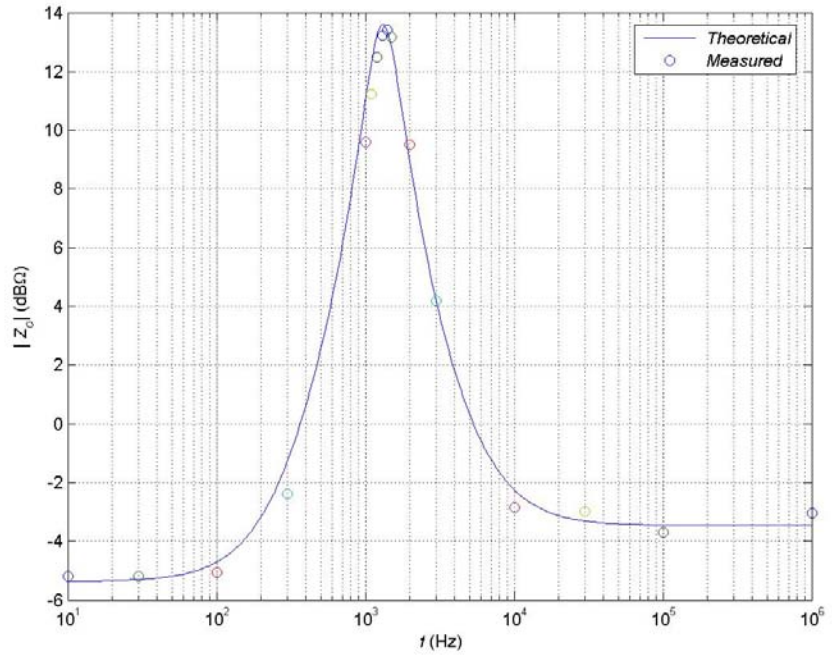

Figure 5.25: Magnitude of open-loop output impedance at V_I = 28 V, D_T = 0.525, and R_L = 16.4 Ω

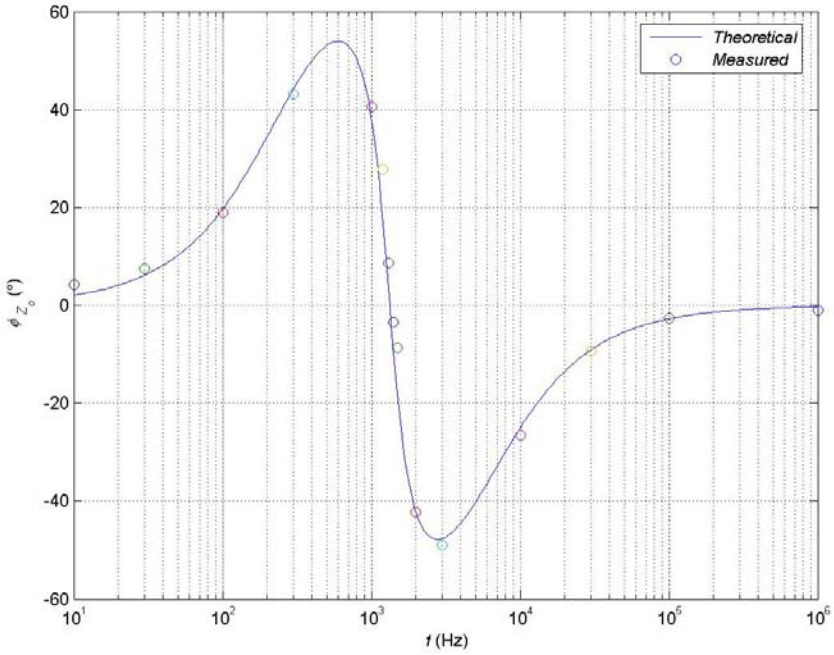

Figure 5.26: Phase of open-loop output impedance at V_I = 28 V, D_T = 0.525, and R_L = 16.4 Ω

Fig. 5.27 shows the step response of the output voltage to a step change in load current from 0.56 A to 0.85 A. The measured results are in good agreement with the model. The response has an initial spike equal to the product of step change in load and the output impedance according to (5.71). The initial output voltage in response to the step change in load falls to 13.804 as determined in (5.72).

$$\left|v_{spike}\right| = r_C \Delta i = 0.7 \times 0.28 = 0.196 \text{ V} \tag{5.71}$$

$$v_O = V_O - \left|v_{spike}\right| = 14.0 - 0.196 = 13.804 \text{ V} \tag{5.72}$$

5.4.3 *Hardware compensator frequency response.*

The transfer function for the compensator was determined using the previously presented method with R_L = 16.4 Ω is given in (5.73). The component values required to synthesis the compensator are given in Table 5.5. The Linear Technology LT1222

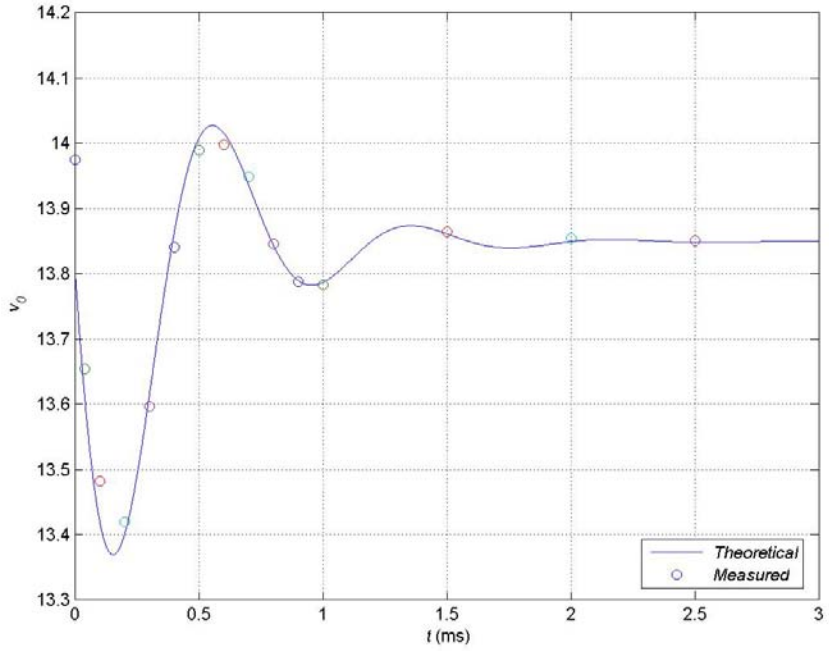

Figure 5.27: Response of output voltage to a step change in load current from 0.56 A to 0.84 A with V_I = 28 V, D_T = 0.525, and R_L = 16.4 Ω

Operational Amplifier was used to implement the compensator using the topology presented in Fig. 5.8. The frequency response of the compensator is presented in Fig. 5.28 and Fig. 5.29. The hardware measurements at selected frequencies are in close agreement with the simulated results.

$$T_C(s) = 80\left[\frac{(s+1650)(s+26550)}{s(s+33580)}\right] \tag{5.73}$$

The frequency response of the loop gain was measured at the nominal input voltage by applying an AC signal at the modulator input and measuring the output of the compensator. The response is shown in Fig. 5.30 and 5.31. The plot shows the cross-over frequency is 25 kHz and the phase margin is 82 degrees.

Parameter	Value	Unit
C_1	1.2	µF
C_2	3.75	nF
C_3	15	nF
R_1	505	Ω
R_2	10	kΩ

Table 5.5: Hardware compensator components

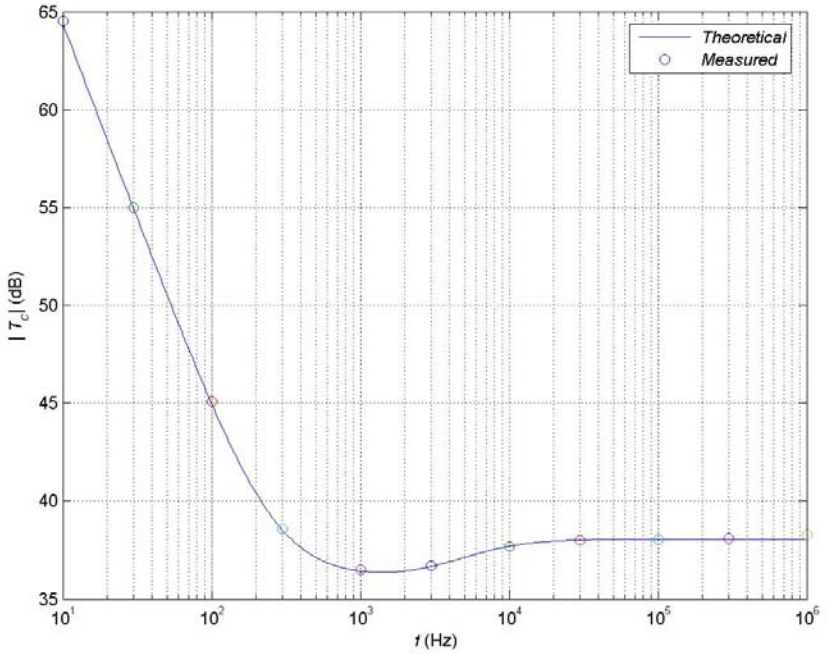

Figure 5.28: Magnitude of hardware compensator / error amplifier

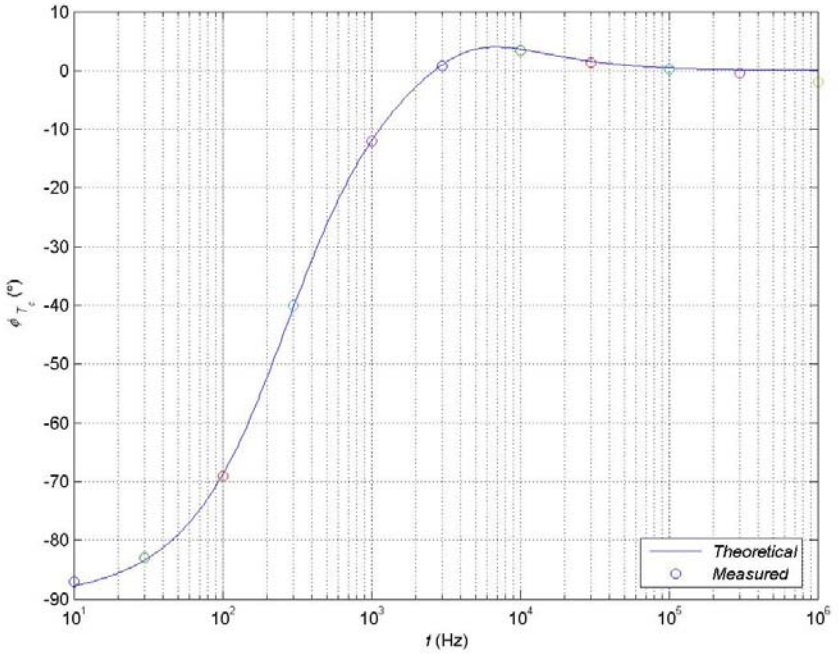

Figure 5.29: Phase of hardware compensator / error amplifier

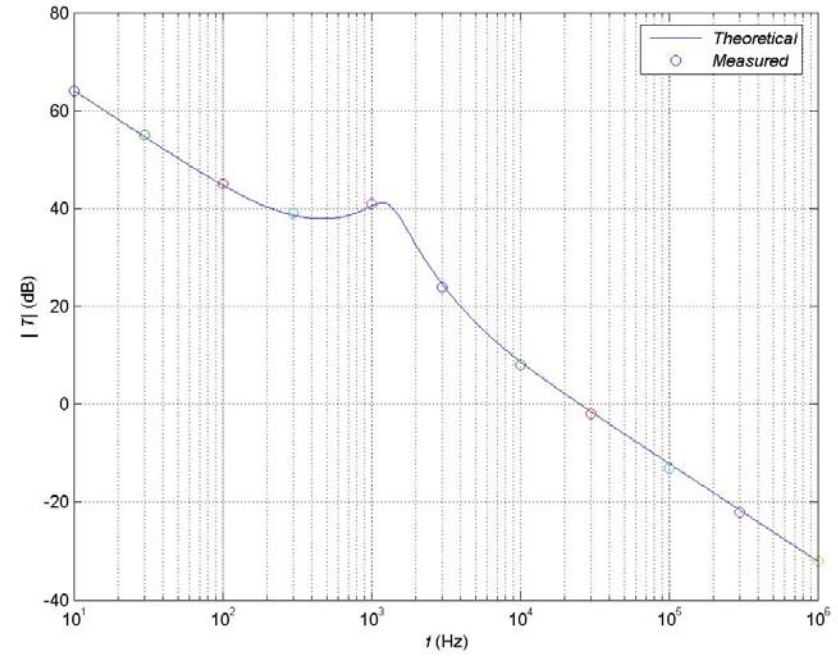

Figure 5.30: Magnitude of loop gain with V_I = 28 V, R_L = 16.4 Ω, L = 364 µH, r_L = 0.3 Ω, C = 42 µF, r_C = 0.7 Ω, r_{DS} = 0.4 Ω, R_F = 0.1 Ω, r = 0.57 Ω, T_M = 0.1, and β = 0.35

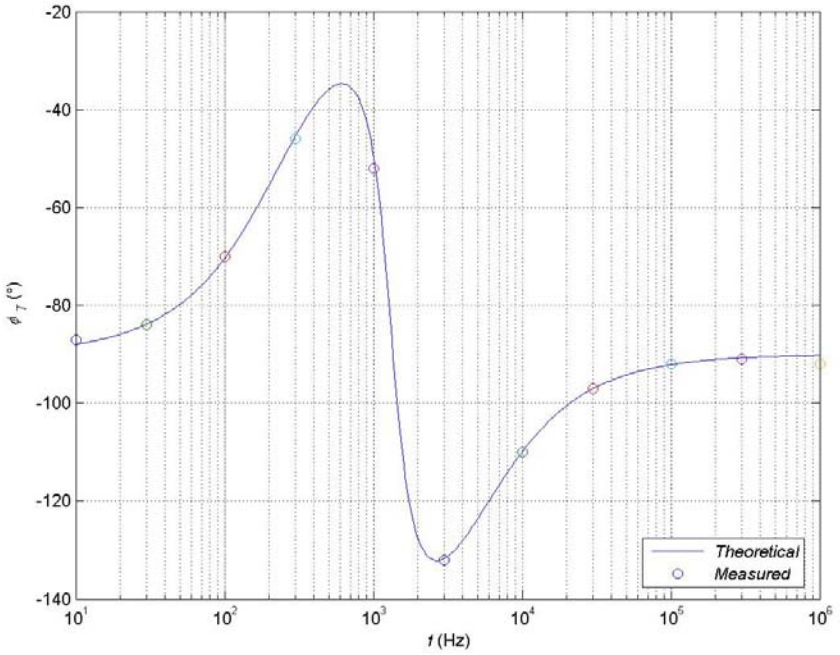

Figure 5.31: Phase of loop gain with V_I = 28 V, R_L = 16.4 Ω, L = 364 µH, r_L = 0.3 Ω, C = 42 µF, r_C = 0.7 Ω, r_{DS} = 0.4 Ω, R_F = 0.1 Ω, r = 0.57 Ω, T_M = 0.1, and β = 0.35

5.4.4 *Closed-loop output impedance.*

The final step to verify the hardware is to measure the frequency response of the output impedance and the step response to a step change in load. Fig. 5.32 shows the circuit used to make the measurements. The current sink circuit is used in the same manner as it was to measure the open-loop response. The input and measurements are the same as those used with the open-loop circuit. The input voltage is fixed at the nominal voltage, 28 V. The load resistance is 16.4 Ω. The duty cycle is not fixed; it adjusts to the input from the comparator.

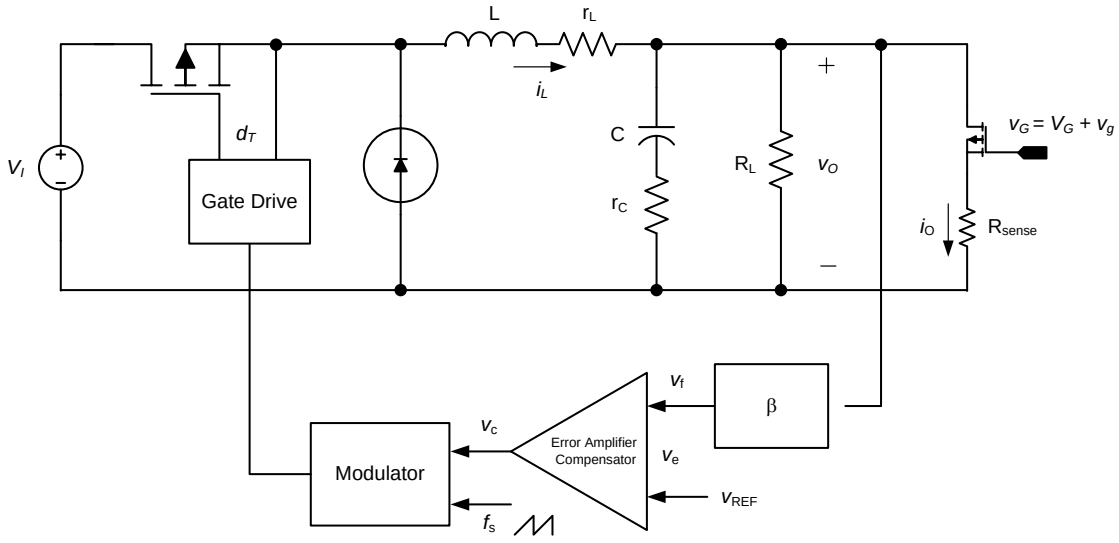

Figure 5.32: Closed-loop Buck Converter with Current Sink to measure Z_{ocl}

Fig. 5-33 through Fig. 5-35 present the frequency response of the closed-loop output impedance. In each figure, the result measured from the actual hardware circuit is compared to the expected result provided by the Matlab simulation. The figures show the hardware is in close agreement with the expected results. The compensator improved the closed-loop output impedance as designed.

Fig. 5-36 provides the response of the Buck Converter to a step change in load current from 0.56 A to 0.84 A. The response is in good agreement with the expected result. The voltage spike is equal to the product of the peak closed-loop output impedance and the step change in load according to (5.74). The minimum output voltage is given by (5.75).

$$\left|v_{spike}\right| = K_Z r_C \Delta i = 0.959 \times 0.7 \times 0.28 = 0.187 \text{ V} \tag{5.74}$$

$$v_O = V_O - \left|v_{spike}\right| = 14.0 - 0.187 = 13.813 \text{ V} \tag{5.75}$$

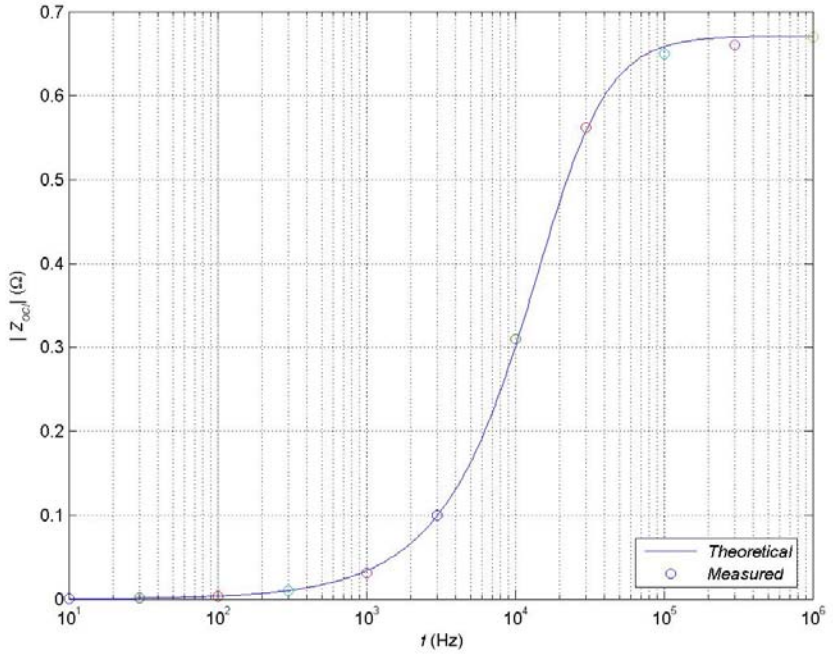

Figure 5.33: Magnitude of closed-loop output impedance at V_I = 28 V and R_L = 16.4 Ω

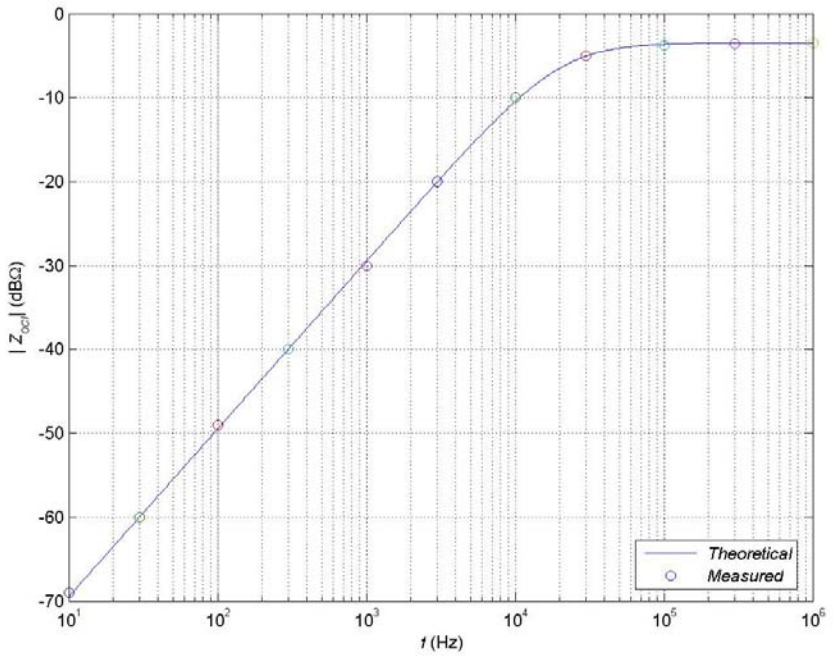

Figure 5.34: Magnitude of closed-loop output impedance at V_I = 28 V and R_L = 16.4 Ω

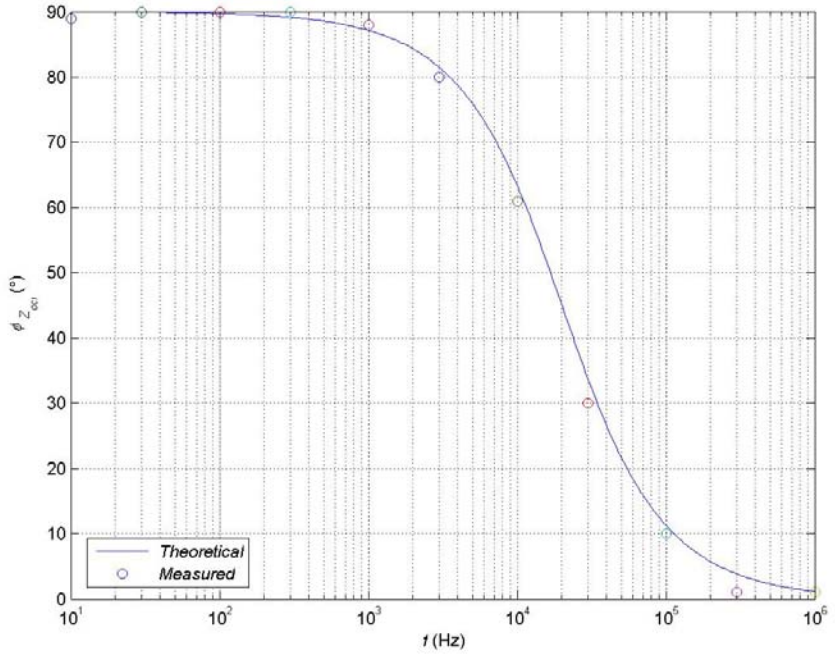

Figure 5.35: Phase of closed-loop output impedance at V_I = 28 V and R_L = 16.4 Ω

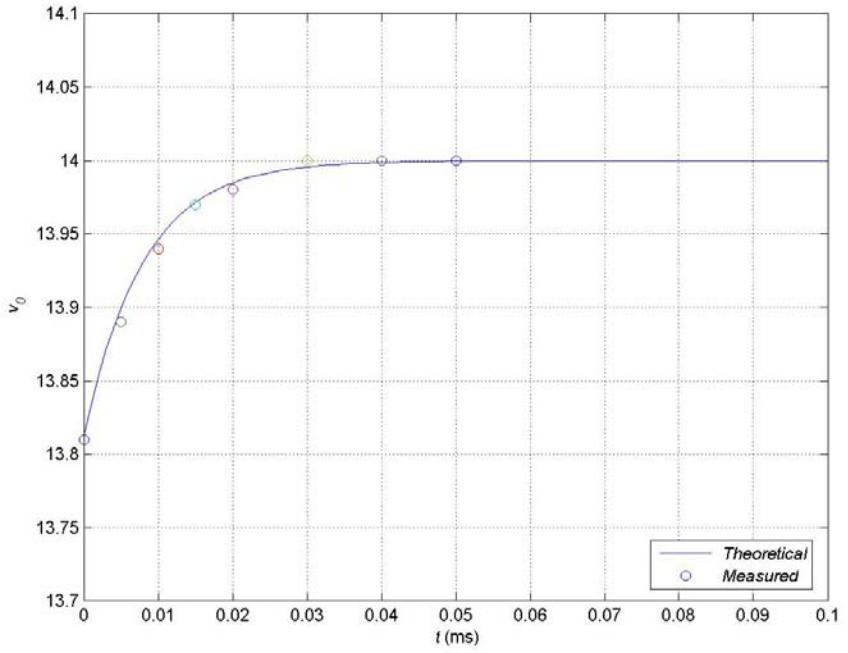

Figure 5.36: Response of output voltage to a step change in load current from 0.56 A to 0.84 A with V_I = 28 V and R_L = 16.4 Ω

6 Summary and Future Work

Reducing the output impedance of the buck converter is a pressing challenge. Common methods include multiple feedback loops, current sensors, and/or output capacitors with low ESR to meet design requirements. The PWM buck converter with VMC offers a size and cost advantage over other topologies and control schemes. In this paper, a method was presented to design a compensator for the PWM buck converter with VMC to achieve a specific closed-loop output impedance. The converter uses a single voltage feedback loop and does not rely entirely on low ESR output capacitors. The loop gain is designed in a way to achieve the desired closed-loop output impedance without relying entirely on low ESR output capacitors. The closed-loop output impedance is specified to be a first-order transfer function with a transient response to comply with given requirements. The transfer function for the compensator was developed. It was shown that a third-order compensator was sufficient to achieve the closed-loop output impedance. Additional tests were rigorously developed to determine if the order of the compensator can be further reduced.

An area of future work could be to apply these concepts to improve the efficiency of the power amplifier used in the envelope tracking technique for RF signal transmission. The main goal of the envelope tracking technique is to maintain a high efficiency over a wide range of the input power [22]. This system uses a power amplifier with dynamic control of the power supply (dc-dc converter). The efficiency of the power amplifier at

the resonant frequency is proportional to the ratio of the signal amplitude divided by the supply voltage. To maximize efficiency, the power supply must provide a voltage that is equal to the signal amplitude. Therefore, the power supply must be able to dynamically respond to rapid change in input voltage. The future work would be to apply the concepts presented in this paper to improve the dynamic response of the dc-dc converter to a step change in input voltage for the purpose of improving the efficiency of the envelope tracking transmitter. In addition, these concepts could be applied to other topologies of dc-dc converters.

7 PSPICE Code Used in Design of Aircraft Electric Power Regulator

7.1 Power Stage Filter

```
EE898 G Cazzell
*
* Student:      Greg Cazzell
* Phone:        (937) 291-1252
* email:        cazzell.2@wright.edu
* Diss.:        Output Impedance in Buck Converter
*
** Filename:   Gpsf bode V1.cir
*
* Aircraft Electric Power Regulator
* MIL-STD-704F
* Design Specifications
* ---------------------
* VImin = 24V;  VInom = 28V; VImax = 32V
* Dnom*VInom = 0.573*28 = 16.04V
* Vo = 14V; n = 90%; Vr < 0.2V
* Iomin = 0.5; Iomax = 0.9A
* fs = 100kHz; T = 0.01ms; DnomT = 0.00573ms;
* Dmin = 0.451; Dnom = 0.573; Dmax = 0.694
* RLmin = 14.4; RLmax = 30.0;
* Gpsf: Bode plot
*
* Circuit
* -------
VI              1               0                                       AC 1.0
r               1               2                                       0.5719
L               2               4                                       364.56uH
C               4               3                                       42.56uF
rc              3               0                                       0.7
RL              4               0                                       14.4
*
* Analysis settings
* -----------------
.AC DEC 20 10HZ .1MEGHZ
*
* View Results
```

```
* ------------
.PLOT AC V(4)
.PROBE
.END
```

7.2 Open-loop Output Impedance

```
EE898 G Cazzell
*
* Student:      Greg Cazzell
* Phone:        (937) 291-1252
* email:        cazzell.2@wright.edu
* Diss.:        Output Impedance in Buck Converter
*
** Filename:   Zo bode V1.cir
*
* Aircraft Electric Power Regulator
* MIL-STD-704F
* Design Specifications
* ---------------------
* VImin = 24V;  VInom = 28V; VImax = 32V
* Dnom*VInom = 0.573*28 = 16.04V
* Vo = 14V; n = 90%; Vr < 0.2V
* Iomin = 0.5; Iomax = 0.9A
* fs = 100kHz; T = 0.01ms; DnomT = 0.00573ms;
* Dmin = 0.451; Dnom = 0.573; Dmax = 0.694
* RLmin = 14.4; RLmax = 30.0;
* Zo: Bode plot
*
* Circuit
* -------
Io              1               0                       AC -1
RL              1               0                       14.4
C               1               2                       42.65uF
rc              2               0                       0.7
L               1               3                       364.56uH
r               3               0                       0.5719
*
* Analysis settings
* -----------------
.AC DEC 20 10HZ .1MEGHZ
*
* View Results
* ------------
.PLOT AC V(1)
```

```
.PROBE
.END
```

7.3 Frequency response of Compensator

```
EE898 G Cazzell
*
* Student:      Greg Cazzell
* Phone:        (937) 291-1252
* email:        cazzell.2@wright.edu
* Diss.:        Output Impedance in Buck Converter
*
** Filename:   Tc bode V2.cir
*
* Aircraft Electric Power Regulator
* MIL-STD-704F
* Design Specifications
* ---------------------
* VImin = 24V;  VInom = 28V; VImax = 32V
* Dnom*VInom = 0.573*28 = 16.04V
* Vo = 14V; n = 90%; Vr < 0.2V
* Iomin = 0.5; Iomax = 0.9A
* fs = 100kHz; T = 0.01ms; DnomT = 0.00573ms;
* Dmin = 0.451; Dnom = 0.573; Dmax = 0.694
* RLmin = 14.4; RLmax = 30.0;
* Tc: Bode plot
*
* Circuit
* -------
VI          1          0                              AC -1
C1          1          2                              1.0u
R1          1          2                              620.
XOP         0          2          4                   OPAMP1
R2          2          3                              10000
C2          3          4                              3.9n
C3          2          4                              12.n
*
*OPMODEL1.CIR - OPAMP MODEL SINGLE-POLE
*
* OPAMP MACRO MODEL, SINGLE-POLE
* connections:              non-inverting input
*                           |   inverting input
*                           |   |   output
*                           |   |   |
.SUBCKT OPAMP1              1   2   6
```

```
* INPUT IMPEDANCE
RIN          1          2                                   10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EGAIN        3          0          1          2             100K
RP1          3          4                                   1K
CP1          4          0                                   0.05915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER      5          0          4          0             1
ROUT         5          6          10
.ENDS
*
* Analysis settings
* -----------------
.AC DEC 20 10HZ 1MEGHZ
*
* View Results
* ------------
.PLOT AC V(4)
.PROBE
.END
```

7.4 Frequency response of Closed-loop Output Impedance

```
EE898 G Cazzell
*
* Student:     Greg Cazzell
* Phone:       (937) 291-1252
* email:       cazzell.2@wright.edu
* Diss.:       Output Impedance in Buck Converter
*
** Filename:   Zocl bode V8.cir
*
* Aircraft Electric Power Regulator
* MIL-STD-704F
* Design Specifications
* ---------------------
* VImin = 24V;  VInom = 28V; VImax = 32V
* Dnom*VInom = 0.573*28 = 16.04V
* Vo = 14V; n = 90%; Vr < 0.2V
* Iomin = 0.5; Iomax = 0.9A
* fs = 100kHz; T = 0.01ms; DnomT = 0.00573ms;
* Dmin = 0.451; Dnom = 0.573; Dmax = 0.694
* RLmin = 14.4; RLmax = 30.0;
* Zocl: Bode plot
```

```
*
* Circuit
* -------
EVId        1       0       9       0       2.8
Ii          3       0                       AC  -1
r           1       2                       0.57
L           2       3                       364.56uH
C           3       4                       42.546uF
rc          4       0                       0.7
RL          3       0                       14.4
RA          3       5                       9180
RB          5       0                       5100
XOP1        5       6       6               OPAMP1
R1          6       7                       620.
C1          6       7                       1.0u
XOP2        0       7       9               OPAMP1
R2          7       8                       10k
C2          8       9                       3.9nF
C3          7       9                       12.nF
*
*OPMODEL1.CIR - OPAMP MODEL SINGLE-POLE
*
* OPAMP MACRO MODEL, SINGLE-POLE
* connections:              non-inverting input
*                           |   inverting input
*                           |   |   output
*                           |   |   |
.SUBCKT OPAMP1              1   2   6
* INPUT IMPEDANCE
RIN         1       2                       10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EGAIN       3       0       1       2       100K
RP1         3       4                       1K
CP1         4       0                       0.05915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER     5       0       4       0       1
ROUT        5       6       10
.ENDS
*
* Analysis settings
* -----------------
.AC DEC 20 10HZ 1MEGHZ
*
* View Results
* ------------
```

```
.PLOT AC V(3)
.PROBE
.END
```

7.5 Step response of closed-loop converter to a step change in load current

```
EE898 G Cazzell
*
* Student:      Greg Cazzell
* Phone:        (937) 291-1252
* email:        cazzell.2@wright.edu
* Diss.:        Output Impedance in Buck Converter
*
** Filename:   Zocl vo_io step V3.cir
*
* Aircraft Electric Power Regulator
* MIL-STD-704F
* Design Specifications
* ---------------------
* VImin = 24V;  VInom = 28V; VImax = 32V
* Dnom*VInom = 0.573*28 = 16.04V
* Vo = 14V; n = 90%; Vr < 0.2V
* Iomin = 0.5; Iomax = 0.9A
* fs = 100kHz; T = 0.01ms; DnomT = 0.00573ms;
* Dmin = 0.451; Dnom = 0.573; Dmax = 0.694
* RLmin = 14.4; RLmax = 30.0;
* Zocl step: Step in io from 0.14A to 1.4A
*
* Circuit
* -------
EVId        1       0       9       0       2.8
IO          3       0                       PWL(0 0.5A
5ms 0.5A 5.00000001ms 0.9A)
r           1       2                       0.57
L           2       3                       364.56uH
C           3       4                       42.546uF
rc          4       0                       0.7
RL          3       0                       14.4
RA          3       5                       9180
RB          5       0                       5100
XOP1        5       6       6               OPAMP1
R1          6       7                       620
C1          6       7                       1.u
XOP2        10      7       9               OPAMP1
VR          10      0                       DC 5V
```

```
R2          7          8                                    10k
C2          8          9                                    3.9nF
C3          7          9                                    12.nF
*
* OPAMP MACRO MODEL, SINGLE-POLE
* connections:              non-inverting input
*                           |  inverting input
*                           |  |  output
*                           |  |  |
.SUBCKT OPAMP1              1  2  6
* INPUT IMPEDANCE
RIN         1          2                                    10MEG
* DC GAIN=100K AND POLE1=100HZ
* UNITY GAIN = DCGAIN X POLE1 = 10MHZ
EGAIN       3          0          1          2              100K
RP1         3          4                                    1K
*CP1        4          0                                    1.5915UF
CP1         4          0                                    0.05915UF
* OUTPUT BUFFER AND RESISTANCE
EBUFFER     5          0          4          0              1
ROUT        5          6                                    10
.ENDS
*
*
* Analysis settings
* -----------------
.TRAN 0.01ms 6.5ms 0US 1US UIC
*
* View Results
* ------------
.PROBE
.END
```

8 Matlab Code

8.1 Intel VRM9.1 Design example using industry methods

```
close all; clear all; clc

% Greg Cazzell
% Date:  Apr 25, 2009
% File name:  diss_vrm91_code_desA_final_25Apr09.m
% Chapter 2
%
% Intel VRM9.1 Regulator

VInom = 12; VImin = 11.04; VImax = 12.6;
Vo = 1.476;
Vonom = 1.476;
Vr = Vo*(1/100);
Iomin = 0.5; Iomax = 10;
Dmax = 0.193; Dnom = 0.180; Dmin = 0.166;
fs = 200*10^3;
RLmin = 0.146; RLmax = 2.982;
nue = 0.70;
L = 13.0*10^-6; rl = 0.009;
C = 3290.0*10^-6; rc = 0.0014;
rds = 0.015;
Rf = 0.015; Vf = 0.39;
beta = 0.8/1.476;
Vtm = 5.;
Tm = 1./5.;

r = Dnom*rds + (1 - Dnom)*Rf + rl;

% Frequency spectrum used for bode plots

f2 = logspace (1,6,500);

% poles and zeros

wz = 1/(C*rc);
```

```
fz = wz/(2*pi);
w0 = ((RLmin + r)/(L*C*(RLmin + rc)))^0.5;
f0 = w0/(2*pi);
wzi = 1/(C*(RLmin + rc));
fzi = wzi/(2*pi);
wrl = r/L;
frl= wrl/(2*pi);
wcr = 1/(C*(RLmin + rc));
fcr= wcr/(2*pi);
zetanum = C*(RLmin*(rc + r) + rc*r) + L;
zetaden = 2*((L*C*(RLmin + rc)*(RLmin + r))^0.5);
zeta = zetanum / zetaden;
Q = 0.5/zeta;
fd = f0*((1-zeta^2)^0.5);

% Buck Converter in CCM Power stage equations

%>> Gpsf: Output filter of buck converter

Gpsfx = RLmin*rc/(L*(RLmin + rc));
Gpsf0 = RLmin/(RLmin + r);
numGpsf = Gpsfx*[1 wz];
denGpsf = [1 2*zeta*w0 w0*w0];
Gpsf = tf(numGpsf, denGpsf);
[MagGpsf, PhaseGpsf] = bode(numGpsf, denGpsf, 2*pi*f2);

figure (1)
semilogx(f2, 20*log10(MagGpsf));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it G_p_s_f}| (dB)');
ylim([-80 10])
saveas(gcf,'Gpsf mag','jpg')

figure (2)
semilogx(f2, PhaseGpsf);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _G_{_p_s_f}} ({\circ})');
saveas(gcf,'Gpsf phs','jpg')

%>> Tp (vo/d): Open-loop control-to-output transfer function

Tpx = VInom*Gpsfx;
Tp0 = VInom*Gpsf0;
Tp = VInom*Gpsf;
```

```
[numTp, denTp] = tfdata(Tp);
[MagTp, PhaseTp] = bode(numTp, denTp, 2*pi*f2);

figure (3)
semilogx(f2, 20*log10(MagTp));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_p}| (dBV)');
saveas(gcf,'Tp mag','jpg')

figure (4)
semilogx(f2, PhaseTp);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_p}} ({\circ})');
saveas(gcf,'Tp phs','jpg')

%>> Mv (vo/vi): Open-loop input-to-output transfer function

Mvx = Dnom*Gpsfx;
Mv0 = Dnom*Gpsf0;
Mv = Dnom*Gpsf;
[numMv, denMv] = tfdata(Mv);
[MagMv, PhaseMv] = bode(numMv, denMv, 2*pi*f2);

figure (5)
semilogx(f2, 20*log10(MagMv));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it M_v}| (dBV)');
saveas(gcf,'Mv mag','jpg')

figure (6)
semilogx(f2, PhaseMv);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _M_{_v}} ({\circ})');
saveas(gcf,'Mv phs','jpg')

%>> Zi (vi/ii): Open-loop input impedance transfer function

Zix = L/(Dnom*Dnom);
Zi0 = (RLmin + r)/(Dnom*Dnom);
numZi = Zix*[1 2*zeta*w0 w0*w0];
denZi = [1 wcr];
Zi = tf(numZi, denZi);
```

```
[MagZi, PhaseZi] = bode(numZi, denZi, 2*pi*f2);

figure (7)
semilogx(f2, MagZi);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_i}| (\Omega)');
ylim([0 100]);
saveas(gcf,'Zi mag ohms','jpg')

figure (8)
semilogx(f2, 20*log10(MagZi));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_i}| (dB\Omega)');
saveas(gcf,'Zi mag','jpg')

figure (9)
semilogx(f2, PhaseZi);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_i}} ({\circ})');
saveas(gcf,'Zi phs','jpg')

%>> Zo (vt/it): Open-loop output impedance transfer function

Zox = L*Gpsfx;
Z00 = L*Gpsf0;
numZo = Zox*[1 (wz+wrl) wz*wrl];
denZo = denGpsf;
Zo = tf(numZo, denZo);
[MagZo, PhaseZo] = bode(numZo, denZo, 2*pi*f2);

figure (10)
semilogx(f2, MagZo);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o}| (\Omega)');
ylim([0 0.09]);
saveas(gcf,'Zo mag ohms','jpg')

figure (11)
semilogx(f2, 20*log10(MagZo));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o}| (dB\Omega)');
```

```
saveas(gcf,'Zo mag','jpg')

figure (12)
semilogx(f2, PhaseZo);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o}} ({\circ})');
saveas(gcf,'Zo phs','jpg')

% Tp step:  Open-loop response of output voltage to step change in duty cycle.

vo_t0 = Vonom;
vi_step = 0.01; %d step from 0.18 to 0.19

sys = tf(numTp, denTp);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Tp_step = vi_step*step(sys,t) + vo_t0;

figure (13)
plot(tms, Tp_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Tp step','jpg')

% Mv step:  Open-loop response of output voltage to step change in input voltage.

vo_t0 = Vonom;
vi_step = 0.6; %vi step from 12 to 12.6 V

sys = tf(numMv, denMv);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Mv_step = vi_step*step(sys,t) + vo_t0;

figure (14)
plot(tms, Mv_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Mv step','jpg')
```

```
% Zo step:  Open-loop response of output voltage to step change in load current.

vo_t0 = Vonom;
i0_step = -9.5; %io step from 0.5 to 10 A

sys = tf(numZo, denZo);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Zo_step = i0_step*step(sys,t) + vo_t0;

figure (15)
plot(tms, Zo_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Zo step','jpg')

%>> Twoc : Open-loop transfer function without compensator

Twoc = beta*Tm*Tp;
[numTwoc, denTwoc] = tfdata(Twoc);
[MagTwoc, PhaseTwoc] = bode(numTwoc, denTwoc, 2*pi*f2);

figure (16)
semilogx(f2, 20*log10(MagTwoc));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_w_o_c}| (dBV)');
saveas(gcf,'Twoc mag','jpg')

figure (17)
semilogx(f2, PhaseTwoc);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_w_o_c}} ({\circ})');
saveas(gcf,'Twoc phs','jpg')

%>> Tci : Compensator used in Industry

fci = 60000;
wci = 2*pi*fci;
wzci = wci/15;
wpci = wci*15;
```

```
Ki = 3758374.043;
Ki = Ki*3535.9;

numTci = Ki*[1 wzci];
denTci = [1 wpci 0];
Tci = tf(numTci, denTci);
[MagTci, PhaseTci] = bode(numTci, denTci, 2*pi*f2);

figure (18)
semilogx(f2, 20*log10(MagTci));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_c}| (dBV)');
saveas(gcf,'Tci mag','jpg')

figure (19)
semilogx(f2, PhaseTci);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_c}} ({\circ})');
saveas(gcf,'Tci phs','jpg')

%>> T : Open-loop transfer function with compensator

Ti = Twoc*Tci;
[numTi, denTi] = tfdata(Ti);
[MagTi, PhaseTi] = bode(numTi, denTi, 2*pi*f2);

figure (20)
semilogx(f2, 20*log10(MagTi));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T}| (dBV)');
saveas(gcf,'Ti mag','jpg')

figure (21)
semilogx(f2, PhaseTi);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T} ({\circ})');
saveas(gcf,'Ti phs','jpg')

%>> Mvcl: Closed-loop input-to-output transfer function with compensator

Mvcli = Mv/(1 + Ti);
[numMvcli, denMvcli] = tfdata(Mvcli);
```

```
[MagMvcli, PhaseMvcli] = bode(numMvcli, denMvcli, 2*pi*f2);

figure (22)
semilogx(f2, 20*log10(MagMvcli));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it M_v_c_l}| (dBV)');
saveas(gcf,'Mvcli mag','jpg')

figure (23)
semilogx(f2, PhaseMvcli);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _M_{_v_c_l}} ({\circ})');
saveas(gcf,'Mvcli phs','jpg')

%>> Zocl: Closed-loop output impedance transfer function with compensator

Zocli = Zo/(1 + Ti);
[numZocli, denZocli] = tfdata(Zocli);
[MagZocli, PhaseZocli] = bode(numZocli, denZocli, 2*pi*f2);

figure (23)
semilogx(f2, 20*log10(MagZocli));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (dB\Omega)');
saveas(gcf,'Zocli mag','jpg')

figure (24)
semilogx(f2, MagZocli);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (\Omega)');
ylim([0 0.002]);
saveas(gcf,'Zocli mag ohms','jpg')

figure (25)
semilogx(f2, PhaseZocli);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o_c_l}} ({\circ})');
saveas(gcf,'Zocli phs','jpg')

% Mvcl step:  Closed-loop response of output voltage to step change in input voltage.
```

```
vo_t0 = 1.476;
vi_step = 0.6; %vi step from 12 to 12.6 V

sys = tf(numMvcli, denMvcli);
time_step = 1*10^-6;
Tfinal = 0.2*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Mvcli_step = vi_step*step(sys,t) + vo_t0;

figure (26)
plot(tms, Mvcli_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Mvcli step','jpg')

% Zocl step:  closed-loop response of output voltage to step change in load current.

vo_t0 = 1.476;
i0_step = -9.5; %io step from 1.4 to 1.5 A

sys = tf(numZocli, denZocli);
time_step = 1*10^-6;
Tfinal = 0.1*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Zocli_step = i0_step*step(sys,t) + vo_t0;

figure (27)
plot(tms, Zocli_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Zocli step','jpg')

% End of Code
```

8.2 Intel VRM9.1 Design example using alternative approach

```
close all
clear all
clc

% Greg Cazzell
% Date:  July 4, 2009
```

```
% File name:  diss_vrm91_code_desB_rev_04Jul09.m
% Chapter 4
%
% Intel VRM9.1 Regulator

VInom = 12; VImin = 11.04; VImax = 12.6;
Vo = 1.476;
Vonom = 1.476;
Vr = Vo*(1/100);
Iomin = 0.5; Iomax = 10;
Dmax = 0.1929; Dnom = 0.1802; Dmin = 0.1675;
fs = 200*10^3;
RLmin = 0.146; RLmax = 2.982;
nue = 0.70;
L = 13.0*10^-6; rl = 0.009;
C = 470.0*10^-6; rc = 0.0015;
rds = 0.015;
Rf = 0.015; Vf = 0.39;
beta = 0.8/1.476;
Vtm = 5.;
Tm = 1./5.;

r = Dnom*rds + (1 - Dnom)*Rf + rl;

% Frequency spectrum used for bode plots

f2 = logspace (1,6,500);

% poles and zeros

wz = 1/(C*rc);
fz = wz/(2*pi);
w0 = ((RLmin + r)/(L*C*(RLmin + rc)))^0.5;
f0 = w0/(2*pi);
wzi = 1/(C*(RLmin + rc));
fzi = wzi/(2*pi);
wrl = r/L;
frl= wrl/(2*pi);
wcr = 1/(C*(RLmin + rc));
fcr= wcr/(2*pi);
zetanum = C*(RLmin*(rc + r) + rc*r) + L;
zetaden = 2*((L*C*(RLmin + rc)*(RLmin + r))^0.5);
zeta = zetanum / zetaden;
Q = 0.5/zeta;
fd = f0*((1-zeta^2)^0.5);
```

```
% Buck Converter in CCM Power stage equations (from Chapter 11).

%>> Gpsf: Output filter of buck converter

Gpsfx = RLmin*rc/(L*(RLmin + rc));
Gpsf0 = RLmin/(RLmin + r);
numGpsf = Gpsfx*[1 wz];
denGpsf = [1 2*zeta*w0 w0*w0];
Gpsf = tf(numGpsf, denGpsf);
[MagGpsf, PhaseGpsf] = bode(numGpsf, denGpsf, 2*pi*f2);

figure (1)
semilogx(f2, 20*log10(MagGpsf));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it G_p_s_f}| (dB)');
ylim([-80 10])
saveas(gcf,'Gpsf mag','jpg')

figure (2)
semilogx(f2, PhaseGpsf);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _G_{_p_s_f}} ({\circ})');
saveas(gcf,'Gpsf phs','jpg')

%>> Tp (vo/d): Open-loop control-to-output transfer function

Tpx = VInom*Gpsfx;
Tp0 = VInom*Gpsf0;
Tp = VInom*Gpsf;
[numTp, denTp] = tfdata(Tp);
[MagTp, PhaseTp] = bode(numTp, denTp, 2*pi*f2);

figure (3)
semilogx(f2, 20*log10(MagTp));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_p}| (dBV)');
saveas(gcf,'Tp mag','jpg')

figure (4)
semilogx(f2, PhaseTp);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_p}} ({\circ})');
```

```
saveas(gcf,'Tp phs','jpg')

%>> Mv (vo/vi): Open-loop input-to-output transfer function

Mvx = Dnom*Gpsfx;
Mv0 = Dnom*Gpsf0;
Mv = Dnom*Gpsf;
[numMv, denMv] = tfdata(Mv);
[MagMv, PhaseMv] = bode(numMv, denMv, 2*pi*f2);

figure (5)
semilogx(f2, 20*log10(MagMv));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it M_v}| (dBV)');
saveas(gcf,'Mv mag','jpg')

figure (6)
semilogx(f2, PhaseMv);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _M_{_v}} ({\circ})');
saveas(gcf,'Mv phs','jpg')

%>> Zi (vi/ii): Open-loop input impedance transfer function

Zix = L/(Dnom*Dnom);
Zi0 = (RLmin + r)/(Dnom*Dnom);
numZi = Zix*[1 2*zeta*w0 w0*w0];
denZi = [1 wcr];
Zi = tf(numZi, denZi);
[MagZi, PhaseZi] = bode(numZi, denZi, 2*pi*f2);

figure (7)
semilogx(f2, MagZi);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_i}| (\Omega)');
ylim([0 100]);
saveas(gcf,'Zi mag ohms','jpg')

figure (8)
semilogx(f2, 20*log10(MagZi));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_i}| (dB\Omega)');
```

```
saveas(gcf,'Zi mag','jpg')

figure (9)
semilogx(f2, PhaseZi);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_i}} ({\circ})');
saveas(gcf,'Zi phs','jpg')

%>> Zo (vt/it): Open-loop output impedance transfer function

Zox = L*Gpsfx;
Z00 = L*Gpsf0;
numZo = Zox*[1 (wz+wrl) wz*wrl];
denZo = denGpsf;
Zo = tf(numZo, denZo);
[MagZo, PhaseZo] = bode(numZo, denZo, 2*pi*f2);

figure (10)
semilogx(f2, MagZo);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o}| (\Omega)');
saveas(gcf,'Zo mag ohms','jpg')

figure (11)
semilogx(f2, 20*log10(MagZo));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o}| (dB\Omega)');
saveas(gcf,'Zo mag','jpg')

figure (12)
semilogx(f2, PhaseZo);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o}} ({\circ})');
saveas(gcf,'Zo phs','jpg')

% Tp step:  Open-loop response of output voltage to step change in duty cycle.

vo_t0 = Vonom;
vi_step = 0.01; %d step from 0.18 to 0.19

sys = tf(numTp, denTp);
time_step = 1*10^-6;
```

```
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Tp_step = vi_step*step(sys,t) + vo_t0;

figure (13)
plot(tms, Tp_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Tp step','jpg')

% Mv step:  Open-loop response of output voltage to step change in input voltage.

vo_t0 = Vonom;
vi_step = 0.6; %vi step from 12 to 12.6 V

sys = tf(numMv, denMv);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Mv_step = vi_step*step(sys,t) + vo_t0;

figure (14)
plot(tms, Mv_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Mv step','jpg')

% Zo step:  Open-loop response of output voltage to step change in load current.

vo_t0 = Vonom;
i0_step = -9.5; %io step from 0.5 to 10 A

sys = tf(numZo, denZo);
time_step = 1*10^-6;
Tfinal = 0.5*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Zo_step = i0_step*step(sys,t) + vo_t0;

figure (15)
plot(tms, Zo_step)
grid on
```

```
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Zo step','jpg')

%>> Twoc : Open-loop transfer function without compensator

Twoc = beta*Tm*Tp;
[numTwoc, denTwoc] = tfdata(Twoc);
[MagTwoc, PhaseTwoc] = bode(numTwoc, denTwoc, 2*pi*f2);

figure (16)
semilogx(f2, 20*log10(MagTwoc));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_w_o_c}| (dBV)');
saveas(gcf,'Twoc mag','jpg')

figure (17)
semilogx(f2, PhaseTwoc);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_w_o_c}} ({\circ})');
saveas(gcf,'Twoc phs','jpg')

% Zocld is the transfer function of the desired closed-loop output impedance

fzocld = 60000;
wzocld = 2*pi*fzocld;
%Kzocld = 0.15*rc;
Kzocld = RLmin*rc/(RLmin + rc);
numZocld = Kzocld*[1 0];
denZocld = [1 2*pi*fzocld];
Zocld = tf(numZocld, denZocld);
[MagZocld, PhaseZocld] = bode(numZocld, denZocld, 2*pi*f2);

figure (18)
semilogx(f2, 20*log10(MagZocld));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (dB\Omega)');
saveas(gcf,'Zocld mag','jpg')

figure (19)
semilogx(f2, MagZocld);
grid on
xlabel('{\it f} (Hz)');
```

```
ylabel('|{\it Z_o_c_l}| (\Omega)');
saveas(gcf,'Zocld mag ohms','jpg')

figure (20)
semilogx(f2, PhaseZocld);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o_c_l}} ({\circ})');
%saveas(gcf,'Zocld phs','jpg')

% Calculate the transfer function of the output impedance compensator, Tcd

wzocld_test = (w0*(wz+wrl)-2*zeta*wz*wrl)/(2*zeta*(wz+wrl)-w0);
R = RLmin*rc/(RLmin + rc);
Kz_test = R*(wz+wrl+wzocld_test)/(2*rc*zeta*w0);
Kz = R/rc;
c3 = (1 - Kz*rc/R)/(wz*wrl*wzocld);
c2 = (wz + wrl + wzocld - 2*Kz*rc*zeta*w0/R)/(wz*wrl*wzocld);
c1 = (wz*wrl + wzocld*wz + wzocld*wrl - Kz*rc*w0*w0/R)/(wz*wrl*wzocld);
c0 = 1;
d2 = 1/wz;
d1 = 1;
Tcx = (Vtm*L*wrl*wzocld)/(beta*VInom*Kz*rc);

numTcd = Tcx*[c3 c2 c1 c0];
denTcd = [d2 d1 0];
Tcd = tf(numTcd, denTcd);
[MagTcd, PhaseTcd] = bode(numTcd, denTcd, 2*pi*f2);

figure (21)
semilogx(f2,20*log10(MagTcd));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_c}| (dB)');
saveas(gcf,'Tcd mag','jpg')

figure (22)
semilogx(f2,PhaseTcd);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_c}} ({\circ})');
saveas(gcf,'Tcd phase','jpg')

% Loop Gain with reduced order compensator

Td = Twoc*Tcd;
```

```
[numTd, denTd] = tfdata(Td);
[MagTd, PhaseTd] = bode(numTd, denTd, 2*pi*f2);

figure (23)
semilogx(f2,20*log10(MagTd));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T}| (dB)');
saveas(gcf,'Td loop gain','jpg')

figure (24)
semilogx(f2,PhaseTd);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T} ({\circ})');
saveas(gcf,'Td loop phase','jpg')

% closed loop output impedance with reduced compensator

Zocld1 = Zo/(1 + Td);
[numZocld1, denZocld1] = tfdata(Zocld1);
[MagZocld1, PhaseZocld1] = bode(numZocld1, denZocld1, 2*pi*f2);

figure (25)
semilogx(f2, 20*log10(MagZocld1),f2, 20*log10(MagZocld), '-.k');
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (dB\Omega)');
legend('Designed', 'Desired',4);
saveas(gcf,'Zocld1 vs Zocld mag','jpg')

figure (26)
semilogx(f2, MagZocld1);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (\Omega)');
ylim([0 0.002]);
legend('Designed', 'Desired',3);
saveas(gcf,'Zocld1 vs Zocld mag ohms','jpg')

figure (27)
semilogx(f2, PhaseZocld1, f2, PhaseZocld, '-.k');
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o_c_l}} ({\circ})');
legend('Designed', 'Desired',3);
```

```
saveas(gcf,'Zocld1 vs Zocld phase','jpg')

% Mv step:  Open-loop response of output voltage to step change in input voltage.

Mvcld1 = Mv/(1 + Td);
[numMvcld1, denMvcld1] = tfdata(Mvcld1);
[MagMvcld1, PhaseMvcld1] = bode(numMvcld1, denMvcld1, 2*pi*f2);

vo_t0 = Vonom;
vi_step = 0.6; %vi step from 12 to 12.6 V

sys = tf(numMvcld1, denMvcld1);
time_step = 1*10^-6;
Tfinal = 1.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Mvcld1_step = vi_step*step(sys,t) + vo_t0;

figure (28)
plot(tms, Mvcld1_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
ylim([1.4760 1.4761]);
saveas(gcf,'Mvcld1 step','jpg')

% Zo step:  Open-loop response of output voltage to step change in load current.

vo_t0 = Vonom;
i0_step = -9.5; %io step from 0.5 to 10 A

sys = tf(numZocld1, denZocld1);
time_step = 1*10^-6;
Tfinal = 0.05*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Zocld1_step = i0_step*step(sys,t) + vo_t0;

figure (29)
plot(tms, Zocld1_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
ylim([1.46 1.48]);
saveas(gcf,'Zocld1 step','jpg')
```

```
figure (30)
semilogx(f2, MagZocld1,f2, MagZo, '-.k');
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (\Omega)');
legend('Closed-loop', 'Open-loop',1);
saveas(gcf,'Zocld1 vs Zocld mag ohms','jpg')

% End of Code
```

8.3 Aircraft Electric Power Regulator Design example with PSPICE data

```
close all
clear all
clc

% Greg Cazzell
% Date:  May 01, 2009
% File name:  diss_aircraft_codes_pspice_03May09b.m
% Chapter 5
%
% Aircraft HW application

VInom = 28.; VImin = 24.; VImax = 32.;
Vonom = 14.; Vomin = 13.; Vomax = 15.;
Vo = Vonom;
Vr = 0.2;
RLmin = 14.4; RLmax = 30.0;
Iomin = 0.5; Iomax = 0.9;
Dmax = 0.694; Dnom = 0.573; Dmin = 0.451;
fs = 100*10^3;
nue = 0.90;
beta = 5/14;
Vtm = 10.;
Tm = 1./Vtm;
fs = 100*10^3;
nue = 0.95;
% Output Filter
L = 344.56*10^-6; rl = 0.3;
C = 42.546*10^-6; rc = 0.7;
% IRF530 Power MOSFET
rds = 0.4;
% MUR820 Power Diode
Rf = 0.1;
```

```
r = Dnom*rds + (1 - Dnom)*Rf + rl;

% Frequency spectrum used for bode plots

f2 = logspace (1,6,500);

% poles and zeros

wz = 1/(C*rc);
fz = wz/(2*pi);
w0 = ((RLmin + r)/(L*C*(RLmin + rc)))^0.5;
f0 = w0/(2*pi);
wzi = 1/(C*(RLmin + rc));
fzi = wzi/(2*pi);
wrl = r/L;
frl= wrl/(2*pi);
wcr = 1/(C*(RLmin + rc));
fcr= wcr/(2*pi);
zetanum = C*(RLmin*(rc + r) + rc*r) + L;
zetaden = 2*((L*C*(RLmin + rc)*(RLmin + r))^0.5);
zeta = zetanum / zetaden;
Q = 0.5/zeta;
fd = f0*((1-zeta^2)^0.5);

% Buck Converter in CCM Power stage equations (from Chapter 11).

%>> Gpsf: Output filter of buck converter

Gpsfx = RLmin*rc/(L*(RLmin + rc));
Gpsf0 = RLmin/(RLmin + r);
numGpsf = Gpsfx*[1 wz];
denGpsf = [1 2*zeta*w0 w0*w0];
Gpsf = tf(numGpsf, denGpsf);
[MagGpsf, PhaseGpsf] = bode(numGpsf, denGpsf, 2*pi*f2);

figure (1)
semilogx(f2, 20*log10(MagGpsf));
grid on
hold on
% PSPICE Data
plot(10,-0.337,'o',100,-
0.293,'o',298.75,0.068,'o',1000,3.9733,'o',1105,4.3675,'o',1203,4.2519,'o',1310,3.65,'o');
plot(1407,2.782,'o',1510,1.4253,'o',2007, -4.7765,'o',3030,-12.9,'o',10000,-
29.505,'o',100000,-50.7,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it G_p_s_f}| (dB)');
```

```
ylim([-80 10])
legend({'{\it Matlab}','{\it PSPICE Data}'},3);
saveas(gcf,'Gpsf mag','jpg')

figure (2)
semilogx(f2, PhaseGpsf);
grid on
hold on
% PSPICE Data
plot(10,-.171,'o',100,-1.7346,'o',298.75,-5.57,'o',1000,-40.667,'o',1105,-54,'o',1203,-
67.3,'o',1304,-80.67,'o');
plot(1402,-92.67,'o',1503,-102.,'o',2007, -126.043,'o',3030,-132.81,'o',10000,-
113.53,'o',100000,-92.6,'o');
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _G_{_p_s_f}} ({\circ})');
legend({'{\it Matlab}','{\it PSPICE}'},3);
saveas(gcf,'Gpsf phs','jpg')

%>> Tp (vo/d): Open-loop control-to-output transfer function

Tpx = VInom*Gpsfx;
Tp0 = VInom*Gpsf0;
Tp = VInom*Gpsf;
[numTp, denTp] = tfdata(Tp);
[MagTp, PhaseTp] = bode(numTp, denTp, 2*pi*f2);

figure (3)
semilogx(f2, 20*log10(MagTp));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_p}| (dBV)');
saveas(gcf,'Tp mag','jpg')

figure (4)
semilogx(f2, PhaseTp);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_p}} ({\circ})');
saveas(gcf,'Tp phs','jpg')

%>> Mv (vo/vi): Open-loop input-to-output transfer function

Mvx = Dnom*Gpsfx;
Mv0 = Dnom*Gpsf0;
Mv = Dnom*Gpsf;
[numMv, denMv] = tfdata(Mv);
```

```
[MagMv, PhaseMv] = bode(numMv, denMv, 2*pi*f2);

figure (5)
semilogx(f2, 20*log10(MagMv));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it M_v}| (dBV)');
saveas(gcf,'Mv mag','jpg')

figure (6)
semilogx(f2, PhaseMv);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _M_{_v}} ({\circ})');
saveas(gcf,'Mv phs','jpg')

%>> Zi (vi/ii): Open-loop input impedance transfer function

Zix = L/(Dnom*Dnom);
Zi0 = (RLmin + r)/(Dnom*Dnom);
numZi = Zix*[1 2*zeta*w0 w0*w0];
denZi = [1 wcr];
Zi = tf(numZi, denZi);
[MagZi, PhaseZi] = bode(numZi, denZi, 2*pi*f2);

figure (7)
semilogx(f2, MagZi);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_i}| (\Omega)');
ylim([0 100]);
saveas(gcf,'Zi mag ohms','jpg')

figure (8)
semilogx(f2, 20*log10(MagZi));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_i}| (dB\Omega)');
saveas(gcf,'Zi mag','jpg')

figure (9)
semilogx(f2, PhaseZi);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_i}} ({\circ})');
saveas(gcf,'Zi phs','jpg')
```

```
%>> Zo (vt/it): Open-loop output impedance transfer function

Zox = L*Gpsfx;
Z00 = L*Gpsf0;
numZo = Zox*[1 (wz+wrl) wz*wrl];
denZo = denGpsf;
Zo = tf(numZo, denZo);
[MagZo, PhaseZo] = bode(numZo, denZo, 2*pi*f2);

figure (10)
semilogx(f2, MagZo);
grid on
hold on
% PSPICE Data
plot(10, 0.55,'o',100,0.595,'o',303,0.909,'o',1000,3.75,'o');
plot(1292, 4.674,'o',2000, 2.679,'o',3030,1.5737,'o',10000,0.766,'o',100000,0.668,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o}| (\Omega)');
legend({'{\it Matlab}','{\it PSPICE}'},1);
saveas(gcf,'Zo mag ohms','jpg')

figure (11)
semilogx(f2, 20*log10(MagZo));
grid on
hold on
% PSPICE Data
plot(10, -5.19,'o',100,-4.51,'o',303,-0.83,'o',1000,11.48,'o');
plot(1292, 13.39,'o',2000, 8.56,'o',3030,3.94,'o',10000,-2.32,'o',100000,-3.50,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o}| (dB\Omega)');
legend({'{\it Matlab}','{\it PSPICE}'},1);
saveas(gcf,'Zo mag','jpg')

figure (12)
semilogx(f2, PhaseZo);
grid on
hold on
% PSPICE Data
plot(10, 2.12,'o',100,20.09,'o',303,44.83,'o',1000,34.581,'o');
plot(1290, 0,'o',2007, -43.152,'o',3030,-47.494,'o',10000,-24.911,'o',100000,-2.74,'o');
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o}} ({\circ})');
legend({'{\it Matlab}','{\it PSPICE}'},1);
saveas(gcf,'Zo phs','jpg')
```

```
% Tp step:  Open-loop response of output voltage to step change in duty cycle.

vo_t0 = Vonom;
vi_step = 0.1; %d step from 0.5 to 0.6

sys = tf(numTp, denTp);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Tp_step = vi_step*step(sys,t) + vo_t0;

figure (13)
plot(tms, Tp_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Tp step','jpg')

% Mv step:  Open-loop response of output voltage to step change in input voltage.

vo_t0 = Vonom;
vi_step = 1.0; %vi step from 28 to 29 V

sys = tf(numMv, denMv);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Mv_step = vi_step*step(sys,t) + vo_t0;

figure (14)
plot(tms, Mv_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Mv step','jpg')

% Zo step:  Open-loop response of output voltage to step change in load current.

vo_t0 = Vonom;
i0_step = -0.40; %io step from 0.9 to 0.5 A

sys = tf(numZo, denZo);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
```

```
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Zo_step = i0_step*step(sys,t) + vo_t0;

figure (15)
plot(tms, Zo_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
legend({'{\it Matlab}','{\it HW Data}'},4);
saveas(gcf,'Zo step','jpg')

%>> Twoc : Open-loop transfer function without compensator

Twoc = beta*Tm*Tp;
[numTwoc, denTwoc] = tfdata(Twoc);
[MagTwoc, PhaseTwoc] = bode(numTwoc, denTwoc, 2*pi*f2);

figure (16)
semilogx(f2, 20*log10(MagTwoc));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_w_o_c}| (dBV)');
saveas(gcf,'Twoc mag','jpg')

figure (17)
semilogx(f2, PhaseTwoc);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_w_o_c}} ({\circ})');
saveas(gcf,'Twoc phs','jpg')

% Zocld is the transfer function of the desired closed-loop output impedance

fzocld = 20000;
wzocld = 2*pi*fzocld;
Kzocld = 1.*rc;
numZocld = Kzocld*[1 0];
denZocld = [1 2*pi*fzocld];
Zocld = tf(numZocld, denZocld);
[MagZocld, PhaseZocld] = bode(numZocld, denZocld, 2*pi*f2);

figure (18)
semilogx(f2, 20*log10(MagZocld));
grid on
xlabel('{\it f} (Hz)');
```

```
ylabel('|{\it Z_o_c_l}| (dB\Omega)');
saveas(gcf,'Zocld mag','jpg')

figure (19)
semilogx(f2, MagZocld);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (\Omega)');
saveas(gcf,'Zocld mag ohms','jpg')

figure (20)
semilogx(f2, PhaseZocld);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o_c_l}} ({\circ})');
saveas(gcf,'Zocld phs','jpg')

% Calculate the transfer function of the output impedance compensator, Tcd

% First Test to Reduce Order of Tcd

R = RLmin*rc/(RLmin + rc);
Kz_test1 = R/rc;
wzocld_c2_test1 = 2*zeta*w0-wz-wrl;
wzocld_c1_test1 = (w0*w0 - wz*wrl)/(wz + wrl);

% Second Test to Reduce Order of Tcd

wzocld_c2_c3_test2 = (w0*(wz+wrl)-2*zeta*wz*wrl)/(2*zeta*(wz+wrl)-w0);
Kz_c2_c3_test2 = R*(wz+wrl+wzocld_c2_c3_test2)/(2*rc*zeta*w0);

% Tcd - set coefficients

Kz = R/rc;
wzocld = 2*pi*20000;
c3 = (1 - Kz*rc/R)/(wz*wrl*wzocld);
c2 = (wz + wrl + wzocld - 2*Kz*rc*zeta*w0/R)/(wz*wrl*wzocld);
c1 = (wz*wrl + wzocld*wz + wzocld*wrl - Kz*rc*w0*w0/R)/(wz*wrl*wzocld);
c0 = 1;
d2 = 1/wz;
d1 = 1;
Tcx = (Vtm*L*wrl*wzocld)/(beta*VInom*Kz*rc);

numTcd = Tcx*[c3 c2 c1 c0];
denTcd = [d2 d1 0];
Tcd = tf(numTcd, denTcd);
```

```
[MagTcd, PhaseTcd] = bode(numTcd, denTcd, 2*pi*f2);

figure (21)
semilogx(f2,20*log10(MagTcd));
grid on
hold on
% PSPICE Data
plot(10,64.16,'o',30.243,54.6,'o',100,44.769,'o',302.4,38.339,'o',1000,36.35,'o');
plot(3024.3,
36.72,'o',10000,37.97,'o',29708,38.353,'o',100e3,38.423,'o',297076,38.556,'o',1e6,40.07,'o
');
xlabel('{\it f} (Hz)');
ylabel('|{\it T_c}| (dB)');
ylim([35 65]);
legend({'{\it Matlab}','{\it PSPICE}'},1);
saveas(gcf,'Tcd mag','jpg')

figure (22)
semilogx(f2,PhaseTcd);
grid on
hold on
% PSPICE Data
plot(10,-86.811,'o',30.243,-82.861,'o',100,-68.281,'o',302.4,-39.267,'o',1000, -11.113,'o');
plot(3024.3, 2.4096,'o',10000,4.5563,'o',29708,1.4683,'o',100e3,-1.1907,'o',297076,-
5.2435,'o',1e6,-22.210,'o');
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_c}} ({\circ})');
legend({'{\it Matlab}','{\it PSPICE}'},4);
saveas(gcf,'Tcd phase','jpg')

% Loop gain with compensator

Td = Twoc*Tcd;
[numTd, denTd] = tfdata(Td);
[MagTd, PhaseTd] = bode(numTd, denTd, 2*pi*f2);

figure (23)
semilogx(f2,20*log10(MagTd));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T}| (dB)');
saveas(gcf,'Td loop gain','jpg')

figure (24)
semilogx(f2,PhaseTd);
grid on
```

```
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T} ({\circ})');
saveas(gcf,'Td loop phase','jpg')

% closed loop output impedance with compensator

Zocld1 = Zo/(1 + Td);
[numZocld1, denZocld1] = tfdata(Zocld1);
[MagZocld1, PhaseZocld1] = bode(numZocld1, denZocld1, 2*pi*f2);

figure (25)
semilogx(f2, 20*log10(MagZocld1));
grid on
hold on
% PSPICE Data
plot(10,-69.036,'o',30.263,-59.417,'o',100,-49.019,'o',302.633,-39.344,'o',1e3,-28.942,'o');
plot(3026,-19.511,'o',10e3,-10.295,'o',30800,-4.9565,'o',100e3,-3.6127,'o',302633,-
3.4584,'o',1e6,-3.3382,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (dB\Omega)');
legend({'{\it Matlab}','{\it PSPICE}'},0);
saveas(gcf,'Zocld1 vs Zocld mag','jpg')

figure (26)
semilogx(f2, MagZocld1);
grid on
hold on
% PSPICE Data
plot(10,353.36e-6,'o',30.263,1.0711e-3,'o',100,3.5403e-3,'o',302.633,10.802e-
3,'o',1e3,35.721e-3,'o');
plot(3026,105.938e-3,'o',10e3,305.654e-3,'o',30263,562.219e-3,'o',100e3,659.729e-
3,'o',302633,671.55e-3,'o',1e6,680.907e-3,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (\Omega)');
legend({'{\it Matlab}','{\it PSPICE}'},0);
saveas(gcf,'Zocld1 vs Zocld mag ohms','jpg')

figure (27)
semilogx(f2, PhaseZocld1);
grid on
hold on
% PSPICE Data
plot(10,89.075,'o',30.2,89.69,'o',100,89.853,'o',302.633,89.329,'o',1e3,86.705,'o');
plot(3026,79.929,'o',10e3,61.886,'o',30263,32.817,'o',100e3,11.149,'o',302633,3.8789,'o',
1e6,1.6956,'o');
xlabel('{\it f} (Hz)');
```

```
ylabel('{\it \phi _Z_{_o_c_l}} ({\circ})');
legend({'{\it Matlab}','{\it PSPICE}'},1);
saveas(gcf,'Zocld1 vs Zocld phase','jpg')

% Zo step:  Open-loop response of output voltage to step change in load current.

vo_t0 = Vonom;
i0_step = -0.4; %io step from 0.9 to 0.5 A

sys = tf(numZocld1, denZocld1);
time_step = 1*10^-6;
Tfinal = 0.1*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Zocld1_step = i0_step*step(sys,t) + vo_t0;

figure (28)
plot(tms, Zocld1_step)
grid on
hold on
% PSPICE Data
plot(0.0005,13.749,'o',0.005,13.854,'o',0.01,13.921,'o',0.015,13.957,'o',0.02,13.976,'o');
plot(0.025,13.986,'o',0.0301,13.992,'o',0.035,13.995,'o',0.04,13.997,'o',0.06,13.999,'o',0.0
8,14.000,'o');
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
ylim([13.7 14.1])
legend({'{\it Matlab}','{\it PSPICE}'},4);
saveas(gcf,'Zocld1 step','jpg')

% Mv step:  Open-loop response of output voltage to step change in input voltage.

Mvcld1 = Mv/(1 + Td);
[numMvcld1, denMvcld1] = tfdata(Mvcld1);
[MagMvcld1, PhaseMvcld1] = bode(numMvcld1, denMvcld1, 2*pi*f2);

vo_t0 = Vonom;
vi_step = 4.0; %vi step from 28 to 32 V

sys = tf(numMvcld1, denMvcld1);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Mvcld1_step = vi_step*step(sys,t) + vo_t0;
```

```
figure (29)
plot(tms, Mvcld1_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Mvcld1 step','jpg')

% End of Code
```

8.4 Aircraft Electric Power Regulator Design example with HW data

```
close all
clear all
clc

% Greg Cazzell
% Date:  May 08, 2009
% File name:  diss_aircraft_codes_hwdata_08May09.m
% Chapter 5
%
% Aircraft HW application

VInom = 28.; VImin = 24.; VImax = 32.;
Vonom = 14.; Vomin = 13.; Vomax = 15.;
Vo = Vonom;
Vr = 0.2;
Iomin = 0.5; Iomax = 0.9;
fs = 100*10^3;
nue = 0.90;
beta = 5/14;
Vtm = 10.;
Tm = 1./Vtm;
%
% HW Measured Values
%
Dmax = 0.654; Dnom = 0.525; Dmin = 0.434;
fs = 100*10^3;
nue = 0.95;
RLmin = 16.4; RLmax = 24.8;
L = 344.56*10^-6; rl = 0.3;
C = 42.546*10^-6; rc = 0.7;
% IRF530 Power MOSFET
rds = 0.4;
% MUR820 Power Diode
Rf = 0.1;
```

```
% Frequency spectrum used for bode plots

f2 = logspace (1,6,500);

%>> Gof: Output filter of buck converter at Max Load Condition

r = rl;

% poles and zeros

wz = 1/(C*rc);
fz = wz/(2*pi);
w0 = ((RLmin + r)/(L*C*(RLmin + rc)))^0.5;
f0 = w0/(2*pi);
wzi = 1/(C*(RLmin + rc));
fzi = wzi/(2*pi);
wrl = r/L;
frl= wrl/(2*pi);
wcr = 1/(C*(RLmin + rc));
fcr= wcr/(2*pi);
zetanum = C*(RLmin*(rc + r) + rc*r) + L;
zetaden = 2*((L*C*(RLmin + rc)*(RLmin + r))^0.5);
zeta = zetanum / zetaden;
Q = 0.5/zeta;
fd = f0*((1-zeta^2)^0.5);

Gofx = RLmin*rc/(L*(RLmin + rc));
Gof0 = RLmin/(RLmin + r);
numGof = Gofx*[1 wz];
denGof = [1 2*zeta*w0 w0*w0];
Gof = tf(numGof, denGof);
[MagGof, PhaseGof] = bode(numGof, denGof, 2*pi*f2);

figure (1)
semilogx(f2, 20*log10(MagGof));
grid on
hold on
% HW Measured Data
plot(10, -0.15,'o',100,-
0.28,'o',300.,0.599,'o',1000,4.868,'o',1100,5.54,'o',1200,6.4,'o',1300,4.31,'o');
plot(1400,3.21,'o',1500,1.7,'o',2000, -4.15,'o',3000,-11.7,'o',10000,-27.6,'o',100000,-
50.7,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it G_o_f}| (dB)');
ylim([-80 10])
legend({'{\it Theoretical}','{\it Measured}'},3);
```

```
saveas(gcf,'Gof mag','jpg')

figure (2)
semilogx(f2, PhaseGof);
grid on
hold on
% HW Measured Data
plot(10, 0.,'o',100,0.,'o',300.,-4,'o',1000,-38,'o',1100,-20,'o',1200,-53,'o',1300,-90,'o');
plot(1400,-63,'o',1500,-76,'o',2000, -136,'o',3000,-138,'o',10000,-107,'o',100000,-90,'o');
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _G_{_o_f}} ({\circ})');
legend({'{\it Theoretical}','{\it Measured}'},3);
saveas(gcf,'Gof phs','jpg')

%>> Gpsf: Output filter of buck converter

r = Dnom*rds + (1 - Dnom)*Rf + rl;

% poles and zeros

wz = 1/(C*rc);
fz = wz/(2*pi);
w0 = ((RLmin + r)/(L*C*(RLmin + rc)))^0.5;
f0 = w0/(2*pi);
wzi = 1/(C*(RLmin + rc));
fzi = wzi/(2*pi);
wrl = r/L;
frl= wrl/(2*pi);
wcr = 1/(C*(RLmin + rc));
fcr= wcr/(2*pi);
zetanum = C*(RLmin*(rc + r) + rc*r) + L;
zetaden = 2*((L*C*(RLmin + rc)*(RLmin + r))^0.5);
zeta = zetanum / zetaden;
Q = 0.5/zeta;
fd = f0*((1-zeta^2)^0.5);

% Buck Converter in CCM Power stage equations (from Chapter 11).

%>> Gpsf: Output filter of buck converter

Gpsfx = RLmin*rc/(L*(RLmin + rc));
Gpsf0 = RLmin/(RLmin + r);
numGpsf = Gpsfx*[1 wz];
denGpsf = [1 2*zeta*w0 w0*w0];
Gpsf = tf(numGpsf, denGpsf);
[MagGpsf, PhaseGpsf] = bode(numGpsf, denGpsf, 2*pi*f2);
```

```
figure (3)
semilogx(f2, 20*log10(MagGpsf));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it G_p_s_f}| (dB)');
ylim([-80 10])
saveas(gcf,'Gpsf mag','jpg')

figure (4)
semilogx(f2, PhaseGpsf);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _G_{_p_s_f}} ({\circ})');
saveas(gcf,'Gpsf phs','jpg')

%>> Tp (vo/d): Open-loop control-to-output transfer function

Tpx = VInom*Gpsfx;
Tp0 = VInom*Gpsf0;
Tp = VInom*Gpsf;
[numTp, denTp] = tfdata(Tp);
[MagTp, PhaseTp] = bode(numTp, denTp, 2*pi*f2);

figure (5)
semilogx(f2, 20*log10(MagTp));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_p}| (dBV)');
saveas(gcf,'Tp mag','jpg')

figure (6)
semilogx(f2, PhaseTp);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_p}} ({\circ})');
saveas(gcf,'Tp phs','jpg')

%>> Mv (vo/vi): Open-loop input-to-output transfer function

Mvx = Dnom*Gpsfx;
Mv0 = Dnom*Gpsf0;
Mv = Dnom*Gpsf;
[numMv, denMv] = tfdata(Mv);
[MagMv, PhaseMv] = bode(numMv, denMv, 2*pi*f2);
```

```
figure (7)
semilogx(f2, 20*log10(MagMv));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it M_v}| (dBV)');
saveas(gcf,'Mv mag','jpg')

figure (8)
semilogx(f2, PhaseMv);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _M_{_v}} ({\circ})');
saveas(gcf,'Mv phs','jpg')

%>> Zi (vi/ii): Open-loop input impedance transfer function

Zix = L/(Dnom*Dnom);
Zi0 = (RLmin + r)/(Dnom*Dnom);
numZi = Zix*[1 2*zeta*w0 w0*w0];
denZi = [1 wcr];
Zi = tf(numZi, denZi);
[MagZi, PhaseZi] = bode(numZi, denZi, 2*pi*f2);

figure (9)
semilogx(f2, MagZi);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_i}| (\Omega)');
ylim([0 100]);
saveas(gcf,'Zi mag ohms','jpg')

figure (10)
semilogx(f2, 20*log10(MagZi));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_i}| (dB\Omega)');
saveas(gcf,'Zi mag','jpg')

figure (11)
semilogx(f2, PhaseZi);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_i}} ({\circ})');
saveas(gcf,'Zi phs','jpg')

%>> Zo (vt/it): Open-loop output impedance transfer function
```

```
Zox = L*Gpsfx;
Z00 = L*Gpsf0;
numZo = Zox*[1 (wz+wrl) wz*wrl];
denZo = denGpsf;
Zo = tf(numZo, denZo);
[MagZo, PhaseZo] = bode(numZo, denZo, 2*pi*f2);

figure (12)
semilogx(f2, MagZo);
grid on
hold on
% HW Measured Data
plot(10,
0.55,'o',30,0.549,'o',100,0.558,'o',300,0.761,'o',1000,3.021,'o',1100,3.646,'o',1200,4.207,'o
',1300,4.586,'o');
plot(1400,4.690,'o',1500,4.552,'o',2000,2.986,'o',3000,1.621,'o',10000,0.721,'o',30000,0.7
10,'o',100000,0.653,'o',1e6,0.704,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o}| (\Omega)');
legend({'{\it Theoretical}','{\it Measured}'},1);
saveas(gcf,'Zo mag ohms','jpg')

figure (13)
semilogx(f2, 20*log10(MagZo));
grid on
hold on
% HW Measured Data
plot(10, -5.19,'o',30,-5.204,'o',100,-5.067,'o',300,-
2.374,'o',1000,9.603,'o',1100,11.236,'o',1200,12.479,'o',1300,13.229,'o');
plot(1400,13.423,'o',1500,13.164,'o',2000,9.502,'o',3000,4.194,'o',10000,-
2.836,'o',30000,-2.974,'o',100000,-3.705,'o',1e6,-3.0485,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o}| (dB\Omega)');
legend({'{\it Theoretical}','{\it Measured}'},1);
saveas(gcf,'Zo mag','jpg')

figure (14)
semilogx(f2, PhaseZo);
grid on
hold on
% HW Measured Data
plot(10, 4.2,'o',30,7.5,'o',100,19,'o',300,43.2,'o',1000,40.6,'o',1200,27.8,'o',1300,8.6,'o');
plot(1400,-3.4,'o',1500,-8.6,'o',2000,-42.2,'o',3000,-49,'o',10000,-26.6,'o',30000,-
9.4,'o',100000,-2.6,'o',1e6,-1,'o');
xlabel('{\it f} (Hz)');
```

```
ylabel('{\it \phi _Z_{_o}} ({\circ})');
legend({'{\it Theoretical}','{\it Measured}'},1);
saveas(gcf,'Zo phs','jpg')

% Tp step:  Open-loop response of output voltage to step change in duty cycle.

vo_t0 = Vonom;
vi_step = 0.1; %d step from 0.5 to 0.6

sys = tf(numTp, denTp);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Tp_step = vi_step*step(sys,t) + vo_t0;

figure (15)
plot(tms, Tp_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Tp step','jpg')

% Mv step:  Open-loop response of output voltage to step change in input voltage.

vo_t0 = Vonom;
vi_step = 1.0; %vi step from 28 to 29 V

sys = tf(numMv, denMv);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Mv_step = vi_step*step(sys,t) + vo_t0;

figure (16)
plot(tms, Mv_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Mv step','jpg')

% Zo step:  Open-loop response of output voltage to step change in load current.

vo_t0 = Vonom;
i0_step = -0.28; %io step from 0.84 to 0.56 A
```

```
sys = tf(numZo, denZo);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Zo_step = i0_step*step(sys,t) + vo_t0;

figure (17)
plot(tms, Zo_step)
grid on
hold on
% HW Measured Data
plot(0.0001, 13.9742,'o',0.04,13.6547,'o',0.1,13.482,'o',0.2,13.4203,'o', 0.3,13.5969,'o');
plot(0.4, 13.8414,'o',0.5,13.9898,'o',0.6,13.9977,'o',0.7,13.9484,'o',0.8,13.8461,'o');
plot(0.9,13.7883,'o',1.0,13.7828,'o',1.5,13.8648,'o',2.0,13.8547,'o',2.5,13.8508,'o');
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
legend({'{\it Theoretical}','{\it Measured}'},4);
saveas(gcf,'Zo step','jpg')

%>> Twoc : Open-loop transfer function without compensator

Twoc = beta*Tm*Tp;
[numTwoc, denTwoc] = tfdata(Twoc);
[MagTwoc, PhaseTwoc] = bode(numTwoc, denTwoc, 2*pi*f2);

figure (18)
semilogx(f2, 20*log10(MagTwoc));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it T_w_o_c}| (dBV)');
saveas(gcf,'Twoc mag','jpg')

figure (19)
semilogx(f2, PhaseTwoc);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_w_o_c}} ({\circ})');
saveas(gcf,'Twoc phs','jpg')

% Zocld is the transfer function of the desired closed-loop output impedance

fzocld = 20000;
wzocld = 2*pi*fzocld;
Kzocld = 1.*rc;
```

```
numZocld = Kzocld*[1 0];
denZocld = [1 2*pi*fzocld];
Zocld = tf(numZocld, denZocld);
[MagZocld, PhaseZocld] = bode(numZocld, denZocld, 2*pi*f2);

figure (20)
semilogx(f2, 20*log10(MagZocld));
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (dB\Omega)');
saveas(gcf,'Zocld mag','jpg')

figure (21)
semilogx(f2, MagZocld);
grid on
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (\Omega)');
saveas(gcf,'Zocld mag ohms','jpg')

figure (22)
semilogx(f2, PhaseZocld);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o_c_l}} ({\circ})');
saveas(gcf,'Zocld phs','jpg')

% Calculate the transfer function of the output impedance compensator, Tcd

% First Test to Reduce Order of Tcd

R = RLmin*rc/(RLmin + rc);
Kz_test1 = R/rc;
wzocld_c2_test1 = 2*zeta*w0-wz-wrl;
wzocld_c1_test1 = (w0*w0 - wz*wrl)/(wz + wrl);

% Second Test to Reduce Order of Tcd

wzocld_c2_c3_test2 = (w0*(wz+wrl)-2*zeta*wz*wrl)/(2*zeta*(wz+wrl)-w0);
Kz_c2_c3_test2 = R*(wz+wrl+wzocld_c2_c3_test2)/(2*rc*zeta*w0);

% Tcd - set coefficients

Kz = R/rc;
wzocld = 2*pi*20000;
c3 = (1 - Kz*rc/R)/(wz*wrl*wzocld);
c2 = (wz + wrl + wzocld - 2*Kz*rc*zeta*w0/R)/(wz*wrl*wzocld);
```

```
c1 = (wz*wrl + wzocld*wz + wzocld*wrl - Kz*rc*w0*w0/R)/(wz*wrl*wzocld);
c0 = 1;
d2 = 1/wz;
d1 = 1;
Tcx = (Vtm*L*wrl*wzocld)/(beta*VInom*Kz*rc);

numTcd = Tcx*[c3 c2 c1 c0];
denTcd = [d2 d1 0];
Tcd = tf(numTcd, denTcd);
[MagTcd, PhaseTcd] = bode(numTcd, denTcd, 2*pi*f2);

figure (23)
semilogx(f2,20*log10(MagTcd));
grid on
hold on
% HW Measured Data
plot(10,64.51,'o',30.08,55.0,'o',100,45.09,'o',300.8,38.59,'o',1e3,36.49,'o');
plot(3e3,
36.71,'o',10e3,37.7,'o',30e3,38.01,'o',100e3,38.05,'o',300e3,38.08,'o',1e6,38.3,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it T_c}| (dB)');
ylim([35 65]);
legend({'{\it Theoretical}','{\it Measured}'},1);
saveas(gcf,'Tcd mag','jpg')

figure (24)
semilogx(f2,PhaseTcd);
grid on
hold on
% HW Measured Data
plot(10,-87,'o',30.08,-83,'o',100,-69,'o',3e2,-40,'o',1e3, -12,'o');
plot(3e3, 0.8,'o',10e3,3.4,'o',30e3,1.4,'o',100e3,0.3,'o',300e3,-0.5,'o',1e6,-2,'o');
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T_{_c}} ({\circ})');
legend({'{\it Theoretical}','{\it Measured}'},4);
saveas(gcf,'Tcd phase','jpg')

% Loop gain with compensator

Td = Twoc*Tcd;
[numTd, denTd] = tfdata(Td);
[MagTd, PhaseTd] = bode(numTd, denTd, 2*pi*f2);

figure (25)
semilogx(f2,20*log10(MagTd));
grid on
```

```
xlabel('{\it f} (Hz)');
ylabel('|{\it T}| (dB)');
saveas(gcf,'Td loop gain','jpg')

figure (26)
semilogx(f2,PhaseTd);
grid on
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _T} ({\circ})');
saveas(gcf,'Td loop phase','jpg')

% closed loop output impedance with compensator

Zocld1 = Zo/(1 + Td);
[numZocld1, denZocld1] = tfdata(Zocld1);
[MagZocld1, PhaseZocld1] = bode(numZocld1, denZocld1, 2*pi*f2);

figure (27)
semilogx(f2, 20*log10(MagZocld1));
grid on
hold on
% HW Measured Data
plot(10,-69,'o',30,-60,'o',100,-49,'o',300,-40,'o',1e3,-30,'o');
plot(3e3,-20,'o',10e3,-10,'o',30e3,-5,'o',100e3,-3.8,'o',300e3,-3.6,'o',1e6,-3.5,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (dB\Omega)');
legend({'{\it Theoretical}','{\it Measured}'},4);
saveas(gcf,'Zocld1 vs Zocld mag','jpg')

figure (28)
semilogx(f2, MagZocld1);
grid on
hold on
% HW Measured Data
plot(10,0.00035,'o',30,0.001,'o',100,0.0035,'o',300,0.01,'o',1e3,0.031,'o');
plot(3e3,0.1,'o',10e3,0.31,'o',30e3,0.562,'o',100e3,0.65,'o',300e3,0.66,'o',1e6,0.67,'o');
xlabel('{\it f} (Hz)');
ylabel('|{\it Z_o_c_l}| (\Omega)');
legend({'{\it Theoretical}','{\it Measured}'},4);
saveas(gcf,'Zocld1 vs Zocld mag ohms','jpg')

figure (29)
semilogx(f2, PhaseZocld1);
grid on
hold on
% HW Measured Data
```

```
plot(10,89,'o',30,90,'o',100,90,'o',300,90,'o',1e3,88,'o');
plot(3e3,80,'o',10e3,61,'o',30e3,30,'o',100e3,10,'o',300e3,1,'o',1e6,1,'o');
xlabel('{\it f} (Hz)');
ylabel('{\it \phi _Z_{_o_c_l}} ({\circ})');
legend({'{\it Theoretical}','{\it Measured}'},3);
saveas(gcf,'Zocld1 vs Zocld phase','jpg')

% Zo step:  Open-loop response of output voltage to step change in load current.

vo_t0 = Vonom;
i0_step = -0.28; %io step from 0.84 to 0.56 A

sys = tf(numZocld1, denZocld1);
time_step = 1*10^-6;
Tfinal = 0.1*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
Zocld1_step = i0_step*step(sys,t) + vo_t0;

figure (30)
plot(tms, Zocld1_step)
grid on
hold on
% HW Measured Data
plot(0, 13.81, 'o', 0.005, 13.89, 'o', 0.01, 13.94, 'o', 0.015,
13.97,'o',0.02,13.98,'o',0.03,14,'o',0.04,14,'o', 0.05,14,'o');
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
ylim([13.7 14.1])
legend({'{\it Theoretical}','{\it Measured}'},4);
saveas(gcf,'Zocld1 step','jpg')

% Mv step:  Open-loop response of output voltage to step change in input voltage.

Mvcld1 = Mv/(1 + Td);
[numMvcld1, denMvcld1] = tfdata(Mvcld1);
[MagMvcld1, PhaseMvcld1] = bode(numMvcld1, denMvcld1, 2*pi*f2);

vo_t0 = Vonom;
vi_step = 4.0; %vi step from 28 to 32 V

sys = tf(numMvcld1, denMvcld1);
time_step = 1*10^-6;
Tfinal = 3.0*10^-3;
t = 0:time_step:Tfinal;
tms = t*(1*10^3); % convert plot scale to milli-seconds
```

```
Mvcld1_step = vi_step*step(sys,t) + vo_t0;

figure (31)
plot(tms, Mvcld1_step)
grid on
xlabel('{\it t} (ms)');
ylabel('{\it v_0}');
saveas(gcf,'Mvcld1 step','jpg')
```

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