

A Soft-Switching Inverter for High-Temperature Advanced Hybrid Electric Vehicle Traction Motor Drives

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Jason Lai, Wensong Yu, and Pengwei Sun
Virginia Polytechnic Institute and State University

Scott Leslie and Duane Prusia
Powerex, Inc.

Beat Arnet, Chris Smith, and Art Cogan
Azure Dynamics



Virginia Polytechnic Institute and State University
Future Energy Electronics Center
106 Plantation Road (0356)
Blacksburg, Virginia 24061
540-231-4741
www.feec.ece.vt.edu

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1. INTRODUCTION

The state-of-the-art hybrid electric vehicles (HEVs) require the inverter cooling system to have a separate loop to avoid power semiconductor junction over temperatures because the engine coolant temperature of 105°C does not allow for much temperature rise in silicon devices. The proposed work is to develop an advanced soft-switching inverter that will eliminate the device switching loss and cut down the power loss so that the inverter can operate at high-temperature conditions while operating at high switching frequencies with small current ripple in low inductance based permanent magnet motors. The proposed tasks also include high-temperature packaging and thermal modeling and simulation to ensure the packaged module can operate at the desired temperature. The developed module will be integrated with the motor and vehicle controller for dynamometer and in-vehicle testing to prove its superiority.

The main objectives are

1. Develop a soft-switching module to minimize the parasitic components and associated losses.
2. Develop an advanced controlled method for the soft-switching inverter to achieve efficiency higher than 98% over a wide speed and torque range.
3. Optimize the resonant circuit design to reduce the auxiliary circuit losses.
4. Develop an advanced package to allow the soft-switching module to operate with a coolant temperature of 105°C.
5. Test soft-switching inverter under dynamometer and in-vehicle conditions to verify the desired performance.
6. Reduce the inverter cost for electric and hybrid electric vehicle applications.

The approaches to achieving the project goals include the following:

1. Obtain inverter component V-I stresses through vehicle level and motor drive simulations.
2. Develop a variable timing controlled circuit for switching loss reduction for a wide speed and torque range.
3. Develop a hybrid soft switch module by combining IGBT and MOSFET for conduction loss reduction.
4. Develop a low thermal impedance module with integrated heat sink for high temperature operation.
5. Develop a highly integrated soft-switch module for low-cost and low parasitic packaging.
6. Predict device junction temperature and optimize module design through modeling and simulation.
7. Develop high-accuracy ratio metric calorimeter for ultrahigh efficiency inverter/dyno testing
8. Test the soft-switching inverter with existing EV platform and dynamometer for EMI and efficiency performance verification.
9. Test electromagnetic interference (EMI) performance

10. Test and validate module level thermal performance

This report will describe the detailed technical design of the soft-switching inverters and their test results. The experiments were conducted both in module level for the module conduction and switching characteristics and in inverter level for its efficiency under inductive and dynamometer load conditions. The performance will be compared with the DOE original specification.

2. PROPULSION SYSTEM SIMULATION

The purpose of the propulsion system level simulation is to determine the voltage and current stresses the inverter will be subjected to in a typical vehicle application. Also, the simulation will confirm that the inverter specification is adequate in all operating conditions for standard vehicle use. The purpose of the simulation is not to find inverter efficiency or motor efficiency. An assumed efficiency is used to provide more accurate inverter voltages and currents, but no great effort is made to accurately model the inverter. Once typical use data is known, typical operating points can be chosen for later efficiency study and reliability study. Table 2.1 shows key parameters used in the vehicle level simulation. Table 2.2 shows circuit parameters of the Siemens 1PV5135 induction motor.

Table 2.1. Parameters used during system simulation.

Parameter	Value	Comment
DC bus voltage: V_{dc}	312 V	Nominal voltage in vehicle application
Battery internal resistance: R_{bat}	0.3 Ω	Medium stiffness battery pack
Inverter efficiency: η_{inv}	0.95	Assumed inverter efficiency for DC bus current calculation
Inverter output peak current: I_{max}	400 A	Peak phase current out of inverter
Vehicle mass: m	1600 kg	Vehicle Mass
Tire radius: r	0.292 m	Tire radius
Gear ratio: g	11	Gear ratio
Density of air: ρ	1.2 kg/m ³	Density of air
Vehicle drag coefficient: c_d	0.32	Vehicle drag coefficient
Vehicle frontal area: A_f	2.5 m ²	Vehicle frontal area

Table 2.2. Siemens 1PV5135 motor parameters.

Parameter	Value	Comment
Stator resistor: R_s	0.012 Ω	Stator resistance
Leakage inductance: L_{lk}	140 μH	Assume same for both stator and rotor
Rotor resistance: R_r	0.0065 Ω	Rotor resistance
Pole pairs: P_p	2	Pole pairs
Magnetizing inductance: L_m	1500 μH	Magnetizing Inductance

The propulsion system simulation is shown below in Figure 2.1. The simulation was conducted using Matlab Simulink and PLECS. PLECS is an electrical circuit simulator that runs within Simulink. The inverter electronics were modeled by a controlled three-phase voltage source, which was then connected to the PLECS AC induction motor model. The motor model was adjusted so that saturation was present at high magnetizing currents. The inverter and motor are represented by the yellow block in Figure 2.1. The inputs to the inverter are the previously mentioned AC voltage command and the motor speed as set by the vehicle speed. The inverter and motor outputs are the phase current, electrical angle of the rotor, torque produced, and several other internal values for troubleshooting purposes.

The vehicle portion of the simulation is represented by the orange block below. The torque acts on the vehicle mass through the gear box and tire diameter to provide traction to the road. Air resistance and a fixed rolling resistance are also modeled. The vehicle block outputs are vehicle speed and motor shaft speed. The inside of the vehicle block is shown in Figure 2.1. For the purposes of this simulation no gear box loss is used.

The motor shaft speed is fed back to the motor control block shown on the center of Figure 2.1 in blue. This block takes in commanded torque, available DC bus voltage, measured current, shaft speed, and flux position. With that information the motor utilization portion of the control decides how to best control the current and voltage to achieve the desired torque. The desired D and Q axis current are fed into a controller, which then looks at the actual DQ current and adjusts the DQ voltage to achieve the desired current. Finally, the DQ voltages are converted to the stationary reference frame and fed to the inverter block. The slip is also brought out so that it can be used to determine the flux position. The inside of this block contains proprietary algorithms and is not shown at this time.

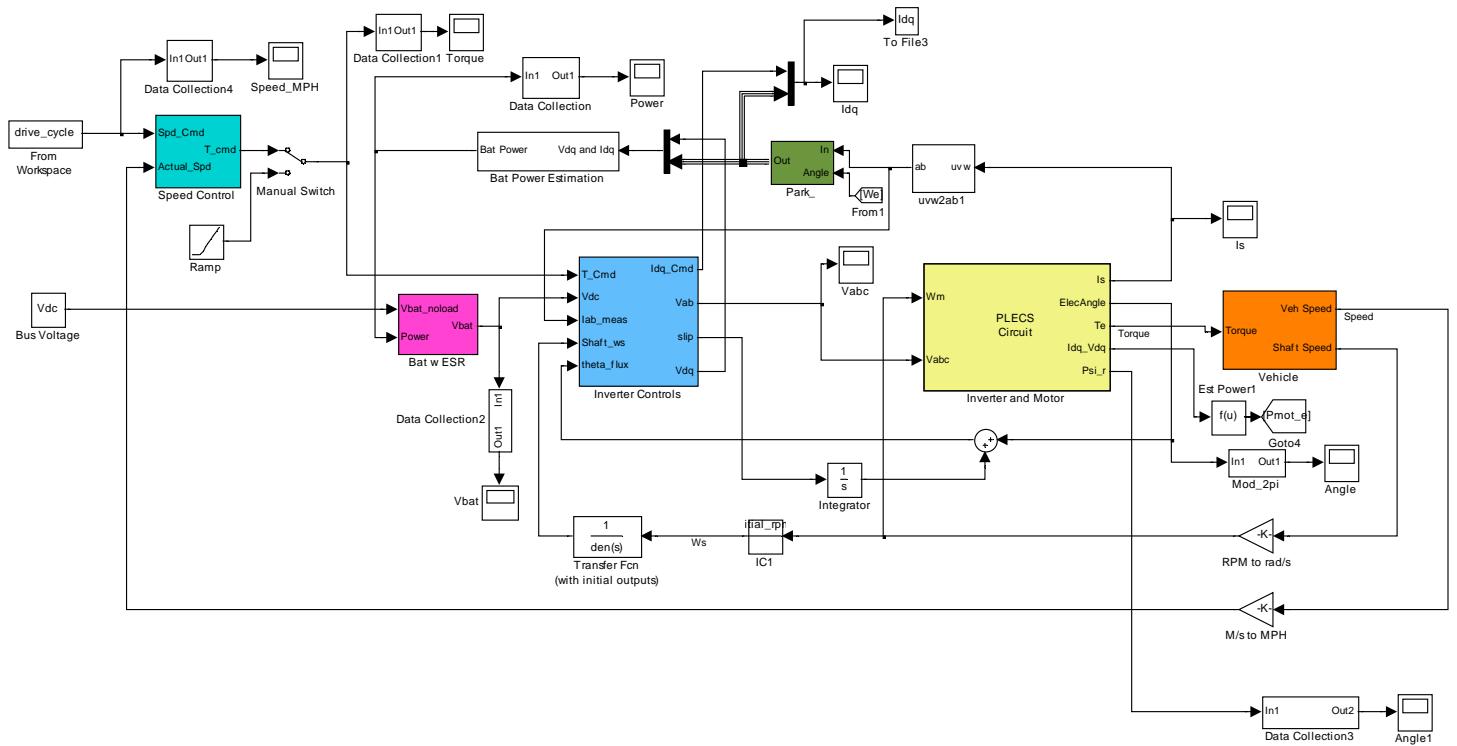


Figure 2.1. The overall propulsion system simulation.

The battery is modeled by the pink block in Figure 2.1. This block takes the open circuit voltage of the battery pack and battery power consumed. With this information it calculates the actual output voltage of the pack using the series resistance parameter. In the white block above the battery block the inverter output power is calculated using the output voltage and current. From there it is assumed that the inverter is 95% efficient and the required input power is calculated.

The speed regulator is shown in teal on the left hand side of Figure 2.1. Its job is to act like the driver of the vehicle. Its inputs are the drive cycle speed and the actual vehicle speed. The actual controller is a PI regulator but it is tuned conservatively so that it does not react too quickly. Its output is the commanded torque which is the same as the accelerator pedal output. The regulator also has a limit for positive and negative torque 210 Nm and -100 Nm respectively. The positive limit is above the actual motor limit and the negative limit is in place to prevent huge power spikes during braking. In an actual vehicle the friction brakes would take over when the regenerative braking had reached its limit.

The US06 drive cycle was chosen because it is one of the more practical drive cycles available. It includes a good mix of both low speed (city) driving and high speed (highway) driving. The drive cycle speed and the actual speed from the simulation are shown in Figure 2.2. It should be noted that the vehicle does not follow the trace exactly for several reasons. First on some of the harder accelerations at high speed (300 s and 580 s) the motor doesn't have quite enough torque available. This is not a huge concern because the purpose of the simulation is only to stress the inverter as it might be used in a vehicle. The trace also misses on some of the steep deceleration areas but as mentioned previously the additional breaking would be provided by friction brakes.

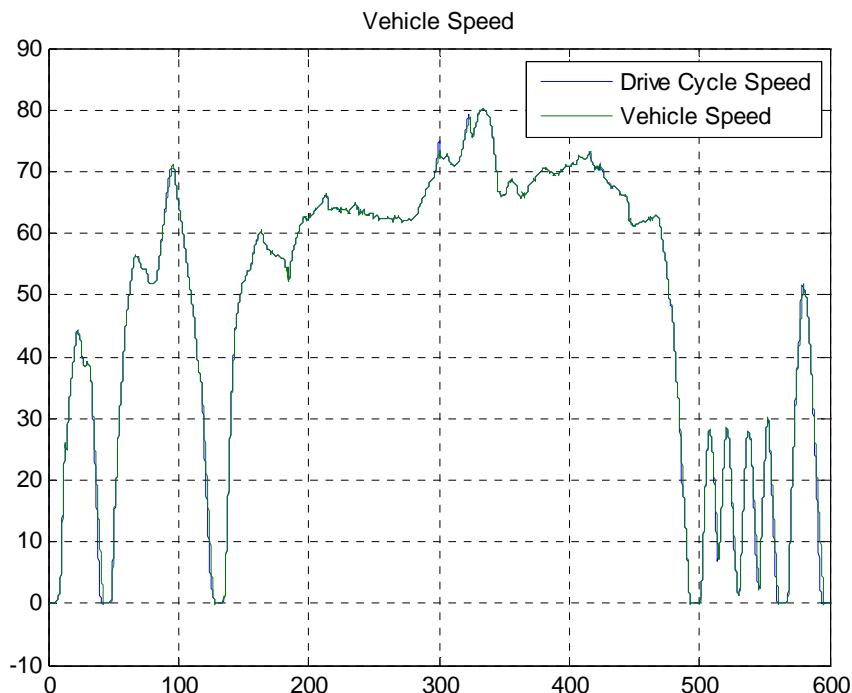


Figure 2.2. Vehicle Speed over US06 drive cycle. Speed is on the Y-axis in MPH. The x-axis is seconds.

The commanded motor torque and actual torque are shown in Figure 2.3. At higher speed the available motor torque is significantly reduced. When the speed regulator starts to stop tracking it saturates the motor torque to its peak output command of 210 Nm. Once the speed is tracking well the commanded torque comes back down to the actual required level.

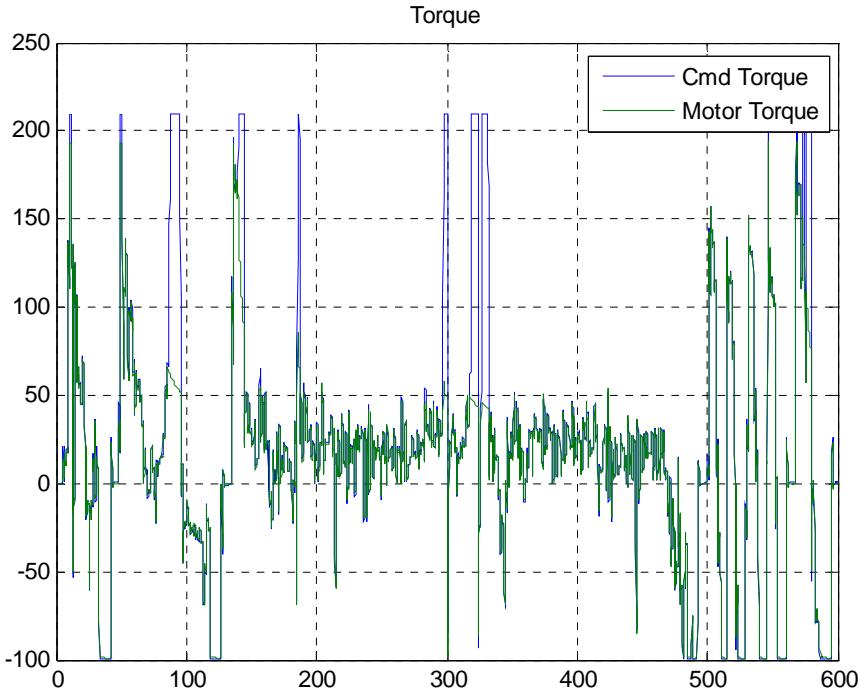


Figure 2.3. The motor torque commanded by the speed regulator and the actual torque produced are shown above. Torque (y-axis) is shown in Newton-meters and time is shown in seconds.

The power required at various places in the simulation is shown below in Figure 2.4. The inverter output is the same as motor input, shown in red. The inverter output peaks at just below 60 kW. The motor shaft output power is also shown in green. The motor output is less than the input for efficiency reasons. It should be noted that this is not a comprehensive motor loss simulation so that data should only be used for comparison purposes.

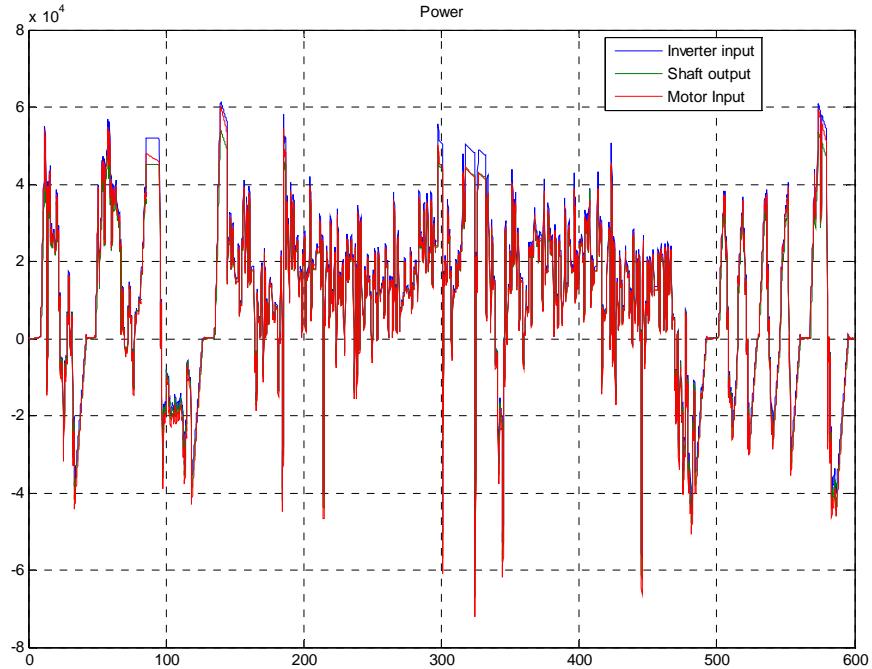


Figure 2.4. The inverter power (y-axis) is shown in watts above. The x-axis is time in seconds.

The inverter output line-to-neutral voltage peak amplitude is shown in Figure 2.5. The commanded current amplitude (again the crest of the sine wave) is shown below in Figure 2.6. It does not include any additional peak due to switching ripple. The peak current exceeds 400 A under heavy load conditions.

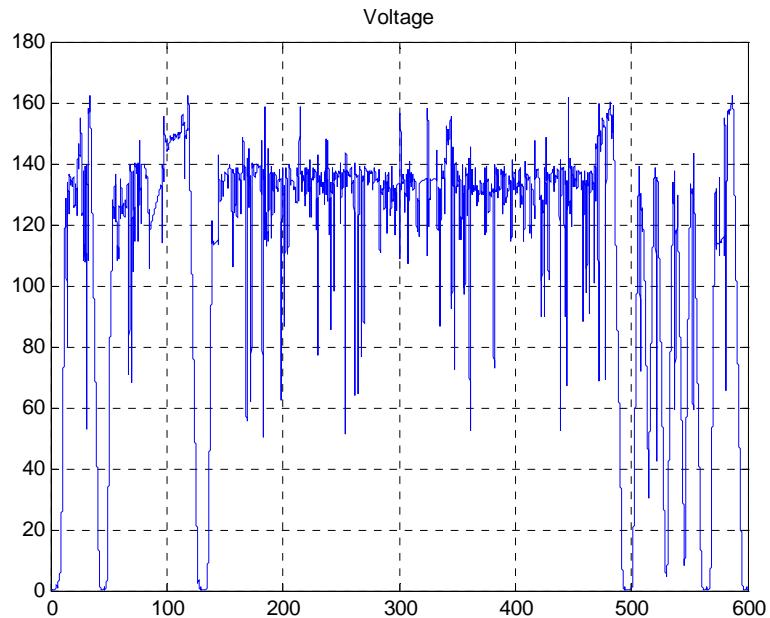


Figure 2.5. The inverter output voltage (line-neutral) amplitude is shown above. The x-axis is time in seconds.

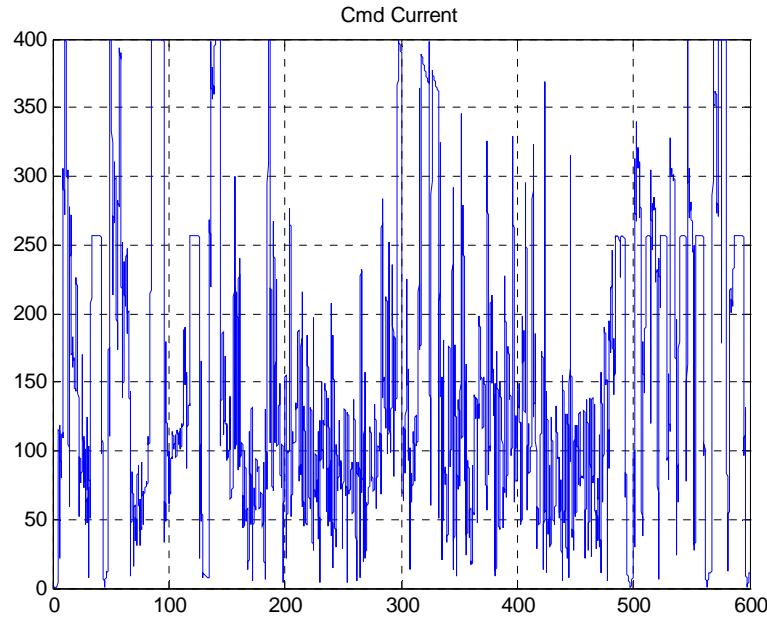


Figure 2.6. The amplitude of the phase current commanded by the motor control block is shown above in Amps (y-axis). The x-axis is time in seconds.

The motor power factor is shown below in Figure 2.7. The power factor varies quite a bit. It can reach all the way up to unity power factor (1) and down to almost all reactive power (0). Negative power factor is present when the current leads the voltage and typically only occurs during transients. The DC bus voltage for the battery under load is shown in Figure 2.8. Under heavy load condition, the DC bus voltage drops below 240 V.

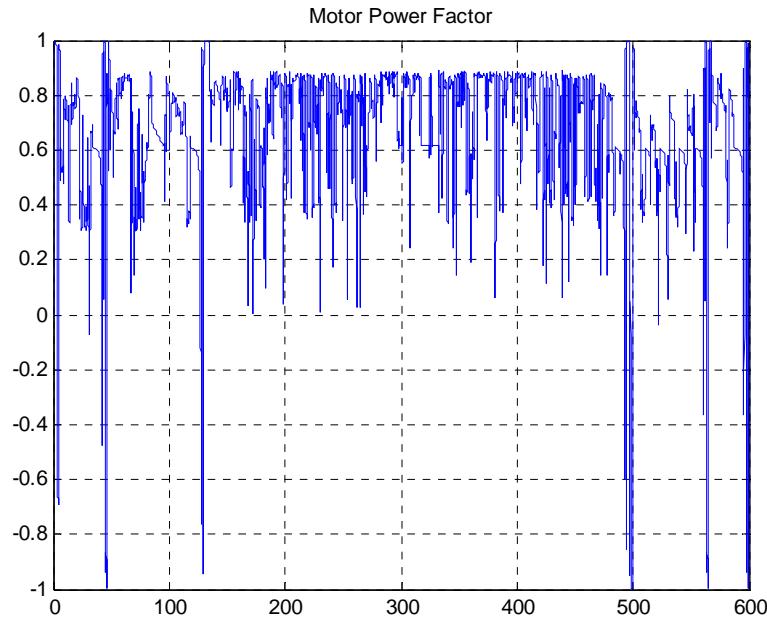


Figure 2.7. The motor power factor average is 0.68 over the entire cycle.

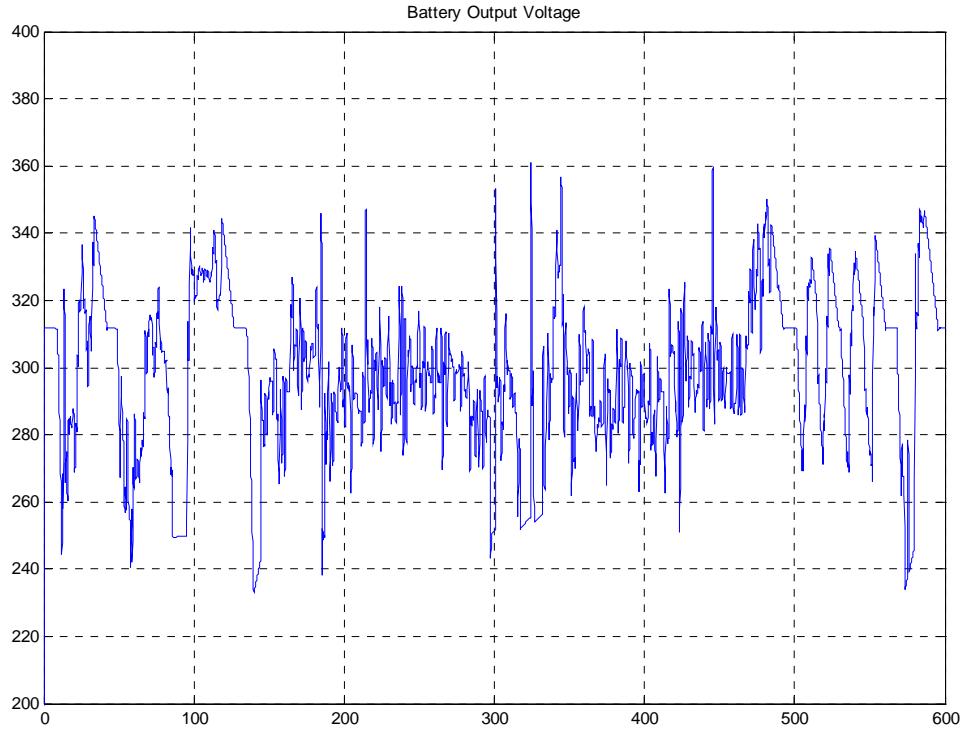


Figure 2.8. The ESR of the battery causes the output voltage to dip or rise when large amounts of current are drawn.

The peak power called out in the DOE proposal was 55kW for 18 seconds. The worst case for this peak is at lower speed. At zero speed it is not possible to achieve this power level due to low output voltage. From the previous sets of figures one could choose the point at about 3 seconds as the lowest speed possible to achieve 55 kW. The inverter conditions at that point are summarized below in Table 2.3.

Table 2.3. The circuit conditions present at the worst case 55-kW operating point

Measurement	Quantity
V_{dc}	244 V
I_{ac-pk}	400 A
V_{ac-ps}	112 V
Power Factor	0.78

The proposed current limit of 400-A peak is adequate for a 55-kW motor or 60-kW inverter for vehicle use. The Siemens motor was chosen because of its ease of integration into a vehicle and its high speed capability. Other motors such as permanent magnet may seem attractive but have their own problems at high speed when the back EMF voltage is dangerously high unless properly controlled. Higher voltage electronics must be used and this contributes to increased cost and lower efficiency. It appears that a permanent magnet design is overall less robust and

more costly in automotive applications. The Siemens motor power factor is quite good (0.85) at certain operating points.

The data shown in the previous figures is available as an accompanying Excel spreadsheet for further analysis such as reliability predictions and thermal modeling. The output current, voltage, and power factor could also be used as an input into a circuit level model of our soft-switching inverter. The data shown is not a comprehensive list of all worst case scenarios. Other operating points such as DC current out of the inverter for an indefinite amount of time should also be considered. The numbers above should be used as an average use profile for the inverter design.

3. SOFT-SWITCHING TECHNIQUE

3.1. Variable Timing Soft-Switching Technique

Figure 3.1 shows a possible implementation for variable timing controlled soft-switching converter circuit, where S and D are the main switch and freewheeling diode, S_x is the auxiliary switch, and C_r is the resonant capacitor. A typical switching sequence is to turn on the auxiliary switch according to the pulse-width modulation (PWM) signal. After the auxiliary current I_{aux} exceeds the load current I_{load} , the excess current will discharge the resonant capacitor C_r and thus resulting in a resonance, which reduces the device voltage V_s down to zero. During the zero voltage period, switch S can be turned on without incurring loss. The conventional approach to turn the main switch on is to use a fixed timing delay or controlling the delay turn-on based on the current magnitude. The proposed variable timing technique is to sense the device voltage and wait until it reaches almost zero, then turn on the main switch at the exact zero-voltage condition. The conceptual implementation circuit in Figure 3.1(a) is to use a comparator that compares reference voltage V_{ref} and the sensed voltage V_s . When V_s drops below V_{ref} , the comparator output becomes high. When both comparator output and PWM signals are high, then the main switch is turned on. The reference voltage can be zero for a low voltage system. For the dc bus voltage V_{dc} higher than a few hundred volts, the reference voltage can be set at a few volts to allow time for the comparator and logic control circuit to react. The output of the comparator goes through a hysteresis to tolerate the noise once the zero-voltage switching is achieved.

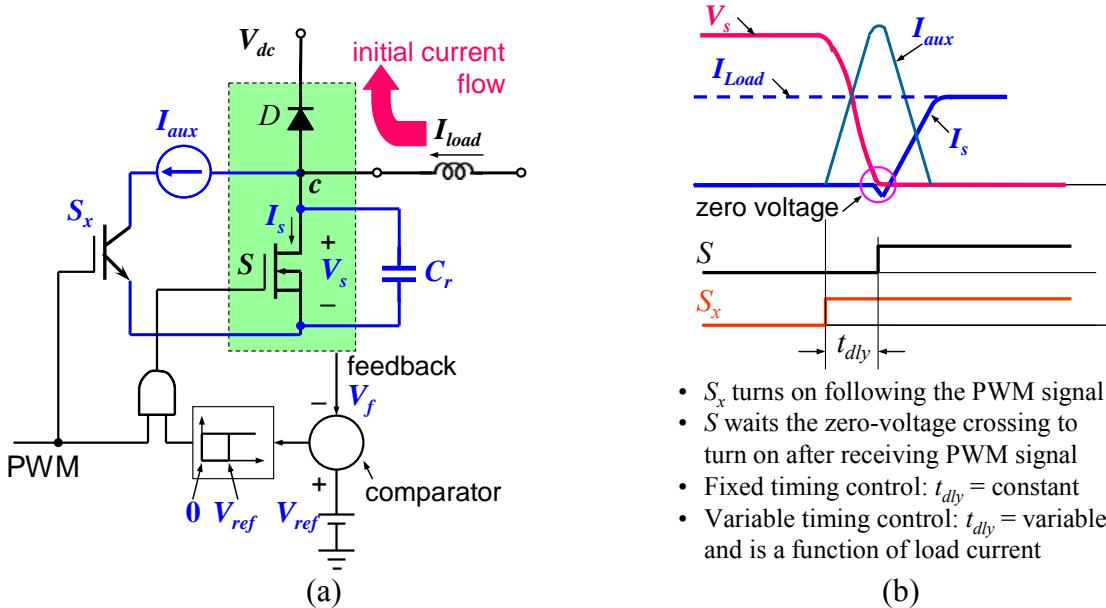


Figure 3.1. Soft-switching converter circuit with variable timing control for zero-voltage switching: (a) conceptual circuit diagram, and (b) switching timing and key voltage and current waveforms.

Figure 3.1(b) shows the switching timing and key voltage and current waveforms of the variable timing controlled soft switching converter. Here S_x follows the PWM command to turn on. The auxiliary current I_{aux} increases linearly until it reaches the load current I_{load} . When I_{aux} is higher than I_{load} , the excess current will discharge the resonant capacitor C_r , which results in a resonance. During resonance, the device voltage V_s swings down to zero, and the main switch S

can be turned on at zero volts. The switch current I_s starts increasing until it reaches the load current I_{load} and then stabilizes. With the proposed approach, the turn-on time of the main switch S is always at zero voltage, which implies the switching delay t_{dly} needs to be variable. Because the time for the auxiliary current to reach the load current varies with the load condition, the fixed delay timing control cannot guarantee the switch turn-on at zero-voltage condition. The variable timing is thus preferred to the fixed timing approach.

Figure 3.2 shows variable timing controlled soft switching simulation results for positive current cycle at high current (300 A), medium current (150 A), and zero current conditions. Under different current conditions, the device current rises after voltage V_{ce} drops to zero with the same timing delay.

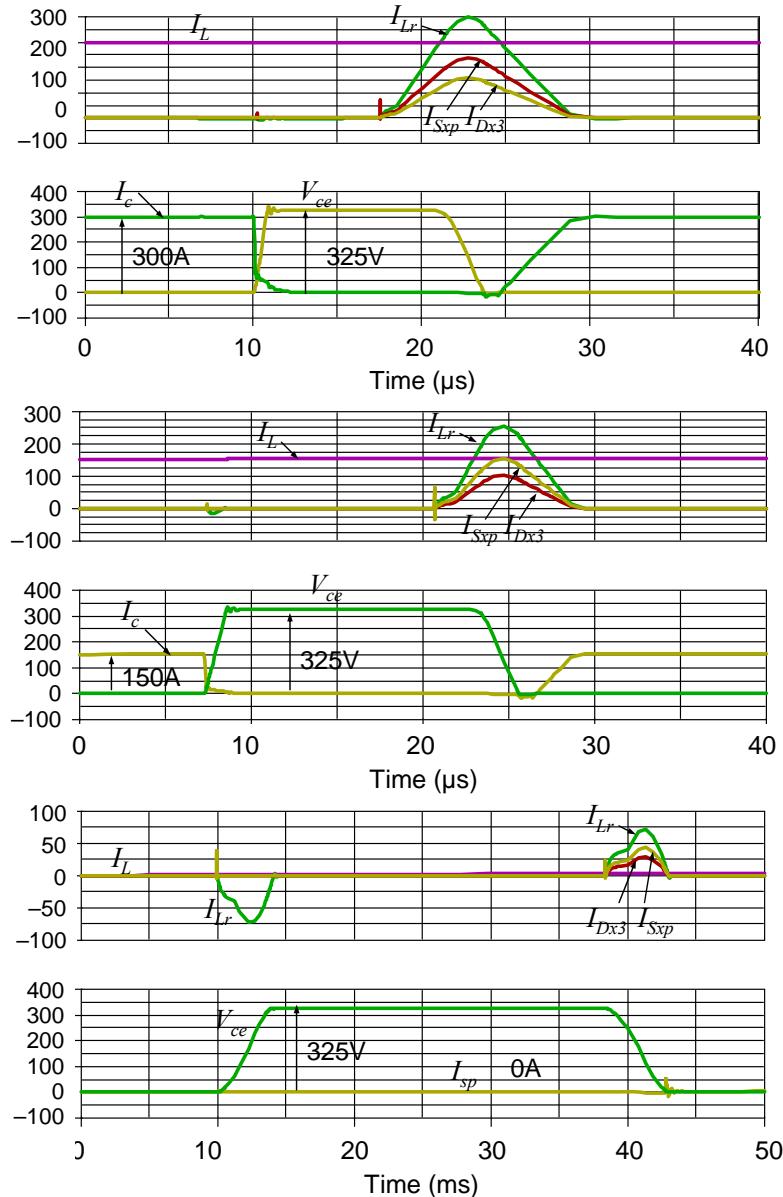


Figure 3.2. Variable timing controlled soft switching simulation for positive current cycle at high current (300 A), medium current (150 A), and zero current conditions.

Figure 3.3 shows variable timing controlled soft switching simulation for negative current cycle at medium current (-150 A), high current (150 A), and zero current conditions. Under different current conditions, the device current rises after voltage V_{ce} drops to zero with the same timing delay.

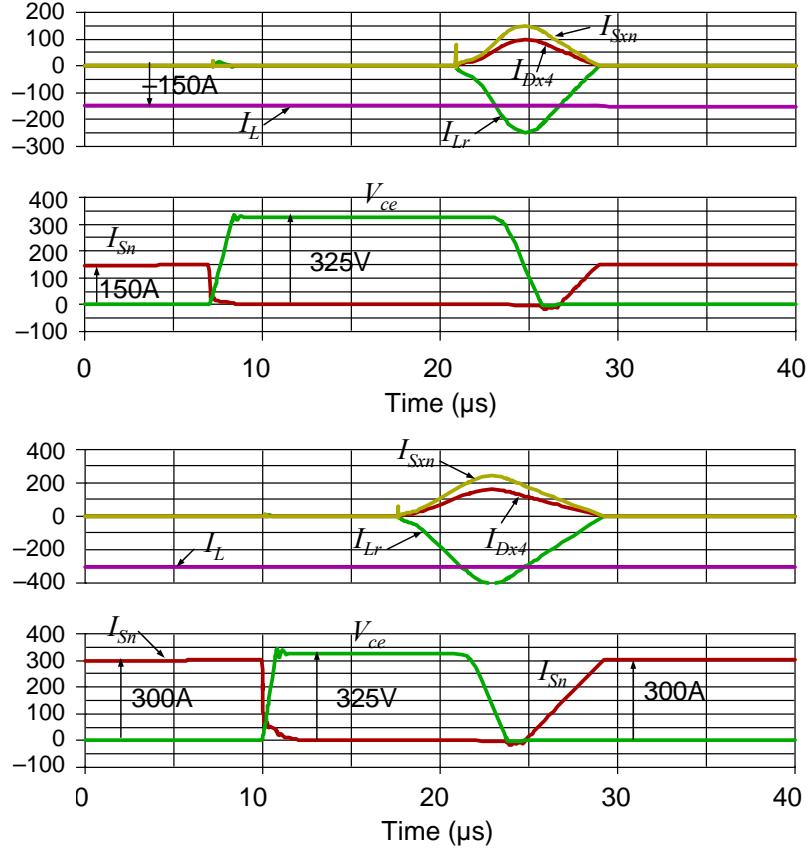


Figure 3.3. Variable timing controlled soft switching simulation for negative current cycle at medium current (-150 A) and high current (-300 A).

Figures 3.4(a) and 3.4(b) show verification of variable timing control with simulation and experimental results. Under different load conditions, the delay time t_{dly} varies. However, the gate turn-on delay after device voltage V_{CE2} drops to zero, t_z , is fixed. Both simulation and experimental results agree with each other very well at three different current conditions.

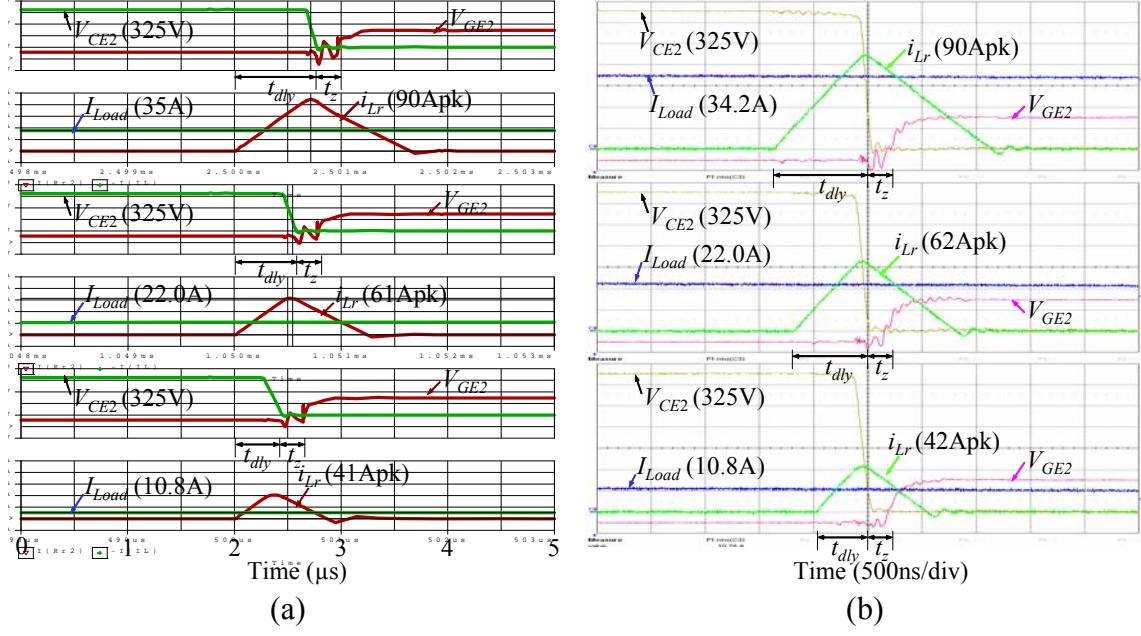


Figure 3.4. Verification of variable timing with simulation and experimental results: (a) simulation of soft switching under different current conditions, and (b) experimental verification of soft switching under different current conditions.

3.2. Circuit Level Simulation for Device Selection

With the base frequency 83.3 Hz, which should produce 2500 rpm for the 2 pole-pair machine, the load torque is 210 Nm. All other circuit parameters are the same as those used in vehicle level simulation. Figure 3.5 shows the simulated closed speed loop control results using the above available voltage at the rated speed and torque. The stator voltage and current are 158.4 V and 340 A, respectively.

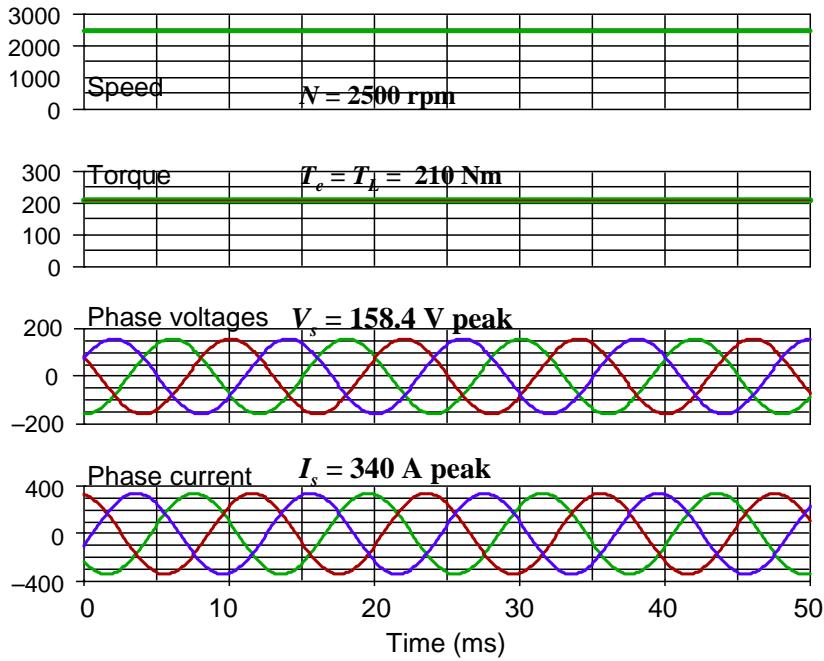


Figure 3.5. Closed speed loop simulation results with fully utilization of DC bus voltage at the rated speed and torque condition.

By connecting the above motor to the standard 6-bridge inverter, the simulated voltage and current waveforms can be shown in Figure 3.6. In this simulation, the inverter output voltage is maximized with space vector modulation (SVM). The DC bus voltage is 280V, and the output peak current is 330 A. With PWM phase voltage, the motor input draws sinusoidal current with a power factor of 0.87.

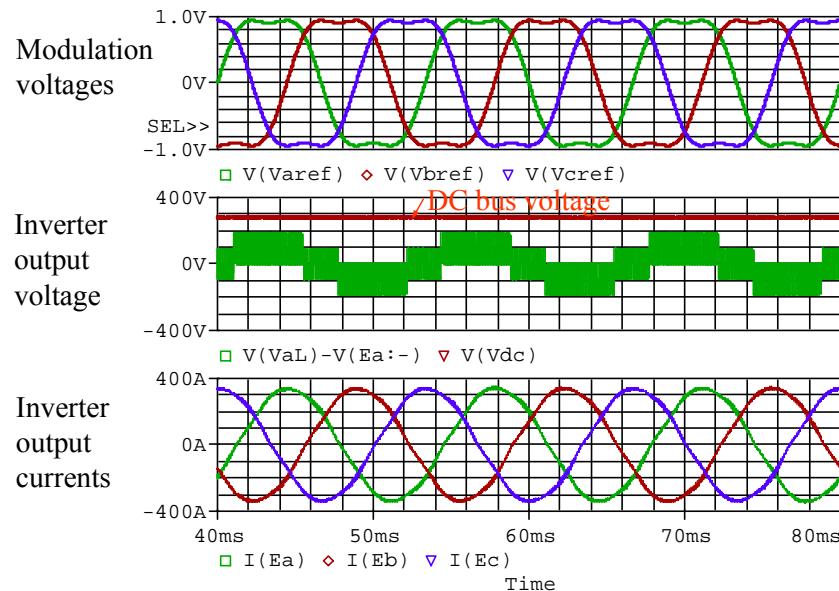


Figure 3.6. Simulated voltage and current waveforms for the entire SVM controlled inverter-motor system.

The complete motor drive has been simulated under hard and soft switching conditions using 300-A, 400-A, and 600-A devices. The purpose of the simulation is to ensure sufficient efficiency and acceptable junction temperature under 105°C operation. Figure 3.7 shows efficiency comparisons between soft switching and hard switching: (a) using 400-A device and (b) using 600-A device. The variable timing achieves higher efficiency at light loads for both 400 and 600-A devices. The 600-A device has a slightly higher efficiency at heavy load conditions for both hard and soft switching inverters; however, its efficiency improvement is insignificant to be noticeable. The junction temperature should be lower with a larger die size, and the use of 600-A device is almost necessary under hard switching condition. However, for soft switching inverter, the efficiency with 400-A is significantly higher than that with 600-A under hard switching condition, and therefore, the soft-switching with 400-A device is favored through the comprehensive comparison here.

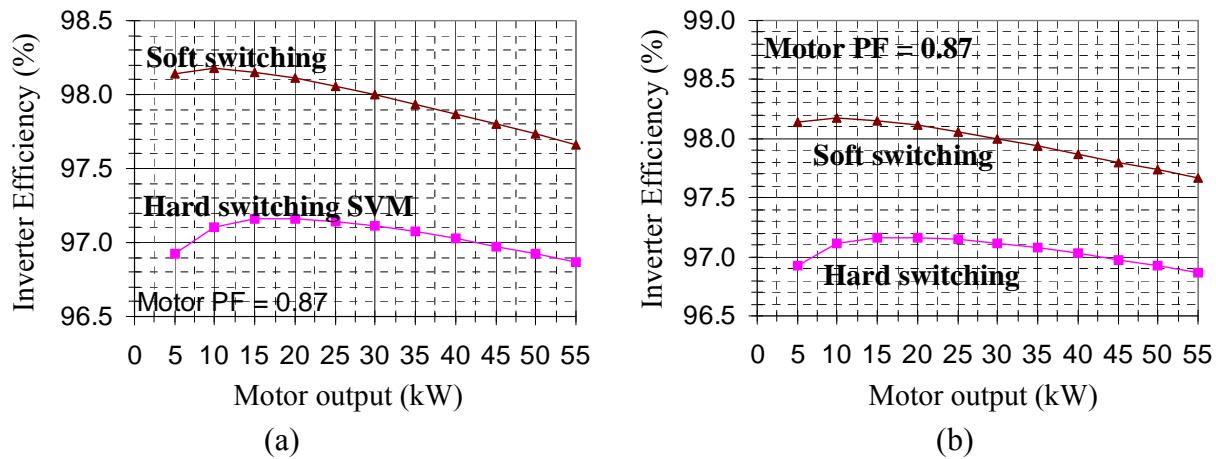


Figure 3.7. Efficiency comparison between soft switching and hard switching: (a) using 400-A device and (b) using 600-A device.

Table 3.1 compares conduction and switching losses at full load condition between hard and soft switching inverter. Under hard switching condition, the switching loss is the same level as the conduction loss. With either device, the soft switching inverter reduces switching loss about 60% or total loss about 30%.

Table 3.1. Loss comparison at full load condition between hard and soft switching inverters.

Device loss at 55-kW output	Use of 400-A IGBT		Use of 600-A IGBT	
	Hard SW.	Soft SW.	Hard SW.	Soft SW.
Conduction (W)	882	882	752	752
Switching (W)	824	360	895	392
Total (W)	1706	1242	1647	1144

Figure 3.8 compares efficiency profiles using different current rating IGBTs for hard and soft switching inverter. Figure 3.8(a) compares the losses using (a) 300-A device, (b) 400-A device,

and (c) 600-A device under hard switching condition. The 300-A device drops the efficiency very quickly under heavy load condition. Although the light load efficiency favors 300-A device, the junction temperature at heavy load is a major concern. Figure 3.8(b) compares the losses using (a) 300-A device, (b) 400-A device, and (c) 600-A device under soft switching condition. The efficiency with 300-A device is the lowest among them, but it is still significantly higher than any of hard switching cases. For cost consideration, 300-A IGBT has a chance to be successfully used in this case even at 105°C coolant condition. However, to be conservative, our first prototype will go with 400-A.

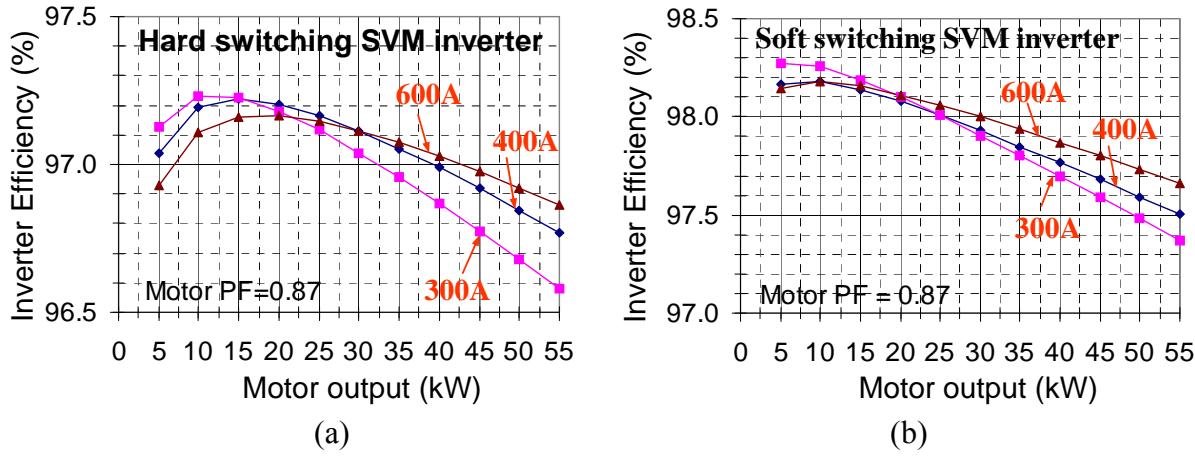


Figure 3.8. Efficiency comparison between different devices under hard and soft switching conditions: (a) hard switching and (b) soft switching.

3.3. Select and Characterize Power Devices for High Temperature Operation

The device conduction and switching performances at high temperature conditions differ among different IGBTs. At high temperatures, some devices have lower conduction voltage drop, and some devices present higher switching loss devices. It is well known that Schottky diodes and power MOSFETs have positive temperature characteristics, and thus it can be easily justified that these two devices are not suitable for high temperatures. Instead, the conventional junction diodes and IGBTs are more suitable for high temperature. However, some IGBTs that are suitable for high temperatures may not be suitable for soft switching operation. The following section compares the three common IGBT configurations: non punch through (NPT), punch through (PT), and light punch through (LPT). Cross sectional views of each device are shown in Figure 3.9. These sections examine how their fabrication affects the current they produce during zero voltage switching.

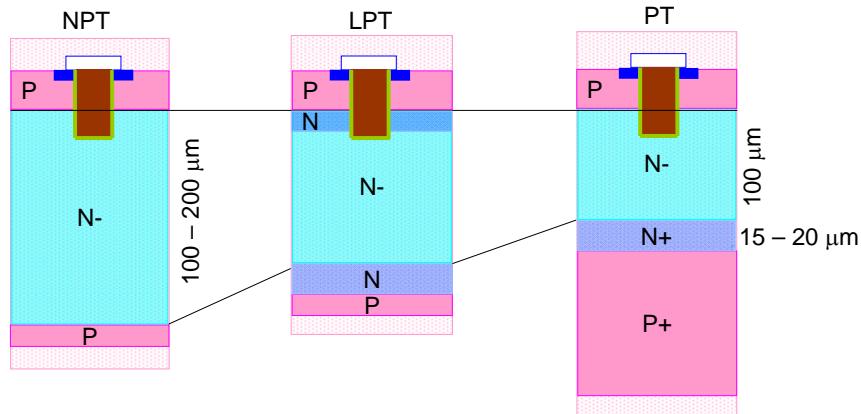


Figure 3.9. Internal structure comparison of different IGBTs.

A. Non-Punch-Through IGBT

Non-punch-through (NPT) devices employ the relative low-cost float-zone wafer and are characterized by having a wide, lightly doped base. High power NPT IGBT's have N^- layer base widths within the range of 100 – 200 μm . With a high value of base width, the gain of the PNP transistor within the IGBT becomes very low. Even when the rated values of forward voltage are dropped across the device and the depletion region is at a maximum, the remaining undepleted base is wide enough to keep the value of β_{PNP} low. The wide base also means charge carriers are distributed over a wider region, driving down the value of δ_p . These characteristics maintain low magnitude current tail during zero voltage switching. However, carrier lifetime is relatively long (1-15 μs) in the base of this device, causing the tail to propagate for long periods.

The conduction voltage drop V_{ce} is proportional to the thickness of the N^- layer. To reduce the V_{ce} drop, thinner N^- layer is necessary. However, it will reduce the blocking voltage capability because it lacks a P-type buffer layer that is present in the punch-through (PT) type IGBT.

B. Punch Through IGBT

The significant difference between PT and NPT IGBTs is within the base region. The PT devices employ relatively expensive epitaxial structure and has a heavily doped n-type buffer (N^+) layer at the emitter-base junction, usually around 15 – 20 μm in width. The buffer layout allows higher blocking voltage capability as compared to that of NPT devices, thus it allows a lightly doped N^- base region, which is significantly thinner than the base region in a comparable NPT device. A thinner N^- base region results in improved forward conduction characteristics, but this thinner base can cause problems with higher values of β_{PNP} during switching and increased carrier concentration close to the collector-base junction. This can potentially cause current tails with significant magnitude. To counter this problem, the carrier lifetime of the base region is significantly reduced using carrier lifetime killing techniques. Typical values of carrier lifetime in the base of a PT device range from 0.5 – 0.01 μs .

Shortening the carrier lifetime causes fast recombination of carriers in the base and significantly reduces current tail. However, when the carrier lifetime is reduced enough, the RC time constant of the IGBT becomes dominant and will affect the response of the device.

C. Light Punch Through IGBT

Light punch through (LPT) devices are relatively new and have a characteristic in between PT and NPT devices by having a moderately doped buried layer between the collector and the base N^- region of the device, often termed the carrier stored layer. This carrier-stored layer helps maintain a suitable number of carriers near the collector-base junction. There is still an N^+ buffer layer between the emitter and the base region, but this is not as heavily doped as buffer layers in PT devices. The width of the LPT base region is greater than a PT but less than a NPT base width. Carrier lifetime killing techniques are not used during the fabrication of LPT IGBTs. The additional buffer layer between the collector and the base of the device is significant in impeding the rapid expansion of the depletion region into the base at the onset of increasing voltage. The concentration of holes and free electrons swept by the depletion region is much smaller and β of the internal PNP transistor remains small because the change in depletion width is greatly impeded, causing the tail current to be negligible through most or all of the switch off transition.

With the compromise in buffer layer and the thickness of N^- region, the LPT device present conduction and switching characteristics in between those of PT and NPT. Figures 3.10 and 3.11 compare the normalized turn-off loss E_{off} and conduction voltage drop V_{ce} among them. Assuming $E_{off} = 1$ at 25° condition, the PT device shows much higher turn-off loss at high temperatures due to a larger current tail magnitude. The NPT device, on the other hand, has a near constant turn-off loss due to small tail current. For the conduction voltage drop V_{ce} , NPT has a positive temperature coefficient, and PT has a negative temperature coefficient. The LPT device characteristic can be anywhere in between.

The problem with NPT is clearly on the positive temperature coefficient that will increase the conduction loss. For a relatively low voltage system, it is not desirable. The problem with PT is also clearly on the turn-off energy penalty at high temperature. However, if the soft switching can reduce or eliminate the turn-off loss, then PT is preferred.

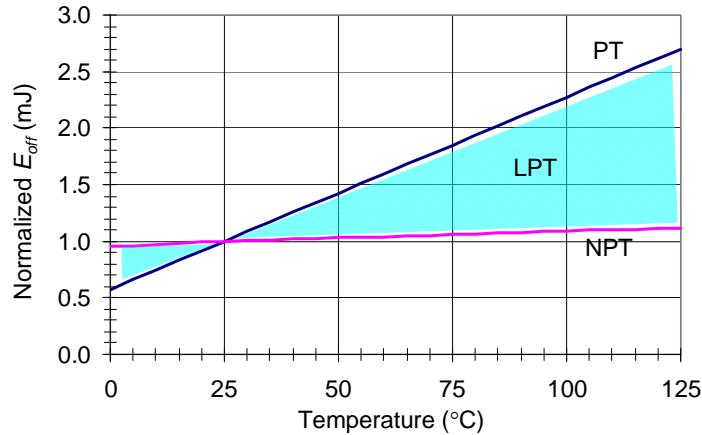


Figure 3.10. Normalized E_{off} comparison among three different IGBTs.

Since the proposed zero-voltage soft switching is to eliminate the turn-on loss and to reduce the turn-off loss by a lossless snubber capacitor. In this case, it depends on how much loss reduction can be gained. If the PT device loss reduction is only 50%, then the overall gain may not be justified. Therefore, our search goes to LPT type, which has near negative temperature coefficient and less sensitive temperature coefficient than that of PT devices. LPT device employs the float-zone wafer material and is potentially lower cost than that of the epitaxial-based PT devices. Through device conduction voltage drop and switching loss evaluation, the commercially available CM400DY-12NF, rated 600V, 400A and 600A LPT type IGBTs are considered the candidate for the high-temperature soft-switching applications.

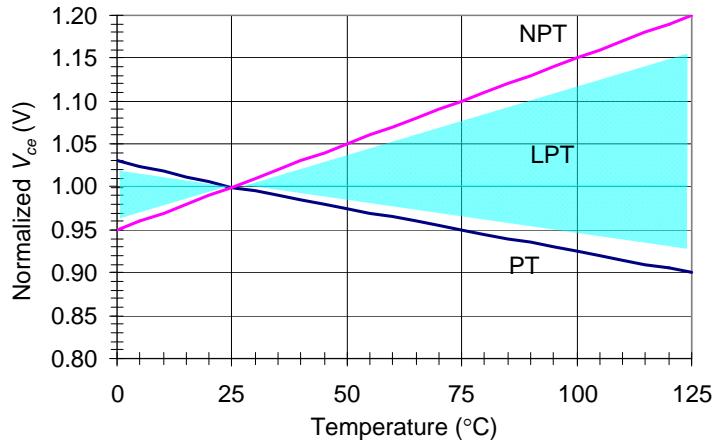


Figure 3.11. Normalized V_{ce} comparison among three different IGBTs.

3.4. Conduction loss Measurement Results

In order to prove that the selected device conduction voltage drop has a negative temperature coefficient, the device conduction voltage drop was measured first against datasheet value and second at different temperatures. Figure 3.12 shows the measured LPT-IGBT and diode voltage

drops against the datasheet. The LPT-IGBT voltage drop tends to be higher than that of the datasheet value possibly due to parasitics, while the diode voltage drop tends to have a lower voltage drop possibly due to self-heating effect.

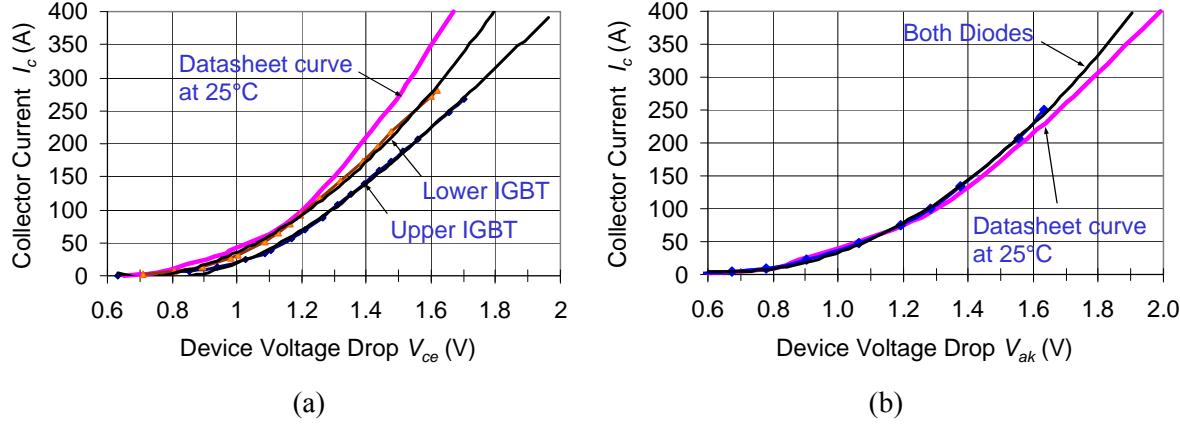


Figure 3.12. Measured LPT-IGBT and diode conduction characteristics in comparison with datasheet results: (a) IGBT, and (b) diode.

Figure 3.13 shows measured LPT-IGBT and diode voltage drops at different temperatures. In this test, the temperature is well regulated with a chiller. Both IGBT and diode show negative temperature coefficient. The diode voltage drop is significantly lower at a higher temperature. The IGBT shows a significant lower voltage drop at lower current region, but the difference is diminishing at higher current condition. However, both IGBT and diode present the desired negative temperature coefficient.

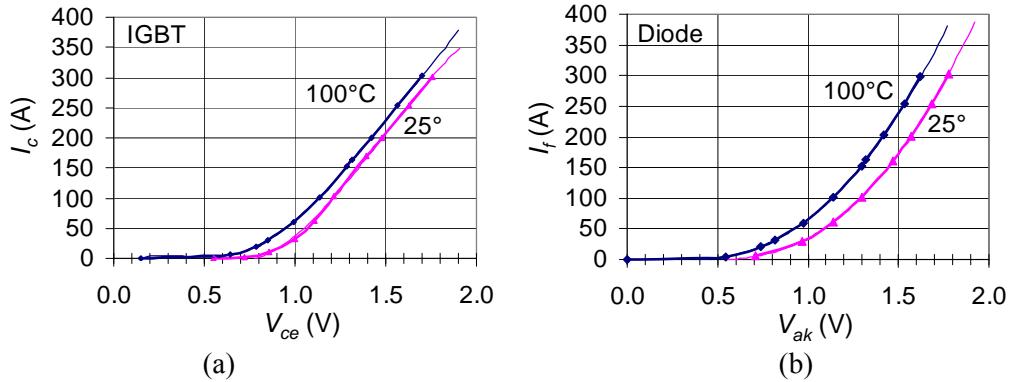


Figure 3.13. Measured IGBT and diode voltage drop as a function of temperature: (a) IGBT and (b) diode.

For comparison purposes, NPT IGBT and SiC Schottky diodes were measured to see their conduction voltage drop performance under different temperature conditions. Figures 3.14(a) and 3.14(b) show conduction voltage drop of NPT IGBT and SiC Schottky diode at 25°C and 100°C conditions. The NPT IGBT is rated 1200V, 400A, and the SiC Schottky diode is rated 1200V, 200A. The voltage drop of both NPT IGBT and SiC Schottky diode under high temperature condition is higher than that under low temperature condition, thus both are considered positive temperature coefficient and are not suitable for high temperature operation.

The VI curves of SiC diode under both temperature conditions do not match with basic diode characteristic due to self-heating effect.

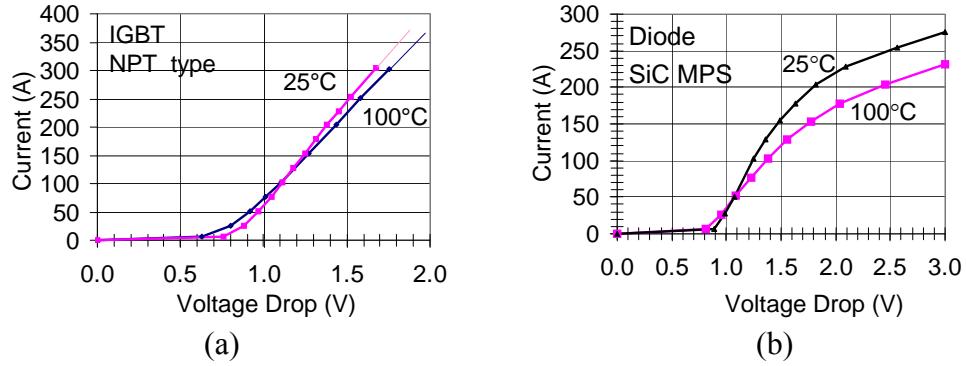


Figure 3.14. NPT IGBT and SiC Schottky diode conduction voltage drop under different temperature conditions.

3.5. Switching Loss Measurement Results

Figure 3.15 shows measured voltage and current waveforms at 300-V, 300-A condition. The switching energy is obtained from the integration of the product of voltage and current. In this case, the turn-on energy is 6.39 mJ, and turn-off energy is 11.93 mJ. The diode reverse recovery energy can be obtained from integration of the product of diode voltage and current. In this case it is 1.24 mJ. Based on the V_{ce} drop during the current rise period, the parasitic inductance that includes the dc bus capacitor, bus bar, bushing, and internal device wire bonds altogether is estimated about 60 μ H. Figure 3.16 shows measured voltage and current waveforms at 300-V, 400-A condition. The turn-on energy is increased to 8.31 mJ, and the turn-off energy is increased to 15.77 mJ.

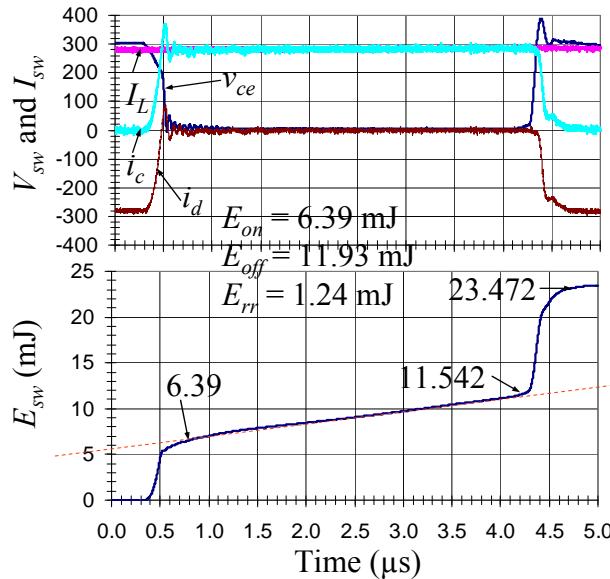


Figure 3.15. Hard switching voltage and current switching measurement results at 300-A, 25°C condition.

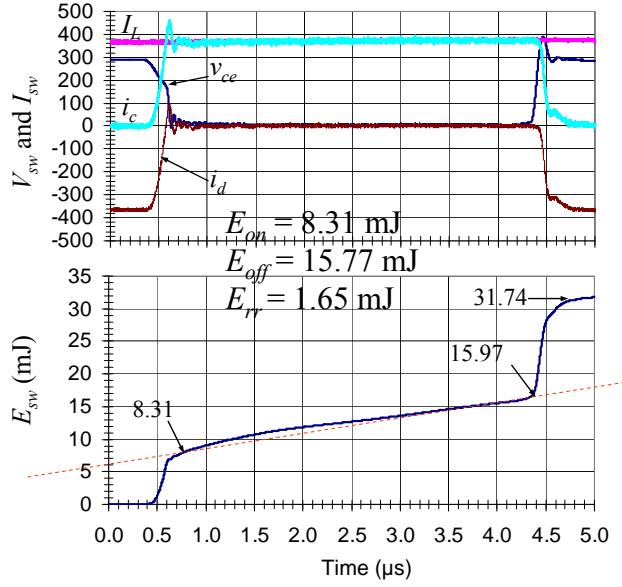


Figure 3.16. Hard switching voltage and current switching measurement results at 400-A, 25°C condition.

Figures 3.17 and 3.18 repeat the measured voltage and current waveforms at 300-V, 300-A and 400-A conditions with 100°C coolant. The switching energy is obtained from the integration of the product of voltage and current. In this case, the turn-on energy is 9.89 mJ under 300-A condition and 15.33 mJ under 400 A condition. The turn-off energy is 18.1 mJ under 300-A condition and 25.6 mJ under 400-A condition.

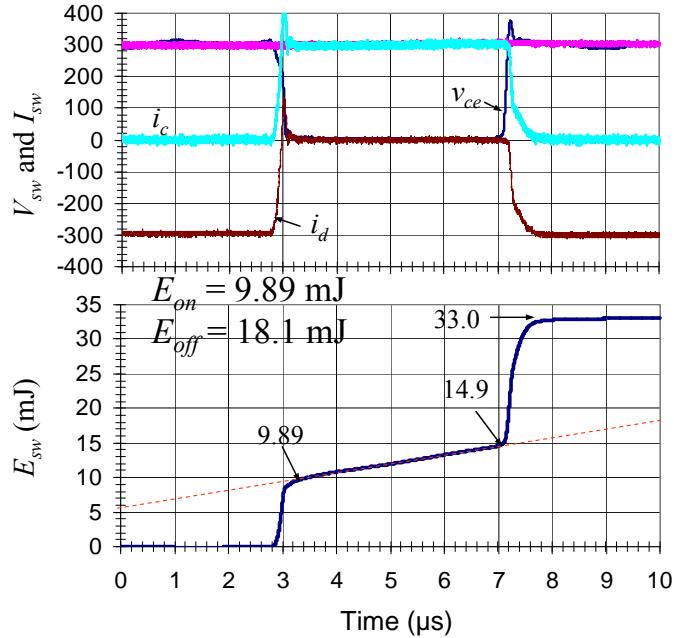


Figure 3.17. Switching voltage and current waveforms under 300-V, 300-A at 100°C

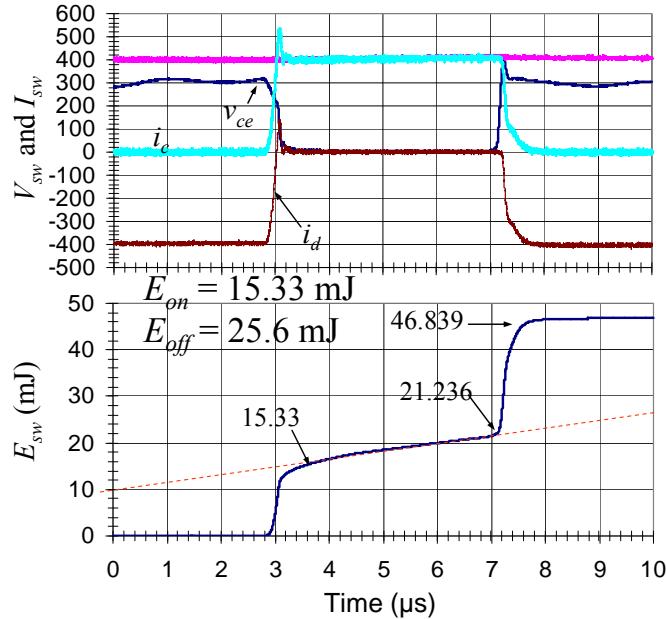


Figure 3.18. Switching voltage and current waveforms under 300-V, 400-A at 100°C.

Figures 3.19 and 3.20 show detailed voltage and current switching waveforms during turn-on and turn-off at 300-A and 400-A respectively. The waveforms also compare voltage, current, and switching energy between 100°C and 25°C conditions. The turn-on and -off speeds are slower at high temperature conditions, and thus their high-temperature switching energies are increased significantly on both 300-A and 400-A cases. Approximately, the switching loss is increased by 40% from 25°C to 100°C.

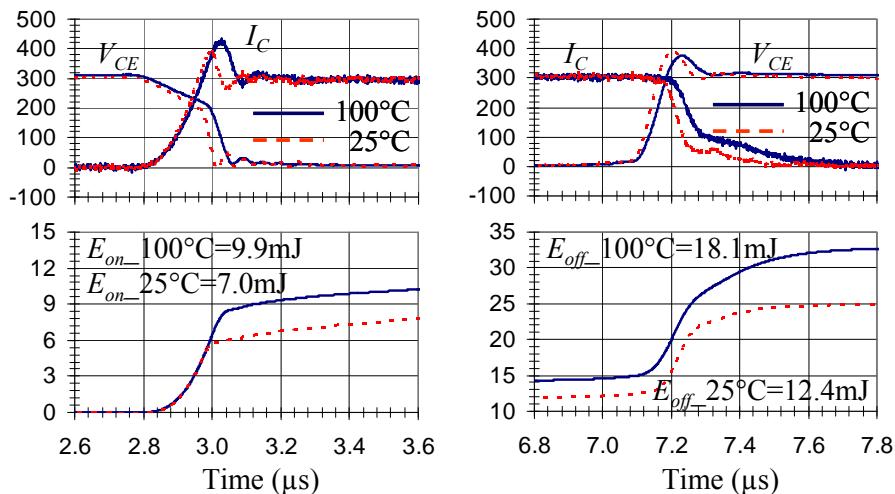


Figure 3.19. IGBT turn-on voltage and current waveforms comparison between 25°C and 100°C under 300-V, 300-A switching.

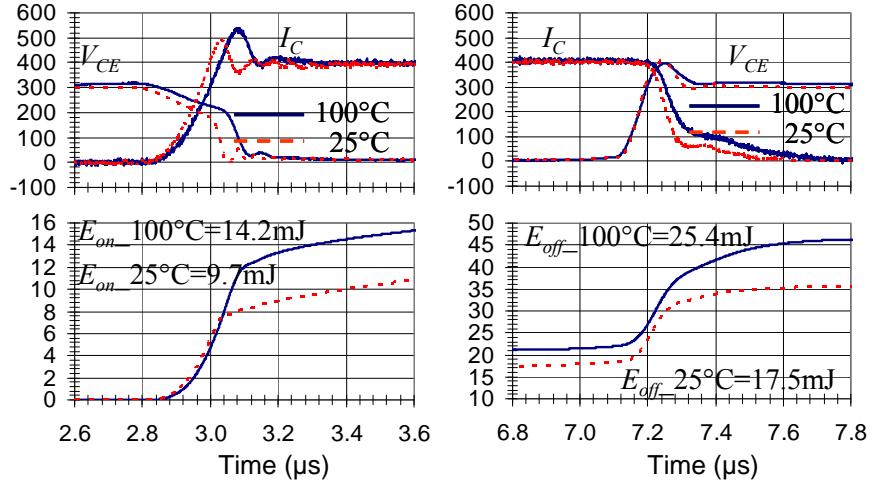


Figure 3.20. IGBT turn-on voltage and current waveforms comparison between 25°C and 100°C under 300-V, 400-A switching.

Figures 3.21 and 3.22 show soft-switching operation under 25°C , 300-V, 150-A and 230-A conditions, respectively. Unlike hard-switching condition, the device voltage V_{CE} drops to zero before the gate signal V_{GE} is turned on, or device current I_C is conducting. The device current tends to oscillate after turn-on because of the parasitic ringing. During turn-off, the device voltage oscillates due to added current sensing elements. The turn-off overlapping period between device current and voltage is significantly reduced, thus the turn-off loss should also be reduced.

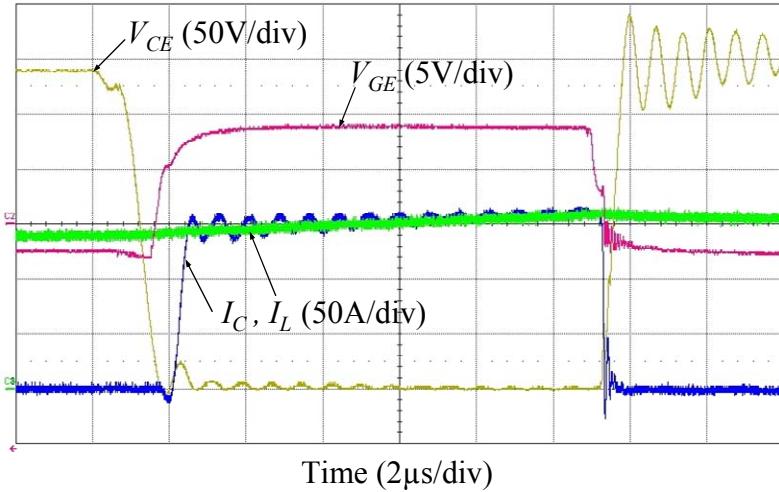


Figure 3.21. Soft-switching voltage and current waveforms under 300-V, 150-A, 25°C test condition.

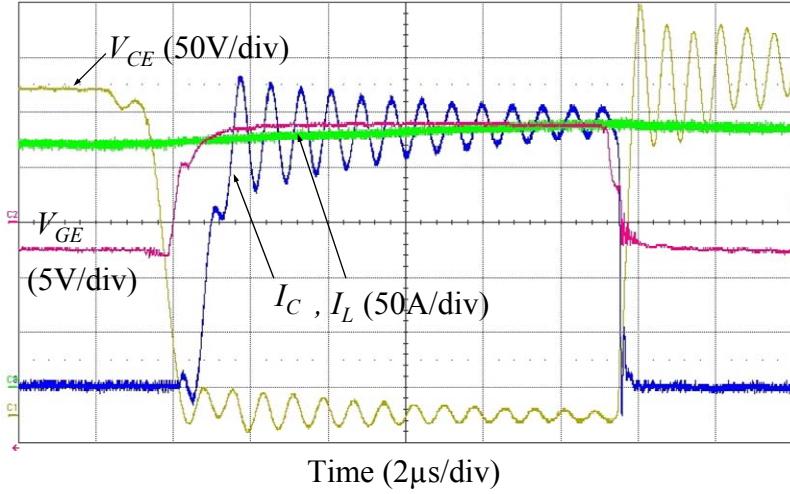


Figure 3.22. Soft-switching voltage and current waveforms under 300-V, 230-A, 25°C test condition.

Figures 3.23, 3.24, and 3.25 show soft-switching operation at 100°C, 300-V, 100-A, 200-A, and 300-A conditions, respectively. The ringing of device voltage and current seems to be reduced, possibly due to a reduction in parasitic path. In this test, a new smaller Rogowski coil is used, which allow cutting down the parasitic inductance in the measurement loop. The resonant current I_{Lr} is not much larger than the device current because of the use of variable timing control, with which the resonant current adapts to load current, so the auxiliary circuit can minimize the resonant peak current requirement. This variable timing should allow efficiency improvement in light loads.

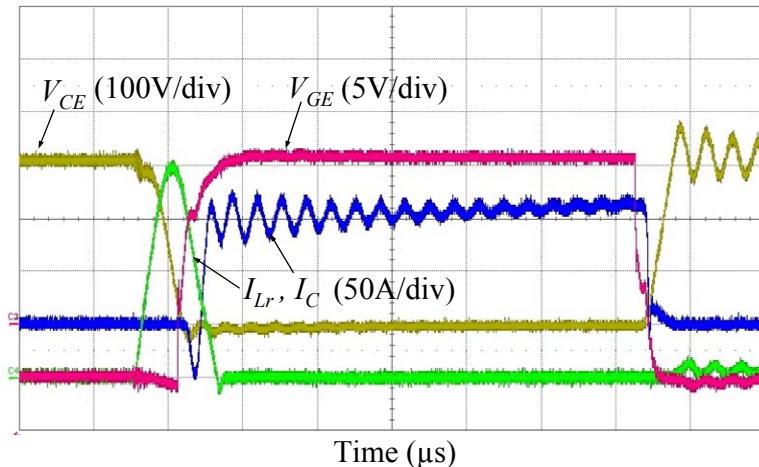


Figure 3.23. Soft-switching voltage and current waveforms under 300-V, 100-A, 100°C test condition.

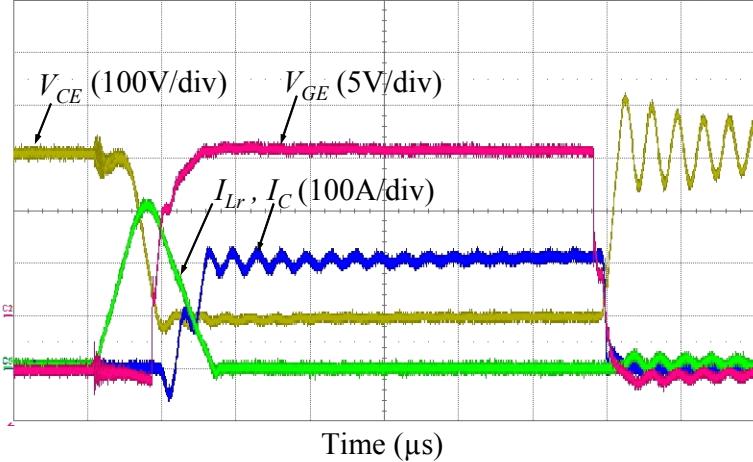


Figure 3.24. Soft-switching voltage and current waveforms under 300-V, 200-A, 100°C test condition.

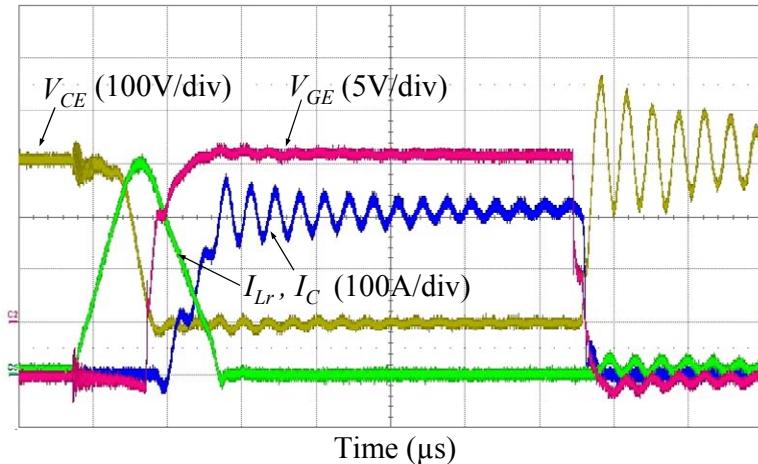


Figure 3.25. Soft-switching voltage and current waveforms under 300-V, 300-A, 100°C test condition.

Figures 3.26 and 3.27 show detailed voltage and current waveforms at 25°C and 100°C and at different current conditions. The stored waveforms are used for switching energy calculation. It was found that the turn-on energy is practically zero, but the turn-off energy remains visible due to increased tail bump, even though the overlap between device voltage and current is much reduced.

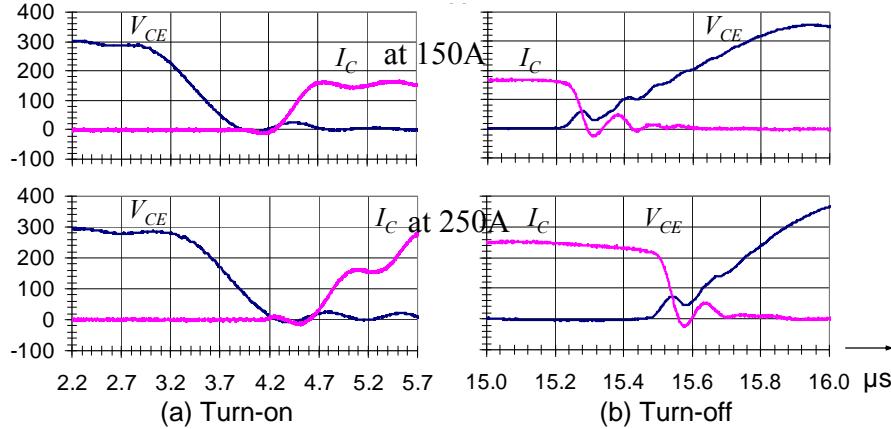


Figure 3.26. Soft-switching voltage and current waveforms at 25°C and at different current conditions: (a) turn-on, and (b) turn-off.

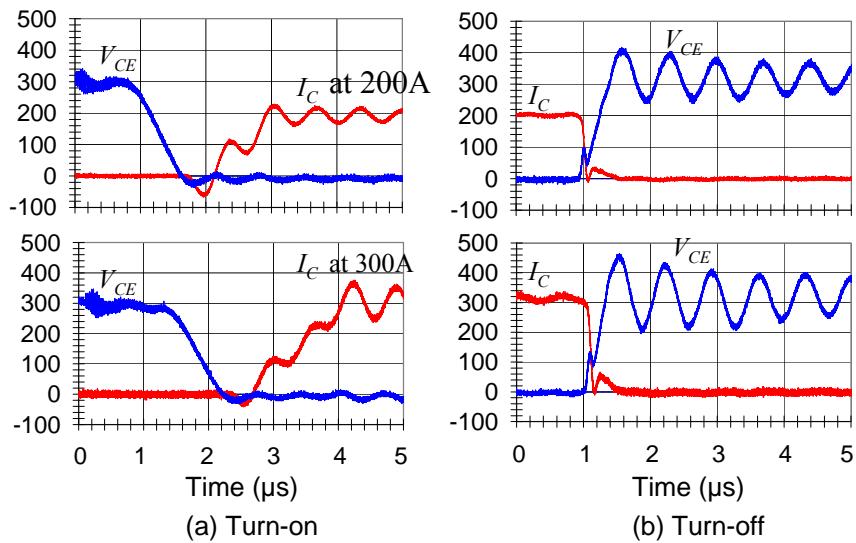


Figure 3.27. Soft-switching voltage and current waveforms at 100°C and at different current conditions: (a) turn-on, and (b) turn-off.

The parasitic ringing is expected to be eliminated with fully integrated module as the evidence of improvement by a smaller current sensor. The tail current induced turn-off loss, as compared to the hard-switching counterpart, is much reduced. Figure 3.28 compares the switching energy under hard- and soft-switching and different temperature conditions. The turn-on loss under soft switching can be considered zero. A small number shown in the plot is due to measurement error or parasitic loss. Under high-temperature hard-switching condition, the device switching losses increases substantially. As a rule of thumb, 40 to 50 percent switching loss increase is observed for the temperature increased from 25°C to 100°C . Under soft-switching condition, however, the turn-on loss remains zero at 100°C . The turn-off loss, as compared to hard-switching case, is reduced by 72%. In NPT devices, this high-temperature turn-off loss reduction is normally within 30%, but the LPT devices apparently demonstrate another advantage that was not obvious from device internal characteristics. The main reason is the resonant capacitor tends to modulate

the turn-off behavior, and thus the NPT device cannot take advantage of relatively low turn-off loss under high-temperature hard-switching condition.

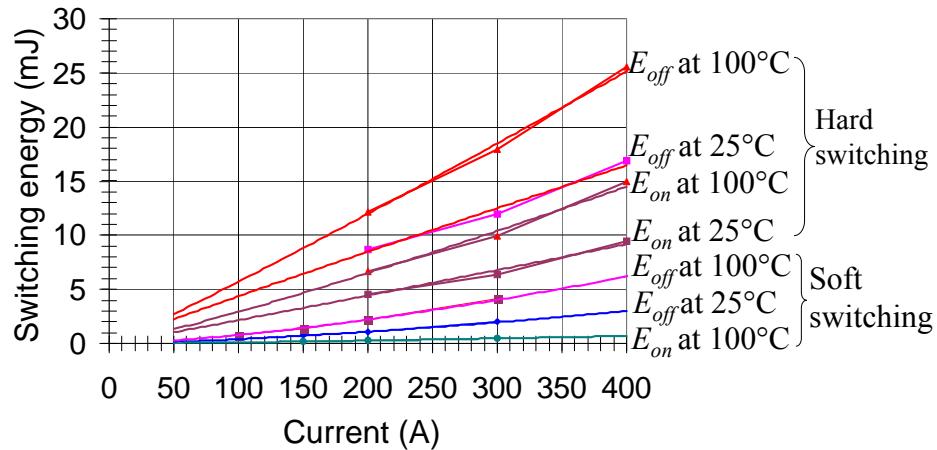


Figure 3.28. Measured switching energy under hard- and soft-switching and at different temperature conditions.

Using the above conduction and switching loss information, the entire inverter loss can be calculated, and the efficiency can be projected, as shown in Figure 3.29. The soft switching inverter maintains above 98.5% up to 30% power and higher than 97.5% at full load. The hard-switching inverter efficiency is slightly higher than 97% for the most power level and drops below 97% at the full load.

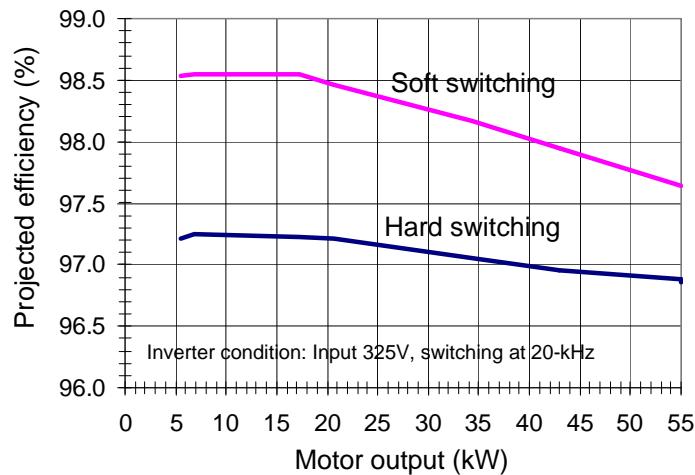


Figure 3.29. Efficiency projection based on the measured device loss calculation.

4. SOFT-SWITCHING POWER MODULE DEVELOPMENT

4.1. Soft-Switching Module Configuration

The purpose of the soft-switching power module development performed by Powerex was to develop a high performance, low-loss, thermally efficient, reliable and cost-effective, soft-switching IGBT module for the 55kW vehicle inverter. The module design and semiconductor device selection along with the soft-switching architecture were all critical to achieving the low losses required to ensure inverter efficiencies >98% over wide operating ranges. Another critical goal of the program was to develop a module that could be either air-cooled or liquid-cooled with the primary vehicle coolant loop while keeping the maximum power semiconductor junction temperatures below 125°C with inlet coolant temperatures rising as high as 105°C.

The strategy to achieve the inverter efficiency and primary coolant loop compatibility goals was to utilize resonant soft-switching of the power switches to minimize losses incurred during the switching, primarily the turn-on, transients. A complementary novel strategy utilizing a parallel combination of IGBTs and MOSFETs in the power switch also served to reduce losses at lower current output levels compared to using IGBTs only. The schematic of the power module is shown in Figure 4.1. The IGBT (Q_1), MOSFET (M_1) and antiparallel diode (D_1) constitute the upper power switch, while Q_2 , M_2 and D_2 form the lower switch of the half H-bridge circuit used in the inverter. Three modules make up the 3-Phase inverter power circuit. The resonant switching is effected by the auxiliary circuit comprised of Q_{x1} , D_{x1} , D_{x3} , D_{x6} , Q_{x2} , D_{x2} , D_{x4} and D_{x5} . The capacitors and inductors required for the resonant soft-switching are located external to the module. The resonant switching method and results are discussed elsewhere in this report.

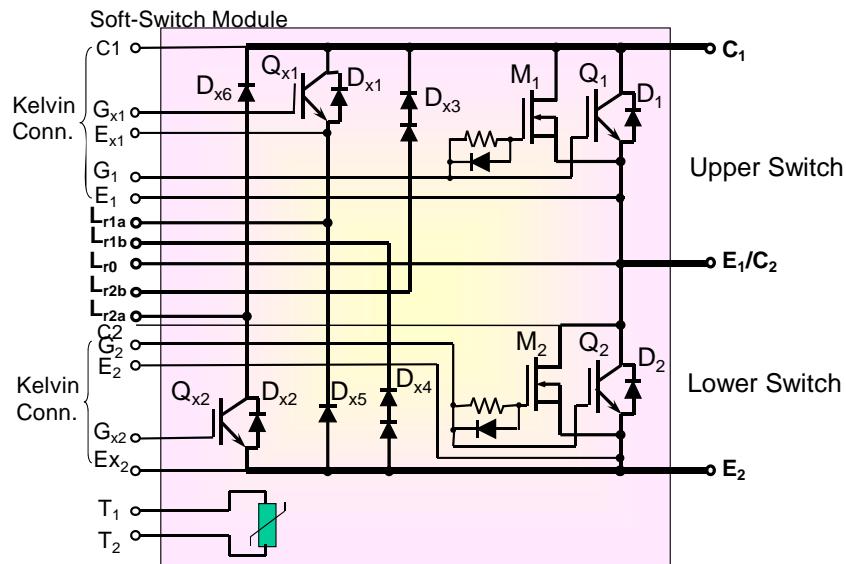


Figure 4.1. Basic circuit configuration for a single phase, soft switched IGBT module.

The parallel combination of the IGBTs and MOSFETs effectively reduces the conduction losses at low current levels, since the unipolar MOSFET acts as a resistor with a voltage drop below

that of the built-in junction drop of the bipolar IGBT. At higher current levels where the resistance of the MOSFET exhibits higher voltage drops, the majority of the current flow is transferred to the IGBT, which has a lower effective on-resistance. Also included in the module is a resistive temperature detector (RTD) to monitor the operating junction temperature of the IGBTs and MOSFETs.

The three generations of power modules are shown in Figure 4.2. The first generation (Gen-1) was designed to be directly liquid-cooled by means of a built-in chill plate. At the onset of the program, we were uncertain of the power dissipation levels that would occur in the module and thus designed the module to have as low a thermal resistance from junction to liquid as possible. Subsequent power dissipation and efficiency measurements in the Gen-1 inverter tests confirmed that the power semiconductor losses were low enough that the module could be either air-cooled or liquid-cooled without the need for a built-in chill plate. The design details and performance of the Gen-1 module will be discussed in subsequent sections. Drawbacks of the Gen-1 design were a high internal inductance, difficulty of assembly and a high profile which made integrating it with the other power components in the inverter and the control boards difficult.

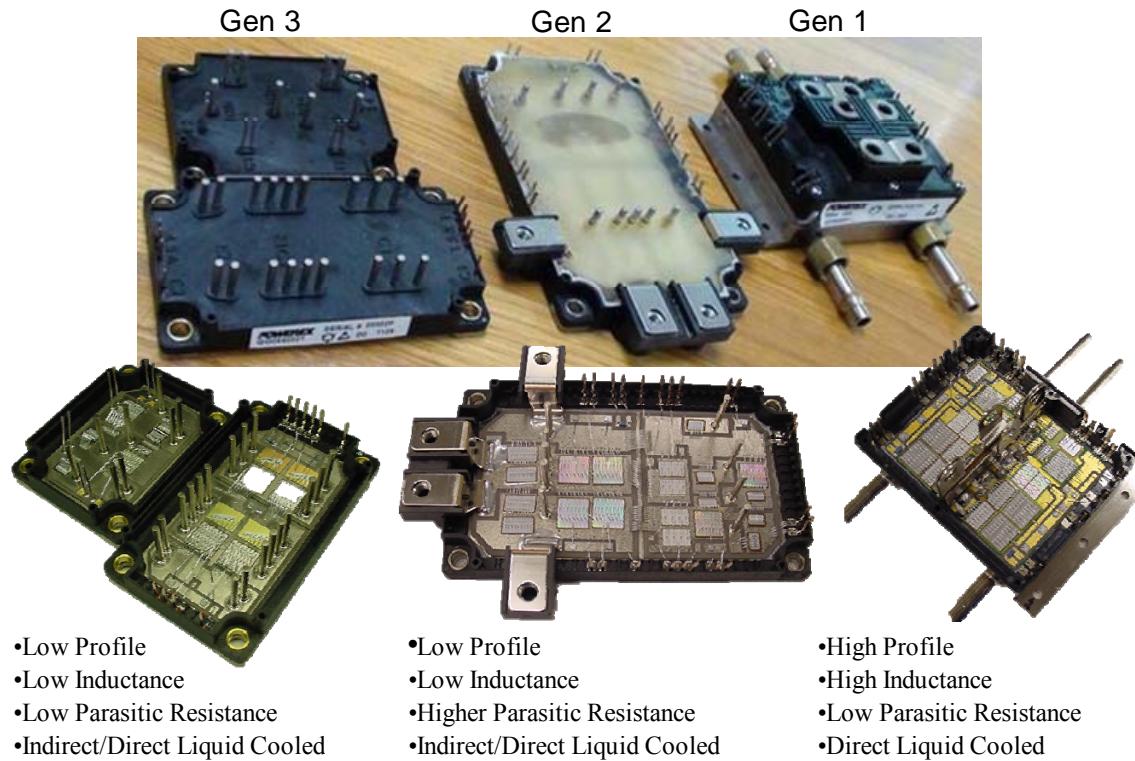


Figure 4.2. Photos showing the evolution of the three generations of power modules along with their significant characteristics.

The second generation module, as shown in Figure 4.2, was designed to have a low profile to dramatically reduce the internal and external inductances while facilitating mating to the power and control printed circuit boards (PCBs) mounted directly on top of it. Even though the modules that were supplied utilized a flat baseplate for mounting on a conventional liquid-cooled chill plate or air-cooled heatsink, they could also have been assembled with a built-in liquid chill plate similar to the Gen-1 design. The Gen-2 module did dramatically reduce the parasitic

inductance in the Gen-2 inverter. However, one disadvantage of the low-profile layout was an increase in the internal parasitic resistance of the module. This was due to the longer distances the current had to travel laterally in the thin layer (0.012" thick) of copper bonded to the top of the aluminum-nitride (AlN) insulator to flow from one power terminal through the IGBT/MOSFET chips and out to the other power terminal. This parasitic resistance effectively increased the conduction losses of the module and resulted in a drop in overall efficiency of the Gen-2 inverter compared to that of Gen-1.

The Gen-3 design was focused on reducing the internal parasitic resistance and inductance, as well as replacing both the existing MOSFET and antiparallel diode with a new, lower on-drop resistance (R_{ds-on}) Mosfet with an improved internal body diode capable of handling the free-wheeling currents. The large, single module was also split into two separate modules to decrease the size of the AlN substrates, which will improve thermal cycling reliability. One module consists of the power stage (half H-bridge) and the other the auxiliary resonant-switching section. As discussed later, the Gen-3 module exhibited lower conduction losses and inductance than both Gen-1 and Gen-2 designs. The Gen-3 module utilizes a flat baseplate like Gen-2, but is capable of being assembled on a built-in liquid chill plate similar to Gen-1. The Gen-3 inverter exhibited such low losses/high efficiency that air cooling was utilized.

4.2. Gen-1 Module Development

A. Gen-1 Module Design

The design for the Gen-1, single phase-leg, soft-switched IGBT module will be discussed in this section. The basic circuit configuration for the module is shown in Figure 4.1. Circuit simulations performed by Virginia Tech provided the average and peak currents for each device in the module and also the power terminals. The modeling also provided the power dissipation for each device, facilitating the selection of the individual semiconductors and determination of the number of paralleled chips. The module requirements based on the results of the circuit simulations are tabulated in Table 4.1.

Table 4.1. Single Phase, Soft-Switched Gen-1 IGBT Module Requirements

Module Section	Device Number	Peak Current/Switch (A)	RMS Current/Switch (A)	Total Avg Power Loss/Switch (W)	Number of Chips/Switch	Total Avg Power Loss/Chip (W)	Peak Current/Chip (A)	RMS Current/Chip (A)
Main Switch	Q1, Q2	340	108	232	2	116	170	54
	D1, D2	290	55	116	2	58	145	28
	M1, M2	50	34	72	2	36	25	17
Auxiliary	Qx1, Qx2	240	21	18	1	18	240	21
Switch	Dx1, Dx2	10	1	0.5	1	0.5	10	1
Re-Setting Diode	Dx3, Dx4	160	14	6.5	1	6.5	160	14
Main Switch Terminals	C1 & E2	400	280					
	E1/C2 (Common)	400	280					
Auxiliary Terminals	Lr1	240	21					
	Lr0	400	35					
	Lr2	240	21					

The power dissipation and peak current requirements drive the IGBT and diode chip selection and quantities of chips to parallel. The peak currents drive the size of the terminals and number of wirebonds per chip. The RMS currents drive the terminal size and internal conductor pad sizes. Table 4.2 lists the chip selections and estimated maximum chip temperatures above the incoming coolant temperature. The IGBT and diode chips selected for the module are the latest generation Mitsubishi/Powerex Carrier Storage Trench-Gate Bipolar Transistor (CSTBT) IGBT's and accompanying fast, soft-recovery diodes. The parallel MOSFETs are Infineon IPW60R045CP Cool MOS chips.

Table 4.2. Estimated Power Dissipation & Maximum Chip Temperatures

Module Section	Device Number	Chip Rating	Chip Size (L x W) (mm)	Chip Area (cm ²)	Number of Chips Used	Total Avg Power Loss/Chip (W)	Total Avg Power Density/Chip (W/cm ²)	Estimated Module Thermal Resistivity Junc - Liq (C·cm ² /W)	Delta Temp Junc - Liq (C)
Main Switch	Q1, Q2	IGBT 200A, 600V	12.0 x 12.0	1.44	2	116	40.3	0.40	16.1
	D1, D2	FWD 600V, 200A	7.1 x 12.0	0.85	2	58	34.0	0.40	13.6
	M1, M2	MOSFET 650V, 60A	6.0 x 9.5	0.57	2	36	31.6	0.40	12.6
Auxiliary	Qx1, Qx2	IGBT 150A, 600V	10.5 x 11.0	1.16	1	18	15.6	0.40	6.2
Switch	Dx1, Dx2	FWD 600V, 75A	4.1x7.8	0.32	1	0.5	1.6	0.40	0.6
Re-Setting Diode	Dx3, Dx4	FWD 1200V, 100A	6.8 x 12.0	0.82	1	6.5	7.9	0.40	3.2

Each IGBT has its own dedicated internal series gate resistor (not shown in Figure 4.1) to ensure sharing of the gate pulse amongst paralleled devices. The IGBTs also have dedicated emitter potential return leads for low internal inductance gate loops and also to prevent gate voltage shifts caused by the emitter currents as the IGBT switches on and off. Also shown in the schematic in Figure 4.1 is an internal temperature sensor mounted as close to possible to both Q_1 and Q_2 for over-temperature sensing & shut down protection. Adequate dielectric insulation is an important consideration for components in electrical systems, particularly HEV automotive inverters. Dielectric insulation internal to the module is provided by silicone rubber gels and potting compounds. These materials, which are used extensively in the power module industry, are effective and stable insulators, even in the presence of ambient laden with moisture. Design rules established by Powerex for internal and external conductor spacing in 600V modules were followed.

The single phase-leg module design is shown in Figure 4.3. The height of the main power terminals (+/- DC Link & AC Output) are at the same height as the main DC Link capacitors, permitting the use of a flat, low-inductance, laminated bus to connect the three modules to the capacitors. The module has a pin-fin baseplate that is mounted to a liquid cooled manifold for thermal management of the semiconductor chips.

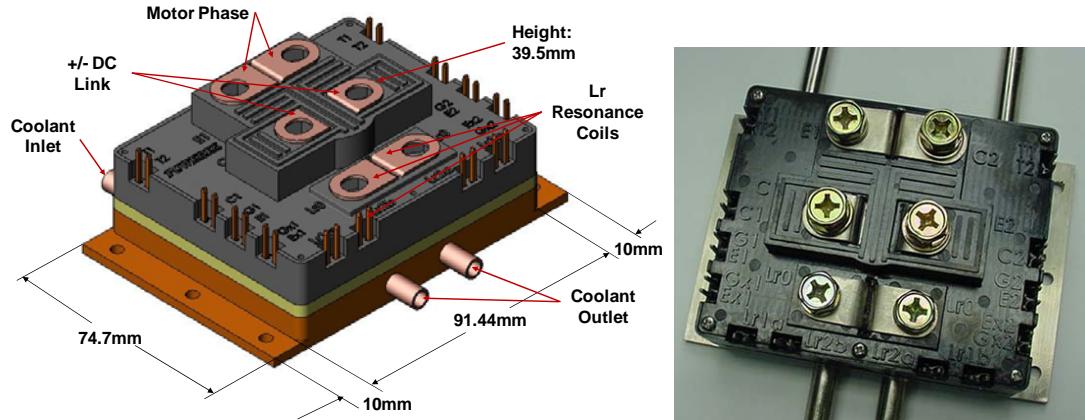


Figure 4.3. Overall view of the Phase 1, single phase, IGBT module.

The internal chip, wirebond and terminal layout is shown in Figure 4.4. The chips are soldered to a 0.025 inch thick aluminum nitride (AlN) ceramic substrate that is clad with direct bond copper (DBCu) layers 0.012 inch thick. Most power modules use DBC AlN as the insulating ceramic due to its relatively high thermal conductivity (170W/mK). This is important since the AlN is in the heat flow path from the chip to the coolant, as shown in Figure 4.5. The DBC AlN substrate is then soldered to the baseplate, which is flat on the top surface and has pin fins protruding from the bottom surface for efficient liquid cooling, as shown in Figure 4.6. The upper (Q_1 & Q_{x1}) and lower (Q_2 & Q_{x2}) switches are on two separate AlN substrates to minimize stress during temperature cycling due to mismatches in the expansion and contraction rates of the ceramic and baseplate materials. Copper was used for the pin-fin baseplate due to its high thermal conductivity.

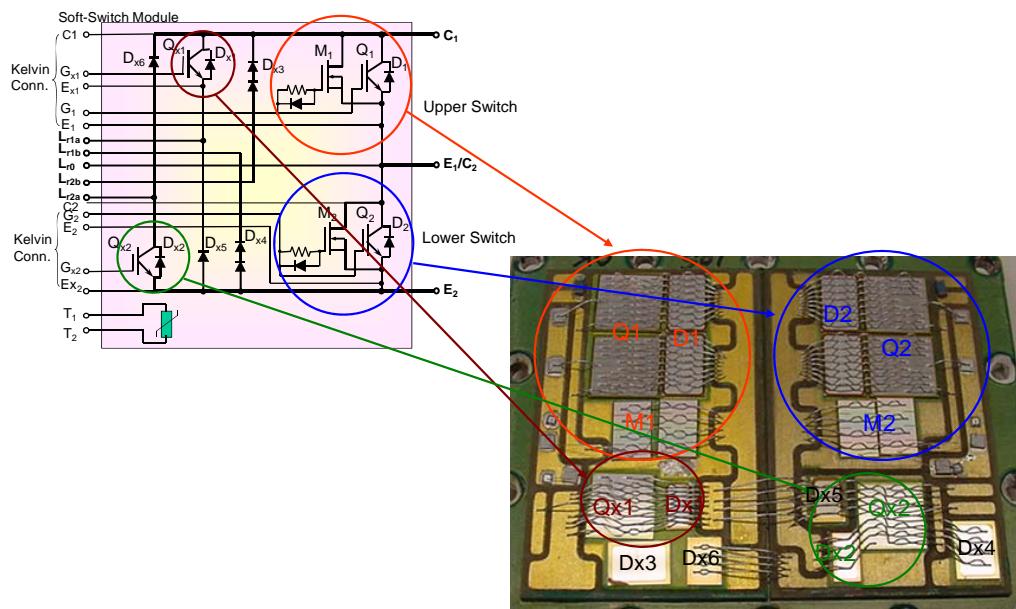


Figure 4.4. Internal chip and wirebond layout for Gen 1 module.

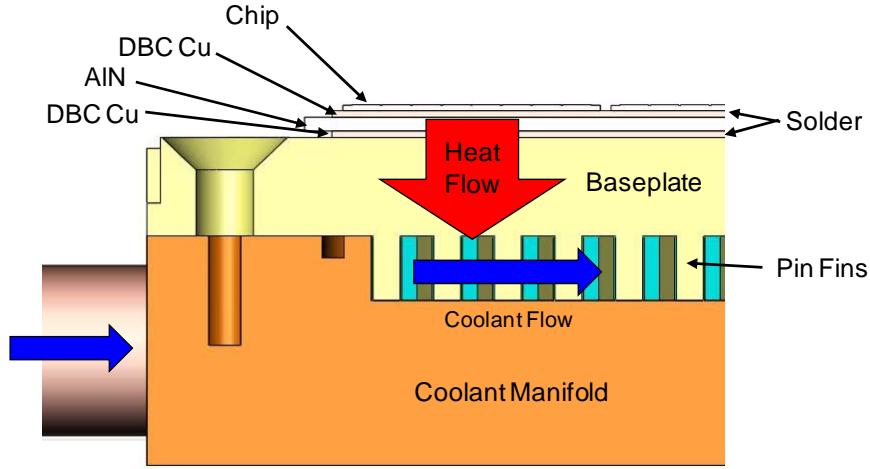


Figure 4.5. Cross section of Gen 1 module showing heat flow path and layers.

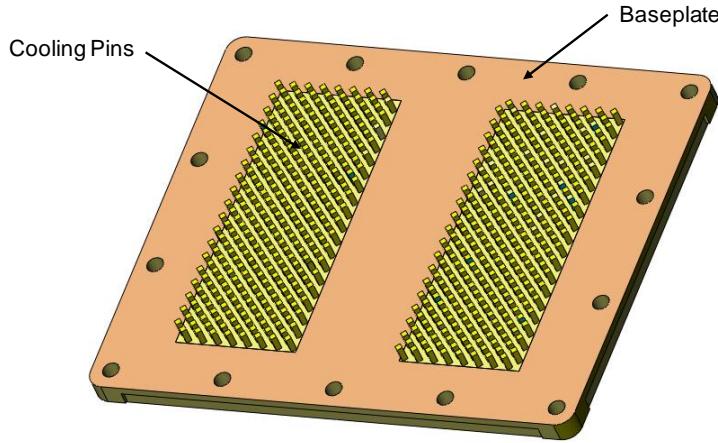


Figure 4.6. Bottom view of module baseplate showing pin-fins for liquid cooling.

B. Gen-1 Module Thermal Simulations

The hybrid vehicle thermal management requirements present a significant challenge for the power module designer. The peak coolant inlet temperature of 105°C, coupled with the desire to keep the maximum junction temperatures below 125°C for good device reliability, dictates a maximum temperature drop from junction to coolant of only 20°C. This low ΔT , along with relatively low coolant flow rates of 5 GPM total for all three modules in the 3-Phase system (1.67 GPM/module or 0.8 GPM/switch), require a low thermal resistance path from the chip to the liquid. In addition, the chips must be sized to minimize power dissipation. Fortunately, the resonant-switching circuit topology used in the inverter for this program minimizes overall power dissipation by virtually eliminating IGBT switching losses.

The temperature gradient from junction to the liquid was modeled using a two-step technique. A 3-dimensional finite element (FEA) model was used to model the temperature gradient from

the junctions of the semiconductor devices to the pin fin cooling surfaces on the bottom of the baseplate. In this simulation, the average power dissipation for each chip listed in Table 4.2 was used. In the second step, the temperature drop from the pin fins to the coolant was scaled from measurements made on similar, but smaller, pin-fin test baseplates fabricated for thermal resistance measurements. The estimated ΔT from pin-fins to coolant was then added to the theoretical drop from junction to pin-fin. The results of the FEA model from junction to pin-fin are shown in Figure 4.7. The total estimated ΔT from junction to coolant is listed in Table 4.2 for each chip. As is evident from Table 4.2, the estimated ΔT is lower than the 20°C objective.

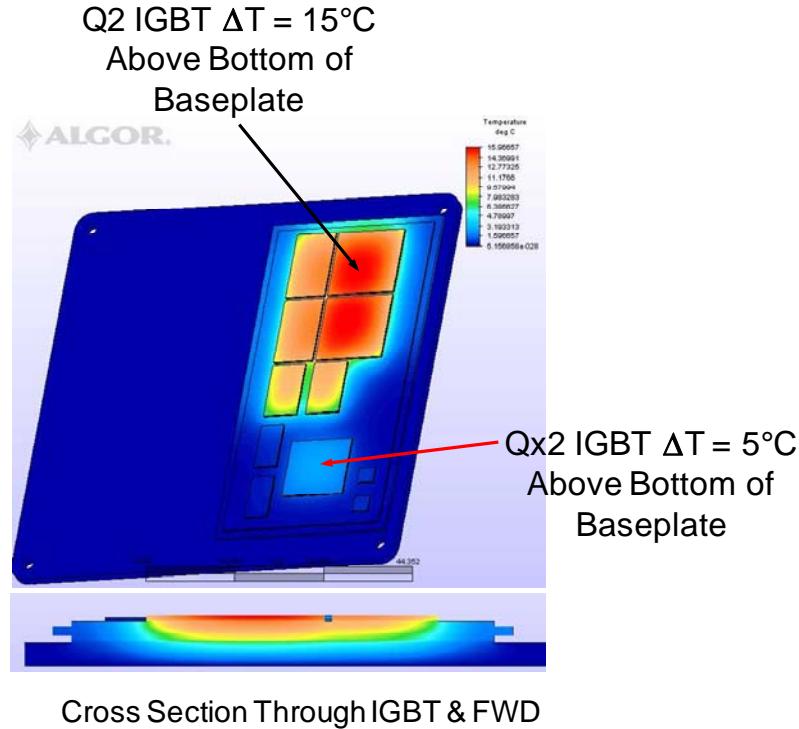


Figure 4.7. Results of FEA simulations of temperature drop from junctions to pin-fins.

C. Gen-1 Module Conduction Characteristics Test Results

Test data from a sample of the Gen-1 modules delivered to Virginia Tech are listed in Table 4.3. Parametric electrical measurements were performed at 25 and 125°C. Average device voltage drop (V_{cesat}) values for Q_1/M_1 , Q_2/M_2 , Q_{x1} and Q_{x2} for Gen 1 modules SN 101 and 102 are plotted versus current in Figure 4.8. The resistive slope of the MOSFET carrying most of the current at levels below 50A is apparent in Figure 4.8, revealing the savings in conduction losses compared to using IGBTs only. The average voltage drops of the diodes (V_f 's) in SN 101 and SN 102 are plotted versus current in Figure 4.9.

Table 4.3. Test Results for a sample of the Gen 1 Modules

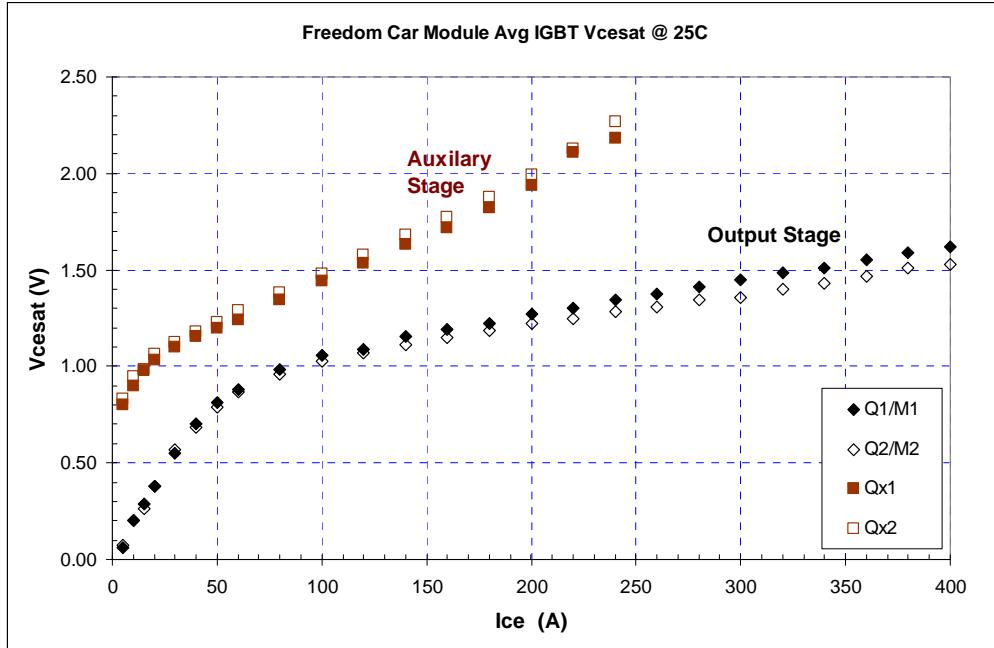


Figure 4.8. Average V_{ce-sat} of the IGBT stages at 25°C for Gen-1 modules SN101 & SN102. The effect of the parallel MOSFET at low current levels is evident in the Output Stage V_{ce-sat} curves.

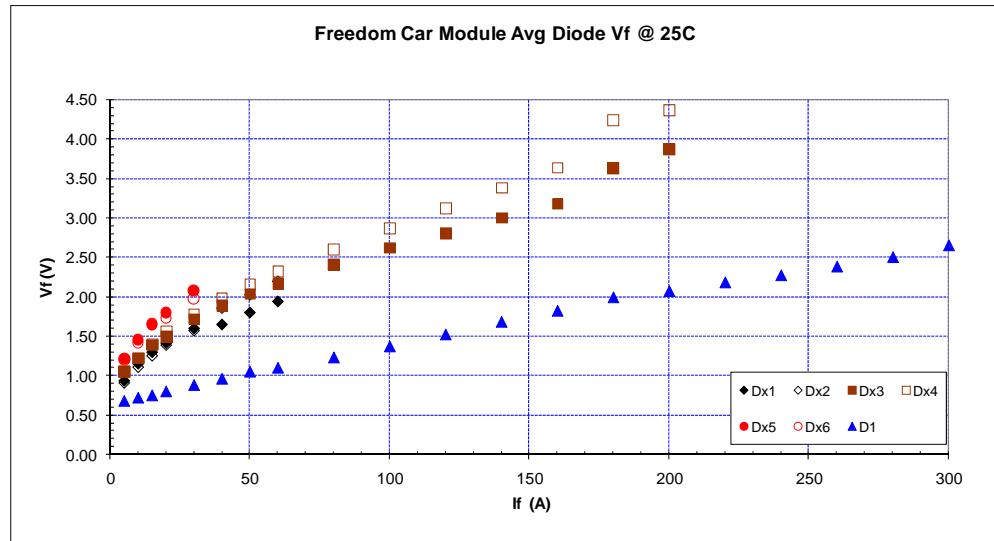


Figure 4.9. Average V_f of the diodes at 25°C for Gen-1 modules SN101 & SN102.

The thermal resistance of the first generation module was measured to determine the performance of the integrated liquid-cooled chill plate. The results discussed in this report are for pure water and a 50/50 water/ethylene-glycol (EGC) mix. The technique used for measuring the thermal resistance was as follows:

1. The V_{cesat} 's of the IGBTs and V_f 's of the diodes were measured at several different pulsed current levels (low duty cycle) at temperatures of 25, 75, 100 & 125°C.

2. Junction temperature vs V_{cesat}/V_f curves at a given current were generated from the parametric data taken in step 1.
3. The module was then connected to a liquid to air heat exchanger system and the coolant was flowed through one switch of the module. Liquid flow rate, inlet/outlet liquid temperature and inlet/outlet liquid pressure were measured. The flow rates were varied from 0.3 to 1.0 liters/minute.
4. Each chip set (Q_1M_1 , D_1 , Q_{x1} , D_{x1} , D_{x3} , and D_{x6}) was powered individually at DC currents matching one or more of the current levels measured in step 1. The V_{cesat} or V_f of each powered chip set was measured.
5. The junction temperature of each chip set was determined using the V_{cesat} or V_f value and the calibration curve for the current used.
6. Chip sets Q_1M_1 , Q_{x1} and D_{x3} were then powered simultaneously with 125, 20 and 20A DC, respectively, to simulate operation under average current conditions. The DC current levels were selected based on the RMS current values from the Virginia Tech inverter simulations.

Individual chip sets were powered to determine the thermal resistance of each chip set without the influence of heating by other chip sets, in order to validate a simple 2-D thermal model. Of course, this is not the way the module actually operates in the inverter, so as many chip sets as possible were subsequently powered simultaneously at their respective average/RMS current levels to determine the true thermal resistance. In these measurements, Q_1M_1 (main switch), Q_{x1} (auxiliary switch) and D_{x3} (re-setting diode) were powered. Since the average current through D_{x6} is normally very low (according to the simulations), it was not powered during these measurements. The coolant flow path of the integrated chill plate is shown in Figure 4.10.

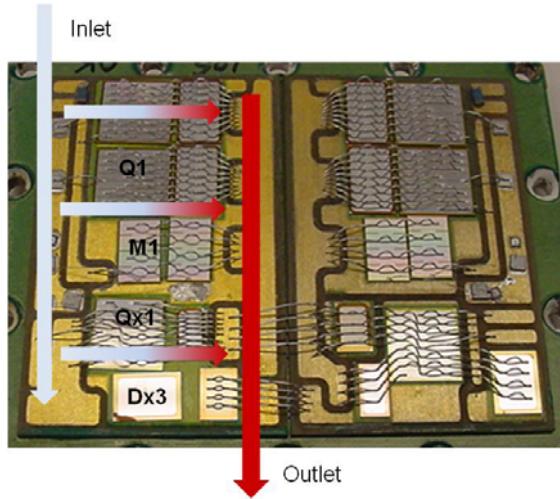


Figure 4.10. Gen 1 module coolant flow.

The experimental results for the Q_1M_1 chip set measurements are listed in Table 4.4 at 125 and 200A for both coolant types. For the Q_1M_1 chip set, the thermal resistance decreases with increasing liquid flow rate, as expected. The working flow rate for each switch in the 3-phase inverter will be 0.4 gallons/min, i.e. 2.5 gpm divided by 6 switches. The maximum flow rate

used in these measurements was 0.26 gpm, which is well below the 0.4 gpm available. Also, the measured thermal resistance of the EGC mixture is higher than pure water, which is also expected.

Table 4.4. Gen-1 module fully powered Q_1M_1 chip set thermal resistance results for pure water & EGC mixtures

Junction - Inlet Liquid Thermal Results For Q1M1 With H₂O Coolant

			Q1M1 (Ic = 125A)			Q1M1 (Ic = 200A)		
Flow Rate (Gal/min)	Flow Rate (L/min)	Pressure Drop (psi)	Power Dissipation (W)	Delta Temperature Junc - Inlet (°C)	R _{th} junc-inlet (C/W)	Power Dissipation (W)	Delta Temperature Junc - Inlet (°C)	R _{th} junc-inlet (C/W)
0.08	0.3	0.2	129.0	8.6	0.067	231.5	26.1	0.113
0.10	0.4	0.3	129.3	7.3	0.056	232.0	20.2	0.087
0.13	0.5	0.5	129.5	5.8	0.045	232.4	14.6	0.063
0.16	0.6	0.7	129.6	5.8	0.045	232.6	12.0	0.052
0.21	0.8	0.8	129.6	5.5	0.042	233.0	6.4	0.027
0.26	1.0	1.1	129.9	4.4	0.034	233.2	3.8	0.016

Junction - Inlet Liquid Thermal Results For Q1M1 With 50 EGC / 50 H₂O Coolant

			Q1M1 (Ic = 125A)			Q1M1 (Ic = 200A)		
Flow Rate (Gal/min)	Flow Rate (L/min)	Pressure Drop (psi)	Power Dissipation (W)	Delta Temperature Junc - Inlet (°C)	R _{th} junc-inlet (C/W)	Power Dissipation (W)	Delta Temperature Junc - Inlet (°C)	R _{th} junc-inlet (C/W)
0.08	0.3	0.3	127.6	19.7	0.154	227.3	56.7	0.249
0.10	0.4	0.4	127.9	17.8	0.139	228.0	54.0	0.237
0.13	0.5	0.5	128.0	16.8	0.131	228.4	52.8	0.231
0.16	0.6	0.6	128.1	16.1	0.126	228.8	51.7	0.223
0.21	0.8	0.8	128.4	14.8	0.115	229.4	50.5	0.220
0.26	1.0	1.1	128.5	14.1	0.110	229.6	50.3	0.219

The results listed in Table 4.4 for the higher flow rates of the pure water coolant indicate lower thermal resistances for currents of 200A compared to 125A. The reason for this is unclear at this time. One of the issues with the V_{cesat} vs junction temperature method used in these measurements is that the V_{cesat} of an IGBT does not vary linearly with temperature. In this case, the rate at which the V_{cesat} decreases is very slow at temperatures from 25 to 60°C. The V_{cesat} decreases more rapidly with temperature above 60°C. As a result, at the lower junction temperatures obtained with higher coolant flows, there is more error in determining the actual junction temperature using the V_{cesat} method, which introduces error in the junction – coolant temperature drop and ultimately the calculated thermal resistances. However, the junction – coolant temperature drops are still less than 20C, even at the low flow rates with the greater accuracy. This will permit the semiconductors in the module to operate below 125C with coolant temperatures up to 105°C.

The results of the fully powered thermal tests are listed in Table 4.5. As expected, the thermal resistance is slightly higher than the case in Table 4.4 where only Q_1M_1 is powered, due to the effects of the simultaneous heat generation of the other chip sets. The temperature drop from

junction to inlet coolant is well below 20°C at 0.26 gpm for both the pure water and EGC mix. The temperature rise from junction to liquid and thermal resistance as functions of coolant flow rates at full average current loading are plotted in Figures 4.11 and 4.12.

Table 4.5. Gen-1 fully powered Q_1M_1 and Q_{x1} thermal resistance results for pure water & EGC mixtures

Junction - Inlet Liquid Thermal Results With H₂O Coolant -- Q1N1, Qx1 & Dx3 Powered

Flow Rate (Gal/min)	Flow Rate (L/min)	Pressure Drop (psi)	Q1M1 (Ic=125A)			Qx1 (Ic=20A)		
			Power Dissipation (W)	Delta Temperature Junc - Inlet (°C)	R _{th} junc-inlet (C/W)	Power Dissipation (W)	Delta Temperature Junc - Inlet (°C)	R _{th} junc-inlet (C/W)
0.08	0.3	0.2	127.9	16.0	0.125	20.0	15.0	0.752
0.10	0.4	0.5	128.2	14.0	0.129	20.1	13.5	0.672
0.13	0.5	0.5	128.4	13.2	0.103	20.2	13.2	0.654
0.16	0.6	0.6	128.6	12.6	0.098	20.2	12.1	0.598
0.21	0.8	0.7	128.8	11.8	0.092	20.3	11.2	0.552
0.26	1.0	1.1	128.9	10.9	0.085	20.3	10.1	0.497

Junction - Inlet Liquid Thermal Results With 50 EGC / 50 H₂O -- Q1M1, QX1 & Dx3 Powered

Flow Rate (Gal/min)	Flow Rate (L/min)	Pressure Drop (psi)	Q1M1 (Ic=125A)			Qx1 (Ic=20A)		
			Power Dissipation (W)	Delta Temperature Junc - Inlet (°C)	R _{th} junc-inlet (C/W)	Power Dissipation (W)	Delta Temperature Junc - Inlet (°C)	R _{th} junc-inlet (C/W)
0.08	0.3	0.2	127.4	19.1	0.150	19.7	18.3	0.927
0.10	0.4	0.5	127.8	16.5	0.129	19.9	16.1	0.810
0.13	0.5	0.6	128.0	15.0	0.117	20.0	14.8	0.741
0.16	0.6	0.6	128.2	14.2	0.111	20.0	14.1	0.704
0.21	0.8	0.9	128.4	12.8	0.100	20.1	12.9	0.642
0.26	1.0	1.0	128.5	11.9	0.093	20.2	11.9	0.590

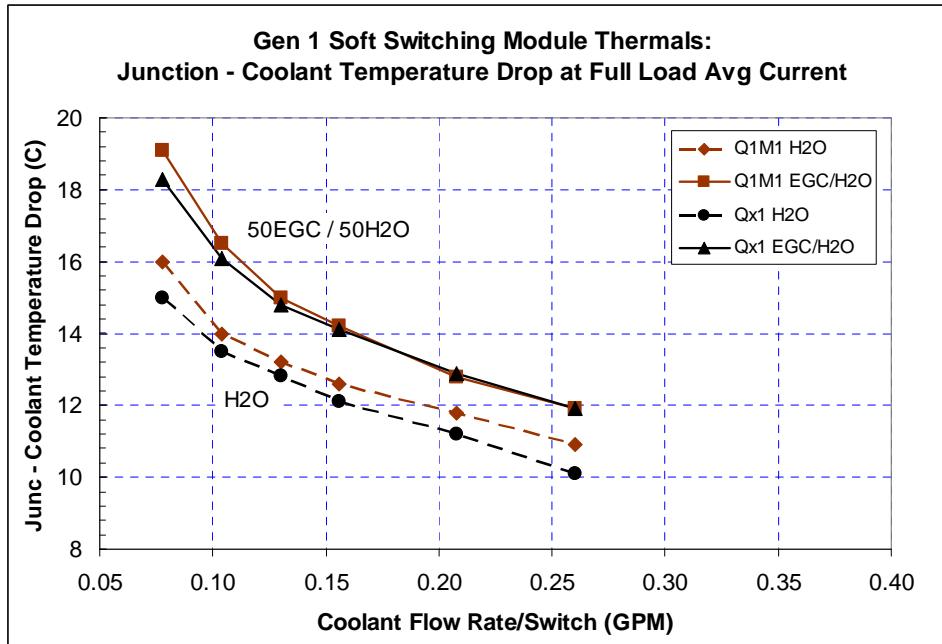


Figure 4.11. Results of Gen-1 module junction-to-coolant temperature drop at full average current of 125A.

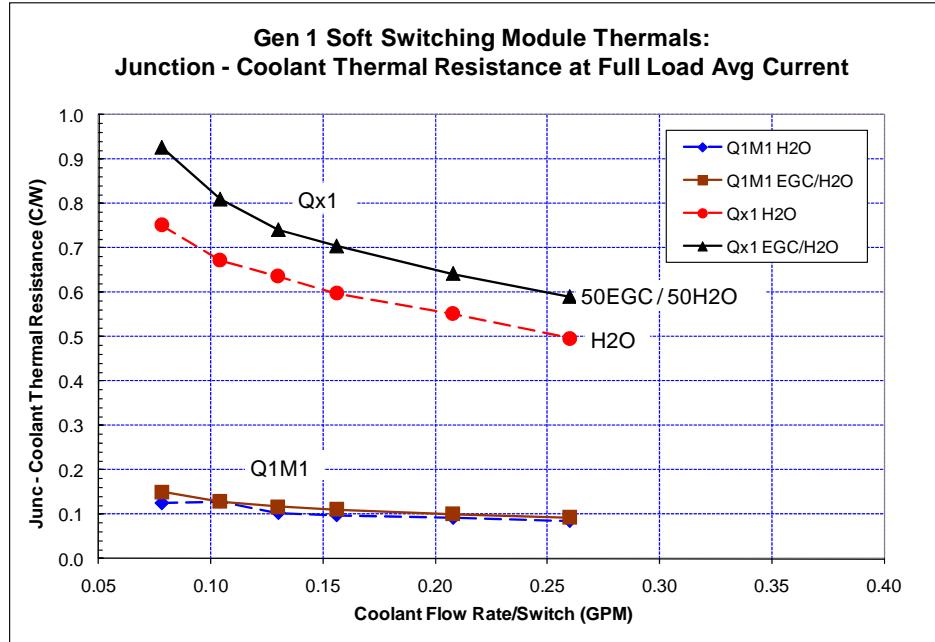


Figure 4.12. Results of Gen-1 module liquid-cooled thermal resistance at full average current of 125A showing the dependence of junction-to-liquid thermal resistance as a function of flow rate.

4.3. Generation 2 Module Development

A. Gen-2 Module Design

The design for the second generation, single phase, soft-switched IGBT module utilizes the same basic circuit configuration as that for the previous generation. The only difference is that the gate connections for $Q_{1,2}$ and $M_{1,2}$ in the power section are brought out separately to permit independent gate control for each type of device. The semiconductor chips, anticipated losses, peak currents and RMS currents per device are also the same for this generation and are summarized in Tables 4.1 and 4.2.

The primary changes in the Gen-2 module are the layout and package designs to reduce internal inductance and cost. The layout has reduced internal path lengths for terminal connections, especially those between the resonant capacitors and chips. Separate power post terminals are brought out directly from the substrate for the resonant capacitor connections. The substrate and housing package adopts the low profile, industry-standard Powerex “NX” series package design. The Gen 2 design has the same height, but will be slightly longer and wider than the standard NX package. Figures 4.13 and 4.14 show the terminal and control pin locations of the module. All gate drive & control pins are located on both sides of the package. Two AC power terminals and DC bus terminals are screw mounted. All of the auxiliary resonant capacitor and inductor connections are through center posts that solder to a heavy copper layer on the power printed circuit board of the inverter. Figure 4.15 shows the chip layout in the module. Photos of the module before and after wirebonding are shown in Figure 4.16. This design can be assembled on

a conventional flat baseplate or a built-in liquid-cooled chill plate used for the Gen-1 module. A conventional flat baseplate was utilized for this generation. The modules were bolted to a liquid cooled chill plate in the inverter.

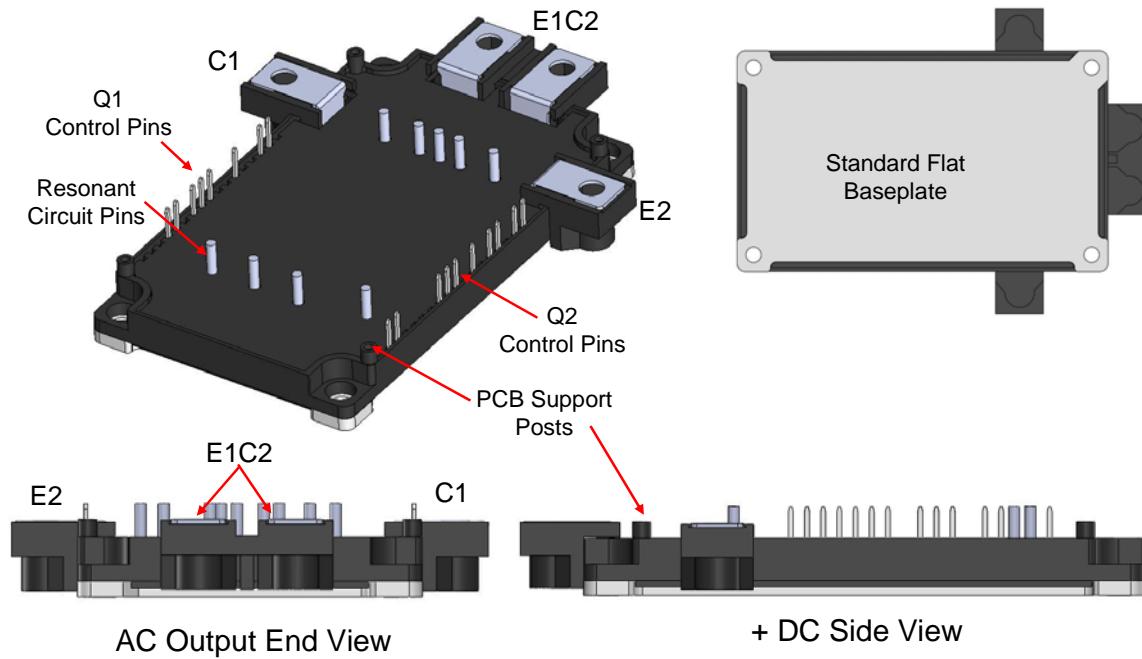


Figure 4.13. Gen-2 low profile package design.

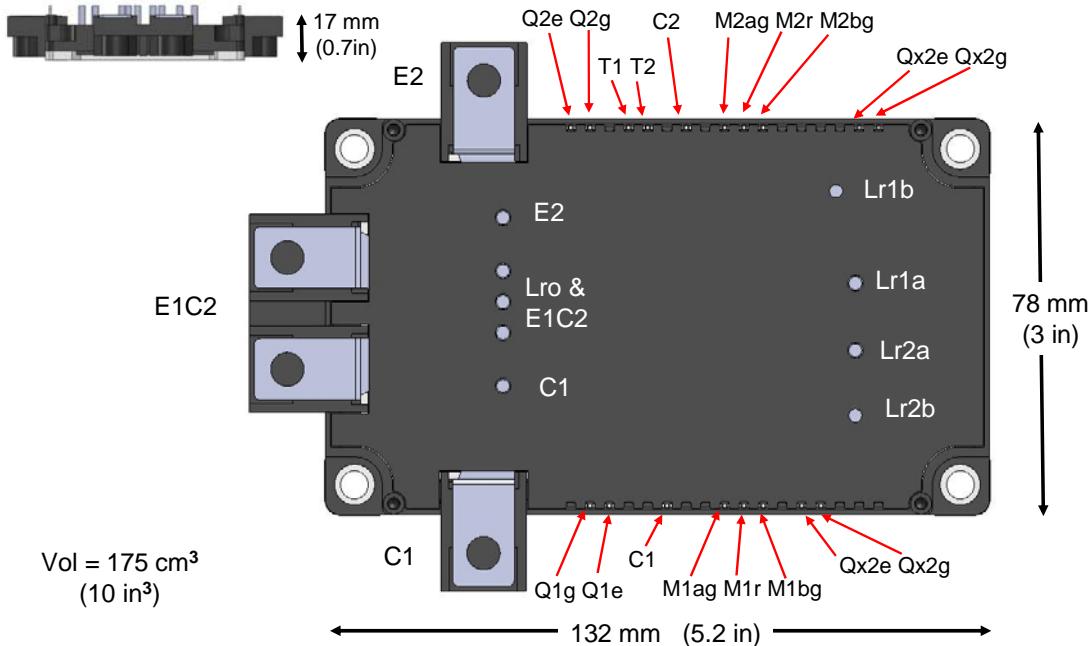


Figure 4.14. Gen-2 low profile package design showing power and control terminal/pin locations.

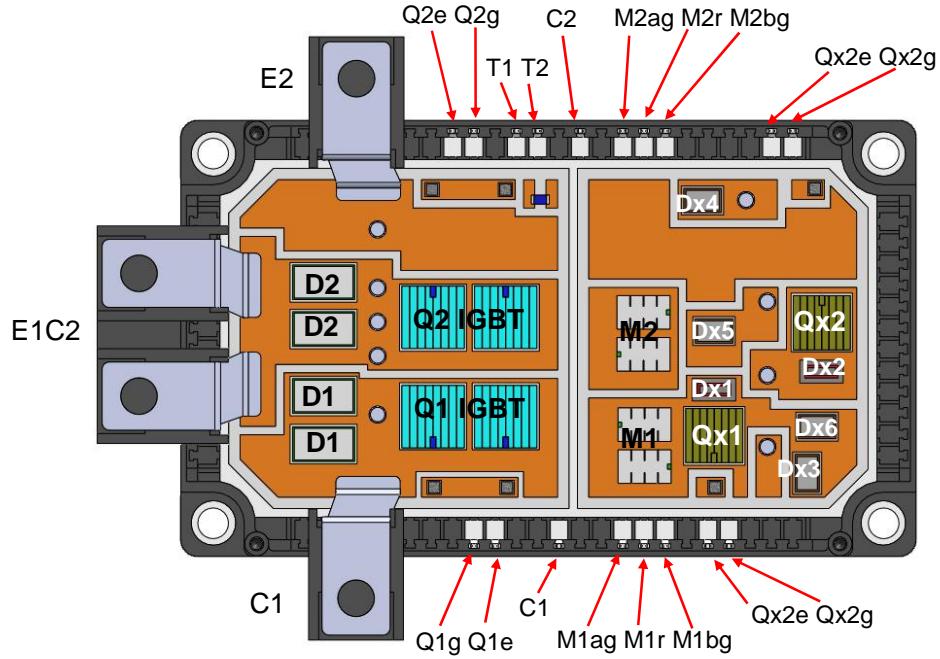


Figure 4.15. Gen-2 low profile package design showing chip locations.

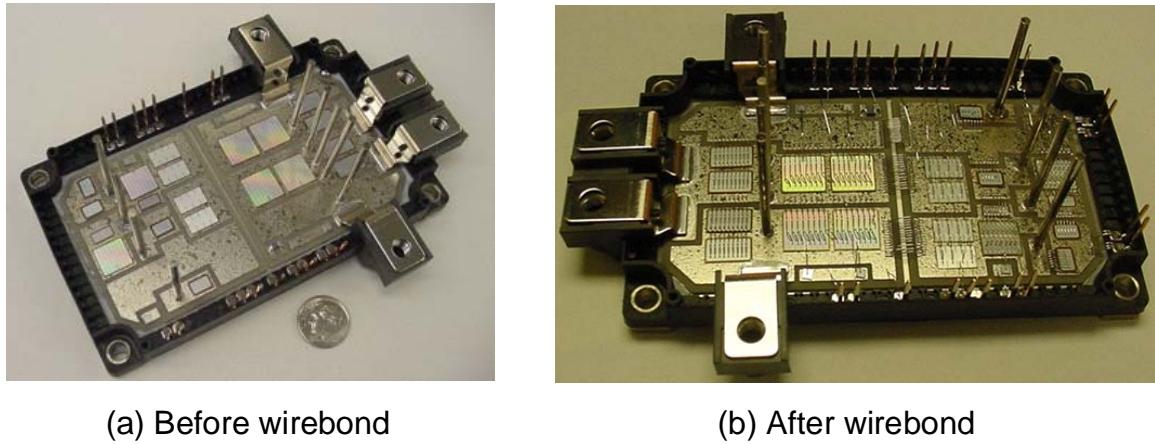


Figure 4.16. Photographs of Gen-2 soft-switching module layout: (a) before wirebond, (b) after wirebond.

B. Gen-2 Module Thermal Simulations

As discussed earlier, the Gen-2 module design is compatible with 3 different cooling options:

- 1) Standard air-cooled (flat baseplate mounted to air cooled heatsink)
- 2) Standard liquid-cooled (flat baseplate mounted to conventional liquid-cooled chill plate)
- 3) Direct liquid-cooled (built-in liquid-cooled chill plate).

Modeling was performed to assess the thermal performance of the three cooling options. The thermal resistances of the three options were estimated using the three methods below:

- 1) Computer 3D Finite Element Analysis (FEA) was used to determine the thermal resistance from junction to baseplate using Algor FEA software. Quasi-3D analytical

calculations were also performed as a “sanity check” to validate the FEA simulations. This was followed by an FEA analysis of the thermal resistance from baseplate to ambient of a bonded-fin, air-cooled heat sink using an on-line simulator provided by a commercial heat-sink supplier. The heat sink simulated was similar to that used by Azure Dynamics in their air-cooled electric vehicle drive systems.

- 2) The datasheet junction-baseplate thermal resistance values of the Powerex CM400DX-12A IGBT module were used, since it uses the same IGBT chips and has a nearly identical thermal-path design as the Gen-2 module. The thermal resistance from baseplate to ambient for the CM400DX-12A was modeled using the same on-line simulator as used in Method 1. Simulations were performed for the same air-cooled heat sink in Method 1 as well as a standard commercial liquid-cooled chill plate.
- 3) The results of the direct liquid-cooled thermal measurements performed on the Gen-1 modules were used to estimate the Gen-2 direct liquid-cooled thermal resistance.

The results of the FEA and Quasi-3D calculations of the junction-baseplate thermal drops at full chip power dissipation levels are shown in Figure 4.17. There is good agreement between the full 3D FEA computer simulations and Quasi-3D analytical calculations. The chip temperatures in the graphic are for the case where the bottom of the baseplate held fixed at 25°C. The values in the table are the chip temperatures in the graphic menu 25°C. This indicates a temperature rise from junction to baseplate of 7°C for the power IGBTs ($Q_{1,2}$) and a 4°C rise for the power MOSFETs ($M_{1,2}$). Of course, this temperature rise must be added to that of the heat sink or chill plate.

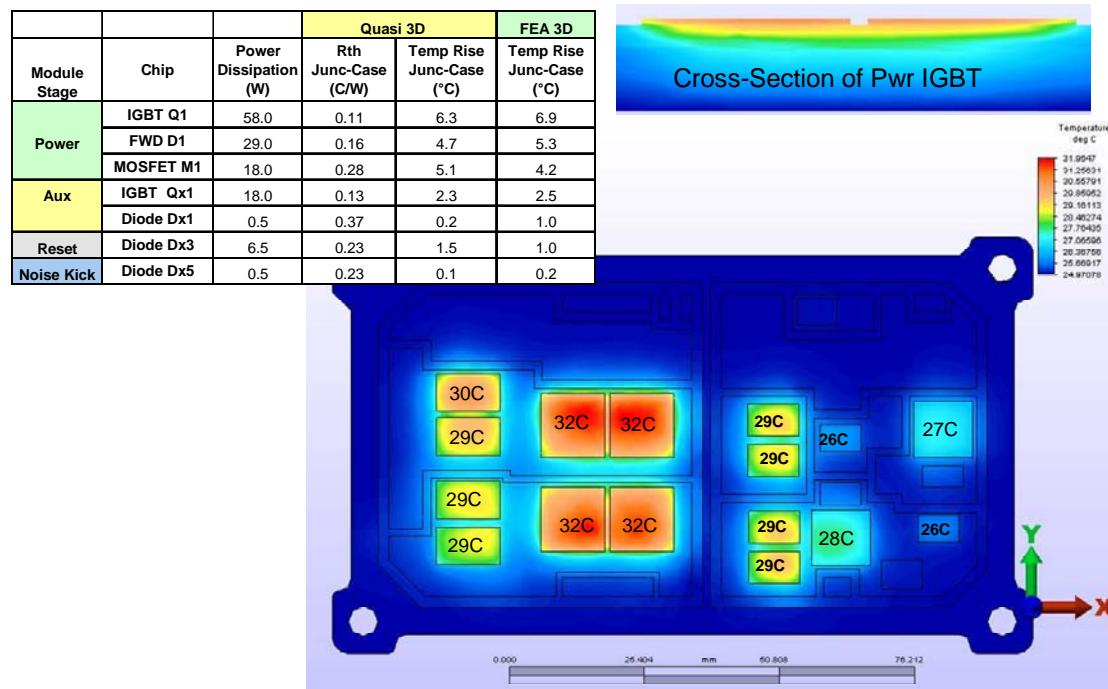


Figure 4.17. 3D FEA simulation results of the temperature rise from junction to baseplate for the various chips in the Gen 2 design at the dissipation levels at full power operation. The comparison between the full FEA 3-D and Quasi-3D analytical results are listed in the table inset. For the results shown in the graphic, the bottom of the baseplate was held at 25C.

The full temperature drops from junction to ambient coolant are shown in Figure 4.18 for the three methods just discussed. As expected, air-cooling results in the highest temperature drops from junction to ambient of 35–37°C, indicating that maximum inlet air temperatures must be kept under 88°C for the IGBT junctions to operate below 125°C. The conventional liquid-cooling design exhibits a 28°C rise from junction to liquid at full power operation, which would result in junction temperatures of 133°C if the inlet coolant was at its peak temperature of 105°C and the inverter was operating at full output power simultaneously. The directly liquid-cooled design maintains junction temperatures well below 125°C, even with maximum inlet temperatures of 105°C.

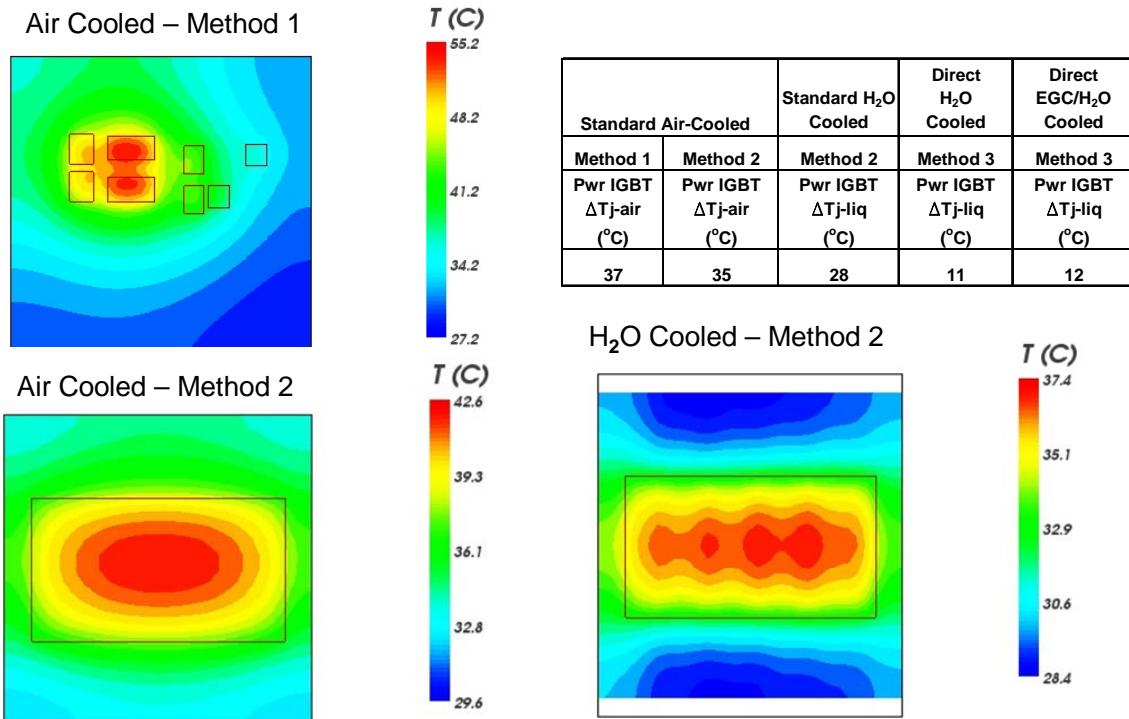


Figure 4.18. Comparison of junction-ambient temperature drops for the three cooling options possible for the Gen 2 module.

C. Gen-2 Module Conduction Characteristics Test Results

Test results from a sample of three of the Gen-2 modules delivered to Virginia Tech are listed in Table 4.6. A complete set of parametric measurements were conducted on three modules (serial numbers 201, 202 and 210). The results for SN 201 are plotted in the following curves in Figures 4.19–4.26 for both switches. The V_{cesat} and V_{ds-on} of the power stage IGBT and MOSFET chips were measured separately by gating one set on while simultaneously biasing the other set off by shorting the gate pin to the emitter/source return pin. The V_{cesat} of the parallel combination was measured by gating both sets of chips on at the same time. The plots in Figures 4.19, 4.20, 4.23, and 4.24 show the low voltage drops at currents < 50A due to the low resistive drop of the

MOSFETs in parallel with the IGBTs. Most of the current above 50 to 75A is carried by the IGBTs. At elevated temperatures, the R_{ds-on} of the MOSFETs increases, resulting in higher conduction losses for $I < 50A$ compared to lower temperatures. This is somewhat offset by the slight reduction in V_{cesat} of the IGBTs at higher temperatures, as shown in Figures 4.20 and 4.24.

Table 4.6. Test Results for a sample of the Gen-2 Modules

Module SN 201 25C

Terminals	Device	Leakage Current @ 600V (uA)
C1 - E1C2	Q1	7.0
C1 - Lr1a	Qx1	7.0
C1 - Lr2b	Dx3	0.7
C1 - Lr2a	Dx6	5.8
E1C2 - E2	Q2	8.7
Lr2a - E2	Qx2	7.1
Lr1b - E2	Dx4	0.6
Lr1a - E2	Dx5	5.9

Module SN 201

25C

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	D1 Vf (V)	D2 Vf (V)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
20	0.42	0.40										
30	0.62	0.60										
50	0.87	0.85										
100	1.15	1.11	0.93	0.93	1.34	1.30	2.35	2.46	2.95	3.10	2.87	2.92
150	1.26	1.20										
200	1.34	1.26										
250	1.41	1.32										
300	1.47	1.37										
400	1.60	1.47										

Module SN 201 125C

Terminals	Device	Leakage Current @ 600V (uA)
C1 - E1C2	Q1	138.0
C1 - Lr1a	Qx1	133.0
C1 - Lr2b	Dx3	3.8
C1 - Lr2a	Dx6	99.0
E1C2 - E2	Q2	145.0
Lr2a - E2	Qx2	131.0
Lr1b - E2	Dx4	3.6
Lr1a - E2	Dx5	99.5

Module SN 201

125C

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	D1 Vf (V)	D2 Vf (V)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
20	0.58	0.57										
30	0.69	0.67										
50	0.81	0.79										
100	1.00	0.95	0.82	0.83	1.25	1.23	2.25	2.38	2.72	2.86	2.71	2.70
150	1.13	1.05										
200	1.24	1.14										
250	1.34	1.22										
300	1.43	1.28										
400	1.60	1.41										

Module SN 210 25C

Terminals	Device	Leakage Current @ 600V (uA)
C1 - E1C2	Q1	10.0
C1 - Lr1a	Qx1	10.9
C1 - Lr2b	Dx3	1.0
C1 - Lr2a	Dx6	6.0
E1C2 - E2	Q2	10.1
Lr2a - E2	Qx2	8.5
Lr1b - E2	Dx4	1.0
Lr1a - E2	Dx5	6.0

Module SN 210

25C

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	D1 Vf (V)	D2 Vf (V)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
20	0.40	0.41										
30	0.60	0.60										
50	0.87	0.86										
100	1.16	1.13	0.93	0.94	1.32	1.37	2.35	2.43	3.07	2.94	2.94	2.92
150	1.27	1.22										
200	1.35	1.28										
250	1.42	1.33										
300	1.49	1.38										
400	1.62	1.48										
Power	C1-E1/C2	E1/C2-E2	E1/C2-C1	E2-E1/C2	C1-Lr1a	Lr2a-E2	Lr1a-C1	E2-Lr2a	Lr2b-C1	E2-Lr1b	E2-Lr1a	Lr2a-C1
Sense	C1pm-Q1er	C2pm-Q2er	C2pm-C1pm	E2pe-C2pm	C1pe-Q1er	Lr2a-Q2er	Q1xer-C1pe	Q2xer-Lr2a	Lr2b-C1pe	E2pe-Lr1b	E2pe-Lr1a	Lr2a-C1pe

Module SN 210 125C

Terminals	Device	Leakage Current @ 600V (uA)
C1 - E1C2	Q1	208
C1 - Lr1a	Qx1	217
C1 - Lr2b	Dx3	9
C1 - Lr2a	Dx6	168
E1C2 - E2	Q2	235
Lr2a - E2	Qx2	236
Lr1b - E2	Dx4	9
Lr1a - E2	Dx5	183

Module SN 210

125C

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	D1 Vf (V)	D2 Vf (V)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
20	0.58	0.57										
30	0.68	0.66										
50	0.79	0.77										
100	0.98	0.93	0.80	0.78	1.23	1.27	2.24	2.32	2.79	2.70	2.71	2.67
150	1.11	1.04										
200	1.23	1.13										
250	1.33	1.21										
300	1.43	1.28										
400	1.61	1.42										
Power	C1-E1/C2	E1/C2-E2	E1/C2-C1	E2-E1/C2	C1-Lr1a	Lr2a-E2	Lr1a-C1	E2-Lr2a	Lr2b-C1	E2-Lr1b	E2-Lr1a	Lr2a-C1
Sense	C1pm-Q1er	C2pm-Q2er	C2pm-C1pm	E2pe-C2pm	C1pe-Q1er	Lr2a-Q2er	Q1xer-C1pe	Q2xer-Lr2a	Lr2b-C1pe	E2pe-Lr1b	E2pe-Lr1a	Lr2a-C1pe

Module SN 211 25C

Terminals	Device	Leakage Current @ 600V (uA)
C1 - E1C2	Q1	7.4
C1 - Lr1a	Qx1	5.9
C1 - Lr2b	Dx3	1.0
C1 - Lr2a	Dx6	5.6
E1C2 - E2	Q2	7.5
Lr2a - E2	Qx2	6.0
Lr1b - E2	Dx4	0.6
Lr1a - E2	Dx5	5.7

Module SN 211

25C

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	D1 Vf (V)	D2 Vf (V)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
20	0.40	395.00										
30	0.60	0.60										
50	0.86	0.86										
100	1.16	1.14	0.93	0.90	1.26	1.30	2.15	2.30	2.92	3.10	2.92	3.07
150	1.28	1.24										
200	1.36	1.31										
250	1.43	1.36										
300	1.50	1.42										
400	1.64	1.51										
Power	C1-E1/C2	E1/C2-E2	E1/C2-C1	E2-E1/C2	C1-Lr1a	Lr2a-E2	Lr1a-C1	E2-Lr2a	Lr2b-C1	E2-Lr1b	E2-Lr1a	Lr2a-C1
Sense	C1pm-Q1er	C2pm-Q2er	C2pm-C1pm	E2pe-C2pm	C1pe-Q1er	Lr2a-Q2er	Q1xer-C1pe	Q2xer-Lr2a	Lr2b-C1pe	E2pe-Lr1b	E2pe-Lr1a	Lr2a-C1pe

The conduction losses of the auxiliary stage IGBT and resonant diodes are shown in Figures 4.21, 4.22, 4.25, and 4.26 for junction temperatures of 25 and 125°C. Since the same 1200V, 50A chip is used for D_{x3} , D_{x6} , D_{x4} and D_{x5} , the V_f values are essentially the same. The slight difference in the V_f values for D_{x4} and D_{x5} in Q_{x2} is due to the placement of the Kelvin probes during the voltage measurement.

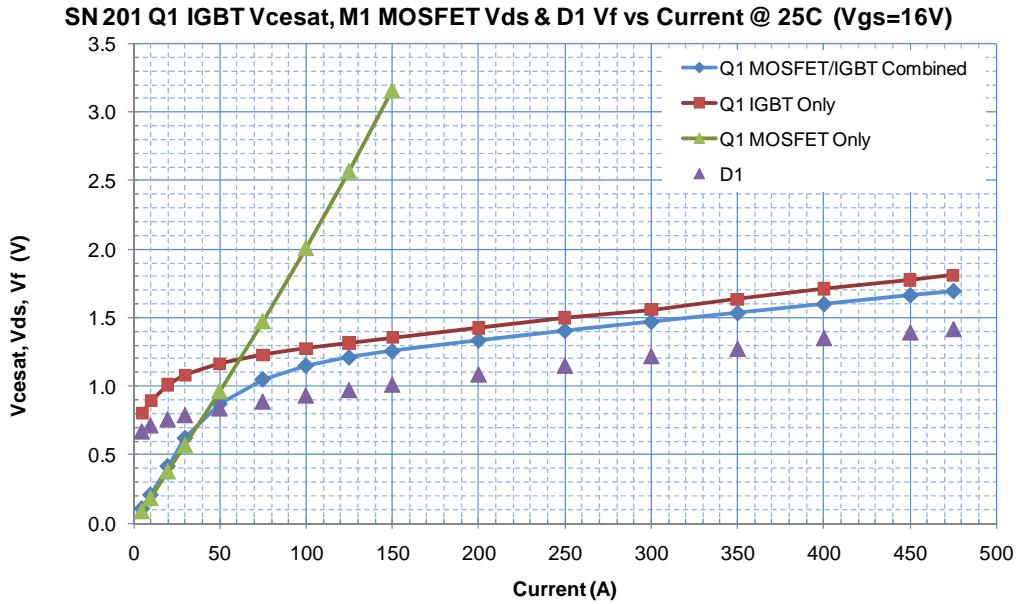


Figure 4.19. Voltage drops for the power stage IGBT, MOSFET, MOSFET/IGBT combination and main free-wheel diode (D_1) at $T_j=25^\circ\text{C}$ for Gen-2 module SN201, Q_1 .

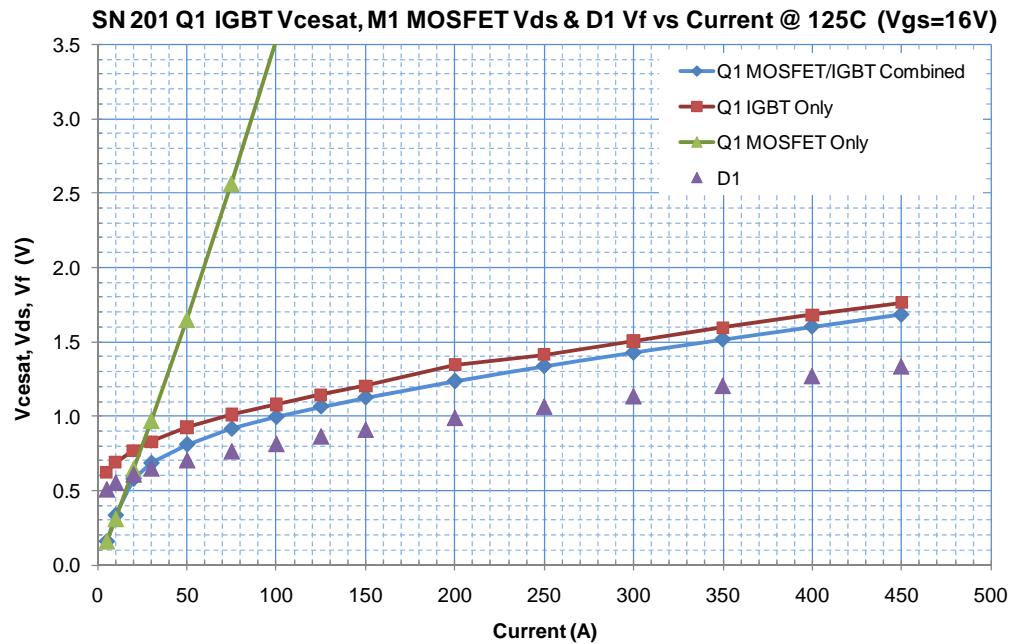


Figure 4.20. Voltage drops for the power stage IGBT, MOSFET, MOSFET/IGBT combination and main free-wheel diode (D_1) at $T_j=125^\circ\text{C}$ for Gen-2 module SN201, Q_1 .

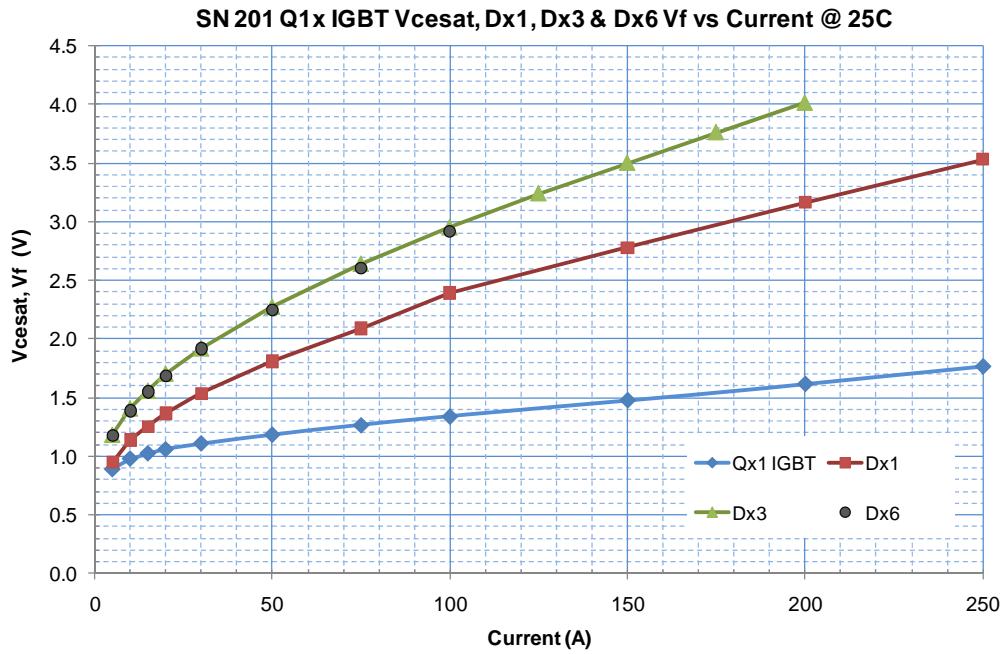


Figure 4.21. Voltage drops for the auxiliary IGBT (Q_{x1}), free-wheel diode (D_{x1}) and resonant diodes (D_{x3}, D_{x6}) at $T_j=25^\circ\text{C}$ for Gen-2 module SN201 Q_{x1} .

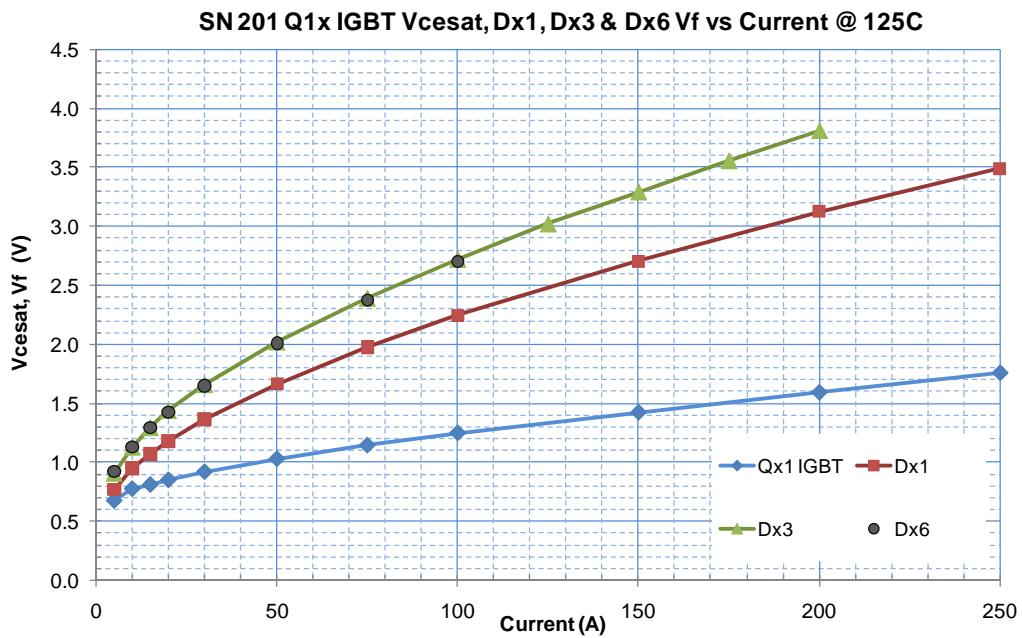


Figure 4.22. Voltage drops for the auxiliary IGBT (Q_{x1}), free-wheel diode (D_{x1}) and resonant diodes (D_{x3}, D_{x6}) at $T_j=125^\circ\text{C}$ for Gen-2 module SN201 Q_{x1} .

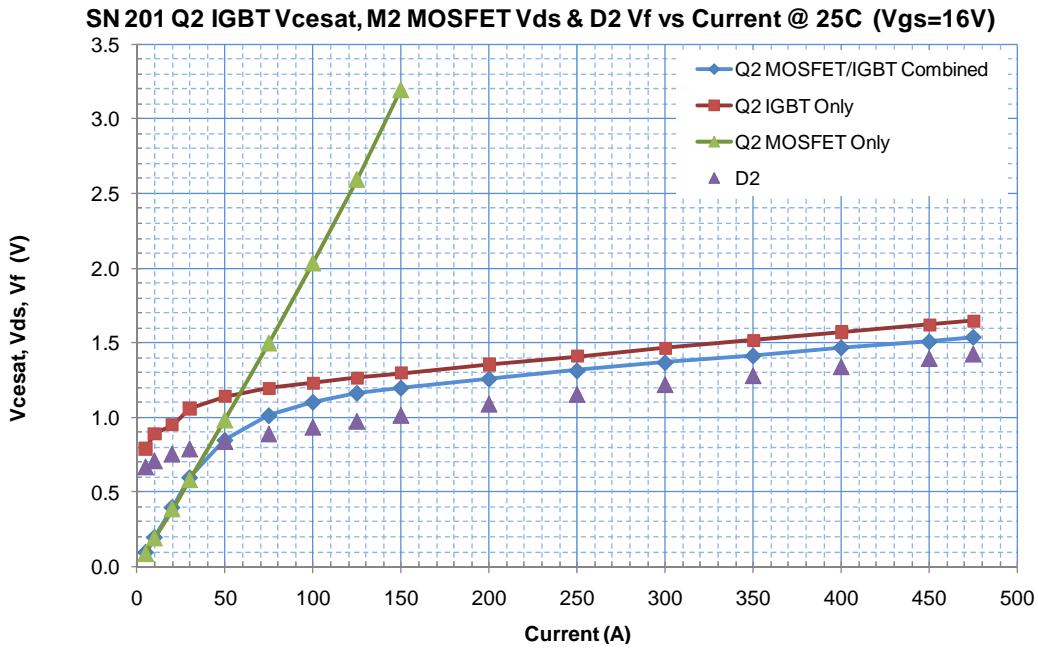


Figure 4.23. Voltage drops for the power stage IGBT, MOSFET, MOSFET/IGBT combination and main free-wheel diode (D_2) at $T_j=25^\circ\text{C}$ for Gen-2 module SN201, Q₂.

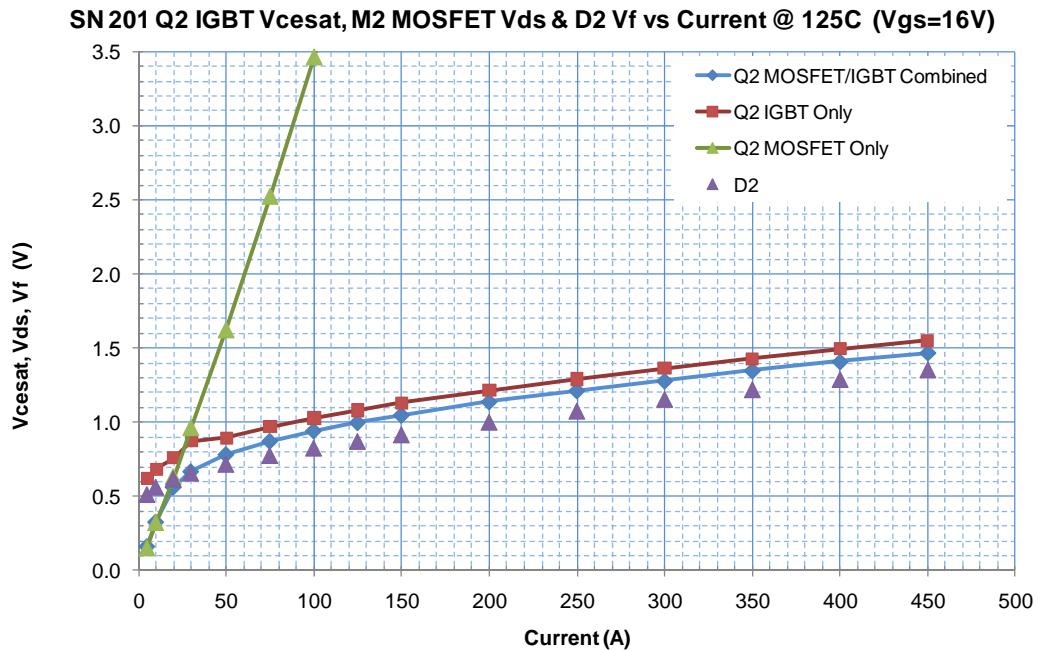


Figure 4.24. Voltage drops for the power stage IGBT, Mosfet, Mosfet/IGBT combination and main free-wheel diode (D_2) at $T_j=125^\circ\text{C}$ for Gen-2 module SN201, Q₂.

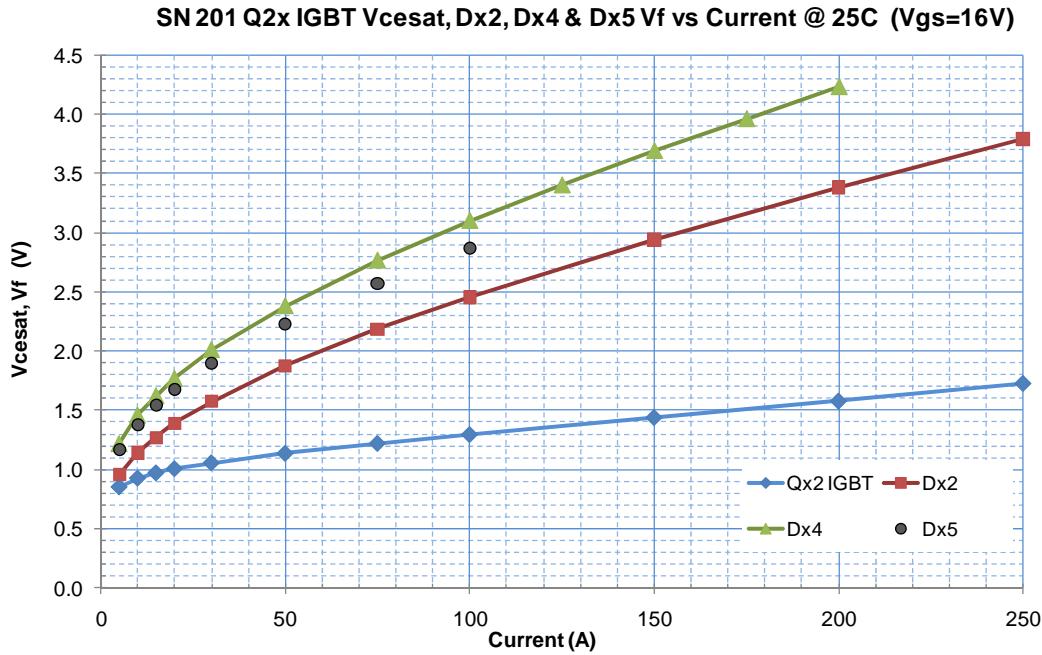


Figure 4.25. Voltage drops for the auxiliary IGBT (Q_{x2}), free-wheel diode (D_{x2}) and resonant diodes (D_{x4}, D_{x5}) at $T_j=25^\circ\text{C}$ for Gen-2 module SN201 Q_{x2} .

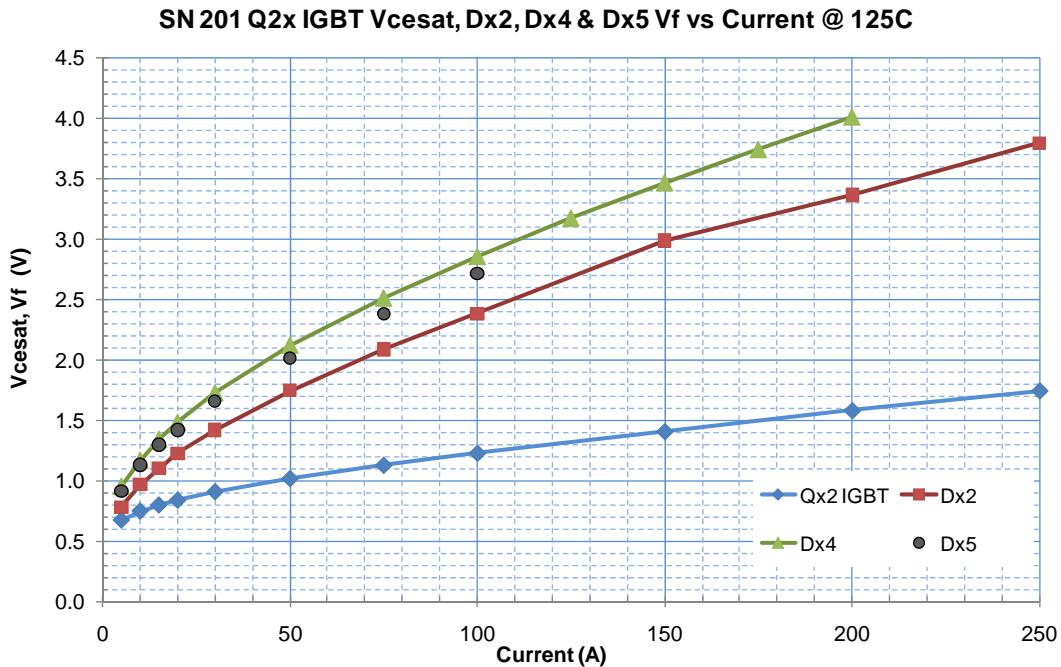


Figure 4.26. Voltage drops for the auxiliary IGBT (Q_{x2}), free-wheel diode (D_{x2}) and resonant diodes (D_{x4}, D_{x5}) at $T_j=125^\circ\text{C}$ for Gen-2 module SN201 Q_{x2} .

Even though the Gen-2 design exhibited a 79% reduction in internal inductance as compared with Gen 1, one disadvantage is the higher internal resistance in the power section due to the longer lateral current-flow paths in the 0.012 inch thick copper pads on the AlN substrate. A comparison of the conduction voltage drops (terminal – terminal) of the Gen-1 and Gen-2 modules is shown in Figure 4.27. The Gen 2 modules have a 200mV higher voltage drop at 400A than the Gen 1 modules, which resulted in at least a 0.3% point reduction in efficiency of the inverter.

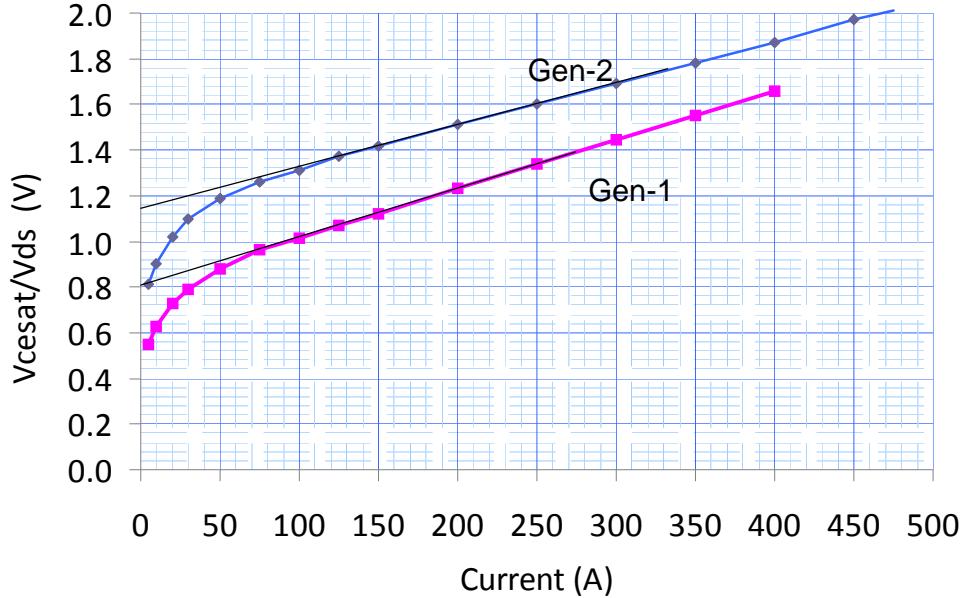


Figure 4.27. Voltage drop comparison of the Gen 1 and 2 modules.

4.4. Gen-3 Module Development

A. Gen-3 Module Design

The Gen-3 design was focused on reducing the internal parasitic resistance and inductance, as well as replacing both the existing MOSFET and antiparallel diode with a new, lower R_{ds-on} MOSFET with an improved internal body diode capable of handling the free-wheeling currents. The large, single module was also split into two separate modules to decrease the size of the AlN substrates to improve thermal cycling reliability. One module consists of the power stage (half H-bridge) and the other the auxiliary resonant-switching section. The Gen 3 module utilizes a flat baseplate like Gen-2, but is capable of being assembled on a built-in liquid chill-plate similar to Gen-1. The Gen-3 inverter exhibited such low losses and high efficiencies that air cooling was utilized. The Gen-2 and Gen-3 designs are compared in Figure 4.28.

The Infineon Cool-MOS MOSFET used in the two previous generations was replaced by a ST Microelectronics STY112N65M5, which has a lower R_{ds-on} than the Infineon device. In addition, testing of the reverse recovery characteristics of the body diode by Virginia Tech indicated comparable performance compared to the Infineon device. The total chip area of ST devices is sufficient to handle the freewheeling current, thus allowing elimination of the extra antiparallel

diodes in the power section. Based on extensive circuit modeling performed by Virginia Tech, it was decided to use two of the new STY112N65M5 MOSFETs (each rated at 93A average) and two of the existing Powerex 200A rated IGBTs per switch for the Gen-3 modules.

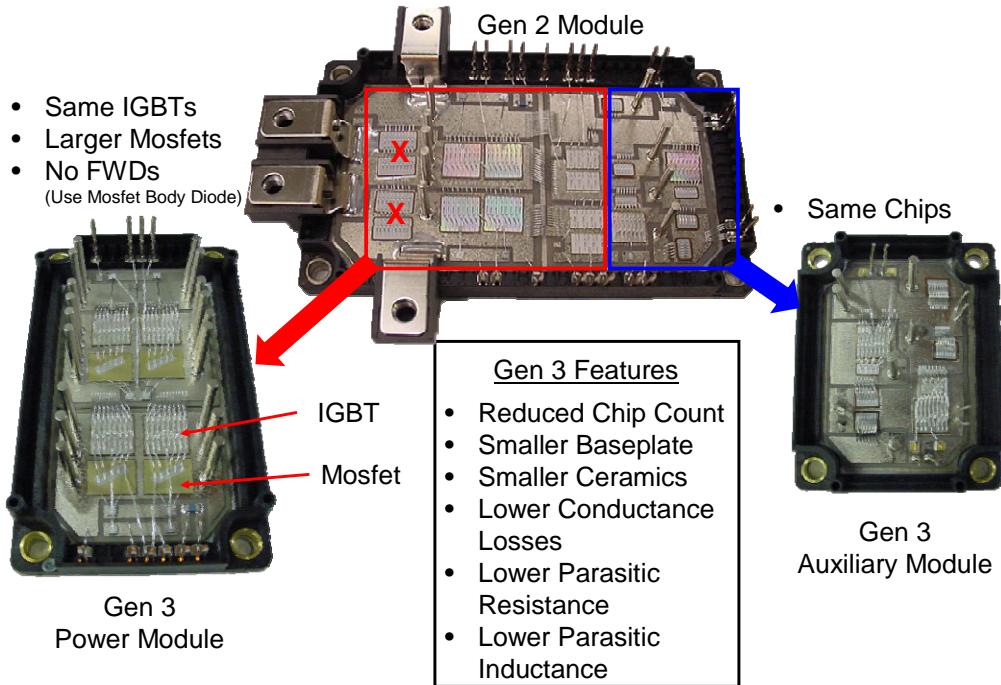


Figure 4.28. Comparison of Gen 2 and Gen 3 modules.

The screw power terminals of the previous generations were replaced by heavy-duty copper posts located adjacent to the IGBT and MOSFET chips as shown in Figure 4.29. The posts are soldered to the power bus PC board located directly above the module. This minimizes both the internal inductance and parasitic resistance of the power stage. The high current connections are made to the auxiliary module in the same manner. The resonant currents during the soft-switching periods circulate between the power and auxiliary modules via the power bus PCB.

Even though the Gen-3 MOSFETs are slightly larger in area than the Gen-2 devices, the two designs are sufficiently similar that it was deemed not necessary to perform thermal resistance simulations for this design.

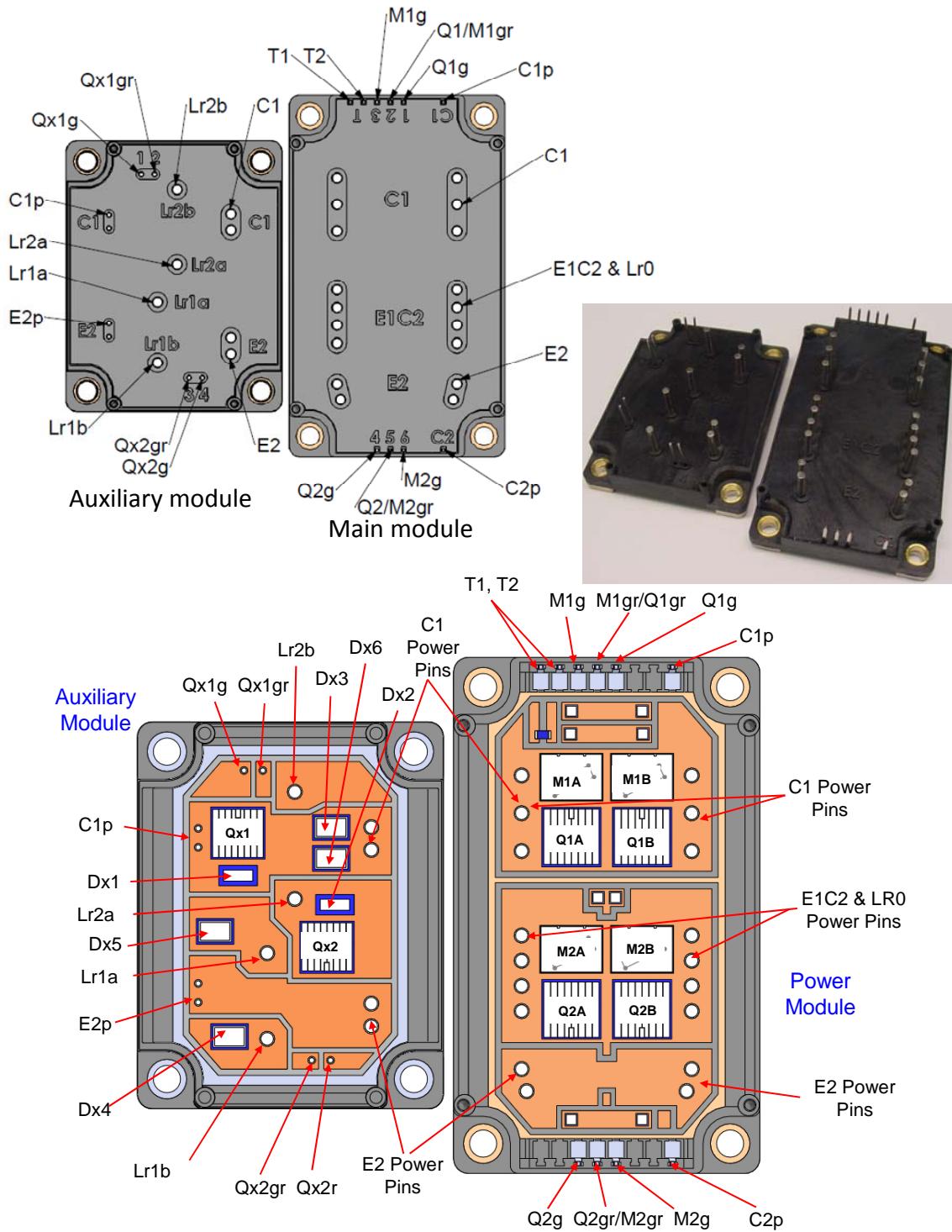


Figure 4.29. Pin locations (top) and chip layout (bottom) for the Gen-3 auxiliary and power modules.

B. Gen-3 Module Test Results

The test results for a sample of the power modules shipped to Virginia Tech are listed in Table 4.7. The test results for the auxiliary modules are listed in Table 4.8. The typical voltage drop curves for forward and reverse conduction are plotted as a function of current in Figures 4.30 and 4.31 for the upper and lower power switches, respectively. Independent control of the MOSFET gates permits the MOSFET to be gated on during the reverse recovery transient, thus reducing the losses during that period as shown in Figure 4.32. Finally, the forward voltage drops of the three generations of modules are compared in Figure 4.33. The reduction of the internal parasitic resistance and the use of higher current MOSFETs in the Gen-3 design resulted in significant decreases in the losses at low and high current levels.

Table 4.7. Test results for Gen-3 power modules

Module SN 301P		25C		Module SN 301P		25C		Shipped 7/22/2011				
Terminals	Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)	Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	M1 Body Diode Vf (V)	M2 Body Diode Vf (V)	Device	Gate Leakage Current @ Vg=+20V (nA)	Gate Leakage Current @ Vg=-20V (nA)	Gate Threshold Voltage @ IC=15mA (V)
C1 - E1C2	Q1M1	6.0	7.0	10	0.08	0.09	0.70	0.71	Q1M1	4.0	5.0	4.03
E1C2 - E2	Q2M2	6.6	7.7	25	0.21	0.22	0.74	0.75	Q2M2	3.0	3.0	4.14
Hipot Pass		2000VACrms, 60 sec		50	0.39	0.42	0.78	0.81				
				75	0.61	0.64	0.80	0.84				
				100	0.78	0.83	0.82	0.87				
				125	0.91	0.96	0.84	0.90				
				150	0.99	1.05	0.86	0.93				
				200	1.09	1.16	0.88	0.98				
				250	1.16	1.23	0.91	1.03				
				300	1.23	1.29	0.93	1.07				
				350	1.28	1.35						
				400	1.34	1.40						
				450	1.40	1.46						
				475	1.42	1.49						
				500	1.45	1.51						
Note: Kelvin Connections on Collector Potential Pins & Gate Return Pins				Module SN 301P		125C		Module SN 301P		125C		
Terminals	Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)	Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	M1 Body Diode Vf (V)	M2 Body Diode Vf (V)	Device	Gate Leakage Current @ Vg=+20V (nA)	Gate Leakage Current @ Vg=-20V (nA)	Gate Threshold Voltage @ IC=15mA (V)
C1 - E1C2	Q1M1	260.0	300.0	10	0.15	0.16	0.52	0.53	Q1M1			3.30
E1C2 - E2	Q2M2	270.0	310.0	25	0.38	0.40	0.57	0.59	Q2M2			3.36
Note: Kelvin Connections on Collector Potential Pins & Gate Return Pins				50	0.59	0.62	0.62	0.66				
				75	0.71	0.74	0.66	0.71				
				100	0.79	0.83	0.68	0.75				
				125	0.87	0.90	0.71	0.79				
				150	0.93	0.95	0.73	0.83				
				200	1.03	1.06	0.76	0.90				
				250	1.13	1.16	0.79	0.96				
				300	1.22	1.24	0.82	1.02				
				350	1.30	1.33						
				400	1.38	1.41						
				450	1.47	1.48						
				475	1.51	1.52						
				500	1.55	1.56						

Module SN 302P

25C

Module SN 302P

25C Shipped 7/22/2011

Terminals	Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
C1 - E1C2	Q1M1	11.0	15.0
E1C2 - E2	Q2M2	8.2	9.6

Hipot	Pass
2000VACrms, 60 sec	

Note: Kelvin Connections on Collector Potential Pins & Gate Return Pins

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	M1 Body Diode Vf (V)	M2 Body Diode Vf (V)	Device	Gate Leakage Current @ Vg=+20V (nA)	Gate Leakage Current @ Vg=-20V (nA)	Gate Threshold Voltage @ IC=15mA (V)
10	0.09	0.09	0.70	0.70	Q1M1	20.0	20.0	4.20
25	0.22	0.23	0.74	0.75	Q2M2	138.0	133.0	4.14
50	0.40	0.42	0.78	0.80				
75	0.62	0.65	0.80	0.84				
100	0.79	0.83	0.82	0.87				
125	0.93	0.96	0.84	0.90				
150	1.04	1.05	0.85	0.93				
200	1.16	1.16	0.88	0.98				
250	1.24	1.23	0.91	1.03				
300	1.31	1.29	0.93	1.08				
350	1.37	1.35						
400	1.43	1.40						
450	1.49	1.46						
475	1.51	1.48						
500	1.54	1.51						

Module SN 302P

125C

Module SN 302P

125C

Terminals	Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
C1 - E1C2	Q1M1	290.0	340.0
E1C2 - E2	Q2M2	270.0	310.0

Note: Kelvin Connections on Collector Potential Pins & Gate Return Pins

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	M1 Body Diode Vf (V)	M2 Body Diode Vf (V)	Device	Gate Leakage Current @ Vg=+20V (nA)	Gate Leakage Current @ Vg=-20V (nA)	Gate Threshold Voltage @ IC=15mA (V)
10	0.16	0.16	0.52	0.53	Q1M1			3.42
25	0.38	0.40	0.57	0.59	Q2M2			3.38
50	0.60	0.62	0.63	0.66				
75	0.73	0.74	0.66	0.71				
100	0.82	0.83	0.68	0.75				
125	0.89	0.89	0.71	0.79				
150	0.96	0.95	0.72	0.83				
200	1.07	1.06	0.76	0.90				
250	1.17	1.15	0.79	0.96				
300	1.27	1.24	0.82	1.03				
350	1.36	1.32						
400	1.44	1.40						
450	1.52	1.48						
475	1.56	1.52						
500	1.60	1.55						

Module SN 303P

25C

Module SN 303P

25C Shipped 7/22/2011

Terminals	Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
C1 - E1C2	Q1M1	5.0	7.0
E1C2 - E2	Q2M2	6.6	7.9

Hipot	Pass
2000VACrms, 60 sec	

Note: Kelvin Connections on Collector Potential Pins & Gate Return Pins

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	M1 Body Diode Vf (V)	M2 Body Diode Vf (V)	Device	Gate Leakage Current @ Vg=+20V (nA)	Gate Leakage Current @ Vg=-20V (nA)	Gate Threshold Voltage @ IC=15mA (V)
10	0.08	0.09	0.70	0.71	Q1M1	18.0	17.0	4.16
25	0.21	0.22	0.74	0.75	Q2M2	22.0	21.0	4.08
50	0.39	0.42	0.78	0.81				
75	0.60	0.64	0.80	0.84				
100	0.78	0.82	0.82	0.87				
125	0.90	0.96	0.84	0.90				
150	0.99	1.06	0.86	0.93				
200	1.10	1.16	0.88	0.98				
250	1.17	1.24	0.91	1.03				
300	1.23	1.30	0.93	1.08				
350	1.29	1.35						
400	1.34	1.41						
450	1.40	1.46						
475	1.43	1.49						
500	1.46	1.51						

Module SN 303P

125C

Module SN 303P

125C

Terminals	Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
C1 - E1C2	Q1M1	270.0	315.0
E1C2 - E2	Q2M2	280.0	320.0

Note: Kelvin Connections on Collector Potential Pins & Gate Return Pins

Current (A)	Q1/M1 Vcesat (V)	Q2/M2 Vcesat (V)	M1 Body Diode Vf (V)	M2 Body Diode Vf (V)	Device	Gate Leakage Current @ Vg=+20V (nA)	Gate Leakage Current @ Vg=-20V (nA)	Gate Threshold Voltage @ IC=15mA (V)
10	0.15	0.16	0.52	0.53	Q1M1			3.39
25	0.38	0.40	0.57	0.59	Q2M2			3.34
50	0.59	0.62	0.63	0.66				
75	0.71	0.74	0.66	0.71				
100	0.80	0.83	0.68	0.45				
125	0.87	0.90	0.71	0.79				
150	0.93	0.96	0.73	0.83				
200	1.04	1.07	0.76	0.89				
250	1.14	1.16	0.79	0.96				
300	1.23	1.25	0.82	1.02				
350	1.32	1.33						
400	1.40	1.41						
450	1.48	1.48						
475	1.52	1.52						
500	1.55	1.55						

Table 4.8. Test results for Gen-3 auxiliary modules

Module SN 302A

Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
Qx1	0.1	0.06
Dx3		0.11
Dx6		0.01
Qx2	0.1	0.33
Dx4		0.02
Dx5		0.01

25C

Shipped 7/22/2011

Current (A)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
10	0.95	0.95	1.10	1.12	1.40	1.46	1.42	1.54
25	1.07	1.06	1.38	1.43	1.80	1.90	1.83	2.02
50	1.18	1.17	1.75	1.84	2.18	2.31	2.22	2.49
75	1.29	1.27	2.00	2.10	2.53	2.69	2.58	2.92
100	1.40	1.36	2.22	2.35	2.83	3.02	2.89	3.28
150	1.60	1.56	2.61	2.78	3.36	3.61	3.45	3.94
200	1.80	1.75	2.96	3.18	3.84	4.14	3.95	4.51
250	2.02	1.95	3.31	3.56				

Note: Kelvin Connection on Same Pin as Power Connection

Module SN 302A

Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
Qx1	100.6	113.4
Dx3		13.1
Dx6		26.1
Qx2	104.0	118.0
Dx4		12.6
Dx5		26.6

125C

Current (A)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
10	0.71	0.70	0.88	0.90	1.07	1.10	1.09	1.13
25	0.86	0.85	1.18	1.22	1.47	1.52	1.49	1.58
50	1.02	1.00	1.58	1.66	1.86	1.94	1.90	2.04
75	1.18	1.15	1.86	1.96	2.22	2.33	2.27	2.46
100	1.32	1.28	2.10	2.12	2.53	2.67	2.60	2.82
150	1.58	1.53	2.53	2.70	3.08	3.27	3.17	3.46
200	1.84	1.76	2.91	3.12	3.56	3.78	3.68	3.95
250	2.10	2.00	3.26	3.50				

Note: Kelvin Connection on Same Pin as Power Connection

Module SN 303A

Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
Qx1	0.2	0.56
Dx3		0.08
Dx6		0.18
Qx2	0.5	1.50
Dx4		0.06
Dx5		0.20

25C

Shipped 7/22/2011

Current (A)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
10	1.07	1.07	1.15	1.15	1.41	1.45	1.47	1.51
25	1.22	1.22	1.48	1.47	1.80	1.87	1.90	1.98
50	1.34	1.33	1.91	1.90	2.18	2.27	2.32	2.43
75	1.45	1.44	2.19	2.20	2.53	2.64	2.71	2.84
100	1.56	1.54	2.45	2.46	2.83	2.97	3.04	3.19
150	1.77	1.74	2.92	2.93	3.36	3.54	3.63	3.82
200	1.99	1.95	3.34	3.36	3.84	4.05	4.17	4.37
250	2.21	2.16	3.74	3.76				

Note: Kelvin Connection on Same Pin as Power Connection

Module SN 303A

Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
Qx1	122.0	136.0
Dx3		13.5
Dx6		25.7
Qx2	118.0	133.0
Dx4		13.7
Dx5		26.7

125C

Current (A)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
10	0.77	0.76	0.91	0.92	1.07	1.09	1.10	1.12
25	0.95	0.94	1.25	1.26	1.47	1.51	1.53	1.56
50	1.13	1.12	1.71	1.73	1.86	1.92	1.95	2.01
75	1.31	1.29	2.02	2.04	2.23	2.30	2.34	2.42
100	1.48	1.45	2.30	2.33	2.54	2.64	2.69	2.77
150	1.79	1.75	2.79	2.84	3.09	3.22	3.28	3.38
200	2.08	2.03	3.28	3.29	3.57	3.72	3.81	3.91
250	2.39	2.33	3.62	3.70				

Note: Kelvin Connection on Same Pin as Power Connection

Module SN 305A

Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
Qx1	0.1	0.12
Dx3		0.06
Dx6		0.40
Qx2	1.1	2.36
Dx4		0.81
Dx5		0.44

25C

Shipped 7/22/2011

Current (A)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
10	0.95	1.07	1.12	1.15	1.46	1.41	1.57	1.40
25	1.07	1.22	1.42	1.47	1.88	1.81	2.07	1.80
50	1.18	1.33	1.80	1.90	2.29	2.19	2.57	2.17
75	1.29	1.44	2.06	2.19	2.67	2.55	3.03	2.51
100	1.39	1.54	2.30	2.45	3.00	2.85	3.42	2.81
150	1.59	1.75	2.71	2.92	3.57	3.40	4.11	3.34
200	1.79	1.95	3.09	3.35	4.09	3.90	4.73	3.82
250	1.99	2.17	3.44	3.75				

Note: Kelvin Connection on Same Pin as Power Connection

Module SN 305A

Device	Leakage Current @ 500V (uA)	Leakage Current @ 600V (uA)
Qx1	103.0	115.0
Dx3		13.3
Dx6		29.8
Qx2	137.0	155.0
Dx4		20.9
Dx5		31.1

125C

Current (A)	Qx1 Vcesat (V)	Qx2 Vcesat (V)	Dx1 Vf (V)	Dx2 Vf (V)	Dx3 Vf (V)	Dx4 Vf (V)	Dx5 Vf (V)	Dx6 Vf (V)
10	0.71	0.76	0.89	0.91	1.09	1.07	1.14	1.07
25	0.86	0.94	1.21	1.25	1.51	1.47	1.61	1.46
50	1.02	1.12	1.62	1.72	1.93	1.87	2.09	1.85
75	1.17	1.29	1.91	2.04	2.31	2.23	2.53	2.23
100	1.31	1.45	2.16	2.32	2.64	2.55	2.91	2.52
150	1.57	1.75	2.60	2.83	3.22	3.11	3.58	3.07
200	1.82	2.04	2.99	3.27	3.48	3.36	3.87	3.31
250	2.08	2.33	3.36	3.68				

Note: Kelvin Connection on Same Pin as Power Connection

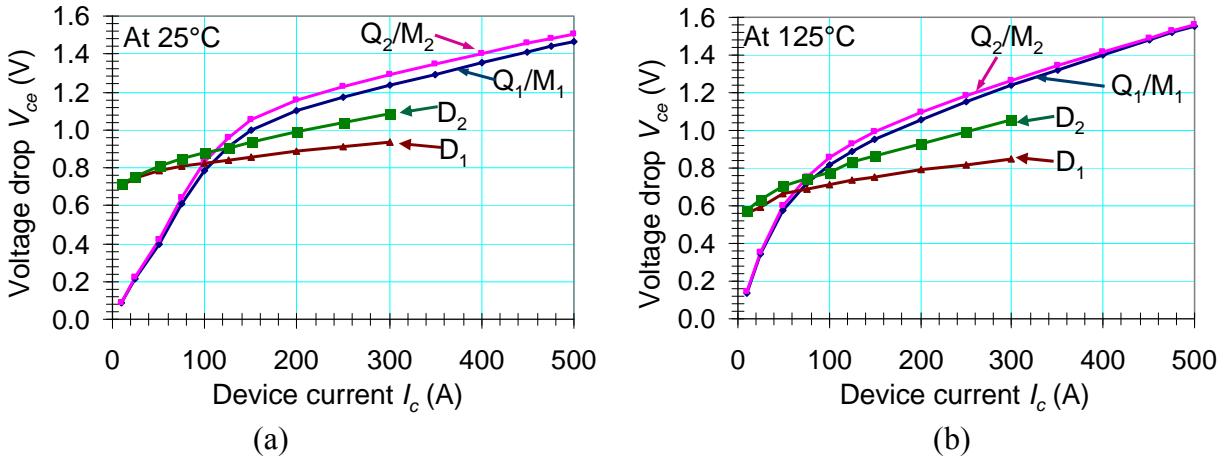


Figure 4.30. Voltage drop of the upper and lower Gen-3 switches at (a) $T_j = 25^\circ\text{C}$ and (b) 125°C as a function of current. Also plotted are the reverse conduction losses of the MOSFET body diodes.

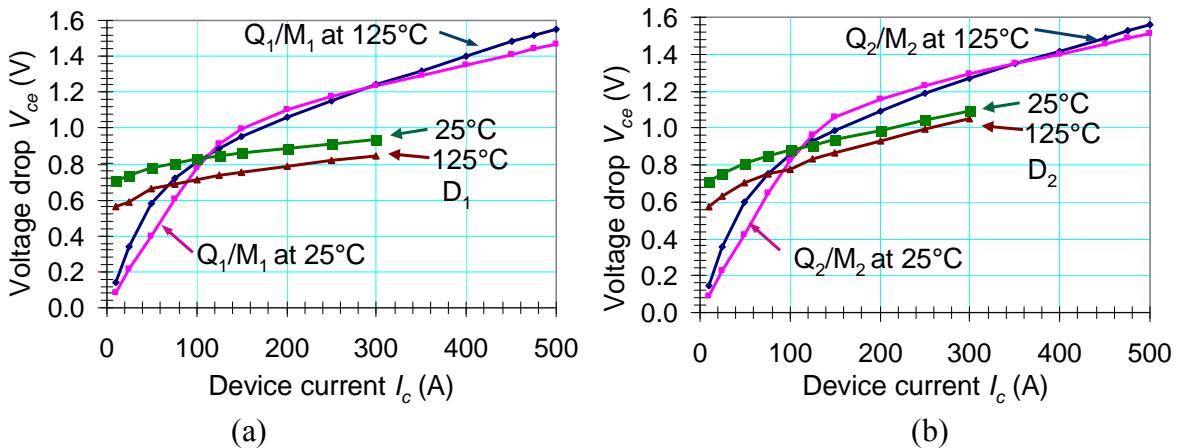


Figure 4.31. Voltage drop of the (a) upper and (b) lower power switches comparing results at $T_j = 25$ and 125°C . Also compared are the reverse conduction losses of the MOSFET body diodes.

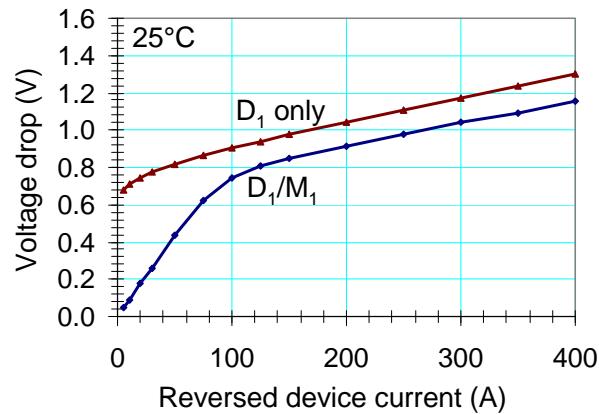


Figure 4.32. Effects of MOSFET channel conduction on the reverse conduction voltage drop comparison between body diode and inclusion of MOSFET channel conduction.

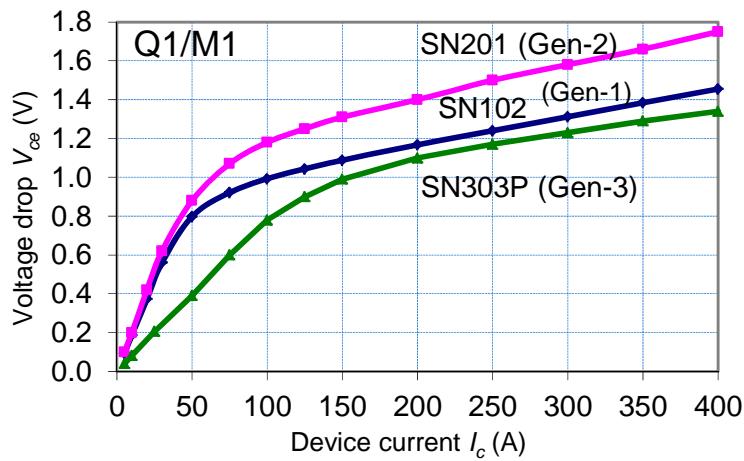


Figure 4.33. Comparison of the forward voltage drops of the three generations of modules.

5. EXPERIMENTAL RESULTS SOFT-SWITCHING INVERTER

5.1. Gen-1 Soft-Switching Inverter

A. Soft-Switching Module Conduction Loss Measurement Results

Table 5.1 shows conduction loss of the main device Q_1-M_1 combination at different temperature conditions. Unlike a conventional IGBT device, which has a fixed voltage drop even at the current near zero, the hybrid switch voltage drop at low currents is proportional to current and at high currents is dominated by the IGBT and increases as the current increases. The rate of increase, however, is much lower than a single IGBT only. It should also be noticed that when the temperature is above 75°C, the voltage drop at high currents tends to be lower. This is because the selected light-punch-through IGBT has a negative temperature coefficient. The current at which the IGBT dominates the conduction voltage drop is at 50 A, where the conduction voltage drop decreases as the temperature increases from 25 to 125 °C. At currents higher than 300 A, the resistive element of IGBT starts showing effect, and the negative temperature coefficient is no longer monotonic.

Table 5.1. Conduction loss measurement of Q_1-M_1 at different temperature conditions

Temperature (°C)	25	75	100	125
Current (A)	V_{cesat} (V)	V_{cesat} (V)	V_{cesat} (V)	V_{cesat} (V)
10	0.186	0.282	0.330	0.375
50	0.798	0.775	0.735	0.688
100	0.992	0.933	0.893	0.844
150	1.088	1.050	1.013	0.967
200	1.168	1.151	1.118	1.077
250	1.240	1.240	1.218	1.177
300	1.312	1.331	1.311	1.277
350	1.384	1.416	1.403	1.371
400	1.455	1.503	1.494	1.467

Figure 5.1 compares the conduction voltage drop between the novel hybrid module and a commercial one. As can be seen, at high temperature 125°C and high current 400 A, the voltage drop of the hybrid module is 1.46 V compared to 1.67 V of the commercial one, which indicates a loss reduction of 14%.

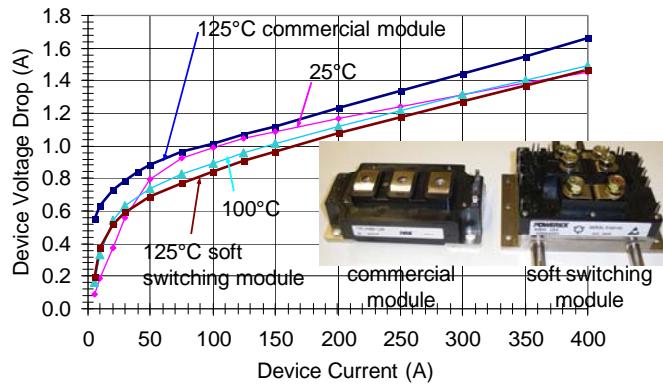


Figure 5.1. Conduction I-V curve comparison between designed module and commercial module.

B. Soft-Switching Module Switching Loss Measurement Results

In order to compare switching losses as a function of temperature, we performed tests at several different coolant temperatures. In each temperature condition, the switching loss was analyzed at the following current conditions: 50 A, 100 A, 150 A, 200 A, 250 A and 280 A. Figure 5.2 shows the switching-on waveforms with 0.1- μ F resonant capacitor at 200-A load current under 25°C and 90°C conditions. For both temperatures, the bus voltage drops to zero first, and then the current rises up. There is no overlap between voltage and current for all load current and temperature cases. In addition, the bus voltage never swings back after reaching zero. So the switching-on energy is essentially zero for all test conditions.

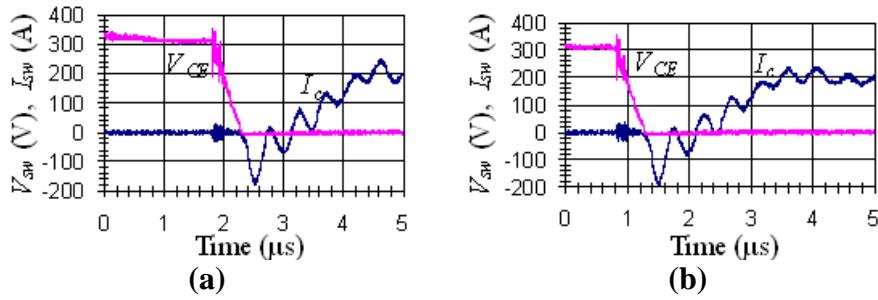


Figure 5.2. Switching-on waveforms with 0.1- μ F resonant capacitance at: (a) 25°C and (b) 90°C.

Note that there is a significant ringing at the beginning of the falling edge of the device voltage. This is because the parasitic inductance inside the module rings with the resonant capacitors when the opposite side diode current is cut off and the diode goes through the reverse recovery process. The snappiness of the CoolMOS body diode worsens the parasitic ringing dramatically. This ringing did not occur in the scaled-down version because a larger resonant inductance was used and the slope of the reverse recovery was not as steep. The solutions to alleviating this parasitic ringing are: (1) further increase resonant inductance, (2) reduce the parasitic inductance in the module to nearly zero, and (3) use a lower voltage drop, but softer recovery diode that would prevent the CoolMOS body diode from conducting. The first method of increasing the resonant inductance has a limit because it will increase the resonant period and thus lengthen the short-pulse elimination period. The second method requires a new module layout that allows the resonant capacitor to sit directly over the chip, reducing the parasitic inductance. It has certain degree of difficulty, but is possible to improve the situation. The third method is ultimately the best solution because it will also allow the main device freewheeling current to go through a diode with a larger die size to ensure proper cooling.

Figure 5.3 shows the detailed switching-off waveforms and energy with 0.1- μ F resonant capacitor at 200-A load current under different temperatures. The switching-off energy increases as the temperature increases. At 25°C, the switching-off energy, E_{off} is 1.6 mJ, and it increases to 3.6 mJ at 90°C. The voltage and current waveforms look similar under the two temperature conditions. The turn-off voltage slew rate (dv/dt) is a function of the resonant capacitance. In this specific case, with 0.1- μ F resonant capacitor, the measured dv/dt at 200 A current is about 1000 V/ μ s and is consistent with the theoretical derivation, which can be simply obtained from $I/(2C_r)$. A larger capacitor will further reduce dv/dt and switching-off energy, and vice versa. The change

of temperature, however, will not affect dv/dt , but will impact the switching energy, as will be explained in the following discussions.

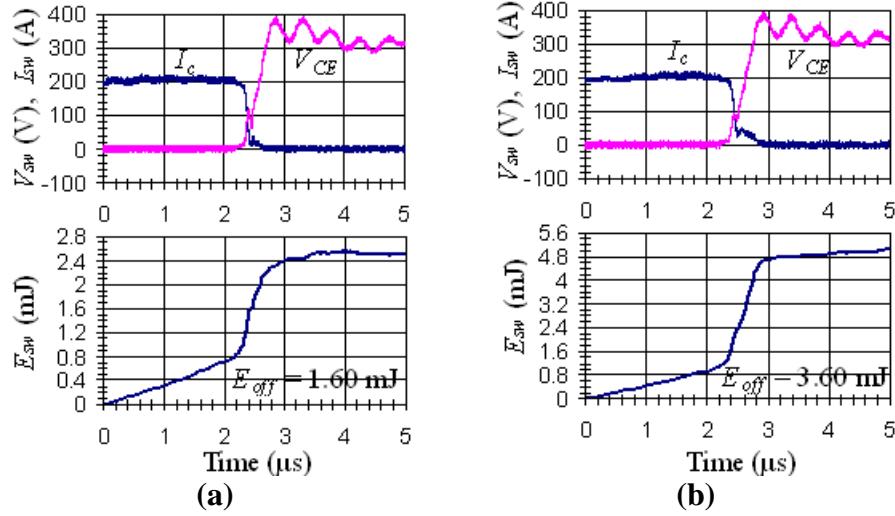


Figure 5.3. Switching-off waveforms with 0.1- μ F resonant capacitance at different temperature conditions: (a) 25°C and (b) 90°C.

Figure 5.4 plots the switching energy as a function of device current and compares the results at 25°C, 50°C, and 90°C temperature conditions with 0.1- μ F resonant capacitance. All the dots were directly from the measurement. The smooth curves were curve-fitted to the following format.

$$E_{on} = hI^k$$

$$E_{off} = mI^k$$

Since switching-on energy is zero for all temperature cases, h and k are all zero here. Switching-off energy increases with temperature rise. The m and k parameters are found as follows.

At 25°C, $h = 0.000061$, $k = 1.9522$

At 50°C, $h = 0.000204$, $k = 1.777$

At 90°C, $h = 0.000777$, $k = 1.60$

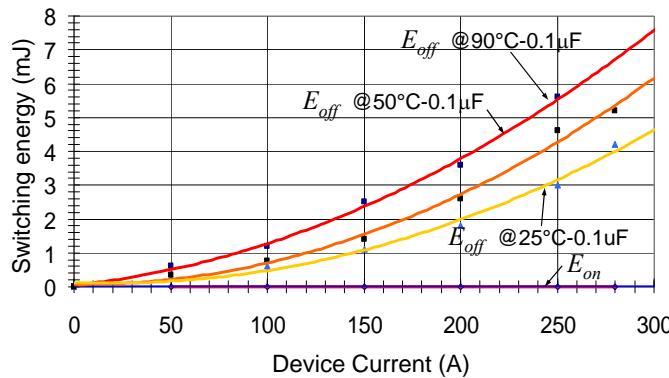


Figure 5.4. Switching energy with 0.1 μ F resonant capacitance at different temperatures.

C. Inverter Power Loss Measurement and Efficiency Prediction Results

Figure 5.5 shows the power loss as a function of the output kVA under different line frequencies and different temperatures: (a) 25°C and (b) 90°C. The figures clearly indicate that the higher line frequency, which represents higher motor speed, the lower power loss. The reason is the voltage level, and thus the power factor, is higher at a higher line frequency. To achieve the same kVA, the case with higher frequency requires less current or produces less power loss.

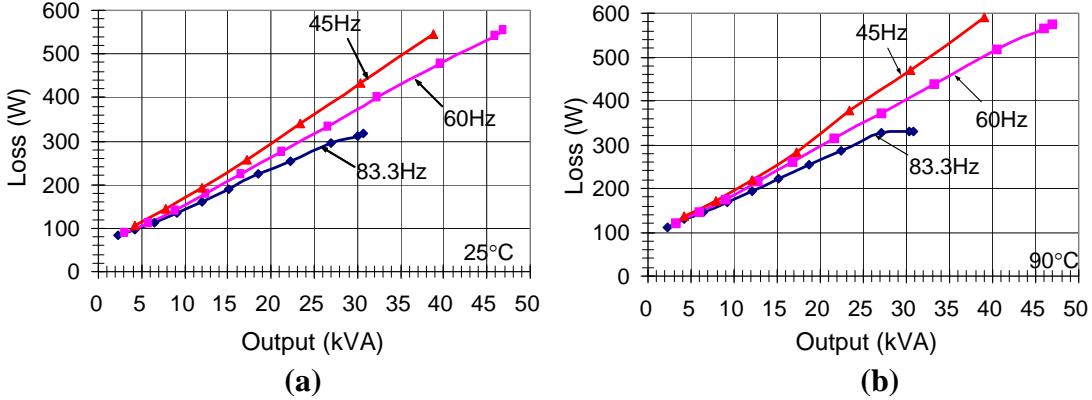


Figure 5.5. Power loss as a function of the output kVA under different line frequencies and different temperatures: (a) 25°C and (b) 90°C.

Figure 5.6 shows the power loss as a function of the output kVA under different temperatures and different line frequencies: (a) 45 Hz and (b) 83.3 Hz. The general trend is the higher temperature, the higher power loss. This indicates that the turn-off loss increases more than the conduction loss decreases. At higher frequency cases, when the modulation index saturates, the loss tends to flatten out, especially at high temperatures, and the loss is less impacted by the temperature. This is because the switching loss is no longer dominating.

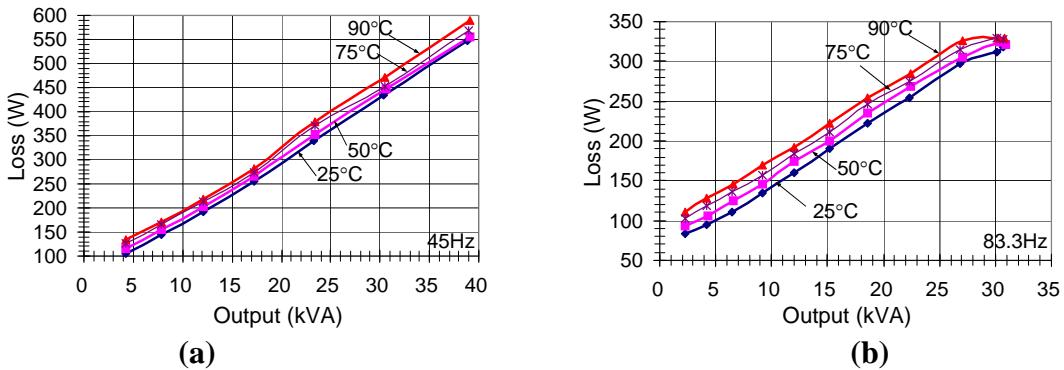


Figure 5.6. shows the power loss as a function of the output kVA under different temperatures and different line frequencies: (a) 45 Hz and (c) 83.3 Hz.

Figure 5.7 shows the projected efficiency based on the inductive load measured loss results at 83.3-Hz output line frequency at different temperatures. The power factor is assumed to be unity in this case. It is noted that at the light load condition, the efficiency decrease with increasing temperature is more obvious than that at the heavy load condition. The reason is that at light loads, the MOSFET shares more current, and with a positive temperature coefficient of the R_{ds-on} , the efficiency suffers. However, at heavy loads, the LPT IGBT shares more current, and with the

negative temperature coefficient, the decrease in efficiency with temperature is not as severe. The peak efficiency approaches 99%.

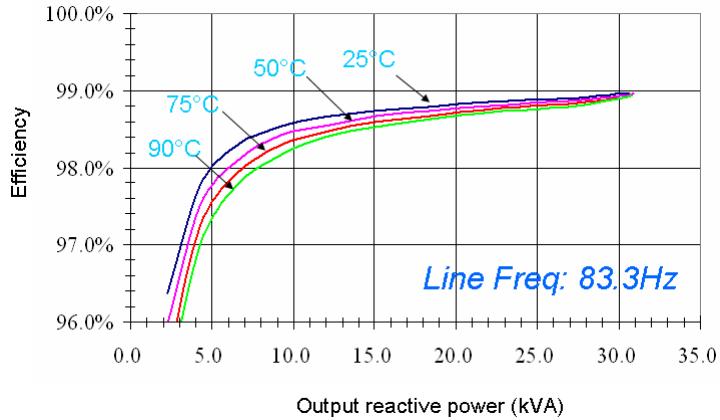


Figure 5.7. Efficiency measurement at 83.3-Hz line frequency and different temperatures.

To compare the efficiency as a function of frequency, the above results are rearranged to compare the projected efficiency at different frequencies under the same temperature condition. Figure 5.8 shows the projected efficiencies for different output line frequencies at 90°C. The power factor in this case is assumed to be 0.83, which is the same as what has been tested for the motor drive cases. As can be seen, at the same output power point, the efficiency is higher at a higher output line frequency. That can be translated into higher speed with higher efficiency, which was proven by later motor tests.

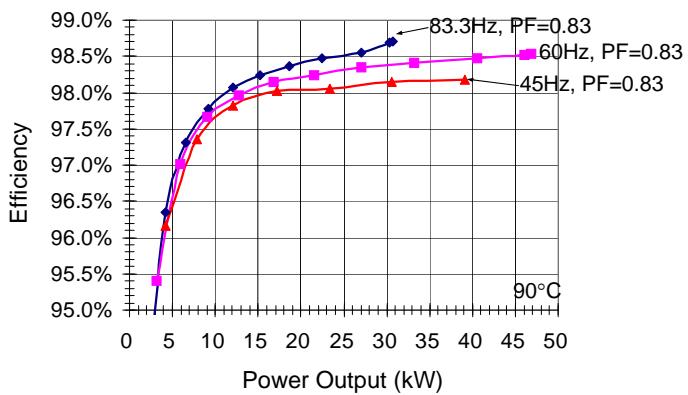


Figure 5.8. Efficiency comparison at 90°C and different line frequency conditions.

D. Inverter Efficiency Test under Motor Load Condition

The motor test setup is the same as that of inductive load except that the load is a motor-dynamometer. We tested the motor at different speed conditions, 1000rpm, 1500rpm and 2000rpm with different output current values, 30A, 40A and 50A at different temperatures, 25°C, 50°C and 75°C. The dynamometer was adjusted to provide the load torque according to motor output current and speed conditions.

Table 5.2 shows the tested inverter efficiency at different speeds and different output currents at different temperatures reflected to power factor 0.83. Due to the limited power supply capacity in the lab, we can only test lower power regions. The high power test will be conducted in the next performance period at Azure Dynamics. As can be seen from Table 5.2, at lower output power, the low-temperature efficiency is slightly higher than the high-temperature one. At higher output power, the high-temperature efficiency catches up and may surpass low temperature one. At higher motor speed and thus higher output frequency, the inverter efficiency is higher than lower speed conditions.

Table 5.2. Efficiency measurement with motor test at different temperatures.

1000rpm (33.3Hz)	75°C		50°C		25°C	
30A	98.1%	9.8kVA	98.2%	9.8kVA	98.3%	9.7kVA
40A	98.2%	14.0kVA	98.3%	14.0kVA	98.4%	14.0kVA
50A	98.3%	18.3kVA	98.3%	18.3kVA	98.4%	18.3kVA
1500rpm (50Hz)	75°C		50°C		25°C	
30A	98.3%	12.1kVA	98.5%	12.1kVA	98.6%	12.2kVA
40A	98.6%	17.4kVA	98.6%	17.4kVA	98.7%	17.4kVA
2000rpm (66.6Hz)	75°C		50°C		25°C	
30A	98.8%	13.7kVA	98.9%	13.7kVA	98.9%	13.7kVA

Figure 5.9 shows the efficiency profile of the soft-switching inverter under motor-dynamometer test at 25°C coolant condition. The motor was tested with different modulation indexes until the power supply reached its limit. For this plot, the measurements at 0.4 power factor were used to project the efficiency at 0.83 power factor. The measurement results show a consistent trend that the higher power factor, the higher efficiency and the higher speed, the higher efficiency. At higher speeds, the motor terminal voltage is also higher, and for the same current, the loss is less. The efficiency profile shows the inverter efficiency is close to 99% even when the speed is still below its nominal 2500 rpm. This projected result is consistent with what has been tested using the calorimeter at 2800 rpm, at which the efficiency is 99.1%.

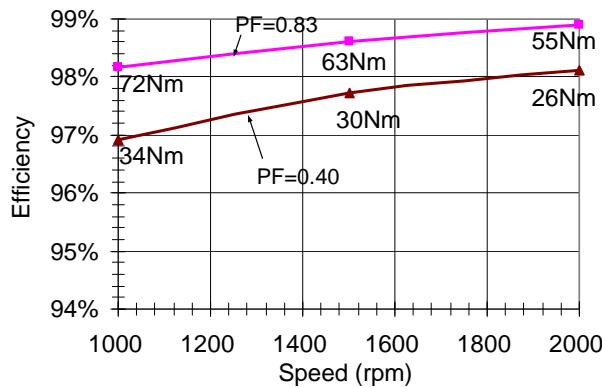


Figure 5.9. Efficiency profile of the soft-switching inverter under motor-dynamometer test.

Table 5.3 shows the efficiency comparison between inductive load test and motor test. The efficiency with inductive load is projected from a power factor of 0.83. At the same output power, the motor test efficiency is higher than the pure inductive load test efficiency. The reason is during motor-dynamometer test, the current is mainly conducting through MOSFET and IGBT channels, while in inductive load test, the duty cycle of the anti-parallel diodes increases, and the efficiency suffers slightly. Previous inductive load tests show that at 83.3Hz (30.6kVA), the efficiency is 98.8%; and at 60Hz (46.8kVA), the efficiency is 98.6%. Therefore, the peak efficiency at higher motor load can be expected to exceed 99%.

The above measurement using our power meter becomes inaccurate when the power is further increased because the instrumentation is not well calibrated at these higher power levels. Table 5.4 lists the power meter readings at 30-minute intervals for the 27-kW, 1600-rpm machine output condition. Such a low-speed machine tends to draw larger current than the same power level case with a high-speed machine. In Table 4, the inverter efficiency reading at 4:00pm was exceeding 100%. This clearly indicates that power meter reading is inaccurate and should not be used for the efficiency index. Its voltage and current readings, however, can be used as the reference for the power level.

Table 5.3. Efficiency comparison between inductive load and motor test at different temperatures.

	75 °C		50 °C		25 °C	
50Hz/motor	98.3%	12.1kVA	98.5%	12.1kVA	98.6%	12.2kVA
45Hz/inductor	97.9%	12.1kVA	98.0%	12.1kVA	98.1%	12.1kVA

	75 °C		50 °C		25 °C	
66.6Hz/motor	98.8%	13.7kVA	98.9%	13.7kVA	98.9%	13.7kVA
60Hz/inductor	98.1%	13.7kVA	98.2%	13.7kVA	98.3%	13.7kVA

Table 5.4. Readings from power meter at 1600 rpm, 27 kW condition

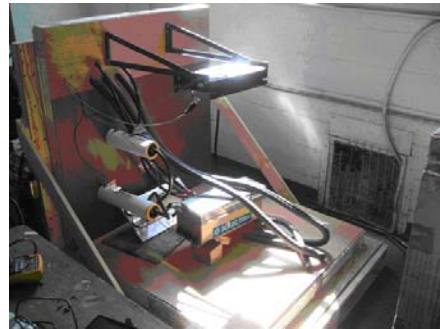
Time	V_{dc} (V)	I_{dc} (A)	P_{inv} (kW)	I_a (A)	I_b (A)	I_c (A)	P_{inv} (kW)	η_{inv}
3:00pm	324	84.92	27.54	91.00	90.80	90.50	26.85	97.5%
3:30pm	325	83.55	27.12	91.00	90.00	90.00	26.55	97.9%
4:00pm	322	82.90	26.69	89.70	89.50	89.10	26.90	100.8%

E. Inverter Efficiency Test with Calibrated Calorimeter

To more accurately measure efficiency, a differential calorimeter has been constructed and calibrated. Figure 5.10 shows photographs of the differential calorimeter setup. Figure 5.10(a) shows the small reference chamber in foreground and the main chamber partially open in the back. Figure 5.10(b) shows the main chamber with the cover removed to see the coolant inlet and outlet. The DC bus and AC output cables passing through the chamber wall can also be seen. A stirring fan, seen at the top of the picture, is to ensure uniform temperature distribution inside the chamber.



(a)



(b)

Figure 5.10. Photographs showing (a) differential-chamber based calorimeter with flow meter box in foreground and inverter chamber partially open in back; (b) main chamber cover removed for the view of coolant inlet and outlet.

The calorimeter test was performed for more than five hours to ensure that the thermal condition reached its steady state for each test point. Figure 5.11 shows the coolant temperatures and the measured inverter efficiency at 27 kW. Different speeds tend to have different power factor were tested. The test was conducted with an MG set with machine rated 90 kW and 1600 rpm. The test was conducted at a higher power output, 27 kW, which is about 50% of the peak power. The power factor is 0.78, and the steady-state efficiency is 98.8%.

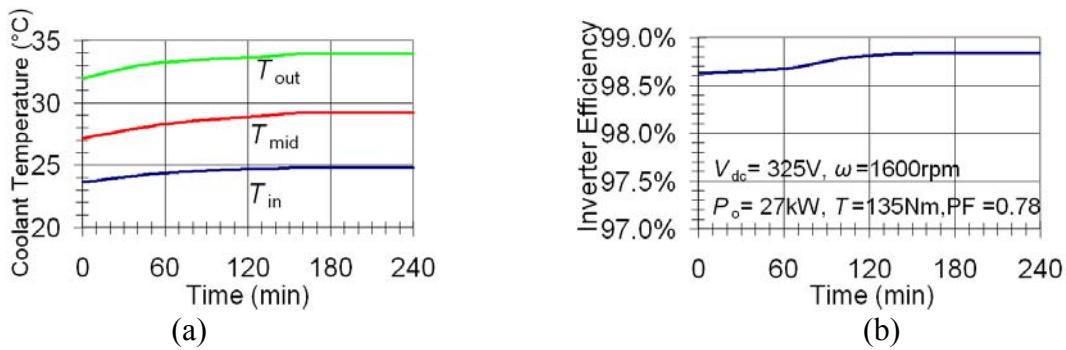


Figure 5.11. Calorimeter measurement at 27kW: (a) coolant temperatures, (b) inverter efficiency.

F. Improve Design with Failure Mode Effect Analysis

The Failure Mode Effects Analysis (FMEA) is a tool commonly used by the automotive industry but was developed from techniques started in the high reliability aerospace area. Its purpose is to identify potential problems and to insure that adequate consideration has been given to each. The possible consequences of a failure are identified and severity rankings are given to each issue. Our goal was to complete a quick FMEA on the power stage alone. A production design would have each piece of the overall system analyzed in detail, but in the interest of getting useful feedback while still in the design phase only the aspects of the inverter that would not be present in a conventional six-switch setup were analyzed. The following analysis shows the currents and voltages for a successful and two failed commutations. The failed commutations can be categorized in to two cases.

1. Q_{x1} opening after D_2 stops conduction, when the resonant current has reached its peak.
2. Q_{x1} opening before D_2 stops conduction, i.e. during the linear phase of the resonant current ramp-up.

Case 1 results in the worst-case peak current for D_{x5} , however the current decays quickly. Case 2 is different. The worst-case diode current is not as high as for case 1, however, the current decays very slowly (as the voltage across the coupled inductor is zero). This suggests that D_{x5} and D_{x6} cannot be 5-A diodes and possibly not even 50-A. Figure 5.12 shows the simulation diagram using MicroCap Ver. 9.

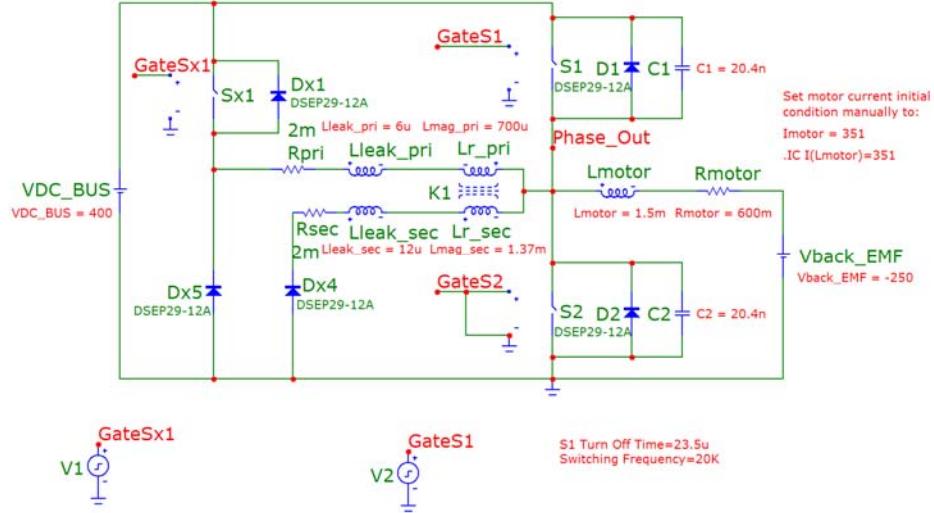


Figure 5.12. Simulation diagram using MicroCap.

Figure 5.13 shows the simulated resonant inductor voltage and current waveforms under normal operation. The top two traces are the gate signals for main (V_{GATESI}) and auxiliary ($V_{GATESX1}$) switches. The middle five traces are the motor line current (I_{LMOTOR}), the primary side resonant inductor current (I_{LEAK_PRI}), the secondary side resonant inductor current (I_{LEAK_SEC}), the clamping diode current (I_{Dx5}), and the total resonant current ($I_{LEAK_PRI}+I_{LEAK_SEC}$). The bottom two traces are output phase voltage (V_{PHASE_OUT}) and the voltage across the secondary side of the resonant inductor ($V_{LEAK_sec} + V_{LEAK_sec}$). Notice that the clamping diode current I_{Dx5} in the middle graph sees very little current during the normal commutation condition.

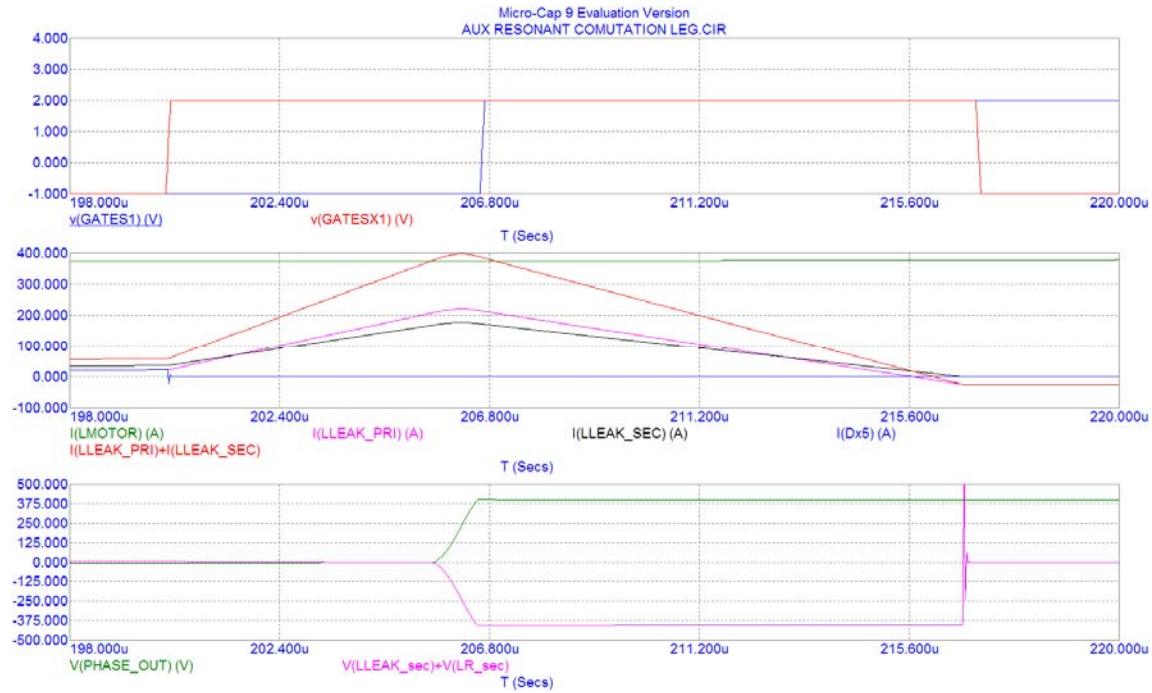


Figure 5.13. Resonant inductor voltage and current under normal operation.

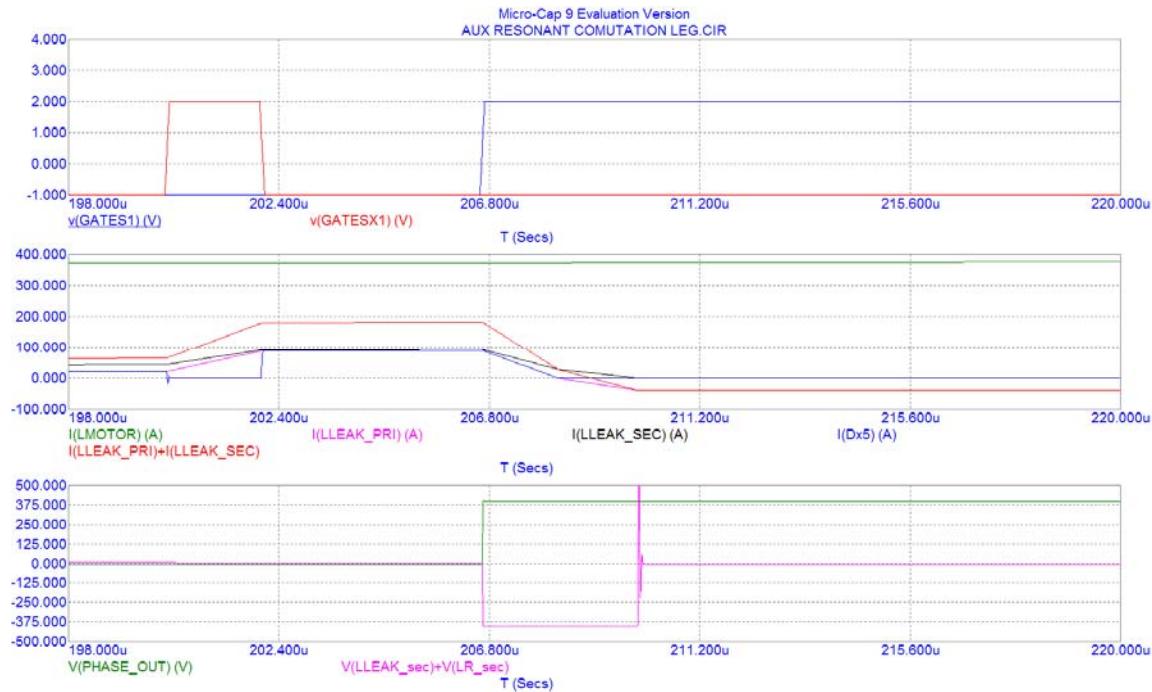


Figure 5.14. Simulated resonant inductor voltages and currents under communication failure.

Figure 5.14 shows the simulated results under the failure of communication between the inverter interface and DSP controller (Case 2 above). At time 202 μ s, the auxiliary switch gate signal is interrupted due to loss of communication. In this case, the resonant current is interrupted, and the clamping diode current I_{Dx5} is equal to the primary resonant current until the main switch gate

is turned on. A peak current of 90 A flows through the clamping diode for about 3 μ s. This suggests that a 5-A rated diode is inadequate to handle such a failure mode condition.

A communication failure can also cause the interruption of the main gate signal. Figure 5.15 shows the simulation result with loss of communication that interrupts the auxiliary and main gate signals. In this case, the clamping diode will conduct a high current for a long period, which is clearly exceeding its 5-A capability. Therefore, this FMEA study suggests that a much higher rated diode is required for the clamping diode.

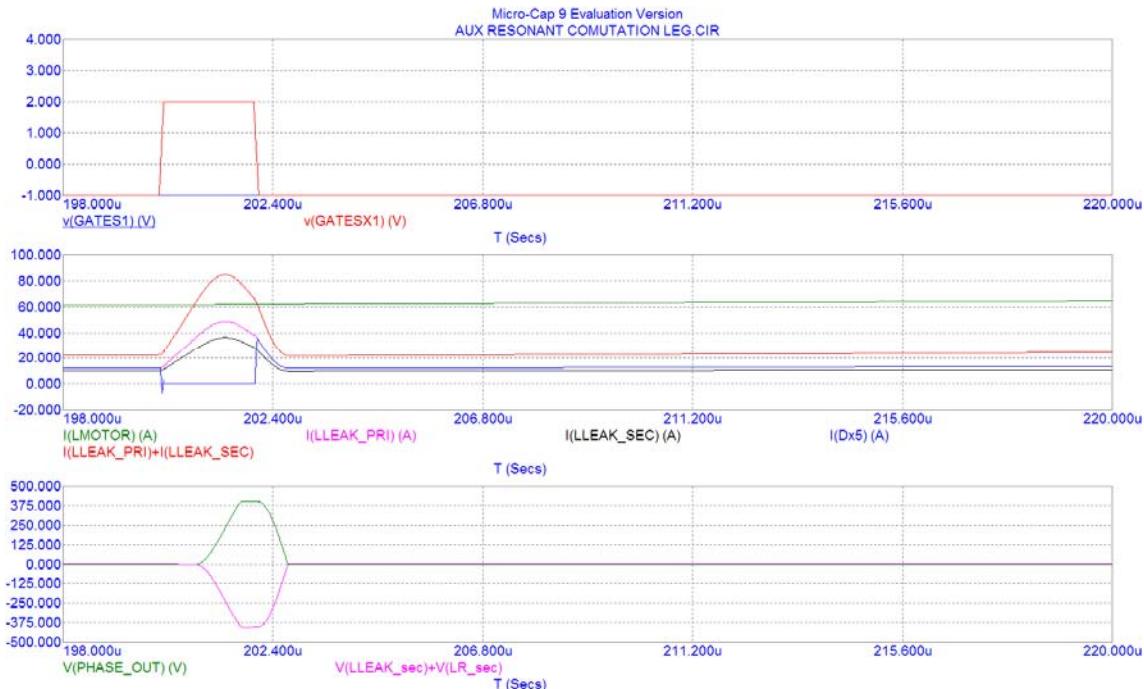


Figure 5.15. Simulation result with loss of communication that interrupts the auxiliary and main gate signals.

G. Test EMI Performance

Figure 5.16 shows the schematic diagram of EMI measurement setup that includes a set of line impedance separation networks (LISN), the inverter under test, and the load. The measurement instrument needs to have frequency-domain analysis capability. Both dc source side and ac load side EMI and differential-mode (DM) and common mode (CM) performances are measured to see the difference of EMI performance between hard-and soft-switching inverters. The source side current sensing comes from two LISN outputs, and the load side current sensing comes from a Rogowski probe that encloses all three cables that go into the load. The DM output EMI is not measured because it is the inherent load current that should not be different between hard- and soft-switching inverter.

Figure 5.17 compares DM noise at dc source side in the high-frequency region, from 0 to 50 MHz. The bottom traces of hard-switching and soft-switching results represent the measured EMI on the two differential lines, or I_{dc+} and I_{dc-} . By subtracting these two lines from each other, the total noise is the DM noise, which is shown in the top trace. Since the scale is much above

the base switching frequency of 10 kHz, the soft-switching inverter is shown to be more effective at diode reverse recovery and parasitic related EMI noise reduction. By looking at the top traces of hard- and soft-switching inverter noises, the soft-switching inverter apparently lowers the EMI noise by 10 to 20 dB across the entire frequency range. The main noise reduction regions are in between 2 and 8 MHz and between 18 and 27 MHz, where 20-dB reduction by soft switching is clearly identifiable. There are two possible noises that tend to be pronounced in the hard-switching inverter: (1) diode reverse recovery related EMI noise and (2) layout and parasitic component related EMI noises. The dc link capacitor needs to have very low equivalent series resistance (ESR) and equivalent series inductance (ESL) to effectively suppress these high frequency noises. In terms of which noise source is located in which region is still unknown, but the soft switching has demonstrated a significant EMI reduction advantage on the dc source side.

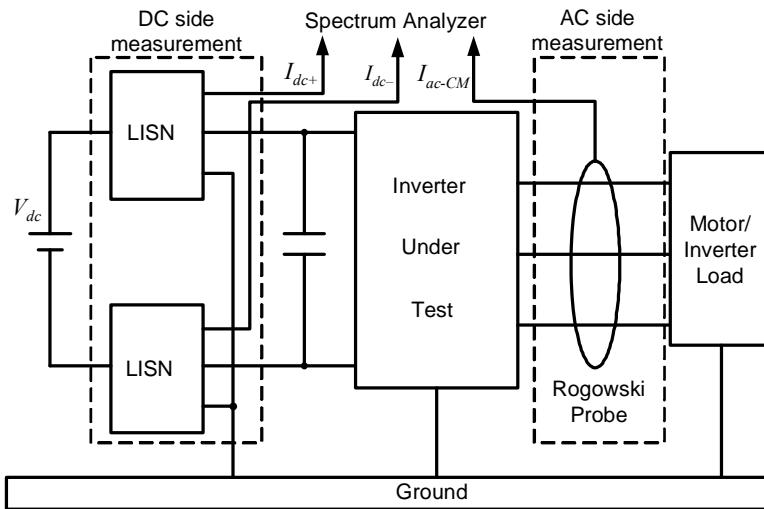


Figure 5.16. Schematic Diagram of EMI Measurement Setup.

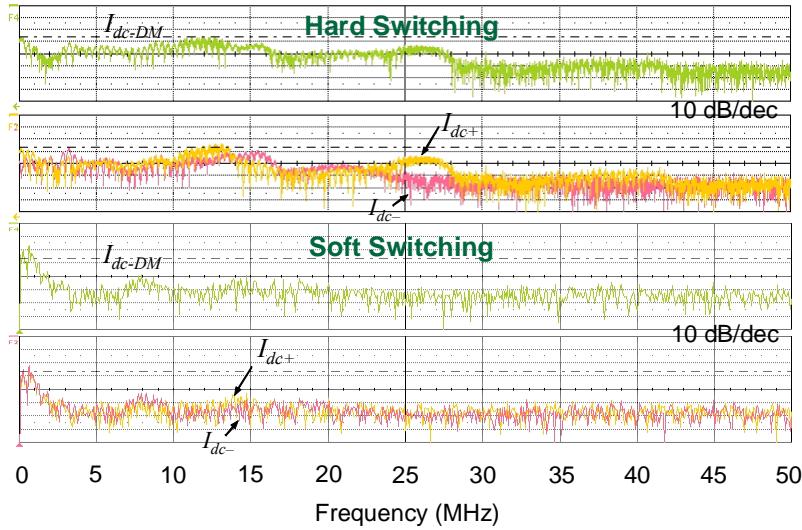


Figure 5.17. Measured High Frequency Range DM Noise at DC Side.

Figure 5.18 compares the CM noise at the dc source side in the high-frequency region. The bottom traces of the hard-switching and soft-switching results represent the measured EMI on

the two differential lines, or I_{dc+} and I_{dc-} . By adding these two lines together, the total noise is the CM noise, which is shown by the top trace. Similar to the DM noise reduction, the main noise reduction regions are spread around certain frequencies. In this case, significant noise reduction is shown between 2 and 7 MHz, between 9 and 15 MHz, and between 17 and 28 MHz regions, where more than 10-dB reduction by soft switching is clearly identifiable. Again, in terms of which noise source is present in which region is still unknown, but soft switching has demonstrated significant CM EMI reduction advantage on the dc source side.

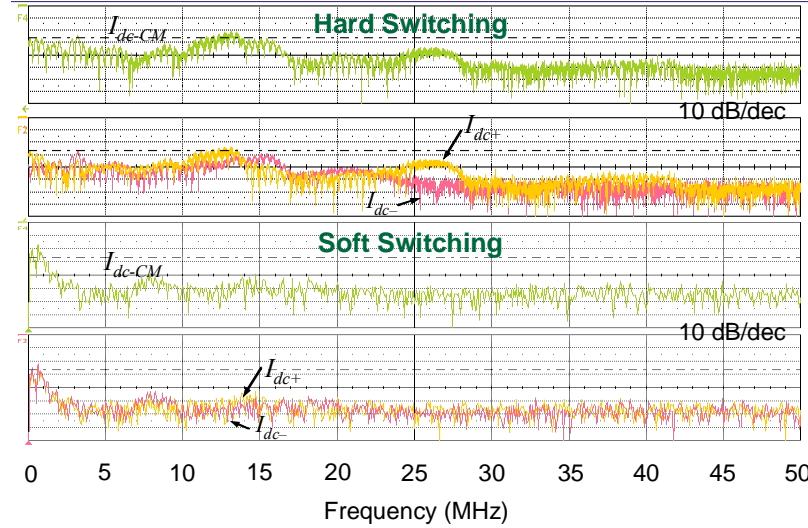


Figure 5.18. Measured High Frequency Range CM Noise at DC Side.

Figure 5.19 compares the ac load-side EMI performance of the hard- and soft-switching inverter in the high-frequency region. Since the low-frequency component is related to the load current, there is not a significant difference between hard and soft switching. At high frequencies, however, the soft-switching inverter demonstrates significant EMI noise reduction. The main noise reduction regions are between 2 and 7 MHz and 13 and 18 MHz, in which more than 10-dB reduction is realized.

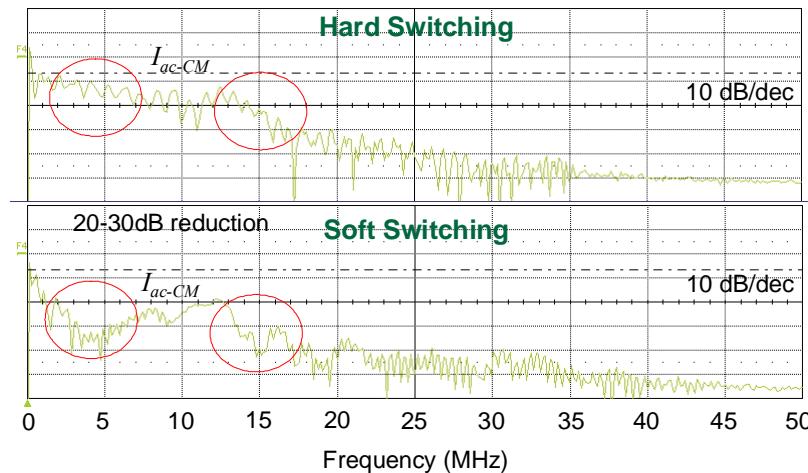


Figure 5.19. Measured High Frequency Range CM Noise at AC Side.

5.2. Gen-2 Soft-Switching Inverter

A. Conduction Loss Measurement Results

Figure 5.20 compares the voltage drop between Gen-1 and Gen-2 modules. SN102 and SN201 represent the Gen-1 number 2 prototype and Gen-2 number 1 prototype, respectively. Both upper device (Q_1/M_1) and lower device (Q_2/M_2) clearly show higher voltage drops on the Gen-2 module. For Gen-1, the measurement points are at the power terminals, which are supposed to be far away from the chip. However, the heavy copper bar does not introduce any appreciable voltage drop. For Gen-2, even though the measurement points are near the chip, the voltage drops are high due to the substrate current path resistance. The upper device is worse because its substrate path is narrower. The lower device voltage drop matches that of the Gen-1 module, but its low current region shows a higher voltage drop because the CoolMOS™ is far away from the measurement point. When measuring from the power terminals, the Gen-2 voltage drop is significantly higher than that of the Gen-1 module. Unlike measuring near the chip, the measurement at the terminal indicates a higher voltage drop on the lower device. This can be explained by looking at the internal layout of the module, where the lower device has an additional length of the substrate.

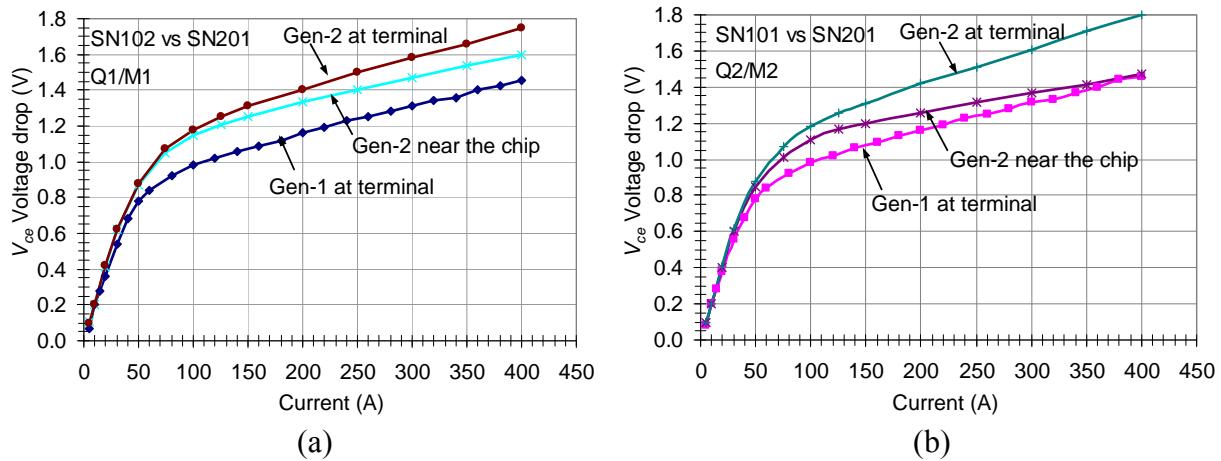


Figure 5.20. Voltage drop comparison between Gen-1 and Gen-2 modules: (a) upper device and (b) lower device.

In order to ensure that the above voltage drop problem is not caused by measurement error, an additional Gen-2 module prototype, SN210, was measured to compare the results obtained with SN201. Figure 5.21 compares the measured upper device voltage drops near the chip between SN201 and SN210. The difference between these two prototypes is negligible, and the voltage drop of the Gen-2 design is apparently a major issue with inverter efficiency reduction.

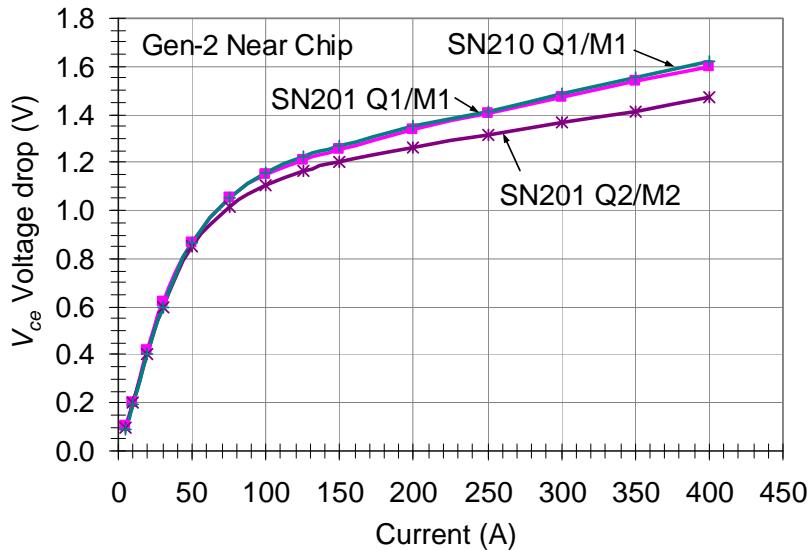


Figure 5.21. Comparison of Gen-2 module prototypes.

To further verify the Gen-2 device voltage drop issue, a production scale Gen-2 module SN211 is compared against the prototype SN201 in Figure 5.22. For comparison purposes, the voltage drops of upper and lower devices of the Gen-1 module are plotted as the base lines. Both lines are overlapped each other, indicating the balance and symmetrical structure of the Gen-1 design. For Gen-2 modules, the voltage drops measured near the chips of SN211 and SN201 are nearly the same and are all significantly higher than the voltage drop measured at the power terminals of the Gen-1 module.

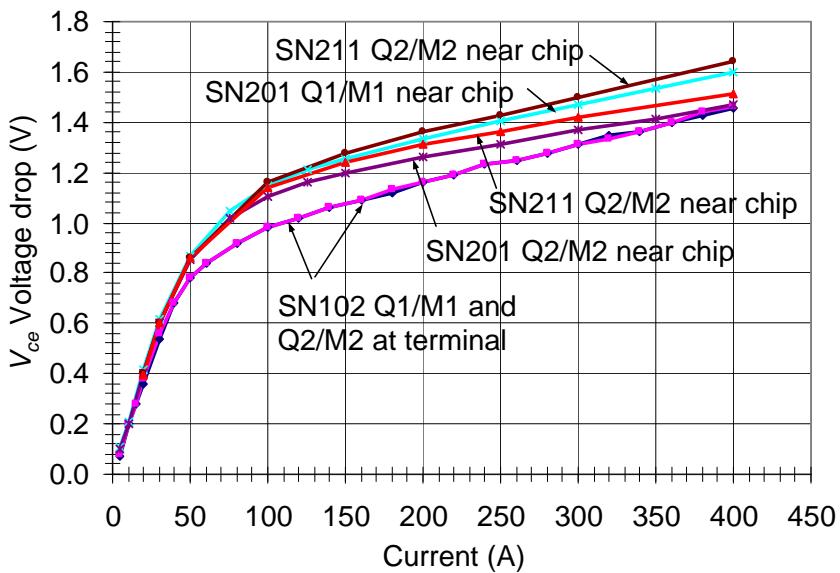


Figure 5.22. Device voltage drop comparison between Gen-1 and Gen-2 modules.

B. Switching Characterization

The Gen-2 module showed much clearer voltage and current waveforms during switching transitions. Thanks to the new internal layout, the parasitic inductance of the Gen-2 module has been significantly reduced. The peak switching current has been tested at 400-A, the desired current under full-rated power condition. The comparison between Gen-1 and Gen-2 module performances is shown in this section, including switching characteristics waveforms and calculated parasitic inductance. Figure 5.23 shows the switching test setup. The test parameters are as follows:

- C_1, C_2 : 0.1 μF , 600V dc; C_3 : 4.7 $\mu\text{F} \times 2$, 630V dc (4.7 $\mu\text{F} \times 5$ for 300A or more)
 - C_4 : 150 μF , 500V dc; C_5 : 16mF, 430V dc
 - L : 240 μH , 260 A rms
 - L_{coupled} : $L_s=540 \mu\text{H}$, $L_p=293 \mu\text{H}$, $L_{\text{lkp}}=3.00 \mu\text{H}$, $N_s=19\text{T}$, $N_p=14\text{T}$, ETD 49#

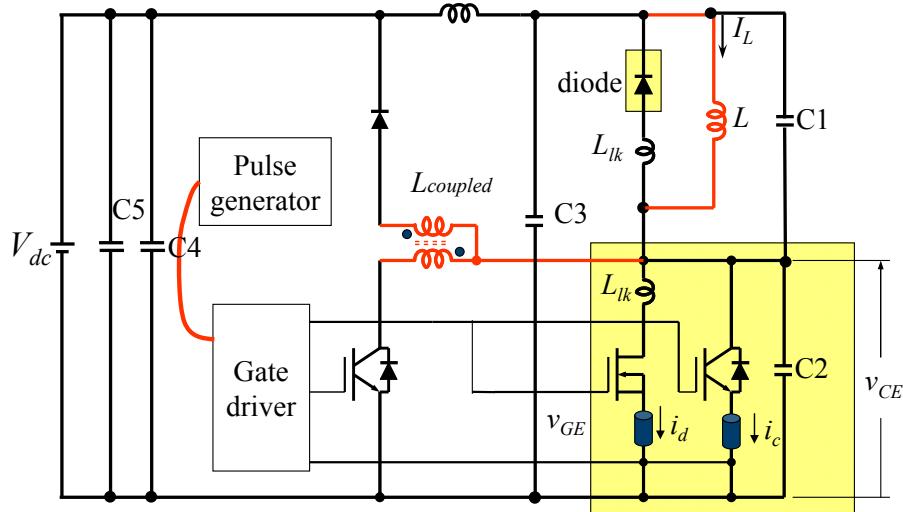


Figure 5.23. Switching characteristic test setup.

Due to the internally-connected power pin E₁/C₂ for Gen-2 module, it is not possible to measure device current for one switch and diode current of the opposite switch independently. Therefore, we measured load current I_L instead for the switching characterization.

The Gen-1 module was only tested up to 280-A load current due to severe parasitic ringing. For the Gen-2 module, the switching current was quite clean, and thus the 400-A full-rated current was tested successfully. Figures 5.24 to 5.26 compare the switching characteristics between Gen-1 and Gen-2 modules at different load current conditions. The left-side waveforms came from Gen-1 module, while the right-side waveforms were generated from Gen-2 module.

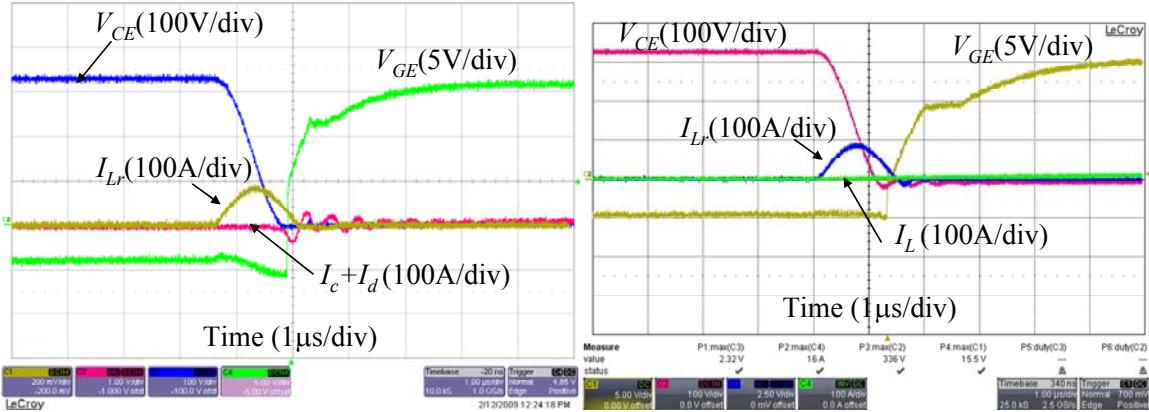


Figure 5.24. Zero load current switching characterization waveforms (left side-Gen 1 module, right side-Gen 2 module).

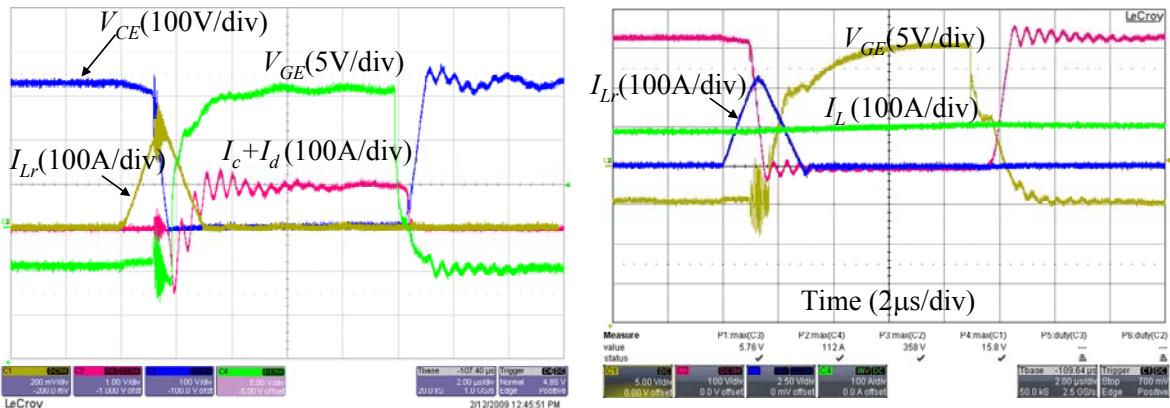


Figure 5.25. 100A load current switching characterization waveforms (left side-Gen 1 module, right side-Gen 2 module).

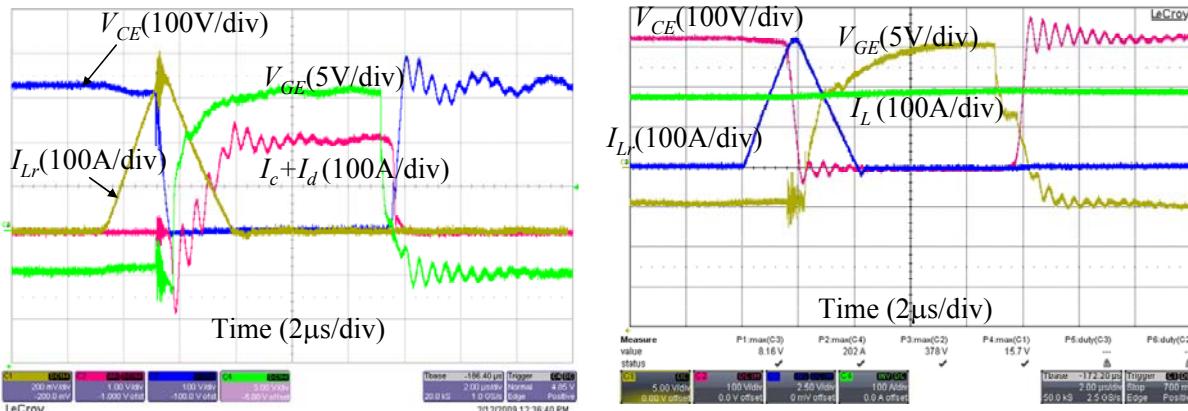


Figure 5.26. 200A load current switching characterization waveforms (left side-Gen 1 module, right side-Gen 2 module).

Figures 5.27 and 5.28 showed the performance of Gen-2 module at load current 300 and 400 A conditions. Note that Gen-1 module could not be pushed to these current levels due to severe parasitic ringing.

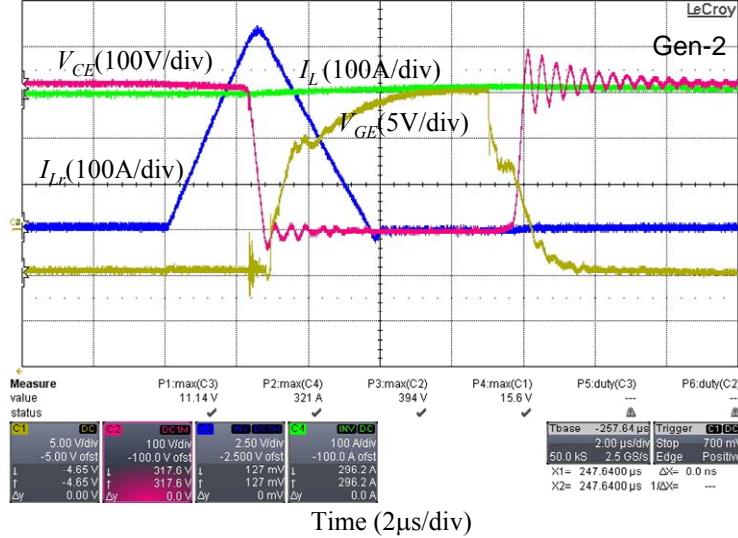


Figure 5.27. 300A load current switching characterization waveforms (Gen 2 module).

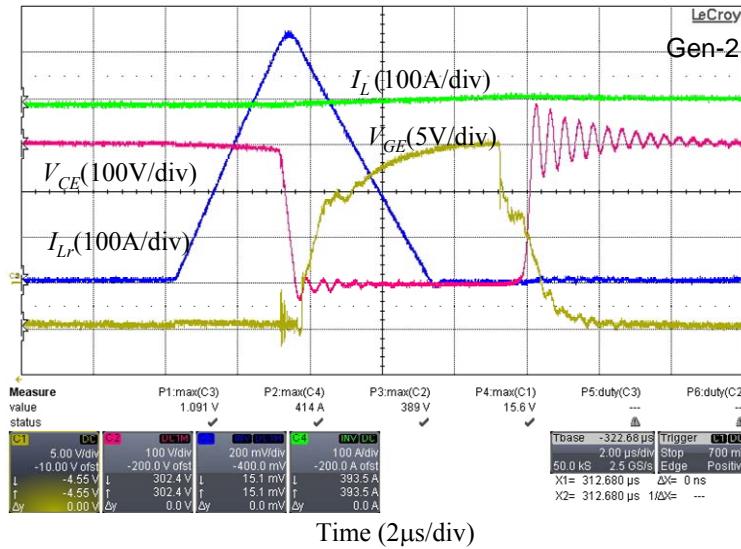


Figure 5.28. 400A load current switching characterization waveforms (Gen 2 module).

From the comparison, we can clearly see that switching transition of Gen-2 module is much improved compared to Gen-1 module. The ringing of voltage and current is greatly reduced. In order to quantify the parasitic improvement, we estimated the parasitic inductance for Gen-2 module by measuring the voltage drop during current rise stage. Figure 5.29 shows the measurement point at 300-A case.

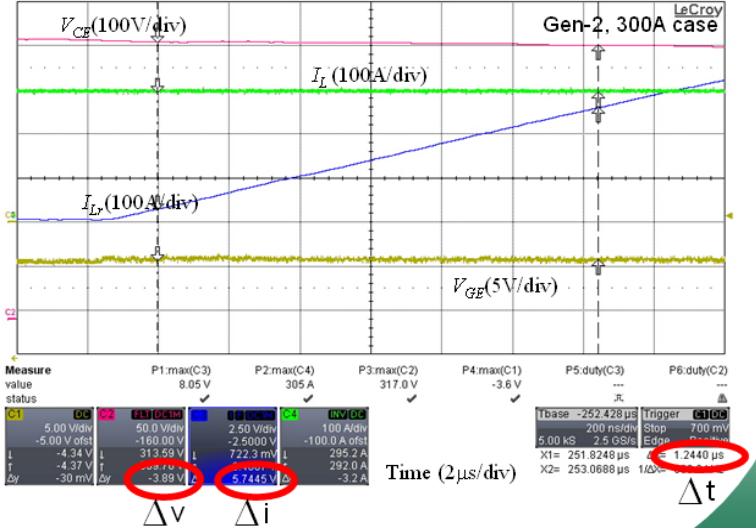


Figure 5.29. Parasitic inductance measurement at 300-A load current case.

The parasitic inductance can be calculated by the equation below:

$$L_{para} = \frac{\Delta v \cdot \Delta t}{\Delta i}$$

Through the repetitive measurements at conditions under 250 and 300-A, the parasitic inductance were estimated and shown in Table 5.5. The results indicate that the measurement results are quite consistent under the same current condition. By taking the average over all six measurement results, the parasitic inductance of Gen-2 module is estimated at 19.4 nH. With the same measurement and estimation method, the parasitic inductance of Gen-1 module was estimated at 90.5 nH. This represents an impressive parasitic reduction, or 78.5% reduction. Note that the current was measured with a Rogowski coil, which has a reading of 40 A/V. Its initial reading is in voltage, which needs to be converted to a current value.

Table 5.5. Gen-2 module parasitic inductance measurement.

Δt (μs)	Δi (V)	Δi (A)	Δv (V)	L_{para} (nH)	Load current
1.1052	5.1629	206.516	3.33	17.8209	250A
1.1052	5.1582	206.328	3.39	18.1586	250A
1.1052	5.1351	205.404	3.42	18.4017	250A
1.2440	5.7445	229.780	3.89	21.0599	300A
1.2440	5.7429	229.716	3.66	19.8203	300A
1.2440	5.7113	228.452	3.94	21.4546	300A

C. Power Loss Measurement Results

Due to limited active power supply capability in the lab, the Virginia Tech only performed the inductive load test in order to push to higher output voltage and current conditions. The reactive

power kVA and the line frequency represent the output power and speed of the motor load, and their losses are in the similar scale. Therefore, it is reasonable to project the efficiency with a reactive power test. The load is a Δ -connected three-phase inductor. Equivalent inductance is about 4.5mH per phase. By controlling the modulation index, the output voltage, and thus the output reactive power can be controlled. The dc bus voltage was fixed at 325V, and the output line frequencies varied at 45Hz, 60Hz and 83.3Hz. Temperature was regulated at four different conditions: 25°C, 50°C, 75°C and 90°C.

Figure 5.30 shows the power loss as a function of the output kVA under different line frequencies and different temperatures: (a) 25°C, (b) 50°C, (c) 75°C, and (d) 90°C. The figures clearly indicate that the higher line frequency, which represents higher motor speed, the lower power loss. The reason is the voltage level, and thus the power factor is higher at a higher line frequency. To achieve the same kVA, the case with higher frequency requires less current or produces less power loss.

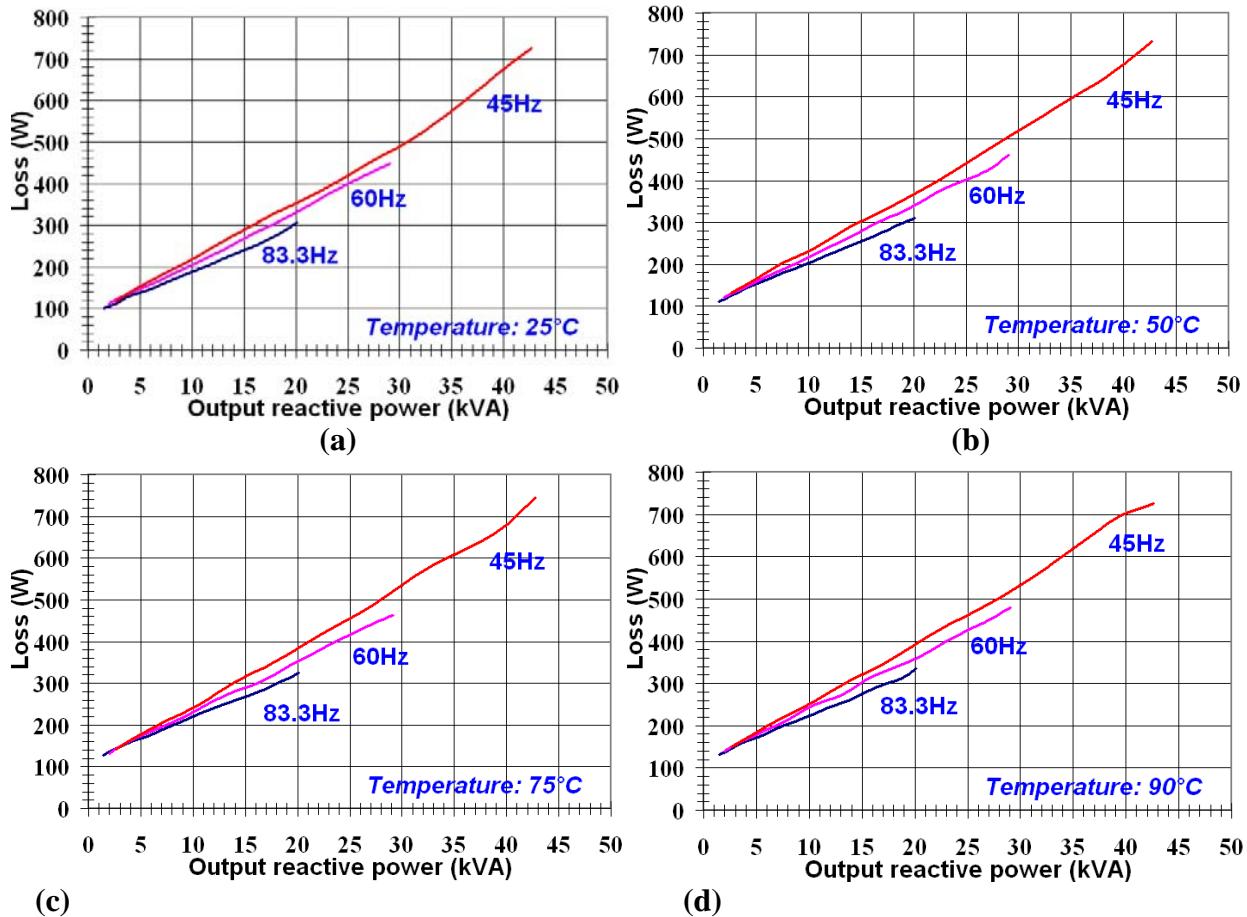


Figure 5.30. Power loss as a function of the output kVA under different line frequencies and different temperatures: (a) 25°C, (b) 50°C, (c) 75°C, and (d) 90°C.

Figure 5.31 shows the power loss as a function of the output kVA under different temperatures and different line frequencies: (a) 45 Hz, (b) 60 Hz, and (c) 83.3 Hz. The general trend is the higher temperature, the higher power loss. This indicates that the turn-off loss

increases more than the conduction loss decreases. At higher frequency cases, when the modulation index saturates, the loss tends to flatten out, especially at high temperatures, and the loss is less impacted by the temperature. This is because the switching loss is no longer dominating.

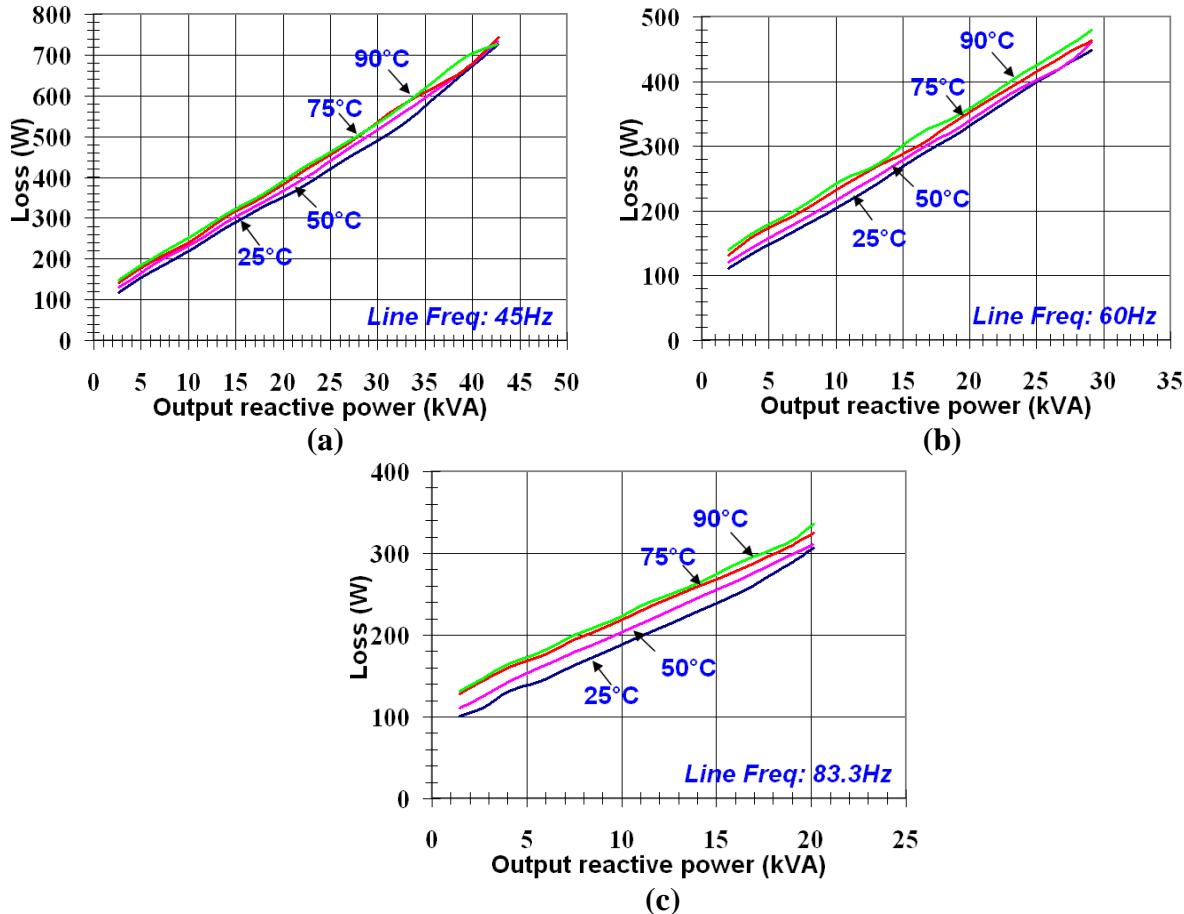


Figure 5.31. Power loss as a function of the output kVA under different temperatures and different line frequencies: (a) 45 Hz, (b) 60 Hz, and (c) 83.3 Hz.

C. Projected Efficiency Using the Loss Measurement Results

Figure 5.32 shows the projected efficiency based on the inductive load measured loss results at 83.3-Hz output line frequency at different temperatures. The power factor is assumed to be unity in this case. It is noted that at the light load condition, the efficiency difference is more obvious than that at the heavy load condition. The reason is that at light loads, the MOSFET shares more current, and with positive temperature coefficient, the efficiency suffers. However, at heavy loads, the LPT IGBT shares more current, and with the negative temperature coefficient, its efficiency impact by temperature is not as severe. The peak efficiency approaches 98.5%.

Figures 5.33 and 5.34 show the projected efficiency based on the inductive load measured loss results at 60-Hz and 45-Hz output line frequencies at different temperatures. The power factor is

again assumed unity in this case. The efficiency differentials at light and heavy loads show the same trend as those in the 83.3 Hz case. Overall efficiency reduces as the frequency reduces because of poorer power factor and less modulation index at the same load condition.

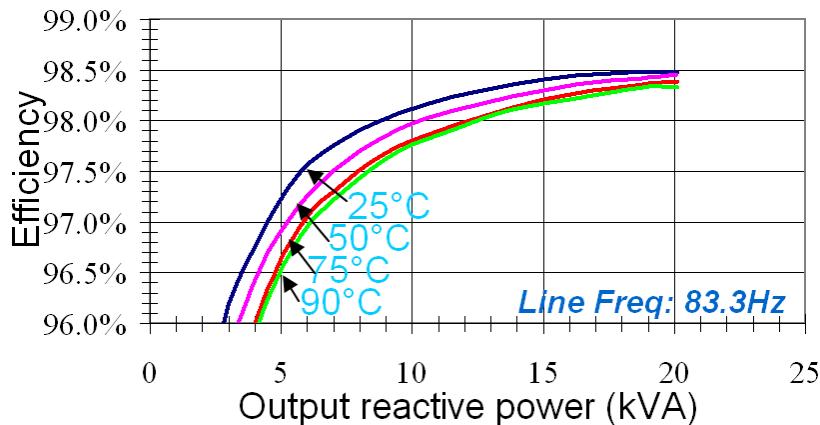


Figure 5.32. Efficiency measurement at 83.3-Hz line frequency and different temperatures.

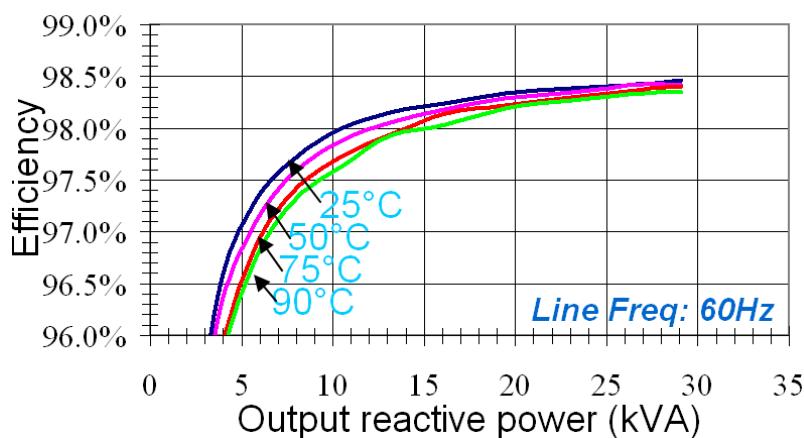


Figure 5.33. Efficiency measurement at 60-Hz line frequency and different temperatures.

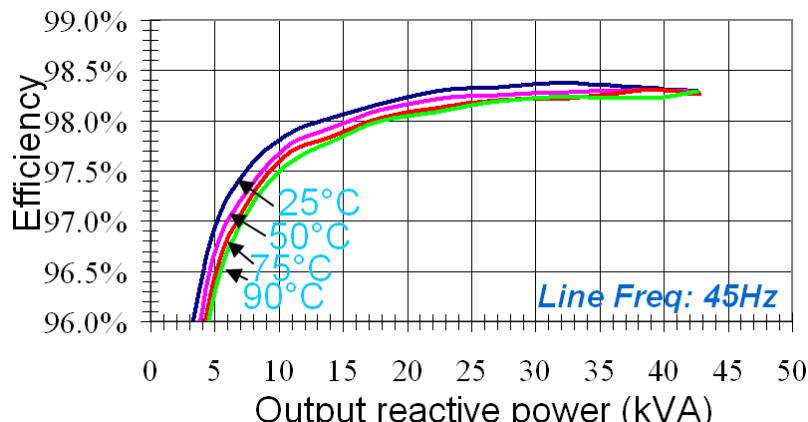


Figure 5.34. Efficiency measurement at 45-Hz line frequency and different temperatures.

To compare the efficiency under different frequency conditions, the above results are rearranged to compare the projected efficiency at different frequencies under the same temperature condition. Figures 5.35 through 5.38 show the projected efficiencies between different output line frequencies at 25°C, 50°C, 75°C, and 90°C, respectively. The power factor in these cases is assumed 0.83, which is the same as what has been tested on the motor drive cases. As can be seen, at the same output power point, the efficiency is higher at a higher output line frequency. That can be translated into higher speed with higher efficiency, which is proven by later motor tests.

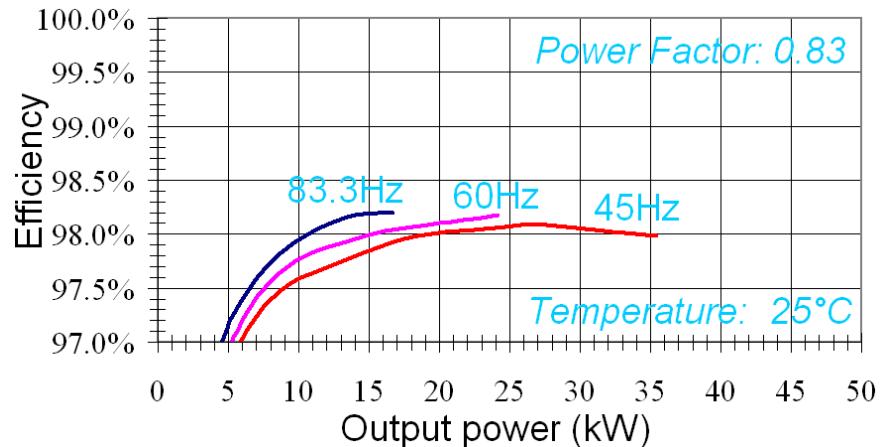


Figure 5.35. Efficiency comparison at 25°C and different line frequency conditions.

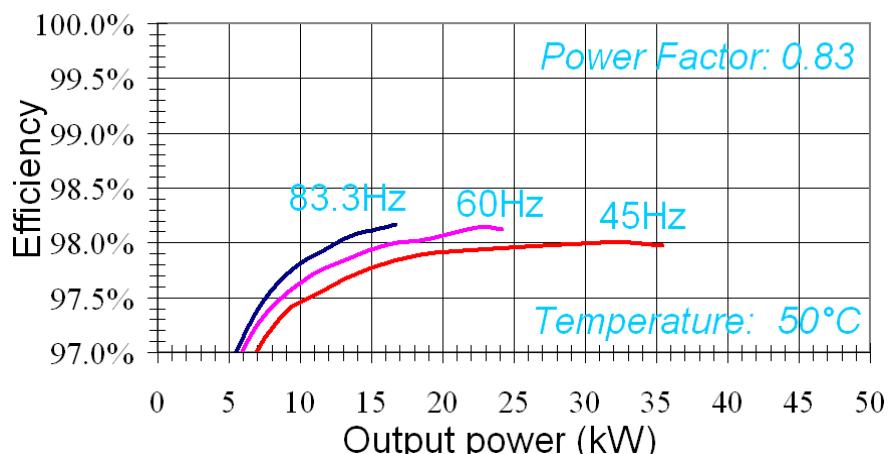


Figure 5.36. Efficiency comparison at 50°C and different line frequency conditions.

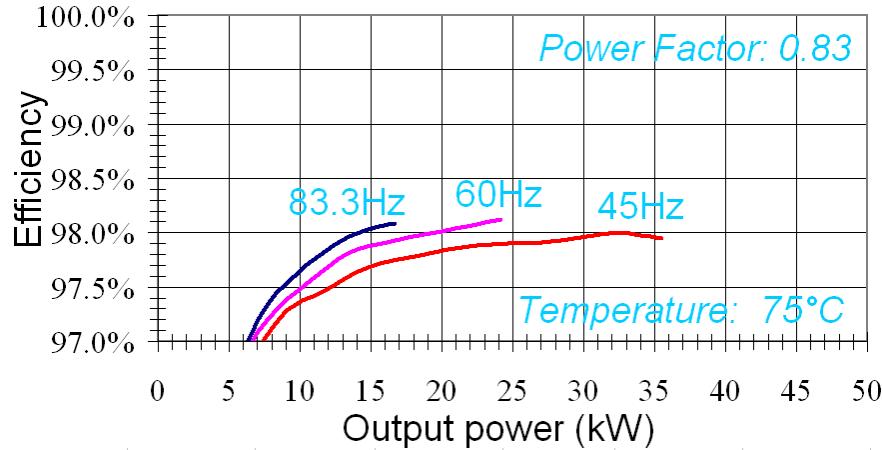


Figure 5.37. Efficiency comparison at 75°C and different line frequency conditions.

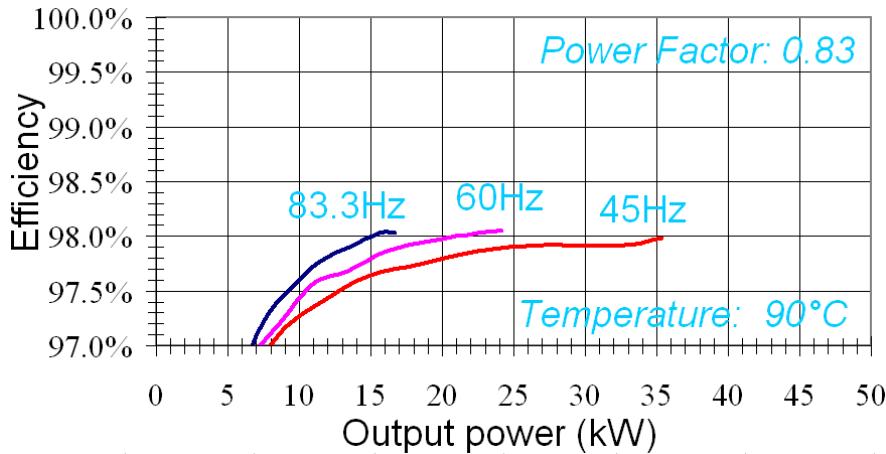


Figure 5.38. Efficiency comparison at 90°C and different line frequency conditions.

5.3. Gen-3 Soft-Switching Inverter

A. Conduction Loss Measurement Results

Voltage drops of two Gen-3 modules are listed in this section to show typical device voltage drops and their variations between upper and lower devices and among different modules. Table 5.6 lists measured main power module voltage drop for serial number SN301P at 25°C and 125°C conditions.

Since each device consists of two 200-A IGBT chips and two MOSFET chips, at low temperature and low current condition, the MOSFET draws more current because it is a resistive device, and its R_{ds-on} is low at low temperatures. After the current reaches 100A, the IGBT starts conducting more current, and the voltage drop becomes near linear. At high temperatures, the R_{ds-on} is nearly doubled, and the IGBT starts drawing more current at about 50A, so the voltage drop at low current is higher as compared to the low temperature condition. When the current continues increasing, the IGBT voltage drop is reduced because of its negative temperature

coefficient characteristic; therefore, the overall voltage drop is nearly the same as at the low-temperature condition. A similar negative temperature coefficient characteristic is also seen in the body diode voltage drop. This implies the inverter efficiency should stay relatively constant over the entire temperature range.

Table 5.6. Measured main power module voltage drop for SN 301P at different temperatures

Module SN 301P at 25°C					Module SN 301P at 125°C				
Current (A)	Q ₁ /M ₁ V _{cesat} (V)	Q ₂ /M ₂ V _{cesat} (V)	M ₁ body diode V _f (V)	M ₂ body diode V _f (V)	Current (A)	Q ₁ /M ₁ V _{cesat} (V)	Q ₂ /M ₂ V _{cesat} (V)	M ₁ body diode V _f (V)	M ₂ body diode V _f (V)
10	0.08	0.09	0.70	0.71	10	0.15	0.16	0.52	0.53
25	0.21	0.22	0.74	0.75	25	0.38	0.40	0.57	0.59
50	0.39	0.42	0.78	0.81	50	0.59	0.62	0.62	0.66
75	0.61	0.64	0.80	0.84	75	0.71	0.74	0.66	0.71
100	0.78	0.83	0.82	0.87	100	0.79	0.83	0.68	0.75
125	0.91	0.96	0.84	0.90	125	0.87	0.90	0.71	0.79
150	0.99	1.05	0.86	0.93	150	0.93	0.95	0.73	0.83
200	1.09	1.16	0.88	0.98	200	1.03	1.06	0.76	0.90
250	1.16	1.23	0.91	1.03	250	1.13	1.16	0.79	0.96
300	1.23	1.29	0.93	1.07	300	1.22	1.24	0.82	1.02
350	1.28	1.35			350	1.30	1.33		
400	1.34	1.40			400	1.38	1.41		
450	1.40	1.46			450	1.47	1.48		

Table 5.7 lists results of the same measurement for serial number SN302P main power module. In this module, the upper device Q₁/M₁ has slightly higher voltage drop than that of the lower device Q₂/M₂. This is opposite to the case in SN301P module, and it indicates possible variations among all the production modules. The variation may be caused by the chip itself and the soldering process.

Table 5.7. Measured main power module voltage drop for SN 302P at different temperatures

Module SN 302P at 25°C					Module SN 302P at 125°C				
Current (A)	Q ₁ /M ₁ V _{cesat} (V)	Q ₂ /M ₂ V _{cesat} (V)	M ₁ body diode V _f (V)	M ₂ body diode V _f (V)	Current (A)	Q ₁ /M ₁ V _{cesat} (V)	Q ₂ /M ₂ V _{cesat} (V)	M ₁ body diode V _f (V)	M ₂ body diode V _f (V)
10	0.09	0.09	0.70	0.70	10	0.16	0.16	0.52	0.53
25	0.22	0.23	0.74	0.75	25	0.38	0.40	0.57	0.59
50	0.40	0.42	0.78	0.80	50	0.60	0.62	0.63	0.66
75	0.62	0.65	0.80	0.84	75	0.73	0.74	0.66	0.71
100	0.79	0.83	0.82	0.87	100	0.82	0.83	0.68	0.75
125	0.93	0.96	0.84	0.90	125	0.89	0.89	0.71	0.79
150	1.04	1.05	0.85	0.93	150	0.96	0.95	0.72	0.83
200	1.16	1.16	0.88	0.98	200	1.07	1.06	0.76	0.90
250	1.24	1.23	0.91	1.03	250	1.17	1.15	0.79	0.96
300	1.31	1.29	0.93	1.08	300	1.27	1.24	0.82	1.03
350	1.37	1.35			350	1.36	1.32		
400	1.43	1.40			400	1.44	1.40		
450	1.49	1.46			450	1.52	1.48		

For the individual devices in the main power module, the MOSFET dominates the conduction voltage drop when the current is below 100A. Figure 5.39(a) shows the voltage drop of individual IGBT and MOSFET and their combination. Both upper and lower devices exhibit similar characteristics. Since the MOSFET also conducts in the negative current direction, or synchronous rectification mode, the actual diode voltage drop should be the combination of M_1/D_1 or M_2/D_2 .

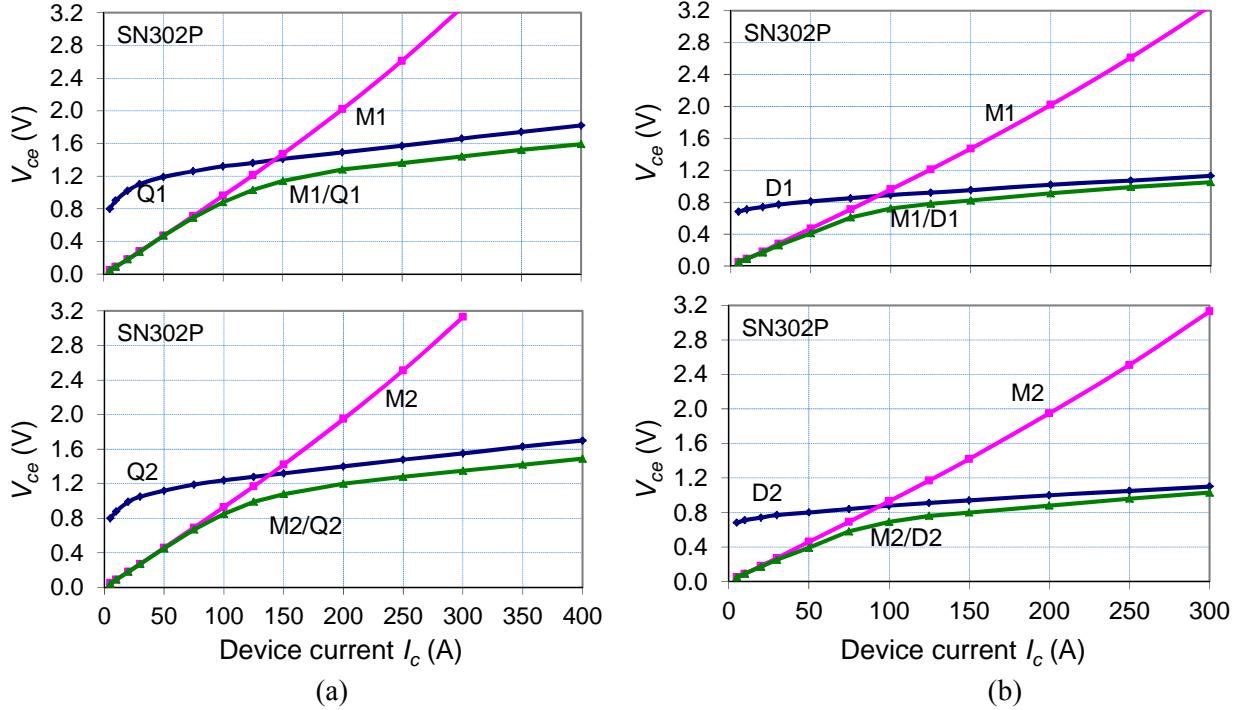


Figure 5.39. (a) voltage drop V_{ce} of individual devices and their combination of Gen-3 module including upper device (Q_1/M_1) and lower device (Q_2/M_2); **(b)** V_{ce} of individual diode and MOSFET and their combination of Gen-3 module including upper device (D_1/M_1) and lower device (D_2/M_2).

Figure 5.39(b) shows the voltage drop in the freewheeling condition, which is much lower than that in the positive current condition. This also implies that soft-switching inverter using hybrid switches has the best chance to achieve 99% efficiency or higher because it avoids the fixed voltage drop portion in both positive current and freewheeling paths. In both Figures 5.39(a) and 5.39(b), this voltage drop is about 0.8V. It represents 80% of conduction loss at 100A or 50% of conduction loss at the rated 400A condition.

Table 5.8 through Table 5.11 list measured voltage drops for the auxiliary modules SN301A and SN302A at different temperatures. The auxiliary IGBT is rated at 150A. Therefore its negative temperature characteristic is only valid below 150A. Above that, the resistive element picks up and the voltage drop tends to be higher at higher temperatures. All the auxiliary diodes are rated 75A, their voltage drop is high as compared to the main diodes because they are ultrafast reverse recovery diodes that tend to have high conduction voltage drop.

Table 5.8. Measured auxiliary module voltage drop for SN 301A at 25°C

Current (A)	Q _{x1} V _{cesat} (V)	Q _{x2} V _{cesat} (V)	D _{x1} V _f (V)	D _{x2} V _f (V)	D _{x3} V _f (V)	D _{x4} V _f (V)	D _{x5} V _f (V)	D _{x6} V _f (V)
10	1.02	0.95	1.14	1.14	1.46	1.42	1.42	1.43
25	1.17	1.06	1.46	1.47	1.88	1.82	1.83	1.83
50	1.27	1.16	1.87	1.88	2.29	2.21	2.22	2.21
75	1.39	1.27	2.15	2.16	2.67	2.57	2.59	2.57
100	1.50	1.37	1.40	2.42	3.00	2.88	2.89	2.87
150	1.70	1.56	2.85	2.87	3.57	3.43	3.45	3.42
200	1.91	1.75	3.26	3.29	3.83	3.68	3.71	3.67
250	2.14	1.95	3.65	3.68	4.08	3.93	3.96	3.91

Table 5.9. Measured auxiliary module voltage drop for SN 301A at 125°C

Current (A)	Q _{x1} V _{cesat} (V)	Q _{x2} V _{cesat} (V)	D _{x1} V _f (V)	D _{x2} V _f (V)	D _{x3} V _f (V)	D _{x4} V _f (V)	D _{x5} V _f (V)	D _{x6} V _f (V)
10	0.75	0.70	0.91	0.91	1.10	1.08	1.08	1.08
25	0.92	0.85	1.24	1.24	1.51	1.48	1.49	1.48
50	1.10	1.00	1.70	1.69	1.93	1.88	1.89	1.87
75	1.27	1.15	1.99	3.00	2.31	2.25	2.27	2.25
100	1.43	1.28	2.26	2.28	2.64	2.57	2.59	2.56
150	1.73	1.53	2.74	2.77	3.22	3.13	3.16	3.11
200	2.02	1.77	3.17	3.20	3.47	3.38	3.42	3.36
250	2.32	2.01	3.55	3.60	3.72	3.63	3.67	3.60

Table 5.10. Measured auxiliary module voltage drop for SN 302A at 25°C

Current (A)	Q _{x1} V _{cesat} (V)	Q _{x2} V _{cesat} (V)	D _{x1} V _f (V)	D _{x2} V _f (V)	D _{x3} V _f (V)	D _{x4} V _f (V)	D _{x5} V _f (V)	D _{x6} V _f (V)
10	0.95	0.95	1.10	1.12	1.40	1.46	1.42	1.54
25	1.07	1.06	1.38	1.43	1.80	1.90	1.83	2.02
50	1.18	1.17	1.75	1.84	2.18	2.31	2.22	2.49
75	1.29	1.27	2.00	2.10	2.53	2.69	2.58	2.92
100	1.40	1.36	2.22	2.35	2.83	3.02	2.89	3.28
150	1.60	1.56	2.61	2.78	3.36	3.61	3.45	3.94
200	1.80	1.75	2.96	3.18	3.60	3.89	3.70	4.23
250	2.02	1.95	3.31	3.56	3.84	4.14	3.95	4.51

Table 5.11. Measured auxiliary module voltage drop for SN 302A at 125°C

Current (A)	Q _{x1} V _{cesat} (V)	Q _{x2} V _{cesat} (V)	D _{x1} V _f (V)	D _{x2} V _f (V)	D _{x3} V _f (V)	D _{x4} V _f (V)	D _{x5} V _f (V)	D _{x6} V _f (V)
10	0.71	0.70	0.88	0.90	1.07	1.10	1.09	1.13
25	0.86	0.85	1.18	1.22	1.47	1.52	1.49	1.58
50	1.02	1.00	1.58	1.66	1.86	1.94	1.90	2.04
75	1.18	1.15	1.86	1.96	2.22	2.33	2.27	2.46
100	1.32	1.28	2.10	1.22	2.53	2.67	2.60	2.82
150	1.58	1.53	2.53	2.70	3.08	3.27	3.17	3.46
200	1.84	1.76	2.91	3.12	3.33	3.53	3.43	3.73
250	2.10	2.00	3.26	3.50	3.56	3.78	3.68	3.95

In resonant circuit operation, all the auxiliary switches and diodes only conduct partial resonant current; therefore they do not need to be fully rated. Depending on the turns ratio, typical current

distribution at 400 A peak current condition is 250A flowing in auxiliary switches and 150A flowing in auxiliary diodes. Furthermore, the auxiliary switches and diodes only conduct in a very short period, typically 3% of main switch conduction period; therefore their conduction loss is negligible.

B. Comparison of Voltage Drop Between Gen-1, Gen-2, and Gen-3 Modules

Figure 5.40 repeats the PSPICE simulation results of the Gen-3 module design reported in the last year's quarterly report. The measured voltage drops of Gen-1 module, CM400DY-12NF, and CM300DY-12NF are also compared in the graph. At the design stage, two possible configurations were considered for Gen-3 module design. The final selection was to use CM400DY-12NF IGBTs in parallel with two STY11265M5 MOSFETs.

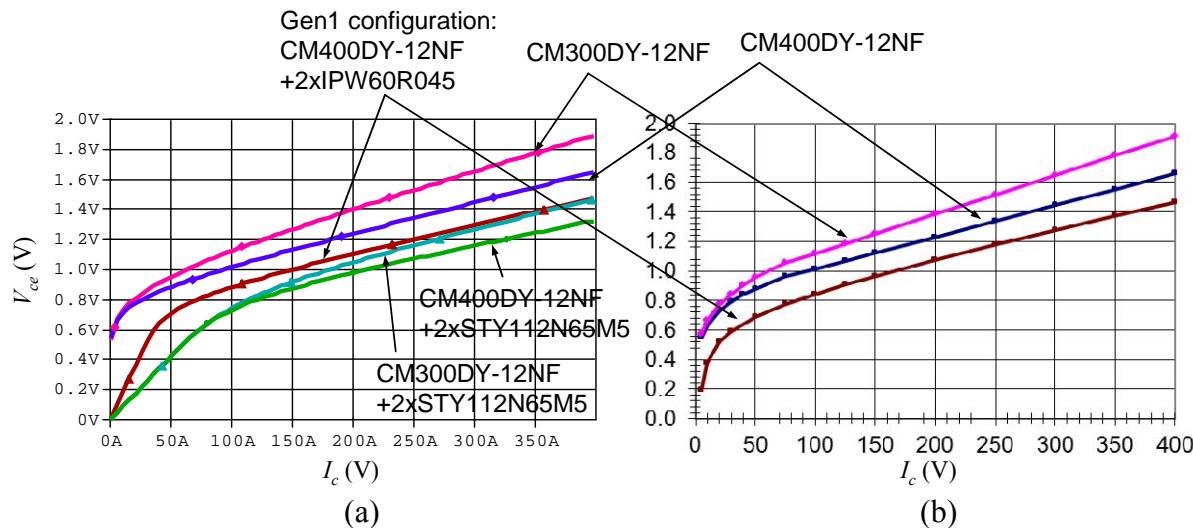


Figure 5.40. Model verification using Gen-1 module to predict performance of possible Gen-3 module designs.

Figure 5.41 shows the comparison of the measured voltage drop between Gen-1 module SN102, Gen-2 module SN201, and Gen-3 module SN302P. As shown in Figure 5.41(a), the upper device (Q_1/M_1) conduction characteristic of SN302P matches the simulated model in Figure 5.40(a) very well, but the lower device (Q_2/M_2) appears to have higher voltage drop at higher current region. The reason of mismatch is most likely caused by the IGBT chip. Some of Gen-3 IGBT chips seemed to have higher voltage drop than that of the Gen-1 IGBT. However, the overall design matches the originally simulated model very well, especially at the lower current region.

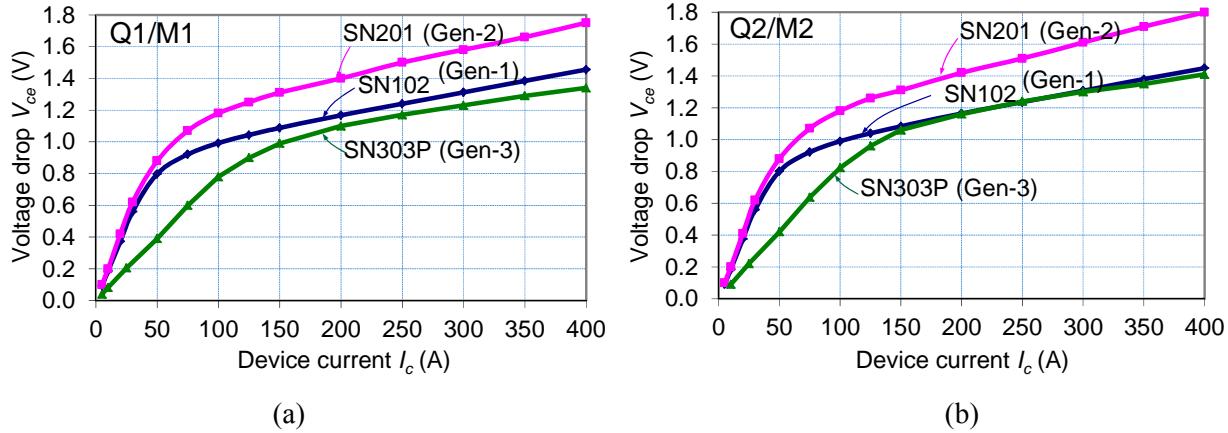


Figure 5.41. Voltage drop comparison between Gen-1, Gen-2, and Gen-3 modules: (a) upper device and (b) lower device.

C. Switching Characteristic Measurement Results

To avoid wiring induced inductance, a multilayer power board is designed to accommodate laminated bus bar and DC bus bypass capacitors. The power board contains 10 copper layers to ensure current carrying capability. Figure 5.42(a) shows the test setup with power board sitting on the main power module and auxiliary module. Figure 5.42(b) shows the complete setup for switching characteristic evaluation. The Gen-3 gate drive board sits on top of the power board with ribbon cables connecting the driving signals from the control board. Low-inductance capacitors are used as the resonant capacitors, which are directly screwed on the right-hand side of the power board. The left-hand side of the power board is for resonant inductor connection.

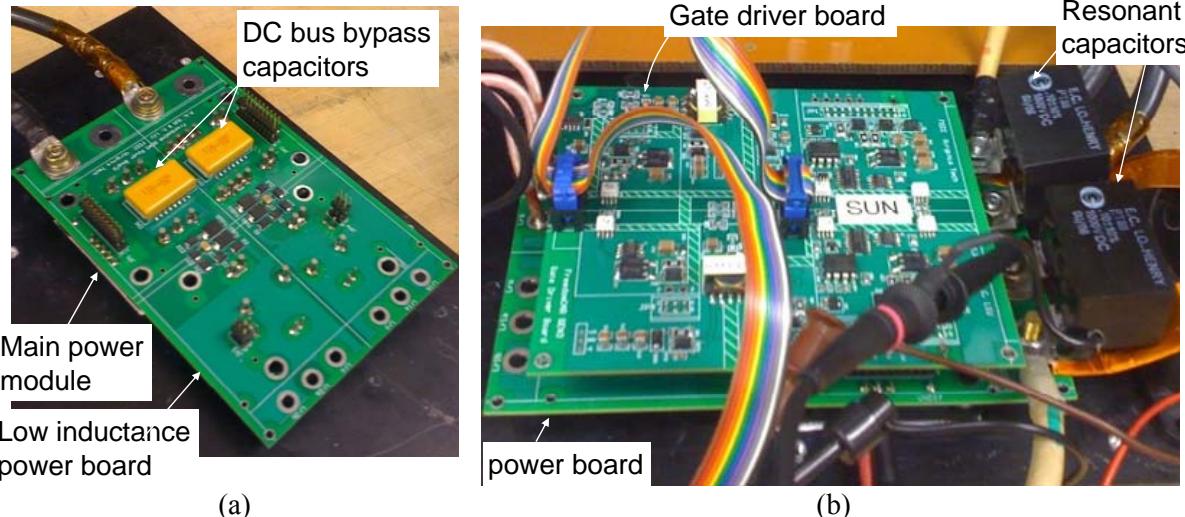


Figure 5.42. Switching characteristics measurement setup: (a) Gen-3 module power board assembly and (b) complete setup with gate driver board and resonant circuit connection.

In order to show how the Gen-3 module design is superior to both Gen-1 and Gen-2 modules, we first compare Gen-1 and Gen-2 switching characteristics, as shown in Figure 5.43. Although

both modules can achieve zero-voltage switching, Gen-1 module has a noticeable ringing on resonant current I_{Lr} and gate voltage V_{GE} . The ringing of I_{Lr} waveform is caused by the parasitic inductances of the module internal structure, while the ringing of the V_{GE} waveform is caused by the gate drive circuit and power bus layout.

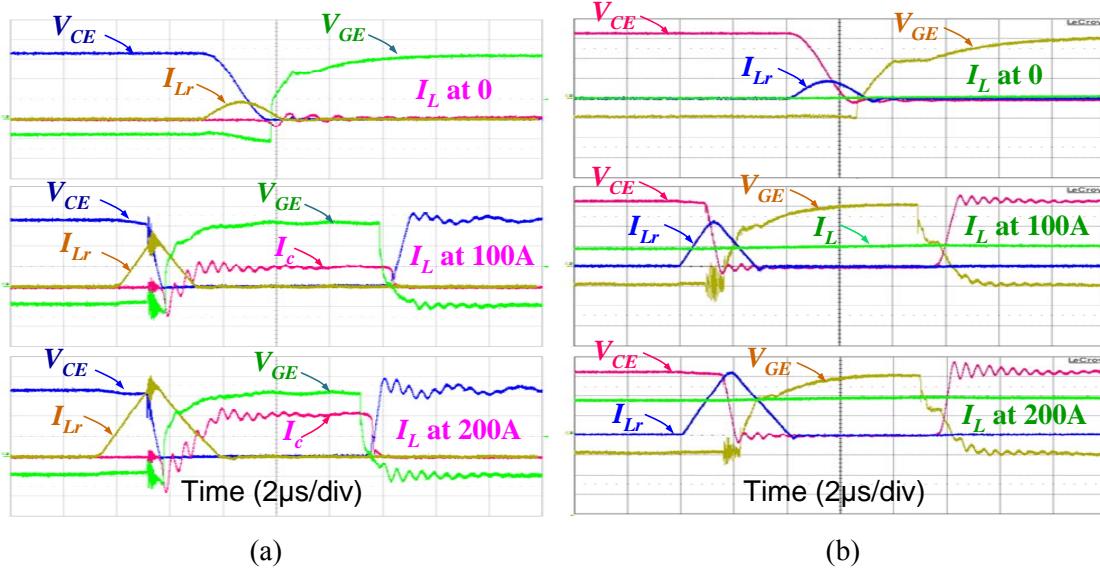


Figure 5.43. Switching characteristic comparison between Gen-1 and Gen-2 modules: (a) Gen-1 module and (b) Gen-2 module.

Figure 5.44 compares switching waveforms between Gen-2 and Gen-3 modules. The Gen-2 low-profile module was able to eliminate the majority of the module internal inductance. However, its gate drive circuit and associated power board still contains significant parasitic inductance. Thus its V_{GE} waveform contains significant ringing at 100-A and 200-A test conditions. In the Gen-3 design, the gate drive and power boards shorten the gate drive signal length and thus reduce associated parasitic inductance; therefore, the V_{GE} waveform shown in Figure 5.44(b) clearly avoids the parasitic ringing. Zero-voltage switching is clearly seen in all Gen-1, Gen-2 and Gen-3 modules and in all current conditions by noticing that the device voltage V_{CE} drops to zero before gate drive V_{GE} is turned on. Measurement results clearly indicate that Gen-3 module is nearly perfect with not only significant conduction loss reduction, but also switching noise elimination. All waveforms are clean, and zero-voltage switching can be achieved at different current levels.

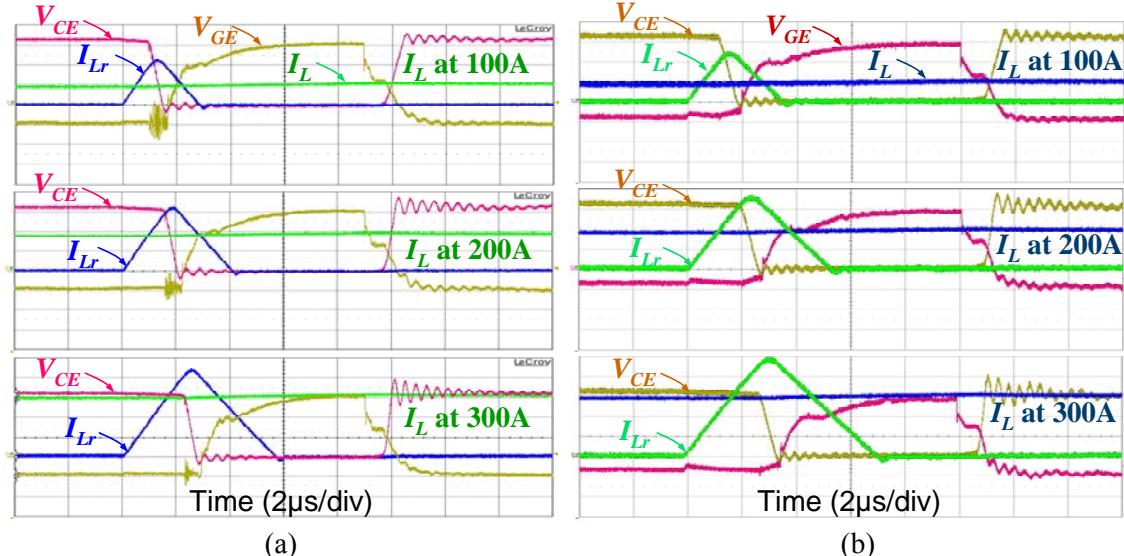


Figure 5.44. Switching characteristic comparison between Gen-2 and Gen-3 modules: (a) Gen-2 module and (b) Gen-3 module.

Using the measured conduction and switching characteristics, the inverter efficiency can be calculated with the loss separation method. Figure 5.45 shows the projected inverter efficiency for inverters using Gen-1, Gen-2, and Gen-3 modules under 10-kHz switching frequency. Gen-2 is least efficient because its substrate conduction paths introduce substantial voltage drop and associated loss. Gen-3 improves light-load efficiency by about 0.4% until about 30 kW and about 0.2% at full load as compared to Gen-1 because of better MOSFETs and freewheeling path voltage drop reduction.

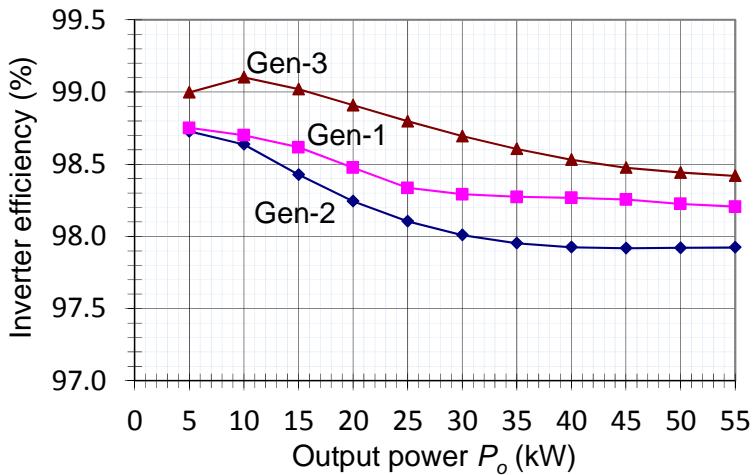


Figure 5.45. Comparison of projected efficiency between Gen-1, Gen-2, and Gen-3 inverters.

As compared to Gen-1, Gen-3 improves efficiency significantly over the entire load range. In average, it shows 0.5% efficiency improvement because of the conduction loss reduction in both positive current and freewheeling current directions. Further experimental verification is needed to verify the projected efficiency profile.

C. Gen-3 Assembly and Preliminary Efficiency Measurement Results

Figure 5.46 shows photographs of the Gen-3 inverter assembly. The heat sink is air-cooled, and the case has screw holes to allow mounting on the chassis of the Azure Dynamics vehicle. In Figure 5.46(a), the front view shows copper bars for input DC and output AC connections. Two high-frequency capacitors are located on each end. The DSP board is mounted on the top case; its signals are connected to the interface board through a ribbon cable.

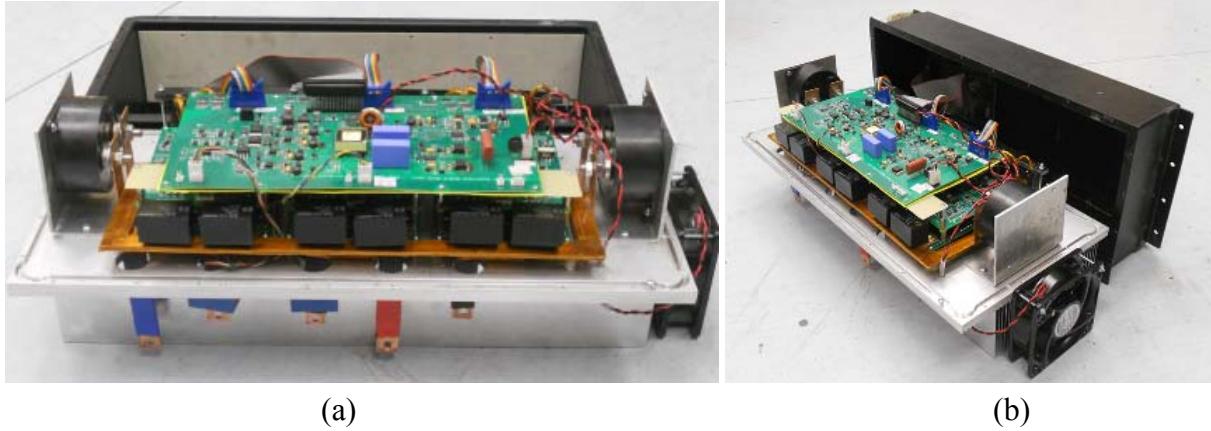


Figure 5.46. Gen-3 soft-switching inverter assembly: (a) front view and (b) side view.

Figures 5.47, 5.48, and 5.49 show all three generations of the soft-switching inverter. Gen-1 inverter has integrated cooling for the modules, and thus the cooling system requires only one external manifold to distribute the coolant. Gen-2 inverter adopts the low-profile modules that allow both liquid- and air-cooled. In this design, a homemade heat sink was designed to fit the module mounting. The size of coupled magnetics was also reduced. Gen-3 inverter is the only air-cooled design. The size of its coupled magnetics is the same as that in Gen-2 inverter, and the overall size can fit the existing chassis quite comfortably.



Figure 5.47. Photograph of Gen-1 inverter assembly.

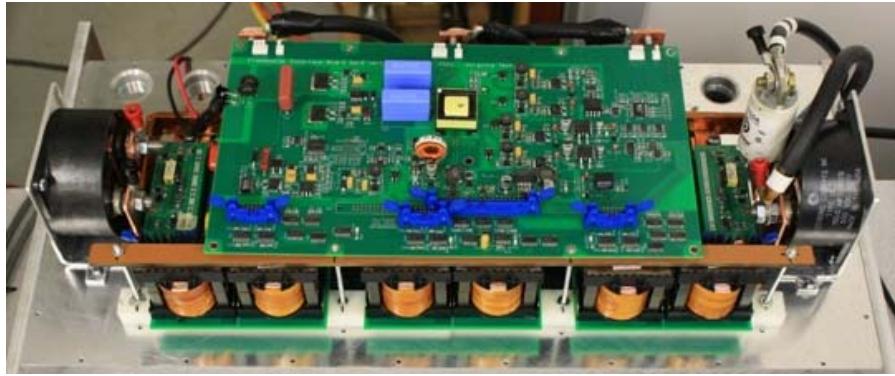


Figure 5.48. Photograph of Gen-2 inverter assembly.



Figure 5.49. Photograph of Gen-3 inverter assembly.

For the efficiency measurement, it is difficult to measure 1% loss because the input and output results are so close that any instrumentation or recording error can cause significant error in efficiency. Therefore, we used the inductor as the load and measured the loss of the inverter under pure inductor load condition. Since the inductor load only circulates the energy through diode freewheeling, the measured loss under certain kVA condition should be about the same as that under the same kW condition. With the synchronous rectification, the reverse conduction loss is comparable to the forward conduction loss, so the inverter efficiency can be calculated using the loss measured with the inductive load. Figure 5.50 compares the inverter efficiency for inverters using Gen-1, Gen-2, and Gen-3 modules under 10-kHz switching frequency at 45-Hz fundamental frequency or 2700-rpm condition. Each of the three generation inverters was tested under the same inductive load conditions. Gen-2 is least efficient because its substrate conduction paths introduce substantial voltage drop and associated losses. Gen-1 has a different modulation method, so its light load efficiency seems to be the same or potentially higher than that of Gen-3, but overall Gen-3 inverter improves the efficiency over Gen-1 by about 0.4% and about 0.7% over Gen-2.

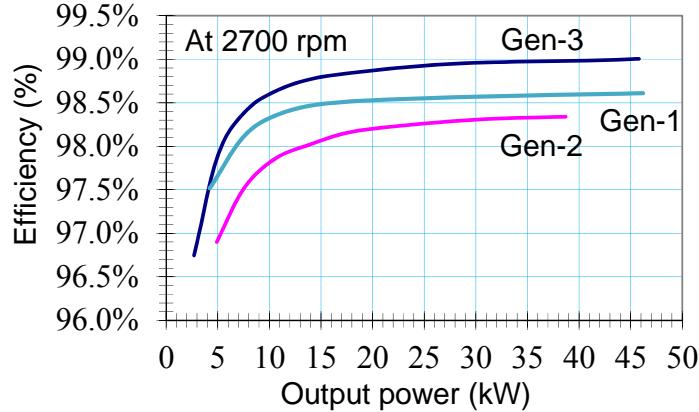


Figure 5.50. Comparison of measured efficiency between Gen-1, Gen-2, and Gen-3 inverters at 2700-rpm condition.

Figures 5.51 and 5.52 compare the inverter efficiency for inverters using Gen-1, Gen-2, and Gen-3 modules under 10-kHz switching frequency at 60- and 83.3-Hz fundamental frequencies or 3600- and 5000-rpm conditions. All three-generation inverters were tested under the same inductive load conditions. Gen-2 is again the least efficient. Gen-1 has tends to have a higher light-load due to a different modulation scheme, but Gen-3 still show the best efficiency overall with the improvement over Gen-1 by about 0.3% and about 0.6% over Gen-2 in most operating range. The results agree with the loss calculation based on conduction and switching loss separation method that were reported in the last quarterly report quite well in 10 to 30 kW range.

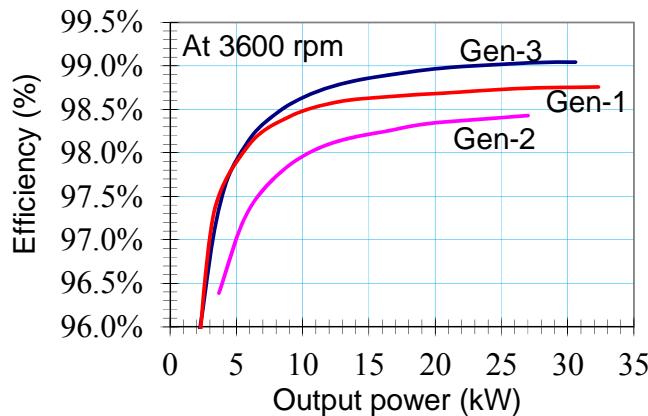


Figure 5.51. Comparison of measured efficiency between Gen-1, Gen-2, and Gen-3 inverters at 3600-rpm condition.

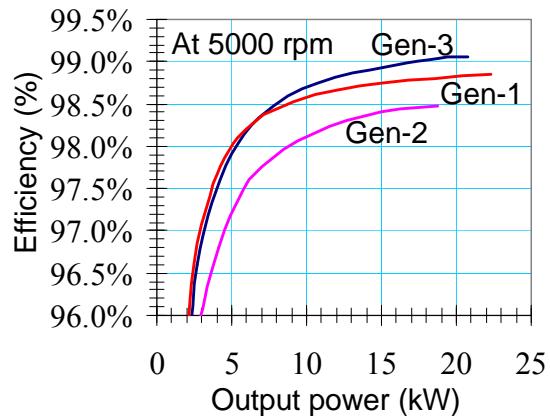


Figure 5.52. Comparison of measured efficiency between Gen-1, Gen-2, and Gen-3 inverters at 5000-rpm condition.

6. IN-VEHICLE TEST

6.1. Dynamometer Testing

Figure 6.1 shows the complete circuit diagram of the three-phase soft-switching inverter prototypes showing the key components of the power circuit including the soft-switching modules, resonant capacitors, and coupled magnetics.

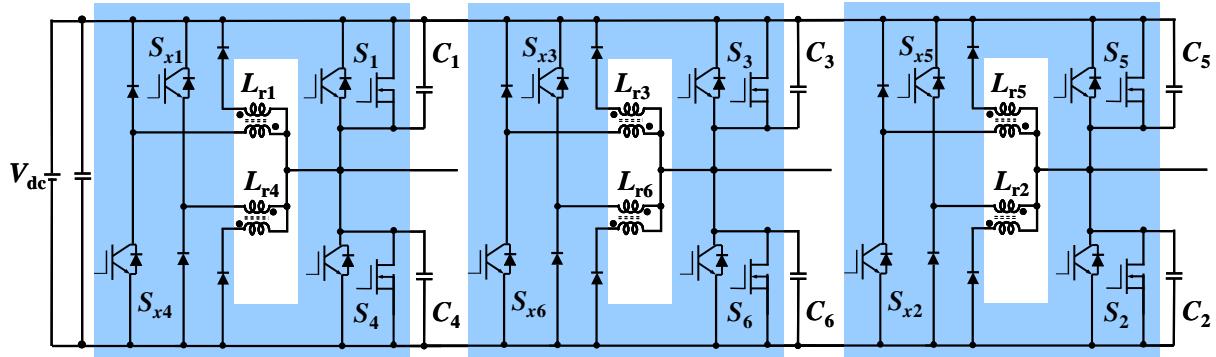


Figure 6.1. Three-phase soft-switching inverter using hybrid switches, and (b) Photograph of a 325-V, 30-kW prototype.

Figure 6.2 shows the photograph of the Gen-3 inverter prototype. It can be seen that the unit fits inside the existing case provided by Azure Dynamics. Figure 6.2(a) shows the front view of the inverter with the key components marked on the figure. Figure 6.2(b) shows the back view of the inverter. The resonant inductors are integrated as a part of the complete assembly. The markings also indicate the temperature monitoring points during the dyno testing.

The entire inverter has only one 3-W cooling fan to serve for air circulation. There are eight thermal couples installed at different locations: module case, DC bus capacitor, three heat sink points, two resonant inductor points, and ambient. The measured module case point is the farthest point away from the fan and is the worst case among all the modules. One of the measured resonant inductor point is also farthest point are from the fan and is the worst case among all the inductors.

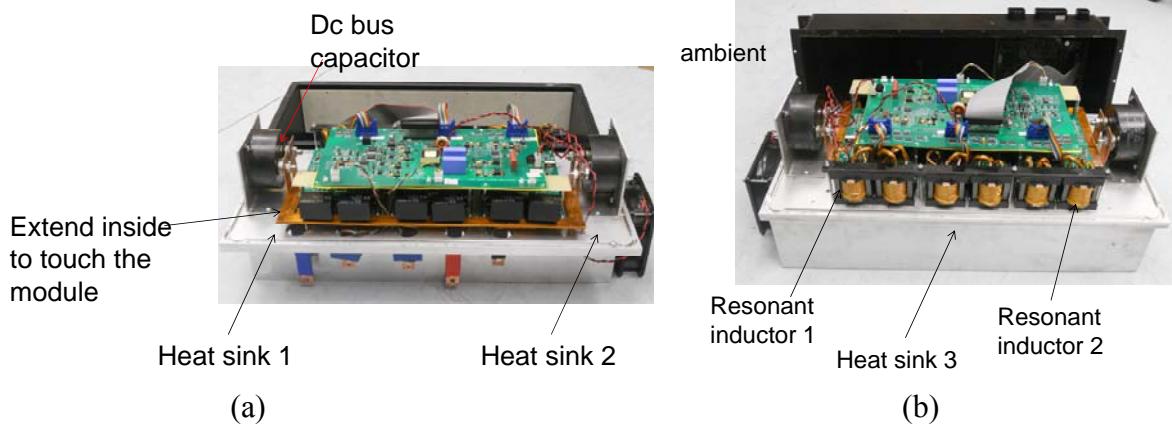


Figure 6.2. Photograph of the Gen-3 soft-switching inverter prototype: (a) front view and (b) back view.

Figure 6.3 shows the photograph of the Gen-3 inverter mounted on the test rack for the dynamometer testing. The control board is attached to the top case. The DC input lines are directly connected to the DC bus capacitor, and the AC output lines are connected through cables to the measurement box and then to the motor under test. Two of the three output cables have current sensors attached to them. The measurement box has voltage and current calibrated to provide signals to a Yokokawa power meter – WT1600. All thermal couples are also connected to a data acquisition system that can record the temperature information for a long period. In this setup, the data were recorded in 1-s interval.

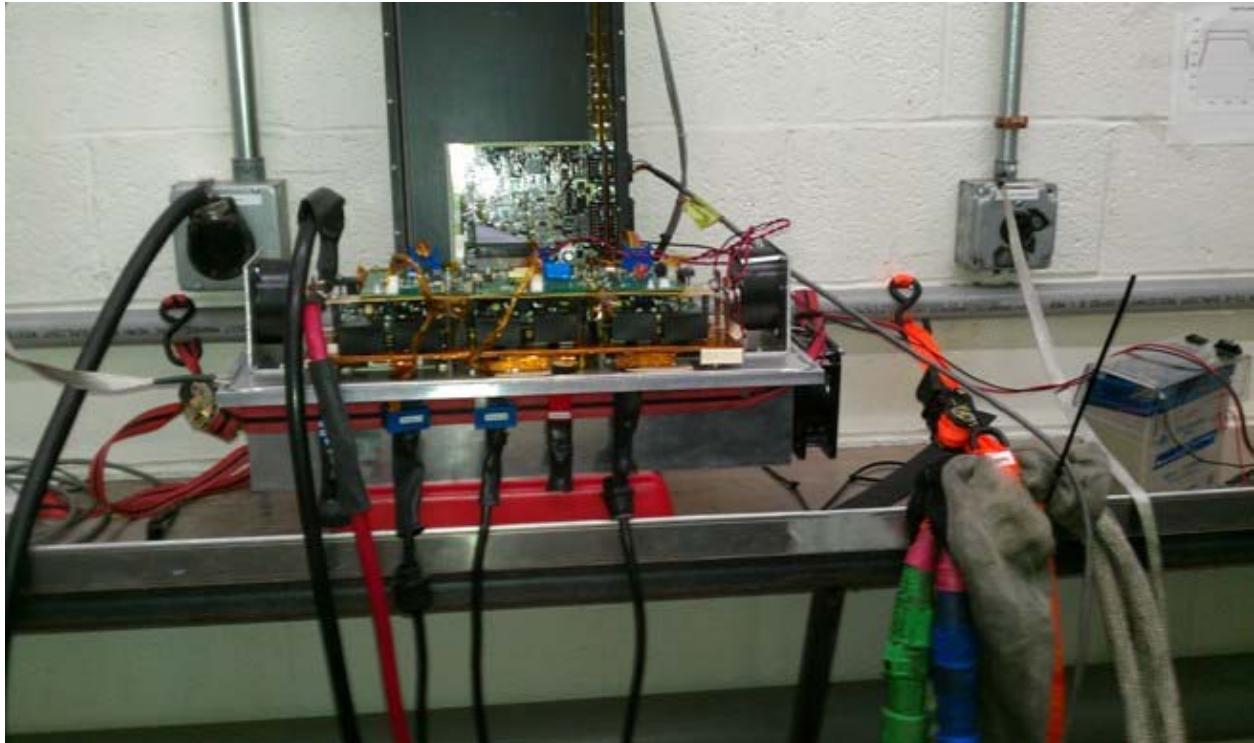


Figure 6.3. Photograph showing the Gen-3 inverter mounted on the test rack for the dyno testing.

The inverter operates under discontinuous PWM mode with 10-kHz switching frequency. It was tested with three voltage levels: 275, 325, and 375 V for a 4-pole, 90-kW induction motor for electric vehicle traction drives. Table 6.1 lists the three different speed and torque test conditions in which the efficiency and other performance such as the output current waveforms were monitored. With a 4-pole machine, the setting at 3000 rpm means a fundamental frequency of 100 Hz, and the setting at 1000 rpm means a fundamental frequency of 33.3 Hz.

The dynamometer is a re-generation type that allows the speed to be set constant while the motor under test can adjust torque from positive to negative. Therefore, we not only tested the motoring mode with positive torque, but also tested one re-gen condition at 1000 rpm, -100 Nm for each voltage setting.

Table 6.1. Test conditions that are run more than 10 minutes for each data set

Op. Point	DC bus supply(V)	Dyno (rpm)	Torque (Nm)
1	325	3000	100
2	325	1000	200
3	325	1000	-100
4	275	3000	100
5	275	1000	200
6	275	1000	-100
7	375	3000	100
8	375	1000	200
9	375	1000	-100

Figures 6.4(a) and 6.4(b) show the output phase current waveforms at 3029 rpm, 115 Nm and 1030 rpm, 225 Nm load conditions. Both conditions were tested with 325-V DC bus. The high-speed operation tends to have waveform distortion due to insufficient voltage. However, in this case, it was due to the control loop parameter mismatch. The program assumed a 55-kW machine, but the motor under test was a 90-kW machine. Therefore, by accident, the inverter was tested at a power level much higher than the initial setting. The inverter output in Figure 6.4(a) condition reaches 40 kW, which is highest power that the Gen-3 inverter has ever been tested. The Azure Dynamics team fixed the control parameters this test, and the waveforms were all clean sinusoidal since then. Figure 6.4(b) represents highest phase current condition. Even though the output power is only 27 kW, the inverter output current rms is 146 A, much higher than the 40-kW output at 3000 rpm condition.

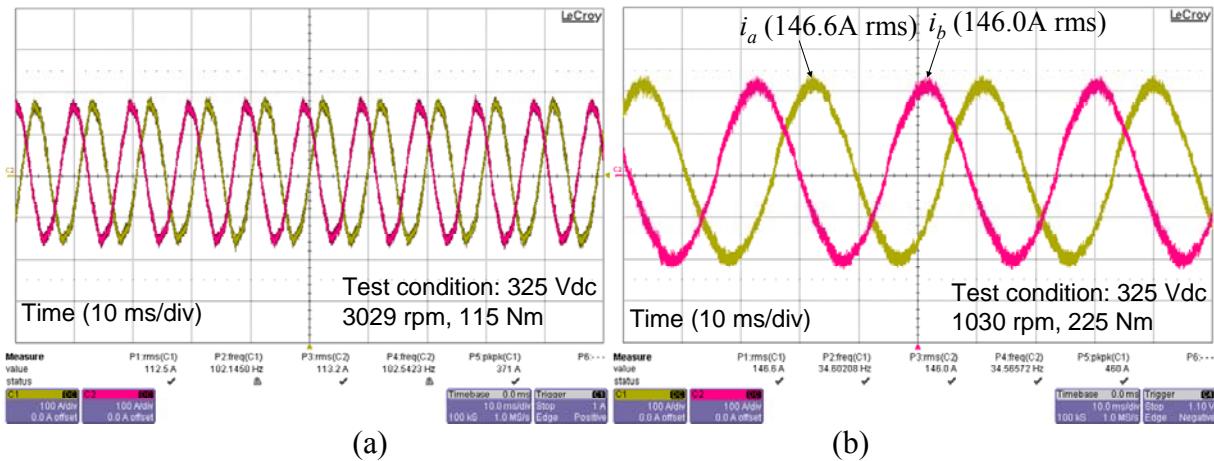


Figure 6.4. Experimental inverter output current waveforms at (a) 40-kW, 3029 rpm, 115 Nm, and (b) 27-kW, 1030 rpm, 225 Nm.

Figure 6.5(a) shows the inverter output current waveforms at 3030-rpm, 110-Nm load condition at 275-V input. In this case, the inverter output current is 150 A rms, and the output power is 39 kW. Notice that the waveform quality is much better than that shown in Figure 6.4(a) even with a lower input voltage because the control parameter has been fully tuned for the 90-kW machine.

Figure 6.5(b) shows the inverter output current waveforms at 2980 rpm, 110 Nm motor load at 375-V dc input voltage condition. In this case, the inverter output current is about 101 A rms, and the output power is 38 kW. Higher input voltage tends to have lower output current at the high speed region because the control loop adapts the maximum torque per ampere (MTPA) control to minimize the motor current with the available input voltage. Note that the tested power level far exceeds the continuous rated power, which is essential because of the need of high currents during startup and short-term acceleration.

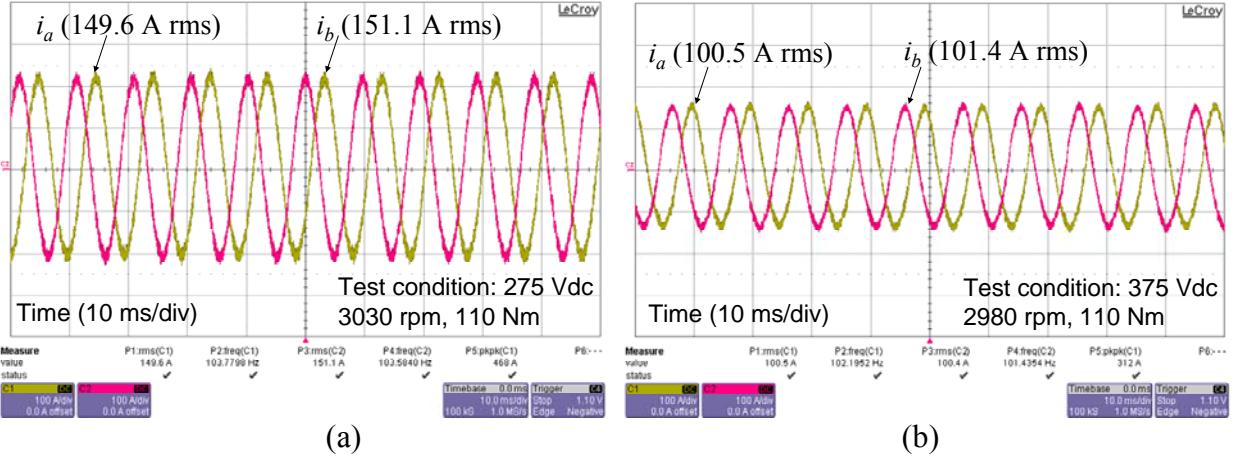


Figure 6.5. Experimental inverter output current waveforms at (a) 275 V, 39 kW and (b) 375 V, 38 kW conditions.

Figure 6.6(a) shows the efficiency as a function of the output power at 3000-rpm condition. In this measurement, the auxiliary power and fan losses are all included as a part of total losses. With hybrid switch and adaptive timing soft-switching operation, the efficiency at 325-V input exceeds 99% at 30-kW nominal load condition. At 375-V input, 38-kW output, the efficiency reaches 99.3%. Such efficiencies are not possible to measure with any power meter that measures the dc input and PWM ac output. In order to verify the efficiency numbers, our approach is to measure the module case temperature over a long period and use it as the loss to project the efficiency. Figure 6.6(b) shows the measured power module case temperature over a 12-minute interval. The 325-V condition was started at a temperature that is considered steady state, so over the 12-minute interval there was not any appreciable temperature rise. At the 20°C room temperature test condition, the entire inverter was only cooled by a 3-W fan, and the monitored module which is far away from the fan has a case temperature of 47°C under steady-state 325-V input, 38-kW output condition.

With soft switching, the achieved ultrahigh efficiency is mainly attributed to the conduction voltage drop reduction by the hybrid switch. Take 375-V case as the example, the conduction voltage drop is less than 2×0.8 V at 100-A condition, or 0.43% of the total loss. With near zero switching loss in both main and auxiliary switches, the remaining major loss component is the resonant circuit conduction, which is estimated to be around 0.1%. The total losses from gate drives, controller, conditioning circuit, fan, and auxiliary power supplies were measured at 19 W, or 0.05%. The dc bus capacitors, power bus, and other parasitic losses attribute another 0.05%. Therefore, 99.3% efficiency at 375-V input, 100-A output current and 38-kW output power is a conservative projection from the temperature measurement.

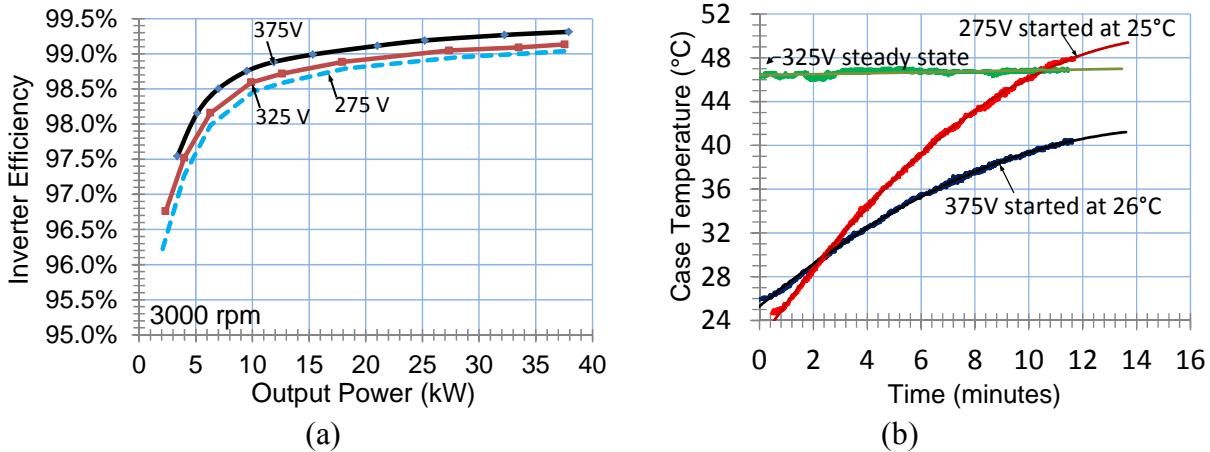


Figure 6.6. (a) Measured efficiency as a function of output power at 3000-rpm operation, and (b) Measured module case temperature over a 12-minute interval at 38-kW output condition.

Table 6.2 lists detailed loss components under three input voltage and two motor load conditions. The first nominal load is 3000 rpm, 100 Nm, and the second nominal load is 1000 rpm, 200 Nm. Actual speed and torque vary during the test because of the error of the control loop tracking.

Table 6.2. Loss separation under three input voltage and two load conditions

Nominal Testing Condition	3000rpm, 100 Nm			1000rpm, 200 Nm		
	275	325	375	275	325	375
DC bus voltage, V	275	325	375	275	325	375
Motor speed, rpm	3011.1	3006.4	3007.9	1028.4	1015.6	1020
Motor torque, Nm	107.1	107.4	109.2	230.4	220	227
Line-line voltage, Vrms	172.2	213.8	247.6	134.2	124.7	130.1
Phase current, Irms	150.6	114.7	101.8	148.62	147.1	147.2
Frequency, Hz	103.26	101.83	101.41	35.4	35.5	34.7
Inductor temperature at 12 minute, °C	56	70.1	51	65.9	62.4	76.7
Module case temperature at 12 minute, °C	48	47.1	42	51.9	45.4	53.9
Main IGBTs, $Q_1 - Q_6$, losses (W)	70.8	28.2	18.3	67.2	66	64.8
MOSFETs, $M_1 - M_6$, losses (W)	240	216	180	247.2	246	243
Auxiliary IGBTs, $Q_{x1} - Q_{x6}$, losses (W)	16.5	12	11.7	16.8	16.8	16.8
Auxiliary Diodes, $D_{x1} - D_{x6}$, losses (W)	6.3	4.8	4.3	6.0	5.8	6.2
Resonant inductor, L_r , loss (W)	36	31	30	37	40	42
Auxiliary power, gate, sensor, IC ckts, (W)	19	19	19	19	19	19
Parasitic bus bar, capacitor, connection (W)	7	6	5	7	7	7
Total losses (W)	395.6	317.0	268.3	400.2	400.62	398.84
Output power, P_o (W)	38244	37213	37591	28036	26846	27201
Input power, P_{in} (W)	38640	37530	37859	28436	27247	27600
Inverter efficiency	98.98%	99.16%	99.29%	98.59%	98.53%	98.55%

With motor current less than 150 Arms for all test conditions, the majority of current conducts through MOSFET. Thus the MOSFET loss is dominant in all cases. The parasitic loss is a lump number that is projected from the load current magnitude. All other losses can be found either by temperature projection or by the switch conduction and switching characteristics. All switch and inductor rms currents can also be obtained from circuit simulation to ensure their accuracy. The

combined loss of the auxiliary power supply, gate drive, and controller board losses was obtained from no-load test.

6.2. In-Vehicle Test

The purpose of in-vehicle test is to verify that the inverter package is secured, and the operating range is wide enough to adapt to different acceleration and deceleration conditions. The test can also verify if the inverter is susceptible to noise or not. Azure Dynamics has an all-electric Citivan that allows the inverter prototype to be placed on a test stand inside the vehicle with all the wiring already hooked up for vehicle driving test. Figure 6.7 shows the photograph of the vehicle under test.



Figure 6.7. Photograph of all-electric Citivan for in-vehicle testing.

Figure 6.8 shows the photograph of in-vehicle test setup. A spare inverter is sitting underneath the test stand. In case the inverter-under-test fails on the road, a simple rewiring would allow the vehicle to operate again.



Figure 6.8. In-vehicle test setup.

During the vehicle test drive, the operating conditions of the inverter and motor were all recorded. Figure 6.9 shows the motor speed and current during a 4-minute driving cycle. The red line is the motor speed and is fluctuating from -200 to 1000 rpm. The blue line is the peak phase current. Maximum recorded peak phase current during hill climbing was 380 A, or 268 A. This current is much higher than the maximum current under dyno test condition, or 150 A. However, its corresponding speed and thus the power level was low at such a high-current condition.

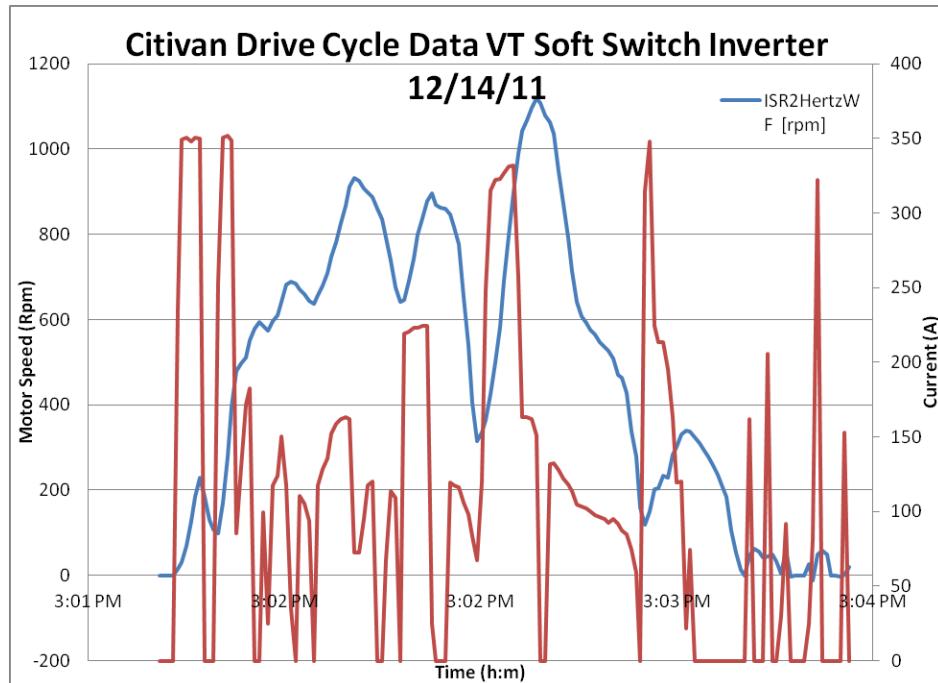


Figure 6.9. Recorded in-vehicle tested motor speed and phase current during a 4-minute city driving cycle.

The complete drive cycle of a city block lasted about 15 minutes. After the van returned, the heat sink did not show an appreciable temperature rise. It was the same as the outdoor temperature. The superiority of ultrahigh efficiency inverter operation was fully proven. At the time stamp between 3.02pm and 3:03pm, the motor current reached the peak current, and the maximum power occurred at 950 rpm, 380 A. This current corresponds to about 400 Nm torque, and the power level is about 40 kW.

7. INVERTER COST ESTIMATE

7.1. Soft-Switching Module Cost Estimate

As compared to the Gen-2 module, the Gen-1 module has lower conduction voltage drop and lower thermal impedance through direct liquid cooling. The measured inverter efficiency reflects the advantage of the low conduction voltage drop. However, the Gen-2 module significantly reduced the height and parasitic loop inductance. The layout has minimum path for terminal connection, especially the connection between resonant capacitor and the chip. A separate power terminal is brought out directly from the substrate for resonant capacitor connection. The substrate and housing package adopts a low profile, industry standard Powerex “NX-M” series package family, which has the same height, but will be slightly longer and wider than the standard NX package. As a result, the standard high volume parts such as terminals, plastics and baseplates will minimize the module cost. The low height profile will reduce size, weight, parasitic inductance, and filling materials. The ease of assembly also contributes to the labor cost reduction. This package is designed to be compatible with either liquid or air cooling. Table 1 shows the cost comparison between Gen-1 and Gen-2 modules.

Table 7.1. Cost comparison between Gen-1 and Gen-2 modules.

	Gen 1	Gen 2		Gen 3	
		Direct Liquid Cooled	Standard Package	Direct Liquid Cooled	Standard Package
		Low Volume	High Volume	High Volume	High Volume
Materials	\$545.87	\$98.25	\$114.25	\$110.95	
Labor	\$360.00	\$35.00	\$35.00	\$35.00	
Total	\$1,222.92	\$179.89	\$201.89	\$197.03	

For the Gen-3 module, further cost reduction is achieved by eliminating two diodes per switch, as shown in Figure 4.28. However, splitting the module into a separate Auxiliary and Power module does result in some duplication of parts such as the plastic case and lid, ceramic substrates and baseplates, thus increasing the overall materials costs slightly over those of Gen 2. The complete phase leg module cost is estimated at \$197.03 when produced in 100,000 quantities. Further module cost reduction is possible when the power semiconductor wafer size is increased from current 8” to 12” diameter. This wafer size reduction has been confirmed by super-junction MOSFET manufacturers. However, the following inverter cost estimate will continue use the 8” wafer as the basis.

7.2. Soft-Switching Inverter Cost Estimate

Table 7.2 lists major circuit components and their price for the Gen-3 inverter cost estimate. The proposed package differs from conventional inverter mainly on the use of coupled magnetics for soft switching and the power circuit board to serve as the bus bar. The rest components should be common and similar to the conventional hard-switching inverter. The overall cost is about \$938 for the 60-kW inverter. There is room for cost reduction. For example, the integration of power and gate drive boards and the integration of interface and DSP boards altogether should

reduce the total cost by at least 10%. If the large wafer power semiconductors are available, the soft-switch module may allow another 10% total cost reduction. Overall we can expect the cost around \$800. Notice that the design allows total elimination of forced-air or liquid cooling system. Overall this is a durable design option for the next generation EV traction motor drive inverter.

Table 7.2. Cost estimate for the soft-switching inverter at 100,000 quantity production

Major components	Quantity	Unit price	Ext. price
Coupled magnetics	6	\$8.40	\$50.40
Power board/bus bar	1	\$43.02	\$43.02
Bus capacitors	2	\$42.00	\$84.00
Soft-switch modules	3	\$197.03	\$591.09
Gate drive boards	3	\$13.49	\$40.47
Interface/sensor board	1	\$37.54	\$37.54
DSP board	1	\$12.44	\$12.44
Heat sink/Case	1	\$43.37	\$43.37
Total Material			\$902.33
Labor/Testing			\$36.20
Total			\$938.53

7.3. Volume and Weight

The inverter was designed to fit into the existing chassis built by Azure Dynamics and can be directly used for in-vehicle testing. Therefore, the design was not to optimize the volume and weight but to focus on the efficiency and reliable operation. For example, the measured weight is 15kg, 3 times the DOE weight target, which assumes liquid cooled system. If our heat sink is removed, the overall weight is less than 5kg, which is not far from DOE target. For the volume, the case of Azure Dynamics chassis is 12.5 liter, which is almost 3 times the DOE target but not by design.

Table 7.3 compares the specification of the VT soft-switching inverter and DOE inverter target. The VT design satisfies electrical performance and efficiency targets, but not size and weight. Some conditions were not tested due to the limitation of the electric motor and the control loop stability. For example, the electric machine in the final test is a 90-kW induction machine, which has much higher torque but relatively lower speed. The maximum frequency was not tested at 1000Hz due to the complicated dynamometer setup. The designed operating range was from 250 to 450V but only tested from 275 to 375V in steady state due to battery bank voltage range. Since our ultimate goal was to test the inverter to operate with the actual vehicle, some variations on the specification were unavoidable. Our successful in-vehicle test should justify such design variations.

Table 7.3. Comparison of the VT prototype and DOE target

Requirement	DOE Target	VT Results
Continuous power output	30kW	40kW (tested)
Peak power output for 18 seconds	55kW	60kW (tested at startup)
Weight	≤4.6kg	5kg electronics, 10kg heat sink
Volume	≤4.6liter	12.5liter; (25cmx50cmx10cm)
Unit Cost for quantities of 100,000	≤\$275	\$938
Operating voltage	200 to 450V; nominal: 325 V	275 to 375 V tested; nominal: 325 V
Power factor of load	>0.8	0.87 typical
Maximum current per phase	400A	400A
Precharge time--0 to 200Vdc	2s	<1s
Efficiency at 10 to 100% of maximum speed for 20% of rated torque	>97%	>99%
Output current ripple –peak to peak (% of fundamental peak)	≤3	<3%
Maximum switching frequency	20kHz	10kHz
Current loop bandwidth	2kHz	Trade secret of Azure Dynamics
Maximum fundamental electrical frequency	1000Hz	Tested at 150Hz
Minimum isolation impedance-input and phase terminals to ground	1Mohm	>1Mohm
Minimum motor input inductance	0.5mH	0.14mH
Ambient operating temperature	-40 to +140°C	Not tested

8. CONCLUSION

Three generations of the advanced soft-switching inverter were progressively developed to achieve ultrahigh efficiency while avoiding excessive cost penalty. The first-generation variable timing, soft-switching inverter was based on a newly developed integrated liquid-cooled soft-switching module. The module characteristics of conduction, switching, and thermal resistance were measured to predict efficiency and junction temperatures first. The efficiency of the three-phase soft-switching inverter was then measured with an inductive load and motor-dynamometer. A peak efficiency higher than 99% was found with power meter measurement, but the accuracy of the power meter became doubtful at higher power outputs. Therefore, the inverter was then tested with a calibrated differential calorimeter for long-time (8 hours) operation. The calorimeter inlet and outlet temperature increases were then used to find the inverter loss for efficiency calculation. The results of calorimeter tests show efficiencies between 98.5% and 99% for loads between 12 kW and 27 kW. As compared to the DOE target of 97% efficiency, the proposed soft-switching already exceeded the goal in the first phase effort.

In addition to efficiency measurements, we also performed extensive FMEA analyses and measured EMI for CISPR-25 compliance. The FMEA results suggest that the auxiliary diodes that are not carrying steady-state current need to be sized large enough to avoid catastrophic device failure during controller malfunction or loss of communication between the DSP controller and the power circuit board. The EMI measurement results show significant high frequency EMI reduction with the soft-switching inverter. Overall, the first-generation soft-switching inverter was successfully developed to demonstrate superior performance in efficiency and EMI.

The effort in the development of the second generation soft-switching inverter was to reduce both cost and volume. The cost reduction was achieved by using more standard low-profile module package. The volume reduction was achieved by using smaller magnetic cores. However, the low-profile module had higher internal parasitic resistances due to chip layout and resulted in additional conduction losses. Nevertheless, the parasitic inductance reduction was noticeable, and the switching noise was significantly reduced.

For the third generation inverter, two soft-switching inverters were constructed and fully tested to higher than the full power range. With the nominal 325-V, 30-kW continuous rating, the actual tests were conducted at three different voltage ratings: 275, 325, and 375 V and three different speed and torque ranges: 3000rpm/100Nm motoring, 1000rpm/200Nm motoring, and 1000rpm/100Nm regenerating. The highest power tested was 39-kW continuous, 30% higher than the specification. The peak power is rated at 55-kW, but it is under transient condition, making the waveforms difficult to capture, and thus the 55kW results are not reported.

The major discrepancies between the test conditions and the specifications of the original Request for Proposals (RFP) are:

1. Voltage levels: the RFP voltage range is between 200 and 450 V. Our test range is between 275 and 375 V. There are two main reasons. The first reason is due to our auxiliary power supply operating range. In order to have a standalone unit, the power

supply is designed have the DC bus as the input and is not good for very wide input voltage range for a high efficiency design. The second reason is the motor control loop stability. The control loop is not suitable to operate at every point under different voltages. At low voltages, it cannot operate in high speed because the supply voltage is lower than the equivalent back electromagnetic force (EMF). At high voltages, the control loop gain increases, and the stability margin is reduced. Through initial tests, we decided to stay within 275 and 375 V range, which works quite well even in real life operation.

2. Temperature operating range: The RFP requires the inverter to operate at 105°C temperature condition. Through our Gen-1 inverter test, we found the main issue of high-temperature operation was the DC bus capacitor and other circuit components such as opto-couplers and current sensors. The power module temperature rise was never a problem with our high-efficiency design. Therefore, we only developed a forced-air cooled package for the Gen-2 inverter and natural convention cooling for Gen-3 inverter, and the actual test temperature was under room temperature condition.

Experimental results of Gen-3 inverter with the total loss projected by the temperature rise indicated that at the nominal 325-V input, 30-kW output, the efficiency was 99%, and at 375-V input, 38-kW output, the efficiency exceeded 99.3%. The inverter also succeeded in-vehicle testing. With a 15-minute city block driving cycle, the heat sink stayed as cold as the outdoor temperature. The maximum current and power recorded during the in-vehicle test were 380 A and 40 kW, respectively.

Key accomplishments include:

1. Completed vehicle level simulation to verify the inverter voltage and current levels at different speed and torque conditions. According to the simulation, semiconductor devices were selected and characterized power for hard- and soft-switching and room temperature and 105°C conditions.
2. Developed a scaled soft-switching inverter with variable timing control showing measured efficiency above 98.5% in a wide load range. Two scaled version variable timing controlled soft-switching inverters.
3. Designed and laid out three generations of soft-switching modules and associated gate drive circuits. Three generations of soft-switching inverters and the DSP interface were designed and built accordingly. The Gen-1 soft-switch module was integrated with chilled plate. Tested a scaled version soft-switching inverter with both RL and motor loads.
4. Tested the scaled inverter with dynamometer under speed reversal conditions.
5. Developed the ratio-metric calorimetric loss measurement method.
6. Failure mode effects analysis for a robust inverter design consideration.
7. Projected junction and inside chassis temperatures using finite element analysis
8. Number of circuit board reductions: Gen-2 module requires two gate drive boards, one power bus board, and associated connectors and mounting bracket. Gen-3 module requires only one gate drive board and one power board. Both boards can be stacked on each other, thus avoiding the external connector and mounting bracket.

9. Thick copper laminated power circuit board: Gen-2 module requires an external power bus bar to conduct the main current. Gen-3 module has a heavy-copper based printed circuit board serving as the current carrying path while reducing inductance significantly.
10. Three-phase board integration: The printed circuit board can be easily integrated in a three-phase configuration to eliminate the external power bus bar to further reduce the cost.
11. Elimination of power screw terminals: Gen-3 module eliminates all the power screw terminals and brings power terminals directly out of the chip to allow significant parasitic inductance reduction. The parasitic inductance reduction of the resonant circuit loop was demonstrated in the Gen-2 module. However, the conducting path from MOSFET to the main screw terminal was too far, resulting in a significant increase in the conduction loss. In Gen-3 module, the loop inductance reduction also allows significant reduction in the conduction path of the MOSFET.
12. Elimination of main diode: The MOSFET used in Gen-3 module has a body diode that has a large enough chip area to conduct the freewheeling current, thus the main diode used in Gen-1 and Gen-2 module can be completely eliminated. This should clearly reduce the cost of the final product.
13. Achieved ultrahigh efficiency operation with the Gen-3 module. A set of dynamometer testing was performed to verify the operation under high speed, high torque, and regeneration operation. Peak efficiency was found at 99.3% under 3000-rpm, 100-Nm test condition.
14. Completed in-vehicle testing with the Gen-3 inverter. The inverter was retrofitted into the Citivan all-electric test vehicle for the road test. A 15-minute drive cycle was recorded. With only one 3-W fan cooling, at the end of the drive cycle, the heat sink temperature rise was less than 5°C.

Overall, the soft-switching design achieved major performance improvements in conduction loss and parasitic inductance reduction, and cost reduction through elimination of circuit boards, connectors, and main diodes. Ultrahigh efficiency operation allows complete elimination of the cooling system.

Although not all the DOE design targets were met, this project has demonstrated some breakthrough designs that should change the conventional wisdom on what a traction motor drive inverter should be. The efficiency of the newly developed soft-switching inverter suggested that natural convection cooling is possible with the soft-switching design. In fact, the soft-switching idea in conventional wisdom was to eliminate the switching loss, but an additional new concept should be the reduction of conduction losses by using resistive-drop devices such as super-junction MOSFETs in parallel with IGBTs. With significant progress on super-junction semiconductor devices in the last decade, it is possible for the soft-switching inverter to reach 99.5% peak efficiency within another year or two if the development path continues. In this case, it is unnecessary to have any external cooling system, and the cost saving on the cooling system should allow room for inverter cost margin. The clean input current with soft-switching along with the elimination of the high temperature cooling loop should also allow the use of conventional capacitors and avoid any expensive high temperature capacitors.

We suggest future work should continue on power module package cost reduction and inverter circuit integration. Our projected entire inverter cost is about three times the DOE target, and the major cost item is the soft-switch module. With significant progress on super junction power MOSFET development in recent years, it is possible to reduce the chip count and the material cost, but the packaging technology needs further improved to cut down the soft-switching module cost. Integrating the main and auxiliary modules into one module for each phase leg or integrating all three phase main and auxiliary modules into one module should also help reduce the packaging cost. Similar integration can also be applied to the rest of the inverter circuitry to reduce the number of circuit boards and interconnections. More circuit integration can not only reduce the cost, but also improve the reliability.

GLOSSARY

A	– Ampere, a current unit
AC	– Alternate current
AlN	– Aluminum nitride
APEC	– Applied Power Electronics Conference and Exposition
CISPR	– Comité International Spécial des Perturbations Radioélectriques
CM	– Common mode
CoolMOS	– A commercial MOSFET trademarked by Infineon
DBC	– Direct bond copper
DC	– Direct current
DM	– Differential mode
DQ	– direct-quadrant axes
DOE	– Department of Energy
DSP	– Digital Signal Processor
Dyno	– Dynamometer
EGC	– Ethylene-glycol
EMF	– Electromagnetic force
EMI	– Electromagnetic interference
ESL	– Equivalent series inductance
ESR	– Equivalent series resistance
FEA	– Finite element analysis
FMEA	– Failure Mode Effect Analysis
GPM	– Gallon per minute
H	– Henry, an inductance unit
Hz	– Hertz, a frequency unit
IEEE	– Institute of Electrical and Electronics Engineering
IGBT	– Insulated Gate Bipolar Transistor
J	– Joule, an energy unit
kHz	– Kilo Hertz, a frequency unit
kVA	– kilo volt-ampere, a power unit
kW	– kilo watts, a power unit
LISN	– Line impedance separation network
LPT	– Light punch through
MDMesh	– A commercial MOSFET trademarked by ST Microelectronics
MG	– Motor-generator set
mJ	– milli Joule, an energy uint
mH	– milli Henry, an inductance unit
MHz	– Mega Hertz, a frequency unit
MOSFET	– Metal Oxide Semiconductor Field Effect Transistor
MPH	– Miles per hour
Nm	– Newton Meter, a torque unit
NPT	– Non-punch through
PCB	– Printed circuit board
PI	– Proportional-Integral
PT	– Punch through

PWM	– Pulse Width Modulation
RPM	– revolution per minute, a unit for rotational speed
RMS	– Root means square
RTD	– Resistive temperature detector
SiC	– silicon carbide
SVM	– space vector modulation
V	– Volt, a voltage unit
Virginia Tech	– Virginia Polytechnic Institute and State University
W	– Watt, a power unit
ZVS	– Zero voltage switching

PUBLICATIONS AND PATENTS

A. Journals

1. P. Sun, J.-S. Lai, C. Liu, W. Yu, "A 55kW Three-Phase Inverter Based on Hybrid-Switch Soft-Switching Modules for High Temperature Hybrid Electric Vehicle Drives Application," *IEEE Trans. on Industry Applications*, June 2012.
2. W. Yu, J.-S. Lai, and S.-Y. Park, "An Improved Zero-Voltage-Switching Inverter Using Two Coupled Magnetics in One Resonant Pole," *IEEE Trans. on Power Electronics*, April 2010, pp. 952-961.

B. Conference Proceedings

1. J.-S. Lai, "Hybrid Switch Based Soft-Switching Inverter for Ultrahigh Efficiency Traction Motor Drives," to appear in *Proc. of IEEE Energy Conversion Congress and Exposition*, Sep. 2012, Raleigh, NC.
2. P. Sun, J.-S. Lai, H. Qian, W. Yu, C. Smith, J. Bates, and B. Arnet, A. Litvinov, and S. Leslie, "Efficiency Evaluation of A 55kW Soft-Switching Module Based Inverter for High Temperature Hybrid Electric Vehicle Drives Application," in *Proc. of IEEE Applied Power Electronics Conference and Exposition*, Palm Springs, CA. Feb. 2010, pp. 474-479.
3. P. Sun, J.-S. Lai, H. Qian, W. Yu, C. Smith, and J. Bates, "High Efficiency Three-Phase Soft-Switching Inverter for Electric Vehicle Drives," in *Proc. of IEEE Vehicle Power and Propulsion Conference*, Dearborn MI, Sep. 2009, pp. 761-766.
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C. Patent Disclosures

1. J.-S. Lai, Wensong Yu, and Huijie Yu, "Soft-Switching Inverter Module," VTIP 08-075 Invention Disclosure, Provisional Application on July 22, 2008.
2. J.-S. Lai and Wensong Yu, "Soft-Switching with Variable Timing," VTIP 09-009 Invention Disclosure, Provisional Application on July 22, 2008.
3. J.-S. Lai and Wensong Yu, "A Hybrid Switch for Soft-Switching Inverter Efficiency Improvement," VTIP 08-080 Invention Disclosure, US Patent filed on August 10, 2010.

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