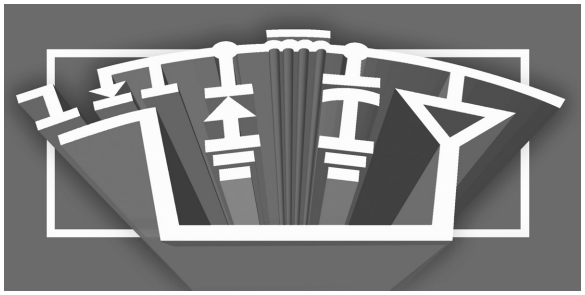

Power Supply Design Seminar

Dual Half-Bridge DC/DC Converter with Wide-Range ZVS and Zero Circulating Current

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Dual Half-Bridge DC/DC Converter with Wide-Range ZVS and Zero Circulating Current

Zhong Ye, Ph.D.

ABSTRACT

A new converter topology that is both high power and digitally controlled combines two half-bridge inverters to operate as a full-bridge power stage using phase-shifting control, but with zero circulating current. Each power switch operates with a nominal 50% duty cycle to achieve zero-voltage switching over a widely varying load, but can also function in PWM mode for increased voltage range. A 1-kW, 385-V/48-V converter designed to validate the concept achieved both 96+% efficiency and high power density.

I. INTRODUCTION

One of the most popular topologies for high-power and high-density switching converter designs is a phase-shifted, full-bridge DC/DC converter (Fig. 1). Favored because of its capability for zero-voltage switching (ZVS) operation, which minimizes switching losses, this converter configuration is described in detail in Texas Instruments application note U-136A [1]. However, a large circulating current in this topology causes significant conduction loss at heavy loads, while at light loads the circulating current becomes too little for switches to achieve ZVS. Both characteristics impact the ability to achieve maximum efficiency. Reducing circulating circuit and extending soft switching over a wider load range are two key areas to improve a phase-shifted, full-bridge converter's performance. Related development information is provided in Appendix A.

This topic explores a new approach to improve power-conversion efficiency. It is well known that an open-loop, half-bridge bus converter operating with the switching duty cycle near 50% can optimally utilize magnetic components and achieve ZVS and high efficiency over a wide load range. Such a converter does not and cannot regulate its output voltage because the PWM is fixed. However, if two such converters operate together in phase-shift mode and superimpose their inverter stage outputs on a common output filter, the circuit can maintain the bus converter's merits while regulating its output voltage. This topic will introduce this topology and provide detailed circuit operation and test results for a 385-V/48-V, 1-kW, dual half-bridge DC/DC converter prototype.

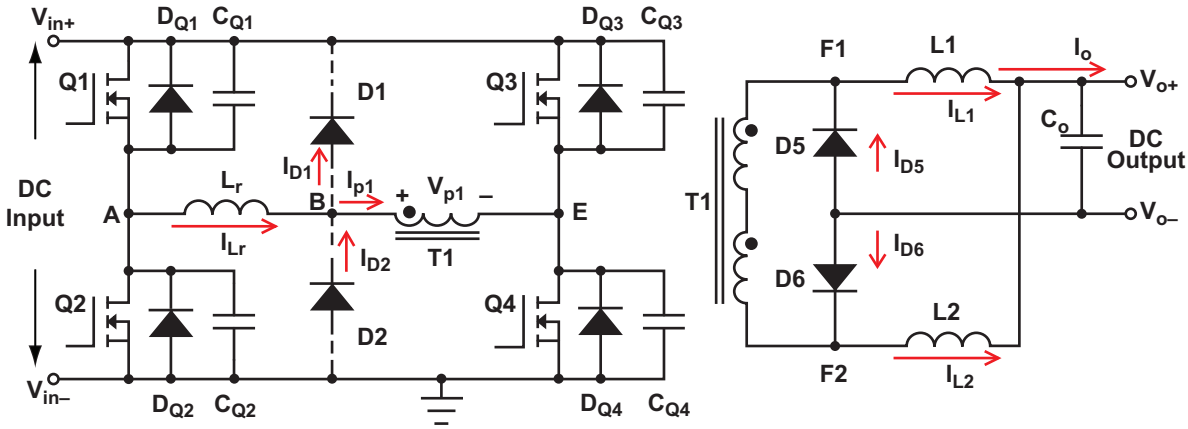


Fig. 1. A phase-shifted, full-bridge DC/DC converter.

II. The Topology and Control of a Dual Half-Bridge DC/DC Converter

A modified open-loop half-bridge bus converter can have a configuration like that shown in Fig. 2. Its output is a current-doubler filter and its power transformer's secondary center tap is connected to power ground. When the primary switches, Q1 and Q2, operate complementally at a 50% switching duty cycle, the inverter outputs a symmetrical square voltage waveform. Because the secondary winding of the inverter's transformer is center-tapped, it can be viewed as two interleaved forward-converter outputs—connected in parallel but with a 180º phase offset between the two outputs. This allows the current-doubler filter to fully cancel its output current ripple such that both the power transformer and the output inductors operate in an optimal 50% duty-cycle condition.

With transformer design techniques that consider magnetizing inductance and proper-dead time control for the bridge primary switch, the primary switch's parasitic capacitance can be fully discharged by the transformer's leakage inductive energy before the switches are turned on. With such control, the converter can maintain ZVS over a wide load range. This open-loop bus converter is one of few topologies that can achieve both high efficiency and power density.

If two of such converters are combined to operate like a full-bridge structure and share a single output filter, a new topology concept—a dual half-bridge DC/DC converter—is created (see Fig. 3). A detailed dual half-bridge configuration is shown in Fig. 4.

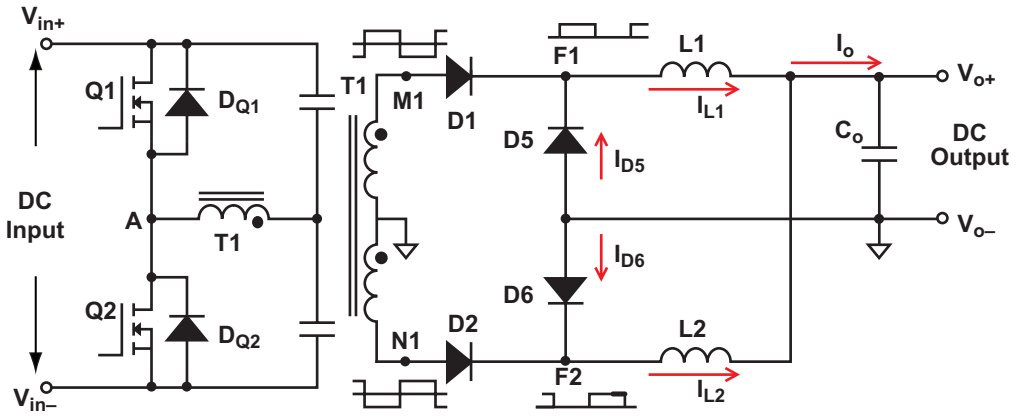


Fig. 2. Modified open-loop half-bridge bus converter.

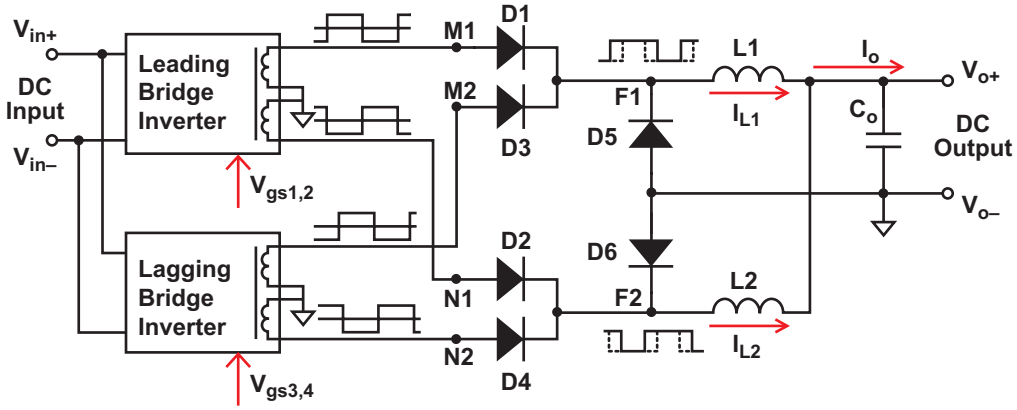


Fig. 3. Block diagram of a dual half-bridge DC/DC converter.

The circuit shown in Fig. 4 has two half-bridge inverters; however, under phase-shift control, one will provide a leading phase while the other supplies a lagging phase. They will be identified as such, where the action of the leading half bridge initiates each output pulse and the lagging half bridge terminates it.

A resonant inductor (L_r) and two clamping diodes (D1 and D2) are added to the leading inverter to perform the same function as in a conventional phase-shifted full bridge [2]. The inductor stores extra energy to extend the soft-switching range and reduce the reverse recovery current of the secondary-side rectifier diodes, while the clamping circuit minimizes converter voltage ringing on both the primary and secondary sides of the transformer.

The two inverters can vary their phase offset from zero to 180°. When the phase offset is zero degrees, (the inverters are in phase) the two inverters operate in parallel, which works in the exact same way as a modified open-loop bus converter. At this operating point, the converter's duty cycle is 0.5 (50%). When the phase offset is 180°, the two inverters still output two square voltage waveforms, but since they are now out of phase, they superimpose on the current-doubler filter input nodes (F1 and F2), making the converter's duty-cycle effectively 1.0 (100%) and the output current very close to DC.

Key waveforms with the phase-shift control are shown in Fig. 5. The two inverters are still operating in open-loop bus-converter mode. During the time (t_{lag}) when the phase-lag offset (φ) is greater than zero degrees, each inverter transfers power to a different half side of the current-doubler output filter. During 180° – φ, the two inverters transfer power to the same half side of the filter. The current of the other half side of the filter is freewheeled by diodes D7 or D8.

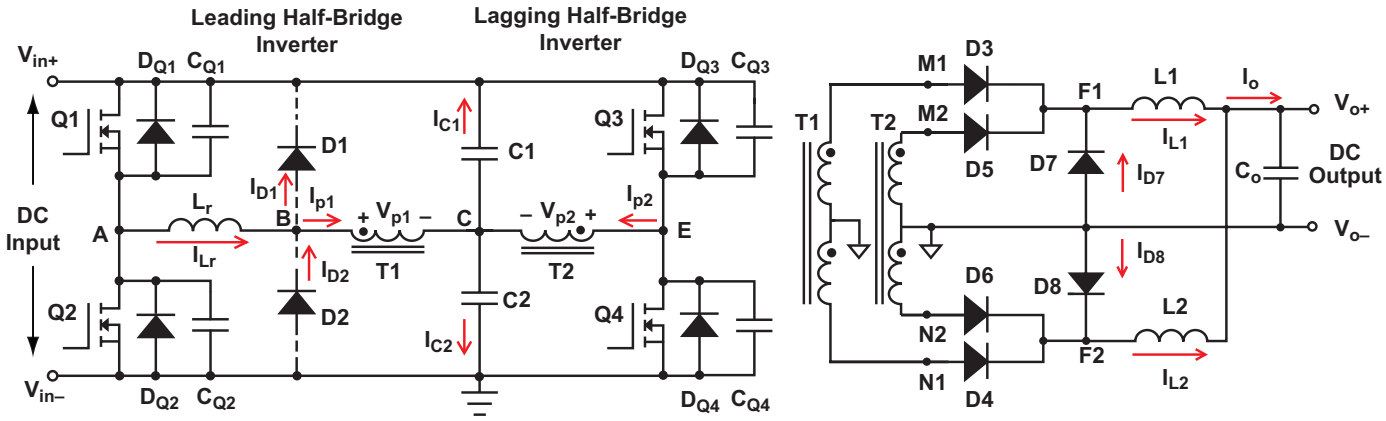


Fig. 4. Detailed dual half-bridge DC/DC converter.

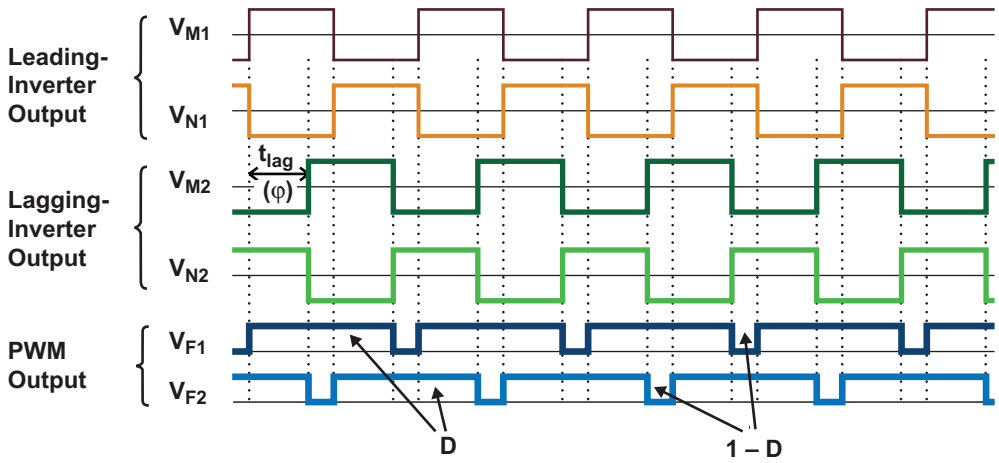


Fig. 5. Key waveforms at phase-shift mode.

If the power transformer's turn radio is n:1:1, the converter input/output voltage relationship is described as

$$V_o = 0.5 \times V_{in} \times \frac{0.5 + \frac{\varphi^\circ}{360^\circ}}{n} \quad (1)$$

and the converter's duty cycle is

$$D = 0.5 + \frac{\varphi^\circ}{360^\circ}. \quad (2)$$

This converter actually transfers power from the primary side to the secondary side during both D and 1 – D periods. This important feature indicates that power is always flowing from primary to secondary at any moment. It is also the reason why there are no circulating currents on the primary side, and substantiates the possibility that this converter could be suitable for high-density designs.

Since φ can only vary from zero to 180º, the minimum regulated output voltage will be 0.5 × V_{in}/n. To have a lower regulated voltage (which happens during power-supply startup, overload and short circuit), the converter needs to switch to PWM mode control.

Fig. 6 shows the switching between phase-shift mode and PWM mode. By using PWM control, the converter can regulate its output down to zero volts, but the two inverters will lose soft switching. A DC/DC power-supply startup normally takes less than 100 ms, so hard switching during this time will have very little effect on overall circuit performance and efficiency.

To avoid component damage, it is a common practice for a converter to respond to a short circuit by shutting down and restarting for a few seconds several times. A converter's thermal constant is usually much longer than a few seconds, so hard switching should not cause thermal stress during this operation.

Another possible cause for damage is overload. When overload occurs, constant power or current control could allow a converter's output to stay somewhere below half of the maximum output voltage, 0.5 × V_{in}/n. Under this scenario, the converter will have to deliver maximum current while operating under hard switching. If it lasts too long, thermal stress could be an issue. However, such cases are usually managed with shutdown controls.

For a 48-V output rectifier, for example, the maximum output voltage is usually designed at 60 V or below. Downstream DC/DC modules or backup batteries would shut down the system before the 48-V bus voltage drops down to 30 V. If this is the case for a given application, the dual half-bridge converter topology could be a good candidate for the design.

When using diodes for rectification, the converter's output-inductor current can become discontinuous when the load becomes light enough and its control loop could adjust the switching duty cycle below 50%. With the decrease of the duty cycle, the half-bridge's top- and bottom-side MOSFETs have a much larger equivalent deadtime. During deadtime, because of the circuit's parasitic

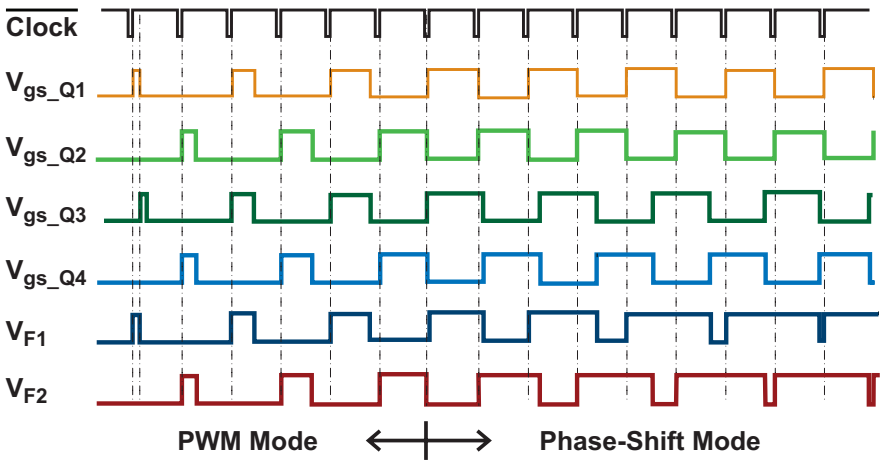


Fig. 6. PWM and phase-shift mode switching.

capacitance and leakage energy, the half-bridge's switching node briefly rings, then settles down at half of the DC bus voltage. If the bus voltage is half nominal, the switching losses are reduced to approximately one-fourth what they would be at the nominal input voltage when the switches are turned on. Because switching loss dominates the total loss at light loads, this natural characteristic of a half-bridge topology would help improve efficiency. And because the two inverters have the same switching duty cycle and operate independently, one inverter can actually be turned off—further reducing the switching loss by half. This is another important feature of this topology.

III. Circuit Operation

To better address the complete operation sequence of this topology, refer once more to the dual half-bridge converter with the diode rectification circuit shown in Fig. 4. The converter's two half-bridge inverters always operate at a 50% switching duty cycle when the output voltage is regulated above half of its maximum input voltage. The magnetizing currents of the power transformers reach a constant and stable peak value at the end of each half switching cycle, assuming that there is no magnetic flux walking and that the circuit operates in continuous conduction mode (CCM).

When one half-bridge's switch is turned off (and during the deadtime before the complementary switch is turned on), the magnetizing current and reflected-output current fast charge and discharge the switching devices' parasitic capacitance until the voltage across the power transformer windings decreases to zero. Both leading and lagging inverters work in the same way in this first part of the commutation period. After that, the lagging inverter continues its commutation by utilizing its magnetizing energy (since its transformer secondary is basically open), while the leading inverter relies on the energy of its power-transformer leakage inductance and resonant inductor to activate a resonation between the inductance and the switches' parasitic capacitance.

A transformer's properly sized magnetizing inductance can usually store enough energy for the lagging bridge to achieve ZVS regardless of the output load. Because magnetizing current only applies to the lagging bridge's parasitic capacitance, the voltage slew rate of the lagging-bridge's switching node becomes much softer during this commutation period compared with a conventional phase-shifted full-bridge converter.

The operation process of the circuit can be divided into five time intervals beginning with t1, which is the end of the last cycle in the sequence. Key waveforms of the circuit operation are shown in Fig. 7. The circuit operation in each time interval is shown in Fig. 8.

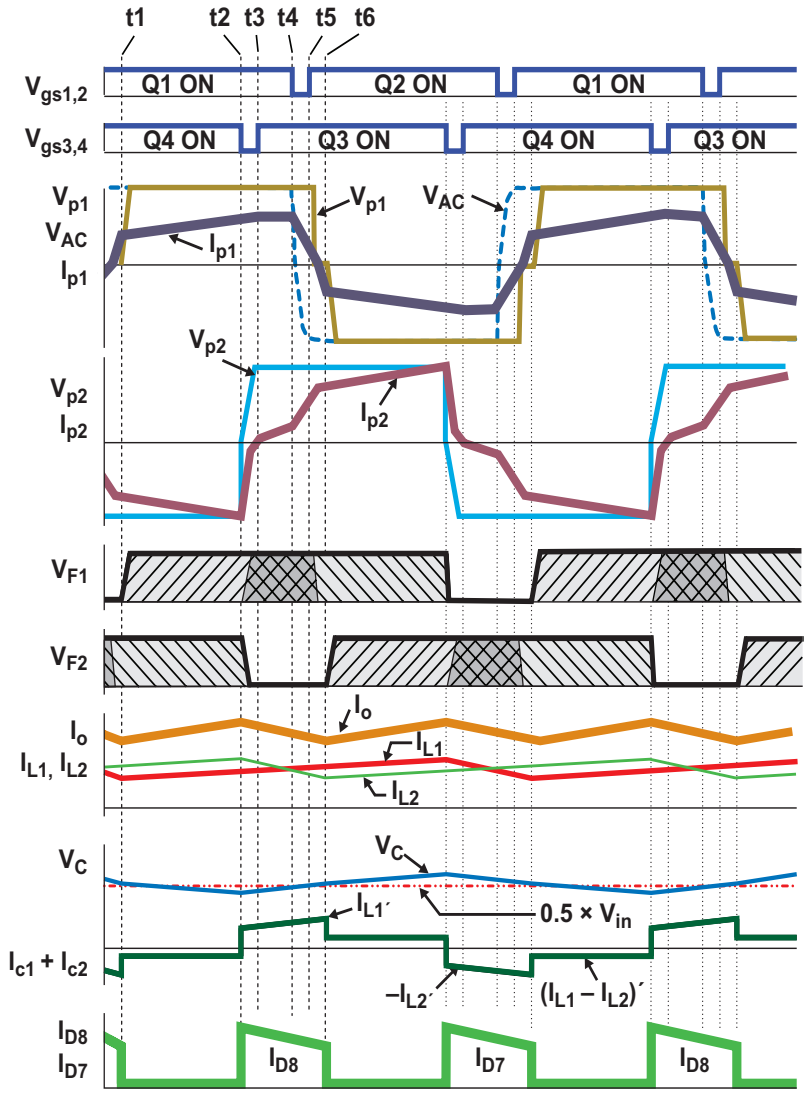


Fig. 7. Key waveforms of a dual half-bridge DC/DC converter.

Mode 1 with t1 ≤ t < t2 (see Fig. 8a)

During this period, switches Q1 and Q4 are on. The t1 time is the moment when freewheel diode D7 ends its reverse recovery. The reverse-recovery current of diode D7 is reflected to transformer T1's primary. Most of its corresponding energy, residing in inductor L_r, is captured by clamping diode D1. The rest of the energy residing in the primary- and secondary-side leakage inductance of T1 cannot be captured by the clamping diode, and could cause some voltage ringing at node N1. To minimize the voltage ringing, the leakage inductance of T1 should be minimized. The captured current (I_{D1}) circulates within the loop formed by Q1, L_r and D1 and begins to decline due to the conduction loss of the loop. Half-bridge capacitors, C1 and C2, are connected to T1 and T2's primary windings, respectively. Their voltages are coupled to the secondaries and then applied to the output filter through the output rectifiers (D3 and D6). Energy is transferred from the primary sides to the secondary sides during this time period, therefore the inductor currents (I_{L1} and I_{L2}) are increasing.

C1 and C2 equally divide the bus voltage. Since the two transformers' primary currents cancel each other when they pass through capacitors C1 and C2, the capacitor voltage ripple can be controlled to a small value, with relatively small capacitance. The capacitors' peak-to-peak ripple can be calculated by the following equation:

$$V_{C\_ripple} = \frac{(2D-1)(1-D)\times V_o}{4n\times D\times L_o\times C\times f_s^2} + \frac{(1-D)\times I_o}{2n\times C\times f_s}, \qquad (3)$$

where D is the converter's duty cycle, C is the total capacitance of half-bridge capacitors C1 and C2, n is the transformer turns ratio, and f_S is the switching frequency. The capacitor ripple reaches its peak value at full power with a 0.5 converter duty cycle.

Mode 2 with t2 ≤ t ≤ t3 (see Fig. 8b)

At t2, transistor Q4 is turned off. After Q4 is turned off, capacitor C_{Q4} is charged up almost linearly by the reflected L2 current (I_{L2}). After its voltage surpasses C2's voltage and transformer leakage energy is fully discharged, the voltage across transformer T2 reverses its polarity and becomes positive. Freewheel diode D8 conducts and takes over the I_{L2} current from D6 such that D6 becomes electrically disconnected. The leading bridge maintains its previous state and continues to apply a voltage to node F1 through diode D3, while both output rectifiers D5 and D6 of the lagging bridge remain open. During this period, capacitor C_{Q4} is continuously charged up by T2's magnetizing current. The worst-case scenario is when the load is zero. The magnetizing inductance is the only current to charge C_{Q4} and discharge C_{Q3}. To achieve ZVS, the lagging bridge's switch deadtime should meet the following requirement:

$$t_{d\_lagging} \geq 8f_s \times L_{T2} \times (C_{Q3} + C_{Q4}), \qquad (4)$$

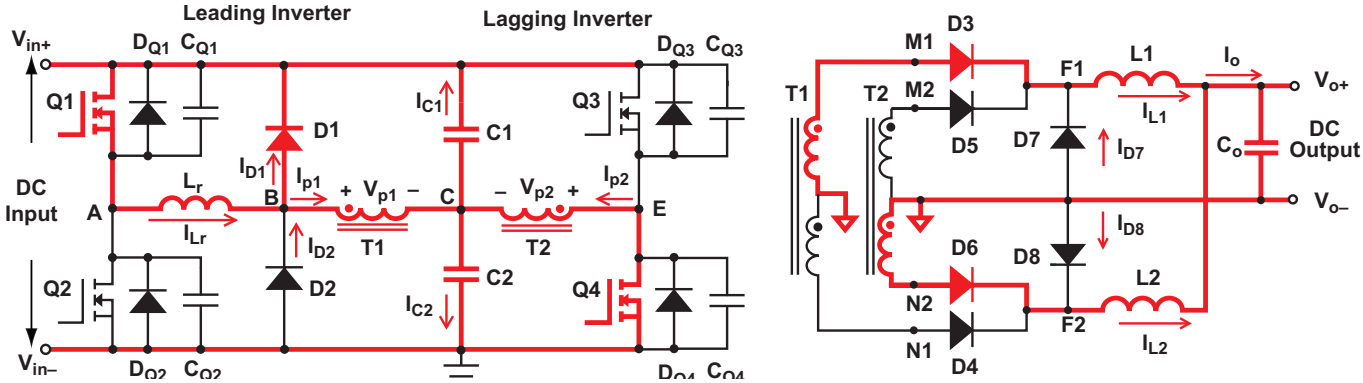
where f_S is switching frequency and L_{T2} is the magnetizing inductance of transformer T2.

The reverse recovery of rectifier D6 could cause D6 and D8 to conduct at the same time and T2's output is essentially shorted for a short period. The short circuit can lock magnetizing current inside T2 and affect the dead time selection.

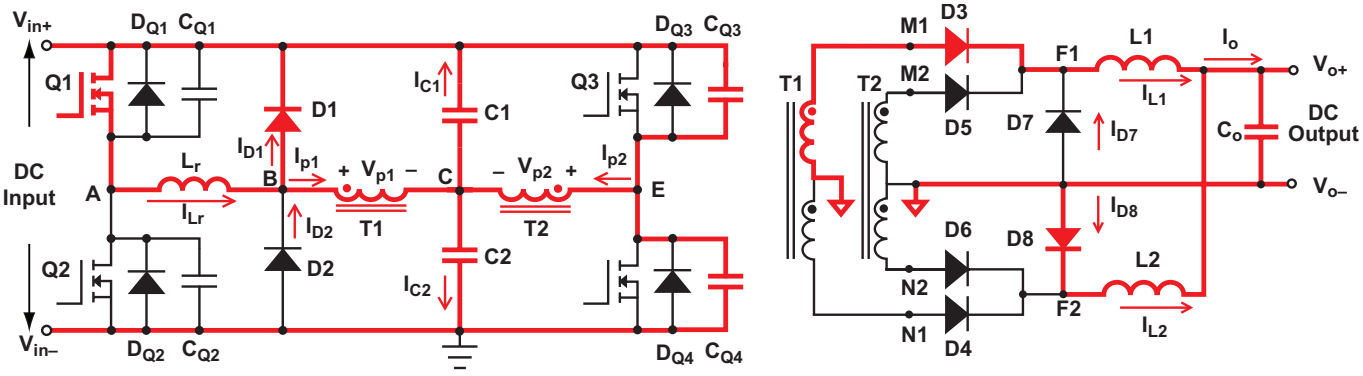
Before Q3 is turned on at t3, C_{Q4} is fully charged up and switching node E is clamped to the input DC source by Q3's body diode (D_{Q3}). Note that C_{Q3} is fully discharged when C_{Q4} is charged up to the DC input voltage. Therefore, Q3 is turned on with zero voltage across it. When C_{Q4} is charged up to the DC input voltage, T2's output voltage (V_{M2}) reaches the same level of T1's output (V_{M1}). Output rectifier diode D5 conducts softly and the leading and lagging inverters begin to share their output current, I_{L1}.

Mode 3 with t3 < t < t4 (see Fig. 8c)

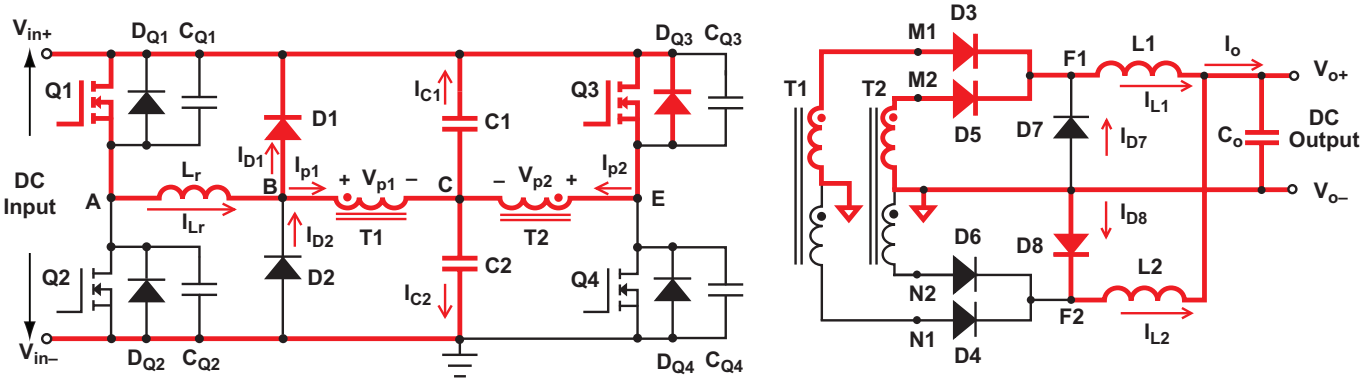
During this period, the two inverters share their output current (I_{L1}). Because the two transformer outputs (V_{M1} and V_{M2}) have almost the same voltage, the current shifting from the leading half bridge to the lagging half bridge is usually slow. Therefore, the leading half bridge usually shares more output current than the lagging half bridge during this time period. In the meantime, freewheel diode D8 maintains its previous state such that conducting currents I_{L1} and I_{L2} start to decrease as V_o applies to L2 with reverse polarity. The decrease of I_{L2} and the increase of I_{L1} lead to a partial current-ripple cancellation, minimizing output ripple voltage.



a. Mode 1 (t1 ≤ t < t2).



b. Mode 2 (t2 ≤ t ≤ t3).



c. Mode 3 (t3 < t < t4).

Fig. 8. Current paths of a dual half-bridge converter in one operation cycle.

Mode 4 with t4 ≤ t < t5 (see Fig. 8d)

At t4, Q1 is turned off. Parasitic capacitance C_{Q2} is discharged. Parasitic capacitance C_{Q1} is charged by the resonant inductor current (I_{Lr}) which includes T1's magnetizing current, the reflected inductor current (I_{L1}) shared by the leading inverter and the captured reverse recovery current of freewheel diode D7 in Mode 1. With the current sharing shifting from the leading inverter to the lagging inverter, I_{Lr} decreases. D3 maintains conduction until I_{Lr} decreases to the magnetizing current value. During this period, C_{Q2} can be completely discharged if the converter output current reaches a certain level and the resonant inductor (L_r) has sufficient energy stored. If the stored energy is not sufficient, D3 turns off softly before C_{Q2} is completely discharged. The voltage across T1 (V_{p1}) starts to decrease and eventually reverses its polarity. Output inductor current (I_{L2}) is still passing through D8 for CCM, so T1's secondary is essentially shorted by D4 and D8. Therefore, T1's magnetizing current (energy) cannot further contribute to the discharge of C_{Q2}. Resonant inductor L_r, however, can continue to resonate with C_{Q1} and C_{Q2} to fully discharge C_{Q2} if the resonant inductor's value meets the following criteria:

$$L_r = 16 \times f_s^2 \times L_{T1}^2 \times (C_{Q1} + C_{Q2}), \qquad (5)$$

where L_{T1} is the magnetizing inductance of leading inverter transformer T1. By inserting a proper deadtime (t4 – t5), Q2 can be turned on at t5 with a zero voltage across it. Here we assume that clamping diodes D1 and D2 have no turn-off delay. If the delay is comparable with half the period of the small-resonance network, the L_r value will have to increase to as much as twice the calculated value. The reverse-recovery current of freewheel diodes D7 and D8 is the major cause of the delay.

For optimal operation, the leading bridge deadtime should be:

$$t_{d\_leading} = \arcsin\left(\frac{V_{bus} / (I_{Lr\_m} \times X_r)}{\omega_r}\right) \qquad (6)$$

and

$$t_{d\_leading} \le \frac{0.5\pi}{\omega_r}, \qquad (7)$$

where

$$\omega_r = \frac{1}{\sqrt{L_r \times (C_{Q1} + C_{Q2})}},$$

$$X_r = \sqrt{\frac{L_r}{C_{Q1} + C_{Q2}}},$$

I_{Lr_m} is resonant inductor (L_r) current when resonation just starts, and V_{bus} is the maximum voltage switching node A can swing.

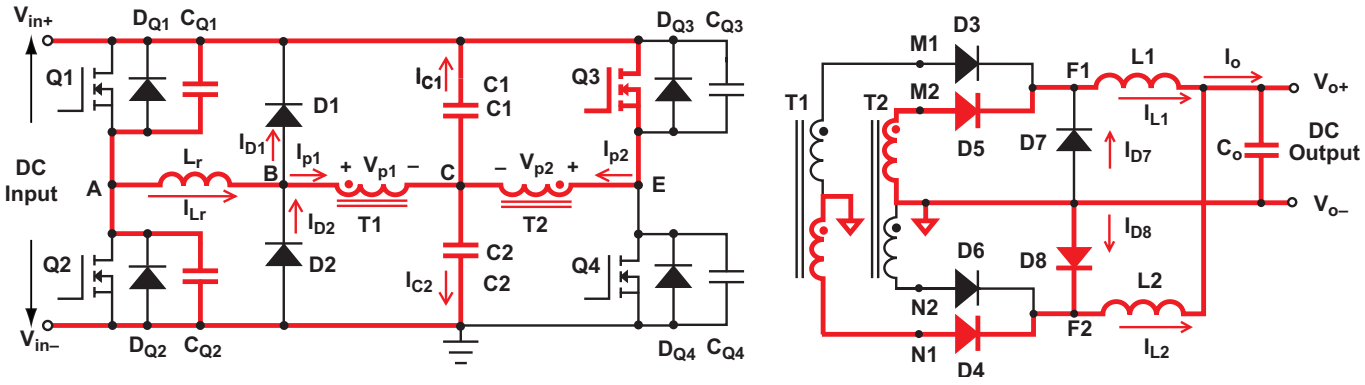
If clamping diodes D1 and D2 have significant turn-off delay compared with the deadtime, V_{bus} should use V_{in} for the calculation, otherwise V_{bus} should be $0.5 \times V_{in}$. This calculation is a good starting point for deadtime setting. To achieve the best efficiency, the final deadtime setting should be fine tuned per test results.

Mode 5 with t5 ≤ t < t6 (see Fig. 8e)

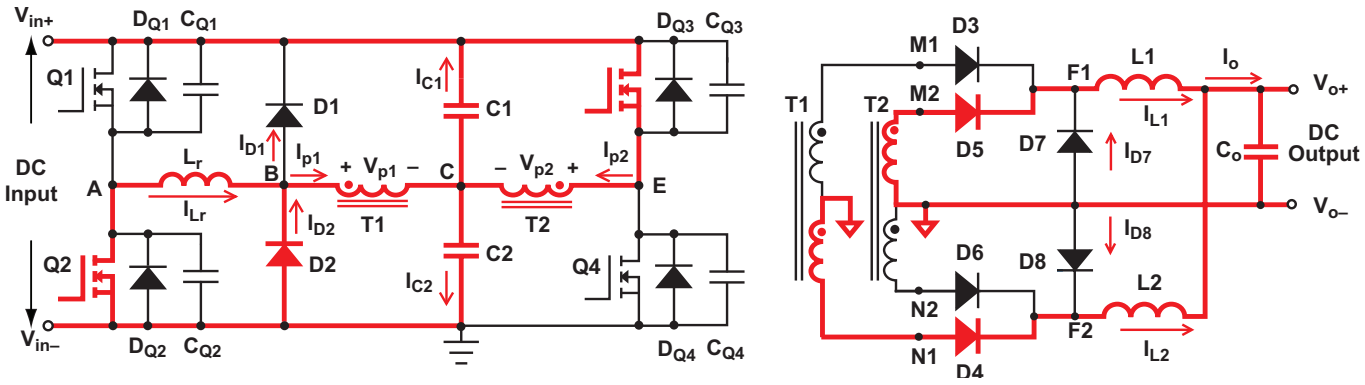
After Q2 is turned on at t5, the inductor current (I_{Lr}) decreases to zero quickly and then begins to build up in the opposite direction. When its reflected current at the secondary surpasses output current (I_{L2}) and D8's reverse-recovery current, D8 stops conducting at t6.

Time t6 is the end of one half-cycle. The process then repeats for the next half-cycle with the complementary components operational. Each complete switching cycle consists of two complimentary half-cycles.

During startup, overload or light load, the converter needs to operate in PWM mode. For this mode, as described previously, the converter is effectively a hard-switching half bridge with two paralleled inverters and a modified current-doubler output. The PWM gate signals applied to the two inverters are in phase. The operation process of



d. Mode 4 (t4 ≤ t < t5).

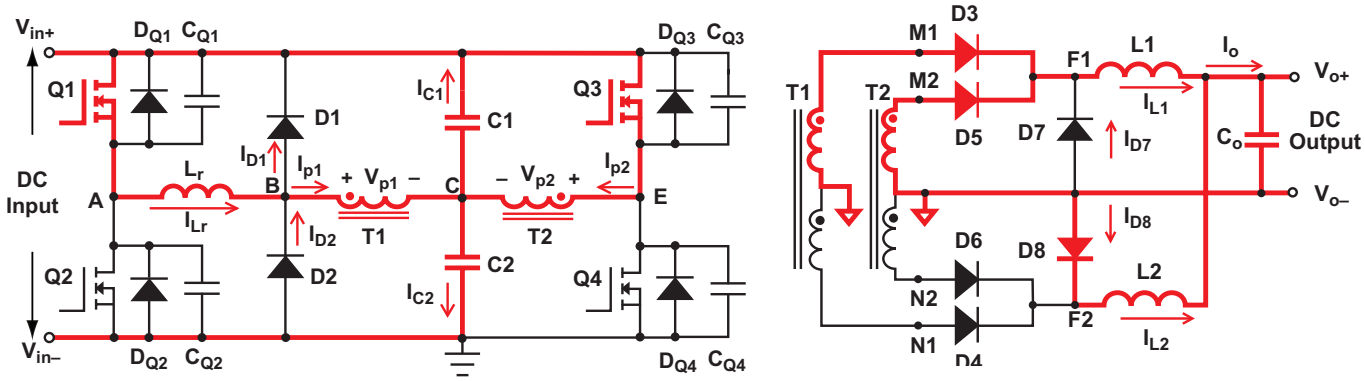


e. Mode 5 (t5 ≤ t < t6).

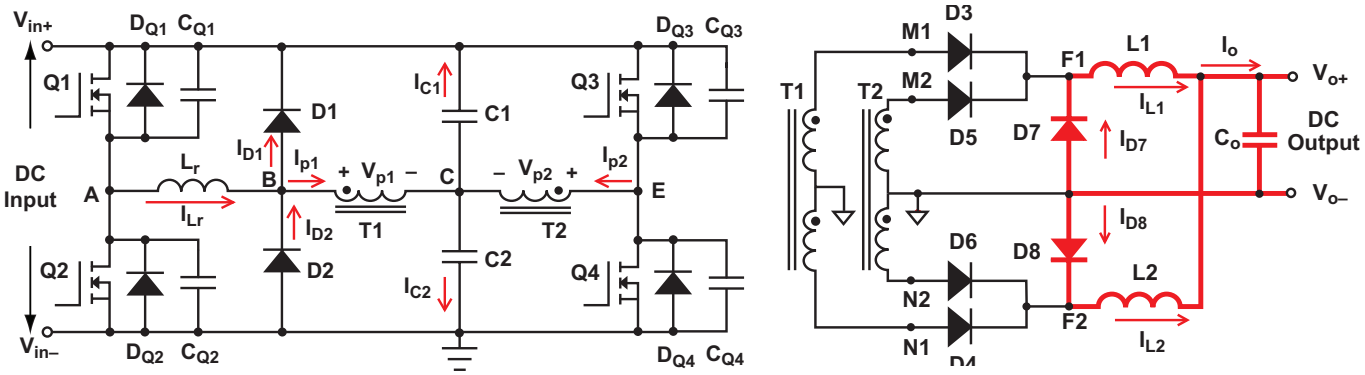
Fig. 8 (continued). Current paths of a dual half-bridge converter in one operation cycle.

this circuit can be divided into three time intervals; the current path of each time interval is shown in Figs. 9a, 9b, and 9c. To save switching loss at light loads, one inverter can be turned off while the other continues to operate and regulate the converter's output voltage. This is a unique feature of this topology.

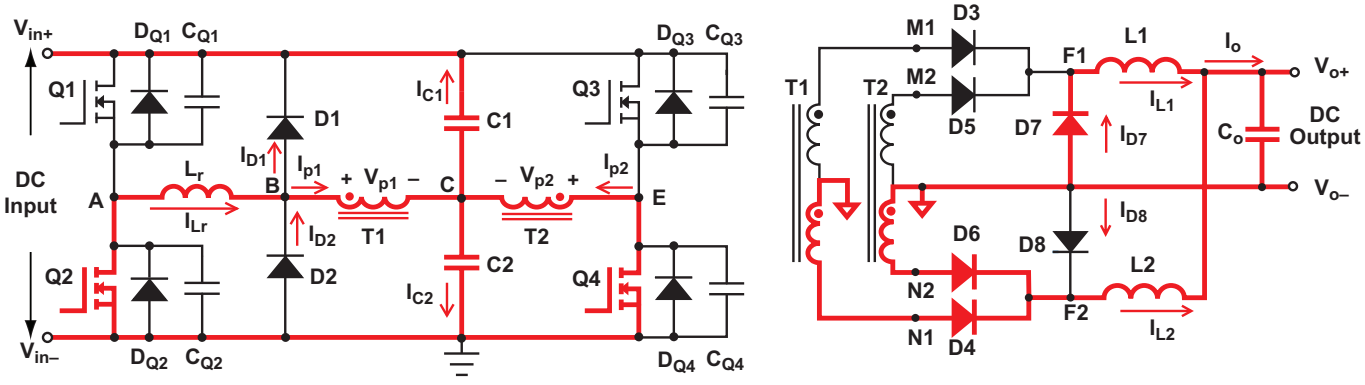
To provide a full range of output-voltage regulation, the circuit needs to operate in both PWM and phase-shift modes and switch from one mode to the other seamlessly. A popular phase-shift control chip (UCC3895), with external analog circuits, is still able to do the job, but digital control provides far more flexibilities for such sophisticated control and simplifies external circuits significantly. To dynamically change the deadtime of the bridge switch and turn on or off one half bridge for better efficiency at different load conditions, a digital controller is a better choice.



a. Both top-side FETs are on.



b. All FETs are off (freewheel mode).



c: Both bottom-side FETs are on.

Fig. 9. A dual half-bridge DC/DC converter operating in PWM mode.

A TI Fusion Digital Power™ controller, the UCD3040, was used in the prototype test. TI's UCD3xxx family devices integrate multiple hardware-digitized control loops and an ARM7® microcontroller into one chip. They are optimized for power-conversion applications. A UCD3xxx digital PWM can be configured to operate in the phase-shift mode or a PWM mode, and the mode switching can be controlled by either firmware or hardware itself. The UCD3138 has a built-in hardware-mode switching function. It is also a good candidate for such applications.

IV. Experimental Results

A 1-kW, 385-V/48-V, DC/DC converter was designed to validate the concept and demonstrate the circuit performance. The physical hardware is shown at the end of this topic and a complete schematic for this prototype is in Appendix B. The UCD3040 controller is located on the secondary side. It generates both converter-bridge gate signals and synchronous MOSFET (SyncFET) drive signals. The bridge gate signals are passed to the primary side by TI digital isolator ISO7240, while SyncFETs are driven directly by the TPS2814.

The output rectification circuit was rearranged as shown in Fig. 10 so that both diodes and FETs could be tested on the same power board with a common ground. Freewheel devices D3 and D4 remain diodes to allow the circuit to operate in discontinuous conduction mode (DCM) and avoid the voltage spike caused by the negative-output inductor current. D3 and D4 can be replaced by FETs to decrease conduction loss. For this case, the rectifier FETs and freewheel FETs should have some turn-on overlapping to avoid any voltage spike. As shown in Fig. 10, DC decoupling capacitor, C3, was used to prevent potential transformer magnetic flux walking, since only voltage-mode control was used in this test. Peak-current mode control can be used to eliminate the capacitor if necessary.

The circuit parameters and components used in this test were:

- Primary power MOSFETs: SPW20N60CFD
- Freewheel diodes: V20100
- Output inductor: 34 µH
- Magnetizing inductance: 625 µH
- DC blocking capacitor: 2 x 0.22 µF
- Secondary rectifier: FDP2532 (SyncFET) or V30200
- Resonant inductor: 20 µH (at zero current)
- Power transformer turns radio: 20:7:7
- Half-bridge capacitors: 2 x 0.47 µF
- Main controller: UCD3040 TI digital power controller

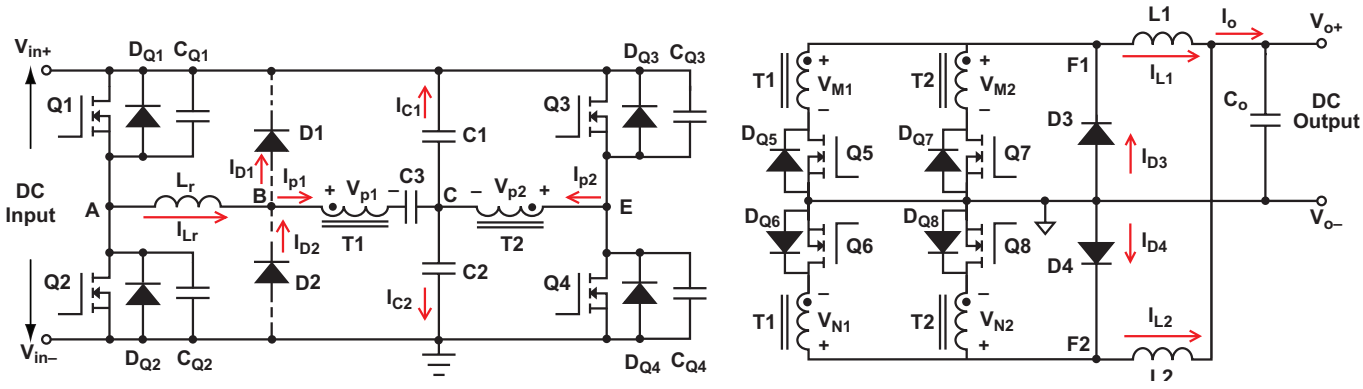


Fig. 10. Prototype dual half-bridge DC/DC converter schematic.

Fig. 11 shows the transformer primary voltage and current experimental waveforms with a 50% load. Both the leading and lagging inverters do not have circulating current, and their voltages and currents are in phase. Fig. 12 shows the switching-node voltage (V_{AC}) waveform of the leading inverter and the resonant inductor current (I_{Lr}). It also includes the transformer voltage and current waveforms of the lagging inverter, which are the same of those shown in Fig. 11. V_{AC} and I_{Lr} waveforms show that they are also in phase. No reactive power is generated by either inverter. The current difference between I_{Lr} shown in Fig. 12 and I_{p1} of Fig. 11 is caused by the reverse recovery of the output freewheel diodes D3 and D4.

Fig. 13 shows the transformer secondary voltage (V_{M1} and $V_{M2)}$ and freewheel diode (D3) voltage (V_{F1}) when the output-rectification circuit uses diodes. $|V_{M1} - V_{M2}|$ is the reverse voltage across the rectifier diodes.

Fig. 14 shows SyncFETs Q5 and Q7's V_{ds} and V_{gs}. All waveforms shown in Figs. 13 and 14 were

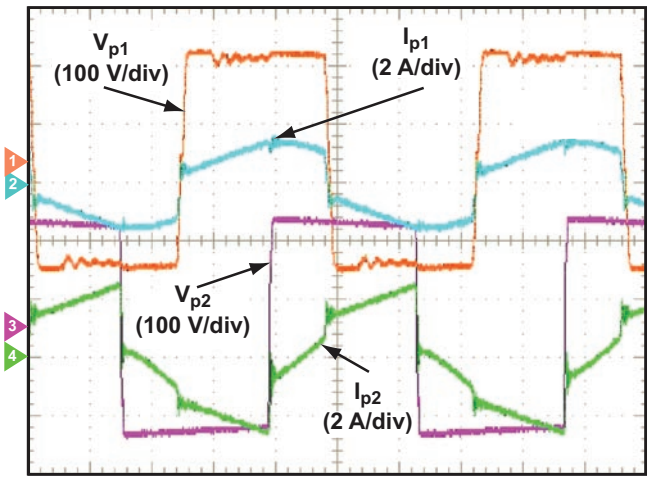


Fig. 11. Transformer primary voltage and current waveforms. (See Fig. 10 for measurement points.)

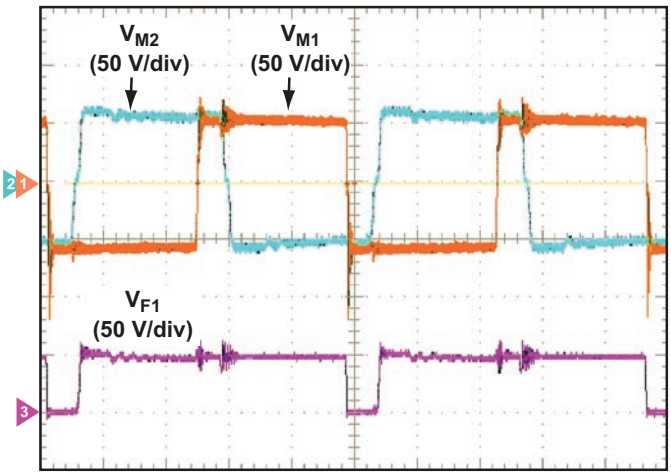


Fig. 13. Transformer secondary and freewheel diode D3 voltage waveforms. (See Fig. 10 for measurement points.)

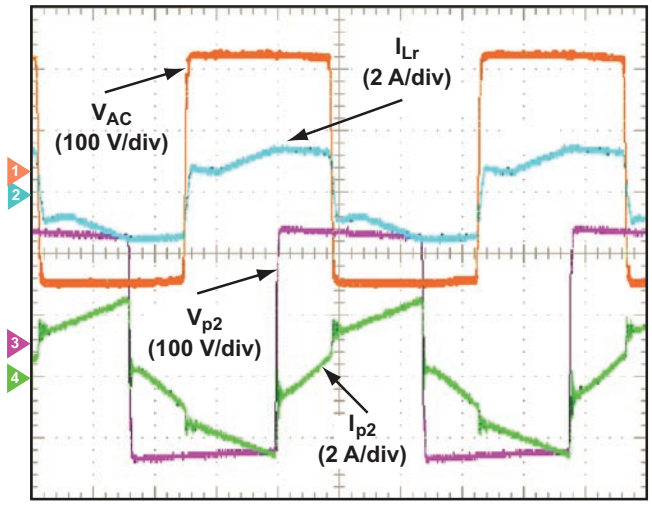


Fig. 12. Switching node and transformer primary voltage and current waveforms. (See Fig. 10 for measurement points.)

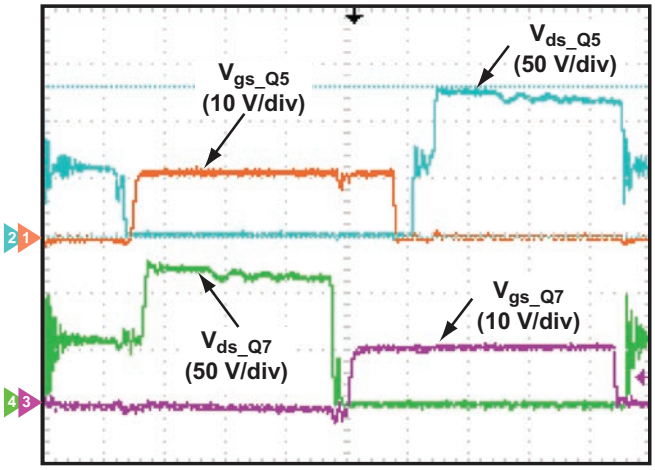


Fig. 14. SyncFET voltage waveforms. (See Fig. 10 for measurement points.)

captured with no snubber added to the rectification circuit. These waveforms demonstrate that clean SyncFET V_{ds} (with almost no voltage spike at different load levels) can be achieved with the proposed topology.

Fig. 15 shows the transformer voltage and current waveforms of the leading and lagging inverters with a 5% load, where both inverters operate in PWM mode. As shown on I_{p1} some oscillation of transformer primary current of the leading inverter is caused by the oscillation between the FET's parasitic capacitance and the resonant inductor. The leading inverter and lagging inverter operate in parallel. Either inverter can be turned off to save switching loss.

Figs. 16 and 17 show that the primary switches achieve ZVS with zero load and a 6-A load. To demonstrate soft switching with zero load, the converter was controlled to maintain phase-shift mode with a fixed phase offset. Its input voltage was decreased so that the output voltage would not trigger overvoltage protection. The converter achieves ZVS even with a zero load. However, during this specific testing, the voltage at switching-node A is oscillating at a frequency determined by the parasitic capacitance of the leading inverter's switches, resonant inductor (L_r), and transformer's leakage inductance. The voltage could also contain some ringing injected at node B during reverse recovery of clamping diodes D1 and D2. The ringing could inhibit the controller's ability to precisely turn on the leading inverter's switches at zero voltage. Thus, the converter may not be able to fully achieve soft switching between 2-A and 5-A loads.

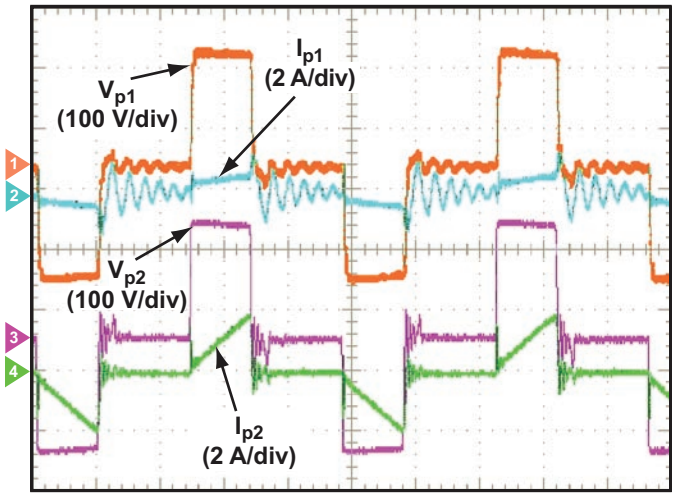


Fig. 15. Transformer primary voltage and current waveforms. (See Fig. 10 for measurement points.)

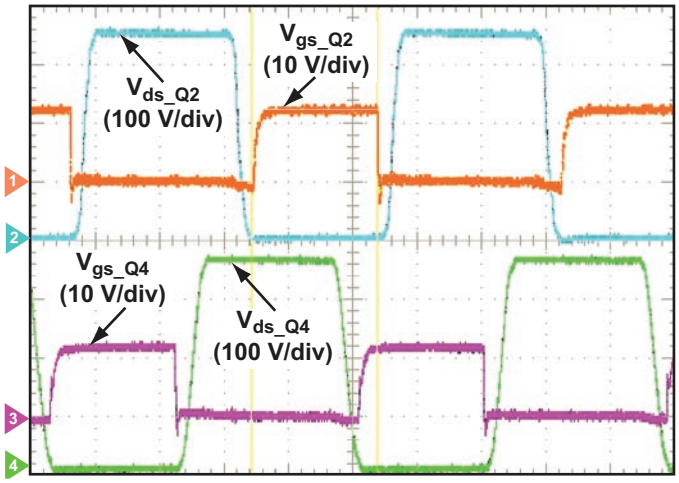


Fig. 16. Leading and lagging inverters achieve ZVS at zero load. (See Fig. 10 for measurement points.)

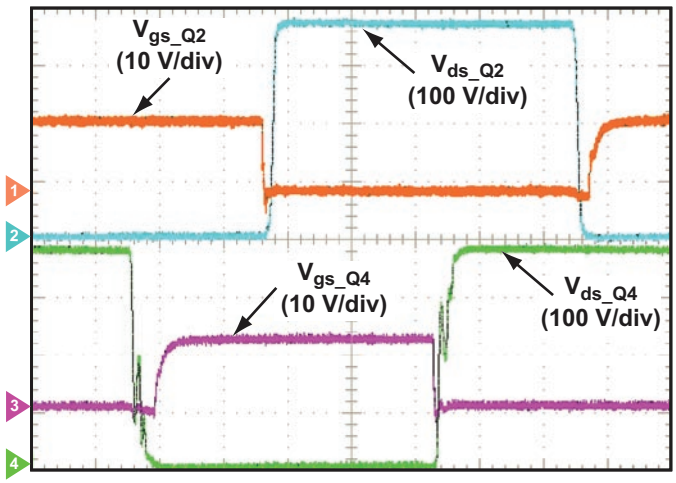


Fig. 17. Leading and lagging inverters maintain ZVS with a 6-A load. (See Fig. 10 for measurement points.)

Fig. 18 provides the efficiency data when the output rectification used diodes as well as SyncFETs. The curves show the 48-V output circuit is able to achieve 95.2% maximum efficiency with a diode-based output rectification, 96% maximum efficiency with a SyncFET rectification circuit, and 92% efficiency at 20% load. When the load was below 7% of the full load, the converter was switched to PWM mode and one half bridge was actually turned off to prevent significant loss. At 0.5-A load, for example, turning one half bridge off saved around 6 W.

The efficiency with a 48-V output was also compared with the LLC converter's efficiency published in APEC 2002's Proceedings [3]. It shows that the two topologies have the almost same efficiency at 50% and above loads. The LLC converter seems to have a better efficiency at light loads, but no efficiency data for loads below 20% was available. Fig. 19 is a photo of the 1-kW, dual half-bridge, DC/DC converter prototype used for all the tests.

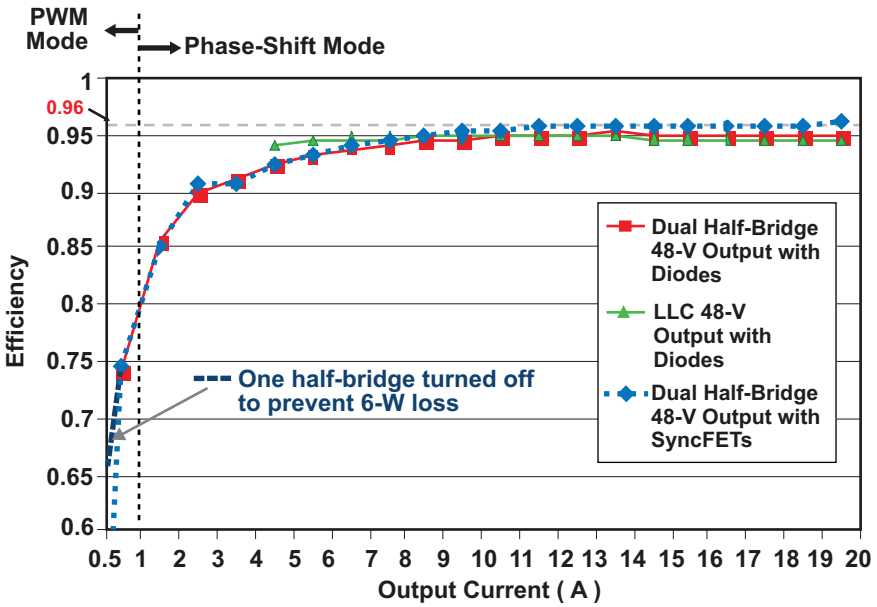


Fig. 18. Efficiency curves of a dual half-bridge DC/DC converter.

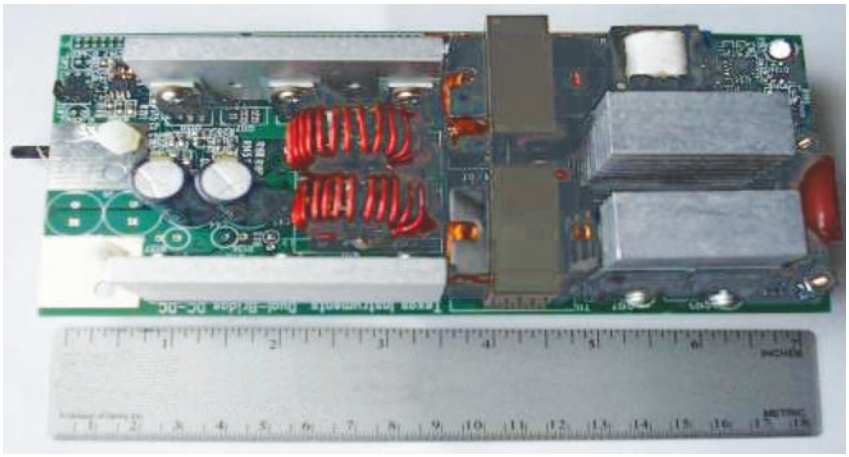


Fig. 19. Prototype of a 1-kW, dual half-bridge, DC/DC converter.

V. Conclusion

The test on the first prototype of the dual half-bridge converter built in the TI Digital Power lab has validated the new topology and control concept and demonstrated the high-efficiency potential of this circuit. This topic explored a different approach to achieving the following goals: Load-independent, wide-range ZVS with efficiency improvement at both heavy and light loads; no circulating current and reactive power; 100% time utilization for power transformation and optimal use of magnetic components; and minimum semiconductor device stress. These are the necessary design elements for a high power density and peak efficiency. The dual half-bridge topology is most suitable for AC/DC power-supply designs that have a preregulated input voltage for its DC/DC stage. It can also be used for DC/DC converter designs that have a relatively narrow voltage ranges for the input-voltage and regulated output. From a packaging point of view, this topology is also a good candidate for high-power, high-density and low-profile designs.

Acknowledgment

The author thanks colleagues Ian Bower for his firmware support and Sean Xu for his assistance with experimental data collection.

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Appendix A. Related Full-Bridge Research and Development

The ZVS full-bridge converter's circulating current causes significant conduction loss at heavy loads, limiting its maximum achievable efficiency. At light loads, the circulating current becomes too little for switches to achieve ZVS. High switching loss at light loads is another drawback of a phase-shifted full-bridge converter. Reducing the circulating current and extending soft-switching over a wider load range are two key areas to improve a phase-shifted full-bridge converter's performance.

To extend the soft-switching range and reduce switching loss at light loads, a resonant inductor is usually added to the converter's primary side. The inductor stores extra energy to extend the soft-switching range and reduce the

reverse-recovery current of the secondary side rectifier diodes. However, this extra energy can also cause a higher voltage spike across the rectifier diodes. A simple but effective clamping circuit can be used to mitigate this problem [2]. The clamping circuit substantially minimizes the converter's voltage ringing on both the primary and secondary sides and captures most of the transient energy on the primary side, which is utilized for soft switching and recycled back to the converter's DC input.

For low output-voltage applications, such as 48 V or below, synchronous MOSFETs (SyncFETs) are often used to replace secondary rectifier diodes to minimize conduction loss. If the SyncFETs remain active, a converter can maintain continuous conduction mode (CCM) operation and a relatively stable duty cycle. Depending on the load, the converter's output-inductor current can be positive, zero or negative at the end of a switching cycle. Both positive and negative currents actually help the primary switches to achieve soft switching. At a certain load point, the output inductor current returns to zero at the end of each switching cycle. For this case, the primary can only rely on its magnetizing current for soft switching. Properly sizing magnetizing inductance and keeping SyncFETs active are good ways to achieve ZVS over a wide load range. At a very light load however, (especially at zero load) the negative current may become so significant that too much energy is cycled back to the primary side, resulting in efficiency loss.

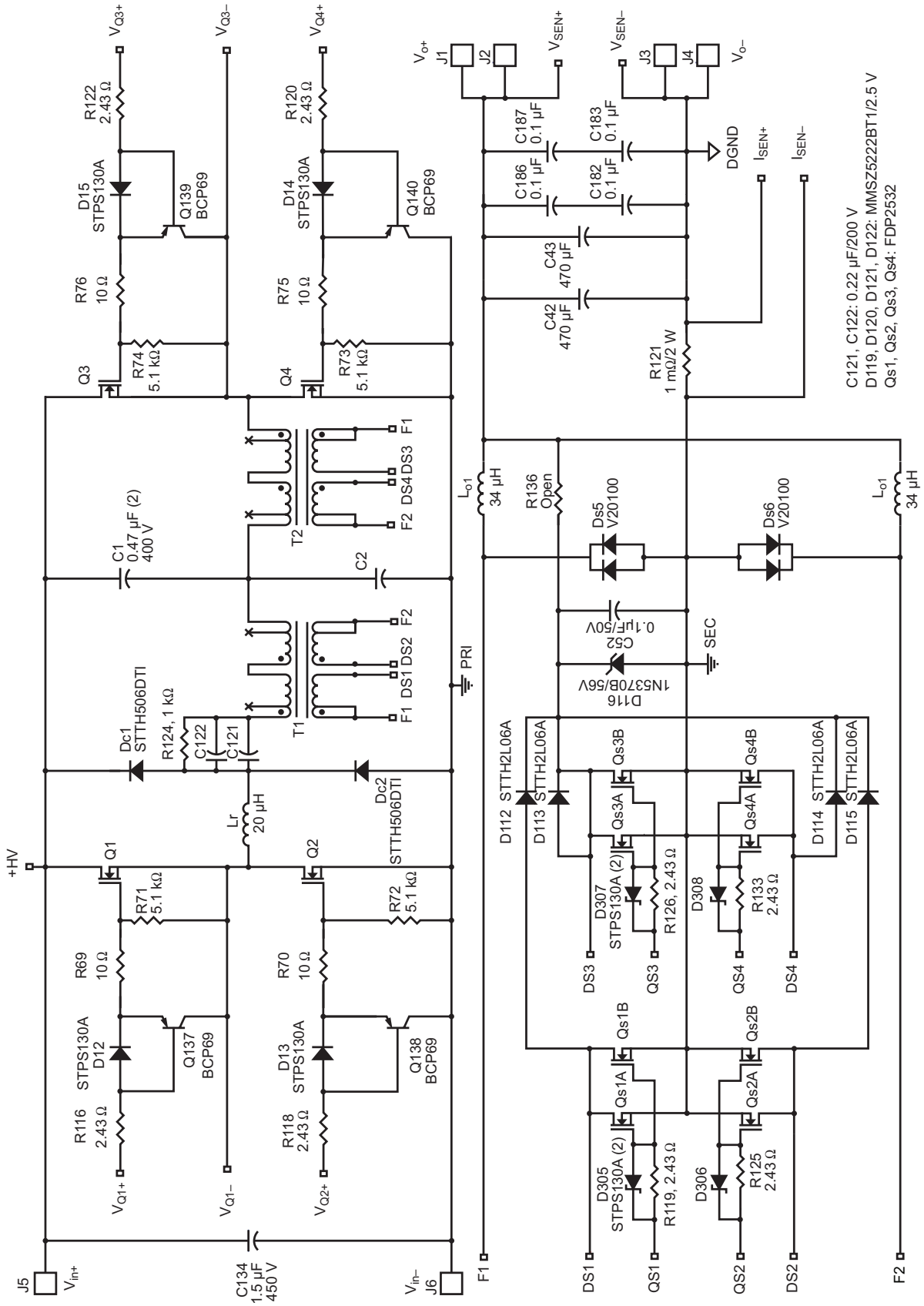
It becomes more challenging to extend the ZVS range when the output-rectification devices are diodes. Many circuits have been proposed to solve this problem. The circuits can be categorized into two types: the first is an active switch-controlled resonance network [4]. Its auxiliary switch(es) can be usually turned on at zero current. It activates a resonation to create a zero-voltage condition for the main switches to turn on. The second type is a passive LC network connecting to the bridge switches [5, 6, 7, 8]. The network produces a load-independent resonant current that helps the bridge switches achieve ZVS over a wider load range. These circuits do indeed increase the ZVS load range, but adding costly and bulky power components would become an issue for a cost-sensitive and space-constrained design.

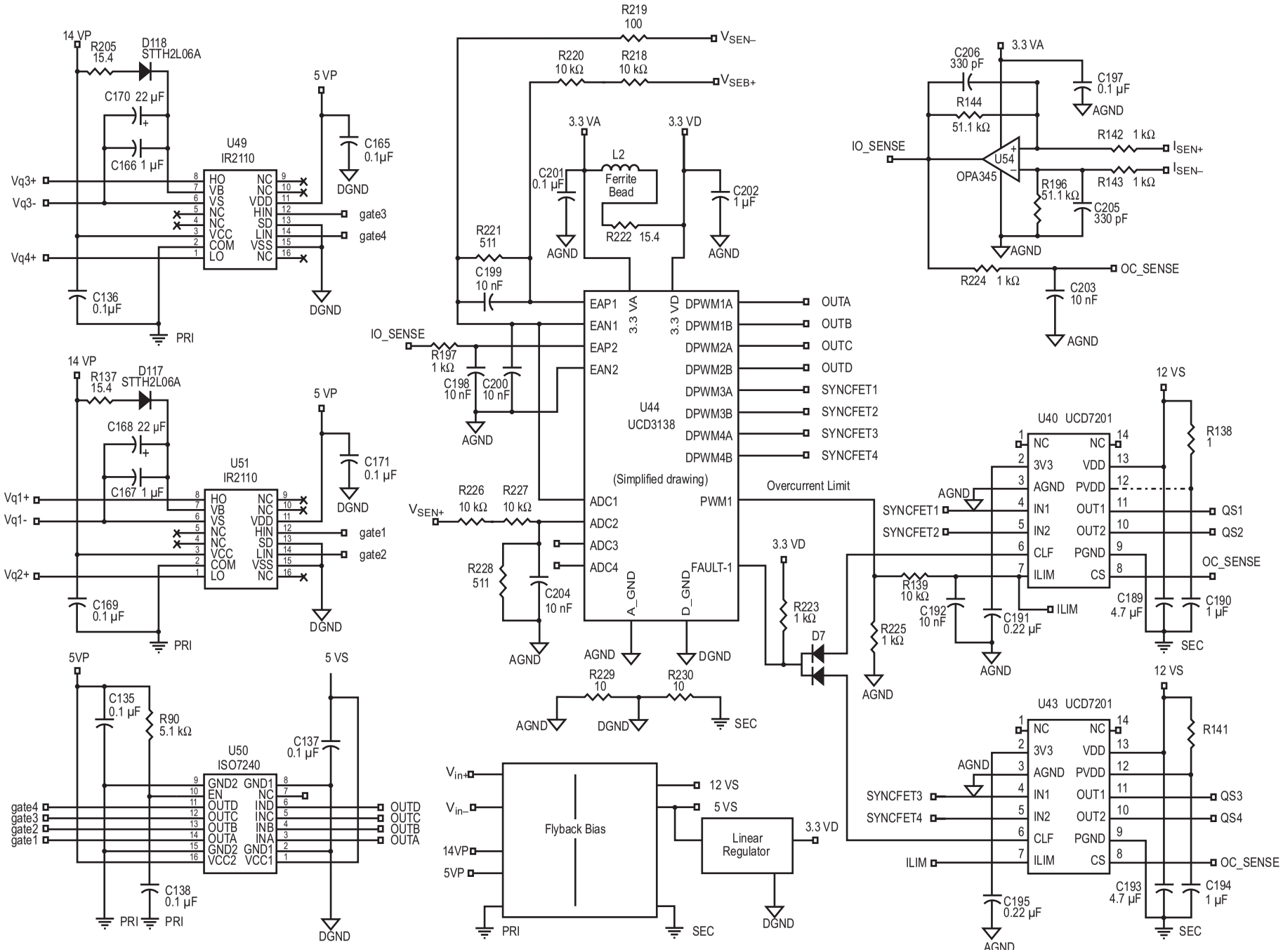
A load-dependent circulating current is one of major drawbacks of the existing ZVS full-bridge DC/DC converters. The circulating current passes through most of the converter's power train during the 1 – D period while no energy is transmitted from the primary side to the secondary side. This causes a substantial power loss. Some resonance networks have been introduced to eliminate the circulating current [8, 9]. However, the resonance network also removes the necessary circulating energy, which is needed for ZVS. These types of circuits would work well for low-frequency applications where low parasitic-capacitance devices, such as IGBTs, are often used.

Another way to eliminate the circulating current is to use asymmetrical control [11]. An asymmetrical-bridge DC/DC converter doesn't have a circulating current but it is able to operate in ZVS mode. The circuit is quite simple and works well, with decent efficiency. It is generally suitable for applications where the DC input and output voltage-variation range is narrow and loop bandwidth is low. Because its primary current passes through the bridge capacitor(s), the capacitance value needs to be relatively large. A large capacitance slows down voltage tracking to PWM duty-cycle variation, while a large step load can easily cause power-transformer saturation. Not many applications based on this control have been seen recently.

In the past few years, a 96% AC/DC telecom rectifier product inspired a wave of research and development of LLC converters [12]. It is indeed good news for this energy-hungry age, but not many successful products have been released to market yet. Significant challenges to today's designs are the wide range of operating frequencies, the complexity of continuous current and power control, PWM/FM mode switching, the difficulties of multiphase interleaving, and precise SyncFET-current crossover detection.

APPENDIX B. DUAL HALF-BRIDGE DC/DC CONVERTER SCHEMATICS




14 VP
R205 15.4
D118 STTH2L06A
C170 22 µF
C166 1 µF
U49 IR2110
HO VB VS NC NC VCC COM LO
NC NC VDD HIN SD LIN VSS NC
Vq3+
Vq3-
Vq4+
gate3
gate4
5 VP
C165 0.1µF
DGND
C136 0.1µF
PRI
14 VP
R137 15.4
D117 STTH2L06A
C168 22 µF
C167 1 µF
U51 IR2110
Vq1+
Vq1-
Vq2+
gate1
gate2
5 VP
C171 0.1 µF
DGND
C169 0.1 µF
PRI
5VP
C135 0.1 µF
R90 5.1 kΩ
U50 ISO7240
GND2 EN OUTD OUTC OUTB OUTA GND2 VCC2
GND1 NC IND INC INB INA GND1 VCC1
gate4
gate3
gate2
gate1
OUTD
OUTC
OUTB
OUTA
C137 0.1 µF
5 VS
DGND
C138 0.1 µF
PRI
PRI
R219 100
VSEN–
R220 10 kΩ
R218 10 kΩ
VSEB+
3.3 VA
3.3 VD
L2 Ferrite Bead
C201 0.1 µF
AGND
R222 15.4
C202 1 µF
AGND
R221 511
C199 10 nF
IO_SENSE
R197 1 kΩ
C198 10 nF
C200 10 nF
AGND
U44 UCD3138
(Simplified drawing)
EAP1
EAN1
EAP2
EAN2
ADC1
ADC2
ADC3
ADC4
A_GND
D_GND
3.3 VA
3.3 VD
DPWM1A
DPWM1B
DPWM2A
DPWM2B
DPWM3A
DPWM3B
DPWM4A
DPWM4B
PWM1
FAULT-1
OUTA
OUTB
OUTC
OUTD
SYNCFET1
SYNCFET2
SYNCFET3
SYNCFET4
VSEN+
R226 10 kΩ
R227 10 kΩ
R228 511
C204 10 nF
AGND
AGND
DGND
R229 10
R230 10
AGND
DGND
SEC
Overcurrent Limit
3.3 VD
R223 1 kΩ
D7
R225 1 kΩ
AGND
C206 330 pF
3.3 VA
C197 0.1 µF
AGND
R144 51.1 kΩ
IO_SENSE
U54 OPA345
R142 1 kΩ
ISEN+
ISEN–
R143 1 kΩ
R196 51.1 kΩ
C205 330 pF
AGND
OC_SENSE
R224 1 kΩ
C203 10 nF
AGND
12 VS
U40 UCD7201
NC 3V3 AGND IN1 IN2 CLF ILIM
NC VDD PVDD OUT1 OUT2 PGND CS
SYNCFET1
SYNCFET2
QS1
QS2
OC_SENSE
ILIM
R138 1
C189 4.7 µF
C190 1 µF
SEC
R139 10 kΩ
C192 10 nF
C191 0.22 µF
AGND
Vin+
Vin–
14VP
5VP
Flyback Bias
12 VS
5 VS
Linear Regulator
3.3 VD
PRI
SEC
DGND
12 VS
U43 UCD7201
NC 3V3 AGND IN1 IN2 CLF ILIM
NC VDD PVDD OUT1 OUT2 PGND CS
SYNCFET3
SYNCFET4
QS3
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R141
C193 4.7 µF
C194 1 µF
SEC
C195 0.22 µF
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