# A Dual-Tuned Active-Inductor-Based LC-VCO and Its Application in a Wideband PLL

by

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B.A.Sc., University of Toronto, 2006

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF

MASTER OF APPLIED SCIENCE

in

The Faculty of Graduate Studies

(Electrical and Computer Engineering)

THE UNIVERSITY OF BRITISH COLUMBIA
(Vancouver)

August 2010

# Abstract

A wideband phase-locked loop (PLL) allows chip designers to use a single PLL for multiple communication standards. In wireline transceivers, such a wideband PLL can be incorporated as a part of a programmable (software-defined) de-serializer, or replace several PLLs for multiple standards if the bands are not used simultaneously. This thesis presents the design of a wideband PLL targeting wireline communication standards with clock frequencies between 0.5 and 5 GHz. To the author's knowledge it is the first wideband PLL using an active-inductor-based VCO and its measured performance results compare favorably, especially in power and area, with state-of-the-art wideband PLLs. Further contributions include: the derivation of the lumped-element model of the PMOS-based two-stage active-inductor, noise contributions of the active-inductor VCO, and a compensated charge pump to reduce locked phase offsets.

Design targets a 0.13-µm CMOS process. In simulations with extracted parasitics, the active-inductor VCO covers the desired 0.5 to 5 GHz range with a small margin. It exhibits coarse and fine VCO gains of 12.8 and 1.48 GHz/V, respectively, across the entire tuning range. The phase noise of the VCO is less than or equal to –78 dBc/Hz at a 1 MHz offset from the carrier. As compared to simulations, the measured maximum operating frequency of the VCO is reduced by 12 %, spanning frequencies up to 4.4 GHz. The measured phase noise degrades by approximately 10 dBc/Hz.

The PLL uses a phase-frequency detector to lock to incoming signal across its entire frequency range and a linear compensated phase detector to achieve less than 5° phase offset between the incoming and locked clocks and a measured output jitter of 1.3 $ps_{rms}$ for a VCO output frequency of 4 GHz. The PLL consumes between 34 mW and 48 mW.

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# List of Acronyms

| | |
|---|---|
| AI | Active inductor |
| ASIC | Application specific integrated circuit |
| $C_{gs}$ | Capacitance between the transistor gate and source nodes |
| $C_{gd}$ | Capacitance between the transistor gate and drain nodes |
| CDR | Clock and data recovery |
| CML | Current mode logic |
| FD | Frequency detector |
| FO4 | Fanout of four (see footnote #1, page 5) |
| IC | Integrated circuit |
| I/O | Input / output |
| LC | Inductor and capacitor |
| PD | Phase detector |
| PFD | Phase-frequency detector |
| PLL | Phase-locked loop |
| RMS | Root mean squared |
| VCO | Voltage controlled oscillator |
| $V_{DS}$ | Transistor drain-source voltage |
| $V_{GS}$ | Transistor gate-source voltage |
| $V_{TH}$ | Transistor threshold voltage |

# Acknowledgements

I would like to thank Professor Shahriar Mirabbasi for all his guidance and support throughout this process. His patience and advice made this work possible. Thank you for this opportunity.

I wish to thank Dr. Roberto Rosales & Roozbeh Mehrabadi for their extensive help with lab equipment, test setup and design, and all kinds of software debugging and support.

To Sadegh Jalali and Alireza Sharif-Bahktiar, thank you for all of the technical support, as well as being available as sounding boards and company in the lab.

I am thankful to my family & friends for helping to keep me focused, but not too focused, and for all the support throughout my degree.

To Rebecca Saari, for whom no amount of praise is sufficient, my most heartfelt thanks and love.

It should also be noted that this research was supported in part by Intel Corporation, the Natural Sciences and Engineering Research Council of Canada (NSERC), and Canadian Microelectronics Corporation (CMC Microsystems).

*To Rebecca:*

*Ou tu iras, je te suivrai*

# 1. Introduction

This chapter provides the motivation for a wideband PLL and an active-inductor-based LC-VCO. It then examines the options for implementing the required and desired circuit blocks and their state-of-the-art design.

## 1.1. Motivation

As the number of transistors on a chip increases, system designers are able to use the system-on-chip paradigm to lower the cost and provide better value to the end user. The term system-on-chip (SoC) is used to describe integrating all the processing and input/output (I/O) blocks of a system on a single chip. This means more functionality on a single chip, but also higher complexity. In these chips, it is feasible to include more than one communication standard to provide cross-compatibility or meet various needs. Combining communication standards and protocols into a single receiver or transmitter block helps to reduce the overall system complexity and bill of material, and can reduce power consumption and area by eliminating otherwise required circuitry. If a single block is insufficient, for example if parallel communication is required, using a single repeated block for multiple protocols increases design reuse and reduces the number of fully characterized high-speed analog blocks.

High-bandwidth communication protocols like PCIE 1.0 and 2.0 [1], USB 2.0 [2] and 3.0 [3], and SATA 2.0 [4] transmit serial data with clock rates between 0.5 GHz and 5 GHz, and either with a single loosely phase-aligned clock for the entire bus or without a clock at all. This allows the chip to have fewer I/Os and thus lower power. To sample the incoming data a phase and frequency aligned clock must be generated with sufficient strength to drive the sampling circuitry. This is usually accomplished with a phase-locked loop (PLL). When a very precise lock is required, or

the clock is not present, a clock and data recovery (CDR) circuit is necessary. The CDR circuit can be thought of as an extension of the PLL that phase aligns the recovered clock and samples the data. In many clock-less protocols using a pilot tone to help the initial lock is typical, and then a PLL can be used [5].

Previous solutions to generating phase-aligned clocks to multi-band or wideband inputs have been to include either multiple PLLs on a chip or multiple oscillators [6]. Multiple PLLs allow targeted design and protocol-specific specifications. Multiple oscillators allow some standard-specific tradeoffs, but are also required to cover the wide range of frequencies. These duplicate circuits consume excess power that shortens the battery longevity in mobile devices and/or increases the power budget for desktop applications. The increased area to accommodate these multiple blocks decreases chip yield and thus adds to the manufacturing cost. (In general, manufacturing defects occur infrequently, but at a small number per wafer. The more die per wafer means a higher percentage of chips are fabricated without contamination defects.) Finally, more circuitry means more design time and higher development costs.

In the context of wideband PLLs, many designs have focused on frequency synthesis for wideband transmit PLLs [6][7][8][9], which uses an external high-quality crystal to generate a transmit clock. However, the architecture cannot be directly used to phase align with a received clock.

Traditional VCO architectures, including ring and LC-VCO structures, have been applied to this wideband problem; however, they exhibit large area and cumbersome layouts [10] or significant extra circuitry to cover the large frequency range [9]. Active inductors (AIs) are re-emerging as a solution for wideband frequency generation [11] , demonstrating wide range of operation

frequencies [12], lower area than LC-VCO structures [13], and steadily improving phase noise characteristics [14].

## 1.2. Objectives

The objectives/contributions of this work are:

- Design an active-inductor-based LC-VCO with a wideband characteristic operating from 500 MHz to 5 GHz with coarse tuning for wideband operation, and fine-tuning for PLL integration
- Derive the noise contributions of the active-inductor to VCO phase noise
- Design a wide-tracking PLL capable of locking across the entire active-inductor VCO frequency range, maintaining low jitter characteristics on the received clock
- Layout, fabricate, and test the designed circuit blocks

## 1.3. Thesis Organization

The remainder of the thesis is organized as follows. Chapter 2 provides a review of gigabit and multi-band PLL design, including building block implementations, as well as state-of-the-art design of active inductors and active-inductor-based oscillators. Chapter 3 presents the theory and design techniques necessary for multi-band PLLs, circuitry required to implement the PLL including the phase detector and charge pump. It also presents the development of LC-VCO architecture, the implemented active inductor, and the effect of the active inductor on VCO phase noise. Chapter 4 discusses design implementation and the application of theory, difficulties encountered in the design, annotated schematics, and simulation results. Chapter 5 details the measurement approach for silicon validation, and enumerates the required testing equipment. Chapter 7 concludes the thesis and discusses future work.

# 2. Literature Review

This chapter presents the state-of-the-art in gigabit and multiband PLL design, and discusses options in PLL block selection including the phase detector, and VCO. Proven wideband and active-inductor VCO structures available in the literature are reviewed and key concepts are highlighted. The first section discusses the PLL-specific blocks, then section two covers the active-inductor and VCO.

## 2.1. Gigabit and Multiband PLLs

Gigabit PLLs in deep submicron CMOS processes highlight the requirements and design considerations for the high-frequency components necessary to lock to a multi-gigahertz input signal. For example, the phase detector and charge pump must be able to operate at the maximum VCO oscillation frequency and the VCO must be able to drive sampling circuitry directly to minimize skew errors that can be significant as the clock period shrinks [15].

The common design approaches used for wideband PLLs have been to use either multiple loops and/or multiple VCOs to cover the entire bandwidth [9], [8], [6] at the cost of increased area and power consumption. These PLLs also often use circuitry to dynamically update loop parameters in order to change the response of the loop, for example in [16] where the charge-pump current is adjusted to stabilize the natural frequency and damping of the PLL. This technique can help by adapting system specifications to the requirements but increases overall complexity.

The circuit blocks used to implement the PLLs have a large impact on output jitter and achievable frequencies of the output clock. The phase detector or phase frequency detector and charge pump must be able to make the correct decision at the highest clock frequency, even if the phase differences are small [17]. The loop filter has a large impact on the final PLL loop

parameters such as natural bandwidth, damping factor, and output jitter, as well as determining the degree of design orthogonality between these parameters,. The VCO, discussed in Section 2.2, will transfer its noise directly to the output of the PLL and must also be able to function across the entire frequency band.

There are three popular architectures of phase- and phase-frequency detectors (PDs and PFDs) that are used in integrated PLLs. First, feedback-less phase detectors, for example the Hogge and Alexander phase detectors [18][19], have a pipelined structure and do not suffer from reset periods. They can operate at high frequencies, but do not inherently resolve frequency differences between input signals. They do, however, allow for good integration of data sampling into the PLL loop which allows for low-offset clock and data alignment [20]. Second, D-flip-flop feedback-based phase-frequency detectors are constructed of basic logic blocks and are designed to inherently resolve frequency differences [21] [22]. Finally, digital implementations using tri-state buffers and pass-transistors [23] [24] have become common in modern designs requiring PFD blocks. Also, referred to as stacked-digital structures they use pre-charging to improve the maximum operation frequency. Furthermore, these phase detectors have a shorter, but non-negligible, reset time compared with the D-flip-flop PFDs.

The D-flip-flop feedback-based phase-frequency detectors can require large delays between clock edges limiting the maximum frequency of operation. The most straightforward application requires 11 FO4[1] inverter delays [22] for a signal to propagate around the feedback loop. Furthermore, all of the D-flip-flop-based structures exhibit significant dead-zones in their transfer curves around the phase offset of $0^{\circ}$ due to this same loop delay. Research has

[1] FO4 denotes “fan-out of four” or a circuit block that has a capacitive loading four times the size of the input capacitance and is a common benchmarking strategy.

successfully and substantially reduced this dead-zone, however, only at the expense of reduced maximum clock frequency [21].

The stacked-digital PFD structures attempt to improve on the D-flip-flop reset loop delay using pre-charging schemes, but still require at least 5.5 FO4 inverter delays between incoming edges before catastrophically failing [25]. Also, as the clock frequency approaches this maximum frequency there are problems with the monotonicity of the phase detector [25]. Combinations of D-flip-flop and pre-charged structures have also been designed in an attempt to eliminate missed edges due to flip-flop resetting and device pre-charging [26].

Unfortunately, since the simulated FO4 inverter delay in 0.13 µm CMOS technology, which is used for the implementation of the prototype design in this work, is approximately 250 ps (Figure 2.1), the design would be on the border of the theoretical limit for the stacked-digital PFD and is not practical for a gigabit PLL. This FO4 delay eliminates the possibility of using a CMOS logic-based D-flip-flop structure.

Furthermore, the fully digital D-flip-flop and pre-charged structures have difficulty operating in low-swing modes, while the pipelined flip-flops can easily be implemented with current-mode logic (CML) and use a differential structure to improve noise immunity and noise injection [27].

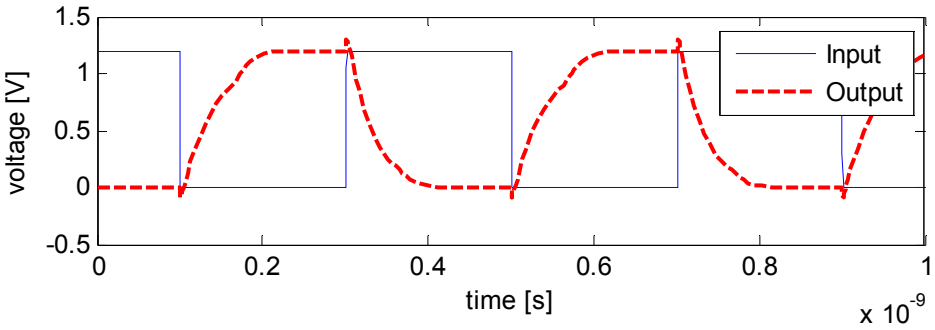



Figure 2.1: FO4 inverter delay

The PLL structure requires high-frequency design techniques for the phase detector and thus the combinatorial-style feedback-less phase detectors are a suitable choice. Half-rate and higher-division-ratio phase detectors, e.g., [20], are not required for 0.13 µm circuits since circuits in this technology can operate at 5 GHz.

The loop-filter implemented in frequency synthesizers, multi-band, and gigabit PLLs, is the same and implemented in this work (Section 4.4.3). It is also suggested in [27] and [22] that this loop fliter provides a theoretically infinite frequency lock range in charge-pump-based PLLs using PFD. This infinite frequency lock range also holds for some PD-based PLL loops despite not inherently accounting for frequency differences [28]. The loop filter also provides designs with decoupled jitter generation and stability. The charge pump proposed in [29] provides a fast response, wide swing, and limited output charge sharing. For these reasons it is used extensively in literature and this design.

## 2.2. Wideband and Active-Inductor LC-VCOs

The final block required for the PLL is an oscillator with a control mechanism compatible with the loop filter output. For a voltage-output loop filter that is an oscillator whose frequency is controllable with an input voltage. Voltage-controlled oscillators (VCOs) that are typically implemented in modern ICs are either ring oscillators or LC-tank-based oscillators.

LC-VCOs are chosen for our application primarily because they exhibit a better phase noise as compared to ring oscillators despite the fact that ring oscillators provide wider tuning ranges and a larger linear control range than a monolithic implementation of an LC-VCO [30]. Also, an LC oscillator only needs two inductors, while a differential ring oscillator that uses inductors will require two inductors per stage. When implemented with active inductors, the active-inductor contributes more noise (as compared to a passive inductor) thus further degrading the ring

oscillator, and without the monolithic inductor the LC-based structure will consume less area using fewer active components.

The oscillation frequency of an LC-VCO is given, approximately, by $f = 1/2\pi\sqrt{LC}$ (see Section 3.2). In order to obtain a large range of oscillation frequencies, either the inductance, L, or the capacitance, C, must vary by a substantial amount. When implementing the oscillation tank using monolithic inductors the bulk of the literature, for example [31], uses one or two monolithic inductors and accomplishes the frequency tuning with the use of varactors[2]. Using long transistors to realize varactors gives a large minimum to maximum capacitance ratio. By connecting and disconnecting banks of varactors large oscillation ranges can be achieved [32].

An alternative technique is to use inductance to change the oscillation frequency. In a monolithic design this can be done by shorting parts of the inductor to provide multiple effective inductances [33] and can be combined with the varactor tuning and capacitive banks for a piece-wise continuous tuning mechanism. Furthermore, it is shown in [33] that using only inductive tuning provides a much better phase noise response. Since phase noise is proportional to $f^2 \cdot L$ [34] but has no relationship with tank capacitance, by tuning the capacitance phase noise drops with increased frequency. However, by tuning frequency using a variable inductance the phase noise will remain constant (to the first order) since oscillation frequency is inversely proportional to $L^{1/2}$. In [35] a switched inductor is used to provide most of the frequency tuning and a capacitance is used for fine tuning to realize a large tuning range and maintaining a fairly constant oscillator phase noise.

[2] A varactor is a variable capacitor whose layout is similar to that of a transistor with its source and drain shorted together. By applying a variable voltage between the gate and drain of this structure a variable capacitance is realized. See [31]

It is also important to note that the size of a monolithic inductor is inversely proportional to frequency, making them unsuitable for low-frequency applications, as the increased size not only consumes extra area but increases resistive losses and parasitic capacitances. Typical sizes for inductors at 5 GHz can easily surpass $100 \times 100\ \mu m^2$, and $150 \times 150\ \mu m^2$ including element spacing to ensure accurate modeling [36]. Also, quality factors over 10 are extremely difficult to realize for optimized geometries at frequencies of 5 GHz and under which will negatively impact phase noise [37].

Active inductors provide a mechanism for tuning the oscillator using the tank inductance. They typically follow the gyrator-C methodology, using single stages for each of the two transconductance stages. A good analysis and derivation of expressions for this active inductor topology can be found in [38]. This paper also lists the two-element single-ended topologies using single transistors for the active stages. Many of the modern active-inductor-based LC-VCOs take their structure from [39], which provides a simple biasing structure. Another common design technique to bias the active inductor is applying a stacked structure, reusing current from the cross-coupled transistors that are offsetting oscillation tank losses in order to save power. [14] follows this progression implementing the active inductors and cross-coupling the outputs to continue to lower the achievable phase noise of the oscillator towards that of monolithic LC VCOs. More recently, the same structure has been coupled with a monolithic transformer in an attempt to isolate some of the active inductor noise from the VCO output [40]. This structure achieves less than –100 dBc/Hz phase noise at 7.9 GHz and exhibits a wide tuning range thanks to the active inductor, but sacrifices area in order to include the transformer. Work has been done in order to maintain constant quality factor with reasonable success [13]. This helps to maintain good phase noise but fixes the active inductor parameters and eliminates the possibility of inductive tuning. Two solutions have been proposed to improve quality factors.

First is adding resistors in the topology to increase the effective inductance [41], and the second is to use current feedback loops to fix the transconductances [13]. Both of these approaches can achieve inductor quality factors above 10 in the low GHz operating range.

# 3. Circuit Theory

This chapter covers the circuit theory required for the analysis of active inductors and presents a new theoretical derivation necessary to design and characterize the proposed PLL and active-inductor-based VCO. The main focus is on the active-inductor theory and architecture. The lumped-element mode and noise contributions of the implemented active inductor are derived. LC-tank VCO theory is presented, including a discussion of the phase noise. The noise characteristic of the VCO including the active inductor is discussed, and its impact on the VCO noise is examined. The PLL circuit blocks described in Chapter 2 that are used to realize the proposed PLL are discussed. Schematics and the design theory are presented for the PFD and charge pump. The steady-state loop operation of a charge-pump PLL is presented, highlighting the important design parameters and concepts. Finally, a design strategy for CML circuits, which are used extensively throughout the design, is developed.

## 3.1. Active-Inductor Theory

The active inductor used in a oscillator structure should have the following properties: limited current draw and current branches to keep the oscillator as low power as possible; low-voltage headroom to simplify integration and allow for large overdrive voltages to minimize power and area of the oscillator's transistors; a wide range of inductances realizable through simple tuning mechanisms; and low parallel loss resistance.

A simple grounded active inductor that incurs no added power by stacking the active inductor on top of the parallel circuitry is shown in Figure 3.1. The derivation of the small-signal impedance of this structure is found in [42]. It can be modeled by the RLC circuit shown in Figure 3.2 and with elements given by (3.2), (3.3), and (3.4) well below its resonance frequency. It

provides a tuning mechanism using the series gate resistance which can be implemented as a triode transistor and a variable gate voltage. A triode transistor has an effective resistance given in (3.6). A second tuning mechanism is the biasing current through the NMOS transistor, which will adjust the small-signal transconductance ($g_m$) of the transistor M.

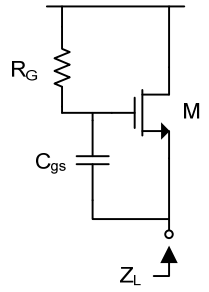



Figure 3.1: Single-NMOS and resistor active inductor

$$Z_L = \frac{V_x}{I_d} = \frac{sR_GC_{gs} + 1}{s^2R_GC_{ds}C_{gs} + s\left(C_{gs} + C_{ds} + R_GC_{gs}g_{ds}\right) + g_{ds} + g_m} \tag{3.1}$$

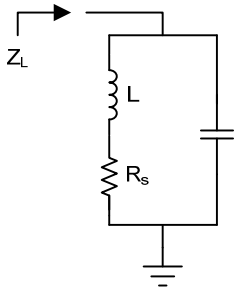



Figure 3.2: RLC lumped element model for the NMOS active inductor

$$L = \frac{R_GC_{gs}}{g_{ds} + g_m} \tag{3.2}$$

$$R_s = \frac{1}{g_{ds} + g_m} \tag{3.3}$$

$$C_p = C_{ds} \tag{3.4}$$

$$g_{ds} = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{gs} - V_{TH}) \tag{3.5}$$

The NMOS device of the active inductor must remain in saturation ($V_{DS} > V_{GS} - V_{TH}$) for the derived impedance equation to remain valid. This means a significant portion of the power supply voltage range is required to ensure proper transistor biasing. The problem becomes worse when the body effect of the NMOS device is taken into account. The required $V_{DS}$ of the cross-coupled transistors and current source in the oscillator structure (e.g., Figure 3.6) added to the minimum headroom requirement of the active inductor makes it difficult to maintain a large $V_{GS}$ across the active-inductor NMOS transistor and provide sufficient voltage at the output to drive subsequent stages. This restricts the AI NMOS transconductance ($g_m$), resonant frequency of the active inductor, and therefore the oscillator's maximum frequency.

An equivalent PMOS-based active inductor is provided in Figure 3.3 as a bridge between the NMOS active inductor and the final design. The input impedance of the NMOS active inductor in Figure 3.1 and the PMOS-based block in Figure 3.3 are the same [42]. Both AI structures convert the voltage across the gate-source capacitance to a current at to the input. The change in polarity of $V_{GS}$ between the NMOS and PMOS structures is negated by the opposite polarity of the current feedback.

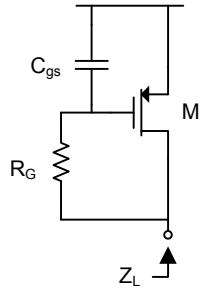



Figure 3.3: Single-PMOS and resistor active inductor

In order to reduce the voltage headroom requirement, a level shifter is added between the series resistor and the gate of the active device, Figure 3.4. A source-follower stage is used to implement the level shifter and adds a single current branch which will increase the overall power consumption. The derivation of the impedance of this topology is given below, with the result provided in (3.9), and the equivalent lumped element model and related equations in Figure 3.5 and equations (3.10)**,** (3.11)**,** and (3.12), respectively, when the frequency of interest is well below the resonance frequency, given in (3.13).

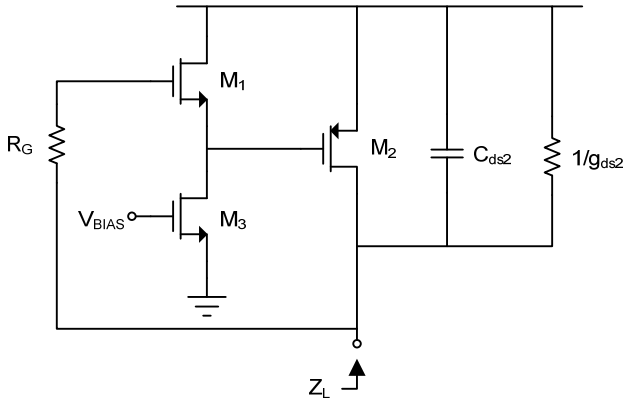



Figure 3.4: Two-stage resistor-based AI with parallel loss and capacitive elements

The derivation is initially performed excluding $g_{ds2}$ and $C_{ds2}$ which are in parallel with the main active-inductor structure.

$$V_{g1} = \frac{V_x}{sC_{gd1}R_G + 1} \tag{3.6}$$

$$V_{g2} = A_1 \cdot \frac{V_x}{sC_{gd1}R_G + 1} = \frac{g_{m1}}{g_{m1} + g_{m3}} \cdot \frac{V_x}{sC_{gd1}R_G + 1} \tag{3.7}$$

$A_1$ is the voltage gain of the source-follower stage.

$$I_x = \frac{g_{m1}g_{m2}}{g_{m1} + g_{m3}} \cdot \frac{V_x}{sC_{gd1}R_G + 1} \tag{3.8}$$

It is also interesting to note that if $g_{m1} >> g_{m3}$, then (3.8) reduces to give the same lumped model in [42]. However, this simplification assumes the source follower gain is identical to one – which rarely occurs, even if it is the ideal outcome. The simplification also eliminates $g_{m1}$ as a tuning mechanism. Therefore, the equation is left in the unsimplified form. Now $Z_L$' can be found by rearranging (3.8). Including the parallel conductance and capacitance of transistor $M_2$ the effective input impedance is:

$$Z_L = \frac{sC_{gd1}R_G + 1}{s^2C_{ds1}C_{ds2}R_G + s(C_{ds2} + C_{ds1}R_G g_{ds2}) + \frac{g_{m1}g_{m2}}{g_{m1} + g_{m3}} + g_{ds2}} \tag{3.9}$$

This impedance can be approximated by the three-element lumped model from Figure 3.5 when the frequencies of interest are well below the resonance of the oscillator. The resonance frequency, $\omega_r$, is given in (3.13) and the lumped element components are now defined by (3.10), (3.11), and (3.12).

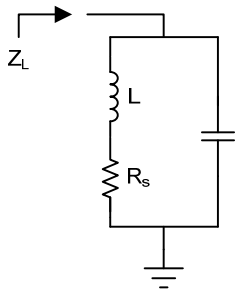



Figure 3.5: Lumped element model for 2-stage active inductor

$$L = \frac{C_{gd1}R_G}{\frac{g_{m1}g_{m2}}{g_{m1}+g_{m3}} + g_{ds2}} \tag{3.10}$$

$$R_s = \frac{1}{\frac{g_{m1}g_{m2}}{g_{m1}+g_{m3}} + g_{ds2}} \tag{3.11}$$

$$C_p = C_{ds2} \tag{3.12}$$

$$\omega_r = \sqrt{\frac{\frac{g_{m1}g_{m2}}{g_{m1}+g_{m3}} + g_{ds2}}{(C_{ds1}C_{ds2}R_G)}} \tag{3.13}$$

The noise analysis will be presented in Section 3.3, combined with the analysis of the LC VCO in order to provide a single framework relating to oscillator phase noise.

## 3.2. LC-VCO Theory

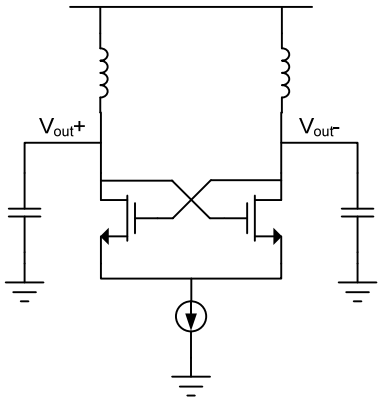



Figure 3.6: Typical LC oscillator structure

A generic structure of an LC-tank VCO is shown Figure 3.6 and has been applied to a wide-frequency range, from kHz to multi-GHz signals [43], [31]. The RLC structure forms the oscillation tank, and defines the frequency at which the circuit will oscillate. The cross-coupled transistors provide power and compensate for losses. In order to study the loop it is convenient to represent it as the passive tank and an active transconductance, as done in Figure 3.7. This circuit has a transfer function given in (3.14) [44].

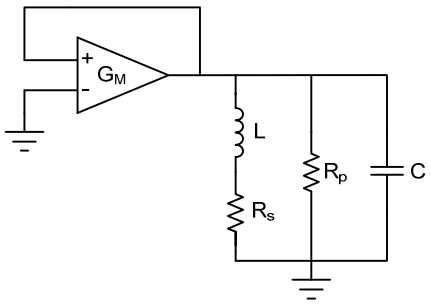



Figure 3.7: RLC tank with $G_M$ feedback loop

$$H_{loop}(s) = G_M * \frac{sL}{1 + \frac{sL}{R_{eq}} + s^2LC} \tag{3.14}$$

$R_{eq}$ is the combined parallel resistance and converted-to-parallel series resistance. This circuit will only oscillate at the frequency where the imaginary part of the transfer function is equal to zero. At this frequency, energy is transferred back and forth from the inductor to the capacitor. This is approximately:

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{3.15}$$

The non-zero real part of the transfer function at this frequency will consume power, due to resistance $R_{eq}$, even when ignoring $G_M$. In order to induce a steady-state oscillation the magnitude of the loop gain must be equal to one and the active transconductance must compensate for the resistive loss. This requirement is also known as the Barkhausen criterion [45]. If this criteria is not met the circuit will settle to a DC common-mode output voltage. Solving (3.15), it is found that $G_M = 1/R_{eq}$ satisfies this condition.

To calculate $R_{eq}$, $R_s$, which is the inductor series loss, must be combined with $R_p$, any parallel losses as seen by the LC tank. These also include the output impedance due to the $G_M$ stage, or other non-idealities.

Near the oscillation frequency the series resistance ($R_s$) can be converted into a parallel resistance by (3.16) [22]. $R_{eq}$ then is equal to the parallel combination of the two resistances: $R_p$ and $R_p$'.

$$R_p^{'} = Q^2 R_s = \frac{L^2 \omega^2}{R_s} \tag{3.16}$$

Another important quantity is Q, the quality factor of the inductor. The larger the quality factor the closer the designed inductor is to an ideal inductor and the lower the effective loss of the passive oscillation tank. The total oscillator quality factor, $Q_{total}$, for a parallel network is the parallel combination of the individual quality factors, (3.18). This is typically dominated by the quality factor of the inductor [44].

$$Q = 2\pi \frac{Peak\ energy\ stored}{Energy\ loss\ per\ cycle} = \frac{L \cdot \omega}{R_s} \tag{3.17}$$

$$Q_{total} = \left(\frac{1}{Q_L} + \frac{1}{Q_C}\right)^{-1} \tag{3.18}$$

In order to combine the above VCO analysis with the active-inductor structure discussed in Section 3.1 the monolithic inductor and its losses found in Figure 3.7 are simply replaced with the active-inductor model derived and provided in Figure 3.5. Analysis of the oscillation frequency and quality factor can then proceed as above.

## 3.3. Noise Analysis of the Active-Inductor LC-VCO

The impact of accumulated noise in an oscillator affects the effective phase of the oscillator, disturbing, for example, the zero crossing of the output sinusoid. This oscillator noise is termed 'phase noise,' and defined in (3.19). This section begins by examining the phase noise of a monolithic LC oscillator. Then the noise contributions of the implemented active inductor are

derived and then applied to the LC oscillator formula to derive a complete equation for phase noise of the active inductor LC-VCO.

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log\left(\frac{power\ in\ 1Hz\ bandwidth\ at\ \omega_0 + d\omega}{carrier\ power}\right)\ \left[\frac{dBc}{Hz}\right] \tag{3.19}$$

Phase noise can be taken as the overall contribution of all of the noise sources: thermal, flicker, and shot noise that are subsequently filtered by the LC-tank and applied to the output sinusoid. Since the circuit operates at a reasonably high frequency only the effect of thermal noise is considered. Flicker noise, or 1/f noise, is assumed to be small in the frequency band of interest, and shot noise is assumed to be more than an order of magnitude smaller than the contributed thermal noise [5].

### 3.3.1. Noise in an LC-VCO

The noise voltage spectral density induced by the tank's equivalent resisitive loss, $R_{eq} = \mathrm{Rp}||\mathrm{R}'_p$ of Figure 3.7 and (3.16), can be written as [44]:

$$dV^2_{out,G_M}\{\Delta\omega\} = kT * R_{eq} * A * F_{G_M} * \left(\frac{\omega_0}{\Delta\omega}\right)^2 * df \tag{3.20}$$

K is the Boltzmann constant, T is the absolute temperature in Kelvin, A is the safety margin over the minimum required startup transconductance and F is the stage noise factor, and the notation $\{\Delta\omega\}$ indicates a frequency offset from the carrier.

When taken as a ratio with the output voltage the expression leads to a single-sided output phase noise given in (3.21).

$$L\{\Delta f\} = \frac{1}{2} * \frac{kT * R_{eq} * \left(1 + A * F_{G_M}\right)\left(\frac{\omega_0}{\Delta\omega}\right)^2}{V_{out,pp}^2} \tag{3.21}$$

### 3.3.2. Noise in an AI-LC-VCO

The noise produced by the oscillator's cross-coupled pair is the same for the active-inductor VCO except $R_{eq}$ is now the equivalent parallel resistance of the active inductor discussed in section 3.1. The total noise, however, now includes the added noise from the active elements within the active inductor. In order to derive the noise in the AI the gyrator model of the active inductor is used. The gyrator model and its noise sources are illustrated in Figure 3.8. In this figure, $g_{mv}$ represents the transconductance of the source-follower stage and $g_{mi}$ represents the transconductance of the PMOS transistor.

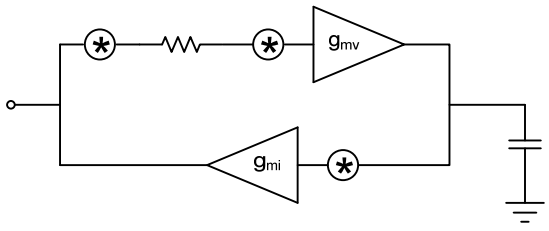



Figure 3.8: Gyrator model of the active inductor with noise sources

Expanding from [46] and [44] to include the input resistor:

$$di_L^2 = g_{mi}^2 * dv_{gmi}^2 \tag{3.22}$$

$$dv_L^2 = dv_{gmv}^2 \tag{3.23}$$

$$dv_R^2 = 4kT * R_{L,G} * df \tag{3.24}$$

*di* is used to characterize the input noise voltage of $g_{m2}$ referred to the output of the transconductance stage, and $di_R$ is the thermal noise due to the gate resistor. $R_{L,G}$ denotes the resistance attached to the gate of the source-follower stage within the active inductor.

$dv_{gmi}^2$ is the input-referred thermal noise of a transconductance stage [27] and is equal to:

$$dv_{gmi}^2 = 4kT * \frac{F_i}{g_{mi}} * df \tag{3.25}$$

Using this equation and after combining the two noise current sources, the noise components from equations (3.22), (3.23), and (3.24) can be re-written into equations (3.26) and (3.27).

$$dv_L^2 = 4kT * \left(\frac{F_v}{g_{mv}} + R_{L,G}\right) * df \tag{3.26}$$

$$di_L^2 = 4kT * (F_i * g_{mi}) * df \tag{3.27}$$

The active inductor noise contribution to the VCO is now modeled using Figure 3.9 where the noise sources represent equations (3.26) and (3.27).

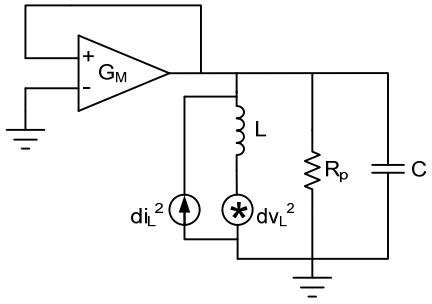



Figure 3.9: Oscillator model with inductor noise sources

This leads to output voltage noise contributions of:

$$dV_{out,Li}^2\{\Delta\omega\} = kT * \frac{1}{(\omega_0 C)^2} * (F_i * g_{mi}) * \left(\frac{\omega_0}{\Delta\omega}\right)^2 * df \tag{3.28}$$

$$dV_{out,Lv}^2\{\Delta\omega\} = kT * \left(\frac{F_v}{g_{mv}} + R_{L,G}\right) * \left(\frac{\omega_0}{\Delta\omega}\right)^2 * df \tag{3.29}$$

Reorganizing and including the $G_M$ noise term gives a total active inductor output noise voltage given in (3.30). The three components of the total VCO noise voltage are due to the losses in the active inductor and the cascaded active stage for compensation, the active-inductor resistor, and the active stages in the inductor.

$$dV_{out}^2\{\Delta\omega\} = kT\left[R_p\left(1 + A * F_{G_M}\right) + R_{L,G} + \frac{1}{\omega_0 C}\left(\frac{F_i * g_{mi}}{\omega_0 C} + \frac{F_v}{g_{mv}}(\omega_0 C)\right)\right] * \left(\frac{\omega_0}{\Delta\omega}\right)^2 * df \tag{3.30}$$

In order to minimize the noise due to the active-inductor resistor its value should be minimized and the capacitance of the LC-tank should be maximized. To minimize the noise contribution of the active stages it is desirable to maximize the value of $g_{m1}$ at the expense of $g_{m2}$. Doing so would increase the swing across the internal active inductor capacitance, $C_i$ in Figure 3.8, generating the effective inductance and this swing would be larger than the swing across the tank capacitance. This goes against the design goal to keep the output swing as large as possible to minimize phase noise from (3.30). To meet these two conflicting goals choosing $F_1=F_2=1$ generates a reasonable low phase noise and maintains the output signal swing.

## 3.4. PLL Design Theory

This section provides a brief overview to PLL design theory, focusing on charge-pump PLLs. These charge-pump PLLs theoretically give $0^o$ phase offset for frequency locking [5] due to the infinite gain around the $0^o$ phase offset. A generic block diagram of a charge-pump PLL is provided in Figure 3.10. Its circuit blocks, discussed in this section, are the phase or phase-frequency detector, charge pump, and loop filter. The VCO is covered separately in Section 3.2.

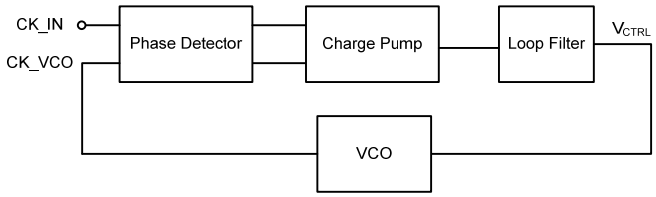



Figure 3.10: Typical charge-pump PLL block diagram

### 3.4.1. Phase and Phase-Frequency Detectors

The purpose of a phase detector (PD) is to determine if the transitions of the incoming clock or data signal are early (before) or late (after) with respect to the edges of a reference signal (the VCO output). Two popular topologies for PDs are linear and bang-bang phase detectors. A linear

PD encodes the relative time difference between the incoming clock and VCO output edges. A bang-bang phase detector, conversely, only provides early or late information and does not include any information on the difference. This section limits the discussion to flip-flop-based implementations, which are amenable to high-frequency applications (see Section 2.1). A commonly used linear phase detector is the "Hogge PD" [18] (Figure 3.11.A), and a popular bang-bang PD is the "Alexander phase detector" [19] (Figure 3.11.B). Typical waveforms for linear and bang-bang phase detectors are given in Figure 3.12.

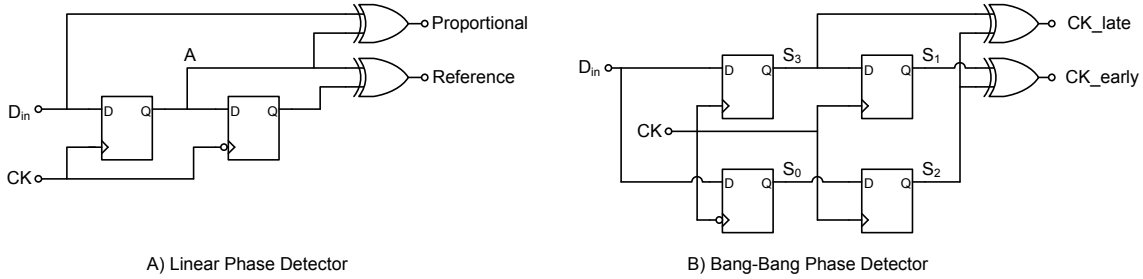



Figure 3.11 Linear and bang-bang phase detectors

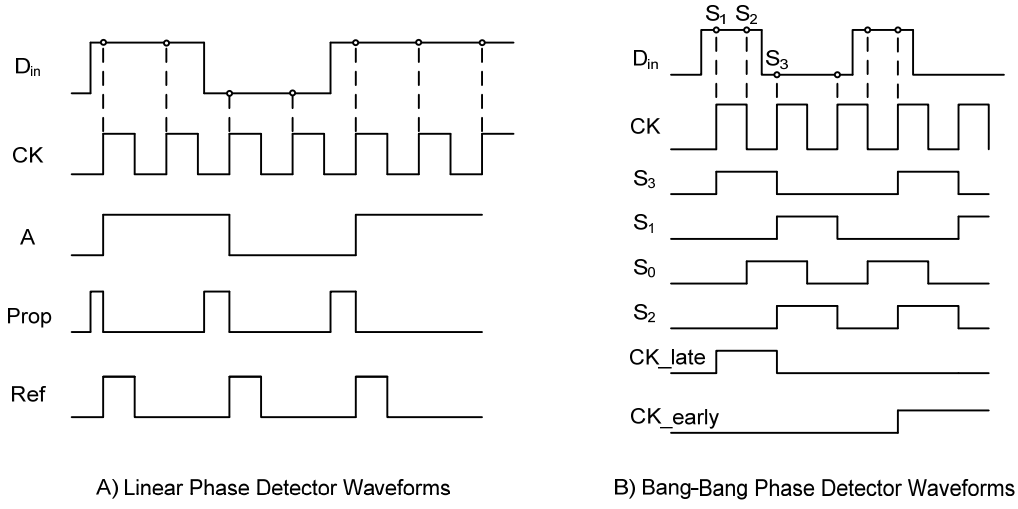



Figure 3.12: Phase detector waveforms

The Hogge phase detector generates a constant width reference signal and a second output proportional to the phase difference fro charge pump control. If a linear phase detector output becomes DC (or zero) when the signals are aligned, the drift of the VCO control voltage, due to leakage through the charge pump or across the loop filter, is likely. This creates low-frequency jitter on the control voltage as the PLL corrects, as well as an average phase offset of the output clock signal. A second downside of the linear phase detector is that as the input phase difference approaches zero, and the difference between reference and proportional signals disappears the loop requires more time to match the input signal phases.

To increase the lock speed, bang-bang phase detectors provide high gain in the vicinity of $\Delta\theta = 0$ at the cost of increased high-frequency jitter. Since the circuit will resolve either early or late – there is no "locked" output signal – even if the phase difference is identically zero there is a minimum noise on the VCO control line equal to (3.31), where $\tau_{pulse}$ is the width of an early/late pulse. This noise caused solely by phase detectors oscillating around the desired solution is called "hunting noise" [28].

$$\Delta V_{\min} = H_{LF}(s) I_{CP} \tau_{pulse} \tag{3.31}$$

Figure 3.13 shows the transfer curve of the input phase difference to output for a generic linear and bang-bang type phase detector.

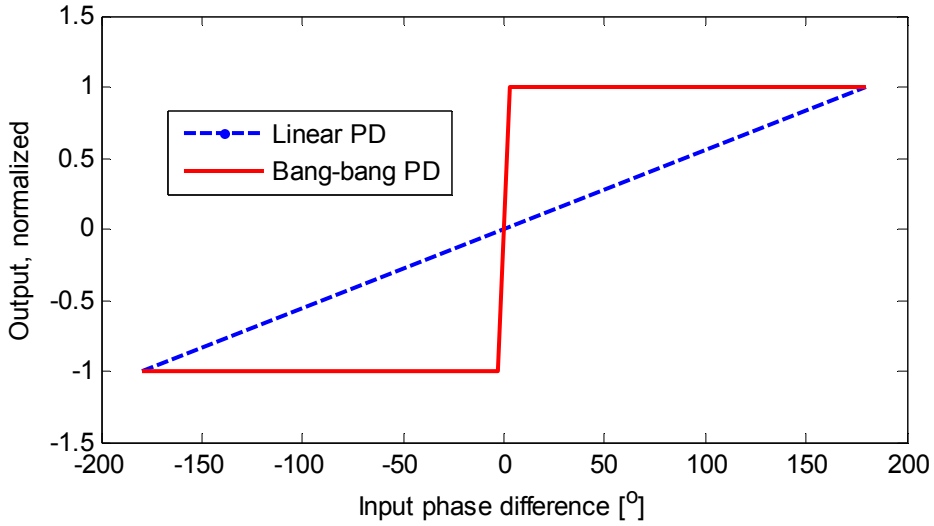



Figure 3.13: Idealized phase detector transfer curves

The similar structures of the Hogge and Alexander phase detectors makes it possible to combine the two into a single topology with three outputs [47]. A multiplexer can then be used to switch between the two phase detectors and use the higher-gain bang-bang PD to approach the target frequency, and then switch to the linear detector to phase lock and improve locked VCO control jitter by eliminating the bang-bang detector hunting jitter. Furthermore, by re-arranging the clock connections and taking advantage of the PLL application where the *CK_in* signal has a 100% transition density the bang-bang PD can be shown to operate as a PFD [47].

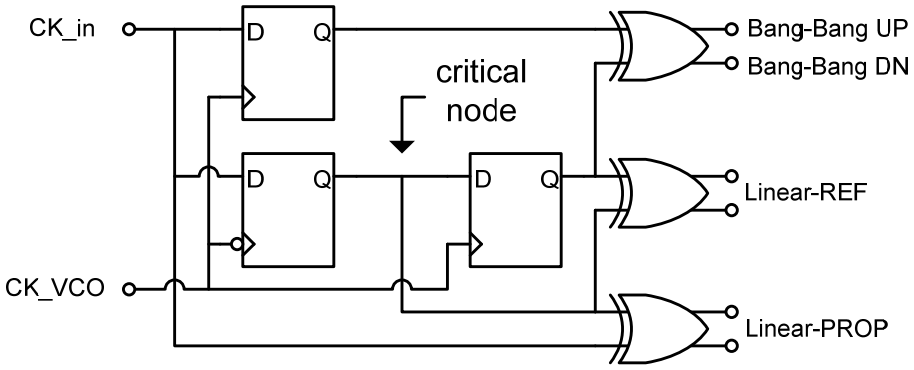



Figure 3.14: Combined linear and bang-bang phase detector

The combined schematic is given in Figure 3.14. This phase detector structure produces both bang-bang and linear outputs adding only a single flip-flop on top of the linear phase detector. It uses one less flip-flop than the Alexander PD by taking advantage of the binary nature of bang-bang early/late pulses – if the clock is not early then the inverse must be true, or, the clock is late.

### 3.4.2. Charge Pump

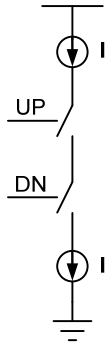



Figure 3.15: Simple charge pump

A simple charge pump is shown in Figure 3.15. It converts up and down signals into charge delivered to the output. The charge is delivered the form of $current \cdot time$ to the output. Ideally the current delivered to the output should remain fixed regardless of the output voltage level and should be zero when both switches are open or closed.

The circuit design concerns include: charge sharing between the output and internal nodes [29], charge injection to the output, limited output swing due to the non-infinite output impedance of the current sources, and changing biasing conditions [48].

Figure 3.16 is the charge pump implemented in the PLL, proposed by [29]. A unity-gain amplifier charges floating nodes to the output voltage to eliminate charge sharing when the charge pump

switches are closed. This also lowers the minimum time required for an up or down pulse width, since there is no charging or discharging internal nodes when inputs are switched. The switches are implemented as pass transistors to reduce charge injection and pass both high and low voltages.

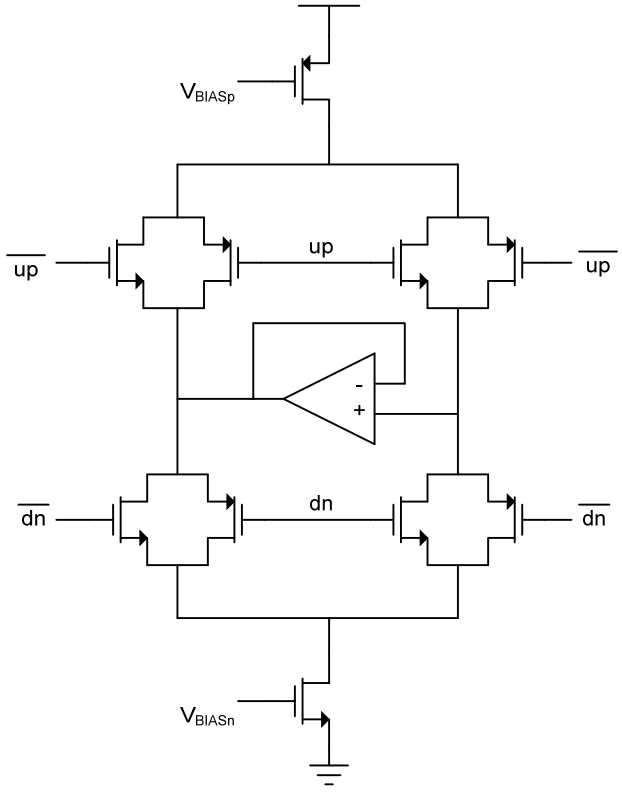



Figure 3.16: Charge pump proposed by [29]

### 3.4.3. Loop Filter

The PLL loop filter is present to smooth the output of the charge pump before applying it to the VCO control. It has a strong impact on loop characteristics including PLL bandwidth, loop damping factor, and phase margin [27]. The loop filter will also determine whether there is a DC error in phase or frequency during locking [28] due to the nature of the PLL feedback loop.

The PLL loop equation will be one order higher than the order of the loop filter equation (see (3.34)). While higher orders give the designer more freedom to design the loop transfer function, this flexibility comes at the expense of design complexity and often stability. It is therefore desirable to have the simplest loop filter that provides for decoupled loop parameter design. This can be accomplished using a series RC filter for both bang-bang phase detectors [5] and linear phase detectors [22].

The transfer function for the loop filter of Figure 3.17 is given in (3.32). Capacitor $C_2$ is to eliminate glitches due to the discontinuous voltage drops across resistor $R_1$ as the charge pump turns on and off. It is set at most $1/10^{th}$ of the size of $C_1$ such that the pole introduced by it is at a very high frequency and has negligible impact on the loop characteristics. For the initial design, with $C_2$ taken much smaller than $C_1$, the loop transfer function used for design is given in (3.33). The RC series creates a zero and a pole allowing for decoupled design of the PLL resonant frequency, $\omega_0$, and damping factor, $\xi$.

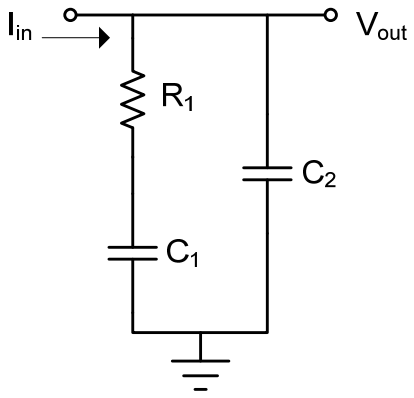



Figure 3.17: Loop filter schematic

$$H_{LF}(s) = \frac{sC_1R_1 + 1}{s^2C_1C_2R_1 + s(C_1 + C_2)} \tag{3.32}$$

$$H_{LF}^{'}(s) = R_1 + \frac{1}{sC_1} = \frac{sC_1R_1 + 1}{sC_1} \tag{3.33}$$

### 3.4.4. Loop Dynamics

The PLL is a highly non-linear system, especially when out of lock. To gain more insight into the PLL dynamics, it is often linearized around the locked state. This way the response of the PLL to phase deviations and small frequency changes can be examined [27], [28], [5]. This small-frequency change approximation allows us to examine the linear and bang-bang PLL in the same framework. The linearized model used to analyze the behavior of the PLL is presented in Figure 3.18. The multiplexer and charge-pump blocks are rolled into the phase-detector gain throughout the remainder of this section for simplicity.

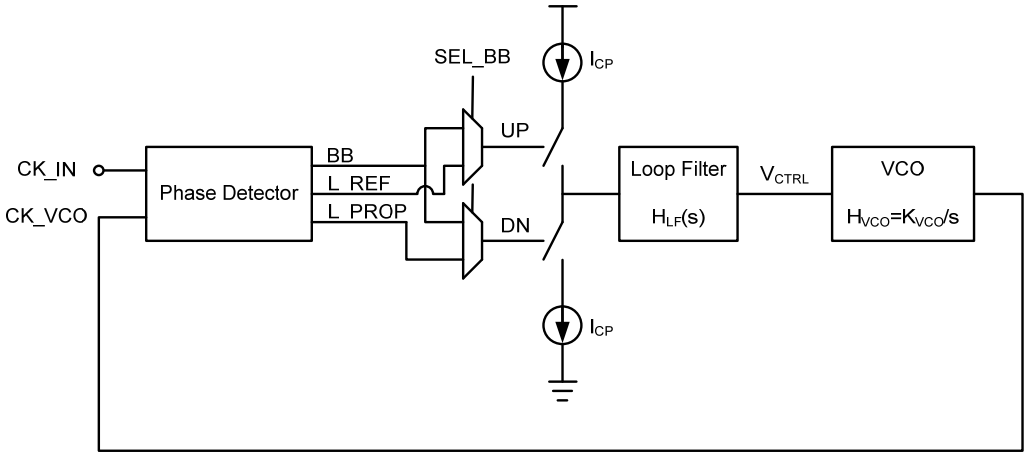



Figure 3.18: s-domain model of a PLL

The generic loop transfer function is given in (3.34). Substituting specific results for the low-pass filter, phase detector, and oscillator gain will determine the response of the system to phase perturbations. $K_{PD}$ represents the combined linearized gain of the phase detector, MUX, and charge pump, with units [C/$^{o}$] (Coulombs per degree).

$$\frac{V_{CTRL}}{\theta_{in}}(s) = \frac{sK_{PD}H_{LP}(s)}{s + K_{PD}K_{VCO}H_{LP}(s)} \tag{3.34}$$

Substituting (3.33) into (3.34) results in (3.35) that is specific to this implementation of a second order PLL.

$$H(s) = \frac{V_{CTRL}}{\theta_{in}} = \frac{\frac{1}{K_{VCO}}s(1 + sR_1C_1)}{1 + sR_1C_1 + s^2\frac{C_1}{K_{PD}K_{VCO}}} \tag{3.35}$$

To find the relationship between the VCO control voltage and input frequency (3.36), which states that phase is the integral of frequency, is substituted into (3.35)**.**

$$\theta(s) = \frac{\omega(s)}{s} \tag{3.36}$$

$$\frac{V_{CTRL}}{\omega_{in}}(s) = \frac{\frac{1}{K_{VCO}}(1 + sR_1C_1)}{1 + sR_1C_1 + s^2\frac{C_1}{K_{PD}K_{VCO}}} \tag{3.37}$$

Comparing the DC (s = jω = 0) values of the transfer functions in (3.35) and (3.37) we see that phase jumps do not cause steady-state changes to the control voltage while a frequency change causes a linear control adjustment proportional to $K_{VCO}$, as is intuitively expected.

The error transfer function is useful for examining the locked response of the PLL, and is denoted as $H_e(s)$.

$$H_e(s) = \frac{\theta_e}{\theta_{in}}(s) = \frac{\theta_{in} - \theta_{VCO}}{\theta_{in}}(s) = \frac{s}{s + K_{PD}K_{VCO}H_{LF}(s)} \tag{3.38}$$

$$H_e(s) = \frac{s^2 C_1}{s^2 C_1 + K_{PD}K_{VCO}(sC_1R_1 + 1)} \tag{3.39}$$

Using the final value theorem the phase error of this PLL goes to zero as $t \to \infty$ when an input phase step is applied.

$$H_{e-STEP}(s) = H_e(s)H_{STEP}(s) = H_e(s) \cdot \frac{\Delta\theta}{s} \tag{3.40}$$

$$\mathcal{h}_{e-STEP}(t \to \infty) = \lim_{s \to 0} s \cdot H_{e-STEP}(s) = 0 \tag{3.41}$$

$\Delta\theta$ is the magnitude of the applied phase step.

It is also helpful to note that the PLL transfer function equations can be re-written in a normalized form where the denominator is expressed as (3.42), where $\omega_o$ is the natural frequency and ξ is the damping factor. In this form well established control theory can be used to understand the dynamic response of the linearized PLL model.

$$Denominator = s^2 + 2\xi\omega_O + \omega_O^2 \tag{3.42}$$

For the implemented PLL:

$$\omega_O = \sqrt{\frac{K_{PD}K_{VCO}}{C_1}} \tag{3.43}$$

$$\xi = \frac{1}{2}\omega_O R_1 C_1 \tag{3.44}$$

The damping factor affects how the transients of the loop will settle. For ξ < 1 the system will exhibit overshoot, while for ξ > 1 PLL can become slow to respond. Typically a maximally flat response, ξ = 1/sqrt(2), is the design goal [28].

The natural frequency, $\omega_O$, provides an indication of the maximum rate of change with which the PLL is able to respond to input changes. It is also the frequency for which the system will no longer be able to track input phase.

From the above analysis, it may be inferred that a natural frequency as high as possible is ideal. However, a higher natural frequency reduces some of the PLL's inherent ability to filter noise. Figure 3.19 shows the PLL loop with three major sources of noise indicated: input source phase noise, noise due to the phase detector, and VCO open-loop phase noise. The open-loop VCO phase noise is the phase noise exhibited by the VCO when the control voltage is fixed at a DC level. These noise sources will be passed through the control loop to the input of the VCO and will modulate the output frequency, creating output jitter.

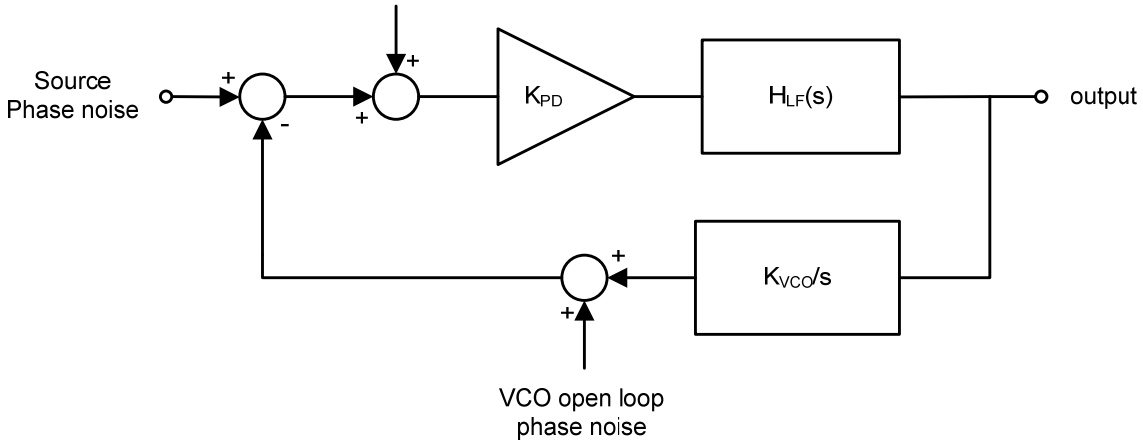



Figure 3.19: PLL with major noise contributors

The noise transfer function for the input source and phase detector is a low-pass filter, given in (3.45), while the noise transfer function for the VCO phase noise is a high-pass filter, shown in (3.54). These transfer functions have knees at $\omega_O$, and the total noise is the RMS sum of all three contributions at the output [5].

$$N_{input,TF}(s) = \frac{s^2 C_1}{s^2 C_1 + K_{PD}K_{VCO}(sC_1R_1 + 1)} \tag{3.45}$$

$$N_{VCO,TF}(s) = \frac{K_{PD}K_{VCO}(sC_1R_1 + 1)}{s^2 C_1 + K_{PD}K_{VCO}(sC_1R_1 + 1)} \tag{3.46}$$

For an optimal speed-to-noise tradeoff a good understanding of the requirements of the system, the magnitude of the noise sources in Figure 3.19**,** and a well modeled system are all required. A comprehensive study of the topic is presented in [49].

Finally, it is helpful to have analytical expressions for important PLL locking parameters. They include: hold range, pull-in range, and lock range. Generic equations are derived in [28]. Implementation specific results are provided below.

Hold range, denotes the maximum frequency range within which the PLL can statically maintain lock. This is dominated by the DC gain of the loop filter. Since the loop filter gain is theoretically infinite, the hold range for both the linear and bang-bang phase detectors is also infinite [28], [5]. In practice this will be larger than the fine-tuning range of the VCO.

Pull-in range is the span on frequencies where the PLL will lock, but may be a slow, highly nonlinear, pull-in process that takes multiple 'beats' of the PLL. An example of a PLL within its pull-in range with the lock range and a beat highlighted is given in Figure 3.20. A beat is the locking process where the phase difference between the VCO and the input signal never changes more than 360-degrees from the initial phase offset. For the linear PD the pull in range is given in (3.47) [28]. The pull-in range of any bang-bang PLL using this loop filter is theoretically infinite.

$$\omega_{PI,lin} \approx \pi\sqrt{2\xi\omega_n K_{PD} - \omega_n^2} \tag{3.47}$$

Lock range is the frequency range within which the PLL will re-lock to a signal within one 'beat'. For the linear phase detector this is given in [28]. As is discussed in Section 3.4.1 the implemented bang-bang PLL operates as a PFD, and therefore its lock range is infinite.

$$\omega_{L,lin} = 2\pi\xi\omega_n \tag{3.48}$$

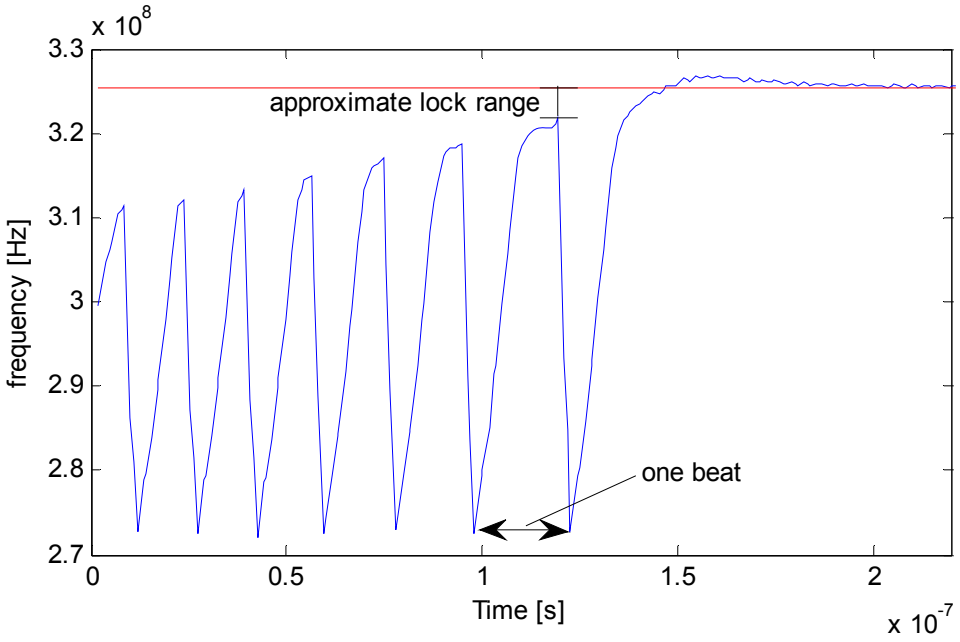



Figure 3.20: Example of a PLL within pull-in range

## 3.5. CML Buffer Circuit Theory

This section gives a recipe for designing buffer circuitry and common-source amplifiers, and covers the design constraints that define this recipe. This circuit architecture is shown in Figure 3.21. The strategy covered also provides guidelines for how to design other CML circuitry, for example the latches, MUX, and XOR used in the phase detector. The design constraints are delay/bandwidth, power, and signal swing; ideally the delay and power are minimized, while bandwidth and signal swing are maximized.

Stages are designed from the output back to the input based on the capacitive loading of the CML chain and the loading the CML circuits can present to the previous block. The extension of this design procedure to other CML blocks is discussed in their respective design sections in

Chapter 4. This tapered design approach is reorganized mostly taken from [50]. The numerical subscripts are omitted from design equations in this section when only dealing with one stage.

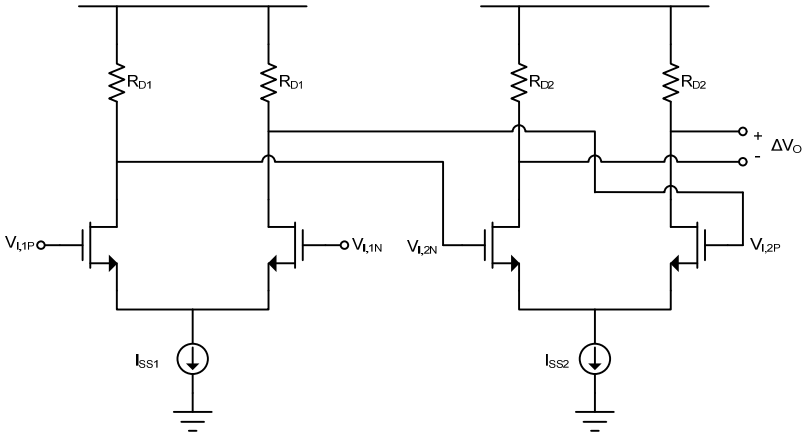



Figure 3.21: Two-stage CML buffer schematic

To avoid overdesign, and since consumed power will be inversely related to the load resistance, the bandwidth of each CML stage should be equal to the maximum signal bandwidth. This is accomplished using the relationship

$$\omega_{3db} = \frac{1}{C_L * R_D} \tag{3.49}$$

This assumes that the output pole is dominant, which is acceptable in the employed single-stage circuit. If delay becomes a significant concern even with this design, the delay of the system can be improved by increasing the bandwidth of each stage [51].

The optimal number of stages from a delay perspective is

$$N_{opt} = \ln\left(\frac{C_{out}}{C_{in}}\right) \tag{3.50}$$

where the output capacitance and input capacitance are denoted by $C_L$ and $C_{in}$ respectively. This result is the same as the optimal number of digital buffers to drive a large capacitive load and is derived under the same assumption – ignoring parasitic drain capacitances [52].

The bias current is chosen to fully switch the differential pair and requires knowledge of the input differential voltage. The input differential voltage for each stage, as well as the input and output common-mode voltages, $V_{i,cm}$ and $V_{o,cm}$, respectively, must be set so that the NMOS devices remain in saturation and approach the edge of cut-off for $V_{in,max}$ thereby completely switching the current between branches. Choosing these voltages requires satisfying the design equations given in (3.51) and (3.52) that define the valid levels for the input common-mode and maximum output voltage levels, respectively.

$$V_{gs,i} + (V_{ds3}) + I_{ss}R_D \leq V_{in,CM} \leq V_{dd} - \frac{I_{ss}}{2}R_D \tag{3.51}$$

$$V_{in,max} - V_{TH,n} \leq V_{o,max} = R_D I_{ss} \leq V_{TH,n} \tag{3.52}$$

Choosing $\Delta V_o = R_D I_{ss} = V_{TH,n}$ and $V_{i,cm} = V_{o,cm}$ gives a large voltage swing, without driving transistors out of saturation and compromising the device linearity. The acceptable range of common mode voltages is

$$V_{TH} + V_{TH}/2 < V_{cm} < V_{dd} - V_{TH}/2 \tag{3.53}$$

Solving equation (3.54) sets the minimum required bias current to generate the differential output voltage, and equation (3.55) sets the device sizes to ensure full current switching between the left and right branches.

$$I_{ss} = \frac{V_{TH}}{R_D} \tag{3.54}$$

$$R_{D1} I_{ss1} \geq \sqrt{\frac{2 I_{ss2}}{\mu_n C_{ox} \left(\frac{W}{L}\right)_2}} \tag{3.55}$$

# 4. Circuit Design and Simulation Results

This chapter covers the implemented design procedures and trade-offs made during the design process. The purpose is to provide a practical design guideline and demonstrate the implementation of circuit block theory discussed in Chapter 3. Schematics are provided for all the circuit blocks implemented.

The organization is as follows: first the design of the active inductor as a stand-alone block and then its design in parallel with the VCO is presented. Following the VCO are the CML logic gates that are used to build the phase-frequency detector including the flip-flop, XOR, and multiplexer. The PLL design is presented, covering the design of the PFD, charge-pump, and then the loop filter and loop design. Next, the design of the CML output and VCO buffers are covered. The chapter concludes with a flow chart is provided as an example implementation for the digital band selection.

## 4.1. Active-Inductor Design

The first-pass of the active-inductor design proceeded as a black-box separated from the oscillator structure. The design goals at this stage were to realize an active inductor that would allow 5 GHz or higher oscillation when added to the VCO structure. This necessitates an inductive characteristic of at least 5 GHz when tuned to the smallest inductance, while simultaneously minimizing the effective resistance to keep inductor and LC-tank losses small.

The estimated of load capacitance seen by the LC-tank was 250 fF, with contributions from the active inductor, cross-coupled transconductance pair, and load capacitance plus a margin for error. This lead to a target 5 GHz inductance value of:

$$L = \frac{1}{(2\pi f)^2 C} = \frac{1}{(2\pi \cdot 5e9)^2 \cdot 400e - 15} = 4nH \tag{4.1}$$

The lumped element model (Figure 3.5) and equations (3.10), (3.11), and (3.12) are repeated here. The derivation of the original equations can be found in Section 3.1.

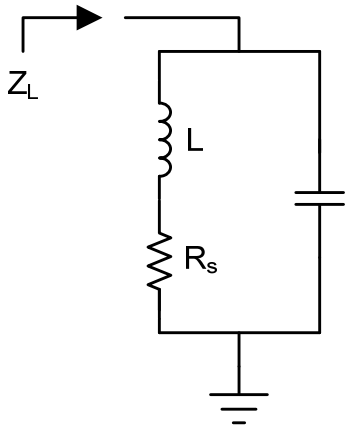



Figure 4.1: Lumped element model for 2-stage active inductor

$$L = \frac{C_{gd1} R_G}{\frac{g_{m1} g_{m2}}{g_{m1} + g_{m3}} + g_{ds2}} \tag{4.2}$$

$$R_s = \frac{1}{\frac{g_{m1} g_{m2}}{g_{m1} + g_{m3}} + g_{ds2}} \tag{4.3}$$

$$C_p = C_{ds2} \tag{4.4}$$

The design concept is to adjust the current sources in the active inductor to sweep the transconductance of transistors $M_1$ and $M_2$ in Figure 4.2. Increasing the current will increase the inductance by reducing the denominator through $g_{m1}$ and $g_{m2}$. The increase in the effective inductance will cause the oscillation frequency to drop. At this stage it is assumed that this tuning mechanism will be sufficient, as we should be able to lower both $g_{m1}$ and $g_{m2}$ arbitrarily to achieve the required inductances.

Simulation results and the annotated schematic for the active inductor used in the final design can be found in Figure 4.2 through Figure 4.4.

These simulations are useful in understanding tradeoffs with the inductive bandwidth, marked in Figure 4.3, and realizable inductances. However, the impact of the loss-compensating cross-coupled transistors, larger DC signal swings, and variances in the biasing current sources collectively have a large impact on the active inductor design. Even with attention to designing the active-inductor, a significant amount of iterative design was necessary after it was combined with the rest of the VCO structure. This is, for example, the reason why the implemented active inductor's minimum effective inductance is much lower than the estimated 4 nH. The simulated output resistance of the active inductor is provided in Figure 4.4.

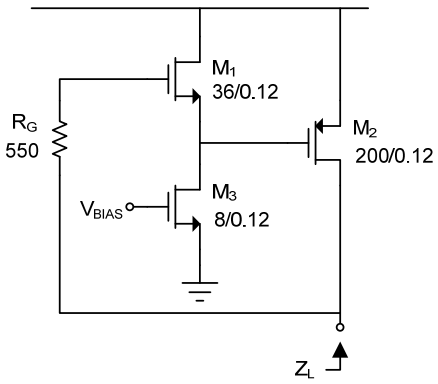



Figure 4.2: Annotated active inductor schematic

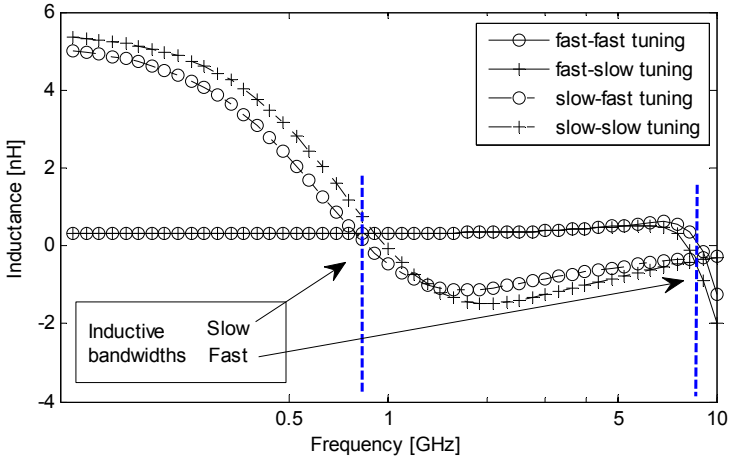



Figure 4.3: Simulated inductances of the active inductor

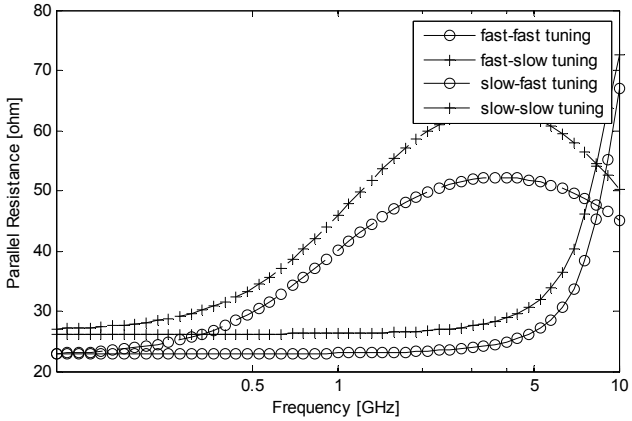



Figure 4.4: Simulated output resistance of the active inductor

## 4.2. Dual-Tuned AI-Based VCO Design

The full active-inductor-based LC-VCO schematic is shown in Figure 4.5, and is annotated with design parameters.

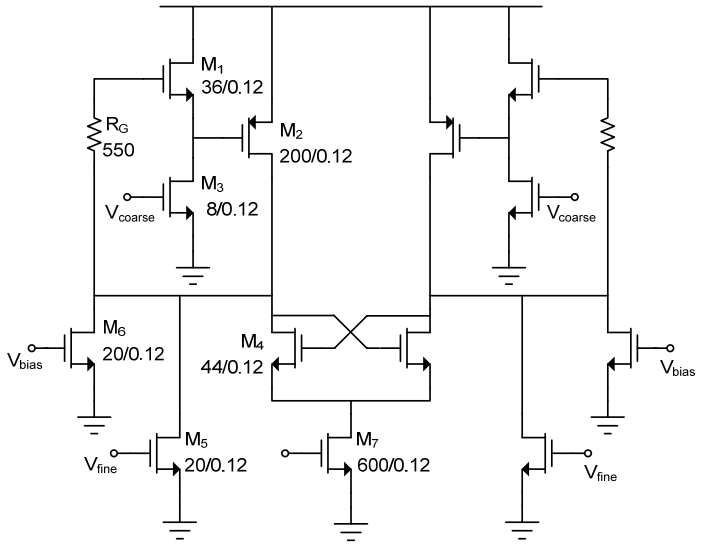



Figure 4.5: Active inductor schematic, annotated

First, the active inductor needed to be adjusted in-place to achieve the expected oscillation frequencies. The oscillation tank capacitor was underestimated in the initial designs, expecting 200 fF at the output node. To achieve an oscillation of 5 GHz and ensure oscillator start up the load of the cross-coupled pair alone approaches $3 * 60fF + 0.5 * 60fF = 210\ fF$ due to the miller capacitance and drain capacitance. The active inductor ended up loading the output with approximately 120 fF after resizing, giving a total of at least 340 *fF*. To help limit the output capacitance a multi-stage CML output buffer was added to the design. Current source parasitic capacitances were kept as small as possible while still providing sufficient tuning by keeping sizes small. This also helped keep the tuning voltage input range large.

Further complicating the stand-alone design of the active inductor is the fact that DC and large-signal biasing has a significant impact on the response of the active inductor. Stacking the inductor on the cross-coupled pair, and the output signal being much larger than the 1 mV used in the S-parameter simulations, changes the small signal parameters and affects both the inductance and output resistance.

The tuning mechanisms were designed after the oscillator was meeting the desired upper-bound frequencies. The fine and coarse tuning characteristic the active inductor means implementing two tuning controls exhibiting different orders of magnitude in their impact. The transconductances of transistors $M_1$ and $M_2$ of Figure 4.5 provide straightforward tuning mechanisms since $g_m \propto V_{gs}$ and $L \propto 1/g_m$. The transconductances were controlled through the branch currents, set by gate voltages of saturated transistors.

Assuming a fixed frequency range, as is the case for this VCO, to minimize the impact of noise on the control voltages it is desirable to use rail-to-rail control voltage swings. This is not practical using NMOS gate voltages, and so the lower limit of the control voltage is set to approximately $V_{TH}$. The top 200 mV of the supply limit is also not used for the fine control to simplify the charge pump design. For a fully integrated design the input voltage range for the coarse tuning control can be increased by decreasing the width of $M_3$ in Figure 4.5. The tuning characteristic of the VCO is plotted in Figure 4.6.

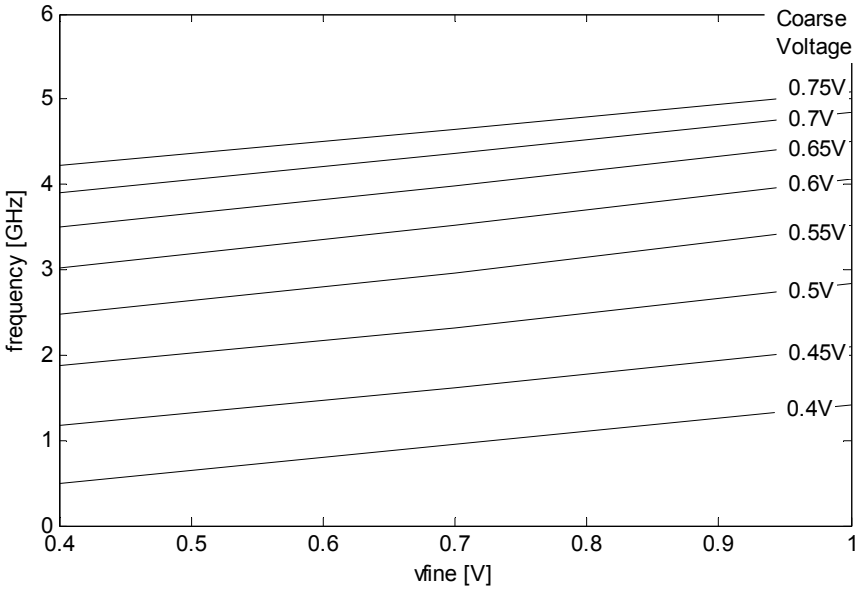



Figure 4.6: VCO tuning bands

Figure 4.6 shows that the VCO demonstrates an almost constant $K_{VCO}$ across the entire tuning band, observed by the parallel nature of the tuning characteristics versus *vfine*. The fine $K_{VCO}$ is 1.475 GHz/V with a range of ±5% across the entire tuning range. This is helpful for the PLL design since parameters like lock range, stability factor, and natural frequency will now be independent of the oscillation frequency.

The coarse tuning $K_{VCO}$ is 12.8 GHz/V. Increasing the coarse tuning past 0.75 V has a diminishing effect on the oscillation frequency as $g_{m1}$ starts to dominate over $g_{m3}$, eliminating its impact as a tuning mechanism. Lowering either the coarse or fine tuning voltages below 0.4 V further lowers the oscillation frequency, but the characteristic becomes non-linear as the transistors begin to operate in the sub-threshold regime. Significantly lowering the tuning voltages turns off the active devices and the circuit stops oscillating.

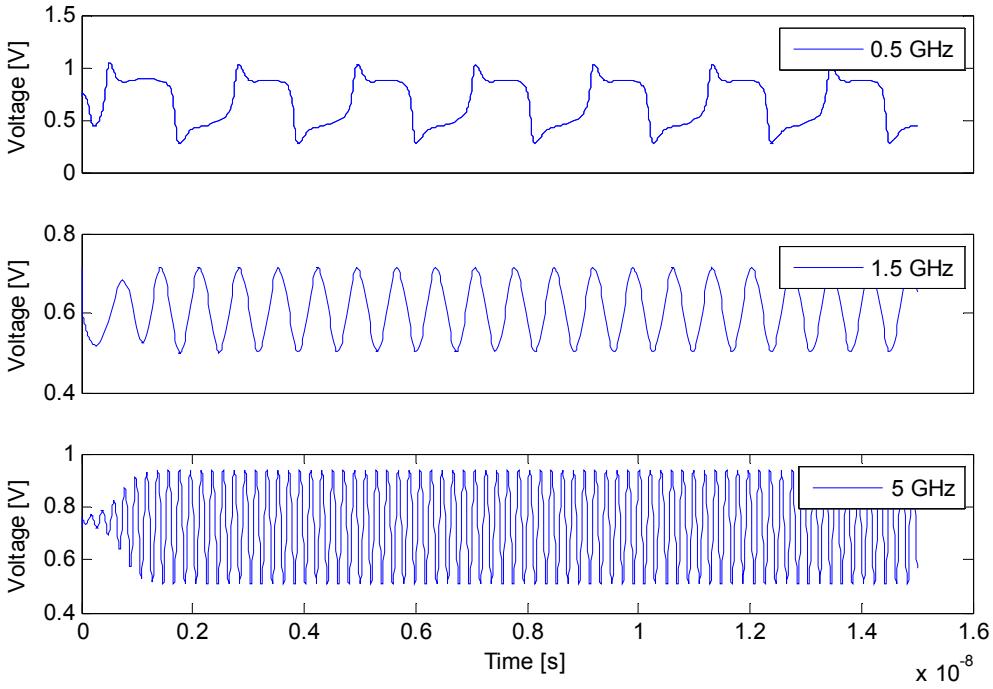



Figure 4.7: Single-ended time-domain VCO outputs

Time domain plots of the oscillator are provided in Figure 4.7**.** Square wave overshoot is due to inductive peaking after which the active inductor large-signal model can't sustain that voltage level and the system settles lower. Differentially the square wave, excluding the overshoot, has a large enough magnitude to fully switch a CML differential pair and the overshoot has little impact on system performance. The low-frequency time domain plots do, however, provide a second motivation for implementing a VCO buffer along with reducing the load capacitance – namely increasing the amplitude of the signal for the low amplitude signals. The limited amplitude observed at 1.5 GHz is a symptom of insufficient active compensation for LC-tank losses, which can lead to startup problems.

The VCO, being an oscillator, relies on a loop gain greater than one to start its oscillation by amplifying the noise of the system . Startup testing is accomplished by including a small (nV)

noise source within the loop and running transient simulations to ensure that the loop gain is sufficient.

To satisfy the startup concerns one option is to decrease the losses of the inductor, which also leads to a lower inductance, but requires larger devices and reduces the active inductor's bandwidth. A second method employed is to increase the size of the cross-coupled transistors to provide extra gain. A combination of both was necessary to ensure startup across all process and tuning corners.

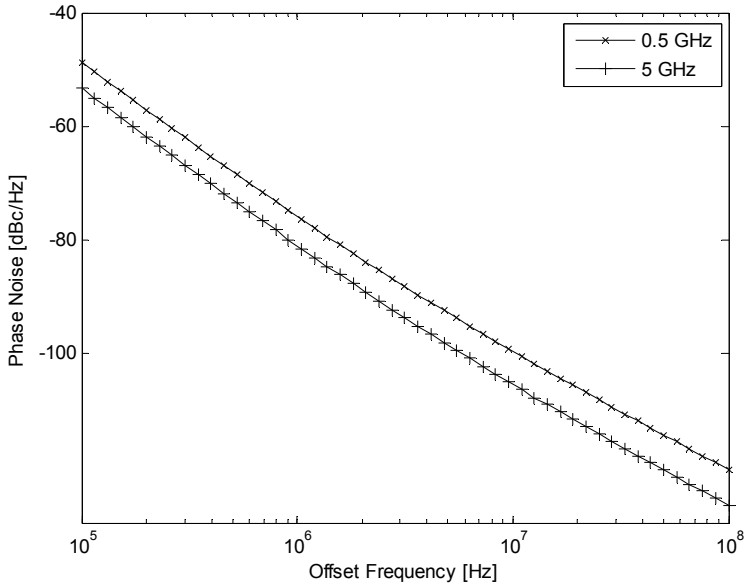



Figure 4.8: VCO phase noise

The simulated minimum and maximum phase noise is plotted in Figure 4.8. It demonstrates limited variability, only 5 dBc/Hz, across the entire tuning range. The phase noise is -81.6 dBc/Hz and -76.5 dBc/Hz at a 1 MHz offset for oscillations at 5 GHz and 1.5 GHz, respectively. The increase in phase noise at lower frequencies can be attributed to the lower signal amplitude, which means that a fixed $\Delta V_{noise}$ will have more impact since the carrier crosses that voltage threshold at a phase further from 0°. Furthermore the VCO buffer exhibits a higher noise per

fractional bandwidth at lower frequencies, shown in Figure 4.34. The power consumption of the VCO is between 18 mW and 36 mW, climbing with both the coarse and fine tuning controls, as they increase the current draw of the circuit.

The layout for this block was non-trivial. Initial layout had a significant margin for manufacturing and reliability, but caused a frequency drop of almost 1.5 GHz out of the maximum 5 GHz oscillation frequency. The design is strongly dependent on the parasitic capacitances at the oscillation node and internal active inductor nodes, so the design was reworked to limit the capacitances at these nodes. The final layout can be found in Appendix A.

Two techniques to reduce layout capacitances are discussed here. First, power and ground rails are placed along both sides and multiple layers are used for horizontal routing to minimize the DC current and therefore width of the horizontal power rails. This allows a more vertically compressed structure and lower routing capacitance. Transistor fingers are horizontally aligned between vertically connected transistors when possible, and are connected directly on lower metal layers instead of grouping, for example all connecting the drains of a transistor before redistributing to the gate of the next transistor. All connections to a single transistor terminal are shorted to prevent any phase or voltage mismatching, but are not used in the signal path. This also helps limit distance between circuit elements and reduces parasitic capacitances.

## 4.3. CML Logic Gate Design

The CML logic gates take much of their design procedure from the CML circuit design techniques discussed in Section 3.5. They use a $V_{TH}$ signal swing to fully switch the current without driving

transistors out of saturation. The output pole sets the circuit bandwidth and maximum the load resistance, which will also allow for the minimum biasing currents.

The required bandwidth of the CML logic is set by the maximum oscillation frequency of the VCO for most blocks, as decisions must be made within one clock cycle of the VCO before being pipelined to the next circuit block. The flip-flop, however, must operate at twice this frequency since its decision must be ready in half a clock cycle due to the phase detector structure.

### 4.3.1. Flip-Flop

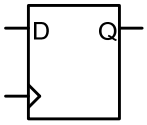



Figure 4.9: Flip-flop schematic symbol

The flip-flops acquire the value of the data signal on the falling edge of the clock. This value is passed through to the output on the next rising clock edge. Figure 4.11 gives an example of this timing. Once the data has been captured it is unaffected by any subsequent changes at the input. The cascaded-latch based flip-flop, see Figure 4.10 for a block diagram or the schematic in Figure 4.12, allow the use of CML latches while exhibiting reasonably ideal capture characteristics.

For an individual latch when the clock is enabled the input value is passed to the output. When the clock goes low the inputs are disconnected and the latch holds the output value steady. There will be some input feedthrough due to the overlap capacitances, obvious in Figure 4.13. This is minimized by keeping the overlap capacitance as small as possible relative to the total capacitance at the output node and increasing the strength of the cross-coupled regenerative transistor pair.

To minimize delay the second latch is sized larger than the first. The sizing is set to minimize the delay of the critical flip-flop, highlighted in the phase detector (Figure 4.16), which must operate at 10 GHz, instead of 5 GHz. The input capacitance of the second latch is taken as the average of the flip-flop output capacitance and an estimate of the input capacitance in order to minimize total delay [52]. The annotated schematics for the two latches creating the flip-flop and simulated I/O characteristics are provided below.

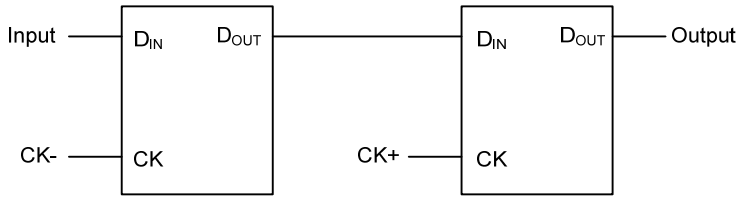



Figure 4.10: A flip-flop comprised of two back-to-back latches

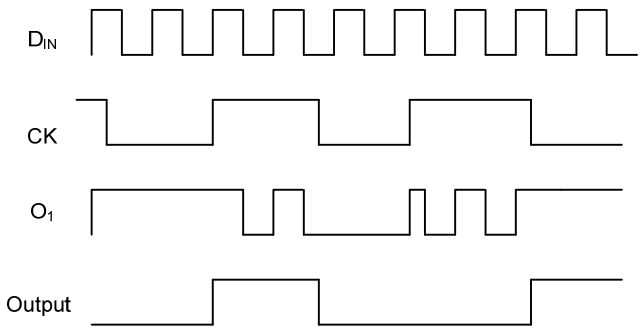



Figure 4.11: Latch-based flip-flop timing diagram

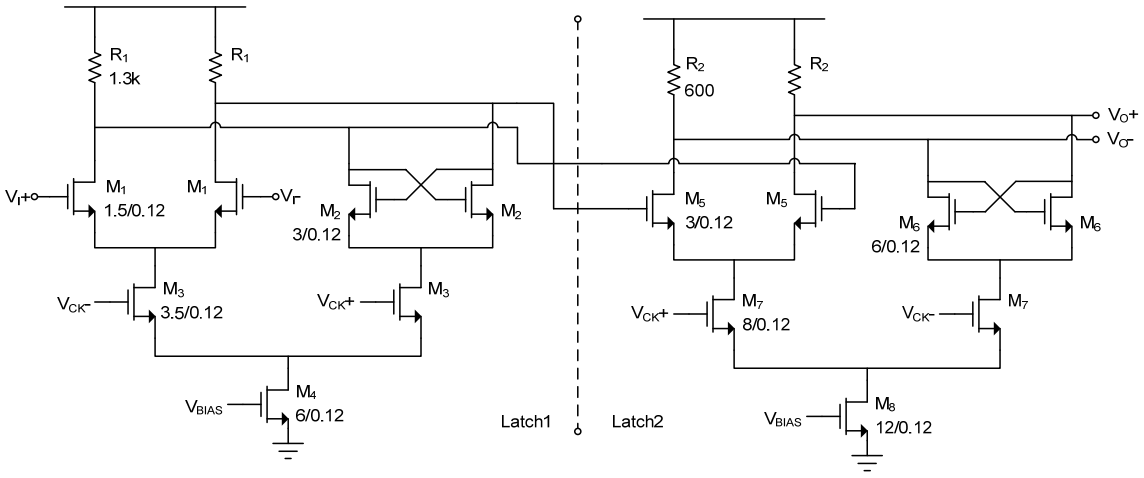



Figure 4.12: Latch based flip-flop schematic

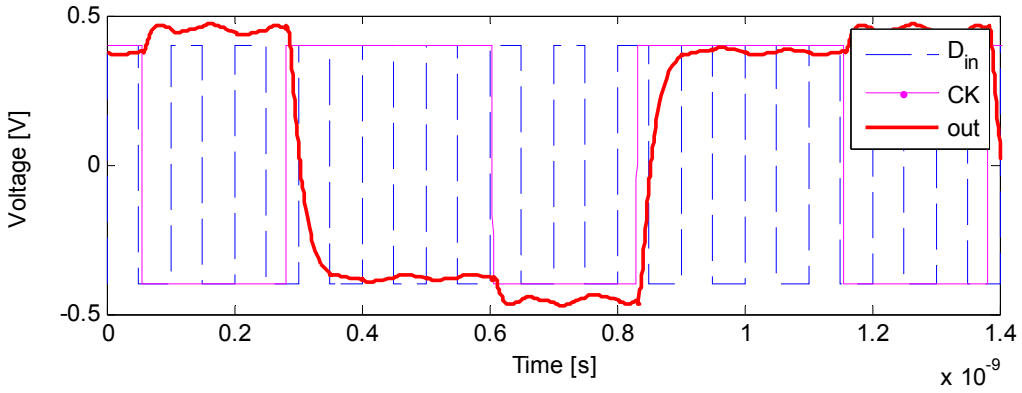



Figure 4.13: Flip-flop transient simulation results

The clock edges in the design will not be vertical which creates uncertainty in pick-off. Ideally the clock-enable transistors ($M_3$ and $M_7$ in Figure 4.12) switch at the precise moment the differential clock crosses 0V, but this is not the case since the transistors will slowly turn off instead of instantaneously. If the data input is changing near the same time as the clock the flip-flop may miss slightly early data edges or catch slightly late data edges.

The single current source ($M_4$, $M_8$) is used to bias both current paths and gives a constant current draw reducing substrate noise injection and generates a consistent common-mode

output voltage though a constant IR drop across output resistors. It necessitates slightly larger transistors and higher biasing currents since overdrive voltages must be smaller to accommodate an extra transistor in the stack.

### 4.3.2. XOR

The truth table for the exclusive-OR block is shown in Table 4.1**.** The schematic implementing the gate used in the phase detector is shown in Figure 4.14.

Table 4.1: XOR I/O truth table

| Input1 | Input2 | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

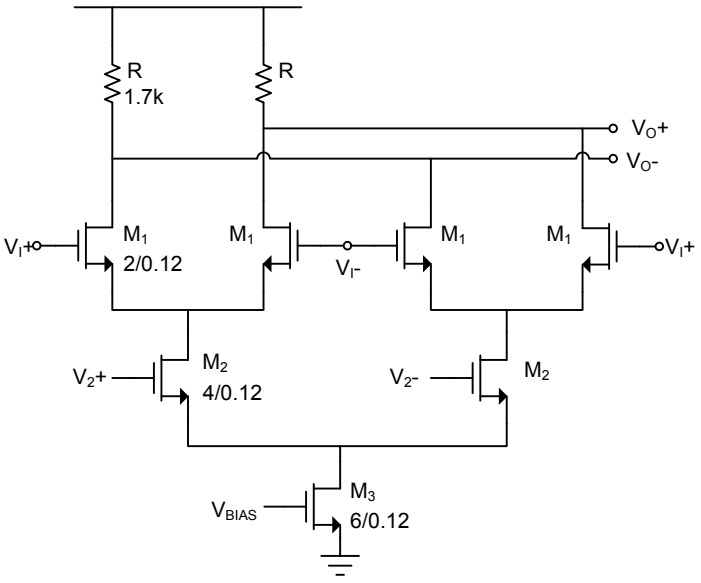



Figure 4.14: Annotated XOR schematic

The design of this block follows the same method as the flip-flop in Section 4.3.1. The input capacitance is set to scale between the preceding (latch) and subsequent (MUX) circuit blocks. The resistance and bias current are set to meet the 5-GHz bandwidth requirement and $V_{TH}$ output voltage swing. It is desirable to keep the input capacitances of the two inputs equal in order to allow for simpler integration in layout; equal input capacitances mean that the inputs can be swapped without impacting the performance of the previous block. To accomplish this the higher inputs, labeled $V_{2+}$ and $V_{2-}$ on the schematic, are sized half that of the $V_{1+}$ and $V_{2-}$ inputs.

### 4.3.3. MUX

The multiplexer circuit passes one of two inputs to the output based on a select signal. The truth table is found in Table 4.2. The schematic is given in Figure 4.15. The purpose of the multiplexer is to allow switching between the bang-bang type phase detector and linear phase detector to change the PLL loop dynamics. It must also drive the charge pump ensuring that the transistors are fully switched to minimize current leakage.

Table 4.2: MUX I/O truth table

| Clock | Output |
|---|---|
| 0 | $V_2$ |
| 1 | $V_1$ |

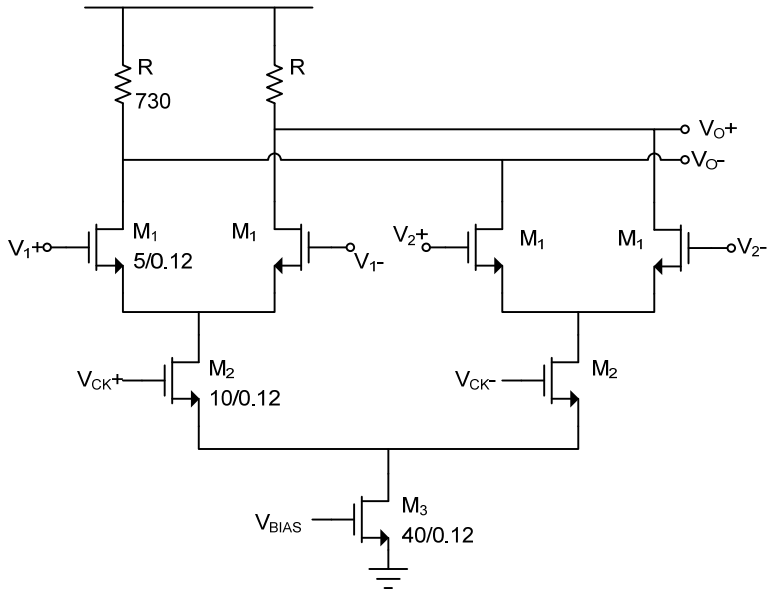



Figure 4.15: Annotated MUX schematic

The output resistor is sized to provide a 5 GHz bandwidth when loaded. The current is set to provide a larger output swing, equal to 0.8 V, instead of $V_{TH}$ in order to completely open and close the charge pump switches. This will cause significant non-linearity in the circuit response and reduces the effectiveness of the hand analysis, so some iterative design can be expected after using the typical CML circuit design strategy as a starting point.

## 4.4. Multiband PLL Design

This section covers the design of the PLL blocks and loops as well as providing simulation results for the discussed blocks. Circuits implemented in the previous sections, the active-inductor-based VCO and CML blocks, are used to build the PLL loop. The VCO buffer, presented in Section 4.5.2 is also included in the PLL loop. The specific blocks discussed are the bang-bang PFD and

linear PD, charge pump with offset compensation, and loop filter. Schematics and simulation results are given for these blocks. The PLL loop is then simulated to show locking characteristics.

### 4.4.1. Phase-Frequency Detector

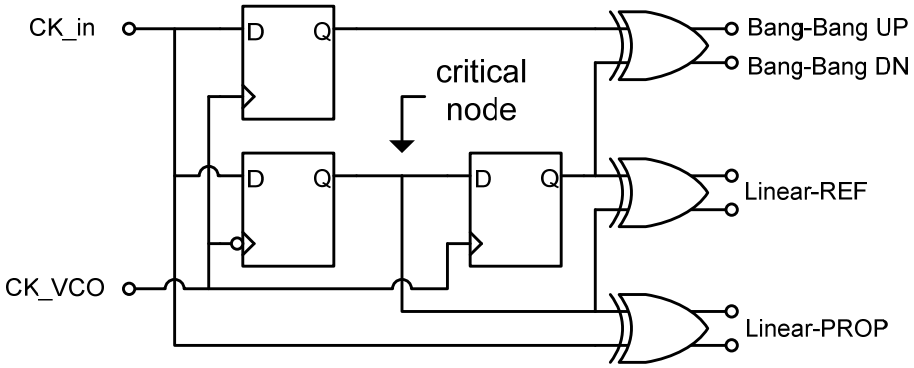
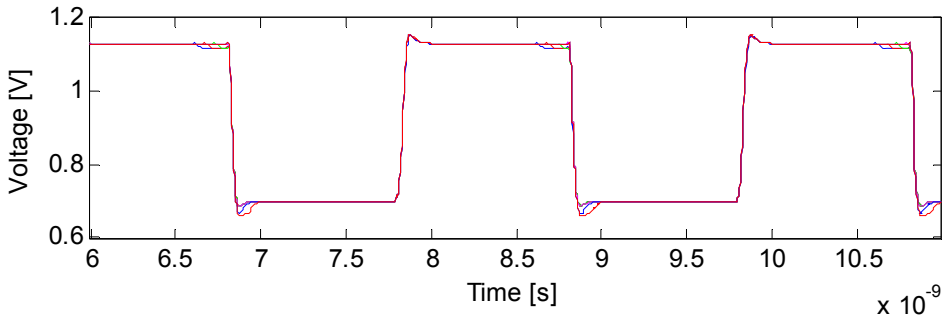


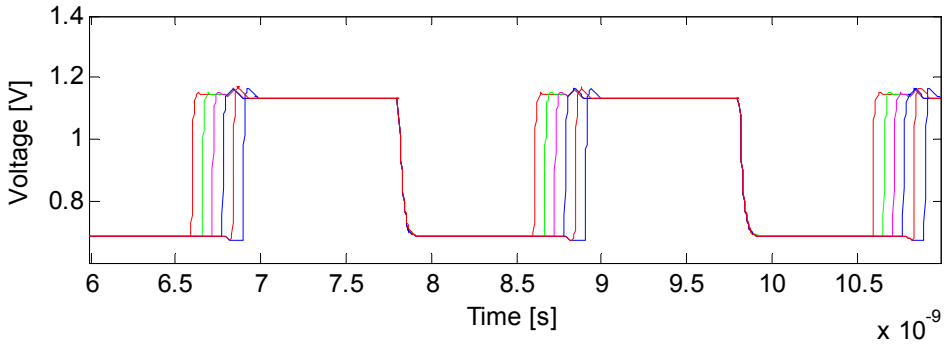

Figure 4.16: Hybrid bang-bang/linear phase detector

For the phase detector presented in Section 3.4.1, and repeated in Figure 4.16, to be reliable, every internal node must be resolved before it is used by the subsequent circuit block. While the maximum operating frequency of the input is 5 GHz, due to the structure of the phase detector, the critical node labeled in Figure 4.16 must be resolved in half a clock cycle. The driving circuit must have a bandwidth of 10 GHz, and is the motivation for the 10 GHz flip-flop design, discussed in Section 4.3.1. The design of the 5 GHz XOR gate is presented in Section 4.3.2.

Simulation results for the phase detector are provided in Figure 4.17 and Figure 4.18 for a 0.5 GHz and 5 GHz input VCO clock, respectively, showing phase misalignments from 0 ° to $\frac{0.1}{f_{ck}}$ ° late. The non-idealities of the circuit implementations smear the signal edges at 5 GHz. As frequency rises the ratio of average area under the reference to proportional pulses drops. Compensation for this is implemented by increasing the strength of the down pump current in the charge pump, as discussed in Section 4.4.2.

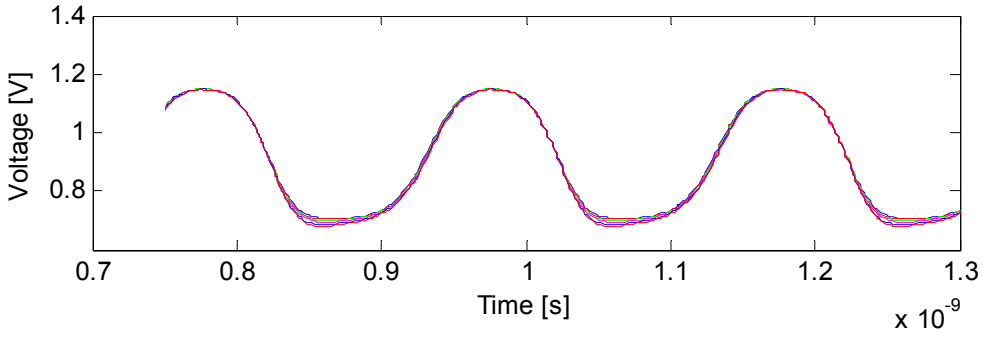



a. Linear reference pulses

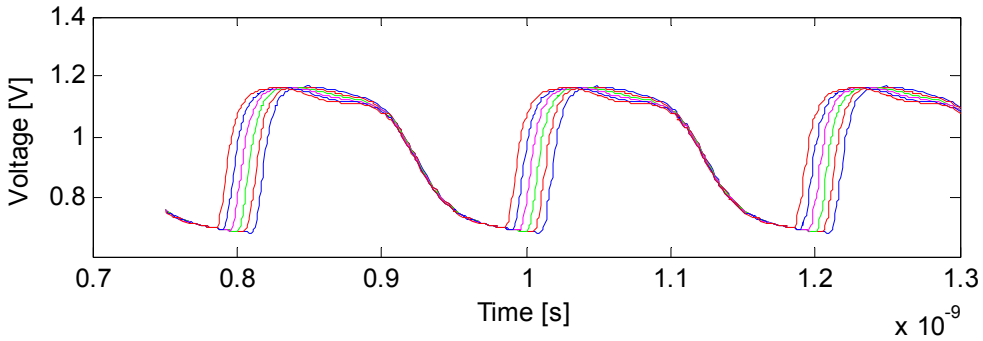



b. Linear proportional pulses

Figure 4.17: Linear phase detector outputs at 0.5 GHz for various phase differences




a. Linear reference pulses




b. Linear proportional pulses

Figure 4.18: Linear phase detector outputs at 5 GHz for various phase differences

### 4.4.2. Charge Pump with Offset Compensation

This section covers the design of the charge pump presented in 3.4.2. The annotated charge pump schematic, including offset compensation circuitry, is provided in Figure 4.19. Table 4.3 provides element values for the charge pump. The <x:y> notation represents an array of size $N = y - x$. Transistors $M_{6\text{-}10}$ all represent multiple, but identical, transistors.

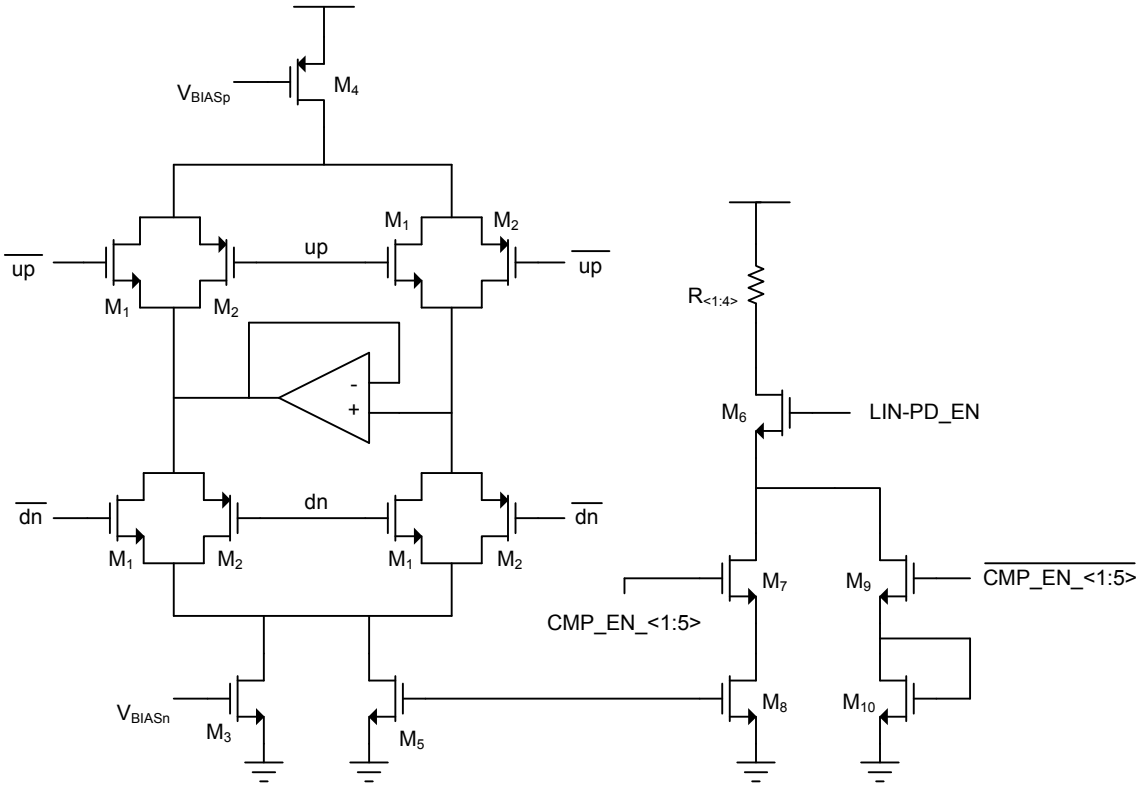



Figure 4.19: Charge pump and compensation circuits schematic

Table 4.3: Element sizes for charge pump schematic

| Element | Size [µm] | Element | Size [µm] | Element | Size [µm] | Element | Size [µm] |
|---|---|---|---|---|---|---|---|
| $M_1$ | 10/0.12 | $M_2$ | 10/0.12 | $M_3$ | 60/0.24 | $M_4$ | 150/0.24 |
| $M_5$ | 5/0.24 | $M_6$ | 10/0.12 | $M_7$ | 10/0.12 | $M_8$ | 5/0.24 |
| $M_9$ | 10/0.12 | $M_{10}$ | 5/0.24 | | | | |
| Element | Size [Ω] | Element | Size [Ω] | Element | Size [Ω] | Element | Size [Ω] |
| $R_1$ | 18.75k | $R_2$ | 26.7k | $R_3$ | 28k | $R_4$ | 14.75k |
| $R_5$ | 16.75k | | | | | | |

The charge pump uses a single MOS sources to minimize headroom at the expense of constant supply current. To improve the output resistance and compensate for the simple architecture non-minimum transistor lengths were used for the source transistors. Widths of the current sources were selected such that when supplying the desired current, in this implementation 100

μA, the gate voltages could be selected to maintain the devices in saturation to provide as constant a current as possible. The transistor lengths were chosen so the percentage difference in minimum to maximum current provided by the charge pump is at most ± 10% from the nominal supply.

Pass gates are used to pass both high and low voltages across the gate even if the voltage is within $V_{TH}$ of the supply rails [52]. They also will absorb some of the charge injection when switched off since their channels accumulate opposite carriers [27]. It is possible to optimize the relative sizes to minimize charge injection [27]. A sizing of $W_p=W_n$ was used.

The sizes of the switches were selected to ensure that the voltage drop across each pass gate was small enough to allow the charge pump to reach the desired output voltage levels when driving the charge pump. This minimum size was used to keep the capacitance presented to the previous as small as possible. Figure 4.20 shows the charge pump charging and discharging the output capacitance to its maximum and minimum output voltages before the up and down pulse width differences are insufficient to overcome the current source non-idealities. The inputs to realize the plot are pulses mimicking the linear phase detector output for a constant phase difference. The achieved voltage range is sufficient to span the VCO control voltage range, passing both 1 V and 0.4 V as the upper and lower limits, respectively. The voltage limits do not vary significantly across frequency bands or for different input phase differences, but the time taken for the charge pump to settle at the maximum or minimum voltages will vary.

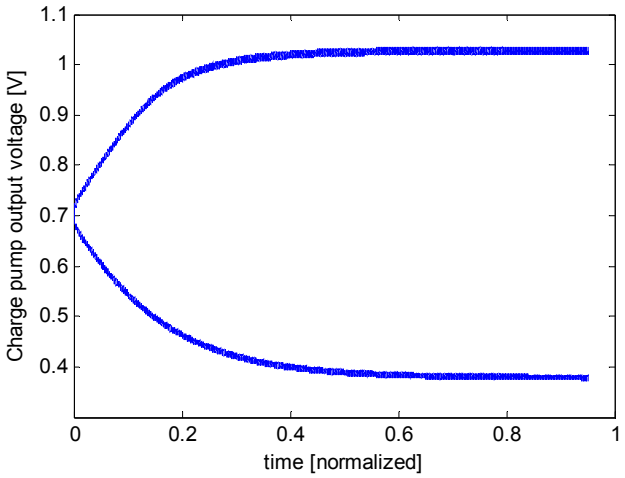



Figure 4.20: Up and down charging of charge pump

The charge pump and phase detector combination should have a zero-current average when the phases are aligned, locking the signals at a constant phase difference. The non-idealities in the PD/PFD and CML circuitry, as discussed in Section 4.4.1, give rise to a phase locking offsets that increase in magnitude as the frequency increases, shown in Figure 4.21. To compensate the charge pump has switched current sources that are activated as the band selection voltage increases to augment the down current source. They are transistors added in parallel with the down current source, whose biasing circuitry is presented in Figure 4.19 ($M_{6\text{-}10}$). The comparator bank determines which extra current sources are necessary, enabling the current mirrors. Figure 4.21 shows the observed average phase difference between the input clock and VCO clock when locked.

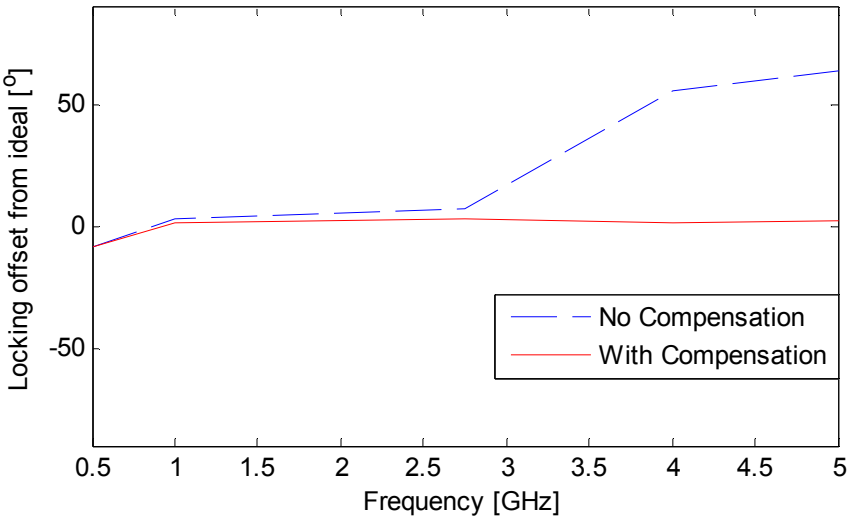



Figure 4.21: Charge pump locking phase offsets due, before and after compensation

The *CMP_EN_x* signals in Figure 4.19 are set high as the VCO coarse tuning voltage increases. The voltages at which the compensation circuits are enabled are given in Table 4.4. The enable voltages could also be controlled, for example, by the output of a thermometer encoded A/D instead of a comparator bank. The envisioned implementation is to use one compensation circuit for each coarse tuning band, however only five circuits are implemented to limit the complexity.

Table 4.4: Enable voltages for charge pump compensation circuits

| Compensation Circuit | Voltage to enable CMP_EN_*x* [V] |
|---|---|
| 1 | 0.4 |
| 2 | 0.475 |
| 3 | 0.525 |
| 4 | 0.645 |
| 5 | 0.745 |

### 4.4.3. Loop Filter

The initial loop filter design is set such that the loop filter bandwidth is approximately 1/10 times the lowest reference frequency, or 50 MHz. This falls within the recommended range of $1/100^{th}$ to $1/10^{th}$ of the VCO output frequency and frequently used as a rule of thumb [53]. Adjusting the capacitances and resistance using Matlab simulations, including phase detector and circuit block parameters highlighted in Section 3.4.4, the phase margin was set to 41.5° for the loop filter given in Figure 4.22. For this loop filter the bandwidth is 50.5 MHz, and sets a PLL natural frequency ($\omega_0$) equal to 1.3 MHz.

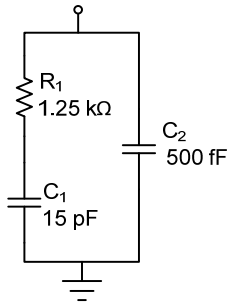



Figure 4.22: Annotated loop filter schematic

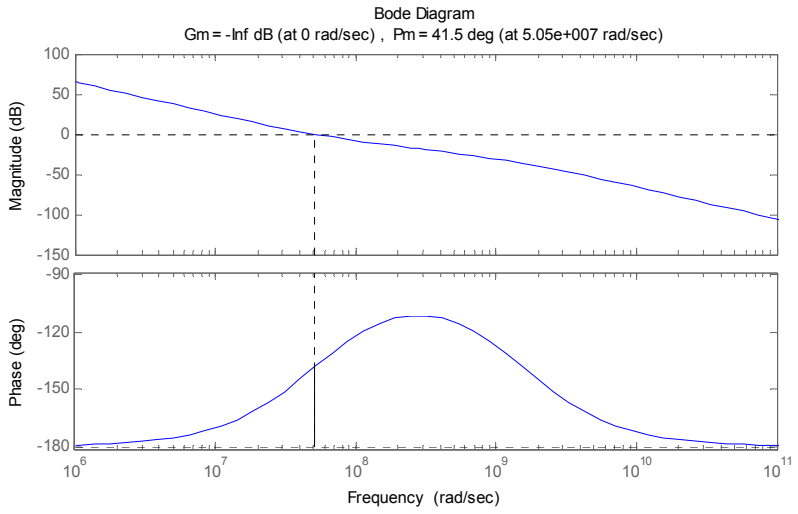



Figure 4.23: Loop phase margin for 2nd-order model

### 4.4.4. Loop Design and Simulation Results

An example of the PLL locking with the bang-bang phase detector is provided in Figure 4.24. There is a significant amount of jitter on the control line after locking. In fact, it is 3-4 times the expected hunting jitter, taking 3-4 bang-bang phase-detector pulse excursions from the locked frequency instead of the expected 1 cycle. This is especially problematic at low frequencies where each up/down pulse causes a significant frequency excursion (Figure 4.25).

Attempts to correct this problem included increasing by using loop filter elements with unrealizable sizes to increase the estimated phase margin to 90-degrees and higher, which at best reduced this hunting jitter to the expected amount for 100 ns. After 100 ns the loop returned to the observed 3-4 cycle correction period. Increasing the charge pump current 2x to increase the loop gain did not have any effect. Decreasing the charge pump current to limit the frequency difference between charge pump pulses reduced the magnitude of the excursion, but not the number. Simultaneously decreasing the charge pump current and increasing the phase margin reduced the settling time of the PLL without eliminating the extra excursions.

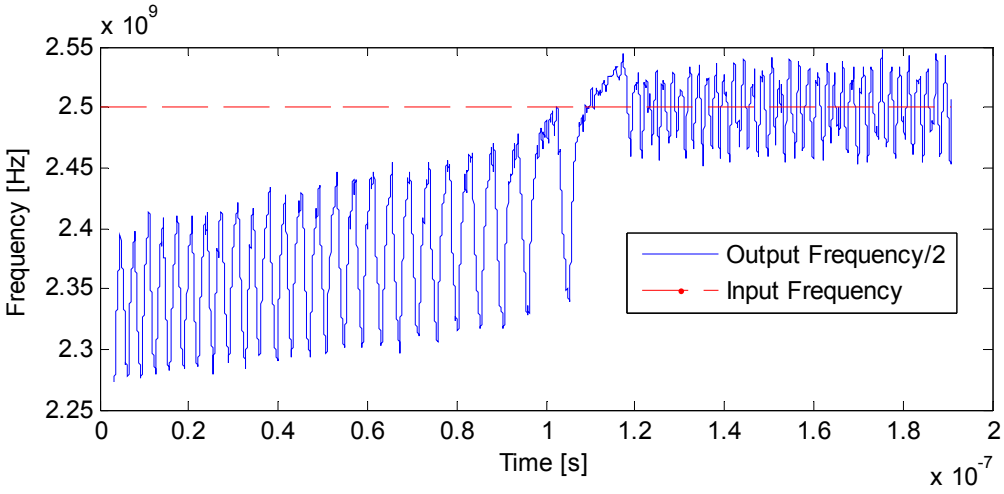



Figure 4.24: Bang-bang PLL locking to 2.5GHz input clock

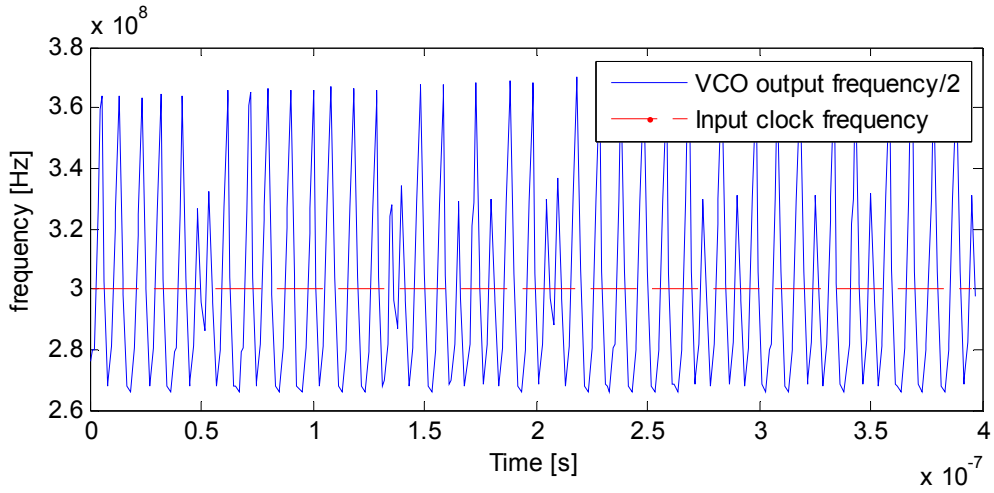



Figure 4.25: Bang-bang PLL locked to 300MHz input clock

The VCO buffer is found to be a significant contributor to this excess jitter problem. There is a 160 ps delay after adjusting the VCO frequency before it is available at the input of the phase detector. Exchanging the AI-VCO for a monolithic LC-VCO at 5 GHz and increasing the phase margin eliminated this problem. Unfortunately it was not feasible to redesign the VCO without

the buffer, which is necessary both to drive the output capacitance at high frequency and ensure sufficient swing to switch the phase detector transistors.

As a result of this added delay, measured locking times for the PLL are also longer than expected, since the loop deviates significantly from the modeled second order loop. Simulations showed that it can take up to 620 ns for the PLL to cross the entire VCO band and lock to the incoming signal.

The linear PD is tested to pull in the VCO frequency by 150 MHz across the frequency bands to ensure that the pull in range large enough to lock to the input phase and frequency despite the large bang-bang jitter. The VCO buffer delay jitter phenomenon is not observable with the linear phase detector due to the zero average current injected into the loop filter when locked. A plot of the PLL locking with the linear phase detector is provided in Figure 4.26.

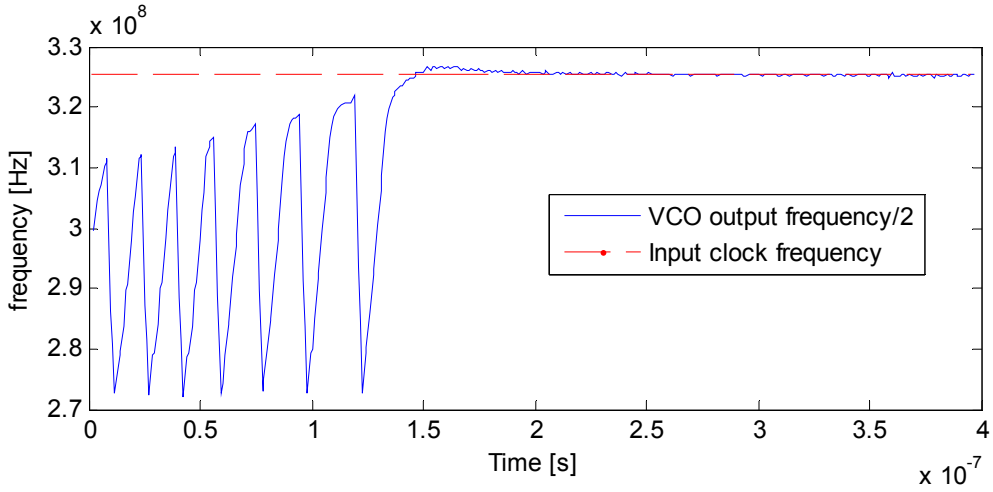


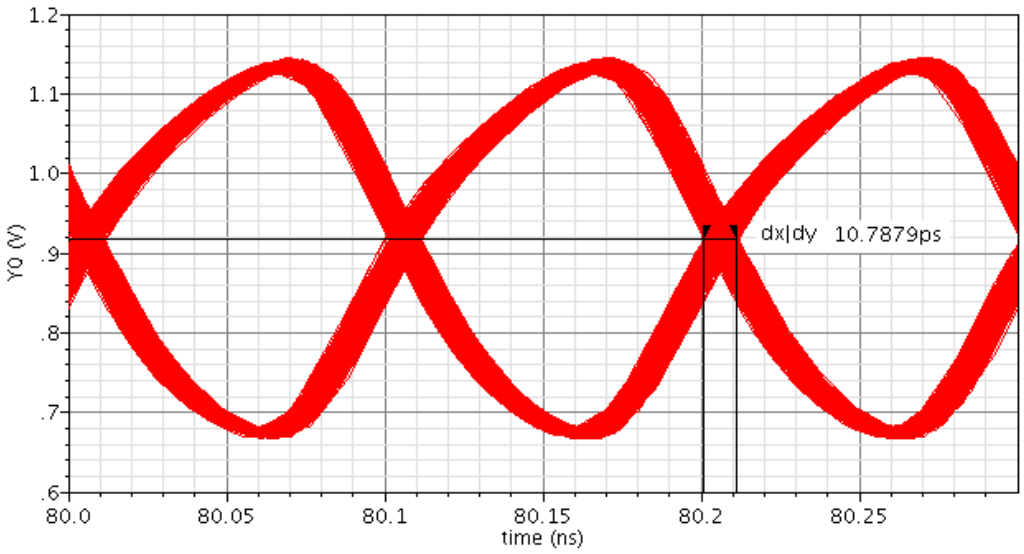

Figure 4.26: PLL locking with linear PD

Simulated eye diagrams for the locked bang-bang PD and linear PD can be found in Figure 4.27 and

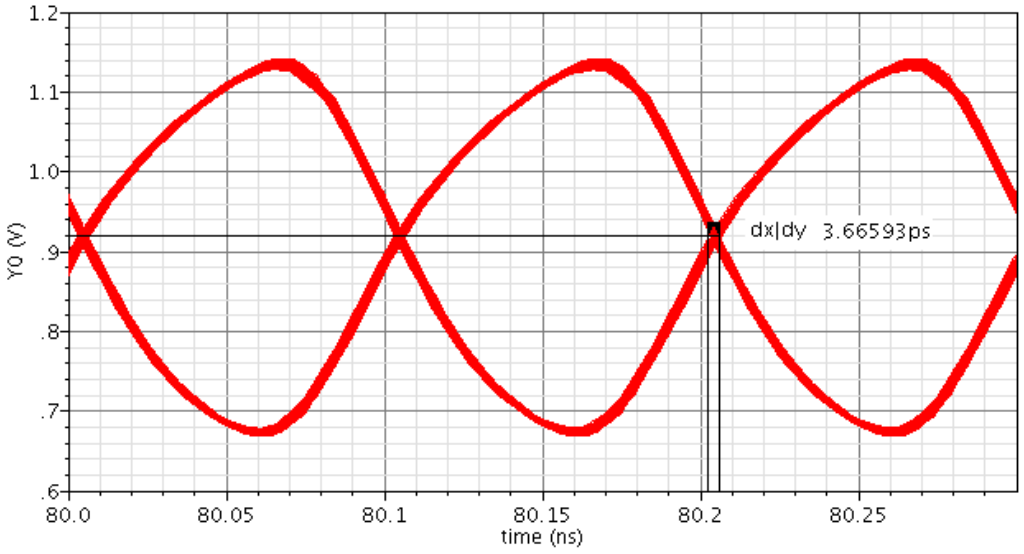
Figure 4.28, respectively. It is obvious from the low-frequency eye diagrams that the bang-bang phase detector is not providing an acceptable locking mechanism and the linear phase detector is necessary. Observed peak-to-peak output clock jitter is recorded in Table 4.5, note that at 0.5 UI the eye is completely closed.

Table 4.5: Simulated peak-to-peak PLL output jitter

| Frequency [GHz] | Linear PD Jitter | | Bang-bang PD jitter | |
|---|---|---|---|---|
| | [UI] | [ps] | [UI] | [ps] |
| 5 | 0.018 | 3.6 | 0.054 | 10.8 |
| 0.6 | 0.013 | 21.7 | 0.37 | 617 |

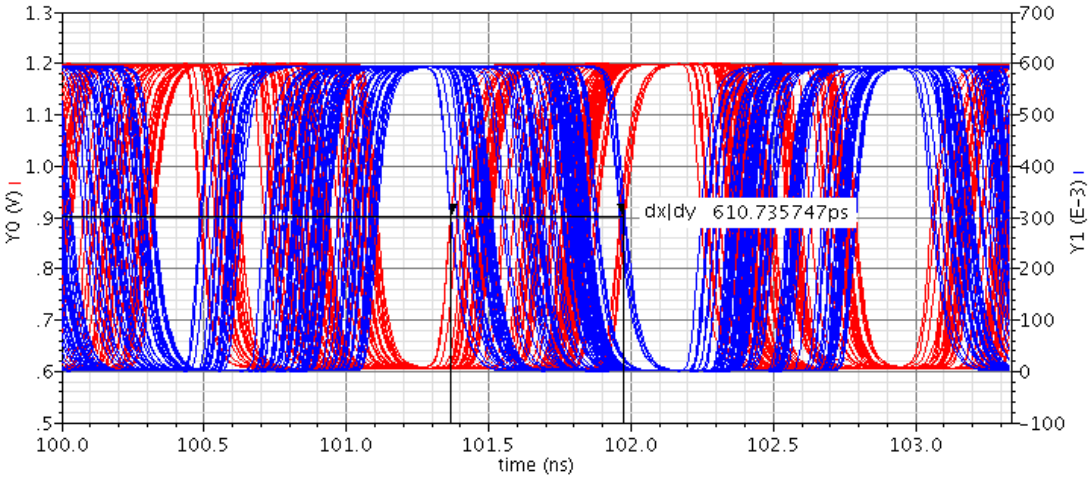



a. Bang-bang PD eye

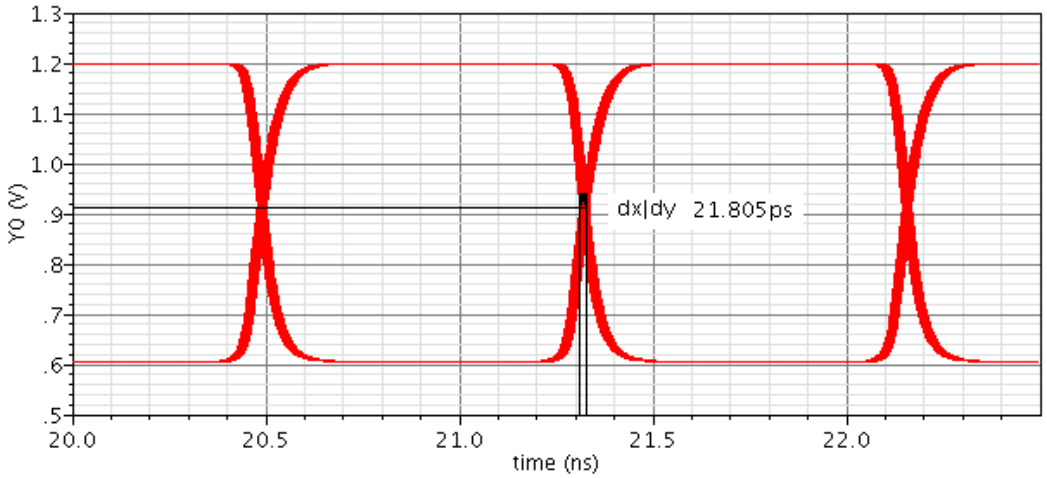



b. Linear PD eye

Figure 4.27: VCO output eye diagrams at 5 GHz




a. Bang-bang PD eye




b. Linear PD eye

Figure 4.28: VCO output eye diagrams at 600 MHz

## 4.5. Buffer Design

This section covers the design of both the VCO and output CML buffers. First covered is the output buffer driving the 50-ohm instrumentation for measurement and then the VCO buffer in order to isolate the VCO output node from the phase-detector and output buffer loading.

### 4.5.1. Output Buffer Design

The output buffer is included to drive the 50-ohm transmission line to the measurement devices and approximately of 100 fF pad capacitance without significantly changing the PLL loop dynamics. A CML buffer is implemented for this purpose, as it will meet this goal as well as exhibiting design simplicity and good linearity. The delay of the buffer can be de-embedded from phase lock measurements as long as it can be characterized, but is minimized anyway since it is relatively straightforward to do so.

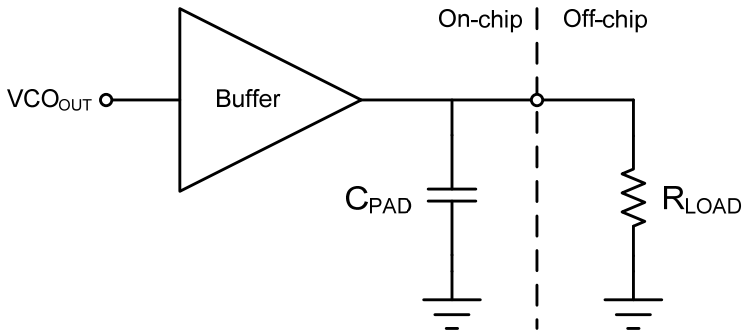



Figure 4.29: VCO output buffer and load schematic

In order to deliver maximum power to the load the output resistance of the buffer shown in Figure 4.29 should be 50 Ω. This is accomplished by assigning the final stage's output resistance equal to 50 Ω. Solving (3.49) for this case gives a cell bandwidth of 63 GHz. Even with parasitic capacitances along any interconnect the circuit will have no trouble driving a 5 GHz signal.

The input capacitance of the buffer is chosen as 3 fF, 10 times less than the total capacitance already seen at the input due to the other blocks (approximately 9 fF + 30 fF). From (3.50) the buffer needs a minimum of 3.5, which is rounded up to 4 stages.

Resistors are sized smaller than required for the 5 GHz bandwidth, by about 15%, to reduce design iterations due to transistor and layout parasitic capacitances, and the bandwidth degradation exhibited by cascaded circuits [54].

As discussed in Section 3.5 the transistors of each preceding stage is sized approximately *e* times smaller than its load. To help limit overall active area single transistor current mirrors are used to define the required bias currents. To maintain the same sizing ratio for the current sources a single gate voltage that keeps the transistors in saturation is used for all the current mirrors.

The final design sizes are listed in Table 4.6. The four-stage buffer schematic is given in Figure 4.30. The AC response of the circuit is given in Figure 4.31 and $\omega_{3dB}$ is approximately 3 GHz. The gain degradation at frequencies less than the maximum input frequency is not a concern, since the input magnitude will be as large as the maximum output frequency and the circuit gain is still greater than one.

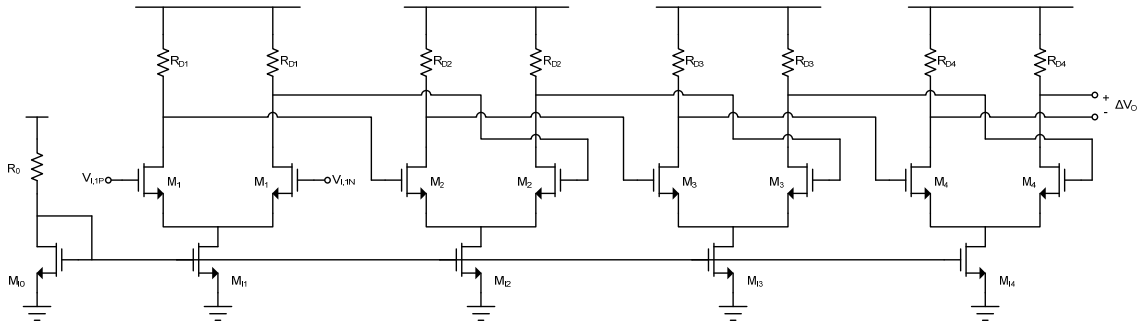



Figure 4.30: Output buffer schematic

Table 4.6: Output buffer design values

| Element | Value | Element | Value |
|---|---|---|---|
| $R_{D1}$ | 2.27 kΩ | $W_{M1}$ | 3 µm |
| $R_{D2}$ | 845 Ω | $W_{M2}$ | 7 µm |
| $R_{D3}$ | 325 Ω | $W_{M3}$ | 20 µm |
| $R_{D4}$ | 50 Ω | $W_{M4}$ | 50 µm |
| $R_0$ | kΩ | $W_{MI0}$ | µm |
| $W_{I1}$ | 4.5 µm | $W_{I2}$ | 13 µm |
| $W_{I3}$ | 32 µm | $W_{I4}$ | 210 µm |

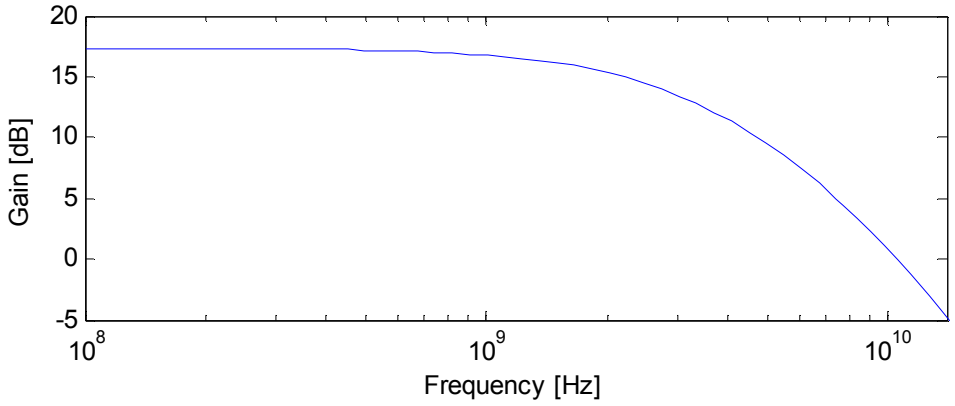



Figure 4.31: Output buffer AC gain

### 4.5.2. VCO Buffer Design

The VCO buffer's purpose is two-fold. First, it minimizes the loading capacitance seen by the VCO . Second, some of the VCO output frequencies generate a peak-to-peak voltage level too small to drive the following CML blocks properly and the buffer compensates by providing extra gain. It is important to minimize the delay of this buffer to limit its impact on the PLL loop, since the modeling does not include any delay at the output of the VCO. Since there is no output

impedance to match like the output buffer its sizing is determined by the capacitive load it must drive and the required gain.

The load capacitance from the phase detector is approximately 35 fF. It is assumed for this design that the output buffer capacitance is negligible.

The required gain is:

$$A = \frac{V_{req}}{V_{in}} = \frac{V_{TH}}{V_{pp,min}} \cong \frac{400mV}{100mV} = 4\ [V/V] \tag{4.5}$$

The buffer is implemented in two stages with scaling factors close to *e* to minimize delay. The schematic is annotated in Figure 4.32. The measured AC gain is given in Figure 4.33. The simulated 15 dB provides a gain just over 5, satisfying the required gain of 4 with a small margin. $\omega_{3dB}$ is approximately 3 GHz, less than the frequency of the maximum input frequency. However, since the input magnitude at this frequency is equal to the maximum output magnitude a gain greater than one is sufficient.

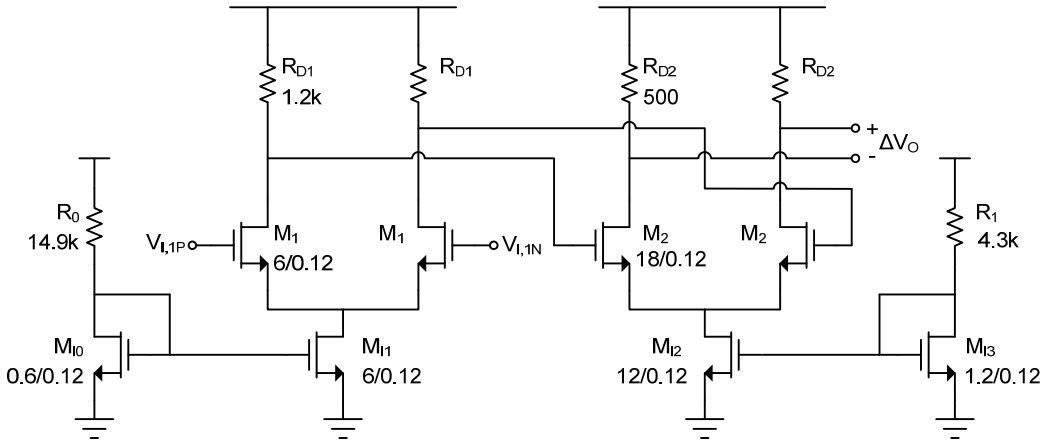



Figure 4.32: VCO buffer schematic

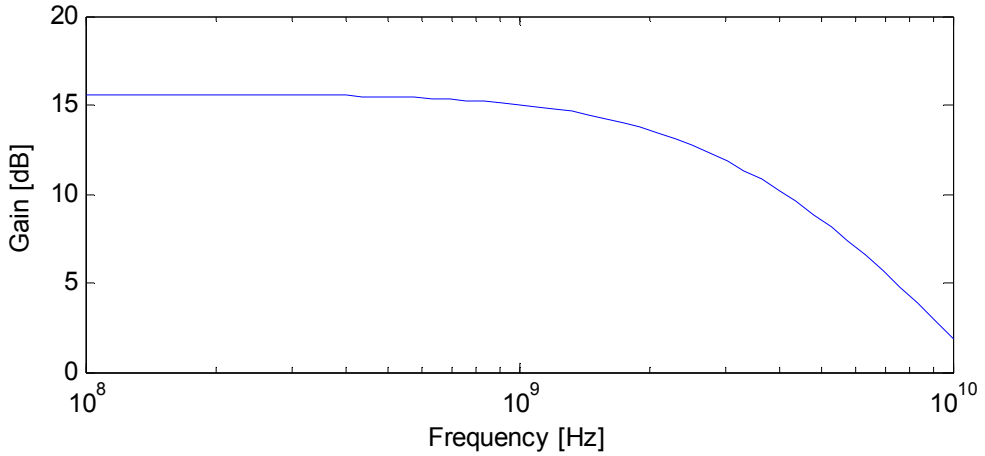



Figure 4.33: VCO buffer gain

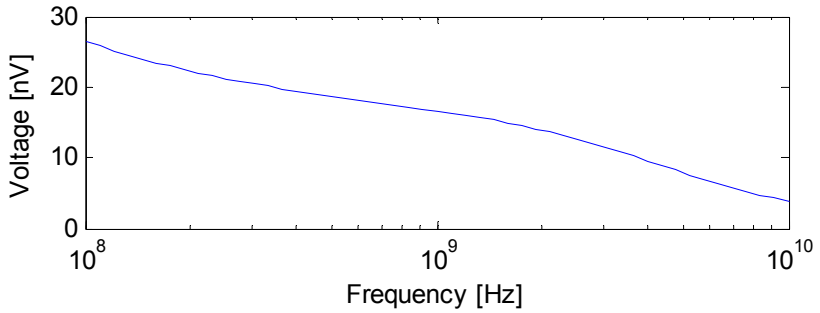



Figure 4.34: VCO buffer noise

## 4.6. Coarse Band Selection

This work does not include any circuitry in order to choose the appropriate band for locking. Ideally this would be accomplished automatically, and so a band-selection approach is described here as a possible solution. The concept is to begin at the top of the second fastest oscillation band and alternate comparing the input and output frequency then lowering the output frequency coarse tuning band. Once the VCO frequency has dropped below the input frequency the analog locking mechanism is engaged at the correct coarse tuning level. A flow diagram is

provided in Figure 4.35. The reason for beginning at the higher frequency bands and descending is to minimize the time required for the frequency search. More intelligent search methods, for example a binary search, can easily be adapted to find the correct frequency band.

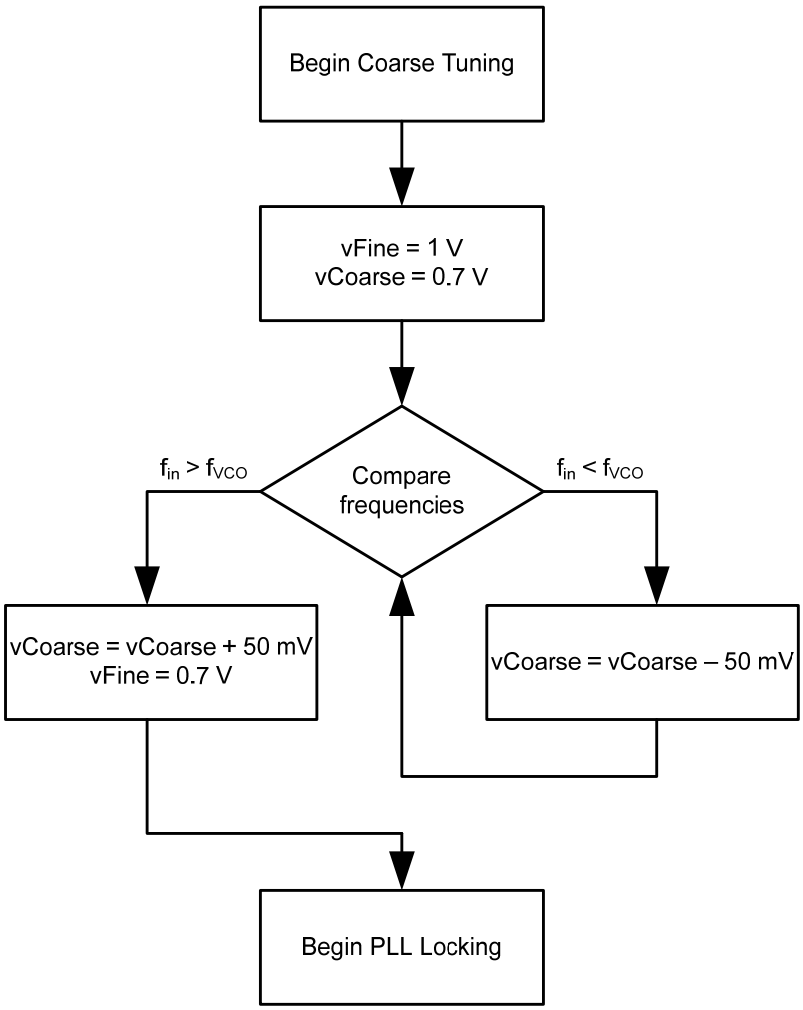



Figure 4.35: Band selection flow diagram

# 5. Experimental Setup and Method

This chapter provides the experimental setup and test procedures for testing both the active-inductor VCO and the PLL. Section 5.1 gives the technique and numerical values to properly characterize the VCO and PLL by de-embedding critical losses. Section 5.2 enumerates the required equipment, as well as test schematics and procedures that are feasible with the available equipment. This section provides the chip pin-out diagram and pin description.

Figure 5.1 is an annotated image of the full-chip layout with net names attached to pins. The input and output signal probes should have bandwidths exceeding 2.5 GHz and 5 GHz respectively. Layouts for individual blocks are provided in Appendix A.

Table 5.1. Fabricated chip pin functions

| Pin Name | Pin Usage |
|---|---|
| CK_in + / - | Differential input clock signal, $V_{CM}$ = 0.6 V, $V_{pp}$ = 400 mV, matched to 50 Ω |
| CK_out + / - | Differential input clock signal, $V_{CM}$ = 600 mV, $V_{pp}$ = 400 mV, matched to 50 Ω |
| VDD12 | 1.2 V supply for phase detector and charge pump |
| VDD_VCO | 1.2 V supply for VCO, VCO buffer, output buffer |
| GND | Ground (0 V) |
| PD_select | Phase-detector select, = 0 V for bang-bang, = 1.2 V for linear |
| vcoarse | Coarse voltage, [0.35 – 1.1] V DC, direct connection |
| vfine | Fine voltage for stand-alone VCO operation, pass-transistor connection[1] |
| vfine_read | PLL loop filter voltage, band limited to approx. 100 MHz |
| vfine_sel_en | Pass transistor control to allow vfine and stand-alone VCO operation |

1. Will not pass full voltage to internal node. See translation in Figure 5.3.

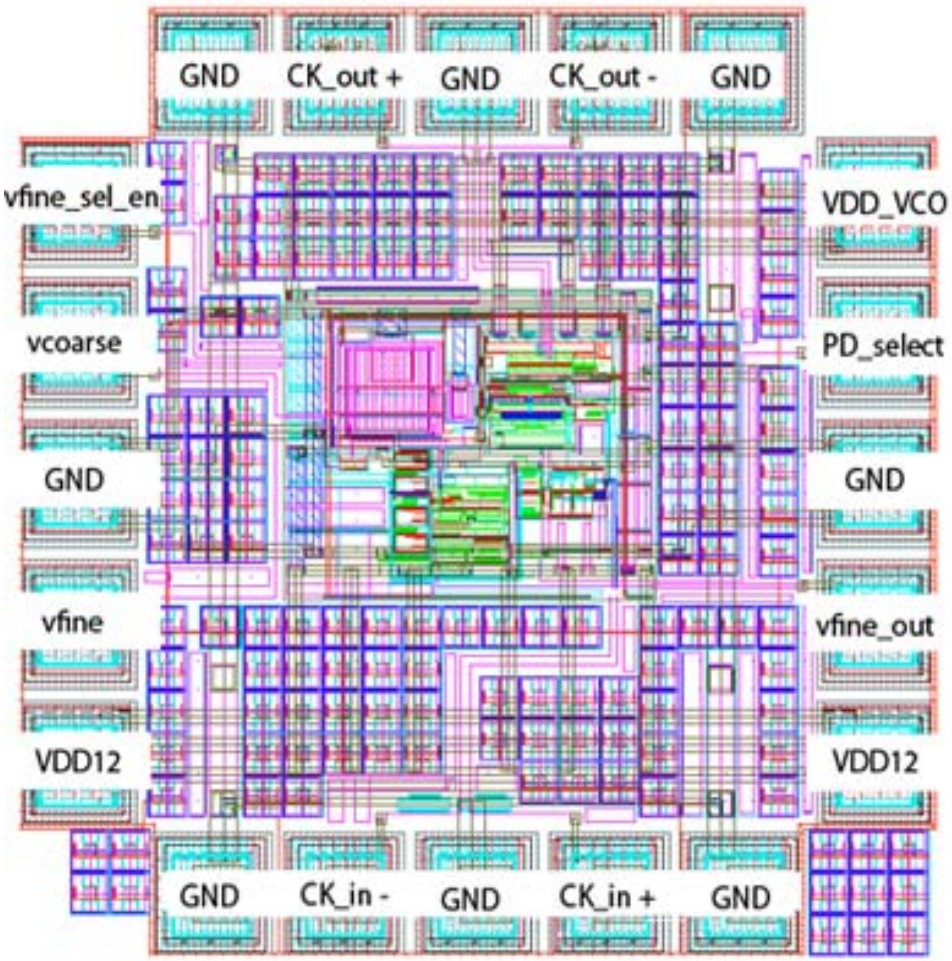



Figure 5.1: Full chip layout with pin labels

To facilitate the interpretation of Table 5.1 a few clarifications are helpful:

First, two power supplies are used. Both are 1.2V supplies: VDD12 for the phase detector and charge pump and VDD_VCO that powers the VCO, VCO buffer and output buffer. This way the VCO can be powered without inducing substrate noise from other on-chip circuitry unnecessary

to test the VCO. Two VDD12 pins are used to minimize the I*R supply voltage drop from the power supply network.

Second, in order to allow both the PLL and an external pin to drive the fine voltage control of the VCO a pass transistor structure is connected to the loop filter output (Figure 5.2). When enabled, the pass transistor will act as a resistor forming an RC network with the loop filter. Transient simulations show that 75 ns is required for the output voltage to settle. Also, the voltage will not be passed at exactly its input level to the internal node. To properly characterize the VCO it is important to use the voltage at the control node, which can be translated from the input voltage using Figure 5.3.

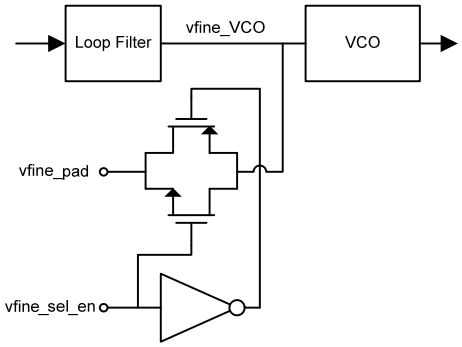



Figure 5.2: Fine control driving circuitry

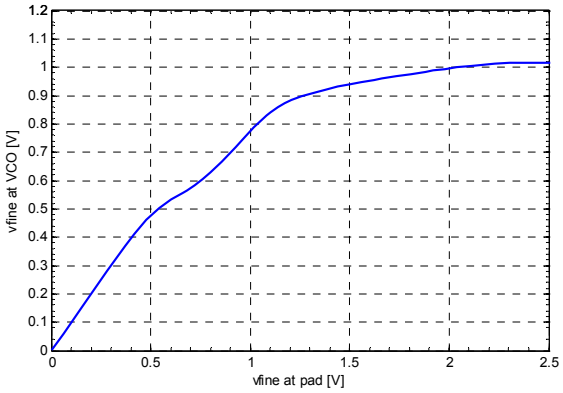



Figure 5.3: *vfine* translation from pad to VCO input

## 5.1. Output Buffer Noise De-Embedding

Measuring the on-chip VCO characteristics is important since it will be that block excluding the output buffer that will drive other on-chip circuitry. Therefore the output buffer must be de-embedded from the VCO measurement. The added noise of the output buffer was simulated and must be subtracted from the output noise. It is plotted in Figure 5.4 up to 10 GHz. Approximating the slope of the sinusoidal output as linear the amount of jitter in seconds induced by the output buffer is equal to the noise of the block in volts divided by the slope of the signal. The RMS noise value for a bandwidth of 10 GHz is 350 nV, which needs to be accounted for in the final jitter measurements.

To correct VCO phase noise measurements, only the noise at 1 MHz from the carrier is considered, since phase noise is reported at 1 MHz from the carrier. The noise voltage added by the buffer can be converted to excess phase noise, denoted as $\mathcal{L}_E$, using (5.1). $V_{pp}$, the magnitude of the VCO output swing, is approximately 400 mV in all cases.

$$\mathcal{L}_E(f) = 20\log\left(\frac{V_{noise}(f)}{V_{pp}}\right) \tag{5.1}$$

The amplification of the buffer will not affect the zero crossings of the output signal relative to the input signal and does not impact output noise.

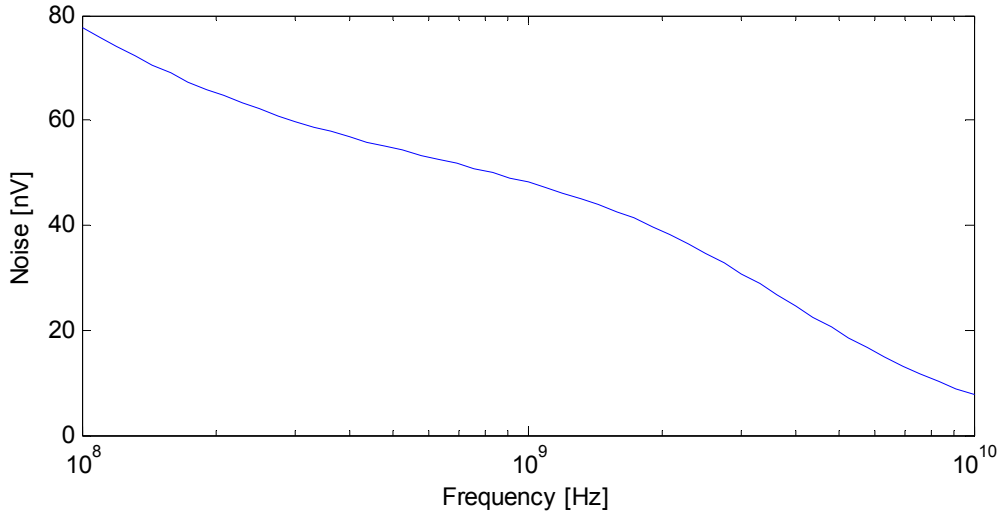



Figure 5.4: Noise added by the output buffer

## 5.2. Experimental Setup, Schematics, and Procedures

This section details the test plan for both VCO and PLL characterization. A list of test equipment required to perform the tests is provided. A list of tests and a quick description of the test methodology follows.

### 5.2.1. Required Equipment

Table 5.2 lists the required equipment necessary for the characterization.

### 5.2.2. VCO Characterization

The testbench schematic for VCO characterization is provided in Figure 5.5. By sweeping $V_F$ and $V_C$ the power consumption is measured via the current draw on the VDD_VCO power supply. The spectrum analyzer will report both the oscillation frequency (carrier frequency) and the

phase noise spectrum/phase noise at 1 MHz offset from the carrier. De-embedding the output buffer noise proceeds as described in 5.1.

Table 5.2: Required equipment list for VCO and PLL characterization

| Qty | Equipment |
|---|---|
| 1 | RF Probe station |
| 1 | GSGSG 2.5 GHz signal probe |
| 1 | GSGSG 5 GHz signal probe |
| 2 | PSGSP DC probes |
| 2 | 2.5 GHz bias-T's |
| 1 | 2.5 GHz differential signal source (eg: Anritsu MP1793B) |
| 1 | 10 GHz spectrum analyzer with phase noise profile (eg: Agilent PSA series) |
| 1 | 10 GHz oscilloscope with 50Ω termination |
| 1 | Low-frequency (eg. 1MHz) oscilloscope with high-impedance termination |
| 6 | 10 GHz cables |
| 2 | Low-frequency cables |
| 6 | DC power supplies |

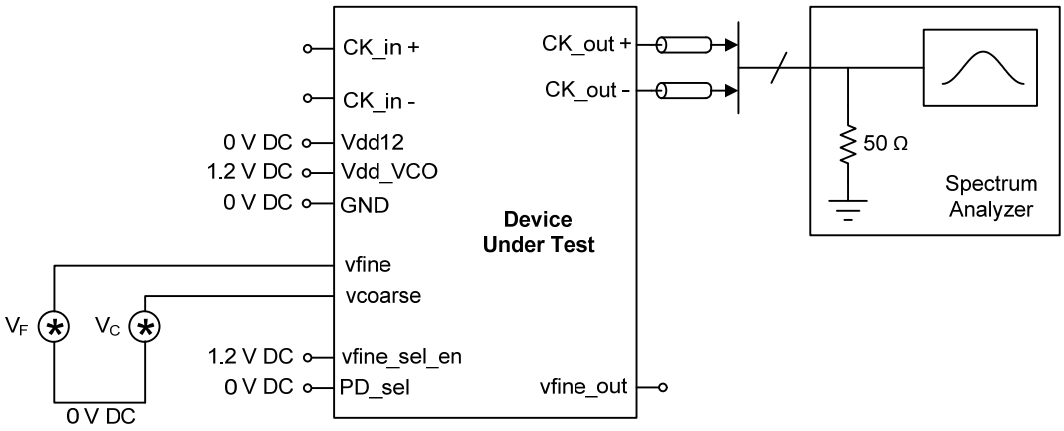



Figure 5.5: VCO characterization setup

### 5.2.3. PLL Characterization

Confirming the locking range using the bang-bang phase detector is the first test to ensure the functionality of the PLL and is accomplished in two steps. The first is to make sure that the PLL will follow the input clock across the frequencies of interest, and second is to test that the PLL will lock across the fine-tuning range after a frequency step at the input. The PLL characterization testbench setup is shown in Figure 5.6. For all bang-bang phase detector tests the *PD_sel* signal should be tied to 0 V DC.

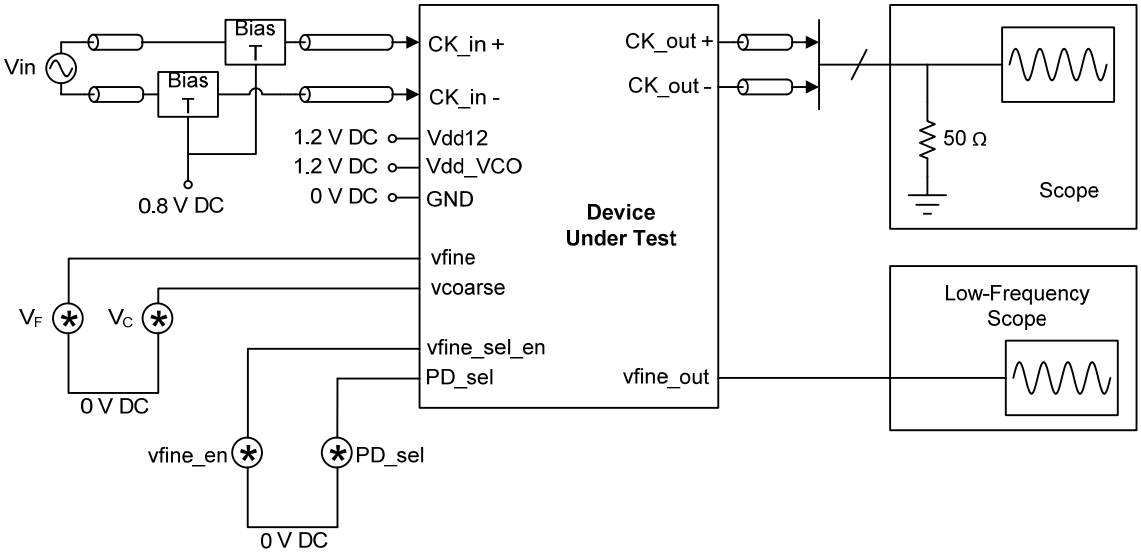



Figure 5.6: PLL characterization setup

For all the discussed experiments, if the lab equipment has the feature, it can be triggered to begin recording on *vfine_en*'s falling edge, when the charge pump is engaged, and used to monitor the loop response. This can be used to measure the time required to achieve PLL lock.

To ensure the PLL follows the input clock across the VCO tuning range and measure locked jitter the following process is followed with both the linear and bang-bang PD enabled, through the use of PD_sel:

1. $V_C$, the coarse tuning voltage, is set first to the lowest voltage
2. $V_F$ is set to 0.7 V, the mid-band voltage, and *vfine_en* is connected to 1.2 V
3. The frequency of $V_{in}$ is set equal to the output clock frequency
4. *vfine_en* is changed to 0 V
5. The frequency of $V_{in}$ is swept and $V_{out}$ is monitored to ensure that the output frequency follows the input frequency.

6. The loop filter output is available through *vfine_out*, and jitter can be recorded by monitoring $V_{out}$
7. Steps 1-6 are repeated for the other frequency bands by increasing $V_C$

Once the PLL is locked the jitter is measured using eye diagram functionality on the oscilloscope. The input frequency and $V_C$ should be swept to find the worse-case jitter across all frequency bands. Bang-bang PD locking jitter is tested with *PD_sel* set to 1.2 V DC. Linear PD locking jitter is tested with *PD_sel* at 0 V DC.

Testing that the linear phase detector can lock after the bang-bang PLL has settled is accomplished using the same methodology listed above, and switching PD_sel from 1.2 V to 0 V after the bang-bang PD has locked and monitoring the output frequency of the VCO. The average output frequency should remain constant and the jitter of the output clock should drop when the linear PD locks.

The procedure to confirm the locking range allowing the PLL to lock to the input clock after input frequency jumps, or to set known initial conditions to test phase locking, is as follows:

1. $V_F$ and $V_C$ are set to generate the desired output frequency while *vfine_en* is set to 1.2 V DC.
2. The input clock is then adjusted to the desired frequency.
3. *vfine_en* is set to 0 V DC to allow the PLL loop lock to the input frequency. The VCO control voltage can be observed via *vfine_out*.

# 6. Experimental Results

This chapter covers the measured results and analysis of the VCO and PLL from the laboratory setting, using the equipment and setup described in Chapter 5.

A micrograph of the fabricated chip, of the same orientation as the annotated Figure 5.1 can be found in Figure 6.1.

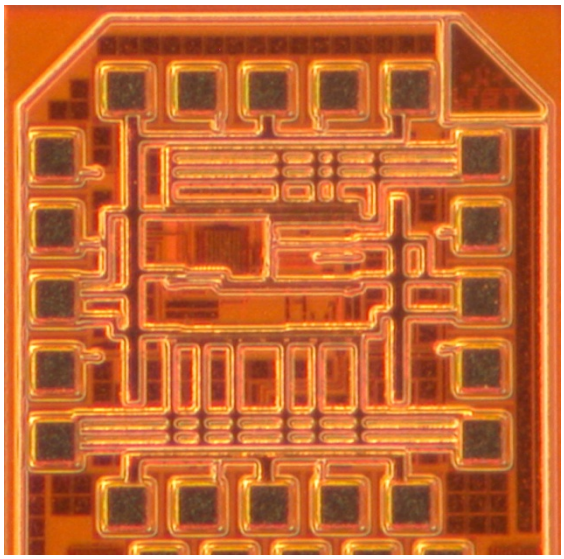


Figure 6.1: Chip micrograph

## 6.1. VCO

The measured VCO tuning characteristic is given in Figure 6.2. The fine-tuning voltage is limited to the same range as was used in simulations. The coarse tuning voltage upper limit is the maximum voltage where the VCO maintains oscillation at a 1 V fine tuning characteristic. The

minimum coarse tuning voltage reported is chosen such that the VCO range encompasses approximately 4.25 GHz. The maximum oscillation speed is 4.4 GHz.

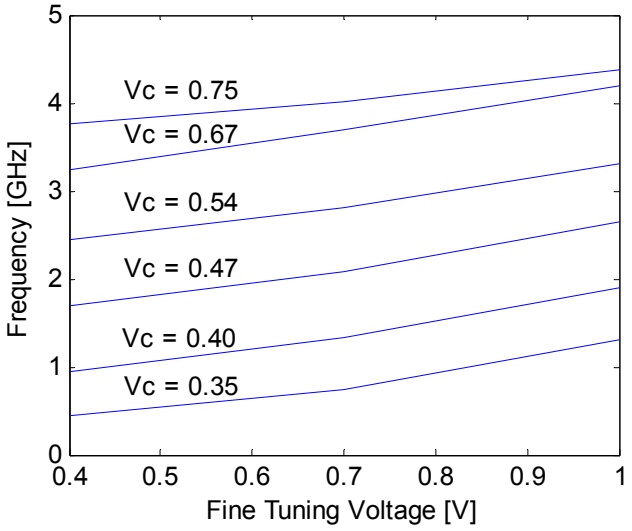



Figure 6.2: Measured VCO tuning characteristic

The tuning characteristic is very similar to the simulated slow-slow PVT corner with extracted layout parasitics. However, this characteristic was measured across multiple dice. By including extra parasitic capacitances on the schematic it is also possible to achieve a similar tuning characteristic. Therefore, it is likely that some of the metal fill and routing added to the design around the VCO impacted the parasitic-sensitive design. Also, while the simulated extracted layout should not have ignored any critical capacitances and resistances in the design itself it does not extract substrate resistances and its associated noise which may also have impacted the design.

The measured coarse $K_{VCO}$ is 8.3 GHz/V. The measured fine $K_{VCO}$ are listed in Table 6.1. The measured variance of the fine tuning is now 21.5% from the nominal 1.3 GHz/V. Eliminating the top coarse band reduces the maximum frequency by 190 MHz, but also reduces the total difference in fine $K_{VCO}$ to 10%. The low and mid-band fine $K_{VCO}$ are similar to the simulated

results of 1.45 GHz/V. The saturating of the VCO oscillation and significant reduction of $K_{VCO}$ at the high coarse tuning voltages is also observed in simulation when the oscillator operates with coarse tuning voltages greater than 0.75 V and the source follower transconductance loses its ability to modulate the output frequency.

Table 6.1: Fine KVCO versus coarse band tuning

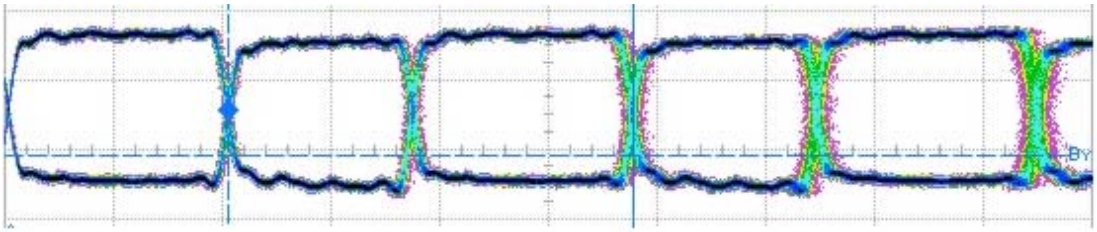
| Coarse band [V] | $K_{VCO}$ [GHz/V] |
|---|---|
| 0.35 | 1.43 |
| 0.4 | 1.58 |
| 0.47 | 1.57 |
| 0.54 | 1.43 |
| 0.67 | 1.58 |
| 0.75 | 1.02 |

The single-ended peak-to-peak output voltages are slightly lower than expected, since the output buffer is not saturated for all the VCO output frequencies. The output magnitudes measured at the oscilloscope are given in Table 6.2. Transient plots of the measured VCO waveforms can be found in Figure 6.3.

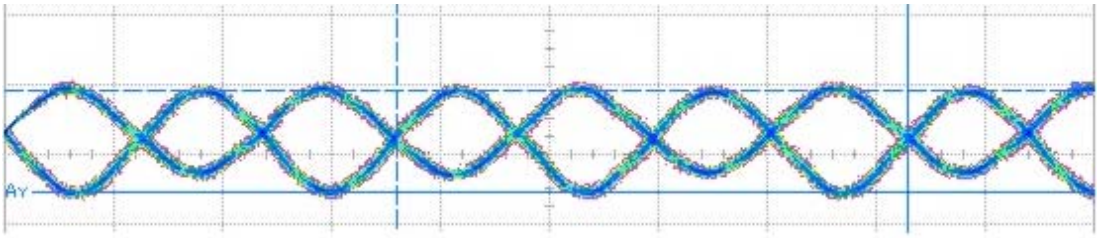
Table 6.2: Measured VCO single ended output magnitude

| Vcoarse | $V_{fine}$ = 0.4 V | $V_{fine}$ = 0.4 V | $V_{fine}$ = 0.4 V |
|---|---|---|---|
| 400 | 468 | 450 | 430 |
| 470 | 468 | 434 | 430 |
| 540 | 468 | 434 | 428 |
| 670 | 430 | 400 | 360 |
| 750 | 410 | 388 | 280 |

* All units in mV



a. 0.5 GHz clock



b. 4.25 GHz clock

Figure 6.3: Transient VCO waveforms

Table 6.3: Measured VCO phase noise

| Frequency [GHz] | Phase noise [dBc/Hz] |
|---|---|
| 0.5 | -67.6 |
| 1 | -69.0 |
| 1.5 | -75.4 |
| 2 | -69.2 |
| 2.5 | -70.9 |
| 3 | -70.3 |
| 3.5 | -73.8 |
| 4 | -74.0 |
| 4.5 | -71.7 |

Assuming that the extracted CML gains are accurate the measured output VCO buffer amplitudes drop to 56 mV. Using this amplitude to drive digital circuits would require very accurate common-mode voltages and sensitive digital circuits. The 112 mV differential voltage is able to drive CML circuits, but will not fully switch the circuits degrading performance.

The phase noise measurements for the VCO are given in Table 6.3. The phase noise trends slightly downwards with increased frequency, as observed in simulations. The absolute phase noise values are approximately +10 dBc/Hz worse at a 1 MHz offset when compared to the simulated results. Some of this can be attributed to unaccounted substrate effects on active circuits during this measurement.

## 6.2. PLL

The PLL tested following the method described in Section 5.2.3, first for the bang-bang PFD driven PLL, then by the linear PD driven PLL. The PLL is able to lock using both the bang-bang PFD and linear PD across the VCO tuning range.

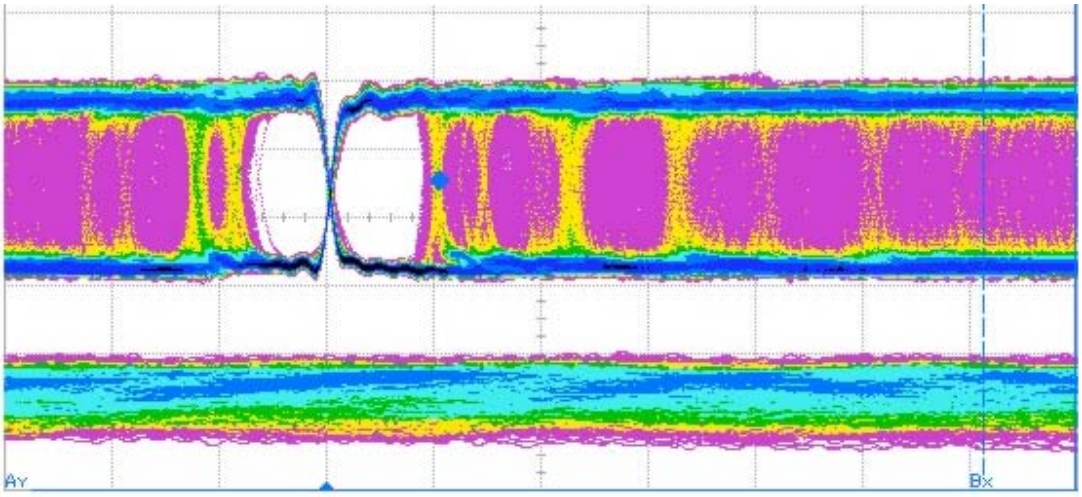
Table 6.4: Recovered clock jitter

| Frequency [GHz] | Bang-bang PFD | | Linear PD | |
|---|---|---|---|---|
| | Peak-to-peak [ps] | RMS [ps] | Peak-to-peak [ps] | RMS [ps] |
| 0.5 | --* | -- | 338 | 54.7 |
| 1 | --* | -- | 36 | 5.8 |
| 2 | --* | -- | 13.5 | 2.2 |
| 3 | 45 | 7.3 | 11.7 | 1.9 |
| 4 | 18 | 2.9 | 8.25 | 1.3 |

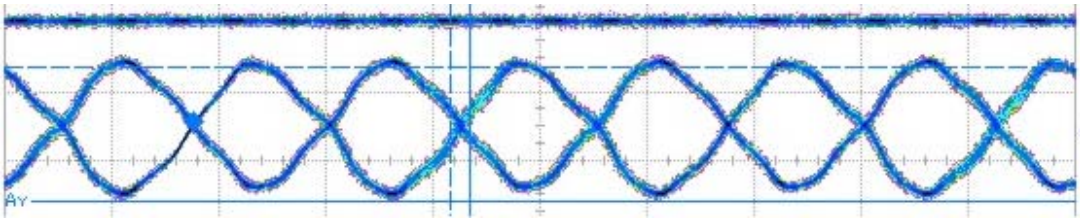
* Recovered eye is closed

The peak-to-peak jitter exhibited by the bang-bang PFD is larger than expected. Jitter results for various locking frequencies are provided in Table 6.4. The trends match those from the simulated results. The bang-bang driven PLL loop provides reasonable jitter characteristics at high frequencies, but locks with excessive jitter resulting in closed eyes in the recovered clock at lower frequencies. The bang-bang PFD exhibits higher jitter than the linear phase detector

across all frequency bands, as expected. The linear PD PLL loop results in approximately 8.25 ps of peak jitter regardless of the operating frequency, except at very low frequencies, where the jitter on the recovered clock jumps.




a. 0.5 GHz lock




b. 4 GHz lock

Figure 6.4: Bang-bang PFD PLL lock waveforms

The measured locked peak-to-peak range of the bang-bang PLL fine tuning voltage drops from approximately 200 mV at low frequency to 50 mV at high frequencies. Combining these results with the measured fine $K_{VCO}$ the output clock frequency is calculated to vary by 290 MHz at frequencies 1 GHz and below and as little as 72 MHz at VCO clock frequencies of 4 GHz and higher. Oscilloscope screen captures of the locked bang-bang PLL at 0.5 GHz and 4 GHz are

provided in Figure 6.4 where the locked jitter and noise on the VCO control line can be observed.

The control mechanism switching between the two phase detectors is not buffered from the input. Since it is connected to a manually varied DC voltage supply the switch is slow and near $V_{dd}/2$ both phase detectors are partially connected to the output through the CML MUX and both phase detectors attempt to drive the loop. This has the observed effect of reducing the pull-in range of the linear PD, and at locked VCO frequencies of 1 GHz and lower switching between the bang-bang PFD and linear PD was unreliable. Two digital inverters on the control signal for the fine-control access switch sharpen the driving edge sufficiently to quickly switch between manual and PLL control of the VCO and it is likely a solution to the manual control of the bang-bang/linear PD select.

The linear PD driven PLL jitter increases at frequencies under 1 GHz, as shown in Figure 6.5. The VCO control voltage exhibits an unexpected sinusoidal form at the input clock frequency. It is possible that the CML circuits are not completely switching or there is significant substrate coupling allowing for significant input feed-through.

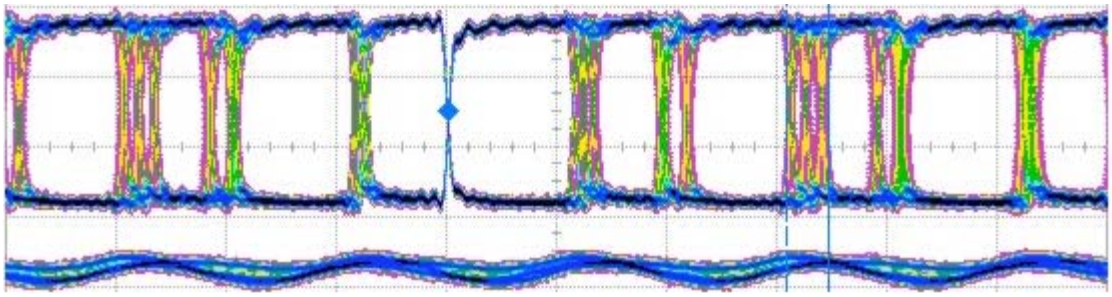


Figure 6.5: 0.5 GHz linear PD lock waveform

# 7. Conclusions

## 7.1. Design Conclusion

This dissertation presents the complete design of a wideband active-inductor-based VCO and a dual-tuned control scheme and an offset-compensated wide-tracking charge-pump PLL that allows frequency and phase locking to signals between 0.5 and 5 GHz.

The PLL and oscillator were fabricated in 0.13 µm CMOS. The VCO consumes only $50 \times 60$ µm$^2$, which would fit within the area required for a single monolithic inductor designed to operate at 5 GHz. The complete PLL including the oscillator and output buffer occupies $275 \times 200$ µm$^2$.

The post-layout-extracted and simulated active-inductor-based VCO oscillates from 500 MHz to 5 GHz and exhibits a consistent fine $K_{VCO}$ of 1.48 GHz/V with a maximum ±5 % deviation across the tuning range. The VCO has overlapping coarse tuning bands using 50 mV coarse tuning levels, and an overall tuning range of 480 MHz to 5.1 GHz. The coarse $K_{VCO}$ is 12.8 GHz/V. The worst-case phase noise is -78 dBc/Hz at 1 MHz frequency offset which improves to –81 dBc/Hz at 5 GHz. The minimum and maximum single-ended output amplitudes are 200 mV and 600 mV, respectively. The VCO consumes between 18 and 36 mW.

The measured VCO consumes the same power, and operates between 250 MHz and 4.4 GHz. It exhibits a phase noise at 1 MHz offset between –67.6 dBc/Hz at 0.5 GHz and –75.4 dBc/Hz at 1.5 GHz. The general trend of the phase noise matches simulations. The coarse measured $K_{VCO}$ is 8.3 GHz/V, and the drop is attributed to the lower 4.4 GHz maximum frequency. The fine $K_{VCO,}$ excluding the highest band is 1.5 ±5%. Including the highest frequency band it is 1.3 GHz/V ±22%.

The wide-tracking charge pump PLL includes a hybrid PFD for fast phase acquisition and low locked jitter. It achieves low-offset locking across the overall 4.5 GHz lock range using charge-pump compensation circuitry that improves the linear locking offset from over 50° to less than 5° by splitting the tuning range into five sections. The phase compensation circuitry is the only wideband specific circuitry and is disabled for the bang-bang PFD locking. The PLL incorporates CML circuitry to reduce noise injection into the VCO.

The simulated PLL results in less than 4 % of a clock period of peak-to-peak jitter using the linear PD over the entire frequency range. The bang-bang driven loop locks across the frequency range but can exhibit a maximum eye opening of only 25% when locked at low frequencies. The PLL power, excluding the VCO, is 22 mW. It exhibits long locking times due to large loop delay impacting the negative feedback dynamics.

The measured PLL provides a lock with approximately 3 % of a clock period of peak-to-peak output jitter and 0.5 % of the clock period in RMS clock jitter for clock speeds of 1 GHz and beyond. The bang-bang PLL locks across the entire VCO band but exhibits closed eyes for VCOs frequencies less than 2.5 GHz. The PLL consumes 20 mW from a 1.2 V supply.

Table 7.1: PLL comparison with published works

| Reference | This work | [55] | [56] | [57] | [58] | [59] |
|---|---|---|---|---|---|---|
| Process [nm] | 130 | 130 | 350 | 350 SiGe | 120 | 45 |
| Freq [GHz] | 0.25 – 4.5 | 1 – 3 | 4kHz – 1.1 | 0.4 – 2.15 | 2.5 – 3.11 | .01 – 5 |
| Jitter [$ps_{rms}$] | 1.3 | 0.4 | 1.26 | 1.29 | 0.86 | 0.5 * |
| Area [$mm^2$] | 0.07 | 0.07 | 0.12 | 1.25 | 0.7 | 2 |
| Power [mW] | 48 | 23 | 28 | 60 | 35 | 115 |

* Not directly reported. Calculated using (10) from [60].

Table 7.1 provides context for the PLL measurement results and comparison with recent related work. As can be seen from the table, the AI-VCO-based PLL solution performance compares

favorably with state-of-the-art wideband PLL structures, in particular, in area and power. The 350 nm solution, [56], uses a 3-stage ring oscillator and will be limited to approximately 3 GHz in a 130 nm process. The relatively larger jitter observed in this work, as discussed, is attributed to both the active-inductors used in the LC-VCO and the excess loop delay increasing the locked jitter.

## 7.2. Future Work

In order to present the system as a ready-to-implement solution for a multi-standard PLL for wireline communication applications there needs to be a few changes and improvements to the design.

First, the design must implement an automatic band selection mechanism, either using a digital implementation, as described in Section 4.6 or an analog solution, e.g., a second PLL loop.

Second, the noise figure of the VCO and output jitter of the PLL needs to be improved in order to meet jitter requirements if the PLL is going to be used in a transmitter or as a transmit clock. This means a complete overhaul of the VCO solution, or implementing the VCO in a faster process. A faster process would increase the operating frequencies of the active inductor and VCO, allowing the design to trade off oscillation frequency for phase noise. Making this more difficult is the fact that the VCO should also be redesigned to increase its driving capability in order to eliminate the VCO buffer. Another option for improving the quality factor of the active inductor, and hence phase noise of the VCO, is to attempt incorporating a gate resistor on the internal inductor node. This improvement in phase noise will need to be balanced against the increased input-referred inductor noise induced by the second resistor.

To match state-of-the-art PLL implementations the locking and locked dynamics of the PLL need to be improved. The linear locked jitter is good, but requires a two-stage locking process – one for the bang-bang PD and one for the linear PD. This increases the total locking time. The VCO redesign with an emphasis on removing the VCO output buffer would also help reduce locking time by eliminating the excess loop delay that impacts the validity of the $2^{nd}$-order system implemented in the design process. Examining the PLL loop and its delay using a hybrid digital/analog rapid simulation tool, like Verilog-AMS, may also help solve the excess hunting jitter exhibited by the bang-bang PD loop.

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# Appendix

## Appendix A: Circuit Block Layouts

This appendix provides layout images for all of the circuit blocks which can be compared to the schematics in the appropriate section. The system-level layout can be found below. The layouts of the PLL blocks are subsequently presented.

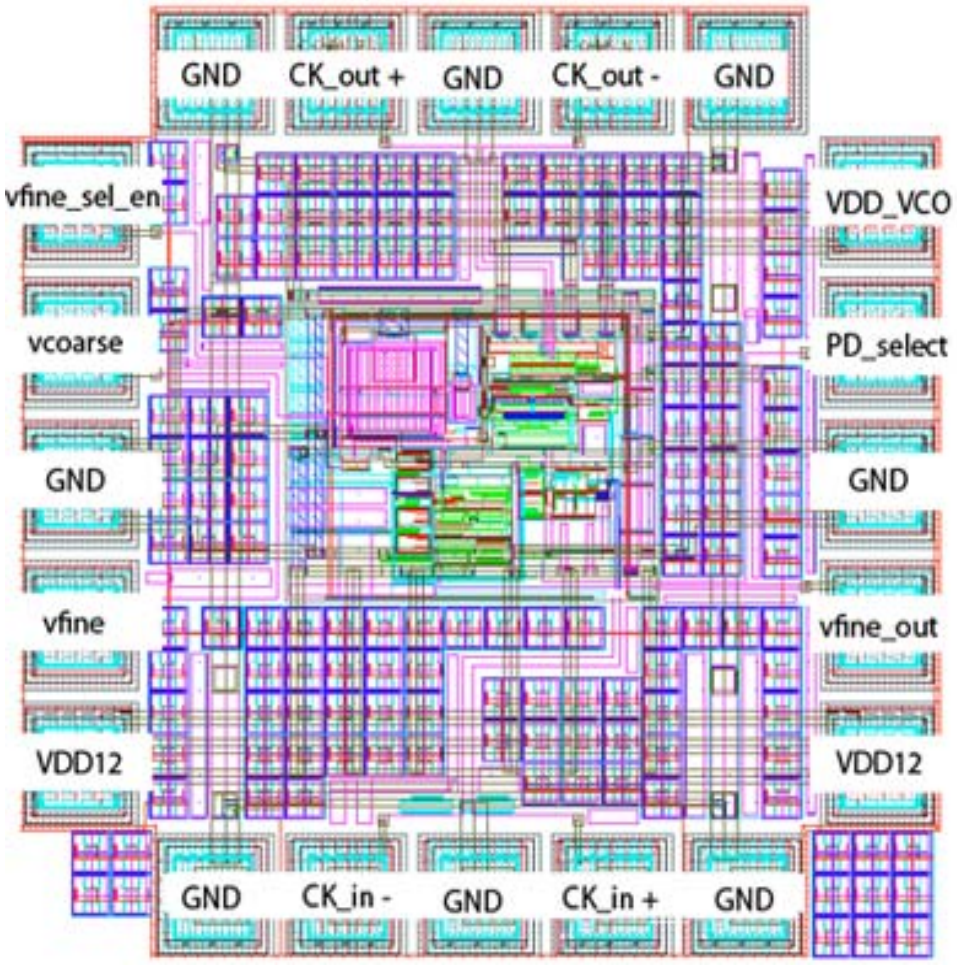


Figure A.1: Full chip layout with pin labels

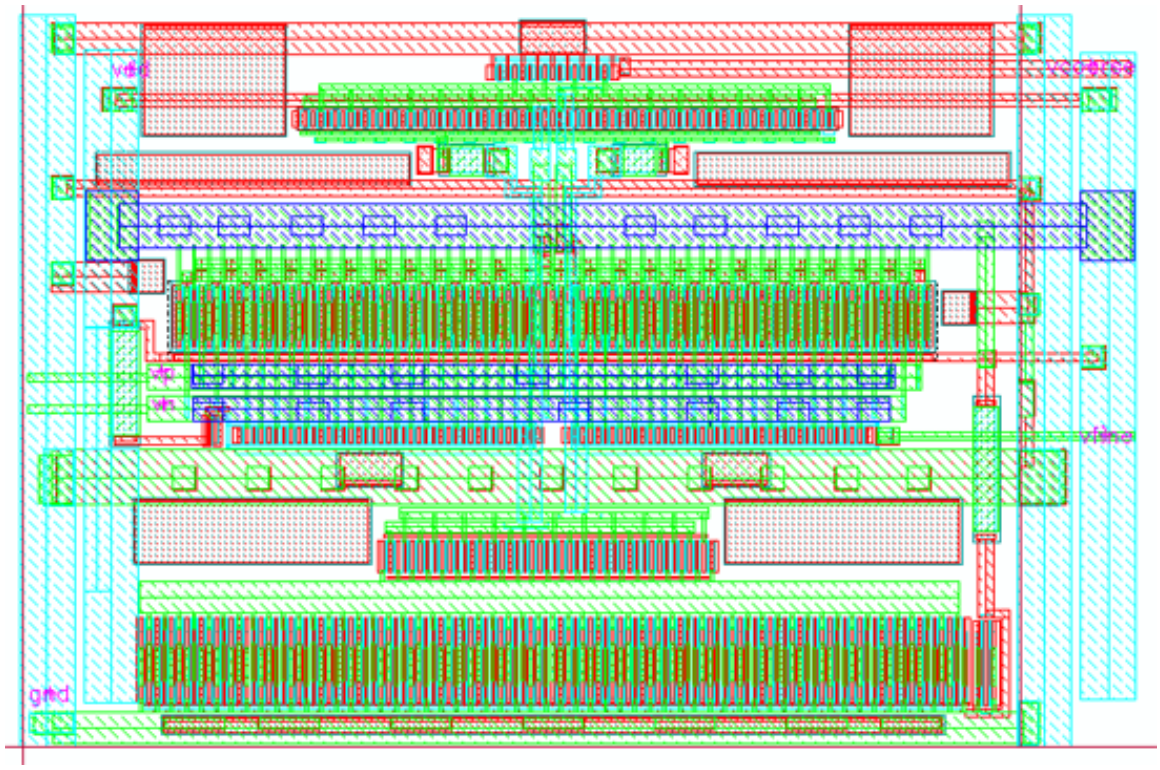


Figure A.2: Layout of the AI-VCO, area extents: 60 x 50 µm$^2$

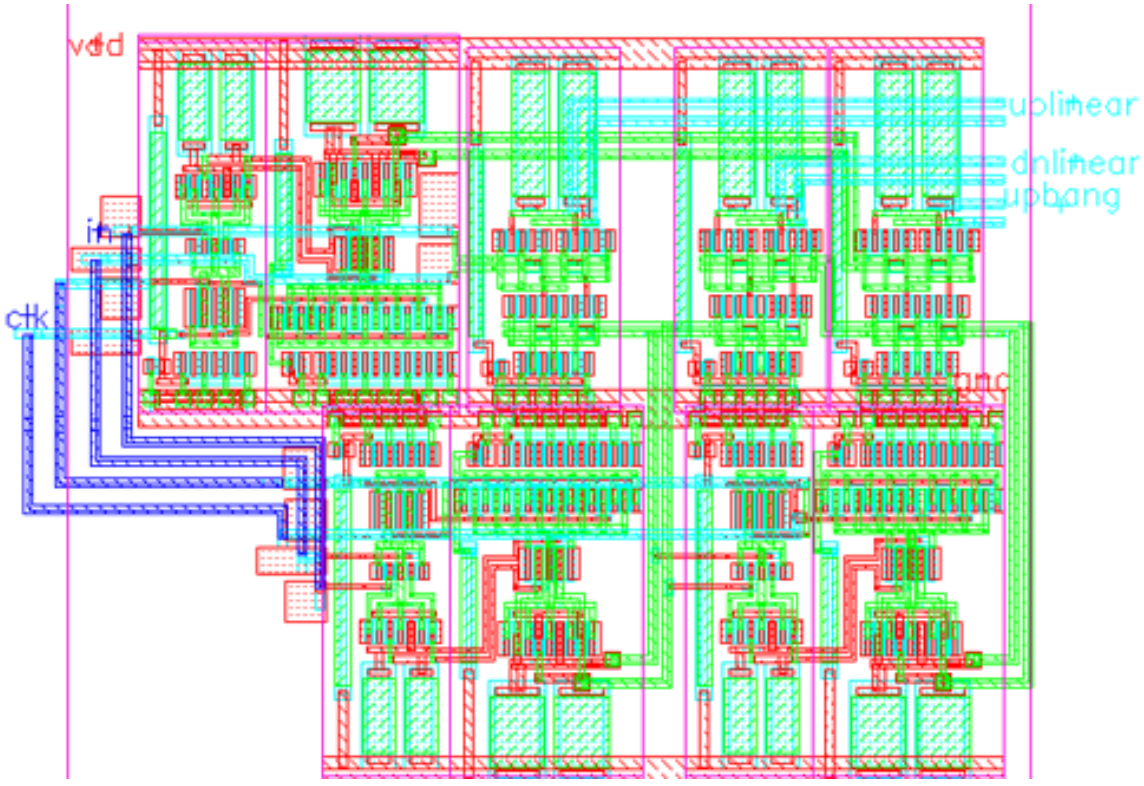


Figure A.3: Layout of the PFD and MUX, area extents: 40 x 33 µm$^2$

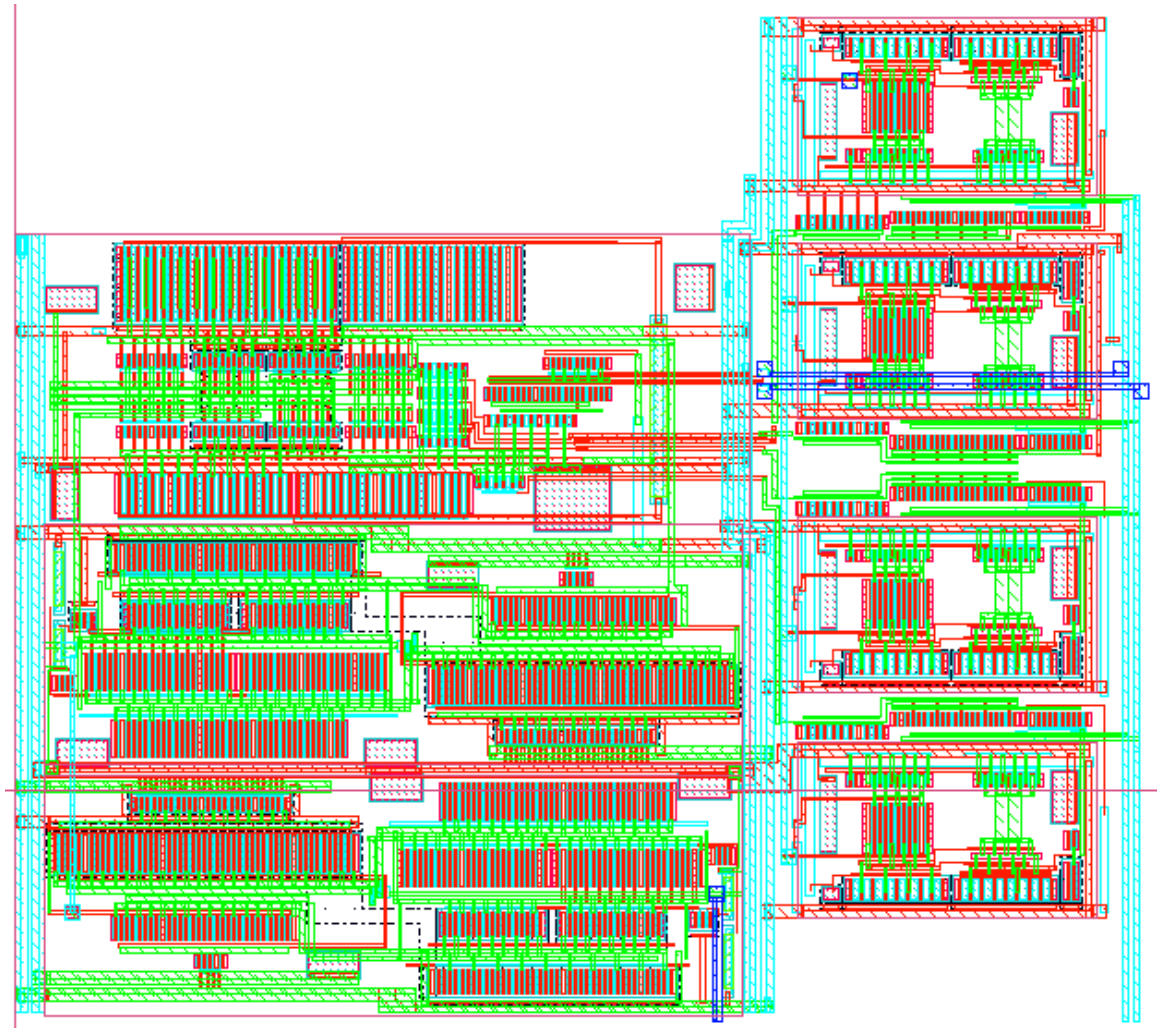

Figure A.4: Layout of the compensated charge pump, area extents: 90 x 80 $\mu m^2$

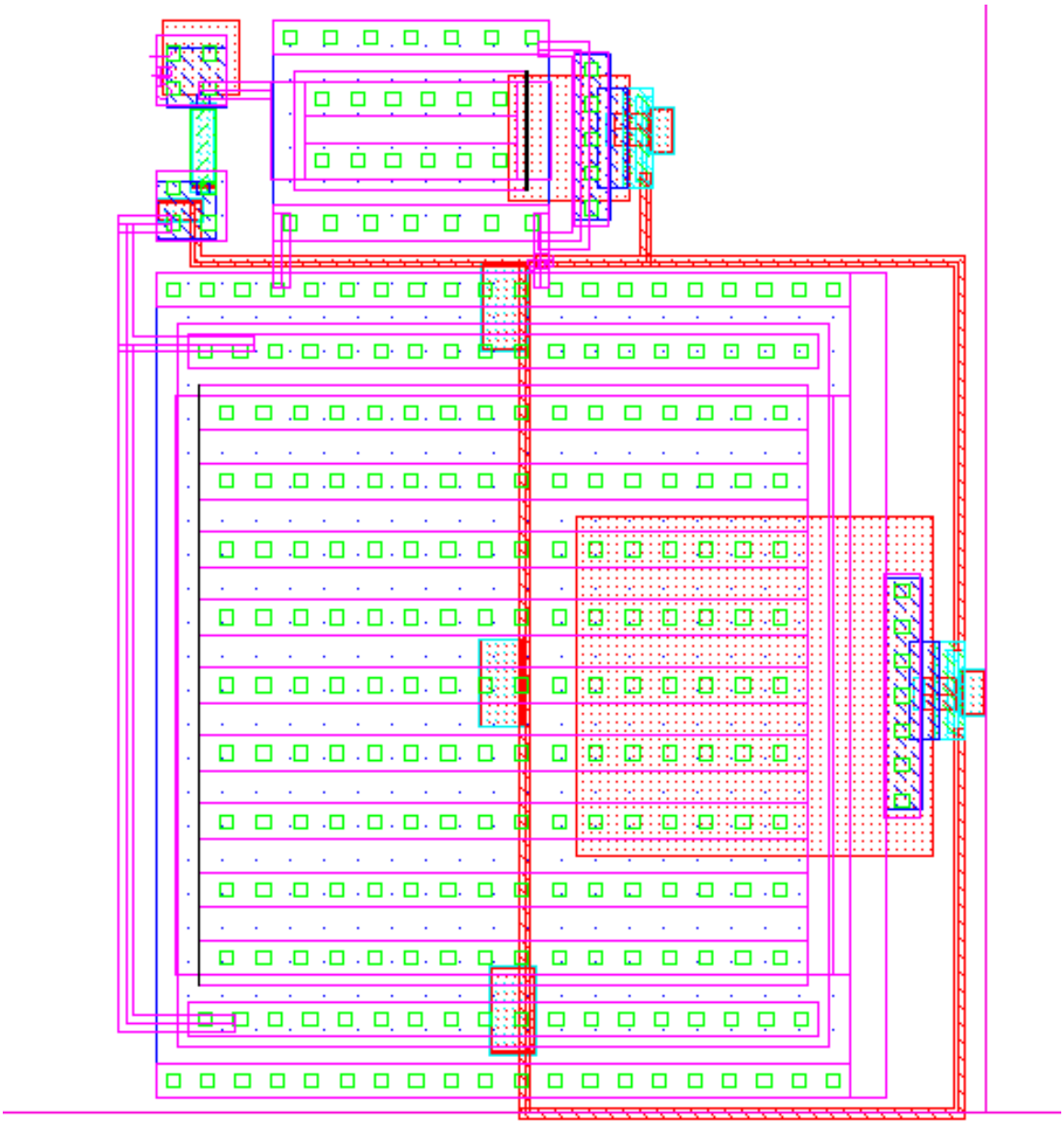

Figure A.5: Layout of the loop filter, area extents: 85 x 105 $\mu m^2$

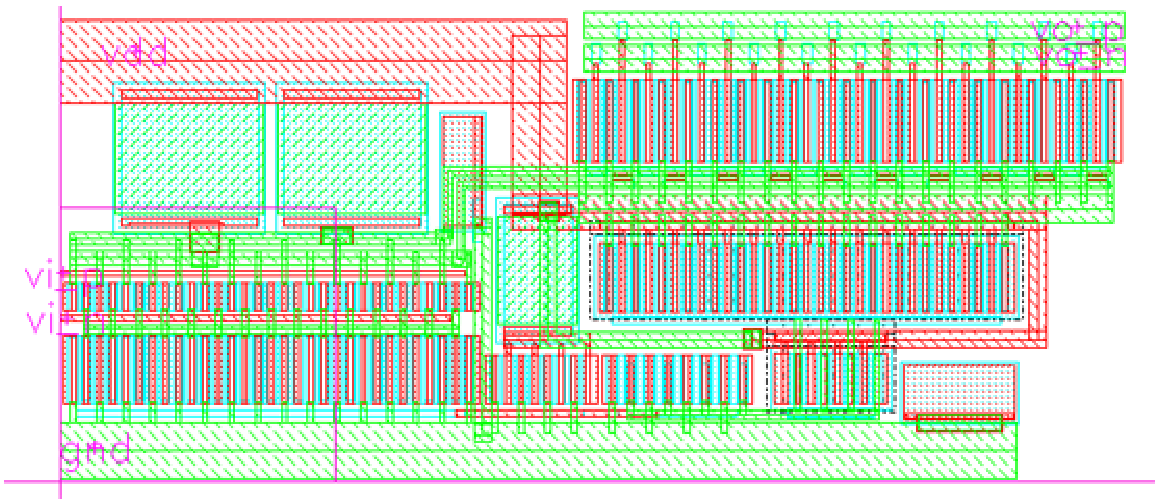


Figure A.6: Layout of the output buffer, area extents: 40 x 20 µm$^2$

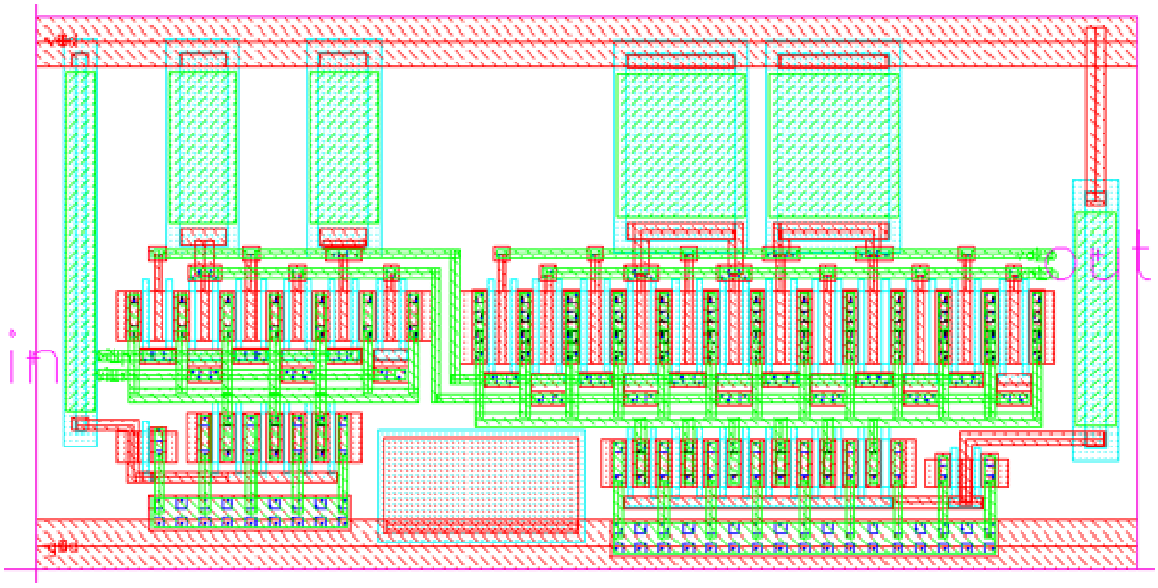


Figure A.7: Layout of the VCO buffer, area extents: 25 x 15 µm$^2$