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Design of Low Drop-Out voltage regulator

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An essential component of today's battery powered SoC's are power management systems which include Low Drop-Out (LDO) voltage regulators. LDO voltage regulators improve battery's power efficiency and life. In this paper design and analysis of an LDO voltage regulator is presented. The designed LDO voltage regulator is designed with self-compensated error amplifier. It provides 30mA load current with a stable 1.6V output voltage. It consumes 172μA quiescent current and has a power efficiency of 88.38 % with dropout voltage of 200mV.

Keywords: Analog circuits, error amplifier, dc-dc regulators and LDO.

Introduction

DC to DC converters are important in portable electronic devices such as cellular phones and laptop computers, which are supplied with power from batteries primarily. LDO voltage regulators are a class of linear regulators widely used in the industry.A series low-drop-out regulator is a circuit that provides a stable dc voltage whose input to output difference voltage is low. The drop-out voltage is defined as the input to output difference voltage where the control loop stops regulating. The operation of the circuit is based on feeding back an amplified error signal used to control the output current flow of the pass transistor driving the load[1,2].The section 2 explains the architecture of the proposed LDO voltage regulator, section 3 describes the operation of LDO voltage regulator. The simulation results are discussed in section 4.

LDO voltage regulator architecture

The designed LDO voltage regulator consists of an error amplifier, a pass transistor, and a feedback network to regulate the output voltage to a constant voltage. Design parameters of LDO given in Table 1. Fig. 1 shows the block diagram of a typical LDO voltage regulator[3] where 'vref' is the reference voltage, 'vin' is the input voltage and 'vout' is the regulated output voltage. The PMOS pass transistor is indicated by 'Mp' with its substrate connected to 'Vin'. The Error amplifier is denoted by 'Erroramp' with 'Vref' and 'Vfb' as its inputs. 'Rf1' and 'Rf2' resistors form the feedback network. The output node is connected to a load resistor 'Rl', a load capacitor 'Cl' and an electrical series resistance (ESR) of capacitor 'R_{ESR}'. The individual blocks are explained below

Error amplifier

The error amplifier designed for this LDO is a two stage differential input single ended output amplifier. The schematic of the designed error amplifier is shown in Fig. 2. The figure consists of start-up circuit, bias generation circuit and amplifier circuit.The start-up circuit (shown in dotted box) is designed for the proper working of the bias and amplifier circuits by ensuring all the transistors are in saturation[4]. It sets the operating points of the bias circuit transistors for stable bias voltage generation. The bias circuit used consists of a self biased current reference designed for 50μA reference current with 5 kΩ resistor as shown in Fig.2. The bias voltage generated keeps the common

Table 1 – Design parameters of LDO.

Parameter	Value
Supply voltage	1.8 +/- 10% V
Output voltage	1.6 V
Load current	30 mA
Load capacitor	4.7uF
Technology	TSMC 90nm
Pass transistor	PMOS (W = 30um, L=200nm)
Feedback resistors	Rf1 = Rf2 = 100 kΩ
Load resistor	Rl = 5 kΩ (no load) to 54 Ω (full load)
Load Regulation	5 mV/A
Transient peak(mV)	< 0.20

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mode tail transistor in saturation.The amplifier first stage uses NMOS transistors as input pair and PMOS, NMOS transistors as diode connected loads[5]. The aspect ratios of transistors are designed to obtain the first stage gain of 42 dB. The second stage of the amplifier is a simple common source amplifier with NMOS active load. The bias voltage for second stage is derived from the other end output of the first stage as shown in Fig.2. The transistor sizes are designed to obtain second stage gain of 32 dB. The error amplifier is compensated using 'self-compensated' technique with 14 pF output capacitor (Cl) to get an overall gain of 84 dB at 2 MHz Unity Gain Bandwidth (UGB).

Pass transistor

$$V_{dropout} \approx 200mV \Rightarrow V_{DSSATPass} \leq 200mV \quad \ldots (1)$$

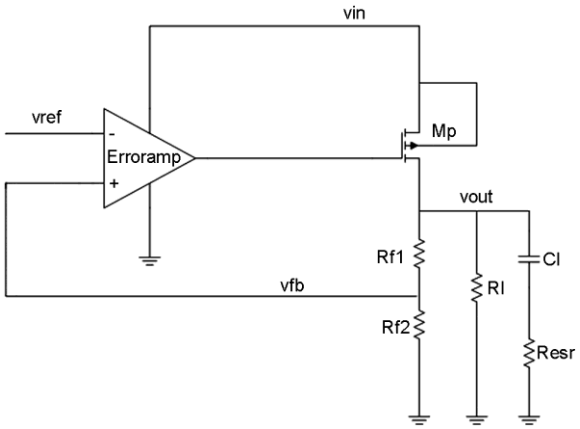

Fig. 1 – LDO voltage regulator[3]

$$\left(\frac{W}{L}\right) = \frac{2I_D}{\mu_p C_{ox} \cdot (V_{DSSATPass})^2} \quad \ldots (2)$$

$$V_{OUT} = \left(1 + \frac{R_{f2}}{R_{f1}}\right) \cdot V_{REF} \quad \ldots (3)$$

The selection of pass transistor depends on the drop-out voltage. Since for our design the required drop-out voltage is less (200 mV), PMOS (depicted as Mp in Fig.1) pass transistor is used. The aspect ratio along with the required multiplier counts is designed using equations (1) and (2) to carry a full load current of 30 mA.

Feedback network

This feedback network consists of two resistors 'R_{f1}' and 'R_{f2}' connected in series. The values of R_{f1} and R_{f2} are calculated as 100 kΩ using equation (3). The output voltage is fed-back to error amplifier's positive input using feedback network as shown in Fig.2.

LDO Voltage Regulator operation

Initially at no-load (320 uA), the LDO voltage regulator's 'V_{OUT}' node is connected to 5 kΩ load resistor. The no-load resistance is calculated, such that all the transistors are operating in saturation. The voltage drop across 'R_{f2}' is fed back to error amplifier's positive terminal as shown in Fig.2. This adjusts the gate voltage of pass transistor (Mp) to keep it in linear region. As the load increases (320 uA to 30mA) i.e., the load resistor decreases from 5 kΩ to 54 Ω, the feedback voltage varies. Due to this, the

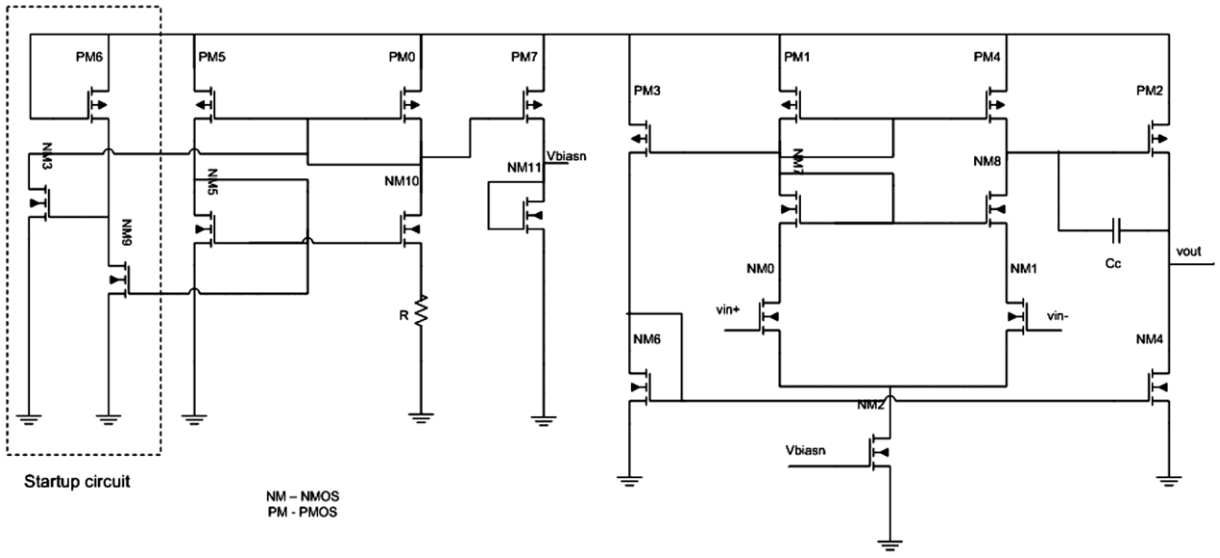

Fig. 2 – Error amplifier

gate voltage of the pass transistor is changed accordingly to keep it in linear region. The resistor divider, error amplifier, and pass element of the PMOS pass transistor regulator form a closed loop. The simulations show that the system is stable with a single pole within the Unity Gain Bandwidth (UGB) 1.75 MHz with the load capacitor Cl (14 pF), ESR resistance (5 Ω) and DC gain of 94 dB.

Simulation details and results

The designed LDO voltage regulator is simulated with 90nm TSMC CMOS technology in CADENCE ADE tool. The feedback resistors R_{f1} and R_{f2} are 100 kΩ each. The input voltage is 1.8V and reference voltage is 0.8V. The LDO is simulated for a load capacitor of 4.7 µF and ESR resistance of 5Ω. The load resistor 'Rl' is varied from 5 kΩ to 54 Ω. The performance summary of the design is shown in Table 2.

Corner analysis

The LDO regulator simulated under Fast-Fast (FF), Normal-Normal (NN) and Slow-Slow (SS) corners. In FF corner, 'Vin' was set to 1.89V (1.8 + 5%) at -40º C temperature whereas in SS corner 'V_{in}' was set to 1.71V (1.8 – 5%) at 125º C temperature. We can observe that even under worst corners (FF and SS) the designed circuit is regulating at 1.6V as required.

Frequency response

The designed LDO is compensated using ESR zero with only one dominant pole present in unity gain bandwidth (UGB). The fig. 3 (a) and (b) presents the open loop frequency response of LDO under no-load (320 µA) and full-load (30 mA) conditions respectively. It can be observed that the UGB varies from 88 kHz to 1.72 MHz from no-load to full-load and the phase margin is above 70 deg in both the cases ensuring the open loop stability.

Table 2 – Performance summary

Parameters	Ref [3]	Ref[4]	Ref[5]	This work
I-load (max)	100mA	100mA	50 mA	30mA
I-load (min)	-			320µA
C (compensation)	3 pF	7 pF	21 pF	Self-compensated
PSRR@ DC	-50 dB	-	-55dB	-78 dB
PSRR	-40 dB @151KHz	-40dB @10 KHz	-	-60 dB @151KHz
Transient peak(mV)	<115	<100	<90	<0.20
Load Regulation	35.3 mV/A	109 mV/A	2%	5.39 mV/A
Technology	180nm	350nm	350nm	90nm

Transient response

The load transient and line transient simulations were performed. For ±10% change in supply voltage the line regulation is 28 µV/V. The load variation of 0 to 30 mA the load regulation calculated as 5.39 mV/A.

Power Efficiency

$$\text{Efficiency} = \frac{I_0 V_0}{(I_0 + I_q)V_i} \quad \ldots (4)$$

I_0 = Output current,I_q = Quiescent Current,

V_0= Output Voltage, V_i = Input Voltage.

Ratio between the output power to the input power[1].If the load current much greater than the quiescent current , then the efficinency will be defined as ratio of output voltage to the input voltage as shown in equation (4) below.In our design at full load, the source current measured was 29.8064 mA and Output current was 29.6338 mA. Output voltage (V_0) regulated to 1.60023 V and Input voltage (V_i) was 1.8 V. Efficiency using above formula is 88.38 %. Since the efficiency is above 85% with low leakage power, this design is power efficient.

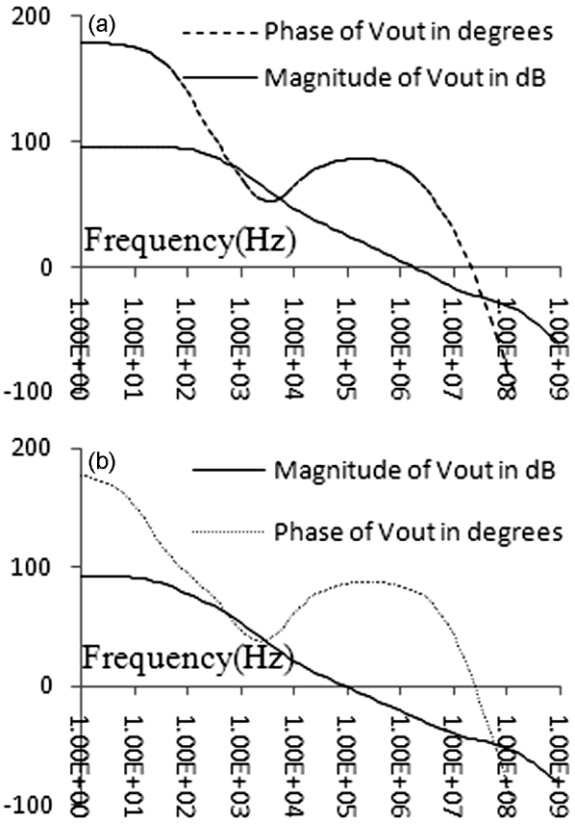

Fig. 3 – Open loop frequency response of LDO. (a) Full-load (30 mA) (b) No-load (320 µA)

Conclusion

In this paper, a power efficient (200mV dropout voltage) on-chip Low Drop-Out voltage regulator is successfully designed and implemented using 90nm CMOS technology. The implemented architecture consists of an error amplifier, a PMOS pass transistor and a feedback network. The designed LDO gives a stable output voltage of 1.6V. Further, the LDO feedback network can be modified to have the multiple regulated output voltages as per the requirement.

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