
A Study on Optimization of Circuit Components in High Boost Ratio DC-DC Converters with Hybrid-based Configuration

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Chapter 1

Introduction

1.1 Background

Renewable energy (RE) sources become significantly important due to climate change and global warming concerns. Basically, the renewable energy sources such as sunlight, wind, tides, and geothermal are constantly generated from the natural process and those energies can be used to generate electricity energy. Meanwhile, the International Energy Agency (IEA) defined the renewable energy as follows [1]:

“Renewable energy is derived from natural processes that are replenished constantly. In its various forms, it derives directly from the sun, or from heat generated deep within the earth. Included in the definition is electricity and heat generated from solar, wind, ocean, hydropower, biomass, geothermal resources, and biofuels and hydrogen derived from renewable resources.”

According to the Renewables 2010 Global Status Report [2], from the end of 2004, worldwide renewable energy capacity grew at rates of 10 – 60% annually for many renewable-based-technologies such as solar photovoltaic (PV), wind power, solar hot water/heating, ethanol production, solar thermal power, geothermal power and biodiesel production. Wind power and many other renewable-based-technologies, growth accelerated in 2009 relative to the previous four years. However, grid-connected PV increased the fastest compared to all renewable-based-technologies, with a 60% annual average growth rate.

Meanwhile, in the Renewables 2015 Global Status Report [3], the renewable energy provided an estimated 19.1% of global final energy consumption in 2013, and growth in capacity and generation continued to expand in 2014. The most rapid growth, and the largest increase in capacity, occurred in the power sector, led by wind, solar PV, and hydropower. By the end of 2014, renewable energies comprised an estimated 27.7% of the world's power generating capacity, enough to supply an estimated 22.8% of global electricity. Based on the current trend, the renewable energy capacity will continue to grow in the future years [2-5].

Figures 1.1 and 1.2 show the renewable energy capacity growth trends of the wind power and solar PV power between 2004 and 2014. Wind power and solar power amongst the important renewable energy sources for electricity generation. In addition, solar-power-based may produce most of the world's electricity within 50 years and consequently it reduces the emissions of greenhouse gases that harm the environment [1, 6]. Thus, these renewable energies will play an important role for the future electricity energy sources.

Wind Power Global Capacity, 2004–2014

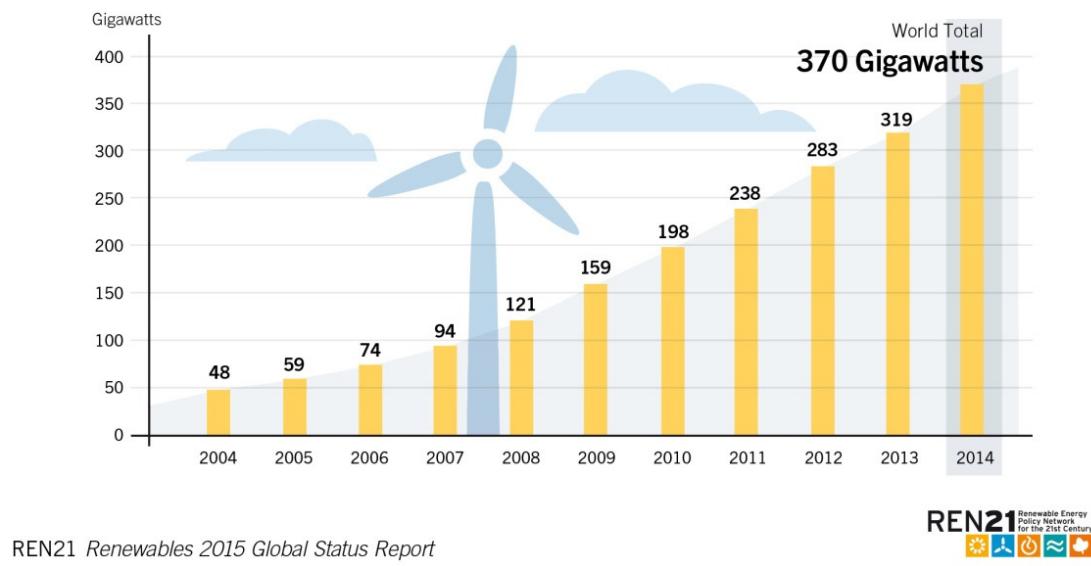


Figure 1.1 Wind power global capacity, 2004 – 2014 [3].

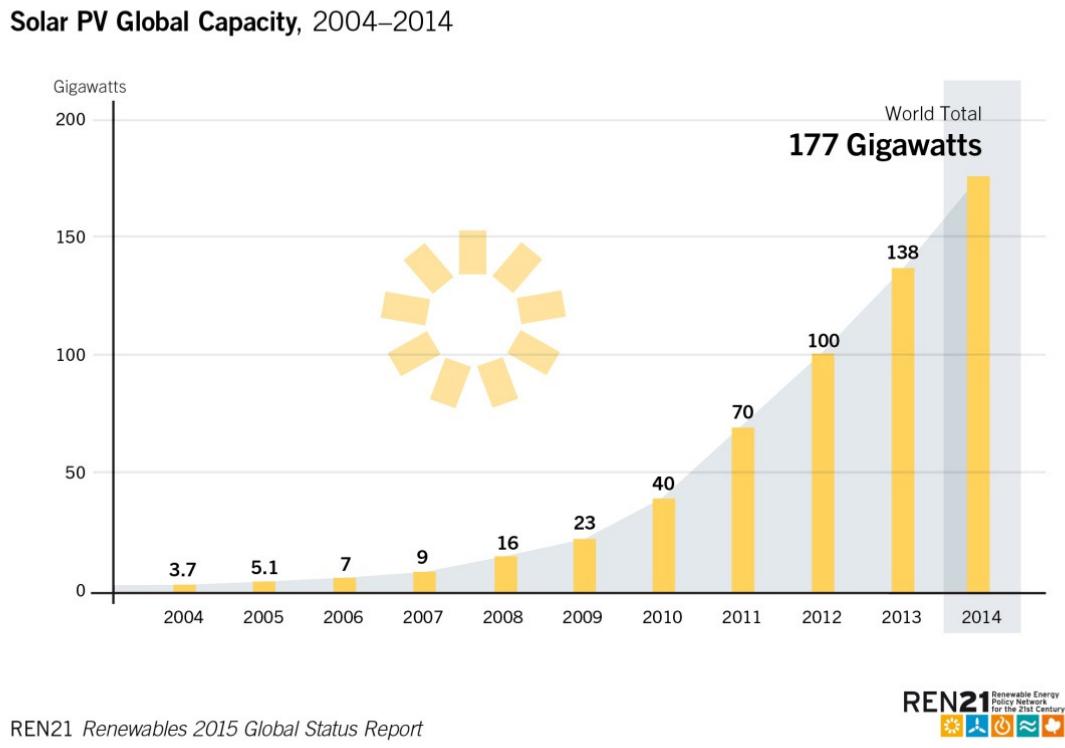


Figure 1.2 Solar PV global capacity, 2004 – 2014 [3].

The generated energies from renewable sources need to be managed and controlled in order to be useful to the humankind. Power conversion technology is one of the methods for the generated energies from renewable sources to be converted into electricity energy. In addition, power conversion technologies are actively and aggressively studied by researchers all over the world since 50 years ago [7-17]. As a result, many power converter technologies, energy conversion systems and energy policies have been introduced in order to optimize and fully utilize those renewable energy

sources. Besides, due to rapid expanded demand and awareness of the renewable energy usage on electrical loads, those power converter technologies and energy conversion systems are improved in order to achieve higher efficiency, reliability and stability. Furthermore, energy policies and regulations especially on renewable energies are frequently revised for monitoring and control purposes.

On the other hand, the generated electricity energy from the renewable sources needs to be managed and controlled for the humankind usage and must be according to the load requirements. Power conversion technologies especially in power electronics field are actively studied since 19th century. Therefore, many kinds of power converter technologies have been introduced and developed. The power converter technologies are improving from time to time for achieving better performance and efficiency due to the renewable energy sources constraints and power devices limitation [18-21].

On top of that, micro-grid system has been introduced in order to manage and control the electricity energy from the renewable energy sources due to advantages of better power quality, environmentally friendly and has good technical aspects on power flow reduction especially on transmission and

distribution networks [22-28]. Basically micro-grid system consists of power generations, power converters, energy storage systems, control systems and protection systems. Generally, micro-grid system focuses on low voltage distribution side and it connected to a grid system. Fig. 1.3 shows the general direct current (DC) micro-grid system. Besides, power converter is one of the important components in the micro-grid system for electricity power conversion in order to power up electrical loads accordingly.

Generally, a datacenter is one of the important loads in commercial buildings. Besides, new datacenters system use DC power supply system due to several advantages compared to alternating current (AC) power supply system [29-33]. Thus new datacenters system can be one of the important DC micro-grid loads. On the other hand, according to some findings, datacenters consume highly electricity power and in fact it needs also reliable supply sources. Although most datacenters rely on the main power grid, the system also requires locally available standby power source in case of power grid failure. Therefore, the micro-grid system can play an important role in order to be a reliable local integrated power supply [34-39].

Fig. 1.4 shows the general datacenters system configuration with HVDC and DC micro-grid connected.

Nowadays DC power supply system in datacenters and telecommunication buildings become current trends for minimizing installation and maintenance costs [40-44]. Hence, DC power supply technologies in datacenters and telecommunication building have been actively studied due to the advantages of high efficiency and high reliability over AC power supply technologies. In DC power supply system, the conversion loss is reduced due to the reduction of power conversion number [45-48]. For example, in a general AC power supply system, four power conversions are required; meanwhile only two power conversions are required in a DC power supply system for data centres [49, 50]. In addition, copper size reduction at load sides also can be achieved. Thus high efficient of DC-DC power converters are needed in order to realize this intention effectively.

DC-DC converter is one of the power converter technologies in order to convert from one level of DC voltage to another level of DC voltage [51-53]. In addition many circuit structures and topologies of DC-DC converters that

able to convert DC voltage levels from one level to another have been introduced and proposed. Generally it can be categorized into two, i.e. isolated and non-isolated DC-DC converters. If an isolation feature of DC-DC converters is not required, the non-isolated type of DC-DC converter is a good option due to transformer-less feature. Generally, isolated DC-DC converters in high voltage applications have several problems of bulkiness, leakage inductance due to imperfect-coupled winding of transformer and leakage current occurrence due to parasitic capacitance between transformer windings. Thus non-isolated type of DC-DC converter becomes an advantage.

Generally, DC voltages can be tapped from the renewable energy (RE) sources with specific arrangements and connections of PV panels by using two-level conventional DC-DC boost converters (CBC). On the other hand, conventionally a two-level conventional DC-DC boost converter (CBC) is considered in order to convert a DC voltage level from RE sources to another level of DC voltages. Unfortunately, the two-level CBC suffers from bulkiness of an input inductor due to circuit structure limitations. In order to reduce the input inductor, multilevel and multistage DC-DC converters are

introduced by many researchers. The generic topologies of DC-DC converter can be categorized into three major topologies, i.e., diode-clamped, cascaded-structure and capacitor-clamped.

This thesis focuses on development of multilevel and multistage DC-DC converter structures with passive components reduction and high conversion ratio of voltage features. Based on the generic topologies of DC-DC converters, a conventional diode-clamped topology requires many diodes and has fewer redundancies of switching schemes operation, consequently the application is limited. Meanwhile, with cascaded-structure topology, it usually needs many switching devices due to inductor-less feature consideration. Some other cascaded-structure topologies need a transformer for a voltage conversion. From these generic topologies of DC-DC converters, flying capacitor topology (based on capacitor-clamped topology) shows attractive features, i.e. this converter needs only a small input inductor and small flying capacitors in order transfer energy from an input side to an output side.

On the other hand, some of the renewable energy (RE) sources only able to generate low DC voltages, thus high conversion ratio of voltage of

DC-DC converters are required in order to generate high DC voltages. Thus, DC-DC converters with high conversion ratio of voltage capability need to be considered in order to realize this intention. A multistage Marx impulse generator topology for high voltage and high current pulses generation has attractive circuit structure and configuration. The circuit structure based on Marx impulse generator topology can be adapted into DC-DC converters in order to achieve high voltage at an output side and high current at an input side configuration. Specifically, parallel connections of stage capacitors at low voltage side and then series connections of the same stage capacitors at the high voltage side are the attractive circuit arrangements for this topology. By considering these configurations, current stress and voltage stress are reduced at low voltage side and high voltage side, respectively. As a result high efficiency of a high boost ratio DC-DC converter can be achieved for medium and high power applications.

Therefore, DC-DC converters based on flying capacitor topology and Marx topology will be described in details in the following chapter for passive components reduction and high conversion ratio of voltage achievement.

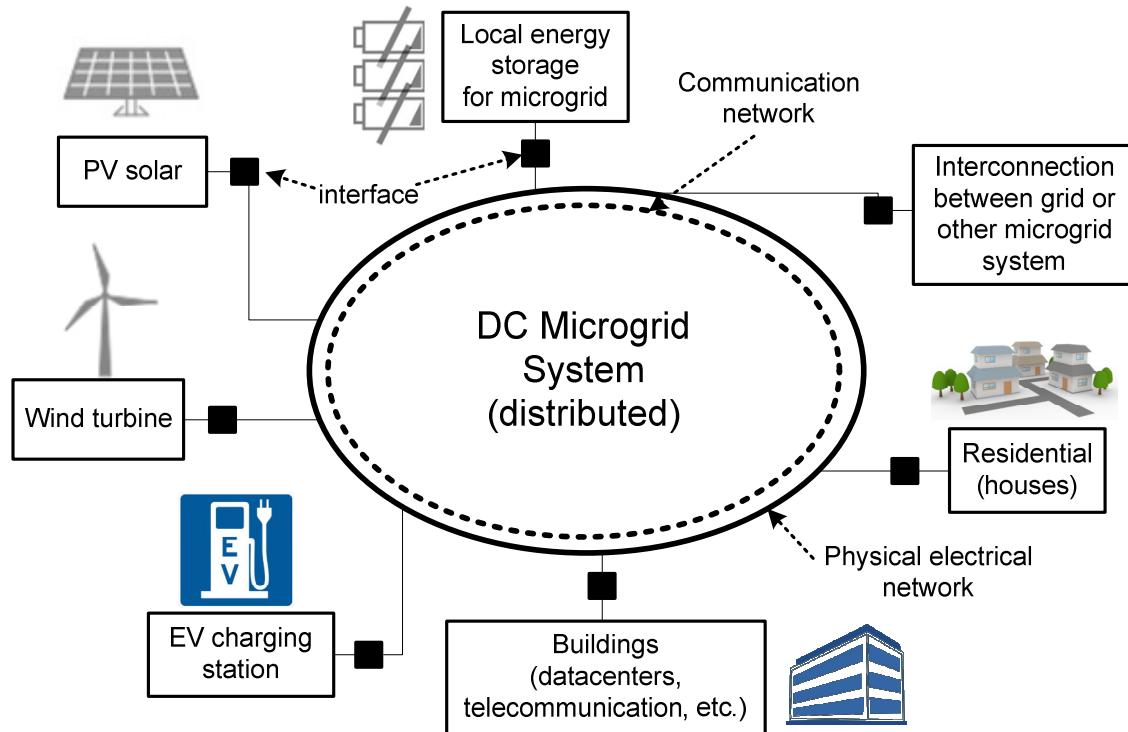


Figure 1.3 General DC micro-grid system.

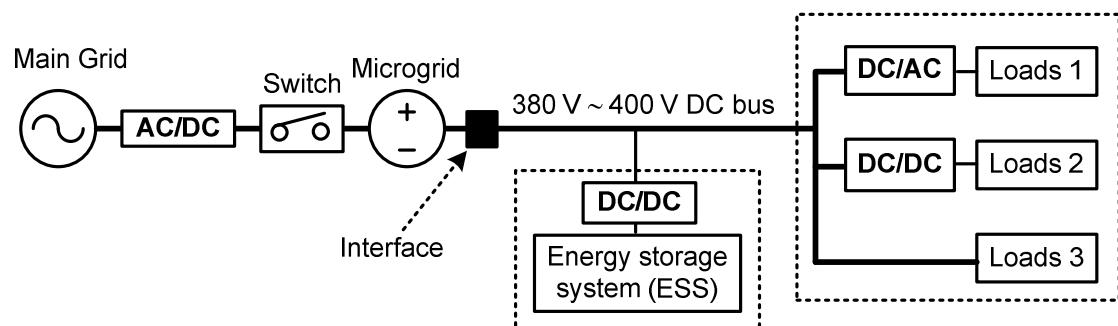


Figure 1.4 Datacenters system configuration with HVDC and DC micro-grid connected.

1.2 Research Objectives

Future datacenters and telecommunication building require DC power supply systems in order to transfer electricity energy to loads. Some of the electricity sources come from RE, such as solar PVs and Wind turbine. Thus, high efficient of DC-DC power converters are required in order to convert DC voltages from one level of DC voltage to other levels as required by loads. Conventional DC-DC converters are usually used due to less required number of components and simple structure. Unfortunately, this conventional DC-DC converter suffers from bulkiness of an input inductor especially when medium and high power applications are considered. Consequently, size, volume and weight of the converter became large and heavy. This is because the conventional DC-DC converter only uses an inductor in order to transfer energy from an input side to an output side. In addition voltage stress on switching devices is high due to circuit structure limitation and only low voltage conversion ratio is suitable in practical.

One of simple ways in order to reduce the inductor volume density is to increase the switching frequency. Principally, the fast and short period time

of charging and discharging can reduce the volume density of required passive components. However, at some extend this approach will degrade performance of the converters since more switching losses are generated and other issue as well. On the other hand, silicon based switching devices have limited ranges of operating frequency. In order to overcome these problems concretely, multilevel and multistage DC-DC converters structures are introduced. With these multilevel and multistage structures, passive components reduction, i.e., inductors and capacitors, voltage stress reduction on switching devices, current stress reduction at low voltage side and high conversion ratio of voltage capability can be achieved.

The objective of this research is to consider passive components reduction, i.e., inductors and capacitors, voltage stress reduction on switching devices and current stress reduction at low voltage side for high conversion ratio of voltage of DC-DC converters. In order to realize this intention, multilevel and multistage structures are considered. This study only focuses on non-isolated DC-DC boost converters type, thus all discussion in this thesis will be based on this view of power converters.

In this thesis, DC-DC converters are categorized based on passive

components perspectives which are magnetic-based, capacitor-based and hybrid-based configurations. Hybrid-based configuration is defined as a combination of inductor and capacitor components in a DC-DC converter.

Basically, a magnetic-based DC-DC converter configuration needs a large output capacitor in order to smooth out current and voltage transients that generated by the switching devices of the converter, and also to act as an energy reservoir for the load when the converter is not delivering power to the output. Meanwhile, with a capacitor-based DC-DC converter configuration, a changing capacitor voltage always follows the exponential function which causes the high spike current will be initiated and caused low efficiency of the converter. This problem can be avoided by introducing inductive elements arrangement in the circuit. Therefore, with the hybrid-based DC-DC converter configuration, the disadvantages of the magnetic-based converter and the capacitor-based DC-DC converter configurations can be properly tackled for high efficiency achievement and for high power applications. In addition by considering the multilevel and multistage circuit configuration, the passive components can be further reduced.

Figure 1.5 shows DC-DC converters are categorized based on the passive components perspective with multilevel and multistage structures consideration. From these configurations, a flying capacitor type is selected for passive components reduction due to an advantage of multilevel structure and Marx topology type is selected for high conversion ratio of voltage achievement due to an advantage of multistage structure. In addition voltage stress on switching devices and current stress at low voltage side are also reduced in the Marx topology and flying capacitor topologies.

Meanwhile Figure 1.6 shows the generic DC-DC boost converters features based on the hybrid-based, capacitor-based and magnetic-based configurations. Thus, the hybrid-based configuration has advantages of small inductive and capacitive elements consideration especially for medium and high power applications as compared to the magnetic-based and capacitor-based configurations. In high power applications, such as in micro-grid system, the hybrid-based configurations of DC-DC boost converters are required due to the advantages on passive component reduction and high conversion ratio of voltage achievement.

First, the DC-DC boost converters based on passive component configurations are described, i.e., magnetic-based, capacitor-based and hybrid-based configurations. Based on these configurations, several generic DC-DC boost converters are identified and categorized. Then, DC-DC converter features from each configuration are discussed for clarifications. After that, multilevel and multistage structures are considered based on these configurations for passive components reduction with high conversion ratio of voltage considerations.

Multilevel flying capacitor boost converters (FCBC) are selected for prototypes development and construction in order to verify passive components reduction design methods, theoretically and experimentally. Many studies have not clarified on how the passive components can be reduced in the flying capacitor DC-DC converter types [54-56]. In this study the passive components reduction methods are theoretically clarified and experimentally verified in the FCBC. Besides, the effectiveness of the reduced and small passive components consideration is experimentally validated.

Furthermore, a multistage Marx topology DC-DC boost converter

(MTBC) is proposed and developed in order to achieve high conversion ratio of voltage feature. In addition this proposed converter has a modular feature at an output side. With this converter, parallel-series configuration is applied on the stage capacitor in order to reduce current stress at low voltage side and to reduce voltage stress on switching devices. In addition, interleaved operation is also considered in the constructed multistage MTBC in order to reduce output inductor volume and to reduce current stress on switching devices.

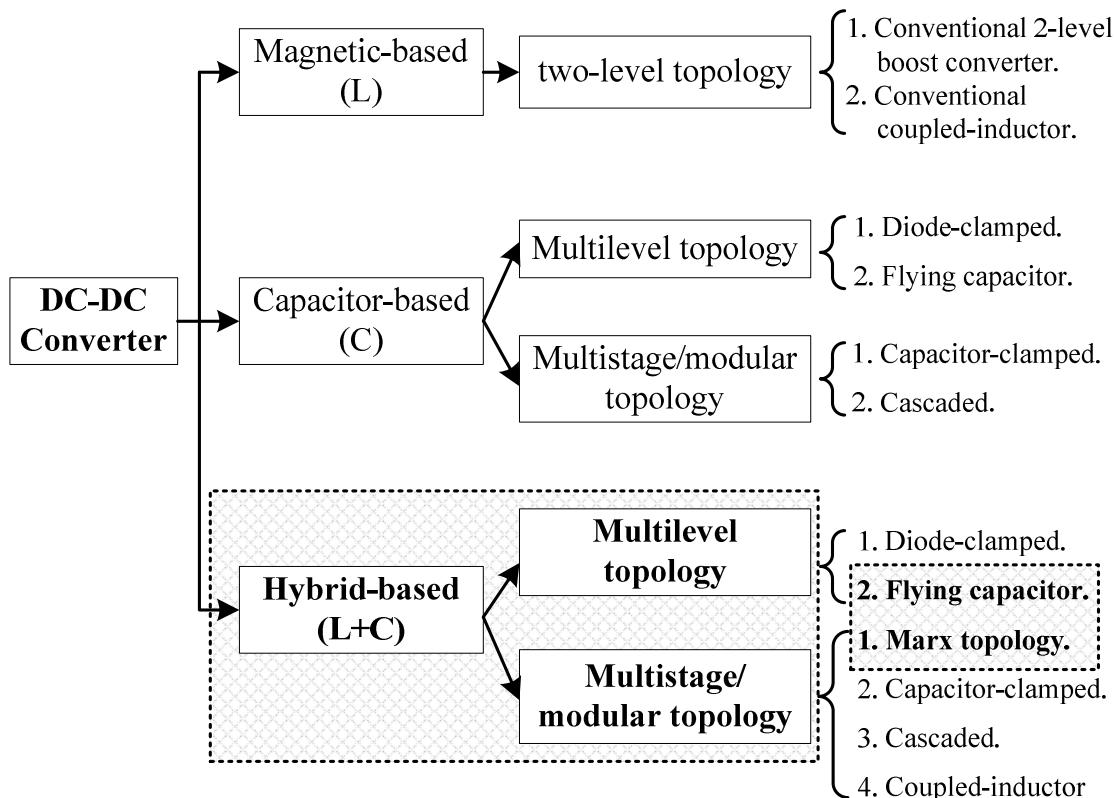


Figure 1.5 DC-DC converter based on passive components perspectives.

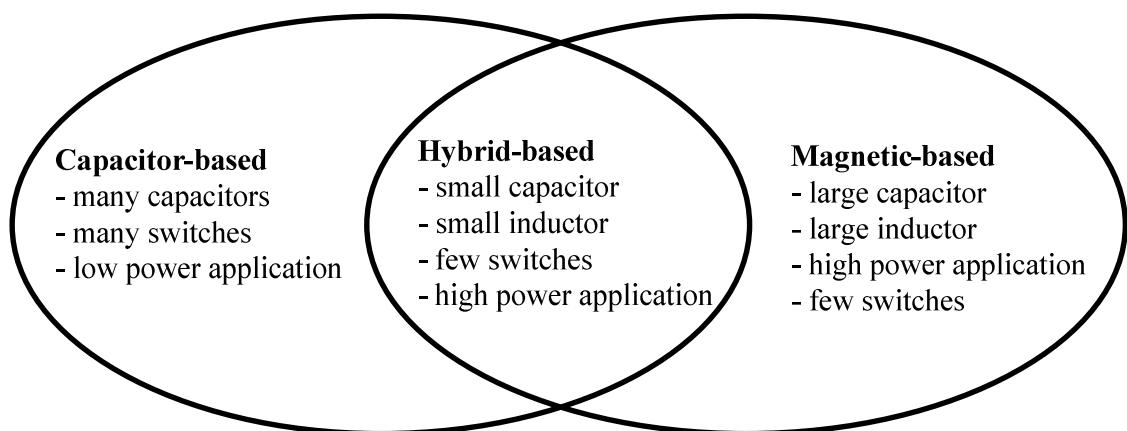


Figure 1.6 DC-DC boost converters features based on the hybrid-based, capacitor-based and magnetic-based configurations.

1.3 Thesis Outline

Figure 1.7 shows the outline of this thesis which is divided into 6 chapters. Chapter 1 is the introduction whereby the importance of renewable energies consideration due to global warming issue is described. Then, the important role of power converters in the renewable energy sector is discussed especially DC-DC converters. The power conversions in DC micro-grid and datacenters systems are the focus applications in this thesis. The objectives of the passive components reduction and the high conversion ratio of voltage achievement in the multilevel and multistage structures of DC-DC boost converters are described.

Chapter 2 reviews the categorization of DC-DC converters based on passive components perspectives. In addition, DC-DC converters based on magnetic-based, capacitor-based and hybrid-based configurations are discussed and compared. By considering the advantages of multilevel and multistage structures, the passive components in the hybrid-based configuration of DC-DC converters are reduced. In addition the current stress at low voltage side and voltage stress on switching devices are reduced as well in the multilevel and multistage topologies. Based on this

justification, the DC-DC converters are developed based on hybrid-based configuration with multilevel and multistage structures. The details discussion and analysis of the developed DC-DC converters are discussed in details in Chapters 3, 4 and 5.

Chapter 3 focuses on the design and development of a DC-DC boost converter whereby three-level flying capacitor boost converter (FCBC) is constructed. The constructed three-level FCBC is based on hybrid-based configuration. With this constructed converter, the input inductor is reduced according to the converter level and based on maximum product of the charging time of inductor T_L and the inductor voltage V_L . In addition, the small capacitance of the flying capacitor can be considered in the three-level FCBC due to independent relationship between the flying capacitor voltage ripple, the input inductor current ripple and the output voltage ripple. Thus the small capacitance can be considered in the constructed converter. However, due to the small capacitance consideration, the flying capacitor ripple voltage is high. Thus the design of the capacitance is clarified and according to the maximum voltage rating of switching devices. Based on this justification, the size and weight of the

converter can be reduced especially the inductance and volume of the input inductor and the capacitance of the flying capacitor for obtaining high power density. In addition power density characteristics for two-level CBC and three-level FCBC are evaluated theoretically.

Chapter 4 discusses effectiveness of the small capacitance of the flying capacitor in the multilevel FCBC. Three-level and five-level FCBCs are constructed in order to evaluate the effectiveness of the small capacitance of the flying capacitors experimentally. The flying capacitor design is based on the voltage rating on switching devices in the multilevel FCBC is clarified. The effectiveness of the small capacitance is analyzed based on the characteristics of the distorted voltage across input voltage and inductor voltage and the distorted current to the output capacitor and load. In addition, the number of level in the multilevel FCBC is influencing the small capacitance of the flying capacitor design. As a result, the distorted voltage and current are reduced when the level is increased with consideration of the small capacitance of the flying capacitor. Thus high power density of the multilevel FCBC can be achieved with minimized input inductor and small flying capacitor considerations.

Chapter 5 discusses a proposal of high conversion ratio of voltage of the multistage Marx topology DC-DC converter (MTBC). This converter is also based on hybrid-based configuration. In the proposed converter, parallel-series connections are applied on stage capacitors. With this configuration, at the low voltage side, parallel connections of the stage capacitors are applied and consequently the current stress is reduced. On the other hand, at the high voltage side, the same stage capacitors are then connected in series and consequently voltage stresses on switching devices are reduced. Thus, if the stage numbers are increased, the current stress at the low voltage side and voltage stresses on switching devices will be further reduced. Besides, the interleaved operation in the three-stage MTBC is considered for the output inductor volume reduction. In addition power density characteristics for the three-stage MTBC and other converter topologies are evaluated and compared theoretically.

Chapter 6 is the conclusion, the advantages and disadvantages of the proposed converters are clarified. The present research works are summarized and the future works are discussed.

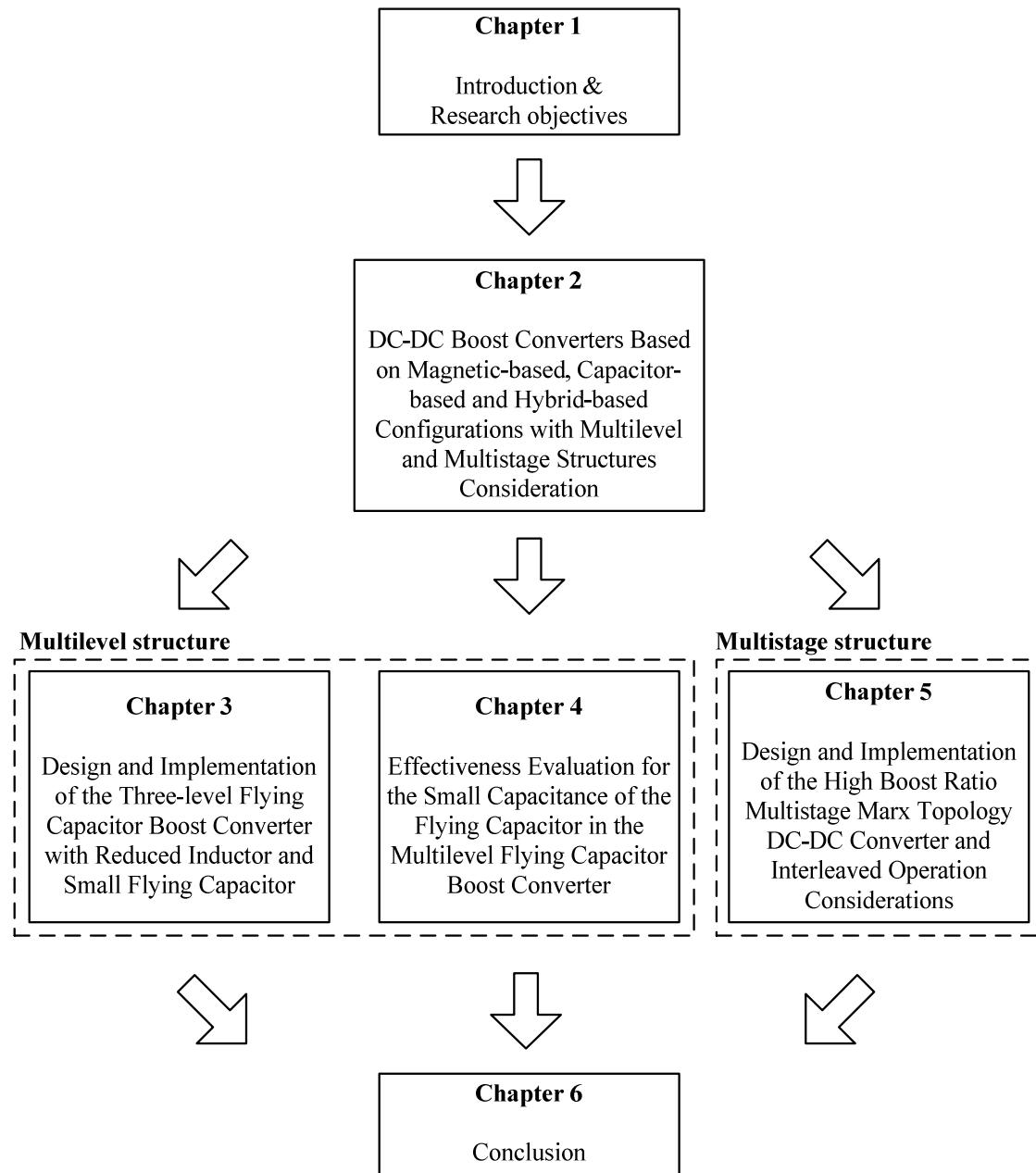


Figure 1.7 Outline of the thesis.

Chapter 2

DC-DC Boost Converters Based on Magnetic-based, Capacitor-based and Hybrid-based Configurations with Multilevel and Multistage Structures Consideration

2.1 Introduction

The previous chapter has illustrated in general the importance of power converters in the DC micro-grid and renewable energy (RE) systems for the data centers system and telecommunication buildings applications. DC power supply system becomes an importance nowadays due to more reliable, stable and flexible over AC power supply system [57-62]. Furthermore, DC power supply system shows significant advantages such as growing of DC loads, power quality issue in AC power supply system

and to reduce the conversion losses as occurred in AC power supply system [29-31, 33].

Many kinds of DC-DC converter topologies and circuit structures have been introduced and developed according to loads, devices and system requirements. The conventional DC-DC boost converters (CBC) are usually suffering from the bulkiness, high losses, large of capacitor and inductor components and low efficiency when dealing with high current and high voltage stresses [51-53]. The passive components, i.e., inductor and capacitor can be further reduced by introducing multilevel and multistage circuit structures. In addition voltage stresses on switching devices are also reduces when multilevel and multistage structures are considered. In this thesis, the author proposes reduction on passive components, i.e., inductor and capacitor in multilevel and multistage DC-DC converters with no compromises of converters efficiency and performance. As a result, total volume and weight of converters are reduced. Furthermore due to the development of high performance switching devices with low-loss and high-voltage stress features [63-66], thus the downsizing factor is higher priority rather than the usage of low-voltage

stress switching devices. As a result the number of levels in DC-DC converters can be optimized accordingly.

In this chapter a state-of-the-art of DC-DC converters based on passive components perspectives is the main concerned. Furthermore, from the passive components perspectives, DC-DC converters are categorized into three main configurations, i.e., magnetic-based, capacitor-based and hybrid-based, respectively whereby the hybrid-based configuration is a combination of magnetic and capacitor components for energy transfer compensating. Following are the brief descriptions of the DC-DC converter based on these three main configurations:

- (i) Magnetic-based configuration – only inductor component is used in order to transfer energy from input to output sides of converters, thus it usually needs a large and bulky inductor especially in high power applications. The DC-DC converters based on this configuration usually get less attention from researchers due to the requirement of large and bulky inductor [51-53, 67]. Generally, typical converters which are based on this configuration are conventional two-level DC-DC boost

converter (CBC) and interleaved multiphase conventional DC-DC converter.

- (ii) Capacitor-based configuration – only capacitor component is used in order to transfer energy from input to output sides, thus it needs very large capacitor in order to balance the voltage level between capacitors. It also suffers from high surge current during charging and discharging conditions of capacitors. The DC-DC converters based on this configuration are actively discussed by many researchers due to lightweight factor and high volume density achievement [51, 68-70]. In addition, it is usually designed for low power applications with narrow input and output voltages variation. However, zero current switching (ZCS) method might be considered in order to reduce switching loss if higher power application is required [71]. Generally, Inductor-less switched-capacitor topology is based on this configuration and widely used.

- (iii) Hybrid-based configuration – a combination of inductor and capacitor components are used in order to transfer energy from

input to output sides, thus the converter only needs small inductor and small capacitor due to energy compensating between these passive components. In contrast, DC-DC converters based on magnetic-based configuration only uses an inductor in order to transfer energy from input to output sides and consequently it needs large inductive element. Meanwhile, DC-DC converters based on capacitor-based configuration, the energy is transferred from input to output sides through many capacitors and usually it connected in series-parallel arrangement, thus it needs large capacitive elements in order to maintain voltage levels and for surge current suppression. In addition, the high surge current problem during charging and discharging of capacitors is usually suppressed by inductive elements [51-53]. The DC-DC converter based on combination of inductive and capacitive elements are very reliable due to energy compensating transfer feature between inductive and capacitive elements [51-53, 55, 56, 72-82]. From this combination of inductor and capacitor components, many

topologies and structures of DC-DC converters have been introduced and developed for many applications with wide load ranges.

General overviews on magnetic-based, capacitor-based and hybrid-based configurations are discussed in Section 2.2. In addition, the intensive overviews of DC-DC converters based on magnetic-based, capacitor-based and hybrid-based configurations are also clarified and discussed in Section 2.2. Furthermore, in this section a conventional two-level DC-DC boost converter (CBC) and a three-level DC-DC converter are selected for clarification based on each configuration. Then, the advantages and disadvantages in terms and circuit structure behaviors are described accordingly. Besides, wide comparisons of various DC-DC converters are also conducted in order to demonstrate the difference among of the various DC-DC converters.

Section 2.3 discusses the non-isolated and isolated DC-DC converters topologies in terms of voltage and voltage conversion ratio capabilities. Several generic non-isolated and isolated DC-DC converters are selected for comparisons.

On the other hand, multilevel and multistage of DC-DC converters based on hybrid-based configurations are considered and it is discussed in Section 2.4. Several generic DC-DC converter topologies based on hybrid-based configurations are selected for details discussion and comparison. Furthermore the advantages of the selected converter topologies are also clarified and described. In addition, the proposed DC-DC converters features based on hybrid-based configuration are also intensively elaborated, i.e., flying capacitor topology and Marx topology of DC-DC converters with high voltage conversion ratio feature. In order to evaluate power density of the proposed converter, a Pareto-front curve is considered. The Pareto-front curve principle is also introduced briefly in Section 2.4.

Conclusion is discussed in Section 2.5. The advantages of multilevel and multistage structures of DC-DC converters based on hybrid-based configuration are emphasized accordingly in this section.

2.2 Overview of DC-DC Boost Converters Based on Magnetic-based, Capacitor-based and Hybrid-based Configurations

Generally many circuit configurations are introduced and developed in order to achieve DC-DC voltage conversion. Furthermore each proposed circuit configuration has its specific advantages and disadvantages, depending on several factors such as application requirements, devices limitation, voltage conversion ratio ranges, maximum output power, power conversion efficiency, number of components, converter weight and size, power density, and galvanic separation requirement between an input and an output sides. In addition, these factors generally contribute to the converter design specifications. However in a DC-DC converter design specifications, it usually refers to specific application requirements although several good features need to be ignored as trade-off constraints and due to application limitations. Moreover, stable operation of converters is considered as an important priority. For example, in order to achieve very few numbers of components, a conventional two-level boost converter (CBC) might be a good option, however the converter has limitations on

high voltage conversion ratio capability achievement and requires large passive component in order to confirm stable operation of the designed converter. These advantages and disadvantages factors are considered as trade-off one another. Thus the specific application requirements are the important factor in designing DC-DC converters.

Figure 2.1 shows the hybrid-based, capacitor-based and inductor-based configurations of DC-DC converters with respect to power and power density parameters. Generally, DC-DC converters based on capacitor-based configuration has superior power density compared to the inductor-based configuration due to inductor-less feature. However this configuration suffers from high surge current during charging and discharging processes of capacitors, consequently large capacitive elements are required. Thus, DC-DC converters based on this configuration usually suitable for low power applications with very narrow voltage conversion ranges.

Meanwhile, DC-DC converters based on magnetic-based configuration are suitable for high power applications due to the existing of inductive element. However with this configuration, the power density becomes low due to the bulkiness of inductive elements especially when the converter

operated in high power applications.

Therefore by considering DC-DC converters based on hybrid-based configuration, several good features from the capacitor-based and magnetic-based configurations are adopted. Figure 2.1 shows that with the hybrid-based configuration of DC-DC converters, high power and optimum power density can be achieved due to the existing of the capacitive and inductive elements.

In this thesis, the definitions of multilevel and multistage of DC-DC converters are defined and differentiated for a reference for the following section discussion. Figure 2.2 shows a generic two cells configuration and each cell has several combinations of switches. In addition, each cell has two input terminals (*a* and *b*) and three outputs terminals (*c*, *d* and *e*). Between cell-1 and cell-2, several possible connections are considered (dashed line) from output terminals of cell-1 to input terminals of cell-2.

From Figure 2.2, if the capacitor voltages of V_{C1} and V_{C2} are not same, this condition is defined as a multilevel structure configuration. In this study, multilevel structure of DC-DC converters is considered for passive components and switching devices voltage stress reductions. In addition,

multilevel structure is suitable for medium to high boost ratio of voltages conversion. Nevertheless it depends on circuit structures and converter configurations.

In contrast, if the capacitor voltages of V_{C1} and V_{C2} are same, this condition is defined as a multistage configuration. In fact, due to the same capacitor voltage at each stage, high conversion ratio of voltage can be achieved by series connection of those capacitors. In addition, the purpose of multistage structure of DC-DC converters is to achieve high conversion ratio of voltage and for switching devices voltage stress reduction. In addition, passive components reduction is also can be achieved due to multistage feature. Therefore, each structure has unique advantages, i.e., converter with multistage structure has advantage on high conversion ratio of voltage achievement and converter with multilevel structure has advantage on passive components reduction.

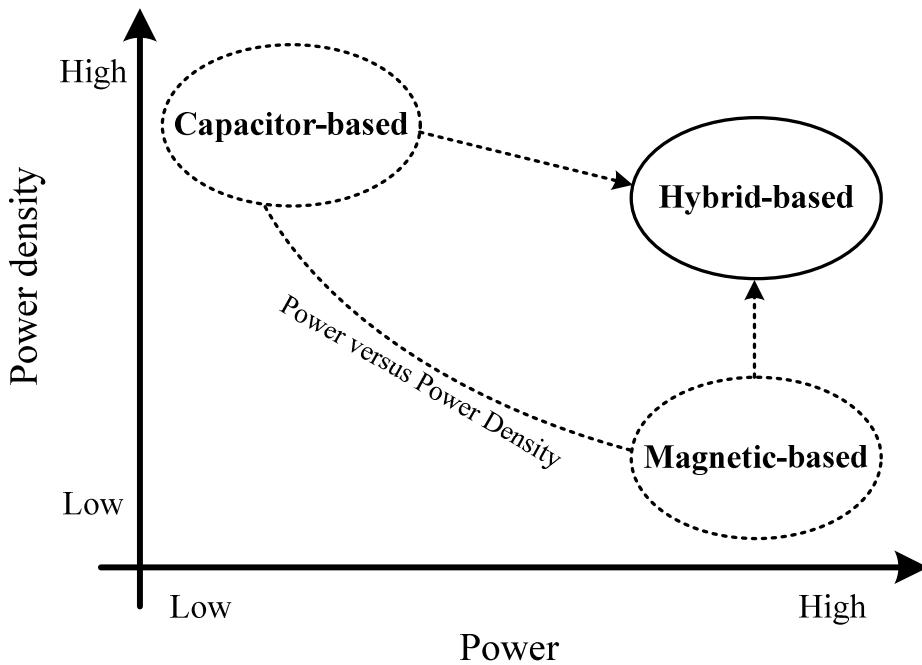


Figure 2.1 Hybrid-based, capacitor-based and inductor-based configurations of DC-DC converters based on power and power density.

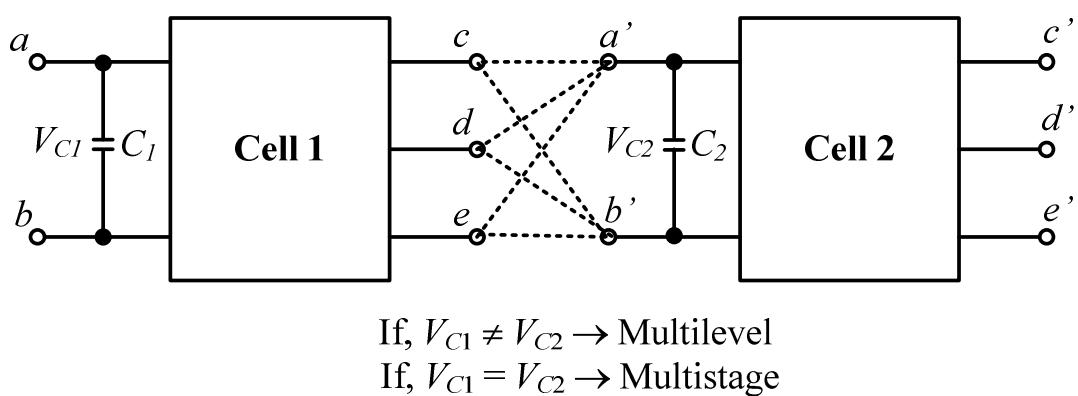


Figure 2.2 Definitions of multilevel and multistage of DC-DC converters.

2.2.1 Magnetic-based configuration of DC-DC converters

Generally, when a DC-DC boost converter uses only inductor components as main energy storage, apparently it requires large inductance and large core volume of the inductor in order to store energy before it transfers to the output side or otherwise the operation of the converter will be affected [51-53, 83].

A conventional two-level boost converter (CBC) is considered as an example in this section. Figure 2.3 shows the circuit configuration of a conventional two-level DC-DC boost converter (CBC) and this converter is also considered based on magnetic-based configuration. For a comparison, all components in the circuit are considered ideal with a large output filter capacitor at the output side. Principally, this conventional two-level DC-DC converter (CBC) has two operation modes. During mode-1, the energy will be charging the input inductor L_{in} by the input DC source. Meanwhile during mode-2 the stored energy in the input inductor L_{in} will be discharging to the output side. Thus the input inductor must be large in order to transfer the energy from the input to the output sides, especially in continuous current mode (CCM) operation. On the other hand, a three-level

DC-DC converter based on hybrid-based configuration has three operation modes as shown in Figure 2.4.

Furthermore, if the conventional two-level DC-DC boost converter (CBC) and the three-level DC-DC boost converter are compared and both converters have same specifications of the input voltage 25 V, the output voltage 100 V, the switching frequency 100 kHz and the output power 1000 W, the conventional two-level DC-DC boost converter requires about three times larger of the inductance of the inductor compared to the three-level DC-DC boost converter when same inductor ripple ΔI_L is considered. This is due to the three-level DC-DC boost converter based on hybrid-based configuration has an additional middle capacitor C_{fc} (also known as a flying capacitor) for transferring energy from the input inductor to the output side as shown in Figure 2.4. Thus, principally only a small inductor and a small middle capacitor are required for the three-level DC-DC boost converter to be operated.

Obviously, from this comparison the number of turn windings of the inductor is increased and also large core volume of the inductor is required in the two-level DC-DC boost converter (CBC). In fact, the conventional

two-level DC-DC boost converter (CBC) requires bulky inductor when high power applications are considered for this converter to be operated.

Figure 2.4 shows the circuit configuration of the three-level DC-DC boost converter based on hybrid-based configuration [80].

Theoretically, the input inductor current ripples ΔI_L in the conventional two-level DC-DC boost converter (CBC) and the three-level DC-DC boost converter can be expressed by Eqs. (2.1) and (2.2), respectively. Obviously, the charging time periods for both converters are different. In one cycle period T , the conventional two-level DC-DC boost converter has one charging time $T_{L-2-level}$ condition of the input inductor as shown in Figure 2.3. Meanwhile the three-level DC-DC boost converter has two charging times $T_{L-3-level}$ conditions of the input inductor in one cycle period T as shown in Figure 2.4.

$$\Delta I_{L-3-level} = \frac{V_{L-3-level}}{L_{3-level}} T_{L-3-level} \quad (2.1)$$

$$\Delta I_{L-2-level} = \frac{V_{L-2-level}}{L_{2-level}} T_{L-2-level} \quad (2.2)$$

where $V_{L-3-level}$ and $L_{3-level}$ are the inductor voltage and the inductance, respectively in the three-level DC-DC converter, meanwhile $V_{L-2-level}$ and

$L_{2-level}$ are the inductor voltage and the inductance in the conventional two-level DC-DC boost converter (CBC).

The stored energies E_{stored} in the inductors for both converters are expressed by Eqs. (2.3) and (2.4), respectively. By considering both converters have the same specifications of the input inductor, the inductor voltage and the input inductor current, Eqs. (2.5) and (2.6) are considered. Hence the three-level DC-DC boost converter only requires approximately 33% of stored energy to be operated compared to the conventional two-level DC-DC converter.

$$E_{stored_2-level} = \frac{1}{2} I_L^2 \left(\frac{V_{L_2-level}}{L_{2-level}} T_{L_2-level} \right) \quad (2.3)$$

$$E_{stored_3-level} = \frac{1}{2} I_L^2 \left(\frac{V_{L_3-level}}{L_{3-level}} T_{L_3-level} \right) \quad (2.4)$$

$$\frac{E_{stored_3-level}}{E_{stored_2-level}} = \frac{T_{L_3-level}}{T_{L_2-level}} = \frac{7.5\mu s}{2.5\mu s} = 0.3333 \quad (2.5)$$

$$E_{stored_3-level} = 33.33\% \text{ of } E_{stored_2-level} \quad (2.6)$$

where I_L is the maximum input inductor current.

Therefore, by considering the DC-DC boost converter based on hybrid-based configuration, the passive component, i.e., the input inductor in terms of size and volume is reduced.

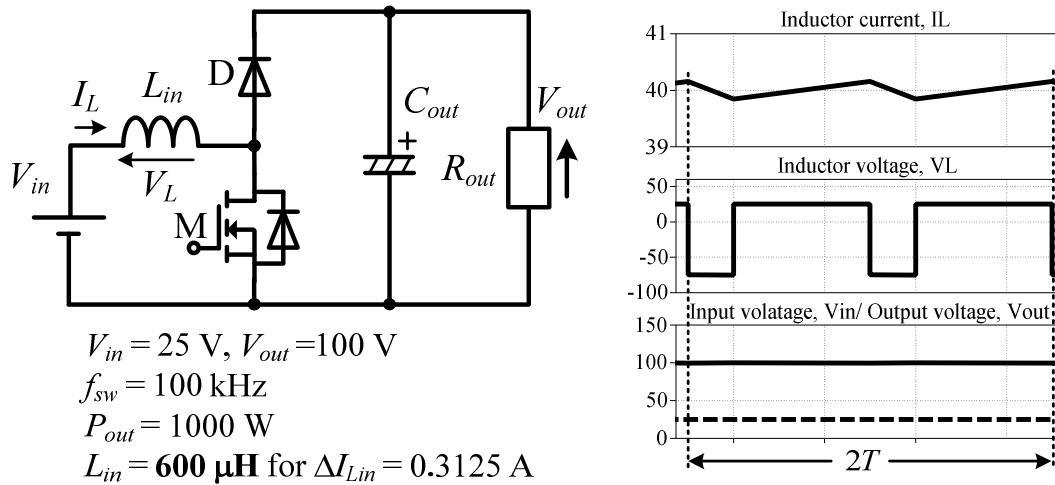


Figure 2.3 Conventional two-level DC-DC converter based on magnetic-based configuration.

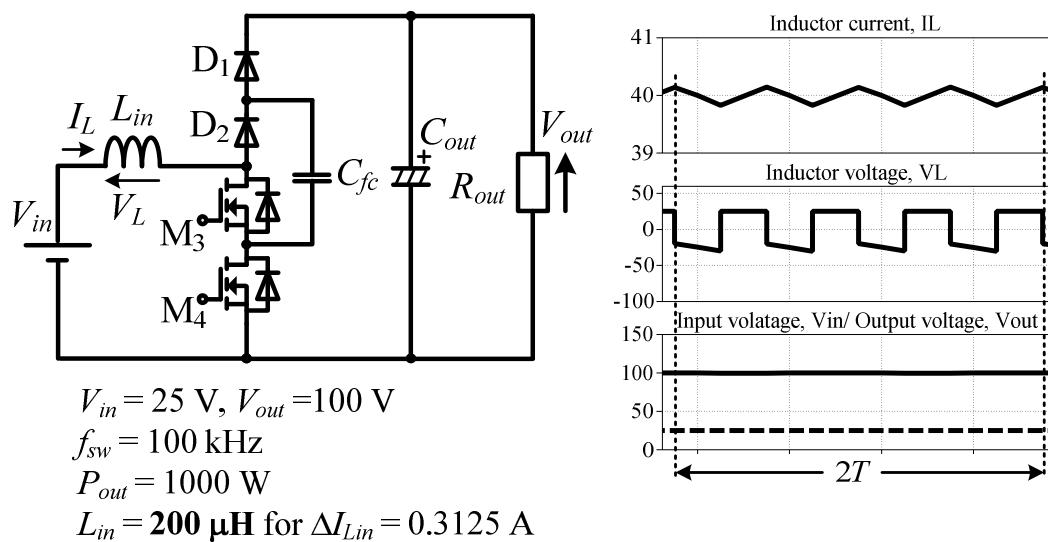


Figure 2.4 Three-level DC-DC converter based on hybrid-based configuration.

2.2.2 Capacitor-based configuration of DC-DC converters

DC-DC boost converters that only considered capacitors as main energy storage are widely used for low power applications [68, 69, 84-88]. In addition, the capacitor should be large enough in order to suppress surge currents during charging and discharging processes of capacitors, and for minimization of capacitor voltage ripple [88, 89]. DC-DC converters with several capacitors as main energy storage can be categorized as a DC-DC switched-capacitor converter type. Generally, the switched-capacitor converter type relies on alternate connection of several capacitors from input to output sides. For an example, a DC-DC switched-capacitor converter might charges two capacitors in series and then discharges those capacitors in parallel. Moreover this converter configuration has limitation on narrow variation ranges of input and output voltages due to inductor-less feature constraint. Thus, this kind of converters usually suitable for low current and low power applications due to high surge current condition occurred during charging and discharging processes of capacitors [88, 90]. As a result, the converter efficiency is degraded.

A three-level DC-DC boost converter based capacitor-based

configuration is considered as an example as shown in Figure 2.5. All components in the circuit are considered ideal. Principally, this converter has two operation modes. During mode-1, the energy from the input side will be transferred to the middle flying C_{fc} . Then during mode-2, the stored energy in the middle capacitor will be transferred to the output side. During charging and discharging operations of the middle capacitor and the output capacitor, high surge current is occurred and large capacitances of the middle capacitor and output capacitor are required in order to suppress the surge current conditions. Consequently the loss due to equivalent series resistance (ESR) of the capacitors is also high although the ripple voltage is small. Meanwhile the three-level DC-DC converter based on hybrid-based configuration has also two operation modes when the boost ratio is 2 (the output voltage is double of the input voltage) as shown in Figure 2.6.

Figures 2.5 and 2.6 show the three-level DC-DC boost converter based on capacitor-based configuration and the three-level DC-DC boost converter based on hybrid-based configuration. Both converters are considered have same specifications of the input voltage 50 V, the output voltage 100 V, the switching frequency 100 kHz and the output power 1000

W. From the simulation results, the three-level DC-DC boost converter based on capacitor-based configuration requires approximately 1000 times larger of the capacitance of the middle capacitor and approximately 50 times larger of the capacitance of the output capacitor compared to the three-level DC-DC boost converter based on hybrid-based configuration.

Figure 2.5 shows that maximum currents of the source and the flying capacitor are still high although very large capacitance of the middle capacitor and large capacitance of the output capacitor are used.

Therefore, the three-level DC-DC boost converter based on capacitor-based configuration requires very large capacitances of the middle capacitor and the output capacitor in order to suppress the surge current during charging and discharging process of the capacitors. Besides, principally capacitor voltage ripples are also reduced when larger capacitance is used.

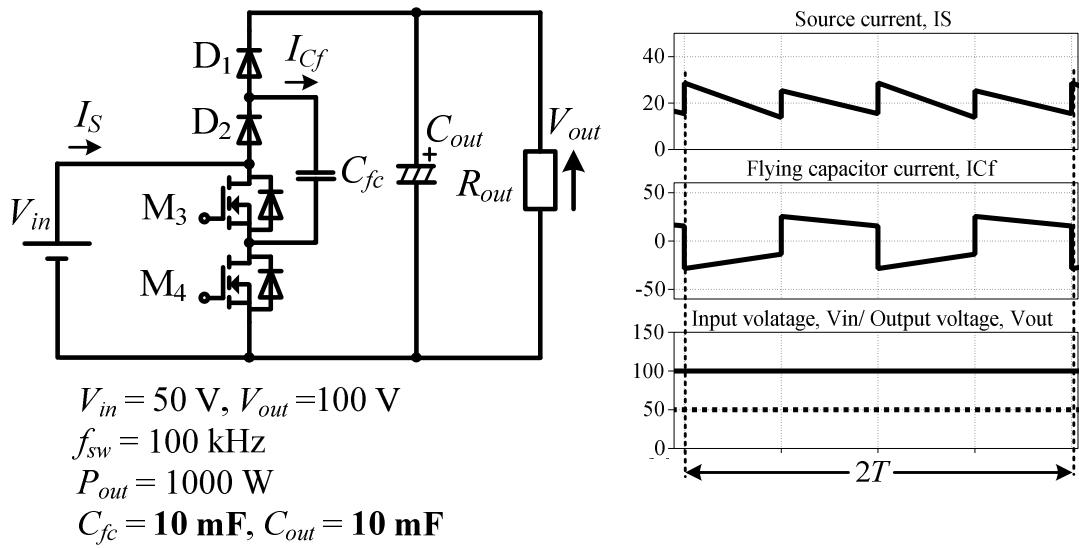


Figure 2.5 Three-level DC-DC converter based on capacitor-based configuration (also known as a inductor-less switched-capacitor configuration).

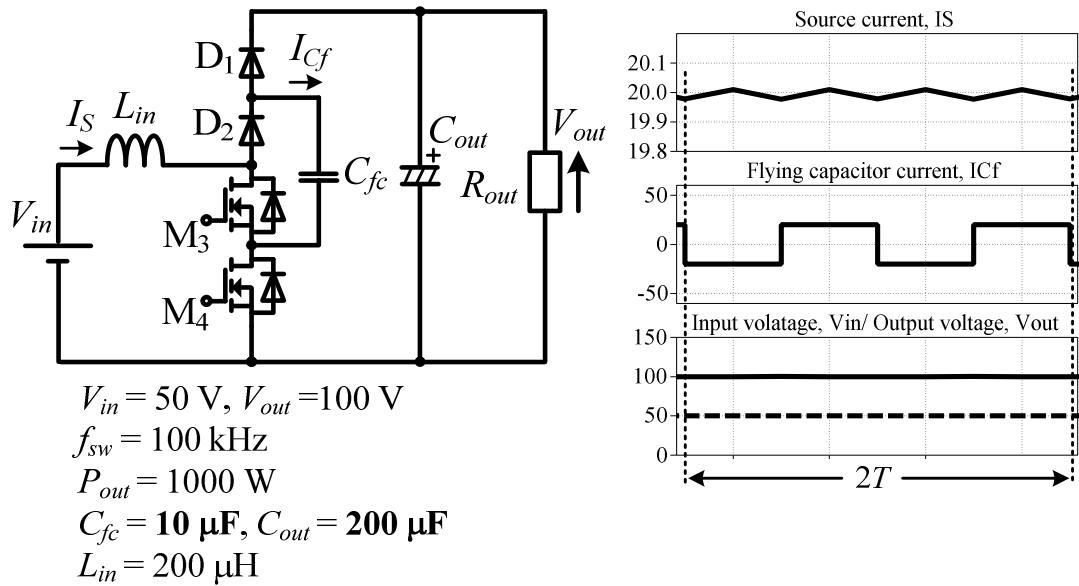


Figure 2.6 Three-level DC-DC converter based on hybrid-based configuration.

2.2.3 Hybrid-based configuration of DC-DC converters

A boost DC-DC converter uses combination of capacitor and inductor components as main energy storage has several advantages, for instances, high power application capability, wide voltage conversion ranges, reduction of high surge current stress, reduction of voltage stress and passive components reduction [79-81].

Sections 2.2.2 (Figure 2.4) and 2.2.3 (Figure 2.6) have described the operation principle and the advantages of the three-level DC-DC converter based on hybrid-based configuration. The unique feature of this hybrid-based configuration is the energy compensating balancing between capacitor and inductor components during transferring process of the energy from the input to the output sides. Consequently the optimization of capacitor and inductor components can be achieved [79].

Table 2.1 shows several generic configurations of DC-DC converters [54, 69, 71, 72, 74, 75, 79-81, 83, 88, 91-93] with common important features are compared. In addition, those selected DC-DC converters are based on magnetic-based, capacitor-based and hybrid-based configurations, respectively. The common features on each generic configuration of the

DC-DC converters are observed. Generally the DC-DC converters based on capacitor-based configuration have low efficiency, but those converters have advantage on high power density feature. Meanwhile the DC-DC converters based on magnetic-based configuration have low power density, however those converters only require few components. On the other hand, the DC-DC converters based on hybrid-based configuration have advantages on several features such as high efficiency and wide voltage conversion ranges. However with the hybrid-based configuration, the converter can be designed according to the application requirements such as devices rating limitation, voltage conversion ratio and efficiency. Thus, power electronics engineers have wide options in selecting the suitable and important features in their converter designs. In addition, the hybrid-based configuration of DC-DC converters have showed a successful history in many power electronics applications and widely used till now.

Table 2.1 Generic configuration of DC-DC converter comparison.

Feature	Generic Configuration of DC-DC Converter		Conventional two-level Boost Converter		Multilevel FCBC (inductor-less)		Multilevel FCFC		Multilevel Modular Capacitor-Clamped (inductor-less)		Multilevel Diode-Clamped		Generalized Multilevel		Cascaded Configuration		Classical Marx Generator		Conventional Marx Topology		Multistage Marx Topology		Coupled-Inductor		Modular Multilevel	
Efficiency	Δ	Δ	O	Δ	O	Δ	Δ	Δ	X	Δ	Δ	O	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ	Δ		
Number of Inductor	1	N/A	1	N/A	1	1	Many	Many	2	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few		
Number of Capacitor	Few	Many	Few	Many	Many	Many	Many	Many	Many	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few		
Number of Diode	Few	Few	Few	N/A	Many	N/A	N/A	Many	Many	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few	Few		
Number of component including switching devices	Few	Many	Many	Many	Many	So Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many	Many		
Boost ratio	Medium	2	High	Medium	High	High	High	Very High	High	High	High	High	High	High	High	High	High	High	High	Very High	Very High	Very High	Very High	Very High		
Modularity	No	No	No	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	No	Yes	No	Yes		
Output Power	High	Low	High	Low	High	High	High	Very High	Very High	Very High	Very High	Very High	Very High	Very High	Very High	Very High	Very High	High	High	High	High	High	High	High		
Power Density	Low	High	Medium	High	Medium	High	Medium	Medium	Medium	Low	Medium	Medium	Medium	Medium	Medium	Medium	Medium	Medium	Medium	Medium	Medium	Medium	Medium	Low		

Symbol: O = Good, Δ = Average, X = Poor, N/A = Not Applicable

2.3 High Voltage and High Boost Ratio of DC-DC Converters

Generally DC-DC converters can be divided into two major groups, i.e., non-isolated and isolated. The isolated DC-DC converter is electrically separated between the input and the output terminals while the input and the output of a non-isolated converter usually share the common ground. Sometimes an isolated DC-DC converter is called isolated ground or galvanic isolated type. Usually, non-isolated DC-DC converters are used in most negative ground application in vehicles and also for various DC powered appliances and equipments. On the other hand, due to small size feature, it allows the converters to be placed physically close to load and the converters also offer performance enhancements. Meanwhile isolated DC-DC converters will have high frequency transformers for providing isolation (barrier) voltage from several hundreds to thousand volts depending on the type of standards. The converters can be used as negative grounded or positive ground or floating ground for various equipments.

Nowadays many researchers actively introduced and developed high voltage gain and high power with high performance of DC-DC converters

with non-isolated configurations [94-98]. Thus due to the advancement of power electronics fields, non-isolated DC-DC converters are applicable for high power and high voltage gain applications, such as for renewable energy system, electric vehicles (EV) charging and micro-grid system.

Figure 2.7 shows the non-isolated and isolated DC-DC converters groups in terms of voltage and boost ratio features. Furthermore, several generic non-isolated DC-DC converters are selected for comparisons as shown in Figure 2.7. In non-isolated group, a conventional two-level DC-DC converter has less capability of high boost ratio and high voltage due to circuit structure limitation. Meanwhile DC-DC converters with multilevel and multistage structures such as a multistage Marx topology boost converter and a multilevel flying capacitor boost converter show superior in high boost ratio and high voltage capabilities. Besides, those multistage and multilevel structures of DC-DC converters can be improved for better performance in high voltage and high boost ratio due to advancement of power converters technologies.

On the other hand, isolated DC-DC converters offer very high boost ratio and very high voltage capabilities due to the existing of isolation

transformers [16, 99-105]. The isolated DC-DC converters configurations usually for the application that requires isolation as a main safety feature such as for an interface between main grid and loads or other converters. Several topologies of isolated DC-DC converter are compared as shown in Figure 2.7. Therefore in order to obtain high boost ratio and high output voltage in DC-DC converters, both groups, non-isolated and isolated can be considered.

In this thesis, DC-DC converters with multilevel and multistage structures are considered in order to achieve high conversion ratio of voltage with reduction of voltage stresses on switching devices. Specifically, in these studies multilevel flying capacitor DC-DC converters and the multistage Marx topology DC-DC converters types are focused and concerned. In addition, those converters types are based on hybrid-based configurations.

On the other hand, from Figure 2.7, generally the multilevel FCBC is suitable for medium to high conversion ratio of voltage and for medium to high voltage applications, such as for electric vehicle (EV) and photovoltaic (PV) systems. However, it depends on circuit structure designs

in order to enhance the boost ratio capability feature. Meanwhile, the multistage MTBC is suitable for high conversion ratio of voltage and also suitable for high voltage applications, such as for micro-grid and datacenters systems. In these applications, high boost ratio DC-DC converters are required. In addition, as discussed in Section 2.2, the multistage structure has capability to achieve high conversion ratio of voltage due to the advantage of series connection of several capacitors.

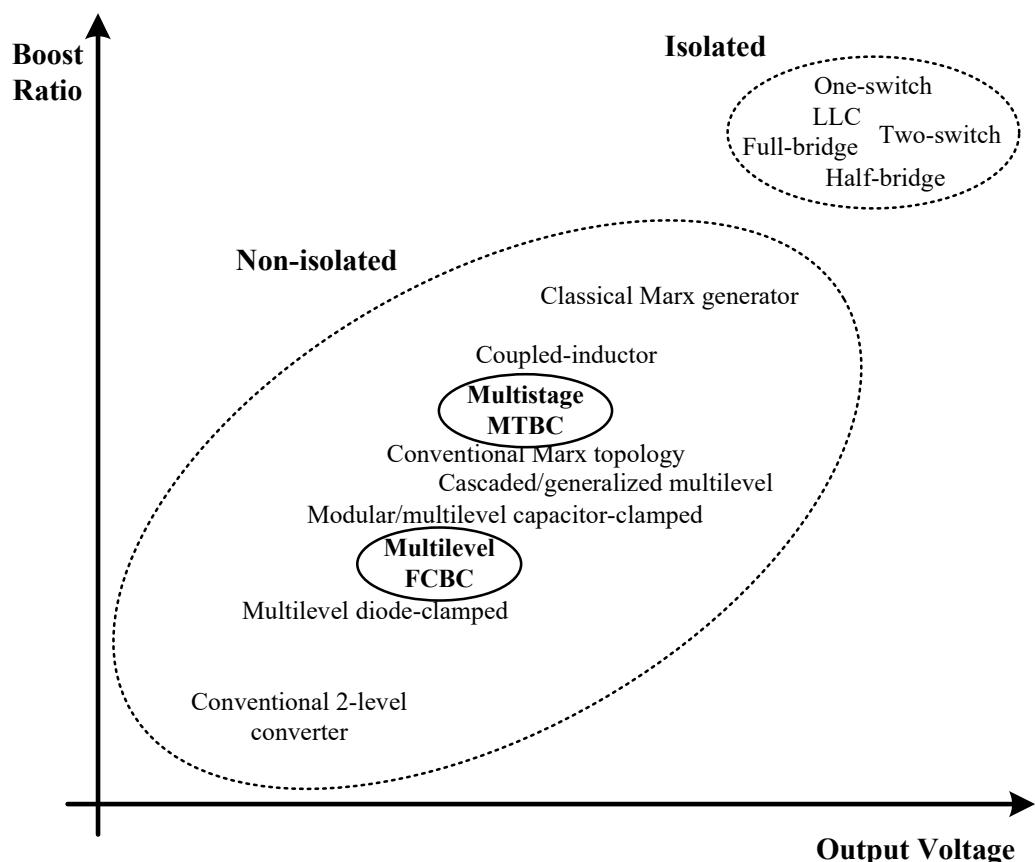


Figure 2.7 Generic non-isolated and isolated DC-DC converters in terms of boost ratio and voltage features.

2.4 Multilevel and Multistage Structures of DC-DC

Converters based on Magnetic-based,

Capacitor-based and Hybrid-based Configurations

Multilevel and multistage structures of DC-DC converters have attracted interest in power converter technologies due to several benefits and advantages over conventional two-level DC-DC converters [51-53, 93]. Those multilevel and multistage structures of DC-DC converters have unique features and it usually designed based on application requirement specifications.

On the other hand, multilevel and multistage structures have shared some common features such as voltage stress reduction, current stress reduction and passive components reduction. Furthermore these features usually give significant impact on converter efficiency and performance as well as on converter design specifications.

For discussions, several switched-capacitor structures of DC-DC converters which are based on the capacitor-based and hybrid-based configurations are compared in details in order to evaluate their features and behaviors. On the other hand, several high conversion ratio of voltage

of DC-DC converter structures which are based on magnetic-based and hybrid-based configurations are discussed and compared in details as well.

2.4.1 DC-DC converters with switched-capacitor structure

In this section, clarifications of DC-DC boost converters based on capacitor-based and hybrid-based configurations are compared and discussed. In addition, several switched-capacitor topologies of DC-DC converters are considered in terms of their features and behaviors. Figures 2.8(a), 2.8(b) and 2.8(c) show the conventional three-level switched-capacitor, the resonant three-level switched-capacitor and the three-level flying capacitor of DC-DC converters, respectively. Those selected converters have multilevel feature structures.

However the conventional three-level switched-capacitor DC-DC converter (CSCC) has no magnetic element and it has been widely used for low power applications with small size, lightweight and high power density features. This converter is considered as capacitor-based configuration category whereby, the maximum output voltage is limited only double of the input voltage. The conventional switched-capacitor DC-DC converter

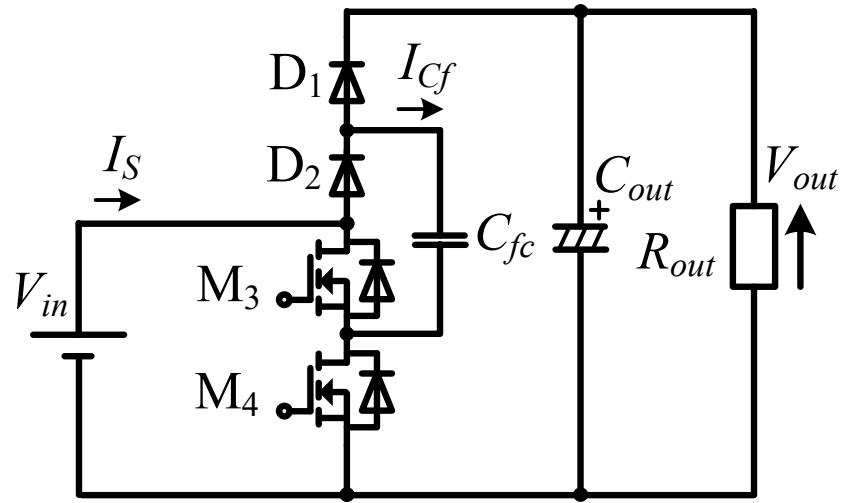
usually suffers from high surge current during charging and discharging processes of capacitors and it contributes to the high switching loss and high conduction loss [106, 107]. Thus, due to these drawbacks, this converter usually limited for low power applications.

In order to solve the surge current problem on the conventional three-level switched-capacitor DC-DC converter, soft-switching technique [90] and several types resonant switched-capacitor DC-DC converter have been introduced [71, 106-110]. By introducing resonant switched-capacitor DC-DC converters, the surge current is suppressed and converter efficiency is improved. Figure 2.8(b) shows the resonant three-level switched-capacitor DC-DC converter (RSCC) types. Although the surge current problem is considered solved, the output voltage range is still limited to double of the input voltage. In addition, the magnitude of maximum input current becomes high due to soft switching condition. Consequently high current rating of components and devices must be selected especially semiconductor devices.

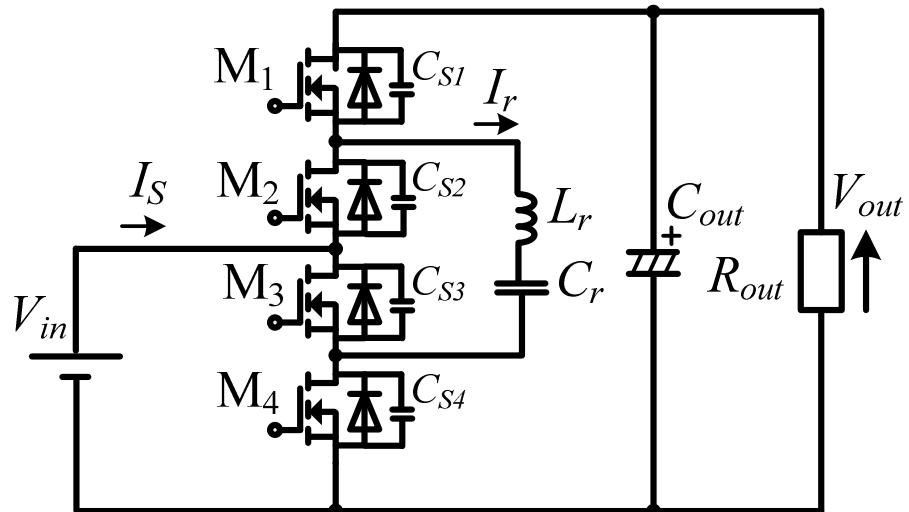
Therefore, in order to increase the input and the output voltage ranges, as well as to reduce the magnitude of maximum input current, a flying

capacitor DC-DC converter is introduced [72, 79-81] whereby it has an inductive element at the input side and based on switched-capacitor converter topology. Figure 2.8(c) shows the three-level flying capacitor DC-DC boost converter (FCBC) based on hybrid-based configuration. Principally, the energy will be transferred from the input inductor to the flying capacitor and then to the output side, thus a small input inductor and a small flying capacitor can be considered in this converter. The transferred energy from the input to the output sides are compensated between the input inductor and the flying capacitor components. Besides, the input and the output voltage ranges are wide. In addition, minimization of the input inductor and small flying capacitor considerations are achieved.

Therefore the three-level flying capacitor DC-DC boost converter (FCBC) which is based on hybrid-based configuration has advantages on wider input and output voltages ranges, maximum input current reduction, and suitable for high power applications as compared to the conventional three-level switched-capacitor DC-DC converter (CSCC) and the resonant three-level switched-capacitor DC-DC converter (RSCC).

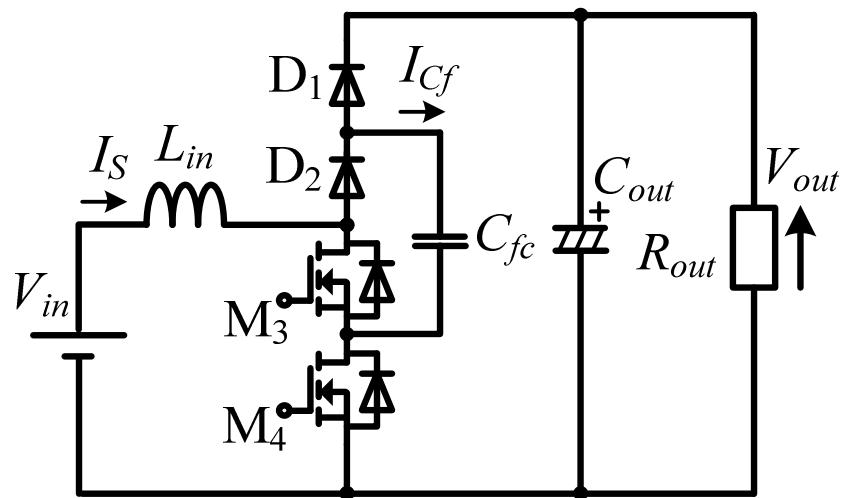


(a) Conventional three-level switched-capacitor DC-DC boost converter (inductor-less) (CSCC).



(b) Resonant three-level switched-capacitor DC-DC boost converter (RSCC).

Figure 2.8 DC-DC boost converter based on capacitor-based and hybrid-based configurations.



(c) Three-level flying capacitor DC-DC boost converter (FCBC).

Figure 2.8 DC-DC boost converter based on capacitor-based and hybrid-based configurations.

2.4.2 DC-DC converters with high boost ratio structure

Then, in this section, clarifications of DC-DC boost converters based on magnetic-based and hybrid-based configurations are compared and discussed. Several topologies of DC-DC converters with high boost ratio and interleaved topologies are compared and analyzed in terms of their features and behaviors. Figures 2.9(a), 2.9(b), 2.9(c) and 2.9(d) show the interleaved three-phase DC-DC converter (IC), the six-cell modular multilevel DC-DC converter (MMC), the two-stage cascaded Marx DC-DC converter (CMC) and the three-stage Marx topology DC-DC boost converter (MTBC), respectively. Those converters have multilevel and multistage features structures. These converters are usually suitable for high power applications due to the existing of magnetic components in the converters.

Figure 2.9(a) shows the three-phase interleaved DC-DC converter (IC) whereby this converter based on the magnetic-based configuration. This converter is fundamentally from the conventional two-level DC-DC boost converter (CBC) circuit structure. If high boost ratio is considered, the conventional two-level boost converter (CBC) is suffered from high current

stress at the input side due to low input voltage and high voltage stress at the output side due to high output voltage. Thus the interleaved topology of DC-DC converter is introduced in order to reduce the maximum current stress at the low voltage side. Unfortunately, with this topology, high output voltage is difficult to be achieved due to the circuit structure limitation.

Several non-isolated DC-DC converters with high boost ratio capability are introduced by many researchers and some of the proposed circuits are based on coupled-inductor topology [74, 111-116]. Figures 2.9(b) and 2.9(c) show the six-cell modular multilevel DC-DC converter (MMC) and the two-stage cascaded Marx DC-DC converter (CMC), respectively whereby these topologies can achieve high conversion ratio of the output voltage without coupled-inductor consideration. Both converters applied resonant conditions in order to reduce switching loss and surge current. In addition, both circuits have considered inductive elements at the low voltage and high voltage sides. Furthermore, both converters have a drawback of high current stress at the low voltage side.

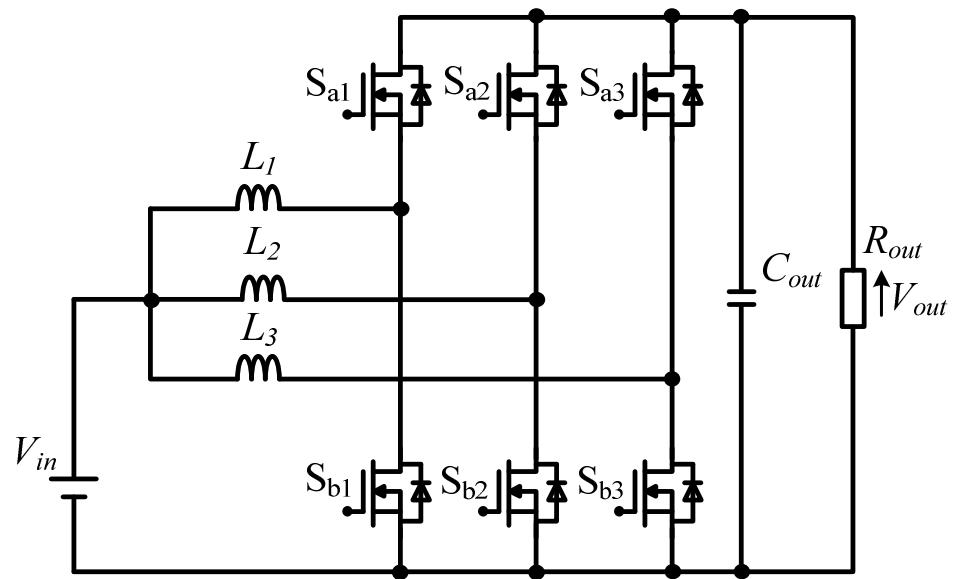
Meanwhile Figure 2.9(d) shows the three-stage Marx topology DC-DC boost converter (MTBC). This topology has several similar features with

the six-cell modular multilevel DC-DC converter (MMC) (Figure 2.9(b))

and two-stage cascaded Marx DC-DC converter (CMC) (Figure 2.9(c)).

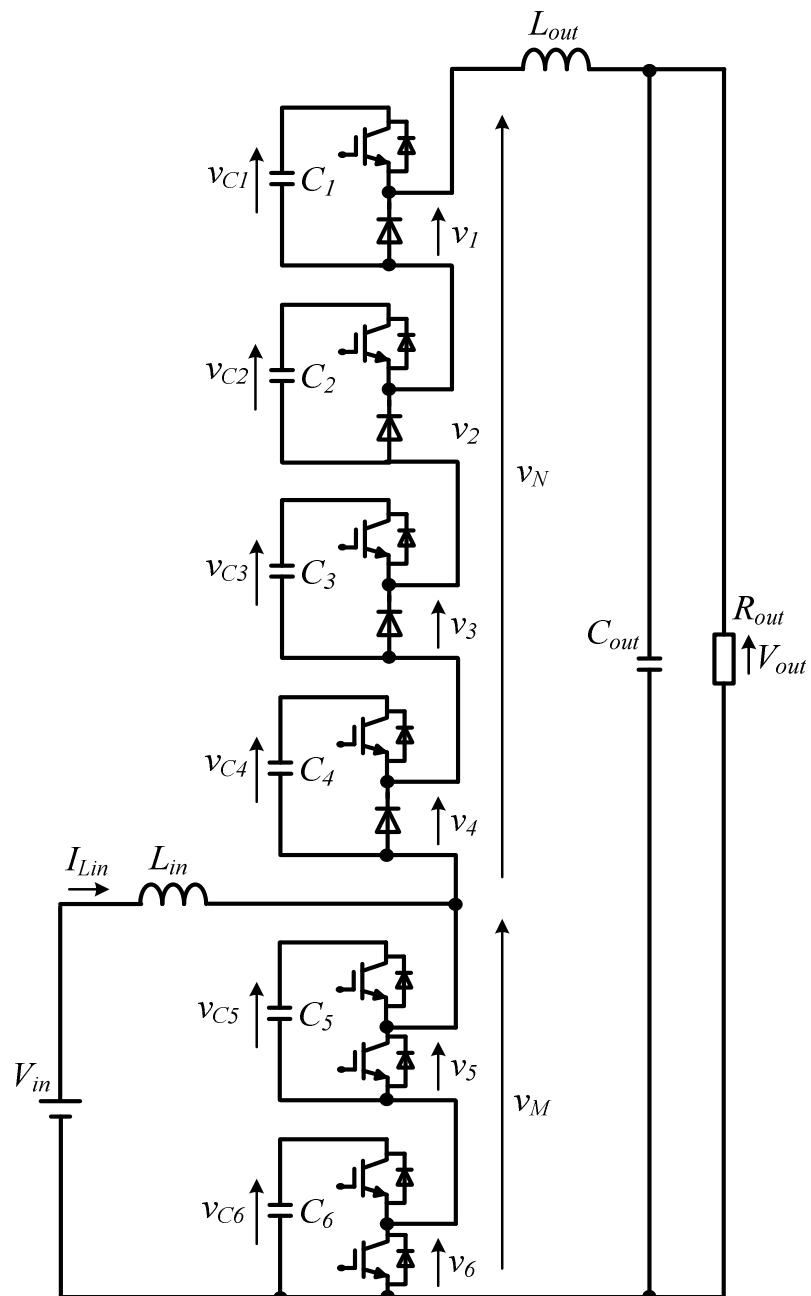
Whereby, those converters have inductive elements at the low voltage and high voltage sides, respectively. In addition the attractive feature of those converter structures is charging and discharging processes of capacitors in parallel-series arrangement in order to obtain high conversion ratio of voltage. The three-stage Marx topology DC-DC boost converter (MTBC) has an advantage of low current stress at the low voltage side due to parallel connection of the stage capacitors. Obviously, the input current stress is reduced according to the number of stages.

Therefore by considering multilevel and multistage circuit topologies based on hybrid-based configurations, many benefits are evaluated and those benefits can be suited for micro-grid system and industrial loads requirement.



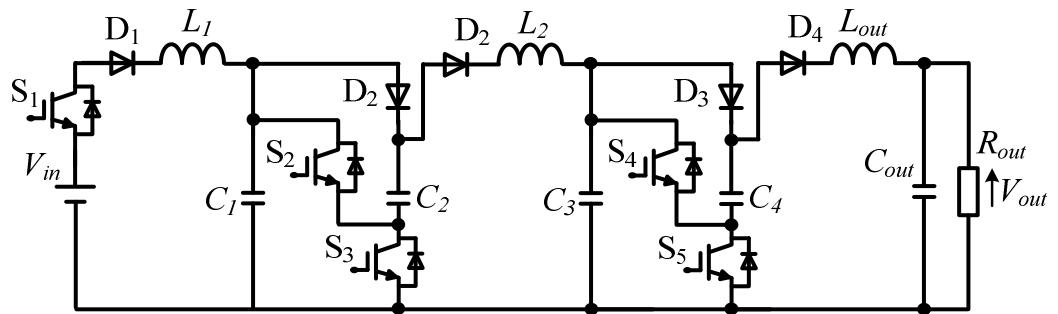
(a) Three-phase interleaved DC-DC converter (IC).

Figure 2.9 DC-DC converters based on magnetic-based and hybrid-based configurations.

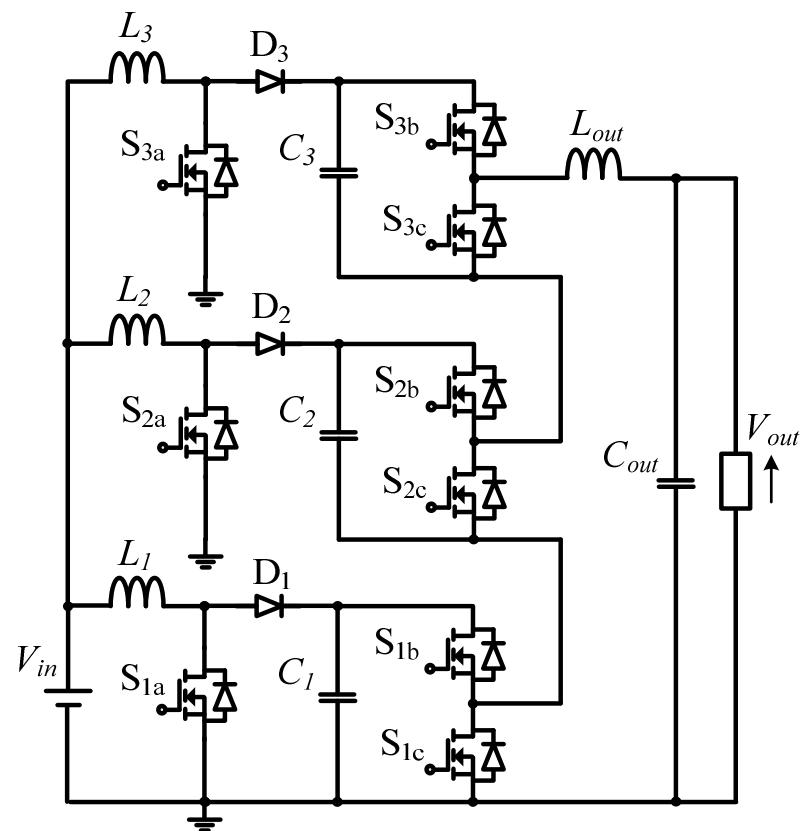


(b) Six-cell Modular multilevel DC-DC converter (MMC) [74].

Figure 2.9 DC-DC converters based on magnetic-based and hybrid-based configurations.



(c) Two-stage cascaded Marx DC-DC converter (CMC) [92].



(d) Three-stage Marx topology DC-DC boost converter [117].

Figure 2.9 DC-DC converters based on magnetic-based and hybrid-based configurations.

2.4.3 Review on the proposed converter features

Table 2.1 and Figure 2.7 show the comparison among generic DC-DC converters. Generally DC-DC boost converters are based on magnetic-based, capacitor-based and hybrid-based configurations. Many researchers agreed that the capacitor-based configuration is the attractive option in order to achieve high power density. However, the hybrid-based structure is still dominant due to the superior features on flexibility, reliability, high power, high efficiency and high performance. Thus, multilevel and multistage structures based on hybrid-based configuration are selected in order to overcome the following issues.

- (i) Passive components reduction in terms of size, volume and weight.
- (ii) Current stress reduction at low voltage side and voltage stress reduction on components and devices especially semiconductor devices.
- (iii) High conversion ratio of voltage capability.

Two topologies of DC-DC boost converters have considered in this study, i.e., flying capacitor topology and Marx topology, whereby these

topologies have applied the multilevel and multistage structures.

Many studies have shown interests on passive components reduction in DC-DC converters for high power density achievement, i.e., capacitor and inductor components. Unfortunately most researchers do not provide concrete evidences in order to design those components in optimum. Thus, in this study, the reduction of inductance and core volume of the inductor are achieved by considering the maximum product of inductor voltage V_L and charging time of inductor T_L in the multilevel flying capacitor DC-DC boost converter (FCBC) is proposed. In addition, the small capacitance of the flying capacitor is also considered and evaluated.

In order to investigate the hybrid-based configuration of DC-DC boost converter for high voltage applications, a high boost ratio DC-DC converter based on Marx topology configuration is proposed. The advantage of this Marx topology is the parallel-series connections arrangement of the stage capacitors is adopted in order to generate high voltage at the output side from low voltage at the input side. In addition, the parallel connection of the stage capacitors and then series connection of the same stage capacitors give advantages on the current stress and voltage stress reductions at the

low voltage side and on the switching devices at the high voltage side, respectively. Thus this topology has attractive features on high voltage and high power applications. In addition, interleaved operation is also considered in order to achieve volume reduction on the output inductor. The details design and operation of the proposed converters are discussed and explained in Chapters 3, 4 and 5.

2.4.4 Power Density Evaluation

Power density of power converters is one of the important parameter need to be considered especially when space and size are the critical considerations. Thus, power density characteristics of designed converters need to be identified clearly. On the other hand, Pareto-front curve method is one of the easier method can be used in order to map out power density characteristics of the designed converters. Basically two parameters, i.e., converter efficiency and power density of the designed converters are considered in the Pareto-front curve. From this characteristic, maximum power density with respect to converter efficiency can be evaluated. Figure 2.10 shows the general Pareto-front curve with efficiency and power

density evaluation parameters.

Generally, in order to obtain the highest power density of any designed converters, higher switching frequency need to be considered and as a trade-off, switching loss will be increased although passive component volumes are reduced. Thus, usually maximum efficiency and maximum power density are the trade-off features.

In this study Pareto-front curve method is used in order to evaluate power density characteristics of the designed converters with respect to converter efficiency. As a result, power density boundary of the designed converters can be obtained and evaluated.

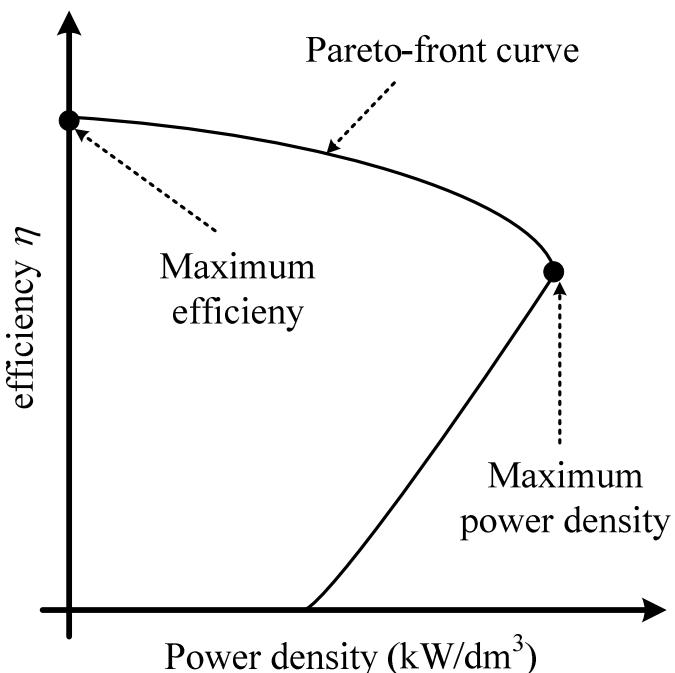


Figure 2.10 General Pareto-front curve.

2.5 Conclusion

In this chapter, DC-DC converters based on magnetic-based, capacitor-based and hybrid-based configurations have clarified and discussed. Basically, the magnetic-based configuration needs very large inductor in order to transfer energy from input to output sides [51-53, 67]. As a result, the converter becomes bulky. Meanwhile, DC-DC converters based on the capacitor-based configuration has problem with high surge current and requires very large capacitor in order to suppress surge current during charging and discharging processes of capacitors. Thus the applications of this converter are limited for low power applications [71, 84, 86, 87]. However several studies have been shown that with this configuration, the converter can be used for medium power application by applying zero current switching (ZCS) method, but the application ranges are still limited [69, 88].

Furthermore, by considering the hybrid-based configuration of DC-DC converters, many studies have been successfully introduced and implemented many converter topologies in order to achieve high performance operation with reduced passive components at high voltage

and high power applications [54, 56, 72, 74, 79-81, 92, 118-120]. In addition, the hybrid-based configuration of DC-DC converters must be coupled with multilevel structure or multistage structure configurations in order to gain and optimize the benefits of these combinations. The benefits, such as passive components reduction, current stress reduction at low voltage side, voltage stress reduction on components especially semiconductor devices and high conversion ratio of voltage capability achievement will give significant impact on converters performance and operation.

Figure 2.11 shows the several converter topologies with multilevel structures and based on hybrid-based configurations whereby those converters have similar structure and feature compared to the multilevel flying capacitor DC-DC boost converter (FCBC). Although the resonant switched-capacitor converter (RSCC) able to suppress surge currents and needs few switches, however this topology is still suffers from narrow voltage regulation. Besides, the coupled-inductor DC-DC converter (CIC) [121] also need few switches in order to achieve wide voltage regulation. However, this converter topology needs large coupled-inductor especially

when it applies in high power applications and voltage stress on switching devices are also high due to single stage structure especially at the output side. Basically, the isolated multilevel resonant converter (IMRC) [122] has ability in wide voltage range operation, but it needs many switches and other components. On the other hand, the MMC, MMCCC and GMC have also limitation on voltage regulation due to the resonant condition. However, for these converter topologies the medium to wide voltage regulation can be achieved by increasing switches and other components. In addition, additional circuits might be required. Besides, the multilevel flying capacitor DC-DC boost converter topology has advantages on wider voltage regulation and requires fewer switches.

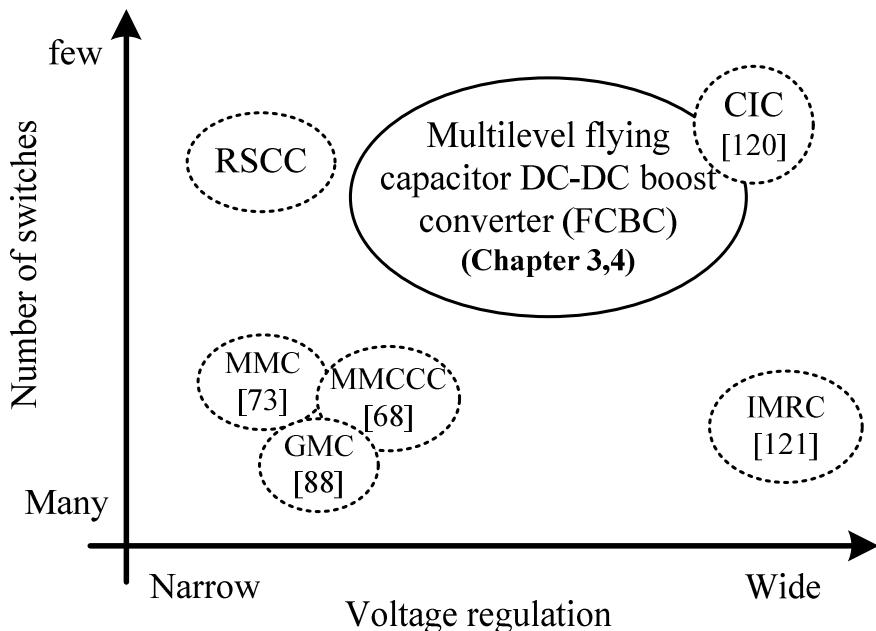
Moreover, Figure 2.12 shows the several converters topologies with multistage and multiphase structures whereby those converters have similar features compared to the multistage Marx topology DC-DC boost converter (MTBC). Basically, the conventional two-level DC-DC converter (CBC) and the interleaved multiphase DC-DC converter (IMC) have capabilities of medium boost ratio variation with only single output capacitor. Meanwhile the cascaded Marx DC-DC converter (CMC) and the modular

multilevel DC-DC converter (MMC) have limitation on wide variation on boost ratio. However, with these converters topologies, the wide variation on boost ratio can be achieved by considering additional capacitors and additional circuit structures as well. On the other hand, the multistage Marx topology DC-DC boost converter (MTBC) has capability of increasing the output voltage by varying the duty ratio or/and by considering additional capacitors. Thus, the significant advantages of the multistage MTBC are the flexibility on stages increment for increasing the output voltage and the ability of controlling the output voltage with variation of the input voltages.

Therefore, by considering multilevel and multistage structures of DC-DC converters based on hybrid-based configurations, several benefits are confirmed by referring to the DC-DC converters based on capacitor-based and magnetic-based configurations. In addition, the multilevel flying capacitor DC-DC boost converter (FCBC) and the multistage Marx topology DC-DC boost converter (MTBC) have depicted several advantages over other converters topologies.

In this study, the multilevel flying capacitor DC-DC boost converter (FCBC) with passive components reduction is proposed. In addition the

effectiveness of the small capacitance of the flying capacitor is confirmed and evaluated. As a result, the weight, size and volume are reduced. In order to further evaluate of the hybrid-based configuration of DC-DC converters, a multistage Marx topology DC-DC boost converter (MTBC) with high conversion ratio of voltage capability is proposed. The proposed converter is adopted from the Marx impulse generator circuit structure whereby parallel connection of capacitors at low voltage side and then series connection with the same capacitors in order to generate high voltage at the output side. In addition this proposed converter has several advantages in terms of current stress at low voltage side and voltage stress reduction on circuit components especially semiconductor devices. In addition, an interleaved operation is also introduced in order to achieve passive component reduction.



*RSCC = Resonant switched-capacitor DC-DC converter

*MMCCC = Multilevel modular capacitor-clamped DC-DC converter

*GMC = Generalized multilevel DC-DC converter

*MMC = Modular multilevel DC-DC converter

*CIC = Coupled-inductor DC-DC Converter

*IMRC = Isolated multilevel resonant converter

Figure 2.11 The advantages of flying capacitor topologies over conventional switched-capacitor and resonant switched-capacitor topologies.

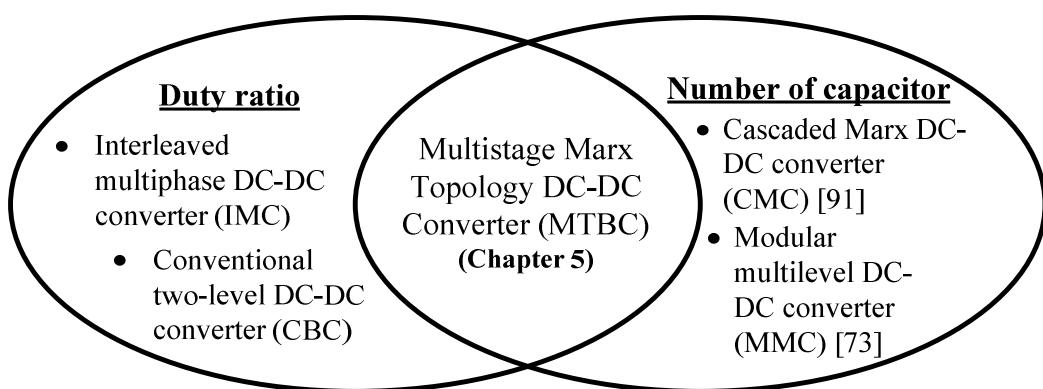


Figure 2.12 The advantages of Marx topology boost converter compared to the interleaved DC-DC converter, cascaded Marx DC-DC converter and modular multilevel DC-DC converter

Chapter 3

Design and Implementation of the Three-Level Flying Capacitor Boost Converter with Reduced Inductor and Small Flying Capacitor

3.1 Introduction

In general, as a power converter, the DC-DC boost converter is important in high-power-capacity applications, such as solar electric systems and electric vehicle systems. These types of applications typically demand high conversion efficiency with low weight, volume, and cost of the converter. Nevertheless, if a conventional DC-DC boost converter (CBC) is considered, the bulkiness of the input inductor must be taken into consideration because a typical conventional DC-DC boost converter requires large inductors for energy storage, especially for

continuous-current-mode operation of the input current. Although conventional DC-DC boost converters are evolving due to these drawbacks, the flying capacitor DC-DC boost converter (FCBC) has become a possible option. The FCBC with an input inductor has several advantages over a conventional DC-DC boost converter. The FCBC requires only a small input inductor and the suppression of an input inrush current due to the existing of an input inductor compared to a conventional FCBC without an input inductor [80, 81, 88, 93].

In addition, a number of researchers have reported that interleaved circuit topologies can be considered for conventional DC-DC boost converters. As a result, the input current can be reduced based on the number of interleaved circuits. Consequently, the inductance and core volume of the input inductors can be reduced [118, 123-128]. Moreover, by considering multilevel structure topologies on the FCBC, the inductance and core volume of the input inductors can also be reduced [80, 81, 88, 93]. However, the interleaved circuit topology and multilevel circuit structure introduce circuit complexity. Furthermore, such topologies require additional inductors, capacitors, and switching devices, as well as other

components and devices. Nevertheless, if a very-high-efficiency DC-DC boost converter is critical, regardless of size and weight, such topologies might be an option [80, 81, 118, 123-128].

Therefore, for single-phase operation and simplicity of the converter circuit, the FCBC offers a good option due to the need for fewer passive components and switching devices. In addition, by considering appropriate designs of the passive components and devices, the sizes and volumes of the components and devices can be minimized.

As in the case of a conventional DC-DC boost converter, the output voltage in the FCBC can be controlled by controlling the duty ratio of the switching signals. One important feature of the FCBC is that the boost-up energy is transferred from the flying capacitor to the output side, which means that the input inductor can be designed with small inductance and a reduced inductor core volume [79-81]. Consequently, the overall size and weight of the input inductor can be greatly reduced as compared to a conventional DC-DC boost converter [79, 81, 88, 129, 130]. Moreover, the power loss in terms of copper loss is also reduced as a result of fewer winding of the input inductor. Generally, passive components and devices

in the FCBC, i.e., the input inductor, the flying capacitor, and the output capacitor, must be designed correctly because these components will have a significant impact on converter operation and efficiency. However, this has not been clarified in previous studies [80, 82, 88, 93, 129, 131].

Moreover, establishing the relationship between the capacitance of the flying capacitor and the output voltage ripple is also important. Unfortunately, this has not been discussed in other studies [80, 81, 88, 132, 133]. Converter circuit components/devices and electrical parameters are significantly related. Therefore, procedures for device estimation and design must be established. Generally, the output voltage ripple should be considered as a factor that influences the estimation of the capacitance of the flying capacitor in the FCBC [51, 52]. Hence, the parametric relationship between the capacitance of the flying capacitor and the output capacitance from the output voltage ripple must to be analyzed. In this section, an FCBC is proposed considering a small capacitance of the flying capacitor in order to reduce the size of the power converter. Principally, a small capacitance of the flying capacitor causes a large voltage ripple across the flying capacitor. In contrast, the voltage stress increases when a

small capacitance of the flying capacitor is used. However, low-power-loss and high-voltage power devices, such as SiC-MOSFETs, have recently been developed [63-66, 134]. Thus, downsizing is a higher priority than the use of low-voltage-stress switching devices. Moreover, ideally, the voltage stress of the switching devices in the FCBC becomes half that of a two-level DC-DC boost converter. Based on this argument, a small capacitance of the flying capacitor in the FCBC is possible to be considered. Moreover, the discussion is focused on issues related to the input inductor and flying capacitor. In particular, the author focuses on the input inductor design and establishing the relationship between the capacitance of the flying capacitor and the output voltage ripple. First, the principle of the FCBC is described. Then, the input inductor design in terms of inductance and inductor core volume is discussed. The parametric relationship between the flying capacitor and output capacitor is discussed considering the output voltage ripple. Experimental and simulation results are analyzed and discussed in order to confirm the validity of the design parameters. Besides, power density comparisons between two-level CBC and three-level FCBC are conducted theoretically.

3.2 Principle of Flying Capacitor Boost Converter (FCBC)

Figure 3.1(a) shows a conventional DC-DC boost converter (CBC) (also known as a two-level CBC). In a conventional DC-DC boost converter, the boost input inductor volume is large. Figure 3.1(b) shows a three-level FCBC with a function for output voltage control and unidirectional operation. Basically, the FCBC consists of two diodes, two switches (MOSFET), an input inductor L , a flying capacitor C_{fc} , and an output capacitor C_{out} . The input inductor allows the output voltage of the FCBC to be controlled independently by controlling the duty ratio D . In addition, if the input inductor is not considered, the maximum output voltage is double the input voltage V_{in} . The relationship between V_{in} and the output voltage V_{out} is expressed as follows:

$$V_{out} = \beta V_{in} \quad (3.1)$$

where the boost ratio β is expressed as

$$\beta = \frac{1}{1-D} \quad (3.2)$$

Figure 3.2 shows the switching patterns of the FCBC. The switching signal is generated by two carrier signals with half the switching period T

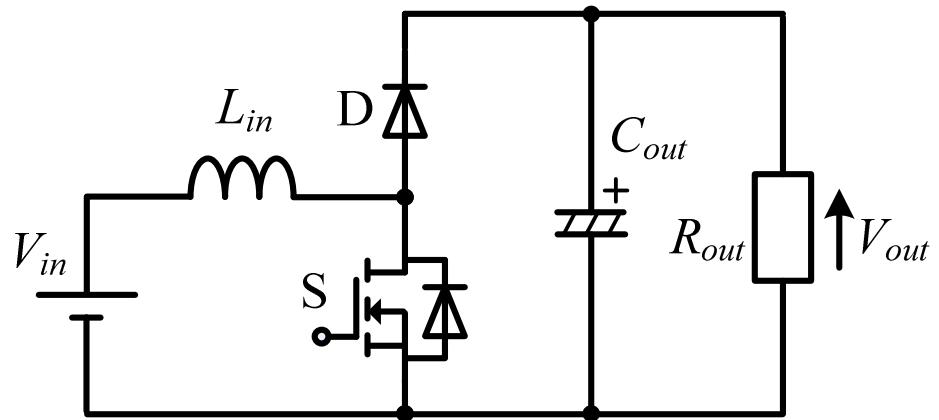
delay between the signals. Half of the switching period T delay is needed in order to balance the charging and discharging times of the input inductor in one switching period T . The charging time of the input inductor is determined by the duty ratio D and both carrier signals.

In the FCBC, the duty ratio D is a value in the range of $0 \leq D \leq 1$. If the duty ratio D is set at 0.25, meaning that only 25% of the switching period T is activated. If the FCBC topology is referenced, M_3 and M_4 will receive only ON pulse widths at 25% of the switching period T . Meanwhile, the D_1 and D_2 pulse widths are opposite the M_4 and M_3 pulses width, respectively, as shown in Figure 3.2.

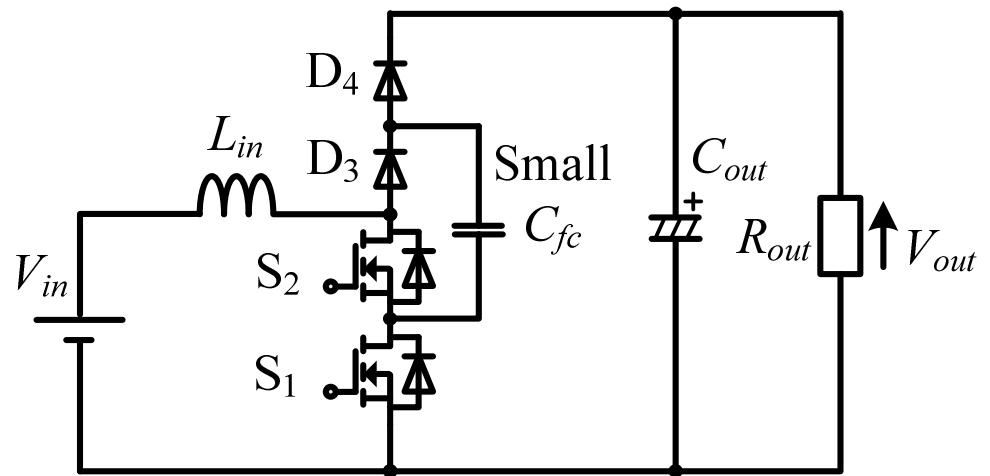
Figure 3.3 shows the operation mode of the FCBC in circuit diagram form. Table 3.1 summarizes the operation mode and the range of β in the FCBC. The maximum required output voltage of the three-level FCBC in the present paper is twice that of the input voltage. Therefore, only the boost ratio in the range of $0 < \beta \leq 2$ is considered.

Table 3.1 Operation mode and boost ratio.

Modes of operation	Boost ratio, β
(I), (II), and (III)	$0 < \beta \leq 2$



(a) Two-level CBC.



(b) Three-level FCBC.

Figure 3.1 DC-DC boost converters.

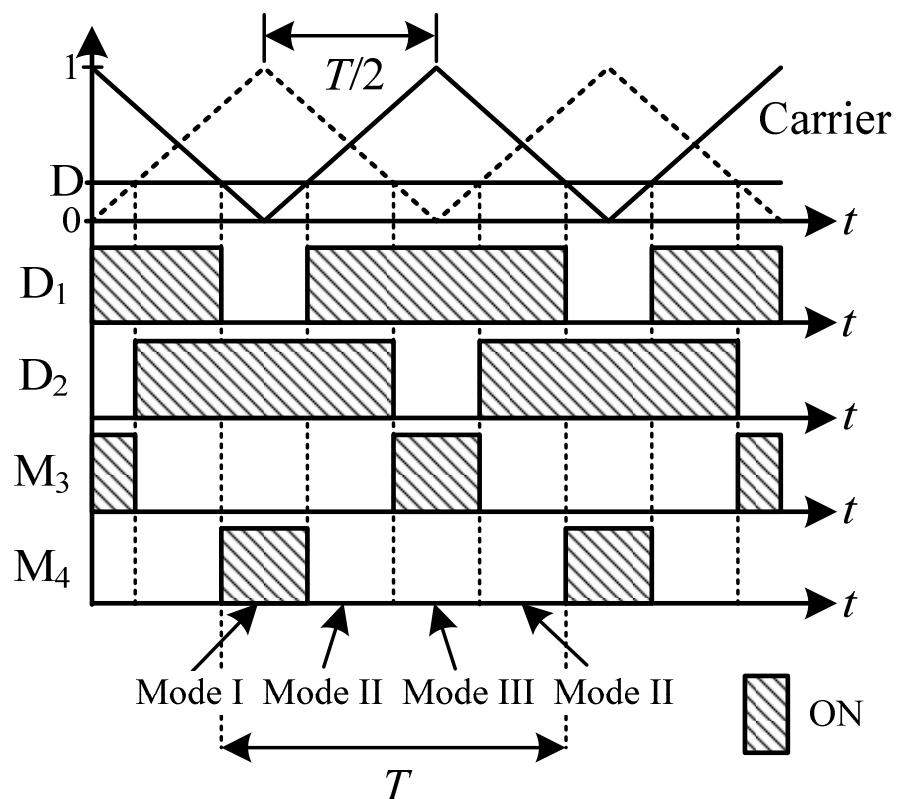


Figure 3.2 Switching pattern of the three-level FCBC.

3.3 Inductor Design

In this section, the inductor design principle is discussed. The parameters of the FCBC circuit are determined according to the specifications shown in Table 3.2. Note that the inductor design is discussed under the assumption of a constant flying capacitor voltage. The validity of this assumption is discussed in Section 5.

3.3.1 Inductance of an input inductor

In order to determine the appropriate inductance of an input inductor L , the desired inductor current ripple ΔI_L is required. For design purposes, it is useful to express the inductance of the input inductor L in terms of the desired inductor current ripple ΔI_L . Ideal characteristics of the switching devices are considered, whereby ripples on the output voltage V_{out} and flying capacitor voltage V_{fc} are ignored due to the independent relationship between the inductor current ripple and capacitance variation of the flying capacitor, as discussed in Section 5.3. Generally, the inductance of an input inductor L can be designed by considering the inductor current ripple ΔI_L as expressed as follows:

$$\Delta I_L = V_L \frac{T_L}{L} \quad (3.3)$$

where T_L is the charging time of the inductance of an input inductor, and V_L is the inductor voltage. The inductor current ripple is maximum when the product of T_L and V_L is maximum, as expressed by Eq. (3.3).

In a conventional DC-DC boost converter, the maximum inductor current ripple occurs when the duty ratio D is 0.5 ($\beta = 2$). Under this condition, the charging time of the input inductor becomes half the switching period T , and the inductor voltage is equal to half the output voltage V_{out} . Therefore, the inductance of an input inductor $L_{conventional}$ for a conventional DC-DC boost converter can be expressed as follows:

$$L_{conventional} = \frac{V_{out}}{2} \frac{T}{2} \frac{1}{\Delta I_L} \quad (3.4)$$

In the FCBC, the maximum inductor current ripple occurs for duty ratios of 0.25 ($\beta = 1.33$) and 0.75 ($\beta = 4$). Figure 3.4 shows the relationship between the product of T_L and V_L and the duty ratio D in the FCBC. Hence, the inductance of an input inductor L_{FCBC} in terms of the desired inductor current ripple ΔI_L can be expressed as follows:

$$L_{FCBC} = \frac{V_{out}}{4} \frac{T}{4} \frac{1}{\Delta I_L} \quad (3.5)$$

Referring to Eq. (3.5), the inductor voltage in the FCBC becomes half

that of a conventional DC-DC boost converter or a quarter of the output voltage V_{out} . Meanwhile, the charging time of the input inductor in the FCBC becomes half that of a conventional DC-DC boost converter or one quarter of the switching period T .

By considering an FCBC and a conventional DC-DC boost converter having the same output voltage, switching frequency and inductor current ripple ΔI_L , the ratio of the inductances of the input inductor between the FCBC and the conventional DC-DC boost converter can be expressed as follows:

$$\frac{L_{FCBC}}{L_{conventional}} = 0.25 \quad (3.6)$$

Thus, referring to Eq. (3.6), the FCBC requires approximately 25% of the inductance of an input inductor, as compared to the conventional DC-DC boost converter, as shown in Figure 3.1(a).

Therefore, the inductance of an input inductor can greatly be reduced for the FCBC topology. Theoretically, the inductance of an input inductor is proportional to the number of windings. Therefore, the copper loss of an input inductor is also reduced.

Table 3.2 FCBC Specifications.

Parameters	Value
Input voltage V_{in}	262.5 V
Output voltage V_o	350 V
Output power P	1 kW
Inductor/Input current I_{in}	4.24 A
Switching frequency f_{sw}	100 kHz

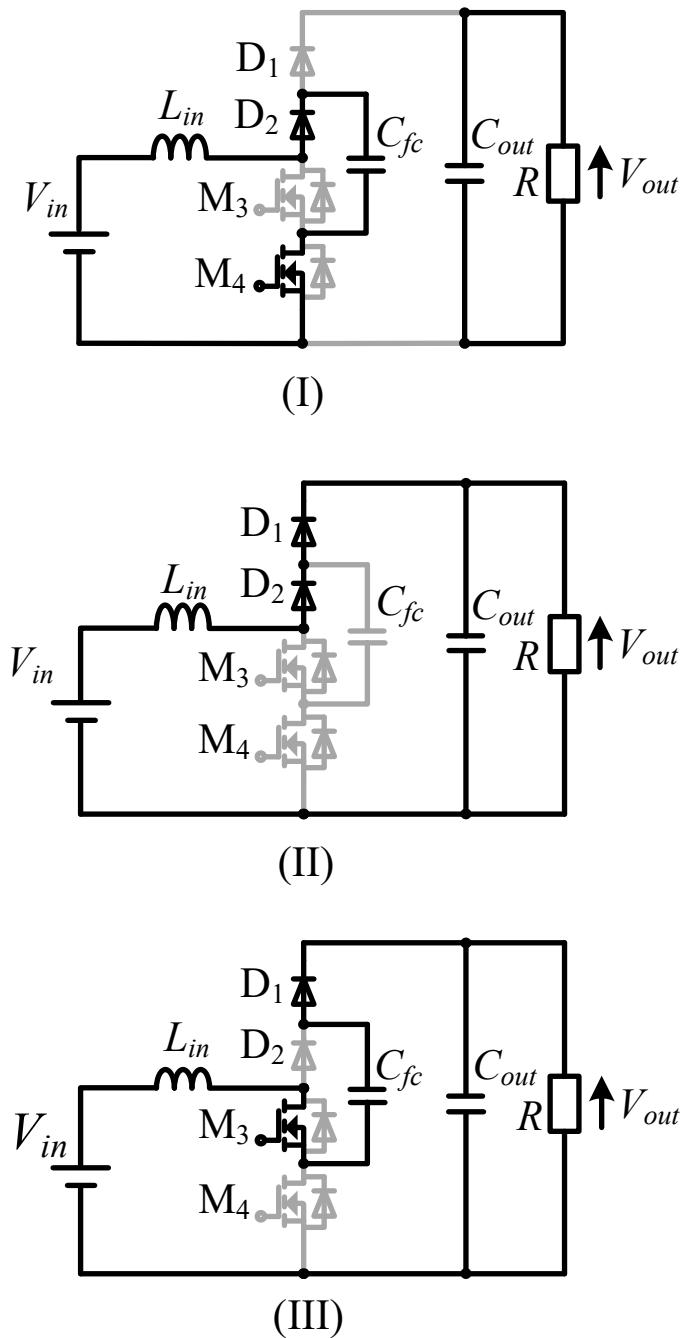


Figure 3.3 Operation modes of three-level FCBC.

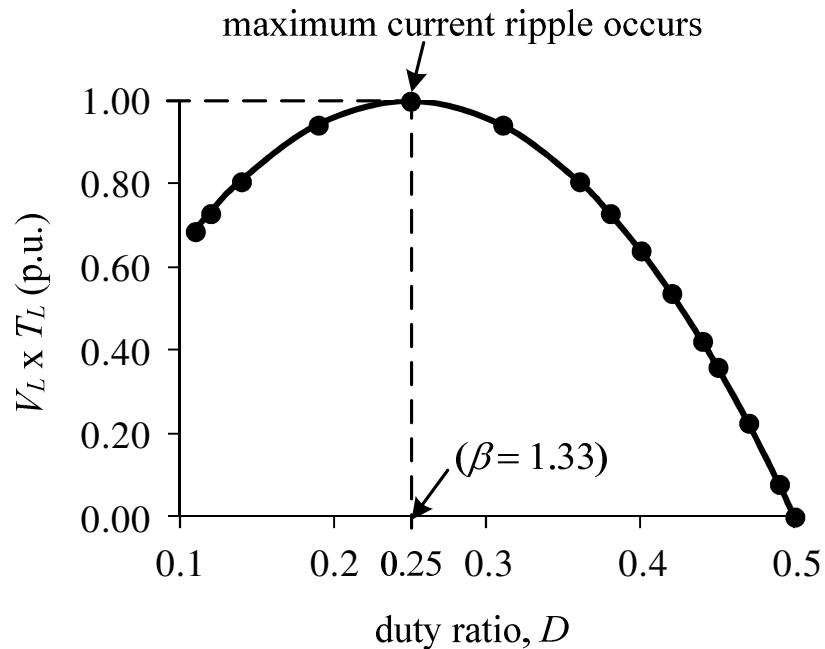


Figure 3.4 Relationship between $V_L \times T_L$ (p.u.) and duty ratio D .

3.3.2 Inductor Core Volume

The core volume of an input inductor is discussed based on the area product theory [135]. In this section, the input inductor core volumes for the FCBC and conventional DC-DC boost converters are compared. The inductor core volume Vol as a function of constant K_{vol} and the area product A_p can be expressed as follows [135]:

$$Vol = K_{vol} A_p^{0.75} = K_{vol} \left[\frac{2W(10^4)}{B_m JK_u} \right]^{0.75} \quad (3.7)$$

where B_m is a flux density. Moreover, the energy-handling capability of an inductor core W is related to the area product A_p . The energy-handling capability of an inductor core W can be expressed as follows:

$$W = \frac{1}{2} L \times I^2 \quad (3.8)$$

where I is a maximum inductor current.

The inductor core volume Vol can be estimated by considering the energy required for an inductor, as expressed by Eq. (3.8). Thus, the inductance required by the FCBC is approximately 25% of that required by the conventional DC-DC boost converter. Furthermore, Eq. (3.8) can also be expressed by the following equations for the FCBC and conventional DC-DC boost converter, respectively:

$$W_{FCBC} = \frac{1}{2} L_{FCBC} \times I^2 = \frac{1}{2} (L_{conventional} \times 25\%) \times I^2 \quad (3.9)$$

$$W_{conventional} = \frac{1}{2} L_{conventional} \times I^2 \quad (3.10)$$

If the inductance $L_{conventional}$ of a conventional DC-DC boost converter is considered as a reference, the required input inductor core volume of the FCBC is approximately 35% of that of the conventional DC-DC boost converter, as expressed by the following equations:

$$\frac{Vol_{FCBC}}{Vol_{conventional}} = \left(\frac{W_{conventional}}{W_{FCBC}} \right)^{0.75} \quad (3.11)$$

$$Vol_{FCBC} = 35\% \times Vol_{conventional} \quad (3.12)$$

Thus, not only is the inductance reduced, but the inductor core volume is also greatly reduced. Consequently, the overall size and weight of the converter are reduced.

3.4 Relationship between the Capacitance of the Flying Capacitor and the Output Voltage Ripple

Principally, the time constant $R_{out}C_{out}$, which consists of the output resistance R_{out} and output capacitance C_{out} , can be considered in order to establish the relationship between the capacitance of the flying capacitor and the output voltage ripple. Based on observations, if the output voltage ripple is always constant, even though the capacitance of the flying capacitor varies, the time constant $R_{out}C_{out}$ should be greater than the switching period $1/f_{sw}$, as expressed by Eq. (3.13).

Meanwhile, if the output voltage ripple varies depending on the capacitance variation of the flying capacitor, the time constant $R_{out}C_{out}$ should be either equal to or less than the switching period $1/f_{sw}$. This principle can be proven mathematically in order to establish whether the relationship between the capacitance of the flying capacitor and the output voltage ripple is independent or dependent.

Moreover, the time constant $R_{out}C_{out}$ can be expressed as a function of the output voltage and output power. Therefore, in order to estimate and design the capacitance of the flying capacitor without considering the

output voltage ripple, the following equation should be satisfied:

$$R_{out}C_{out} = \frac{V_{out}^2}{P}C_{out} > \frac{1}{f_{sw}} \quad (3.13)$$

Based on the simulation and experimental setup, three output capacitances and an output resistance are selected, as shown in Table 3.3. The switching frequency f_{sw} is set to 100 kHz, which is equivalent to a switching period of 10 μ s. Referring to Table 3.3, it is obvious that all of the time constants $R_{out}C_{out}$ for the numerous output capacitances are greater than the switching period T . This condition is in agreement with Eq. (3.13). Therefore, the output voltage should be constant.

Furthermore, the minimum time constant $R_{out}C_{out}$ for these three conditions is 16.5 times greater than the switching period T . Thus, based on this analysis, the time constant $R_{out}C_{out}$ is always greater than the switching period T as expressed by Eq. (3.13). This condition leads to the capacitance of the flying capacitor and the output voltage ripple always being independent of each other.

Theoretically, the peak-to-peak measurement of the output voltage ripple of a conventional DC-DC boost converter can be calculated by referring to the output capacitor current waveform, whereby the change in

the output capacitor charge Q must be considered [51, 52]. This principle can also be considered in order to establish the relationship between the capacitance of the flying capacitor and the output voltage ripple. Table 3.4 shows the charging and discharging conditions of the passive components/devices, i.e., the input inductor, flying capacitor, and output capacitor according to the operation mode, as shown in Figure 3.3.

In order to clarify the charging and discharging conditions of the output capacitor, the converter operation modes shown in Figure 3.3 are referenced. By referring to the operation modes shown in Figure 3.3, the output capacitor only discharges during Mode I and charges during Modes II and III. Hence, the total charge Q_{total} from these charging and discharging processes for one switching period is equal to zero. This condition can be expressed as follows:

$$Q_{charge} = Q_{discharge} \quad (3.14)$$

Figure 3.5 shows the simulation results for the waveforms of the output capacitor current, I_{Cout} , the output voltage, V_{out} , the flying capacitor voltage, V_{fc} , and the inductor current, I_L . The specifications of this simulation condition are as follows: output voltage, $V_{out} = 350$ V, input voltage, $V_{in} =$

262.5 V, output capacitance, $C_{out} = 1.5 \mu\text{F}$, capacitance of the flying capacitor, $C_{fc} = 0.35 \mu\text{F}$, and flying capacitor voltage, $V_{fc} = V_{out}/2$. These simulation results indicate that the peak-to-peak output voltage ripple can be determined by referring to the output capacitor current waveform, as shown in Figure 3.5. The change in the output capacitor charge can be calculated as follows [51, 52]:

$$|\Delta Q_{discharge}| = \left(\frac{V_{out}}{R_{out}} \right) DT = C_{out} \Delta V_{out} \quad (3.15)$$

By considering this principle, the output capacitance C_{out} can be estimated in terms of the output voltage ripple ΔV_{out} in the FCBC. Based on Eq. (3.15), the output voltage ripple ΔV_{out} can be expressed as follows:

$$\Delta V_{out} = \frac{V_{out} D}{R_{out} C_{out} f_{sw}} \quad (3.16)$$

If the boost ratio β and output power P_{out} are considered, Eq. (3.16) can be rewritten as follows:

$$\Delta V_{out} = \frac{P_{out} (\beta - 1)}{\beta V_{out} C_{out} f_{sw}} \quad (3.17)$$

Based on Eq. (3.17), the output voltage ripple is proportional to the output power and inversely proportional to the output voltage, the output capacitor, and the switching frequency.

Thus, based on Eq. (3.17), the capacitance of the flying capacitor and the output voltage ripple are independent. This finding is confirmed by the simulation and experimental results. Therefore, it is confirmed that the capacitance of the flying capacitor can be estimated without relying on the output capacitance or output voltage ripple.

Table 3.3 Time constant and switching period.

Output Capacitor C_{out}	Output Resistor R_{out}	Time Constant $R_{out}C_{out}$	Switching Period $1/f_{sw} = T$
1.5 μ F	110 Ω	165 μ s	10 μ s
6 μ F		660 μ s	
9 μ F		990 μ s	

Table 3.4 Charging and discharging states of the input inductor, the flying capacitor, and the output capacitor according to the operation mode of the FCBC.

Operation Mode	Input Inductor (L)	Flying Capacitor (C_{fc})	Output Capacitor (C_{out})
Mode I	charging	charging	discharging
Mode II	discharging	unchanged	charging
Mode III	charging	discharging	charging
Mode II	discharging	unchanged	charging

Note: 1) 'charging'/'discharging' = component is either in charging or discharging conditions. 2) 'unchanged' = component is not in charging or not in discharging conditions.

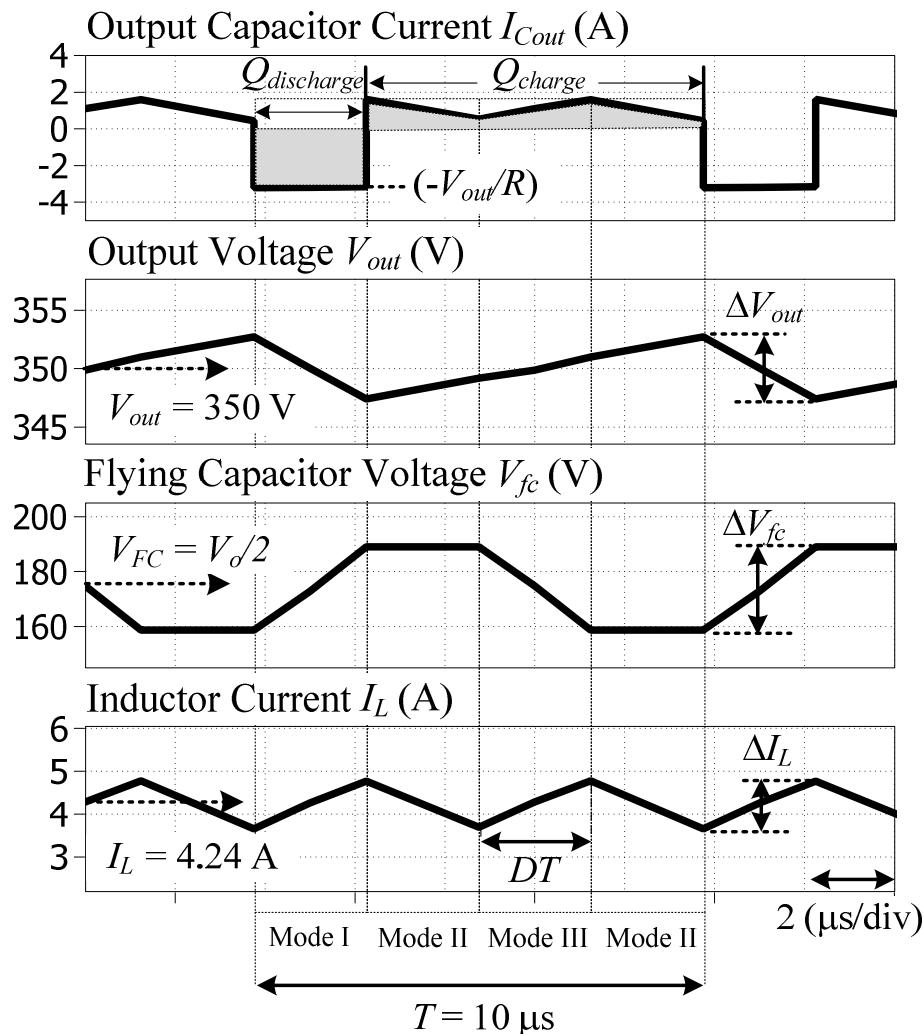


Figure 3.5 Simulation waveforms of the output capacitor current, the output voltage, the flying capacitor voltage, and the inductor current.

3.5 Experimental Results

In this section, the experimental results and experiment specifications are shown. The details of the experiment specifications are depicted in Table 3.5. Practically, the selected inductance of an input inductor is 200 μH , which is based on the design principle, as described in Section 3. The maximum output power for the conditions of the experiment and the simulation is 1 kW. However, Table 3.6 also lists the experiment specifications for the observation of the relationship between the capacitance of the flying capacitor and the output voltage ripple.

3.5.1 Input inductor design and inductor current ripple

Table 3.5 lists the experiment specifications. For the design specifications of this prototype, the maximum inductor current ripple, $\Delta I_{L\text{-max}}$, is designed at 1.1 A, as expressed by Eq. (3.5). Moreover, based on the experimental results, the inductor current ripple is 1.1 A, as shown in Figure 3.6. Therefore, the simulation and experimental results are in good agreement, and the inductor current ripple design is confirmed. However, the potential for an unbalanced flying capacitor voltage must be considered

for the stable operation of the converter [82, 136-138].

The inductance and core volume of the input inductor are designed by considering the maximum inductor current ripple as expressed by Eqs. (3.5) and (3.12). Theoretically, if the same specifications of the inductor design are considered, the conventional boost DC-DC converter requires an inductance of the input inductor of approximately 800 μH , whereas the FCBC requires an inductance of only approximately 200 μH .

Moreover, the copper loss is reduced due to the small inductance of the input inductor. Hence, the FCBC needs only approximately 25% and 35% of an inductance and an inductor core volume of the input inductor, respectively compared to the conventional DC-DC boost converter. Therefore, the reductions in the inductance and inductor core volume of the input inductor are reflected in the reduction of the size and weight of the converter.

Table 3.5 Specifications of the simulation and experiment.

Specification	Value
Input Voltage V_{in}	262.5 V
Output Voltage V_o	350 V
Output power P_{out}	250 ~1100 W
Input current I_{in}	4.24 A
Switching frequency f_{sw}	100 kHz
Duty ratio D	0.25
Input inductor L	200 μ H
Flying capacitor C_{fc}	0.11, 0.35, 0.6, 1.1, μ F
Output capacitor C_{out}	1.5, 6, 9 μ F
Maximum inductor current ripple ΔI_{L-max}	1.1 A
MOSFET	IRFB4229PBF
SiC Schottky Diode	IDW30G65C5

Table 3.6 Specifications of the output voltage ripple measurement.

Parameters	Value
Output capacitor C_{out}	1.5, 6, 9 μ F
Flying capacitor C_{fc}	0.11, 0.35, 0.6, 1.1 μ F
Output resistor R_{out}	110 Ω
Duty ratio D	0.25

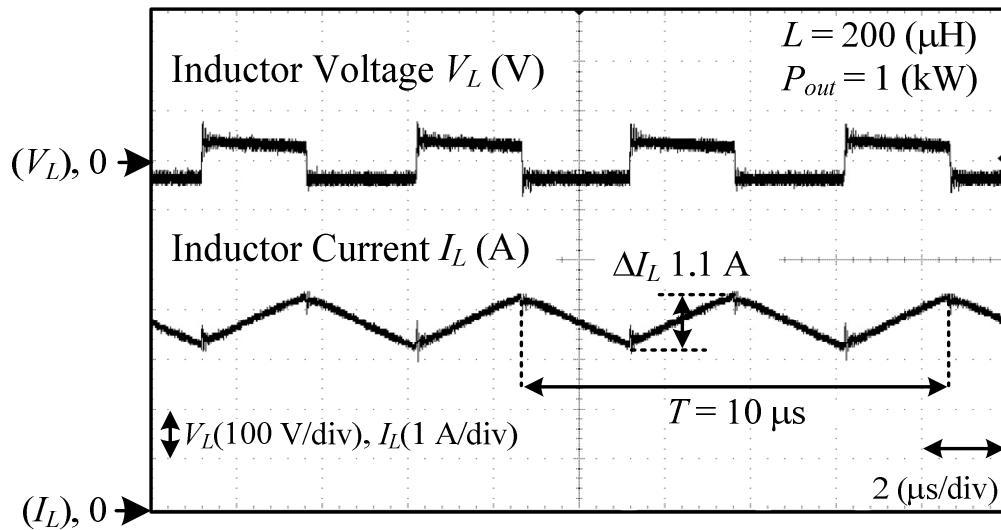


Figure 3.6 Experimental waveforms of the inductor voltage and inductor current.

3.5.2 System Relationship between the capacitance of the flying capacitor and the output voltage ripple

In this section, only the conditions with an output capacitance of $1.5 \mu\text{F}$ and several capacitances of the flying capacitor is considered in the discussion of the relationship between the capacitance of the flying capacitor and the output voltage ripple, as shown in Figure 3.7.

Figure 3.7 shows the details of the experimental waveforms of the output voltage ripple for an output capacitance of $1.5 \mu\text{F}$ and various capacitances of the flying capacitor, i.e., $1.1 \mu\text{F}$, $0.6 \mu\text{F}$, $0.35 \mu\text{F}$, and $0.11 \mu\text{F}$, respectively. Table 3.6 lists the specifications of the experiment. In this

prototype, film capacitors are used for the output capacitor and the flying capacitor. The experimental results confirm that the peak-to-peak output voltage ripple is 5.6 V for all capacitances of the flying capacitor, because the capacitance of the flying capacitor and the output voltage ripple are independent, as indicated by Eq. (3.16).

Figure 3.8 shows a summary of the experimental results of the relationship between the capacitance of the flying capacitor and the output voltage ripple with a fixed output capacitance and various capacitances of the flying capacitor. Table 3.6 lists the experiment specifications. In order to clarify this phenomenon, small output capacitances (1.5 μ F, 6 μ F, and 9 μ F) and small capacitances of the flying capacitor (0.11 μ F, 0.35 μ F, 0.6 μ F, and 1.1 μ F) are selected. The output voltage ripple is confirmed to remain unchanged with respect to the capacitance variation of the flying capacitor, as shown in Figure 3.8.

Therefore, these experimental results indicate that the capacitance of the flying capacitor and the output voltage ripple are independent of each other. Hence, the capacitance of the flying capacitor can be estimated without considering the output voltage ripple, as indicated by Eqs. (3.16)

and (3.17). However, due to the influence of parasitic components and the ESR of the output capacitor, the measured output voltage ripples differ slightly from the simulation results. The errors between the simulation and experimental results are 0.3 V, 0.05 V, and 0.06 V for output capacitances of 1.5 μ F, 6 μ F and 9 μ F, respectively, as shown in Table 3.7.

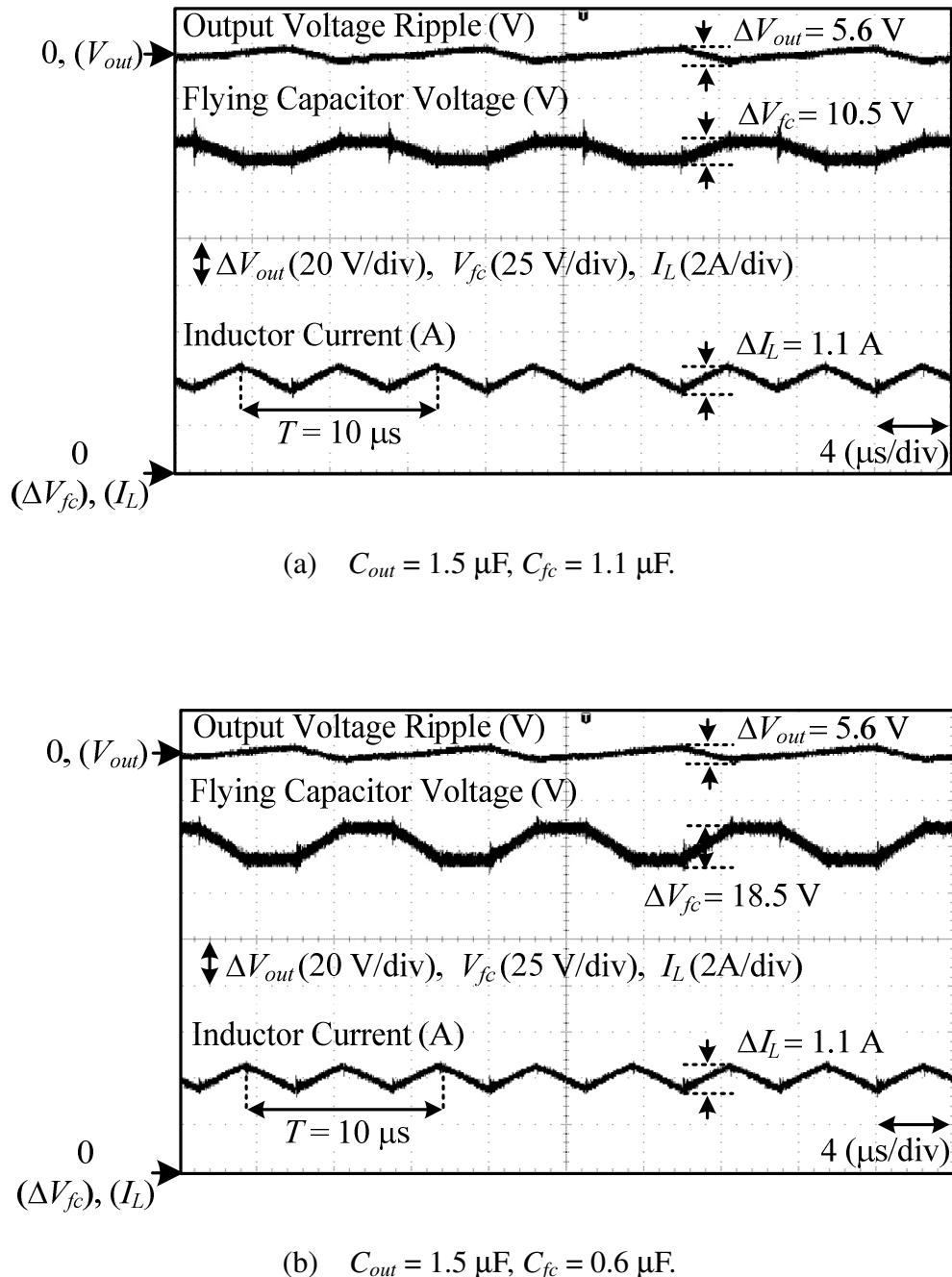


Figure 3.7 Experimental waveforms of the output voltage, the flying capacitor voltage, and the inductor current.

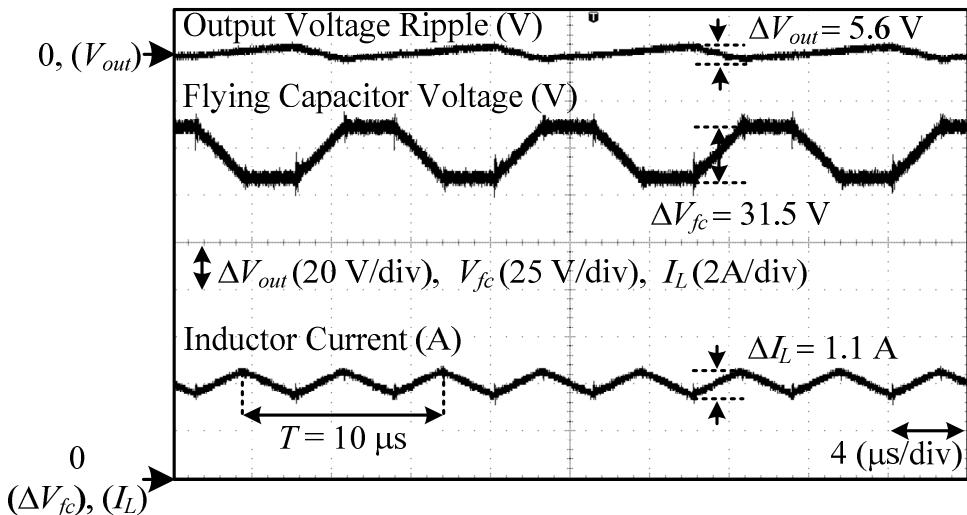
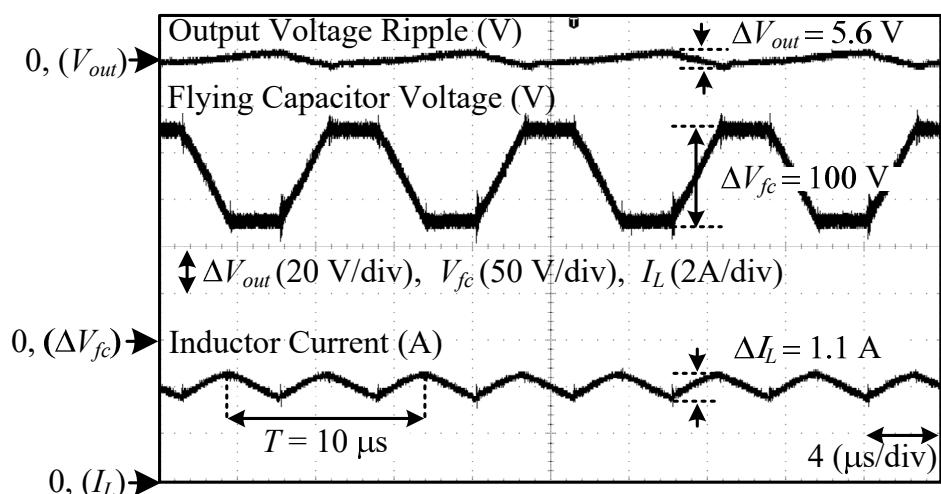
(c) $C_{out} = 1.5 \mu\text{F}$, $C_{fc} = 0.35 \mu\text{F}$.(d) $C_{out} = 1.5 \mu\text{F}$, $C_{fc} = 0.11 \mu\text{F}$.

Figure 3.7 Experimental waveforms of the output voltage, the flying capacitor voltage, and the inductor current.

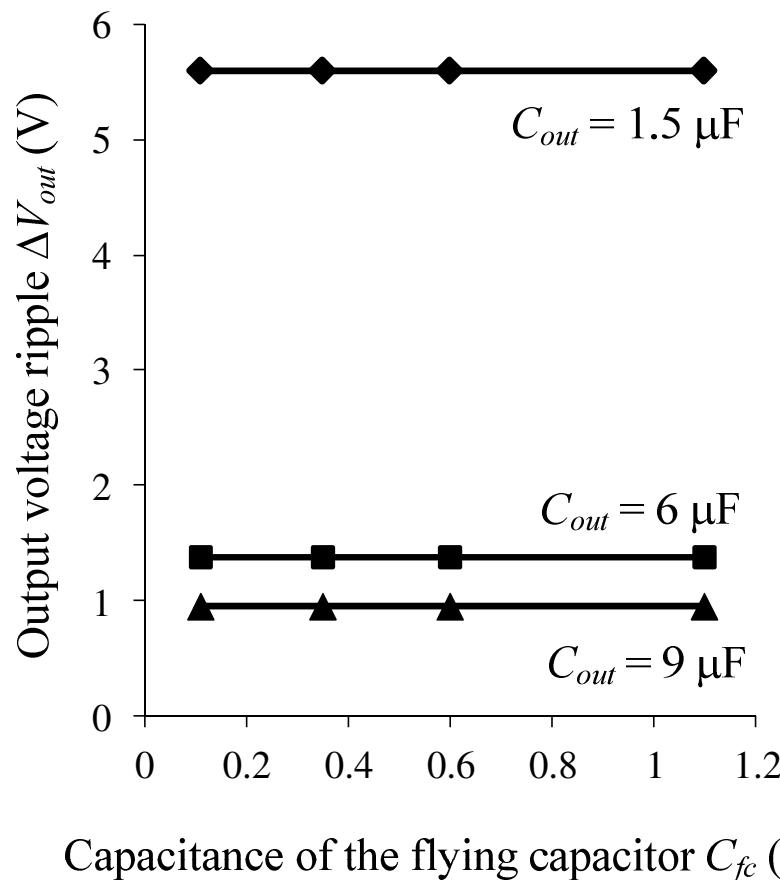


Figure 3.8 Relationship between the capacitance of the flying capacitor C_{fc} and the output voltage ripple ΔV_{out} .

Table 3.7 Error ratio between the simulation and experimental results for the output voltage ripple.

Output Capacitor C_{out}	Flying Capacitor C_{fc}	Error (between simulation and experimental results)
1.5 μ F	0.11 μ F	0.3 V
	0.35 μ F	
	0.6 μ F	
	1.1 μ F	
6 μ F	0.11 μ F	0.05 V
	0.35 μ F	
	0.6 μ F	
	1.1 μ F	
9 μ F	0.11 μ F	0.06 V

3.5.3 Relationship between the inductor current ripple and the flying capacitor voltage ripple for various capacitances of the flying capacitor

Figure 3.9 shows the relationship between the inductor current ripple and the flying capacitor voltage ripple for various capacitances of the flying capacitor, i.e., $1.1 \mu\text{F}$, $0.6 \mu\text{F}$, $0.35 \mu\text{F}$, and $0.11 \mu\text{F}$. Based on these relationships, the inductor current ripple is confirmed to remain unchanged with regard to the capacitance variation of the flying capacitor. The flying capacitor voltage ripple depends on the capacitance variation of the flying capacitor, where the flying capacitor voltage ripple becomes high when a small capacitance of the flying capacitor is selected. For further observation, the experimental waveforms of the inductor current ripple and flying capacitor voltage ripple are referenced in order to describe the relationship between the inductor current ripple and the capacitance variation of the flying capacitor, as shown in Figure 3.7.

Therefore, based on these experimental results, the inductor current ripple and capacitance variation of the flying capacitor are independent of each other. The reason for this condition is that the inductor current ripple

is dominated by the difference in voltage between the input and output voltages in Mode II, as shown in Figure 3.3. As a result, the inductance of an input inductor can be estimated without considering the voltage ripple on the flying capacitor, as described in Section 3.

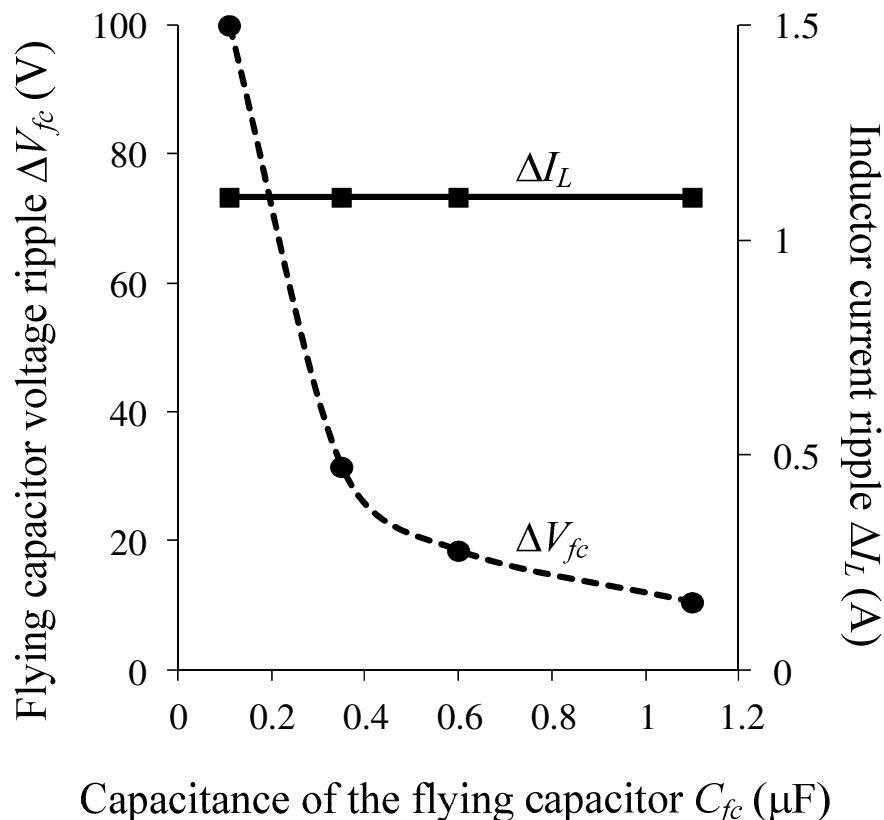


Figure 3.9 Relationship between the flying capacitor voltage ripple and the inductor current ripple with the capacitances of the flying capacitor.

3.5.4 Converter efficiency for several output power levels

Figure 3.10 shows the converter efficiency characteristics. Several output power levels are considered for these experimental results. The output voltage is fixed at 350 V. Several capacitances of the flying capacitor are considered for the efficiency measurement of the constructed prototype circuit. The achieved maximum efficiency is 98.5% for an output power of 1 kW. During this achieved maximum efficiency condition, the capacitances of the flying capacitor are 1.1 μ F and 0.6 μ F. Moreover, for the same output power condition and a capacitance of the flying capacitor of 0.11 μ F, the efficiency is decreased to 98.2% due to the high value of the ESR of the capacitor, as compared to that of the other flying capacitors. Based on these efficiency characteristics, the converter efficiency decreases when the output power is decreasing, as shown in Figure 3.10.

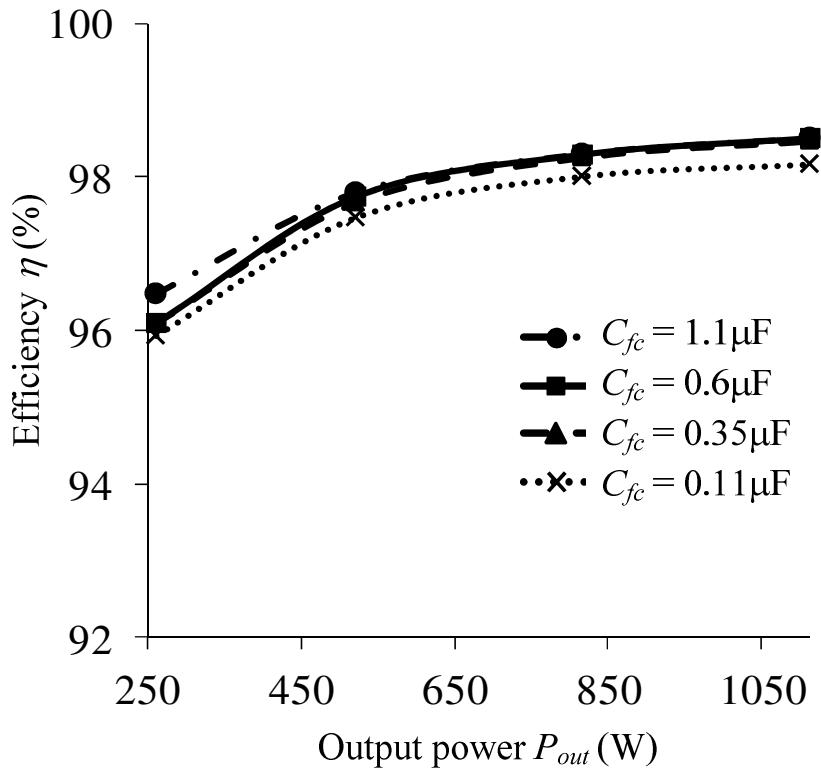


Figure 3.10 Relationship between the converter efficiency characteristics and the capacitance variation of the flying capacitor.

3.5.5 Power loss analysis based on output power levels

The distribution of the converter power losses is analyzed based on the converter output power. The power losses are distributed into seven parts, i.e., diode conduction loss, MOSFET conduction loss, MOSFET switching loss, inductor copper loss, equivalent series resistance (ESR) loss of the flying capacitor and the output capacitor, no-load loss, and other losses. Moreover, due to the complexity of the estimation of the power losses,

other losses such as wiring loss, iron loss, and ringing loss are included in the ‘other losses’ category, as shown in Figure 3.11. In addition, the diode reverse-recovery loss is not considered in the present paper because SiC Schottky barrier diodes without reverse-recovery loss are used in the prototype circuit.

Figure 3.11 shows the details of a power loss distribution of the FCBC for several output power levels for a capacitance of the flying capacitor of $1.1\text{ }\mu\text{F}$ and an output capacitance of $6\text{ }\mu\text{F}$ are considered. The total power loss of 100% is based on the total power loss when the converter power is increased approximately at 1 kW. Hence, the total power loss is considered as a reference for this power loss distribution analysis.

Based on this power loss distribution analysis, one of the major power losses is dominated by the diode conduction loss for converter power levels approximately of 1 kW and 800 W. However, it was dominated by the ‘other losses’ for a converter power level approximately of 500 W. The inductor copper loss was the lowest component of the total power loss. Moreover, at output power levels approximately of 1 kW and 800 W, ‘other losses’ were the second largest power losses, followed by the diode

conduction loss for a converter power level approximately of 500 W.

Based on this power loss analysis, the inductor copper loss is small due to smaller number of inductor windings. Moreover, MOSFET conduction loss is considered to be small due to the low input current with regard to the small boost ratio. If the boost ratio is high, the input current becomes high. As a result, the conduction loss of the MOSFET becomes high.

Since one of the major power losses is associated with the diodes, low-on-voltage diodes must be considered in order to reduce the conduction loss of the diodes. Moreover, the conduction loss in the flying capacitor is considered to be high due to the high value of the ESR. Therefore, a low ESR for the flying capacitors must be selected in order to reduce the flying capacitor conduction loss. In order to reduce the power loss in the MOSFETs when a high boost ratio is considered, low-on-resistance MOSFETs must be selected. As an option, the on-resistance can be further reduced by connecting the MOSFETs in parallel connection. Therefore, by considering these available options, the overall converter efficiency can be improved further.

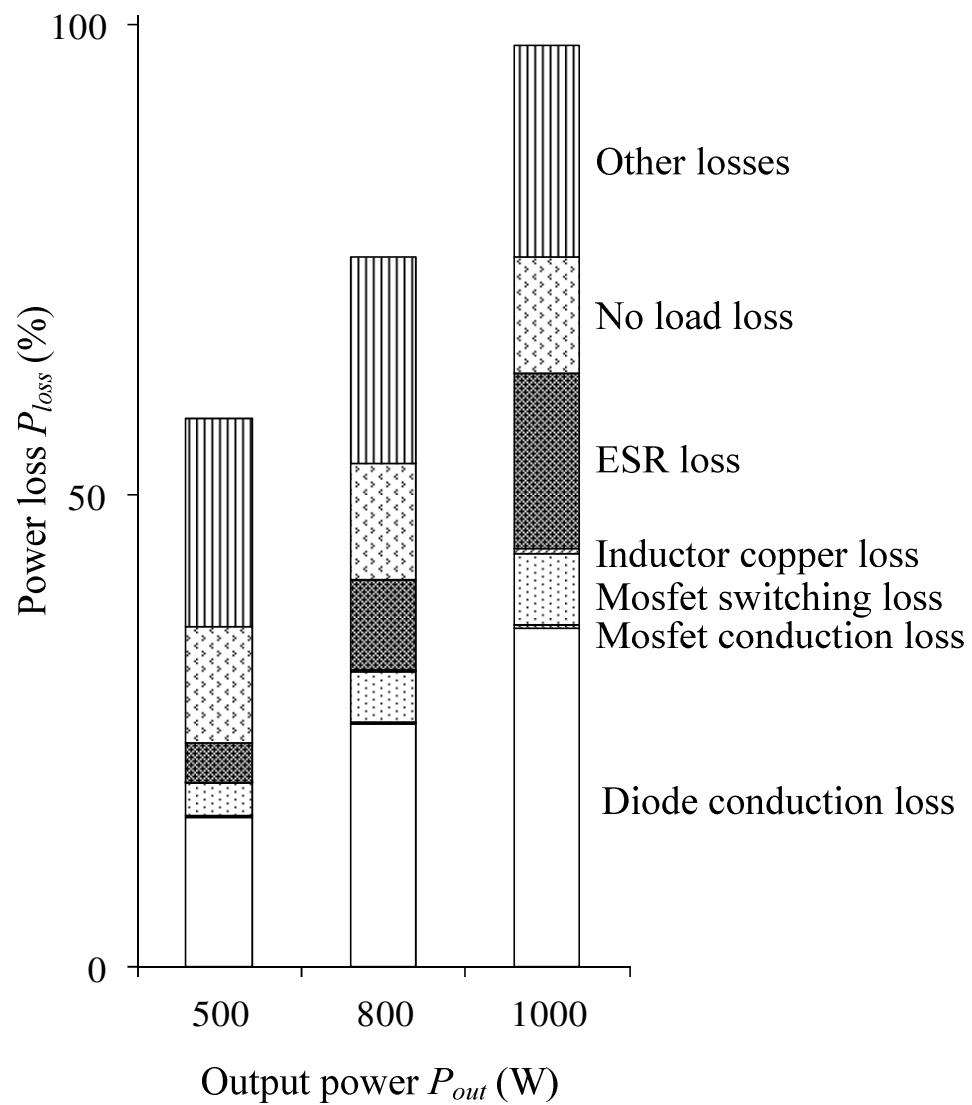


Figure 3.11 Converter loss distribution when the capacitance of the flying capacitor is $1.1 \mu\text{F}$.

3.6 Power Density Comparison

In order to evaluate the advantage of three-level FCBC over two-level CBC (conventional two-level DC-DC boost converter) in terms of power density, Pareto-front curve method is used. The power density estimation for all converters is conducted theoretically. The specifications of all selected converters are as follow: the input voltage is 262.5 V, the output voltage is 350 V, the duty ratio is 0.25, the switching frequency ranges are from 25 kHz to 500 kHz and the output power is 1 kW. For the volume estimation, only heatsinks, input inductor, flying capacitor and output capacitor components are considered whereby usually these components give a significant impact on the converter volume. In addition, it should be noted that copper and iron losses of the input inductor are not considered. Besides, ESR losses of flying capacitor and output capacitor are very small. Thus the efficiency estimation for all converters is based on semiconductor devices losses.

Heatsinks volume estimation is based on the power loss of semiconductor devices and the cooling system performance index (CSPI) [139-141]. For the heatsinks volume estimation, the considered CSPI is 4.

Besides, the simulation results of the conduction and switching losses for the both converters are considered for the heatsink volume estimation. The heatsink volume estimation is expressed as follows:

$$Vol_{heatsink} = \frac{1}{R_{th}CSPI} = \frac{P_{loss}}{(T_j - T_a)CSPI} \quad (3.18)$$

where R_{th} is the thermal resistance of the cooling system, P_{loss} is the sum of conduction and switching losses of the semiconductor devices, T_j is the junction temperature and T_a is the ambient temperature.

Then, the volume estimation for the input inductor is estimated by using the Area Product [135] principle. From the Area Product principle, the inductor volume is proportional to the stored energy in an inductor. Thus, the input inductor volume is expressed as follow:

$$Vol_{inductor} = K_{vol} \left(\frac{LI^2}{K_u B_m J} \right) \quad (3.19)$$

where K_{vol} is the constant related to the core configuration, L is the inductance of an inductor, I is the maximum inductor current, K_u is the window utilization factor, B_m is the flux density and J is the current density.

On the other hand, the three-level FCBC has a flying capacitor and an output capacitor; meanwhile the two-level CBC has only an output

capacitor. Fundamentally, between capacitor volume and stored energy in a capacitor has a linear relationship [139-141]. Thus, the capacitor volume can be estimated based on stored energy in capacitors. In this section, ceramic capacitors type is considered for the capacitor volume estimation. Thus, the capacitor volume is expressed as follows:

$$Vol_{capacitor} = \gamma_{V_c}^{-1} \frac{1}{2} CV_c^2 \quad (3.20)$$

where C is the capacitance of a capacitor, V_c is the voltage across a capacitor and $\gamma_{V_c}^{-1}$ is the proportionality factor between the energy and the volume.

Figure 3.12 shows the three-level FCBC has higher power density and efficiency compared to the two-level FCBC. The maximum power density for two-level CBC and three-level FCBC are 15.42 kW/dm^3 and 18.95 kW/dm^3 , respectively. Therefore from this comparison, three-level FCBC has advantage on input inductor volume reduction and consequently it contributes to a higher power density compared to the two-level CBC.

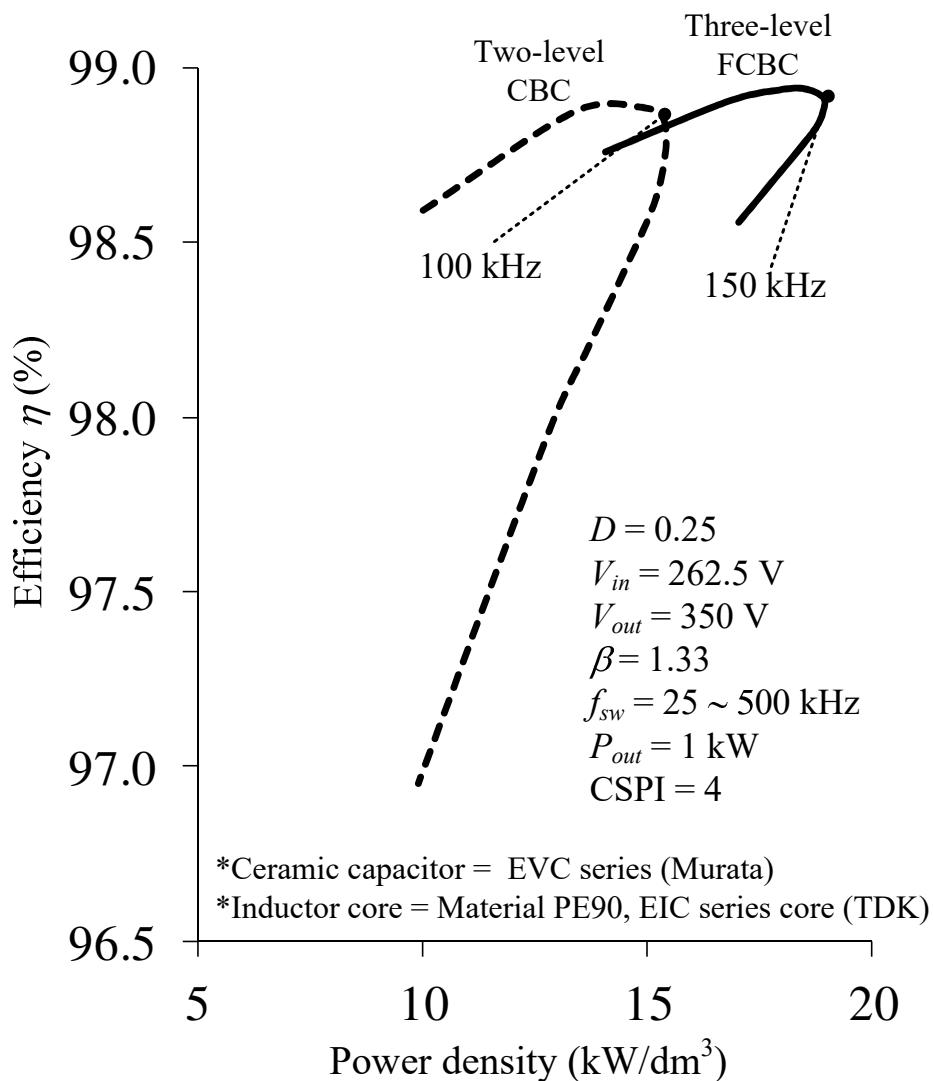


Figure 3.12 Power density characteristics of the two-level CBC and the three-level FCBC using Pareto-front curve method.

3.7 Conclusion

In the present paper, the authors examined an FCBC with a small-capacitance flying capacitor considering the output voltage ripple. Moreover, the authors discussed the analysis of the input inductor design. In the present paper, the authors have discussed (i) the fundamental circuit operation confirmation of the FCBC, (ii) the design method of an input inductor, and (iii) the relationship between the capacitance of the flying capacitor and the output voltage ripple.

The principal in designing the input inductor in terms of the inductance and inductor core volume is explained. As a result, the inductance and inductor core volume of the input inductor are reduced by approximately 25% and 35%, respectively. Moreover, the relationship between the capacitance of the flying capacitor and the output voltage ripple is established mathematically. The experimental results confirmed that the capacitance of the flying capacitor and the output voltage ripple are independent of each other. Moreover, the maximum efficiency is 98.5% at an output power of 1 kW. In addition, power density comparisons between two-level and three-level FCBC are conducted theoretically.

Chapter 4

Effectiveness Evaluation for the Small Capacitance of the Flying Capacitor in the Multilevel Flying Capacitor Boost Converter

4.1 Introduction

Generally, an inductor-less of the three-level flying capacitor boost converter (FCBC) is based on the capacitor-based component configuration whereby the capacitance of the flying capacitor should be large in order to keep the flying capacitor voltage always half of the output voltage and to suppress the surge current [69, 71, 79-81, 84, 86-88, 93]. For instance, in this circuit structure if the output voltage is 300 V, thus only 150 V will be across on the flying capacitor and switching devices. Thus voltages stress on switching devices only half of the output voltage. Due to this condition,

low-voltage-rating switching devices with fast switching performance and low on-resistance features can be used instead of using high-voltage-rating devices which is usually suffer from low-switching-speed and high on-resistance features.

However, nowadays low-power-loss and high-voltage-rating switching devices, such as SiC-MOSFETs have been developed [63-66, 134, 142]. Thus, small capacitances such as from ceramics and films types with high voltage capability can be considered together with high-voltage-rating switching devices. As a result, the volume of the flying capacitor can be reduced compared to conventional FCBCs. The three-level FCBC with a small flying capacitor is extensively discussed in Chapter 3. However, the minimum capacitance selection and its influence in the multilevel FCBC have not been discussed [80, 82, 93, 132, 136].

In Chapter 3, the details design principle and operation of the three-level FCBC have illustrated and described, including reduction of the input inductor principle based on inductor current ripple compared to the conventional two-level boost converter. Besides, the relationship between the capacitance of the flying capacitor and the output voltage ripple has

been established. The finding shows that the relationship between the capacitance of the flying capacitor and the output voltage ripple is independent one another. As a result the capacitance of the flying capacitor can be designed regardless of output voltage ripple influences. Furthermore the relationship between the inductor current ripple and the flying capacitor voltage ripple is also investigated. The finding indicated that the inductor current ripple is confirmed to remain unchanged with regard to the capacitance variation of the flying capacitors. As a result the inductance of the input inductor can be designed without considering voltage ripple of the flying capacitor [72, 79].

Basically, the approach that have considered in order to observe the effectiveness evaluation of the small capacitance of the flying capacitor in the multilevel FCBC is the observation on the distortion voltage across the input voltage source and input inductor at input side and the distortion current to a load at the output side. Hence, by investigating these distortion voltage and current, the effectiveness of using small capacitances of the flying capacitor are identified and clarified on the multilevel FCBC.

The organization of this chapter as follows, the multilevel FCBC considering a small capacitance of the flying capacitor is proposed in order to reduce the size and weight of the power converter. First, the principle of the multilevel FCBC is described. Next, a design method for minimum capacitance of the flying capacitor is clarified. Then, the minimum capacitance design method for the flying capacitor is experimentally verified. Finally, the distortion of the voltage across a input voltage source and a input inductor and the current to the output side which the output capacitor and the load are investigated for the three-level and the five-level of the FCBCs in terms of small capacitance of the flying capacitor.

4.2 Principle of the Multilevel FCBC

First, a principle of a three-level FCBC is described. Next, parameters of passive components in a n-level FCBC is described.

4.2.1 three-level FCBC

Basically, the three-level FCBC consists of two diodes, two switches, an input inductor L , a flying capacitor C_{fc} , and an output capacitor C_{out} . The input inductor is used in order to control independently the output voltage by controlling the duty ratio D . The relationship between the input voltage V_{in} and the output voltage V_{out} is expressed by (4.1) using the boost ratio β ,

$$V_{out} = \beta V_{in} \quad (4.1)$$

β is expressed by (42).

$$\beta = \frac{1}{1-D} \quad (4.2)$$

Figure 3.2 shows the circuit configuration and the operation mode of the three-level FCBC. During one switching period, the operation mode is repeated. Only the boost ratio in the range of $1 < \beta \leq 2$ is considered in this study. The inductance of the input inductor $L_{(3-level)}$ and inductor core

volume $Vol_{(3-level)}$ in the three-level FCBC is expressed by (4.3) and (4.4) [79, 81].

$$L_{(3-level)} = 0.25 \times L_{conventional} \quad (4.3)$$

$$Vol_{(3-level)} = 0.35 \times Vol_{conventional} \quad (4.4)$$

where $L_{conventional}$ is the inductance of the input inductor and $Vol_{conventional}$ is the volume of the input inductor in the conventional two-level DC-DC boost converter.

From (4.3) and (4.4) the inductance of the input inductor and the inductor core volume are greatly reduced compared to the conventional two-level DC-DC boost converter.

4.2.2 n-level FCBC

Figure 4.1 shows the circuit configuration and the operation mode of the five-level FCBC for the boost ratio in the ranges of $1 < \beta \leq 2$. It has four operations modes. During modes I and IV, the flying capacitors C_{fc3} and C_{fc1} , respectively are in charging conditions. Meanwhile, during mode II, the flying capacitor C_{fc2} in charging condition and the flying capacitor C_{fc3} in discharging condition. Furthermore, during mode III, the flying

capacitor C_{fc1} in charging condition and the flying capacitor C_{fc2} in discharging condition.

Meanwhile, Figure 4.2 shows the n -level FCBC circuit configuration. In the n -level FCBC, the balancing of each flying capacitor voltages need to be considered. The unbalanced condition is due to improper charging and discharging of the flying capacitor [129, 133, 138]. This condition will lead to an increasing the voltage stress of switches. In the section III (C), the important expressions for the n -level FCBC are discussed.

The inductance of the input inductor $L_{(n\text{-level})}$ and inductor core volume $Vol_{(n\text{-level})}$ in the n -level FCBC are expressed by (4.5) and (4.6), respectively.

$$L_{(n\text{-level})} = \frac{L_{conventional}}{(n-1)^2} \quad (4.5)$$

$$Vol_{(n\text{-level})} = \left(\frac{1}{(n-1)^2} \right)^{0.75} \times Vol_{conventional} \quad (4.6)$$

From both of (4.5) and (4.6), it is confirmed that the inductance of the input inductor and inductor core volume are inversely proportional to the number on level n . Thus the inductance of the input inductor and inductor core volume are reduced when the higher level of a FCBC is considered.

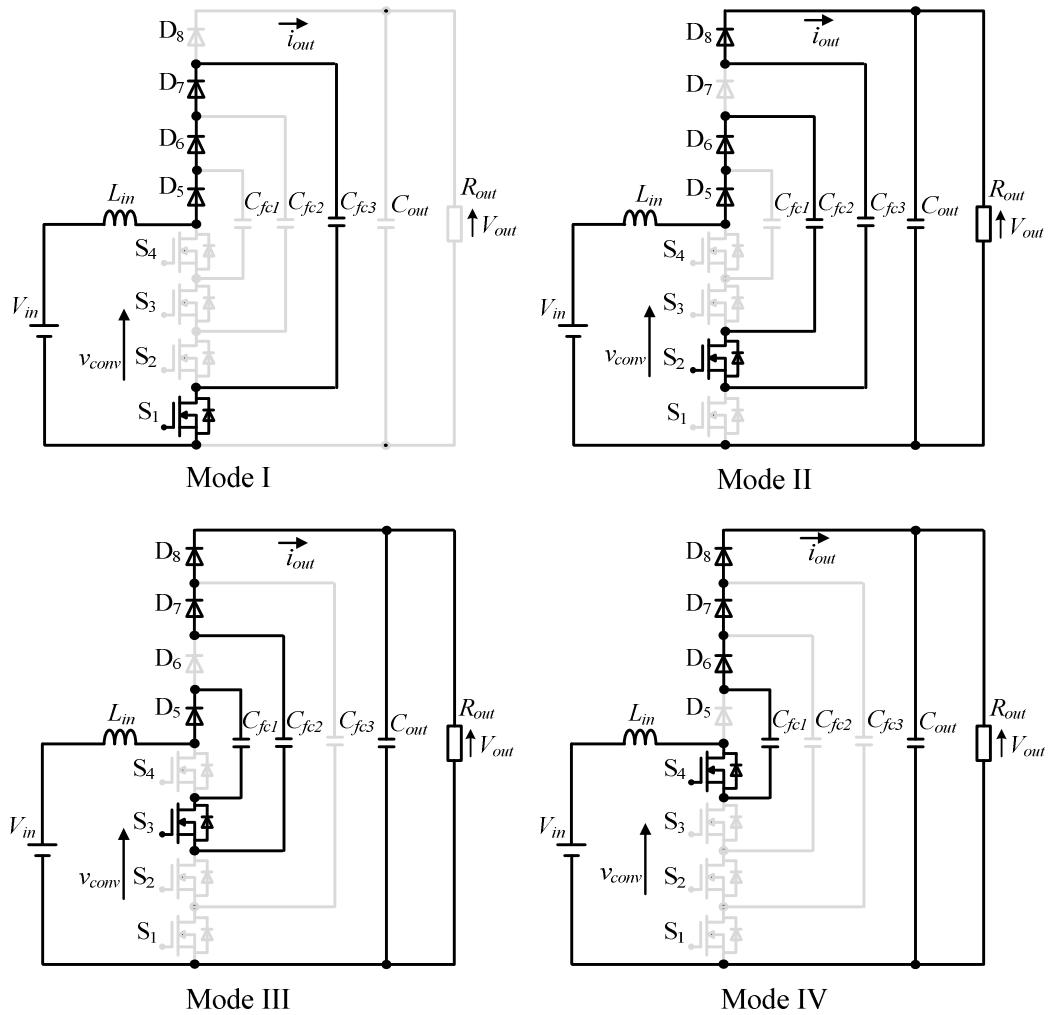
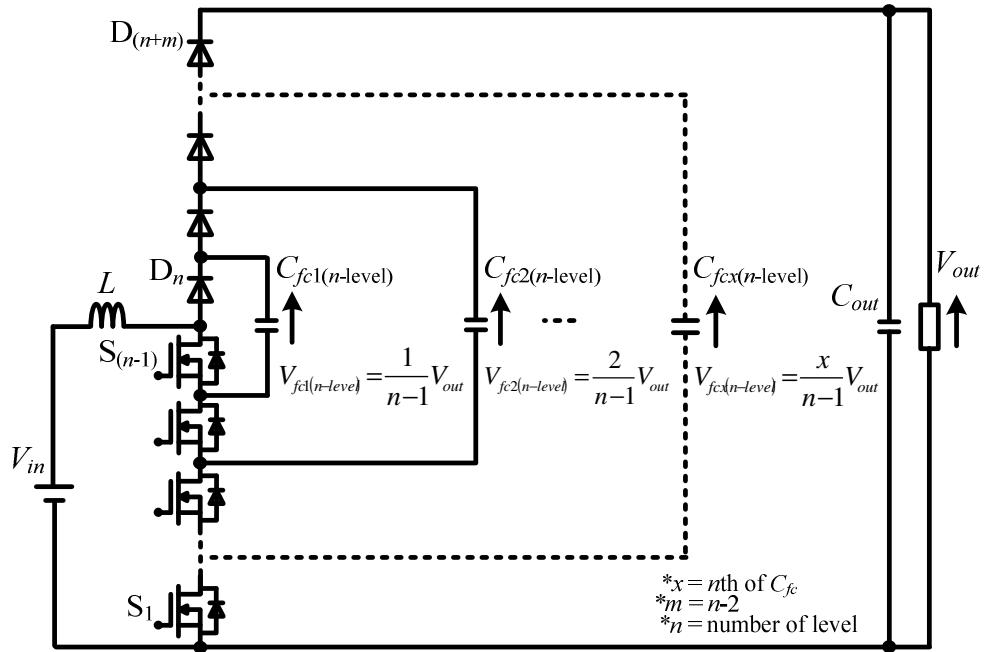


Figure 4.1 Operation modes of five-level FCBC.

Figure 4.2 n -level FCBC.

4.3 Minimum Capacitance Estimation of the Flying Capacitor

In this section, the minimum capacitance design of the flying capacitors in the multilevel FCBCs are described and discussed.

4.3.1 three-level FCBC

Table 4.1 shows the specification of the simulation and experiment conditions. First, the detailed analysis of minimum capacitance of the flying capacitor is based on three-level FCBC. In this chapter, the relationship between the capacitance of the flying capacitor $C_{fc(3\text{-level})}$ and the output voltage ripple ΔV_{out} is considered.

Principally, the time constant $R_{out}C_{out}$, which consists of the output resistance R_{out} and output capacitance C_{out} , is considered in order to estimate the relationship between the capacitance of the flying capacitor and the output voltage ripple. If the output voltage ripple is always constant even the capacitance of the flying capacitor varies, the time constant $R_{out}C_{out}$ should be greater than the switching period $1/f_{sw}$, as expressed by (4.7)

$$R_{out}C_{out} = \frac{V_{out}^2}{P_{out}} C_{out} > \frac{1}{f_{sw}} \quad (4.7)$$

where P_{out} is the output power.

In the simulation and the experiment, three capacitances of the output capacitor and an output resistor are selected. The switching frequency f_{sw} is 100 kHz and equal to the switching period of 10 μ s. Table 4.2 shows the calculation results which are all of the time constants $R_{out}C_{out}$ for the numerous output capacitances are greater than the switching period. In the condition of the Table 4.2, the capacitance of the flying capacitor and the output voltage ripple is always independent of each other. The output voltage ripple ΔV_{out} can be expressed as (4.8).

$$\Delta V_{out} = \frac{P_{out} (\beta - 1)}{\beta V_{out} C_{out} f_{sw}} \quad (4.8)$$

From (4.8), it is obvious that the relationship between the flying capacitor and the output voltage ripple is independent. Consequently, the capacitance of the flying capacitor is designed without the consideration of the output capacitor and output voltage ripple.

Next, the design of the small capacitance of the flying capacitor $C_{fc(3\text{-level})}$ based on the maximum switching device voltage rating

$V_{DS(3\text{-level})-\max}$ is described. If Mode I in Figure 4.1 is referred, the maximum voltages across the flying capacitor $V_{fc(3\text{-level})-\max}$ and the switch S_2 $V_{S2(3\text{-level})-\max}$ are same due to the parallel connection of the flying capacitor and the switch S_2 . In addition, In Mode I, both voltages are reached up to maximum. Therefore, the maximum voltage rating of the switch $S_{2(3\text{-level})}$ is according to the maximum flying capacitor voltage. The maximum voltage rating of other switches also can be based on it.

Theoretically, in the three-level FCBC, the average voltage of the flying capacitor is half of the output voltage as expressed by (4.9). Meanwhile, from the operation mode of the three-level FCBC, the flying capacitor and drain-source terminal of MOSFETs of $S_{1(3\text{-level})}$ and $S_{2(3\text{-level})}$ are connected in parallel. Thus, the maximum voltage stresses for both devices can be expressed by (4.10).

$$V_{fc(3\text{-level})} = \frac{V_{out(\text{average})}}{2} \quad (4.9)$$

$$V_{S1(3\text{-level})-\max} = V_{S2(3\text{-level})-\max} = V_{fc(3\text{-level})-\max} \quad (4.10)$$

Figure 4.3 shows the simulation results of the waveforms of the inductor current $I_{L(3\text{-level})}$, the flying capacitor voltage $I_{fc(3\text{-level})}$, the flying capacitor voltage $V_{fc(3\text{-level})}$ and the output voltage V_{out} , respectively. The

total charge Q_{total} from charging and discharging processes for the flying capacitor current is equal to zero. Therefore, the charge for both of the charge Q_{charge} and the discharge $Q_{discharge}$ are expressed by (4.11) as in Figure 3, [51, 52, 135].

$$Q_{ch \arg e} = Q_{disch \arg e} \quad (4.11)$$

The peak-to-peak flying capacitor voltage ripple $\Delta V_{fc(3\text{-level})}$ is determined by the flying capacitor current as shown in Figure 4.3. The flying capacitor voltage ripple in the three-level FCBC $\Delta V_{fc(3\text{-level})}$ is expressed by (4.12).

$$\Delta V_{fc(3\text{-level})} = \frac{I_{in\text{-max}} D}{C_{fc(3\text{-level})} f_{sw}} = \frac{P_{in} D}{V_{in} C_{fc(3\text{-level})} f_{sw}} \quad (4.12)$$

where P_{in} is the input power.

The average flying capacitor voltage is $V_{out}/2$. Therefore, the maximum flying capacitor voltage $V_{fc(3\text{-level})\text{-max}}$ is expressed by (4.13). The maximum voltage across the switch S_2 $V_{S2(3\text{-level})\text{-max}}$ is also determined by the maximum of the flying capacitor voltage $V_{fc(3\text{-level})\text{-max}}$ as shown by (4.13). Therefore, referring to (4.13), the minimum capacitance of the flying

capacitor $C_{fc(3\text{-level})-\min}$ in the three-level FCBC is expressed by (4.14) from (4.13).

$$\begin{aligned} V_{fc(3\text{-level})-\max} &= V_{S2(3\text{-level})-\max} = \frac{V_{out}}{2} + \frac{1}{2} \Delta V_{fc(3\text{-level})} \\ &= \frac{V_{out}}{2} + \frac{1}{2} \frac{P_{in} D}{C_{fc(3\text{-level})-\min} V_{in} f_{sw}} \end{aligned} \quad (4.13)$$

$$C_{fc(3\text{-level})-\min} = \frac{P_{in} D}{(2V_{fc(3\text{-level})-\max} - V_{out})V_{in} f_{sw}} \quad (4.14)$$

Table 4.1 Specifications of the simulation and experiment for three-level and five-level FCBCs.

Specification	Value
Input Voltage V_{in}	262.5 V
Output Voltage V_{out}	350 V
Output power P_{out}	1000 W
Switching frequency f_{sw}	100 kHz
Duty ratio D	0.25
Input inductor L	200 μ H
Flying capacitor C_{fc}	0.11, 0.35, 0.6, 1.1, 5, 10, 15 μ F
Output capacitor C_{out}	1.5, 6, 9 μ F
Maximum inductor current ripple ΔI_{L-max} (for three-level FCBC)	1.1 A
MOSFET	IRFB4229PBF
SiC Schottky Diode	IDW30G65C5

Table 4.2 Time constant and switching period.

Output Capacitor C_{out}	Output Resistor R_{out}	Time Constant $R_{out}C_{out}$	Switching Period $1/f_{sw} = T$
1.5 μ F	110 Ω	165 μ s	10 μ s
6 μ F		660 μ s	
9 μ F		990 μ s	

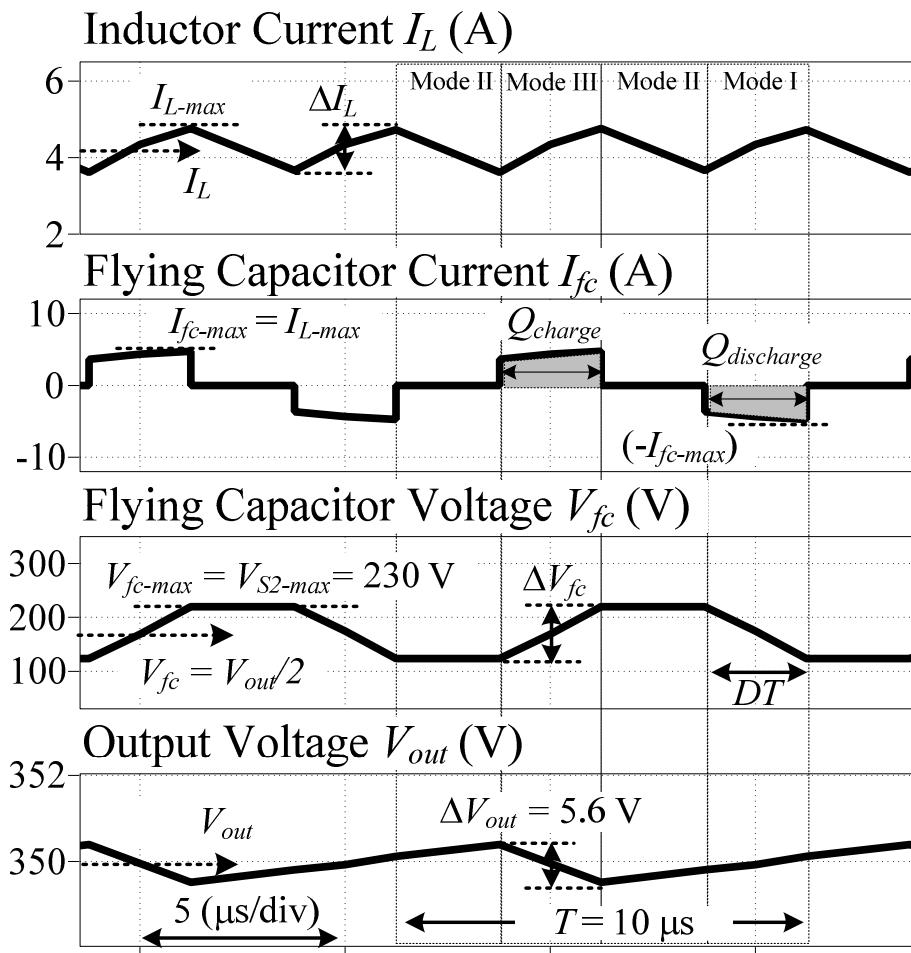


Figure 4.3 Simulation waveforms of the inductor current, the flying capacitor current, the flying capacitor voltage and the output voltage.

4.3.2 five-level FCBC

In the five-level FCBC, three flying capacitors are required which are $C_{fc1(5\text{-level})-\min}$ and $C_{fc2(5\text{-level})-\min}$, $C_{fc3(5\text{-level})-\min}$. The maximum flying capacitor voltages which are $V_{fc1(5\text{-level})-\max}$, $V_{fc2(5\text{-level})-\max}$ and $V_{fc3(5\text{-level})-\max}$ in the five-level FCBC are expressed by (4.15), (4.16) and (4.17), respectively.

$$V_{fc1(5\text{-level})-\max} = \frac{1}{4}V_{out} + \frac{1}{2} \frac{P_{in} D}{C_{fc1(5\text{-level})-\min} V_{in} f_{sw}} \quad (4.15)$$

$$V_{fc2(5\text{-level})-\max} = \frac{1}{2}V_{out} + \frac{1}{2} \frac{P_{in} D}{C_{fc2(5\text{-level})-\min} V_{in} f_{sw}} \quad (4.16)$$

$$V_{fc3(5\text{-level})-\max} = \frac{3}{4}V_{out} + \frac{1}{2} \frac{P_{in} D}{C_{fc3(5\text{-level})-\min} V_{in} f_{sw}} \quad (4.17)$$

Furthermore, capacitance of each flying capacitors in five-level FCBC are expressed by (4.18), (4.19) and (4.20), respectively.

$$C_{fc1(5\text{-level})-\min} = \frac{2P_{in} D}{(4V_{fc1(5\text{-level})-\max} - V_{out})V_{in} f_{sw}} \quad (4.18)$$

$$C_{fc2(5\text{-level})-\min} = \frac{2P_{in} D}{(4V_{fc2(5\text{-level})-\max} - 2V_{out})V_{in} f_{sw}} \quad (4.19)$$

$$C_{fc3(5\text{-level})-\min} = \frac{2P_{in} D}{(4V_{fc3(5\text{-level})-\max} - 3V_{out})V_{in} f_{sw}} \quad (4.20)$$

The maximum voltage stress on switching devices for the five-level FCBC is expressed by (4.21).

$$V_{sw(5-level)-\max} = \frac{1}{4}V_{out} + \frac{1}{2} \frac{P_{in} D}{V_{in} C_{fc1(n-level)-\min} f_{sw}} \quad (4.21)$$

4.3.3 n-level FCBC

In this section, the capacitance of the flying capacitor and the maximum voltage stress on switching devices in the n -level FCBC are explained.

The flying capacitor voltage in the n -level FCBC $V_{fcx(n-level)}$ and the required number of flying capacitor m are expressed by (4.22) and (4.23), respectively.

$$V_{fcx(n-level)} = \frac{x}{(n-1)} V_{out} \quad (4.22)$$

$$m=n-2 \quad (4.23)$$

where x is the n th of flying capacitor in n -level FCBC.

The minimum capacitance of the flying capacitor in n -level FCBC is expressed by (4.24).

$$C_{fcx(n-level)-\min} = \frac{(n-1)P_{in} D}{(2(n-1)V_{fcx(n-level)-\max} - 2xV_{out})V_{in} f_{sw}} \quad (4.24)$$

On the other hand, the ripple voltage of the flying capacitor for n -level FCBC is expressed by (4.25).

$$\Delta V_{fcx(n-level)} = \frac{P_{in} D}{V_{in} C_{fcx(n-level)} f_{sw}} \quad (4.25)$$

Therefore the maximum voltage stress on switching devices for the n -level FCBC is expressed by (4.26).

$$V_{sw(n-level)-\max} = \frac{1}{(n-1)} V_{out} + \frac{1}{2} \frac{P_{in} D}{V_{in} C_{fc1(n-level)-\min} f_{sw}} \quad (4.26)$$

4.4 Experimental Results

In order to confirm the operation of the FCBC under the minimum capacitance of the flying capacitor and the maximum voltage stress on switching devices in the n -level FCBC, three-level and five-level FCBCs prototypes are constructed. The specifications of the experiment and simulation conditions are shown in Table 4.1.

Figure 4.4 shows the experimental waveforms of the flying capacitor voltage ripples and the output voltage ripple when the output capacitance is $1.5 \mu\text{F}$ and the capacitances of the flying capacitors are $1.1 \mu\text{F}$ and $0.35\mu\text{F}$ in the three-level and five-level FCBCs. From Figures 4.4(a) and 4.4(b), it is confirmed that the peak-to-peak output voltage ripple is always 5.6 V at the three-level FCBC although various capacitance of the flying capacitor are used. In addition, the output voltage ripple is always 5.6 V at both of the three-level FCBC and the five-level FCBC although various capacitances of the flying capacitor are used. These experimental results are agreed with the theoretical analysis in the section III whereby the relationship between capacitances of the flying capacitor and the output voltage ripple are independent.

Besides, Figure 4.4 shows the flying capacitor voltage ripples in the three-level and five-level FCBCs when the capacitance of the flying capacitor of $1.1 \mu\text{F}$ and $0.35 \mu\text{F}$ are used. From these results, the flying capacitor voltage ripples are same when same capacitance of the flying capacitors is used. The flying capacitor voltage ripples are approximately 10 V and 29 V, respectively as shown in Figure 4.4. Therefore, it is confirmed that the experimental result agrees with the theoretical analysis shown in the section III.

Figure 4.5(a) shows the experimental waveforms of the voltage of the switch S_2 is 230 V when the capacitance of the flying capacitor which of $0.11 \mu\text{F}$ is used in the three-level FCBC. Experimental value of the maximum voltage of the switch S_2 agrees with the calculated value which is 230 V by (4.13).

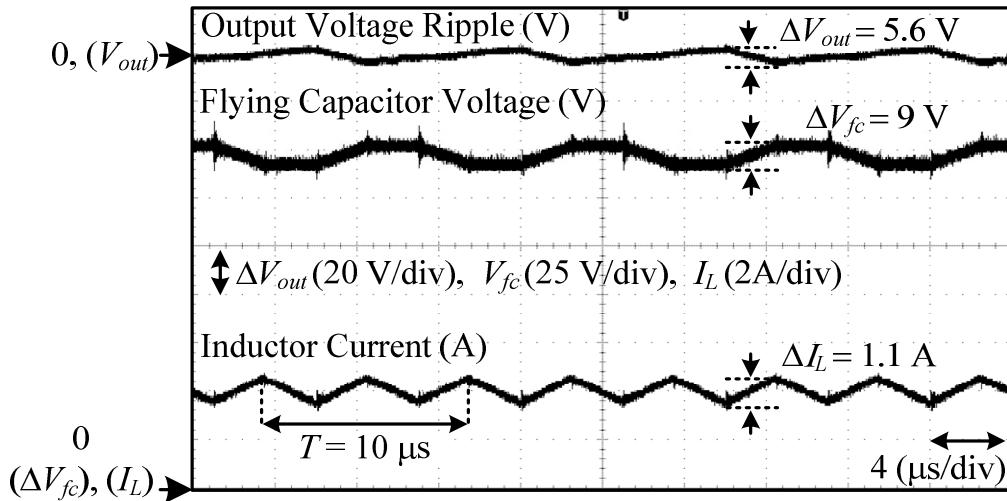
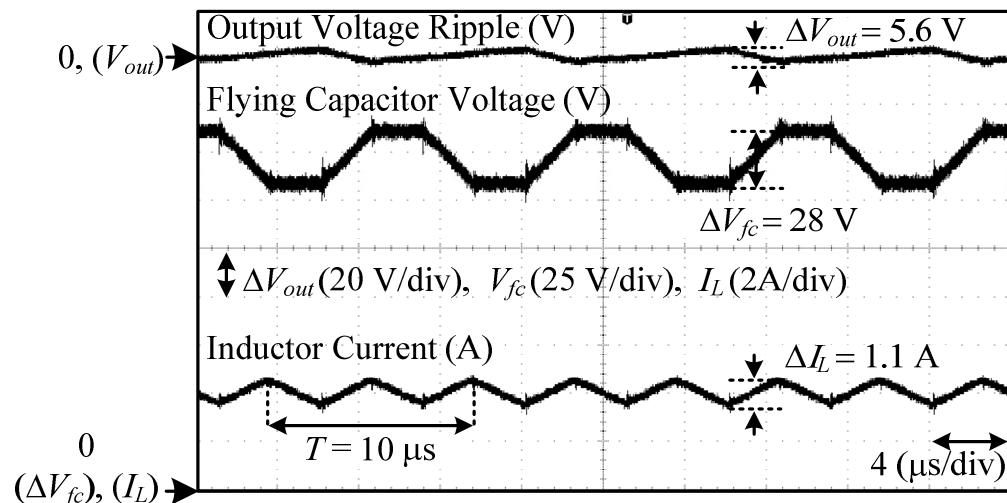
(a) three-level FCBC: $C_{out} = 1.5 \mu\text{F}$, $C_{fc} = 1.1 \mu\text{F}$.(b) three-level FCBC: $C_{out} = 1.5 \mu\text{F}$, $C_{fc} = 0.35 \mu\text{F}$.

Figure 4.4 (a), (b): Experimental waveforms of the output voltage, the flying capacitor voltage and the inductor current in three-level FCBC; (c), (d): Experimental waveforms of the flying capacitor voltage ripples and the output voltage ripple in five-level FCBC.

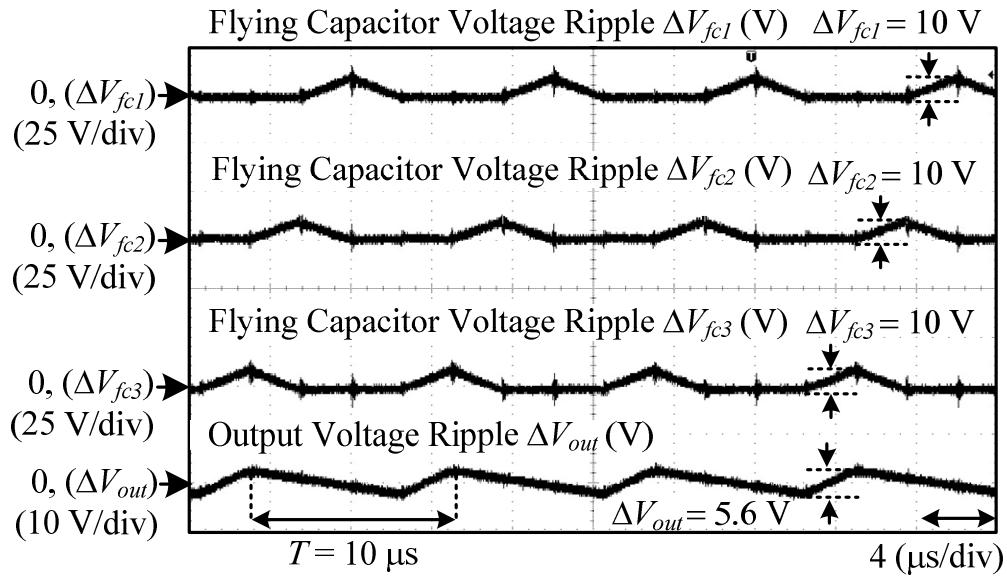
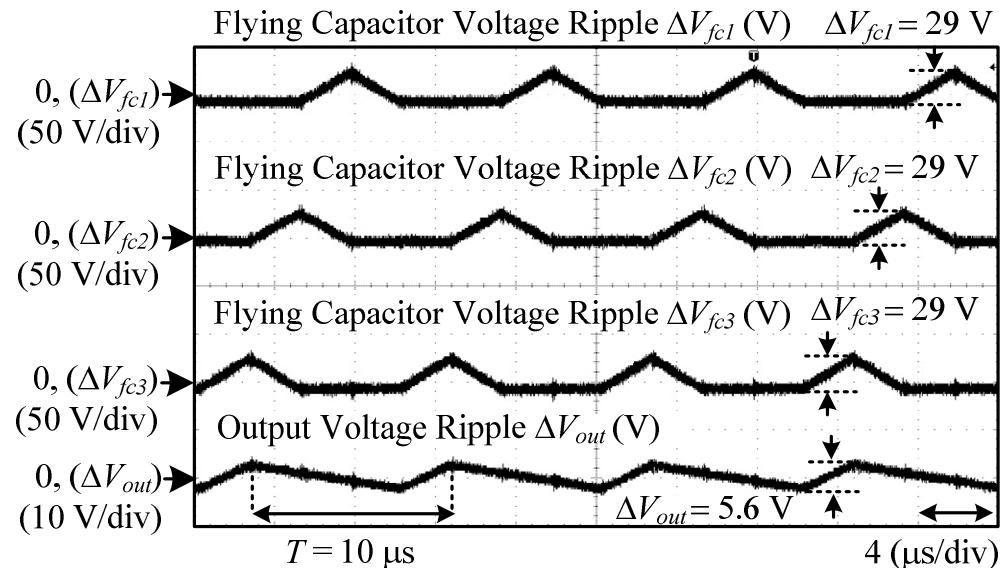
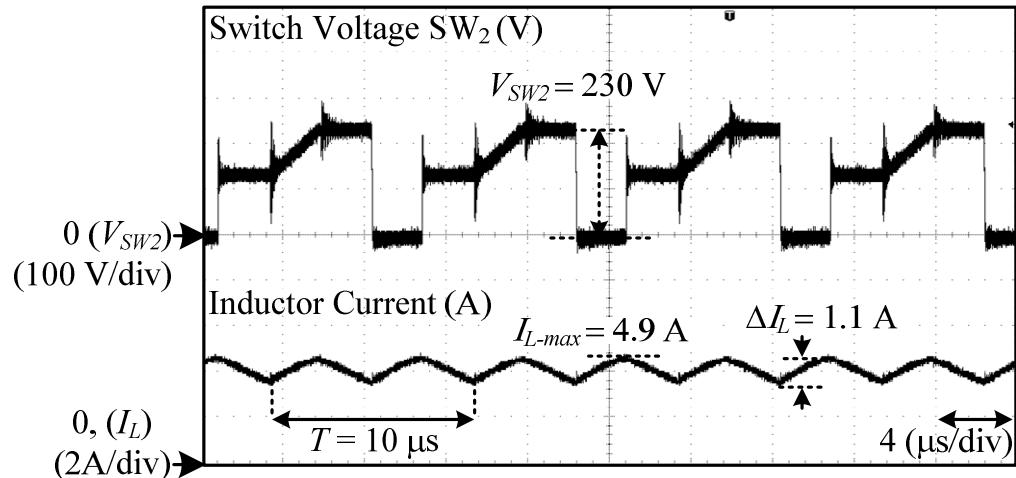
(c) five-level FCBC: $C_{out} = 1.5 \mu\text{F}$, $C_{fc} = 1.1 \mu\text{F}$.(d) five-level FCBC: $C_{out} = 1.5 \mu\text{F}$, $C_{fc} = 0.35 \mu\text{F}$.

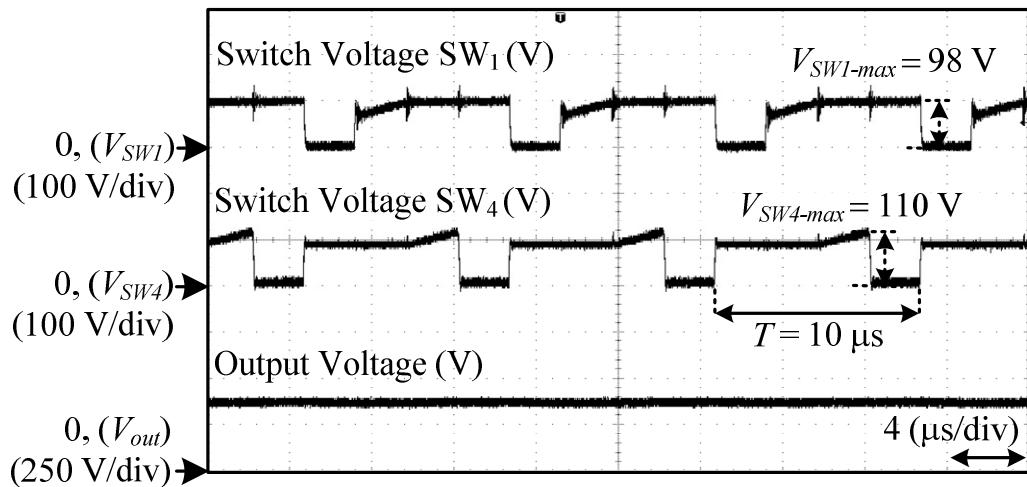
Figure 4.4 (a), (b): Experimental waveforms of the output voltage, the flying capacitor voltage and the inductor current in three-level FCBC; (c), (d): Experimental waveforms of the flying capacitor voltage ripples and the output voltage ripple in five-level FCBC.

Besides, Figure 4.5(b) shows the experimental waveform of the switch voltages S_1 and S_4 when the capacitance of the flying capacitor of $0.35 \mu\text{F}$ is used in the five-level FCBC. The experimental maximum switch voltage of S_4 is 110 V. It is confirmed that the experimental value agrees with the calculated value based on (4.21).

Furthermore, the voltage across a switching device is determined based on the flying capacitor voltage ripple and capacitance of the flying capacitor. Thus, the design method to determine the minimum capacitance for the flying capacitor was experimentally verified.



(a) three-level FCBC.



(b) five-level FCBC.

Figure 4.5 (a) Experimental waveforms of the switch S_2 voltage and the inductor current in the three-level FCBC; (b) Experimental waveforms of the switch voltages (S_1 and S_4) and the output voltage in the five-level FCBC.

4.5 The Effectiveness of Small Capacitance of Flying Capacitor

4.5.1 Ripple voltage of the flying capacitor characteristic

Figure 4.6 shows the relationship between flying capacitor voltage ripples and several capacitances of the flying capacitors in the three-level and five-level FCBCs. It is confirmed that each voltage ripple of the flying capacitors are same when same capacitance of the flying capacitor is selected in the three-level and five-level FCBCs although five-level FCBC has different switching patterns and three different flying capacitor voltages. As a result, it is experimentally confirmed that the ripple voltage of the flying capacitor voltage does not depend on the number of level as shown in (4.25). Besides, it is confirmed that the flying capacitor voltage ripples is reduced with regard to the increasing capacitances of the flying capacitor as shown in (4.25).

The increasing of the flying capacitor voltage ripples will contribute into switching loss of the semiconductor switches. However the performance of high voltage semiconductor switches is improving recently.

Therefore, high flying capacitor voltage ripple is acceptable although small capacitance of the flying capacitor is used.

The flying capacitor voltage ripples are same in the three-level and five-level FCBCs when same capacitance of the flying capacitor is considered even the number of the levels are different. Therefore, the capacitance of the flying capacitor can be reduced by considering the constant ratio of the flying capacitor voltage ripples against capacitances of the flying capacitor. In order to design the minimum capacitance of the flying capacitors in the five-level FCBC, (4.18)-(4.20) are referred.

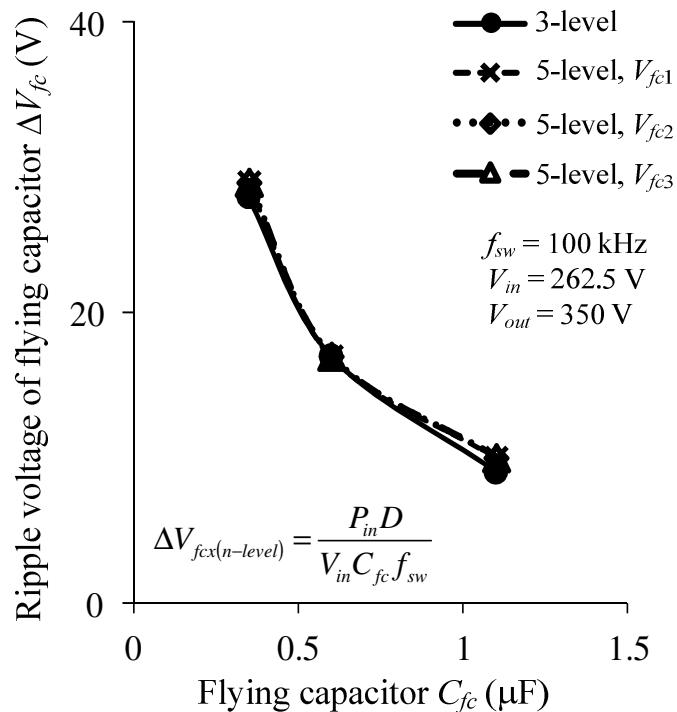


Figure 4.6 Experimental results of the flying capacitor ripple voltage with various of capacitances of the flying capacitors.

4.5.2 Harmonics analysis of the voltage across the input voltage source and the input inductor, and the current to the output side in the three-level and five-level FCBCs

Figure 4.7(a) shows the experimental results of the k_{iout} which is the ratio between the effective values of distorted components I_{nfs_w} against DC component I_{dc} , which is introduced in order to evaluate the distorted current to the output side which is the output capacitor and the load. The results show ratio of k_{iout} converges into a constant value with various capacitances of the flying capacitors. Therefore, the ratio of k_{iout} is not affected on the variation of capacitances of the flying capacitors although small capacitance is used. Thus, the small capacitances can be used for the flying capacitor in the three-level and five-level FCBCs.

Figure 4.7(b) shows the experimental results of the k_{vconv} which is the ratio between the effective values of distorted components V_{nfs_w} against DC component V_{dc} , which is introduced in order to evaluate the distorted voltage across the input voltage source and the input inductor. It is confirmed that the ratio k_{vconv} converges into a constant value when the capacitance of the flying capacitor is increased.

From Figure 4.7, the small capacitance can be used for the flying capacitor in both three-level and five-level FCBCs. From these experimental results, five-level FCBC has obviously lower k_{vconv} compared to the three-level FCBC. Thus the k_{vconv} has significant difference when the level is increased. Meanwhile, five-level FCBC also has lower k_{iout} compared to the three-level FCBC. However the different is small.

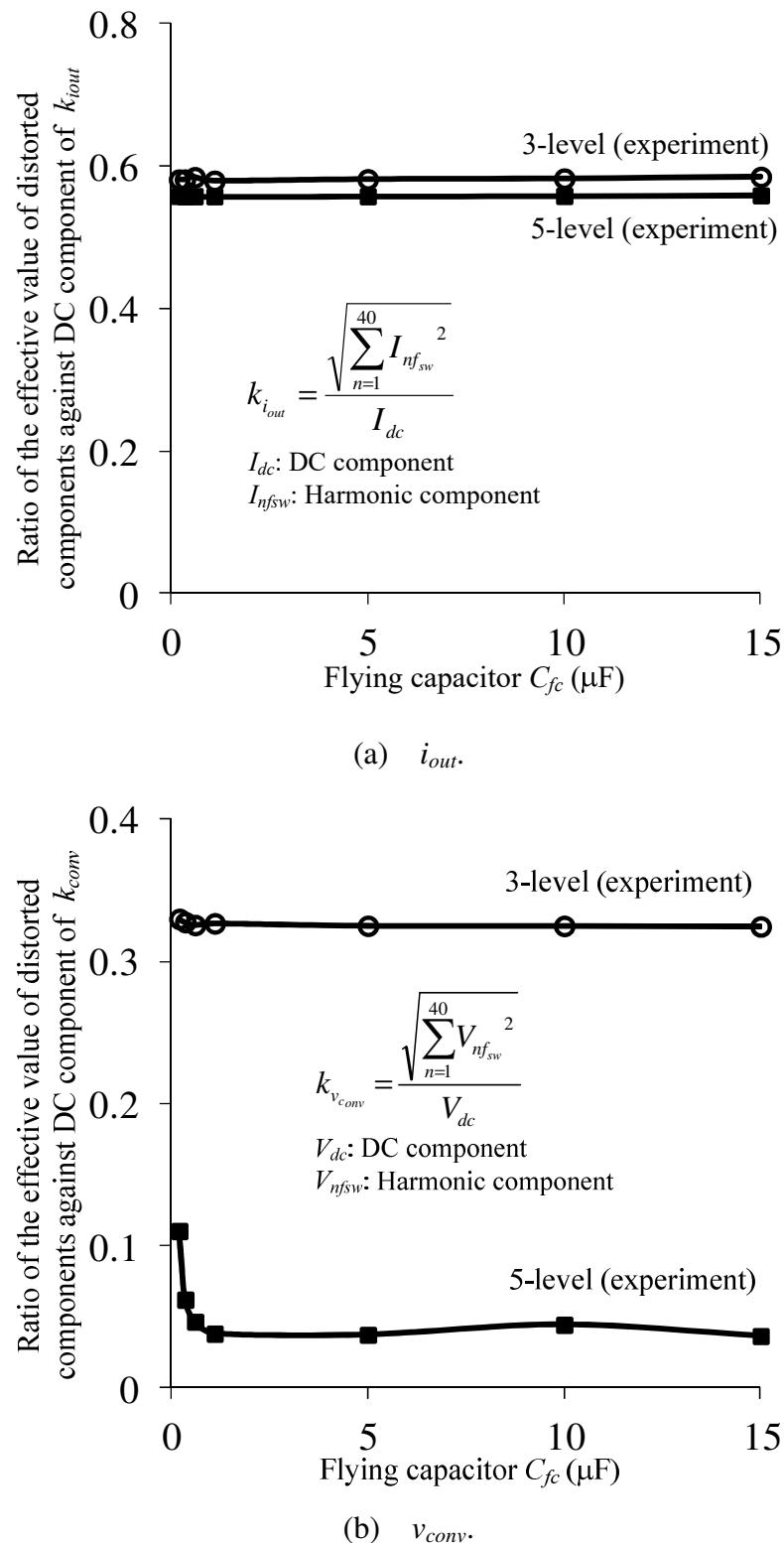


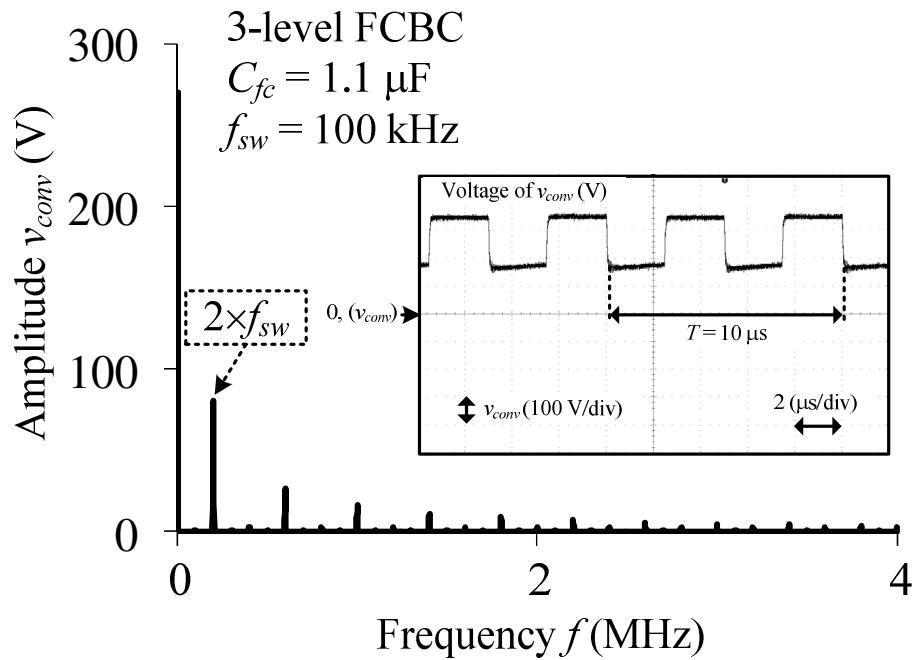
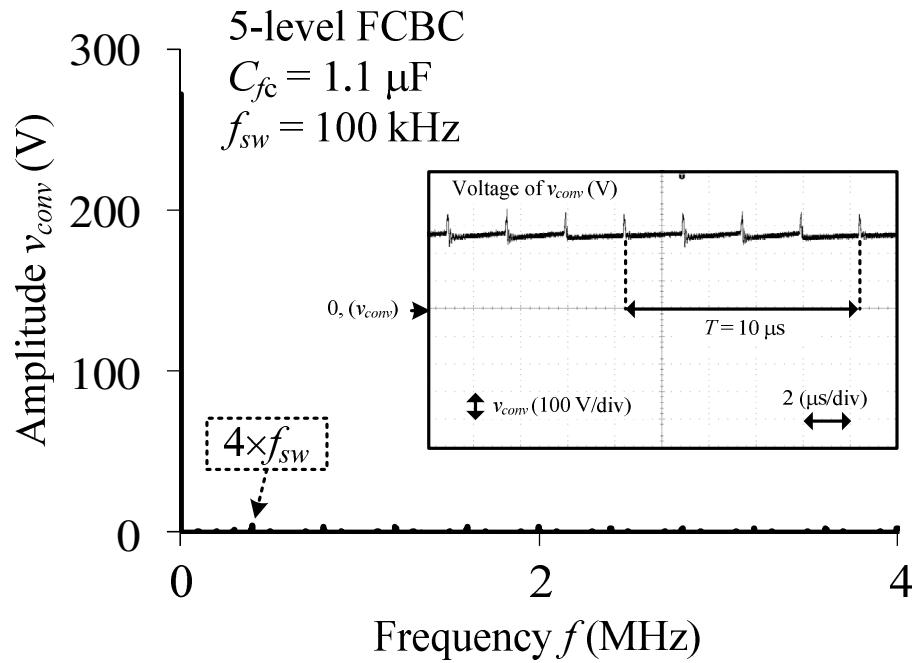
Figure 4.7 Ratio of the effective value of distorted components against DC component.

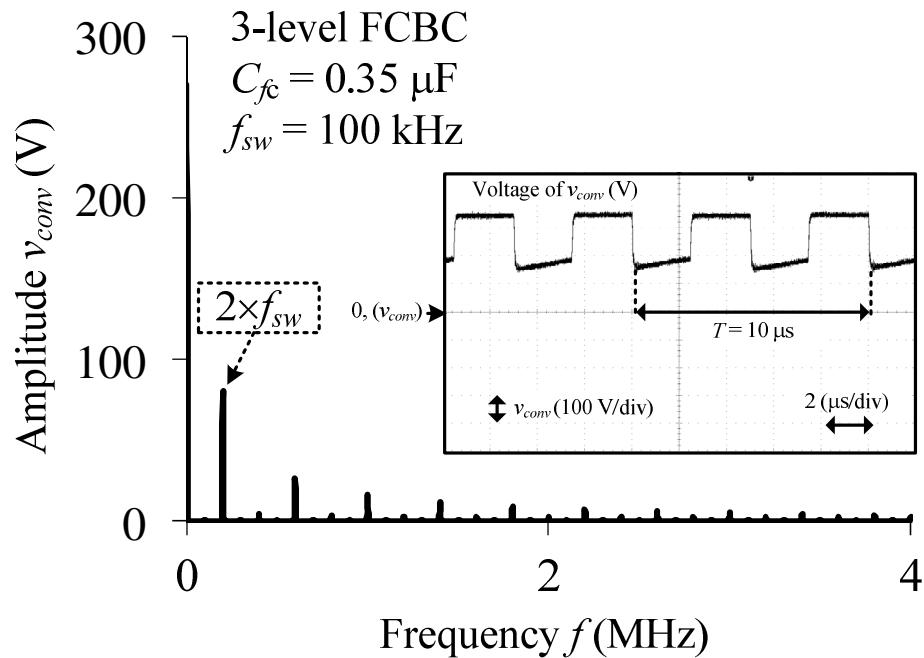
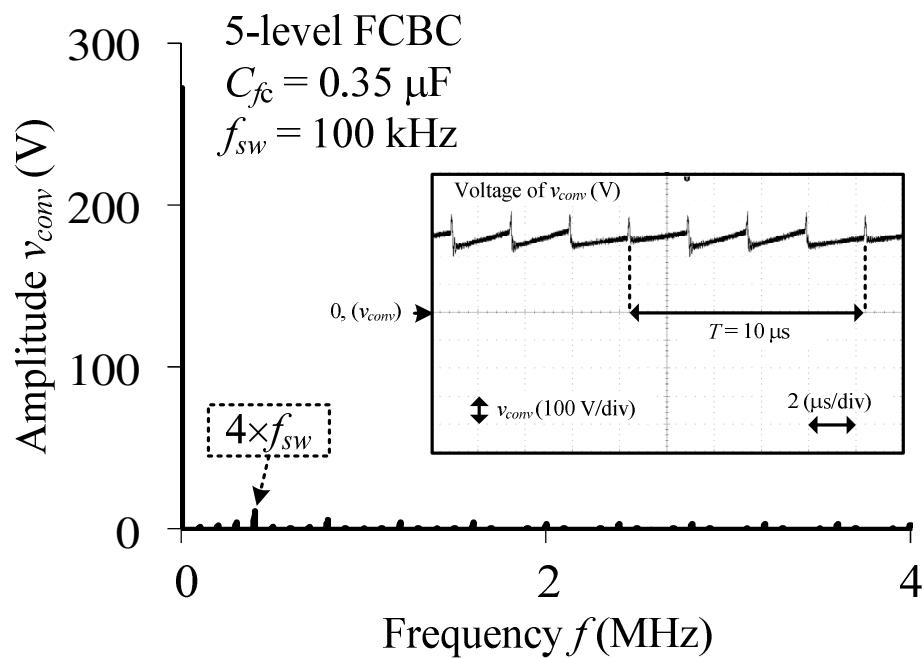
4.5.3 Harmonics components of v_{conv} and i_{out} in the three-level and five-level FCBCs

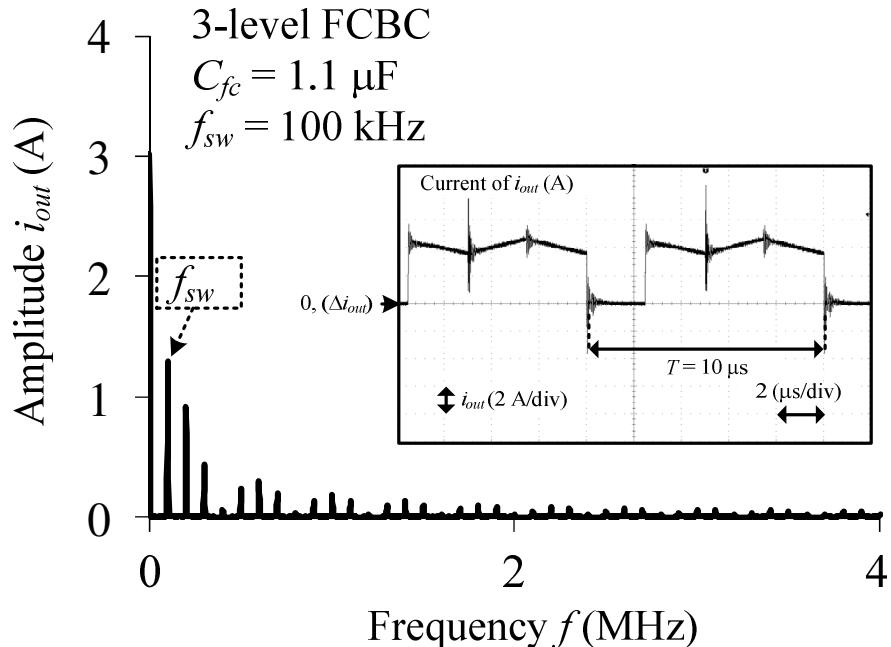
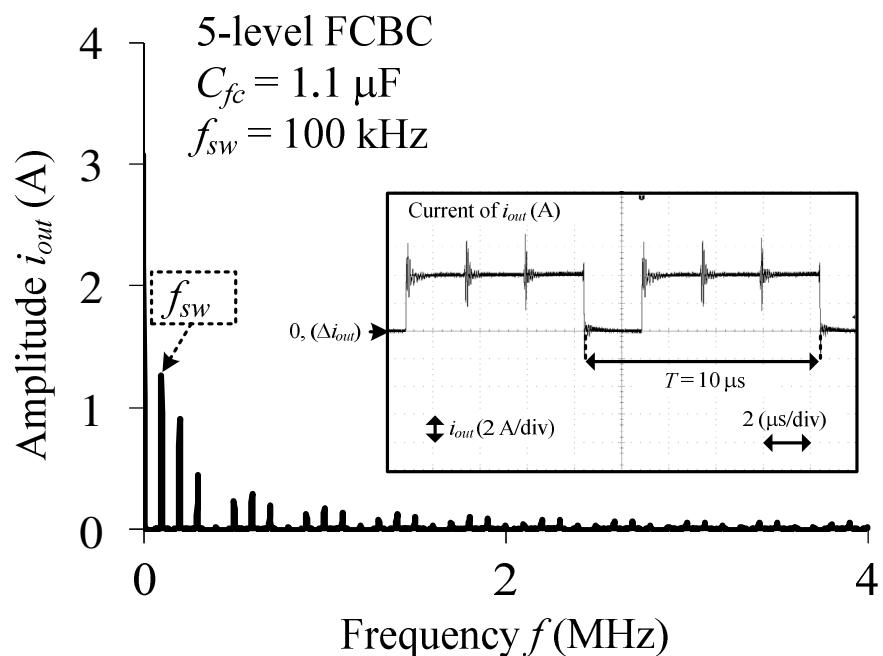
Figure 4.8 shows the harmonics spectrum of v_{conv} and i_{out} with various capacitances of the flying capacitors in the three-level and five-level FCBCs. For these experimental results, only two capacitances of the flying capacitors are selected which are 1.1 μ F and 0.35 μ F.

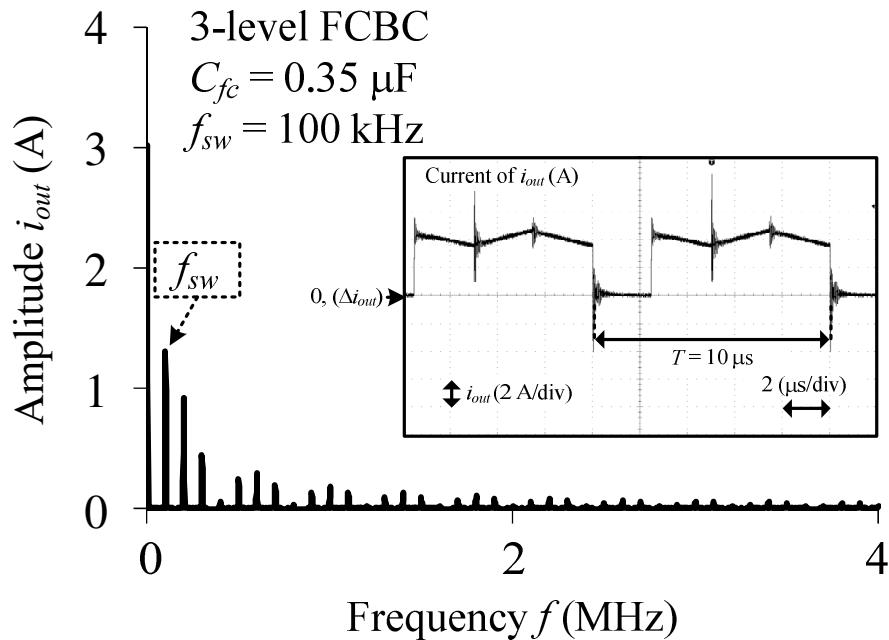
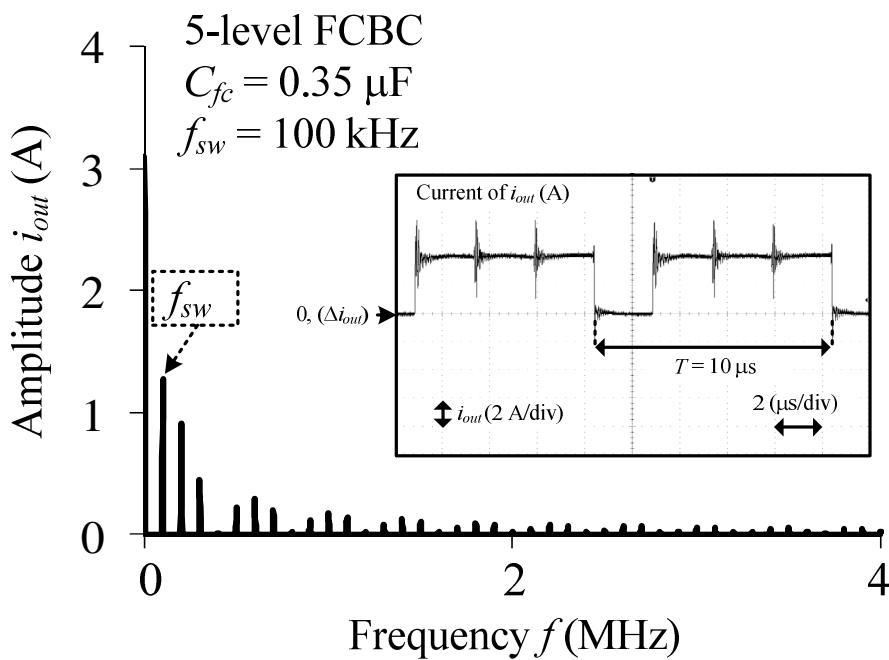
Figures 4.8(a), 4.8(b), 4.8(c) and 4.8(d) show the harmonics spectrum of v_{conv} in the three-level and five-level FCBCs. From these experimental results, five-level FCBC has obviously lower harmonic components compared to the three-level FCBC when capacitances of 1.1 μ F and 0.35 μ F for the flying capacitor are used.

Meanwhile, Figures 4.9(a), 4.9(b), 4.9(c) and 4.9(d) show the harmonic components of i_{out} in the three-level and five-level FCBCs. From these results harmonics spectrum, the patterns between three-level and five-level FCBCs are almost same. The difference of harmonic components is not obvious because the ripple current of i_{out} is not different from between two FCBCs due to their operation modes.

(a) Three-level FCBC: v_{conv} components, $C_{fc} = 1.1 \mu\text{F}$.(b) Five-level FCBC: v_{conv} components, $C_{fc} = 1.1 \mu\text{F}$.Figure 4.8 Harmonics components of v_{conv} .

(c) Three-level FCBC: v_{conv} components, $C_{fc} = 0.35 \mu\text{F}$.(d) Five-level FCBC: v_{conv} components, $C_{fc} = 0.35 \mu\text{F}$.Figure 4.8 Harmonics components of v_{conv} .

(a) Three-level FCBC: i_{out} components, $C_{fc} = 1.1 \mu\text{F}$.(b) Five-level FCBC: i_{out} components, $C_{fc} = 1.1 \mu\text{F}$.Figure 4.9 Harmonics components of i_{out} .

(c) three-level FCBC: i_{out} components, $C_{fc} = 0.35 \mu\text{F}$ (d) five-level FCBC: i_{out} components, $C_{fc} = 0.35 \mu\text{F}$ Figure 4.9 Harmonics components of i_{out} .

4.6 Conclusion

In this study, the authors revealed the minimum capacitance of the flying capacitor consideration in multi-level FCBC based on the switching device voltage rating. Moreover, the relationship between the capacitance of the flying capacitor and the output voltage ripple is independent of each other and it was confirmed by simulation and experimental results. Meanwhile, the minimum capacitance based on the maximum voltage rating of switching devices was confirmed by the experimental results in the three-level and five-level FCBCs. Besides the expression clarification in order to design minimum capacitance of the flying capacitor in the n -level FCBC is also shown. Then, the distortion of the voltage across the input voltage source and the input inductor is measured. In addition, the distortion of the current to the output side which is the output capacitor and the load is also measured. As a result, it is experimentally confirmed that a small capacitance of the flying capacitors can be used in the three-level, five-level and n -level FCBCs.

Chapter 5

Design and Implementation of the High Boost Ratio Multistage Marx Topology DC-DC Converter and Interleaved Operation Considerations

5.1 Introduction

DC-DC converter with high boost ratio is required for low DC voltage energy sources such as for electric vehicle (EV) system, fuel-cells system and photovoltaic (PV) systems. These systems usually need low-voltage and high-current power converters in order to supply DC power to a DC bus or a load.

In a conventional DC-DC boost converter, a high boost ratio can be achieved by connecting those converters in cascade connection [143]. However, this topology cannot achieve high efficiency due to a number of

required cascade-connected DC-DC converters. Especially, high conduction losses occur at input side due to large input current. Besides, generally DC-DC converters using high frequency transformers are also used in order to obtain a high boost ratio [143-147]. However, those converters usually suffer from the bulkiness and large losses due to the bulky transformer. In addition, leakage current causes false operation of the DC-DC converter due to the parasitic capacitance and high voltage difference between the transformer windings. On the other hand, a high boost ratio is achieved with switched capacitor DC-DC converters [79, 148, 149]. However, the output voltage stress on the output capacitor is very high due to high output voltage and it requires many capacitors connected in series. Meanwhile, with diode clamped converters, the low on-resistance of switching devices is difficult to be achieved due to high voltage stress at the output side [150-152]. Especially if a high boost ratio is considered, those circuit configuration is not practical.

Besides, a Marx generator topology is one of an attractive topology that able to achieve a high boost ratio in DC-DC converter. Basically the purpose of Marx generator is to generate a high-voltage pulse from a

low-voltage DC source [153, 154]. However, the conventional Marx generator has high conduction losses and copper losses due to large input current. As a result, the efficiency of the conventional Marx generator is low. Therefore the main application of the Marx generator is limited for low power applications. On the other hand, the Marx topology DC-DC converters with resonant condition operation are proposed in order to achieve the ZCS condition [92, 153, 155]. However, due to the resonant condition, the input inductor current should be in discontinuous current mode (DCM) and consequently the input inductor is bulky. Furthermore the conduction loss is also increased.

This paper proposes a new high boost ratio of a Marx topology DC-DC converter. In the proposed circuit, the parallel-connection of conventional two-level boost DC-DC converters are applied at the input side in order to reduce the conduction loss and the copper loss. In addition, the multi-stage connections are applied at the output side in order to reduce the voltage rating of stage capacitors and switches. Meanwhile, voltage stress of the lower switches side in the input side is same to that of components at the output side. Therefore, lower voltage semiconductors which have low

on-resistance can be used for the switches in the proposed circuit. Meanwhile, high voltage rating diodes at the input side are required. However, high voltage rating of SiC diodes which have low forward voltage and low reverse recovery time can be used nowadays. As a result, a high-efficiency boost converter can be achieved.

This paper is organized as follows. First, the principle of the n -stage Marx topology DC-DC converter is described. Then, the input inductors and stage capacitors designs on each stage are established. The relationship between the voltage stress on stage capacitors and the number of stages is evaluated. Furthermore, the loss distribution analysis based on a theoretical analysis is clarified for MOSFETs, diode and copper losses estimation. Then, the converter efficiency and the total power loss at each of the output power based on measurement values are discussed. All measurement values are based on the 3-stage MTBC. The interleaved operation of the three-stage MTBC is confirmed experimentally for the output inductor reduction and the current stress reduction on bottom switch. Finally, power density comparisons are conducted theoretically between three-stage MTBC and other topologies.

5.2 Converter Principle and Circuit Configuration

Fig. 5.1 shows the operation of the conventional multilevel Marx circuit impulse generator operation [156, 157]. Principally, in order to generate very high voltage, a bank of capacitors C are connected in parallel for charging process, then connecting the same capacitors C in series for discharging process through the spark gaps G . Thus, very high DC pulse voltage can be generated at the output side from this arrangement. The purpose of charging resistor R_S is to limit the charging current. Meanwhile the discharging time constant is very small as compared to the charging time constant, hence no discharge condition occurs through the charging resistor R_S . Some of the impulse generator applications are for fabric sterilizations, photolithography and pulsed X-ray [158-161].

Based on the circuit operation, parallel-series connection of capacitors has advantages of current stress reduction at the input side and voltage stress reduction at the output side. Besides, practically this conventional multistage Marx impulse circuit configuration is not suitable for a power converter application due to a high loss on charging resistors R_S , low operation frequency, short life-time on the gaps G and the volume is high

especially if sphere gaps are used. The original circuit configuration can be modified and improved by replacing the gaps G with semiconductor devices and avoiding the usage of charging resistor R_S . In this paper, the conventional Marx impulse circuit configuration is adopted into a DC-DC converter whereby a high boost ratio is realized as shown in Fig. 5.2.

Figure 5.2 shows a circuit configuration of the n -stage Marx topology boost converter (MTBC). Basically, each stage of the MTBC consists of a conventional two-level boost DC-DC converter, a capacitor and two additional switches. The converter is designed based on a principle of the Marx pulse generator whereby a high-output voltage is generated from a low-voltage DC source [153]. This principle is realized by charging several capacitors in parallel and then suddenly connecting those capacitors in series. Therefore, by arranging these combinations of capacitors in the proposed converter, a high output voltage is generated. It is noted that 10 to 20 stages might be required in order to reduce input currents stress, switching devices voltage rating and stage capacitor voltages stress in the actual application. In addition, this proposed topology has a modular feature at the output side, which is on each stage, the stage capacitors and

additional two switching devices having same voltage stress characteristics, as shown in Figure 5.2.

In order to analyze the MTBC operation and its characteristic, a three-stage MTBC is introduced as a specific example in this section. In principle, the relationship between the input voltage V_{in} and the output voltage V_{out} is expressed as follows:

$$V_{out} = \beta V_{in} \quad (5.1)$$

where β is the boost ratio. Meanwhile the duty ratio D in terms of boost ratio β can be expressed as follows:

$$D = \frac{1}{1 + \frac{n}{\beta}} \quad (5.2)$$

where D is the duty ratio for the switches S_{1a} , S_{1b} , S_{2a} , S_{2b} , S_{3a} and S_{3b} and n is the number of stage. Thus the output voltage V_{out} in terms of the duty ratio D , the number of stage n and the input voltage V_{in} can be rewrite as follows:

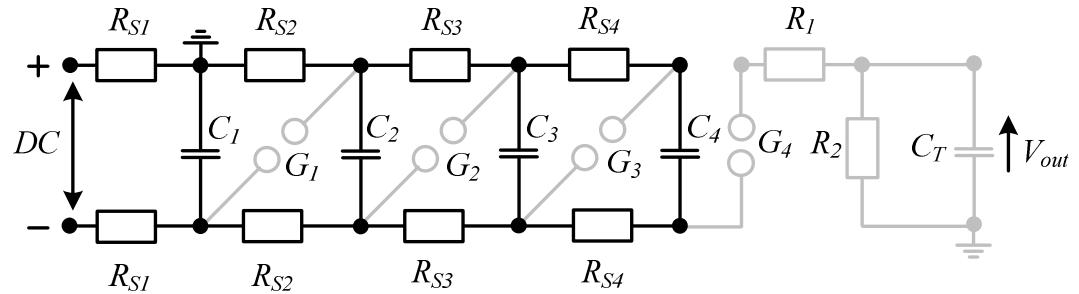
$$V_{out} = \left(\frac{D}{1 - D} \right) n V_{in} \quad (5.3)$$

Figures 5.3 and 5.4 show the switching pattern and operation mode of the three-stage MTBC, respectively. The switching pattern with dead-time

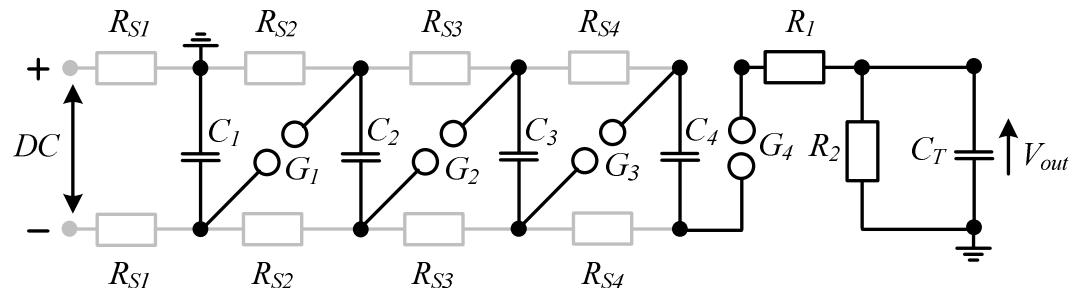
T_d and additional time-delayed T_a is considered for reducing of surge voltage of the switch. The three-stage MTBC needs four operation modes.

Table 5.1 shows the conditions of the stage capacitors. The stage capacitors C_1 , C_2 and C_3 are charging when those capacitors are connected in parallel as shown in Figure 5.4. Then, those stage capacitors are connected in series during discharging condition as shown in Figure 5.4. Thus, the output voltage is boost-up by the advantage of a series connection of the stage capacitors. Therefore, a high boost ratio is achieved.

The voltage stresses on the switching devices S_{1a} , S_{1b} , S_{1c} , S_{2a} , S_{2b} , S_{2c} , S_{3a} , S_{3b} and S_{3c} are determined by each of the maximum stage capacitor voltages V_{C1} , V_{C2} and V_{C3} . Each stage capacitor voltage is lower than the output voltage. Therefore, lower voltage stress semiconductors which have low on-resistance can be used. Meanwhile, the voltage stresses on the diodes D_1 , D_2 and D_3 are equal to the V_{C1} , $2V_{C2}$, and $3V_{C3}$, respectively. Thus the top diode voltage stress is equal to total stage capacitor voltage stresses. However, high voltage SiC diodes which have low forward voltage and low reverse recovery time can be used nowadays.

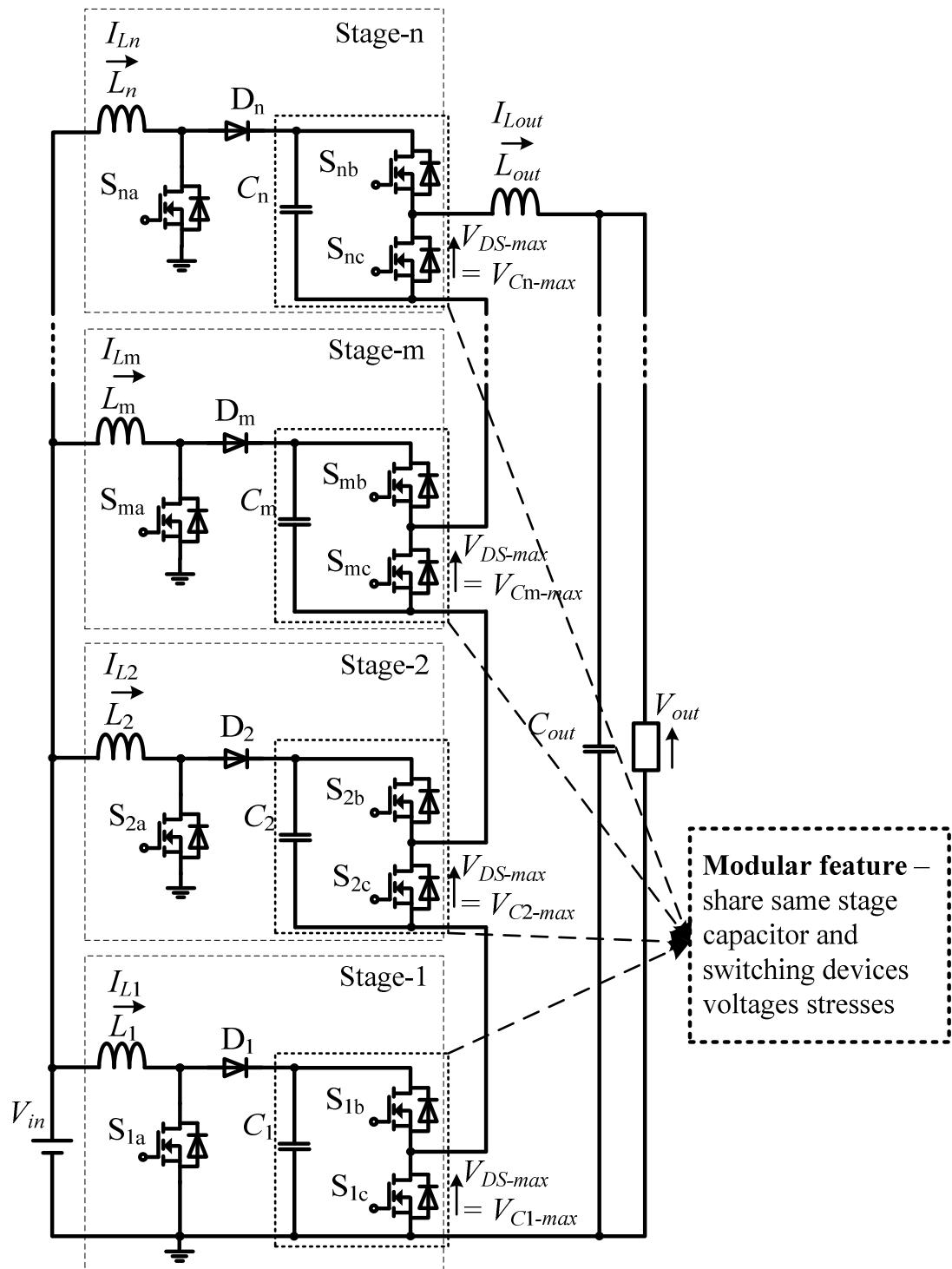


(a) Capacitors are charging in parallel.



(b) Capacitors are discharging in series.

Figure 5.1 Conventional multistage Marx impulse generator operation [156, 157].

Figure 5.2 n -stage MTBC circuit configuration.

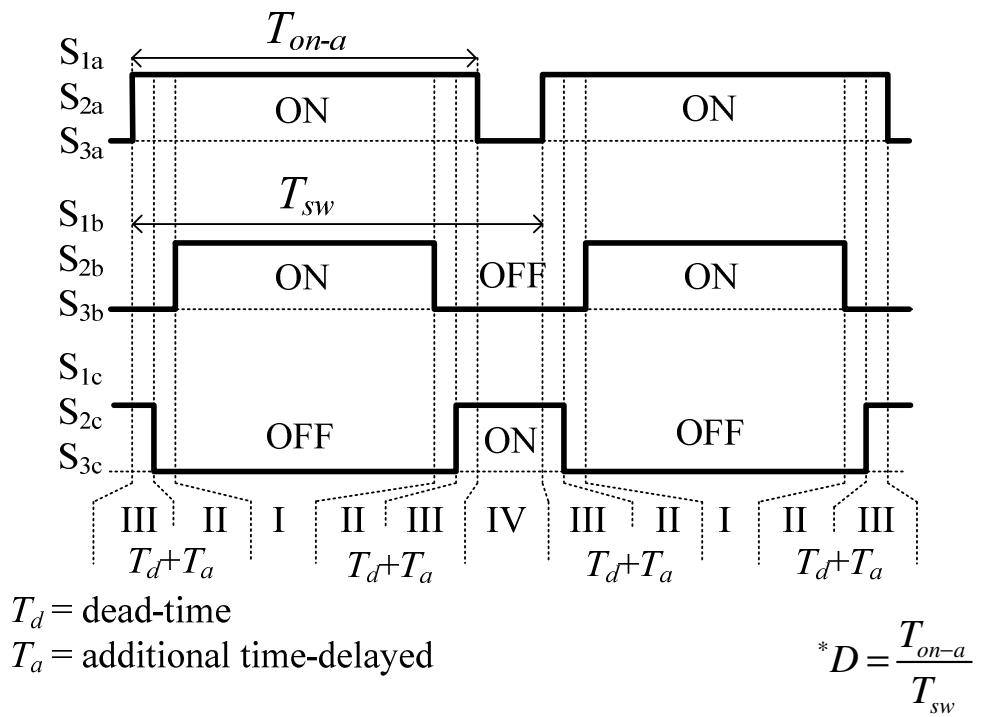


Figure 5.3 Switching pattern.

Table 5.1 Stage capacitor operation on three-stage MTBC.

Mode	S_{1a}, S_{2a}, S_{3a}	S_{1b}, S_{2b}, S_{3b}	S_{1c}, S_{2c}, S_{3c}	C_1, C_2, C_3
(I)	ON	ON	OFF	Discharging in series
(II)	ON	OFF	OFF	Unchanged
(III)	ON	OFF	ON	Unchanged
(IV)	OFF	OFF	ON	Charging in parallel

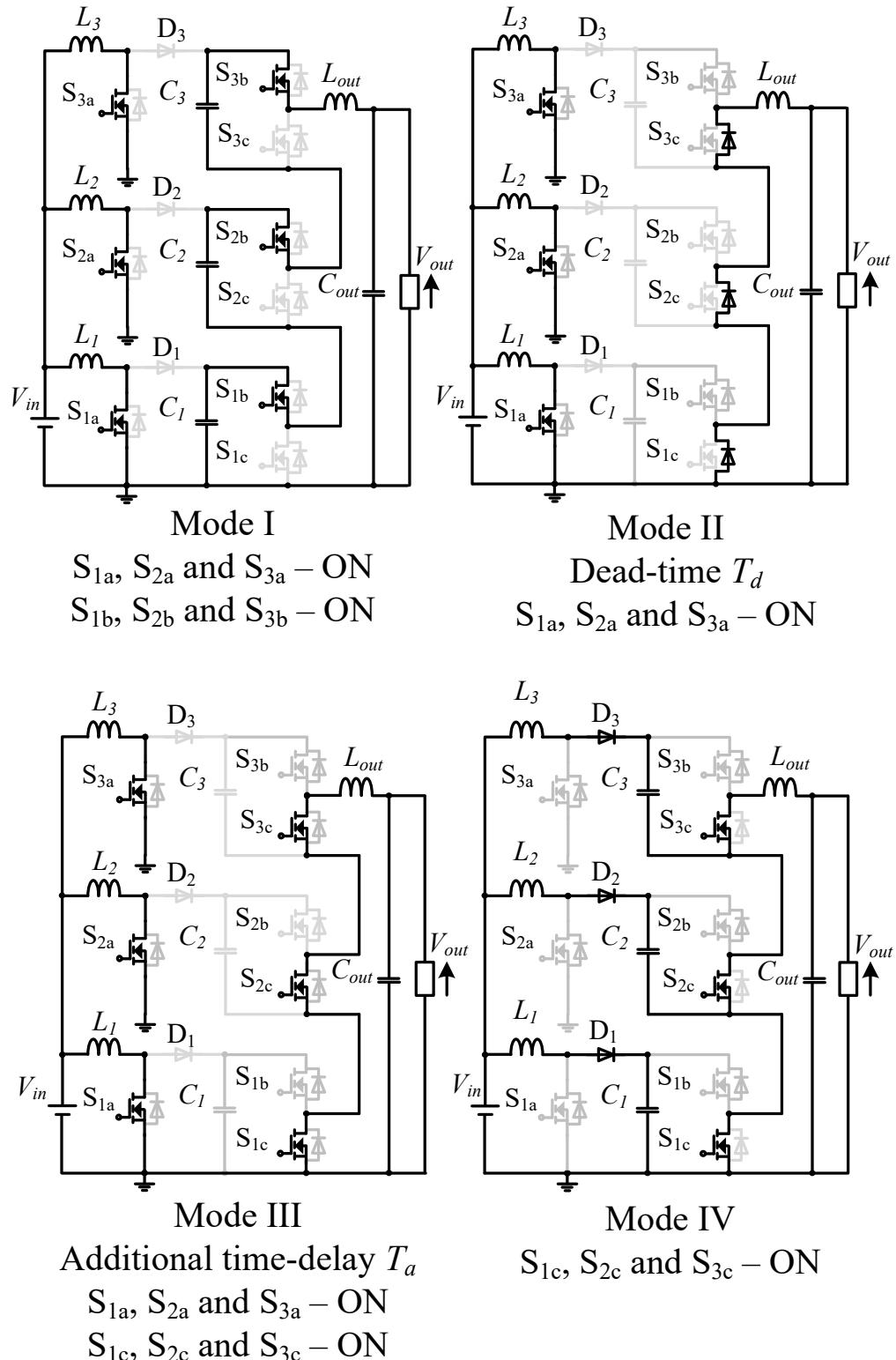


Figure 5.4 Operation mode of the three-stage MTBC.

5.3 Passive Components Design and Selection

In this section, the inductor current of each stage in the MTBC is designed to be operated in continuous current mode (CCM) in order to minimize the peak input current. Thus the minimum inductor current of each stage should be greater than zero in order to ensure a CCM condition is achieved. Then the minimum inductance of the input inductor of each stage $L_{in(m)}$ for CCM operation is expressed as follows:

$$L_{in(m)} > \frac{n(V_{in})^2 D}{2 P_{out} f_{sw}} \quad (5.4)$$

where m is the stage, n is the number stage, P_{out} is the output power and f_{sw} is the switching frequency. Meanwhile the inductor current ripple on each stage $\Delta I_{Lin(m)}$ can be expressed as follows:

$$\Delta I_{Lin(m)} = \frac{V_{in} D}{f_{sw} L_{in(m)}} \quad (5.5)$$

The capacitance of the stage capacitor is expressed as follows:

$$C_{(m)} = \frac{I_{L(m)-ave} (1 - D)}{\Delta V_{C(m)} f_{sw}} = \frac{P_{in} (1 - D)}{n V_{in} \Delta V_{C(m)} f_{sw}} \quad (5.6)$$

where $C_{(m)}$ is the capacitance of the stage capacitor and $\Delta V_{C(m)}$ is the stage capacitor voltage ripple.

Principally, the maximum stage capacitor voltage $V_{C(m)-max}$ and the average inductor current on each stage $I_{L(m)-ave}$ are expressed as follow:

$$V_{C(m)-max} = V_{DS-max} = V_{in} + \frac{V_{out}}{n} \quad (5.7)$$

$$I_{L(m)-ave} = \frac{P_{in}}{nV_{in}} \quad (5.8)$$

where V_{DS-max} is the maximum drain-source voltage of a MOSFET, P_{in} is the input power.

According to the circuit arrangement as shown in Figure 5.4, the maximum stage capacitor voltage is equal to the maximum of drain-source voltage of MOSFETs as shown by (5.7). Furthermore, the maximum stage capacitor voltage and average stage current are inversely proportional to the number of stage as shown by (5.7) and (5.8). Thus the maximum stage capacitor voltage and average stage current will be reduced according to the increasing the number of stage n .

5.4 Loss Analysis Based on Theoretical Equation

The theoretical loss analysis is conducted in order to clarify the losses of MOSFETs, diodes and copper (input and output inductors copper windings), respectively in the 3-stage MTBC. In this section, the effective and average currents for the MOSFETs and diode are derived mathematically for loss analysis calculation. Then, the conduction power losses of the MOSFET and diode in the three-stage MTBC are analyzed theoretically.

5.4.1 Conduction loss for MOSFETs S_{1a} , S_{2a} and S_{3a}

Principally, the effective currents of $i_{S1a(eff)}$, $i_{S2a(eff)}$ and $i_{S3a(eff)}$ are same because the input side of the MTBC are synchronized. The effective current is expressed as follows:

$$i_{S1a(eff)} = i_{S2a(eff)} = i_{S3a(eff)} \quad (5.9)$$

$$i_{S1a(eff)} = \left(\frac{\left(I_{Lin_max}^2 - 2I_{Lin_min}I_{Lin_max} + I_{Lin_min}^2 \right) D}{3 + (I_{Lin_max} - I_{Lin_min})I_{Lin_min}D + I_{Lin_min}^2 D} \right)^{\frac{1}{2}} \quad (5.10)$$

where I_{Lin_max} and I_{Lin_min} are the maximum and minimum input inductor currents, respectively at each stage and the currents equal to the maximum

and minimum currents of the MOSFET S_{1a} I_{S1a_max} and I_{S1a_min} , respectively.

The maximum and minimum currents I_{S1a_max} and I_{S1a_min} are expressed as follow:

$$I_{S1a_max} = I_{Lin_max} = \frac{I_{in}}{n} + \frac{V_{in}D}{f_{sw}L_{out}} \quad (5.11)$$

$$I_{S1a_min} = I_{Lin_min} = \frac{I_{in}}{n} - \frac{V_{in}D}{f_{sw}L_{out}} \quad (5.12)$$

where I_{in} is the average input current. Thus the summation of conduction losses for S_{1a} , S_{2a} and S_{3a} are expressed as follows:

$$P_{cond_Sma} = i_{Sma(eff)}^2 R_{on} \times n \quad (5.13)$$

5.4.2 Conduction loss for MOSFETs S_{1b} , S_{2b} and S_{3b}

The effective currents of $i_{S1b(eff)}$, $i_{S2b(eff)}$ and $i_{S3b(eff)}$ are same. It equals to the output inductor current I_{Lout} when these switches are on-state. The effective current of these switches is expressed as follow:

$$i_{S1b(eff)} = i_{S2b(eff)} = i_{S3b(eff)} \quad (5.14)$$

$$i_{S1b(eff)} = \left(\frac{(I_{Lout_max} - I_{Lout_min})^2 D}{\frac{3}{2} + \frac{2I_{Lout_min}(I_{Lout_max} - I_{Lout_min})D}{2} + I_{Lout_min}^2 D} \right)^{\frac{1}{2}} \quad (5.15)$$

where I_{Lout_max} and I_{Lout_min} are the maximum and minimum output inductor currents, respectively and the currents are equal to the maximum and minimum currents of the MOSFET S_{1b} I_{S1b_max} and I_{S1b_min} , respectively. The maximum and minimum currents I_{S1b_max} and I_{S1b_min} are expressed as follow

$$I_{S1b_max} = I_{Lout_max} = I_{out} + \frac{nDV_{in}}{2f_{sw}L_{out}} \quad (5.16)$$

$$I_{S1b_min} = I_{Lout_min} = I_{out} - \frac{nDV_{in}}{2f_{sw}L_{out}} \quad (5.17)$$

where I_{out} is the average output current. Thus the summation of conduction losses for S_{1b} , S_{2b} and S_{3b} are expressed as follow:

$$P_{cond_Smb} = i_{Smb(eff)}^2 R_{on} \times n \quad (5.18)$$

5.4.3 Conduction loss for MOSFET S_{1c} , S_{2c} and S_{3c}

Principally, the MOSFETs S_{1c} , S_{2c} and S_{3c} are operated during charging condition of the stage capacitors. Furthermore, the currents $i_{S1c(eff)}$, $i_{S2c(eff)}$ and $i_{S3c(eff)}$ are not same one another due to circuit configuration at the output side as shown in Mode IV of Figure 5.4.

The effective current for $i_{S1c(eff)}$ is expressed as follows:

$$i_{S1c(eff)} = \left(\frac{\left(I_{S1c_max}^2 - 2I_{S1c_max}I_{S1c_min} + I_{S1c_min}^2 \right) (1 - D^3)}{3(D-1)^2} + \left(\frac{\left(I_{S1c_max} - I_{S1c_min} \right) I_{S1c_min}}{D-1} - \frac{\left(I_{S1c_max}^2 - 2I_{S1c_max}I_{S1c_min} + I_{S1c_min}^2 \right)}{(D-1)^2} \right) (1 - D^2) + \left(I_{S1c_min}^2 - \frac{2I_{S1c_min} \left(I_{S1c_max} - I_{S1c_min} \right)}{D-1} + \frac{\left(I_{S1c_max}^2 - 2I_{S1c_max}I_{S1c_min} + I_{S1c_min}^2 \right)}{(D-1)^2} \right) (1 - D) \right)^{1/2} \quad (5.19)$$

where I_{S1c_max} and I_{S1c_min} are the maximum and minimum current of the MOSFET S_{1c} , respectively. The maximum and minimum currents I_{S1c_max} and I_{S1c_min} are expressed as follow:

$$I_{S1c_max} = \frac{2I_{in}}{n} - I_{out} + \frac{V_{in}D}{f_{sw}L_{in}} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad (5.20)$$

$$I_{S1c_min} = \frac{2I_{in}}{n} - I_{out} - \frac{V_{in}D}{f_{sw}L_{in}} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad (5.21)$$

Thus the conduction loss for S_{1c} is expressed as follows:

$$P_{cond_S1c} = i_{S1c(eff)}^2 R_{on} \quad (5.22)$$

Then, the effective current for $i_{S2c(eff)}$ is expressed as follows:

$$I_{S2c(eff)} = \left\{ \begin{array}{l} \left(\frac{(I_{S2c_max}^2 - 2I_{S2c_max}I_{S2c_min} + I_{S2c_min}^2)(1-D^3)}{3(D-1)^2} \right. \\ \left. + \left(\frac{(I_{S2c_max} - I_{S2c_min})I_{S2c_min}}{D-1} \right) \right. \\ \left. - \left(\frac{(I_{S2c_max}^2 - 2I_{S2c_max}I_{S2c_min} + I_{S2c_min}^2)}{(D-1)^2} \right) \right) (1-D^2) \\ + \left(\frac{I_{S2c_min}^2 - \frac{2I_{S2c_min}(I_{S2c_max} - I_{S2c_min})}{D-1}}{D-1} \right. \\ \left. + \left(\frac{(I_{S2c_max}^2 - 2I_{S2c_max}I_{S2c_min} + I_{S2c_min}^2)}{(D-1)^2} \right) \right) (1-D) \end{array} \right\}^{\frac{1}{2}} \quad (5.23)$$

where I_{S2c_max} and I_{S2c_min} are the maximum and minimum currents of the MOSFET S_{2c} , respectively. The maximum and minimum currents I_{S2c_max} and I_{S2c_min} are expressed as follow:

$$I_{S2c_max} = \frac{I_{in}}{n} - I_{out} + \frac{V_{in}D}{2f_{sw}L_{in}} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad (5.24)$$

$$I_{S2c_min} = \frac{I_{in}}{n} - I_{out} - \frac{V_{in}D}{2f_{sw}L_{in}} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad (5.25)$$

Thus the conduction loss for S_{2c} is expressed as follows:

$$P_{cond_S2c} = i_{S2c(eff)}^2 R_{on} \quad (5.26)$$

Meanwhile, the effective current for $i_{S3c(eff)}$ is expressed as follows:

$$i_{S3c(eff)} = \left\{ \begin{array}{l} \left(\frac{(I_{S3c_max}^2 - 2I_{S3c_max}I_{S3c_min} + I_{S3c_min}^2)(1-D^3)}{3(D-1)^2} \right. \\ \left. + \left(\frac{(I_{S3c_max} - I_{S3c_min})I_{S3c_min}}{D-1} \right. \right. \\ \left. \left. - \frac{(I_{S3c_max}^2 - 2I_{S3c_max}I_{S3c_min} + I_{S3c_min}^2)}{(D-1)^2} \right) \right. \\ \left. (1-D^2) \right. \\ \left. + \left(I_{S3c_min}^2 - \frac{2I_{S3c_min}(I_{S3c_max} - I_{S3c_min})}{D-1} \right. \right. \\ \left. \left. + \frac{(I_{S3c_max}^2 - 2I_{S3c_max}I_{S3c_min} + I_{S3c_min}^2)}{(D-1)^2} \right) \right. \\ \left. (1-D) \right) \end{array} \right\}^{\frac{1}{2}} \quad (5.27)$$

where I_{S3c_max} and I_{S3c_min} are the maximum and minimum currents of the MOSFET S_{3c} , respectively. The maximum and minimum currents I_{S3c_max} and I_{S3c_min} are expressed as follow:

$$I_{S3c_max} = I_{Lout} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad (5.28)$$

$$I_{S3c_min} = I_{Lout} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad (5.29)$$

where I_{Lout} is the average output inductor current. Therefore the conduction loss for S_{3c} is expressed as follows:

$$P_{cond_S3c} = i_{S3c(eff)}^2 R_{on} \quad (5.30)$$

5.4.4 Conduction loss for diodes D1, D2 and D3

The average diode currents $i_{D1(ave)}$, $i_{D2(ave)}$ and $i_{D3(ave)}$ are same. The average diode current is expressed as follow:

$$i_{D1(ave)} = i_{D2(ave)} = i_{D3(ave)} \quad (5.31)$$

$$i_{D1(ave)} = \left\{ \begin{array}{l} \frac{(I_{Lin_max} - I_{Lin_min})(1 - D^2)}{2(D-1)} \\ - \frac{(I_{Lin_max} - I_{Lin_min})(1 - D)}{(D-1)} + (1 - D)I_{Lin_min} \end{array} \right\} \quad (5.32)$$

The maximum and minimum diode currents I_{D1_max} and I_{D2_min} are expressed as follow:

$$I_{D1_max} = I_{Lin_max} = \frac{I_{in}}{n} + \frac{V_{in}D}{f_{sw}L_{out}} \quad (5.33)$$

$$I_{D2_min} = I_{Lin_min} = \frac{I_{in}}{n} - \frac{V_{in}D}{f_{sw}L_{out}} \quad (5.34)$$

Therefore the summation of conduction losses for D₁, D₂ and D₃ are expressed as follows:

$$P_{cond_Dm} = i_{Dm(ave)}V_F \times n \quad (5.35)$$

5.4.5 Copper and iron losses

In the constructed three-stage MTBC, the copper loss is contributed by the three input inductors and one output inductor. The copper resistances of each inductor are measured for copper loss estimation. The expression for the copper loss is expressed as follows:

$$P_{copper} = \sum_{m=1}^n (i_{Lm(eff)}^2 R_{copper_m}) + i_{Lout(eff)}^2 R_{copper_out} \quad (5.36)$$

where $i_{Lm(eff)}$ is the effective stage input inductor currents, $i_{Lout(eff)}$ is the effective output inductor current, R_{copper_m} is the inductor winding resistance of the stage input inductor and R_{copper_out} is the inductor winding resistance of the output inductor.

Meanwhile, iron loss is not analyzed by the theoretical equation in this paper. Instead, based on the power loss measurement and theoretical calculation of other power losses, the difference between both power losses is considered as the iron loss.

5.4.6 Switching loss for MOSFETs and diodes

All switching device voltages have same minimum and maximum voltages of the stage capacitor. The minimum and maximum voltages can be expressed as follow:

$$V_{C(m)_{\max}} = \frac{nV_{in} + V_{out}}{n} + \frac{1}{2} \frac{(1-D)P_{out}}{nf_{sw}C_{(m)}V_{in}} \quad (5.37)$$

$$V_{C(m)_{\min}} = \frac{nV_{in} + V_{out}}{n} - \frac{1}{2} \frac{(1-D)P_{out}}{nf_{sw}C_{(m)}V_{in}} \quad (5.38)$$

The generalization of each switching loss for S_{1a} , S_{2a} and S_{3a} is expressed as follows:

$$P_{SW_Sma} = \left(\frac{V_{C(m)_{\min}} I_{Sma_max}}{6} f_{sw} t_r \right)_{on} + \left(\frac{V_{C(m)_{\max}} I_{Sma_min}}{6} f_{sw} t_f \right)_{off} \quad (5.39)$$

On the other hand, the switching losses for S_{mb} and S_{mc} are defined by the same equation of (5.39).

Furthermore from the converter operation modes as shown in Fig. 5.4, in Mode II the switches S_{mc} are conducted through anti-parallel parasitic diodes and then in Mode III the switches S_{mc} are turned on, thus zero voltage switching condition occurs. In an experiment, the voltage across

switches S_{mc} during Mode II and Mode III are considered approximately zero compared to the output voltage. Moreover, the dead-time period during Mode II and the additional time-delay period during Mode III are very short compared to the switching period. Thus, the switching losses on switches S_{mc} during Modes II and III are very small compared to the total power loss. As a result, it can be neglected in the switching loss expression. Therefore, the switching loss equation is generalized and expressed as Eq. (5.39).

5.4.7 Total conduction and switching losses for all switches and diodes

The total conduction and switching losses for all switches and diodes in three-stage MTBC is expressed as follows:

$$\begin{aligned}
 P_{cond+SW_total} &= P_{cond_total} + P_{SW_total} \\
 &= P_{cond_S1a+S2a+S3a} + P_{cond_S1b+S2b+S3b} \\
 &\quad + P_{cond_S1c} + P_{cond_S2c} + P_{cond_S3c} \\
 &\quad + P_{cond_D1+D2+D3} \\
 &\quad + P_{SW_S1a+S2a+S3a} + P_{SW_S1b+S2b+S3b} \\
 &\quad + P_{SW_S1c} + P_{SW_S2c} + P_{SW_S3c}
 \end{aligned} \tag{5.40}$$

5.5 Experimental Results

Table 5.2 shows the specifications of the experimental prototype circuit. The inductance of the input inductor on each stage is designed by using (5.5).

Figure 5.5 shows the experimental results of the input inductor current ripples on stage-1 (I_{L1}), stage-2 (I_{L2}) and stage-3 (I_{L3}), which are 1.9 A, 1.8 A and 1.8 A respectively at the output power of 1 kW. However the designed input inductor current ripple on each stage is 1.5 A and the design principle is according to (5.5). The different between experimental results and designed value is due to the voltage drop on the winding resistance of the inductors. The stage average inductor current is divided by three due to three parallel-connections at the input side. Therefore, if many stages are considered, the input current will be divided by the factor of the stage number and consequently the input current stress, the conduction loss and the copper loss will be reduced.

Figure 5.6 shows the experimental results of the capacitor voltages on each stage V_{C1} , V_{C2} and V_{C3} of the three-stage MTBC. The results show that each stage capacitor voltage is 190 V. On the other hand, it is

experimentally confirmed that the output voltage is 400 V when the input voltage is 48 V. Meanwhile if the number of stage is increased the voltage stress on stage capacitors and the maximum voltage stress on switching devices will be reduced as well. Thus according to the (5.9), the voltage stress on stage capacitor voltages and the maximum voltage stress on switching devices are inversely proportional to the number of stage.

Figure 5.7 shows the efficiency characteristic of the prototype circuit under various input voltages. The nominal input voltage is 48 V with 25% fluctuation and the output voltage is fixed at 400 V. The maximum efficiencies are 94.5% and 95.0% when the input voltages are 48 V (boost ratio β is 8.33) and 60 V (boost ratio β is 6.67), respectively when the output power is 500 W. Meanwhile, when the input voltage is 36 V (boost ratio β is 11.11), the maximum output power is limited up to 500 W due to the limitation of the current rating of the switching devices on the input side. The efficiency becomes higher when the boost ratio is low. Besides, the power loss is dominated by the iron loss when the output power is low. As a result, the efficiency is low.

Figure 5.8 shows the distribution of the power losses based on theoretical calculation. The power losses are distributed into nine parts, i.e., diode conduction loss, MOSFET conduction loss at input and output sides, MOSFET switching loss at input and output sides, inductor copper loss, ESR loss, no load loss (discharging power losses for drain-source parasitic capacitances of MOSFETs) and others. The total power loss of 100% is based on the measured total power loss by experiment when the output power is 1 kW. From the loss analysis, it shows that the converter loss is dominated by the ‘Others’ loss whereby it includes the iron loss, wiring loss and so on. It is estimated that the iron loss is dominant in the ‘Others’ loss.

The iron loss is considered not constant with regard to the output power variation due to the increasing of the input current ripples ΔI_{L1} , ΔI_{L2} and ΔI_{L3} . Furthermore, the inductor current ripple is increased due to the increasing of voltage drop on the winding resistance of the inductors when output power is increasing. As a result, the iron loss is considered varies with regard to the variation of the output power.

Based on circuit configuration, the proposed three-stage MTBC has input and output inductors. Thus, the iron loss is considered dominant especially at the output inductor side due to the high voltage stress at the output. The second major losses are the MOSFET conduction loss and copper loss. From the experimental results, the input current ripple is increased when the output power is increased and this condition leads the iron loss increasing according the increasing the output power. Besides, according to [135], the iron loss is influenced by the voltage stress on the inductor and the applied switching frequency. Thus principally, the iron loss is reduced when the voltage stress and the applied switching frequency are reduced. These options will be further analyzed in a future research work for iron loss reduction.

Table 5.2 Experiment specification.

Specification	Value
Input voltage V_{in}	48 V
Output voltage V_{out}	400 V
Output power P_{out}	1000 W
Switching frequency f_{sw}	50 kHz
Input inductor $L_1 = L_2 = L_3$	500 μ H
Output inductor L_{out}	800 μ H
Stage capacitor $C_1 = C_2 = C_3$	44 μ F
Output capacitor C_{out}	50 μ F
Power MOSFET (SiHG25N40D)	400 V/25 A
SiC Schottky Barrier Diode (SCS220KGC)	1200 V/20 A

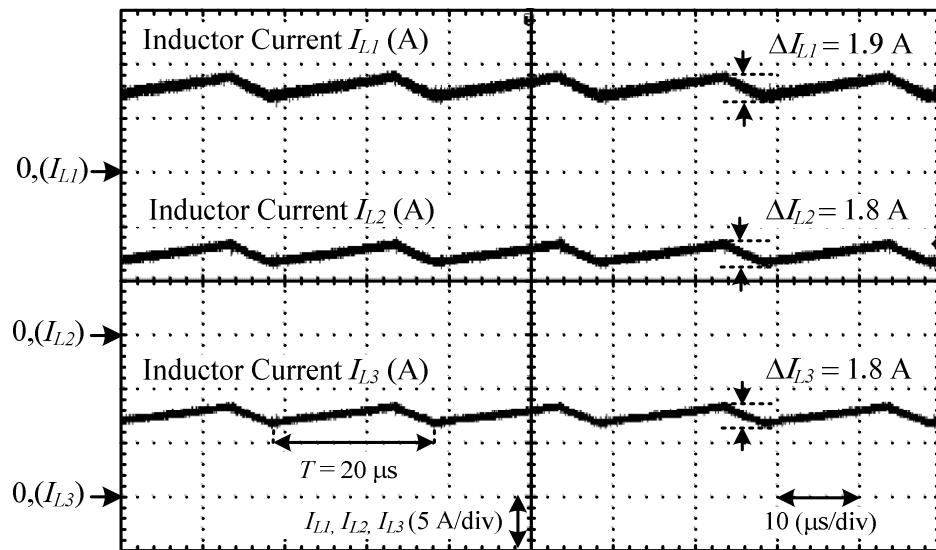


Figure 5.5 Experimental waveforms of the stage-1, stage-2 and stage-3 inductor currents.

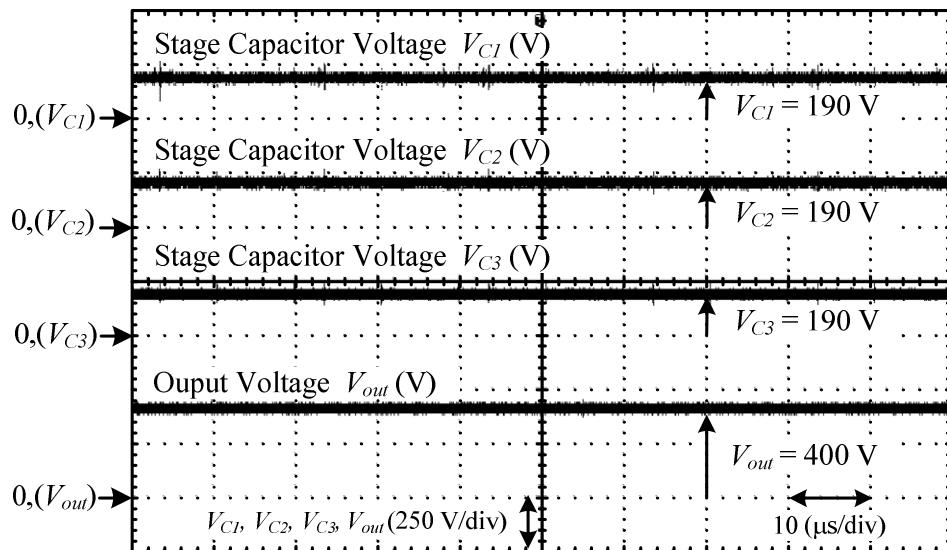


Figure 5.6 Experimental waveforms of the stage-1, stage-2 and stage-3 capacitor voltages, and the output voltage.

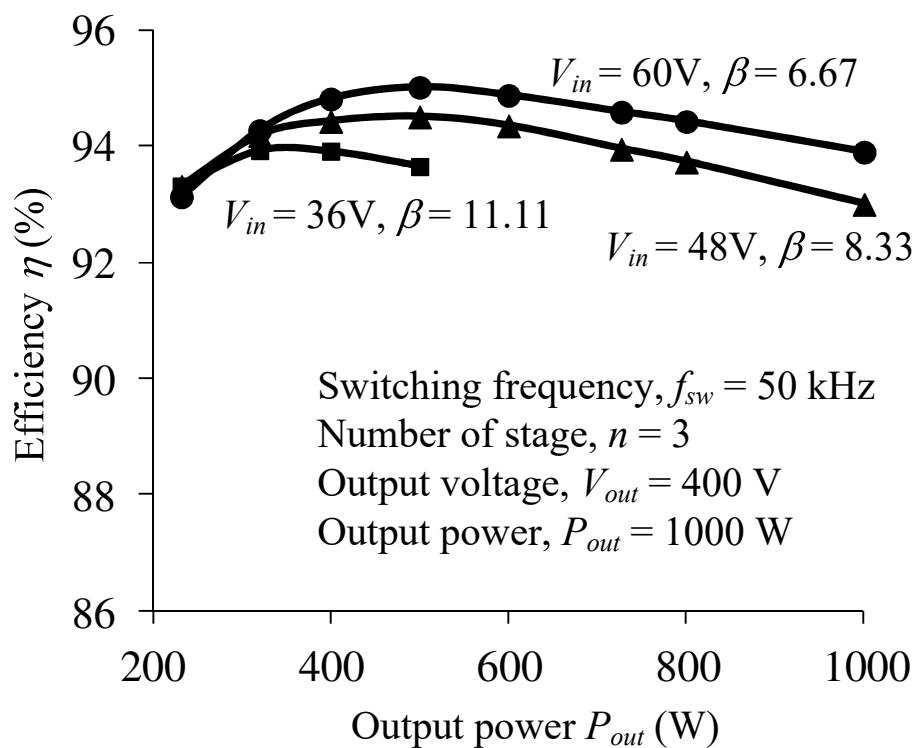


Figure 5.7 Efficiency of the three-stage MTBC.

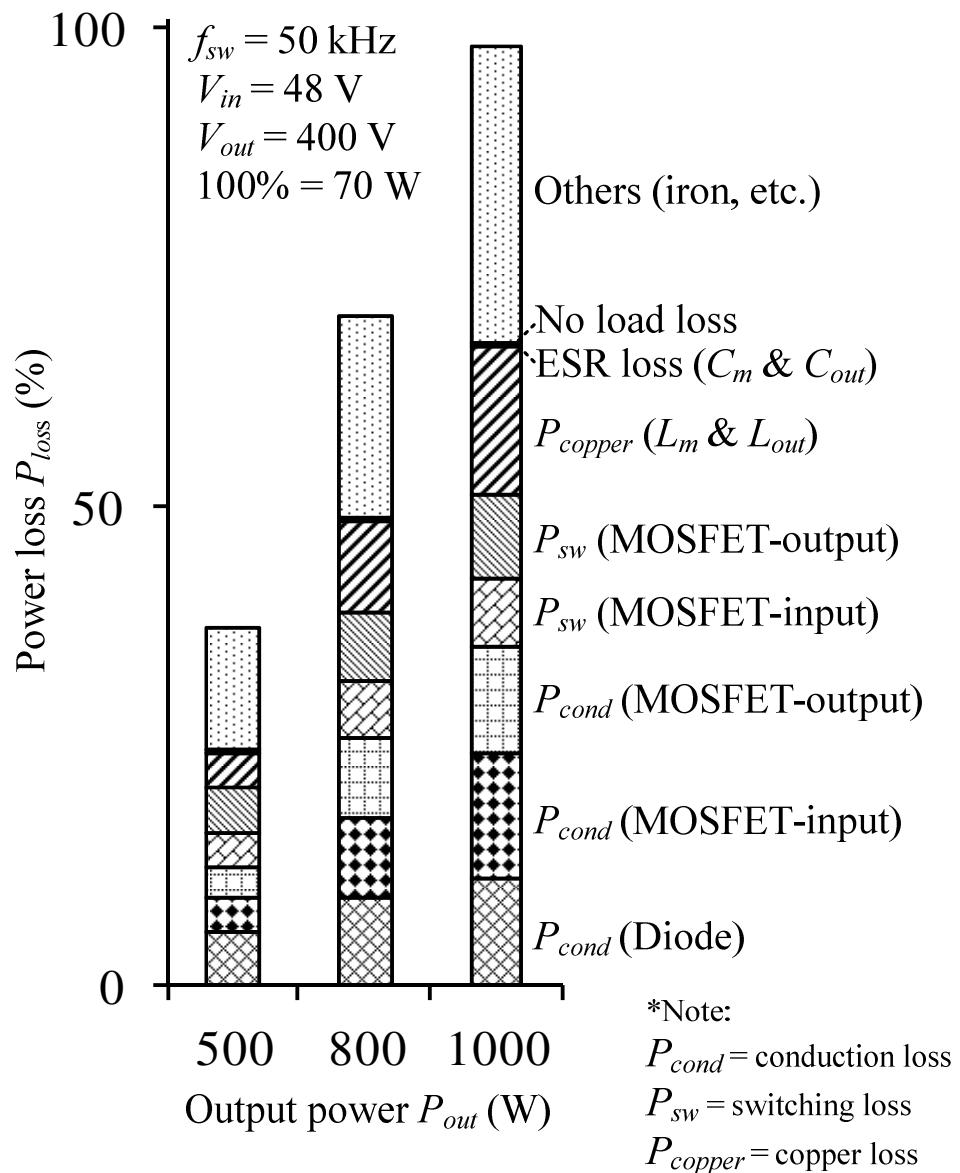


Figure 5.8 Loss distribution of the three-stage MTBC.

5.6 Interleaved operation in the three-stage MTBC

In this section an interleaved Marx topology DC-DC converter with high boost ratio for the inductance and volume reductions of the output inductor is reduced. The interleaved switching scheme is defined as the stage-III operates alternately with stage-I and stage-II, meanwhile the synchronized switching scheme (as discussed in Section 5.2) is defined as all stages are operated synchronously. Thus, by introducing the interleaved switching scheme in the three-stage MTBC, the current stress at the bottom switching device of the stage-I is reduced half compared to that of the synchronized switching scheme as shown on Figure 5.9. Furthermore the equivalent frequency at the output side becomes twice. As a result, the inductance and core volume of the output inductor are reduced.

5.6.1 Converter Principles with the Synchronized and Interleaved Switching Schemes

In order to analyze the MTBC characteristic, the three-stage MTBC with the synchronized switching scheme and the interleaved switching

scheme are analyzed. In principle, the relationship between the input voltage V_{in} and the output voltage V_{out} is expressed by Eq. (5.1).

Meanwhile the boost ratios β in terms of duty ratio D for the synchronized and interleaved switching schemes are expressed as follow, respectively:

$$\beta_{synchronized} = \frac{D_{synchronized}}{1 - D_{synchronized}} n \quad (5.41)$$

$$\beta_{interleaved} = \frac{2D_{interleaved} - 1}{1 - D_{interleaved}} n \quad (5.42)$$

where $D_{synchronized}$ and $D_{interleaved}$ are the duty ratio for the switches S_{1a} , S_{1b} , S_{2a} , S_{2b} , S_{3a} and S_{3b} , respectively. Thus the output voltage V_{out} in terms of the duty ratio D , the number of stage n and the input voltage V_{in} can be rewrite as follows:

$$V_{out(synchronized)} = \left(\frac{D_{synchronized}}{1 - D_{synchronized}} \right) n V_{in} \quad (5.43)$$

$$V_{out(interleaved)} = \left(\frac{2D_{interleaved} - 1}{1 - D_{interleaved}} \right) n V_{in} \quad (5.44)$$

The inductor current of each stage of the three-stage MTBC in the synchronized and interleaved switching schemes is designed to be operated in continuous current mode (CCM) in order to minimize the peak input current. Thus the minimum inductor current of each stage is based on Eq. (5.4). Meanwhile the inductor current ripple on each stage and the capacitance of the stage capacitor $\Delta I_{Lin(m)}$ are based on Eqs. (5.5) and (5.7).

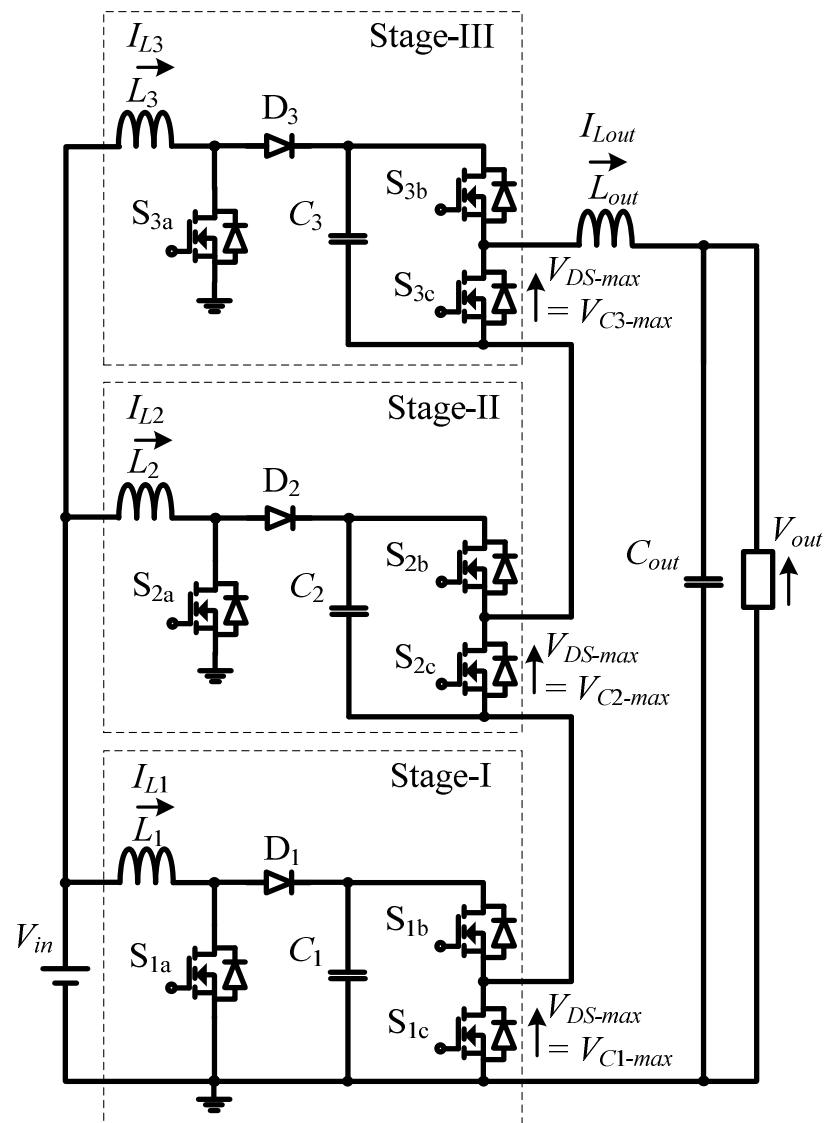


Figure 5.9 Three-stage MTBC circuit configuration.

5.6.2 Operation modes and switching schemes

The discussion of this section is based on the three-stage MTBC. The groups of switches have been divided into two, whereby S_{1a} , S_{2a} and S_{3a} are considered in the input side switches group; meanwhile S_{1b} , S_{1c} , S_{2b} , S_{2c} , S_{3b} , S_{3c} switches are considered in the output side switches group.

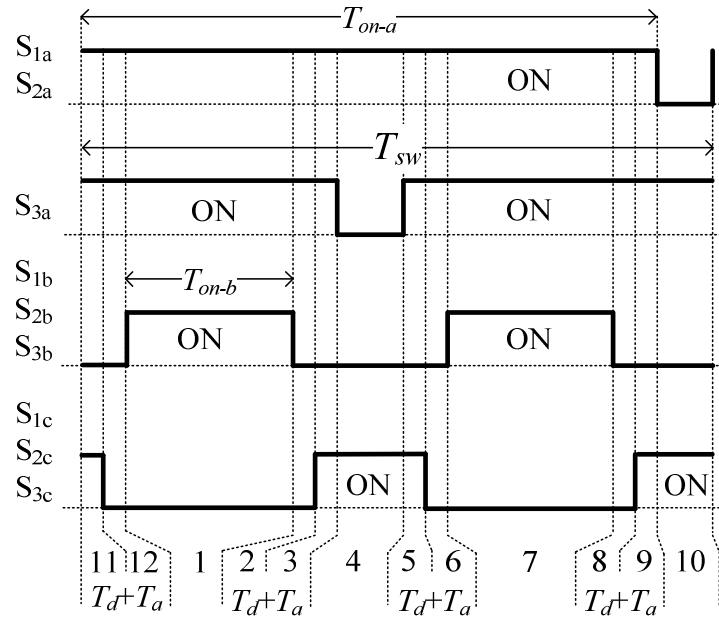
Figure 5.10 shows the switching schemes of the synchronized and the interleaved. Both switching schemes are considered the dead-time T_d and the additional time-delayed T_a in order to prevent from a short circuit and a surge voltage. In the interleaved switching scheme, the output side switches group has a twice of the equivalent frequency of the input side switches group.

Figure 5.11 shows the operation modes of the synchronized switching scheme and the interleaved switching scheme. The synchronized switching scheme has four operation modes; meanwhile the interleaved switching scheme has 12 operation modes. In the synchronized switching scheme, the stages capacitors C_1 , C_2 and C_3 are charging in parallel at the same time and then those stage capacitors are discharging in series at the same time. Thus

from these conditions, the output voltage can be boost-up by advantage of a series connection of the stage capacitors.

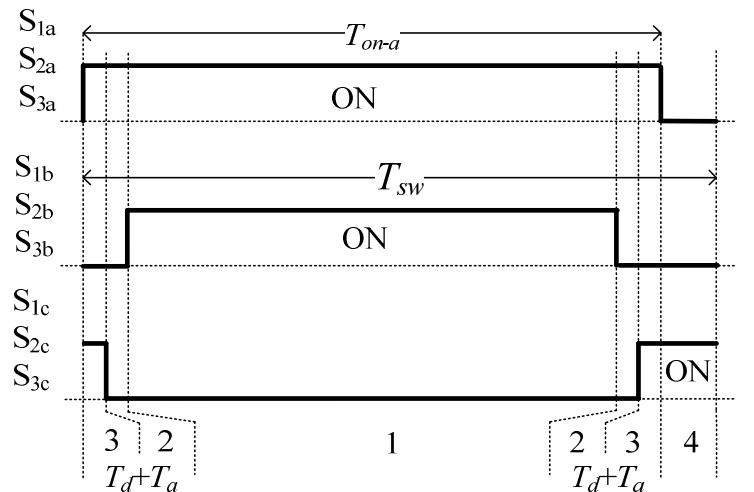
On the other hand, in the interleaved switching scheme, the stage capacitors C_1 and C_2 are charging in parallel together at the same time; meanwhile C_3 is charging in opposite. During discharging condition, the stage capacitors C_1 , C_2 and C_3 are discharging in series at the same time. Thus in one cycle with interleaved switching scheme, the stage capacitors are charged and discharged twice. Consequently, the equivalent frequency of the output inductor current ripple at the output side is a twice of the switching frequency. A high boost ratio is achieved in the synchronized and interleaved switching schemes.

In the synchronized switching scheme and interleaved switching scheme, the maximum voltage stresses on the switching devices S_{1a} , S_{1b} , S_{1c} , S_{2a} , S_{2b} , S_{2c} , S_{3a} , S_{3b} , S_{3c} are determined by each of the maximum stage capacitor voltages V_{C1} , V_{C2} and V_{C3} . Meanwhile the voltage stresses on the D_1 , D_2 and D_3 are equal to the V_{C1} , $2V_{C2}$, and $3V_{C3}$, respectively. Thus the top diode voltage stress V_{D3} is equal to total stage capacitor voltages stress.



$$T_d = \text{dead-time} \quad T_a = \text{additional time-delayed} \quad {}^*D_1 = \frac{T_{on-a}}{T_{sw}} \quad {}^*D_2 = \frac{2T_{on-b}}{T_{sw}}$$

(a) Interleaved switching scheme.



$$T_d = \text{dead-time} \quad T_a = \text{additional time-delayed} \quad {}^*D = \frac{T_{on-a}}{T_{sw}}$$

(b) Synchronized switching scheme.

Figure 5.10 Switching schemes.

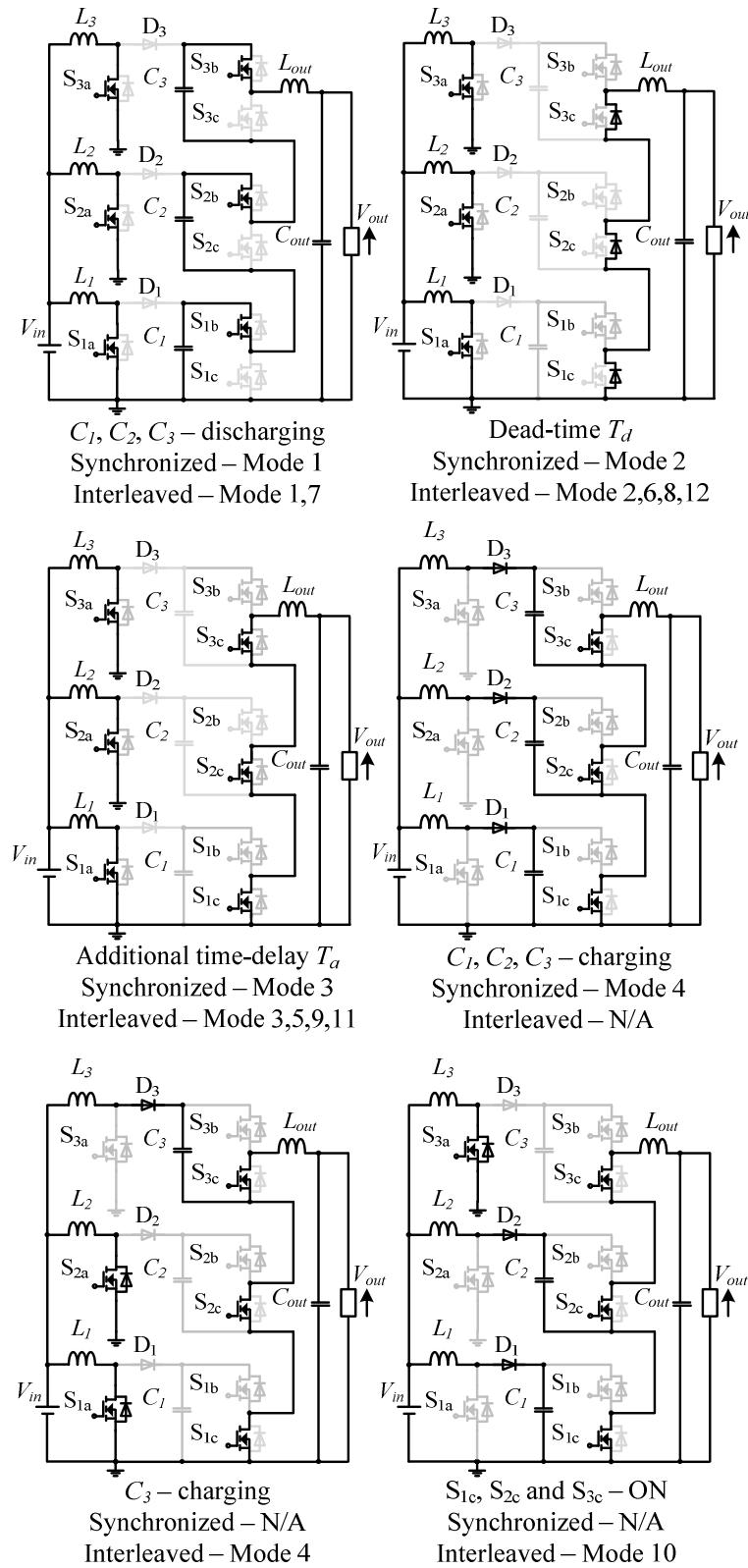


Figure 5.11 Three-stage MTBC operation modes of synchronized and interleaved switching schemes.

5.6.3 Comparison Between Synchronized And Interleaved Switching Schemes

In this section the experimental results comparison in terms of the input inductor current, the output inductor current, the current between stage-III and stage-II ($I_{S3C-S2C}$), and the current between stage-II and stage-I ($I_{S2C-S1C}$) between the synchronized and interleaved switching schemes is discussed. These experimental results are based on the output power of 1 kW. Table 5.1 shows the experiment specifications.

Figure 5.12 shows the experimental results of the current $I_{S3C-S2C}$, the current $I_{S2C-S1C}$, the stage-III inductor current I_{L3} and the output inductor current I_{Lout} of the synchronized and interleaved switching schemes.

Figure 5.12(a) shows the current $I_{S2C-S1C}$ has higher amplitude compared to the current $I_{S3C-S2C}$ when the synchronized switching scheme is applied with $L_{out} = 800 \mu\text{H}$. Furthermore, the frequency of the inductor current ripple at the input side and the output side is same.

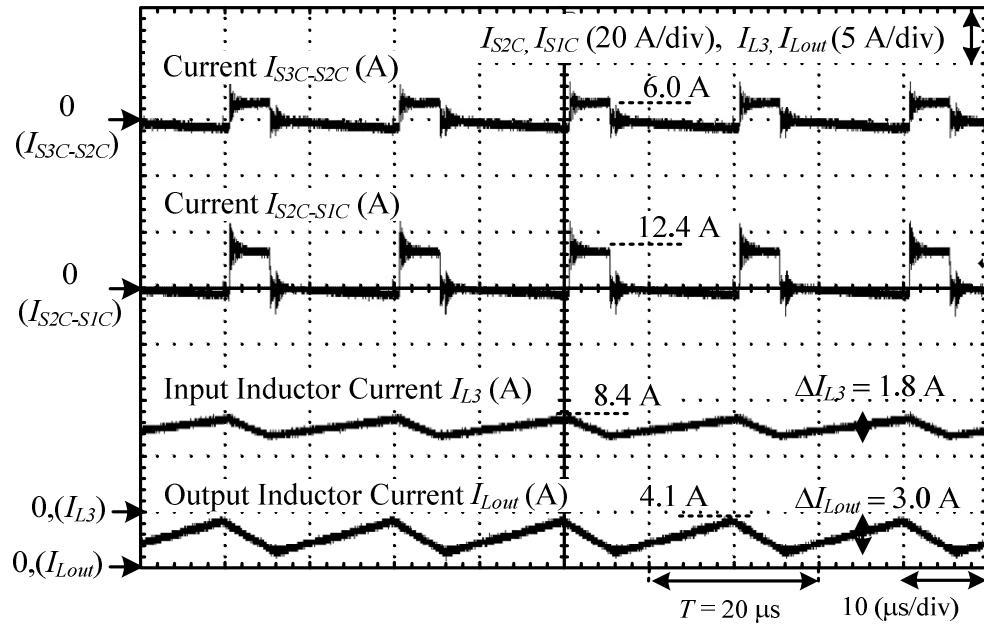
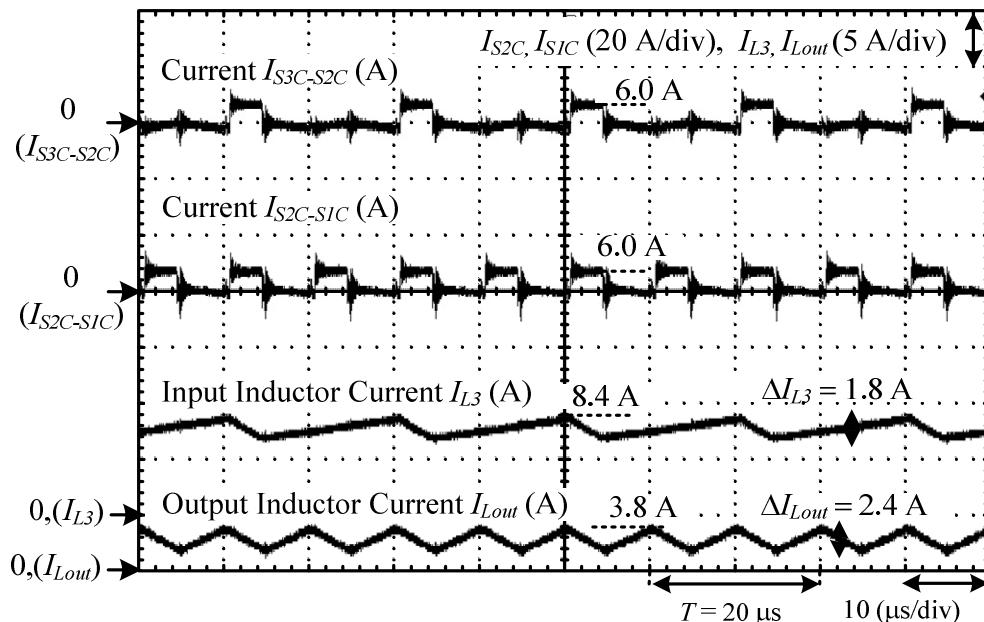
Figure 5.12(b) shows that the current $I_{S2C-S1C}$ has same amplitude value compared to the current $I_{S3C-S2C}$ when the interleaved switching scheme is applied with $L_{out} = 800 \mu\text{H}$ which is same to that of the synchronized

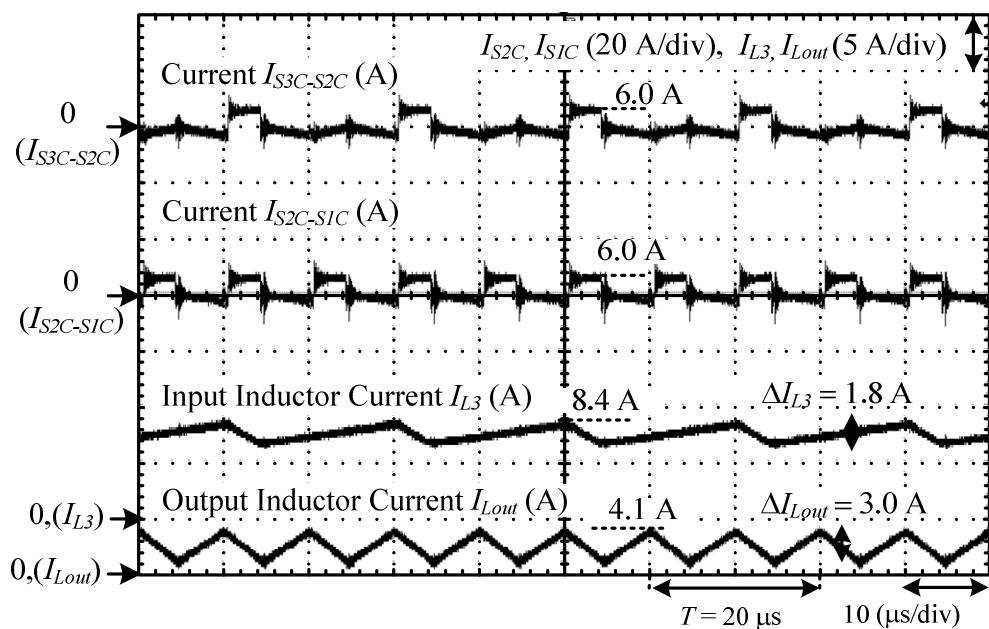
switching scheme. Thus, by applying the interleaved switching scheme, the current $I_{S2C-S1C}$ is reduced half. Therefore, by applying interleaved switching scheme, the maximum current stress of the switching device S_{1C} which is the bottom switch in the stage-I is reduced due to the reduction of the current $I_{S2C-S1C}$. Besides the equivalent frequency at the output side becomes twice of the switching frequency in the interleaved operation. As a result, the inductance of the output inductor is reduced compared to that of the synchronized switching scheme. Therefore, the core volume of the output inductor is reduced due to the equivalent frequency at the output side which has twice of the switching frequency.

Figure 5.12(c) shows the experimental results of the currents $I_{S3C-S2C}$, $I_{S2C-S1C}$, the stage-III input inductor current I_{L3} , and the output inductor current I_{Lout} when the interleaved switching scheme is applied with $L_{out} = 640 \mu\text{H}$ which is designed for same output inductor current ripple of the synchronized switching scheme. It is confirmed that the output inductor current ripple ΔI_{Lout} is 3.0 A which is agreed with that of the synchronized switching scheme as shown in Figure 12(a). Therefore, it is experimentally confirmed that the inductance of the output inductor is reduced on the

three-stage MTBC when the interleaved switching scheme is applied. In addition, the effective value of the current $I_{S2C-S1C}$ is same between the synchronized switching scheme and the interleaved switching scheme. Only the maximum current stress is different. Hence, the overall conduction and switching losses between the two switching schemes are same. Consequently, the heatsink volume is also same at the two switching schemes. On the other hand, the capacitors volumes are considered same.

In a high power application such as 10 kW, the interleaved operation has an advantage of the current stress reduction of the switching devices S_{1C} . Thus lower current stress switching devices can be selected.

(a) With synchronized switching scheme when $L_{out} = 800 \mu\text{H}$.(b) With interleaved switching scheme when $L_{out} = 800 \mu\text{H}$.Figure 5.12 Experimental waveforms of the current $I_{S3C-S2C}$, the current $I_{S2C-SIC}$, the stage-3 inductor current and the output inductor current.



(c) With interleaved switching scheme when $L_{out} = 640 \mu\text{H}$.

Figure 5.12 Experimental waveforms of the current $I_{S3C-S2C}$, the current $I_{S2C-S1C}$, the stage-3 inductor current and the output inductor current.

5.6.4 The Inductance and core volume reduction with interleaved switching scheme

In this section, the inductance and core volume of the output inductor are analyzed and compared between the synchronized switching scheme and the interleaved switching scheme. It is experimentally confirmed that the equivalent frequency at the output side becomes twice of the switching frequency when the interleaved switching scheme is applied. In this prototype, the switching frequency f_{sw} is 50 kHz. Therefore, the equivalent frequency at the output side becomes 100 kHz in the interleaved switching scheme. Figures 5.12(a) and 5.12(b) show the output inductor current ripples during the synchronized and interleaved switching schemes, 3.0 A and 2.4 A, respectively. The ratio between both output inductor current ripples is 0.8 (80%), thus the inductance of the output inductor is reduced in interleaved switching scheme by 20%. Consequently the volume of the output inductor is also reduced.

Figure 5.13 shows the comparison of the inductance and core volume of the output inductor. The relationship between the inductance of the output inductors $L_{out(interleaved)}$ and $L_{out(synchronized)}$ is expressed as follows:

$$L_{out(interleaved)} = 80\% \times L_{out(synchronized)} \quad (5.45)$$

Meanwhile based on the Area Product principle, the core volume of the output inductors between synchronized and interlead $Vol(L_{out(interleaved)})$ and $Vol(L_{out(synchronized)})$ is expressed as follows:

$$Vol(L_{out(interleaved)}) = 84\% \times Vol(L_{out(synchronized)}) \quad (5.46)$$

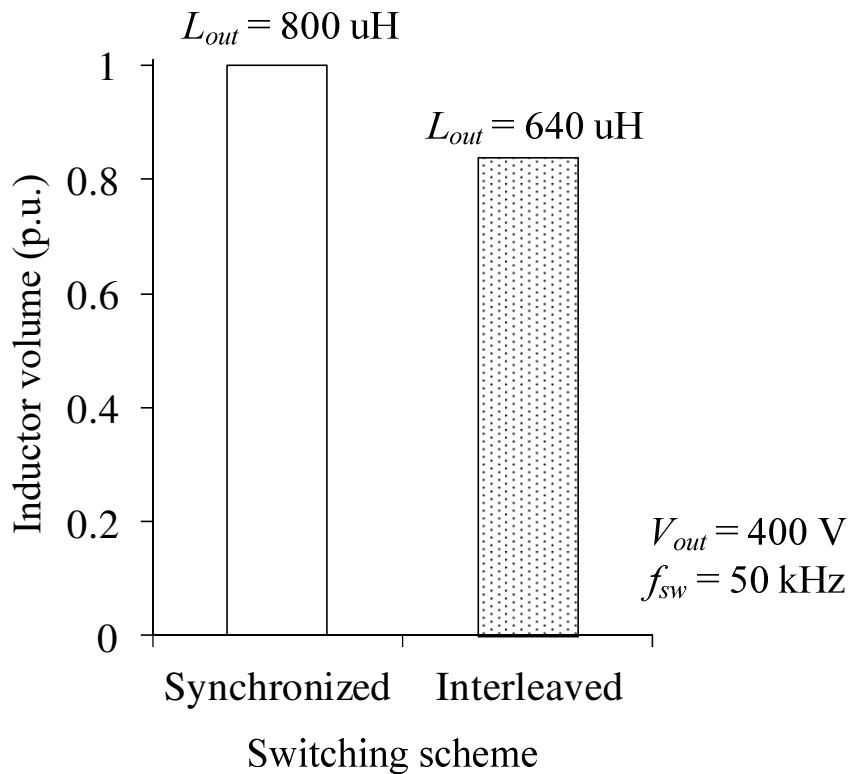


Figure 5.13 Output inductor volume estimation with the synchronized and interleaved switching schemes.

5.7 Power Density Comparison

Power density for the three-stage MTBC is compared with other topologies in order to emphasize the advantage of this converter topology. In this comparison, the two-level CBC, the three-level FCBC, the-level FCBC and the three-stage MTBC have compared theoretically. The specifications for all converters are as follow: the input voltage is 48 V, the output voltage is 400 V, the boost ratio is 8.33, the switching frequency ranges are from 25 kHz to 500 kHz, the output power is 1 kW. For the volume estimation, only heatsinks, input inductors, output inductors, flying capacitors and output capacitors components are considered. Meanwhile, the efficiency for all converters is based on semiconductor devices losses. Furthermore, copper and iron losses of the inductors are not considered. ESR losses of flying capacitor and output capacitor are very small to be considered. Moreover, the principles of heatsinks, inductors, and capacitors volumes estimation are explained in details in Section 3.6.

Figure 5.14 shows the three-stage MTBC has the highest efficiency when a power density is at maximum (5.16 kW/dm^3), while the three-level FCBC has the highest power density (5.48 kW/dm^3). The boost ratio of

8.33 is considered for all converters. On the other hand, the two-level CBC has the lowest power density (3.71 kW/dm^3) compared to the others. From this power density comparison, the three-stage MTBC and the three-level FCBC show advantages on efficiency and power density, respectively. Therefore, the reductions of passive components in the designed converters are achieved compared to the conventional two-level DC-DC boost converter.

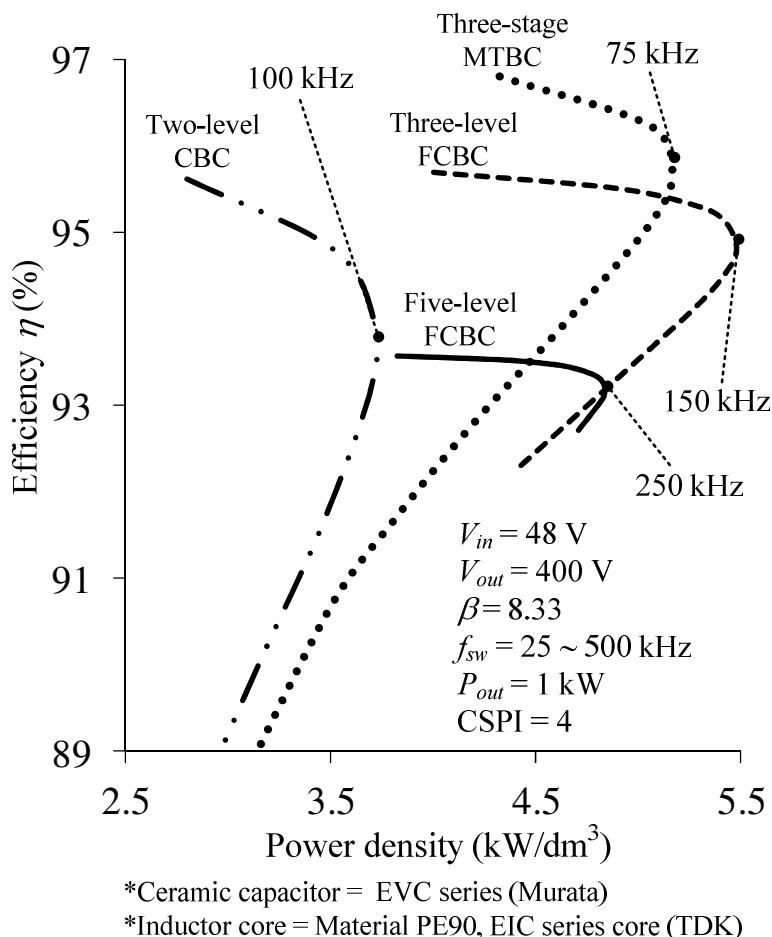


Figure 5.14 Power density characteristics of the two-level CBC, the three-level FCBC, the five-level FCBC, and the three-stage MTBC using Pareto-front curve method.

5.8 Conclusion

A high boost ratio multistage Marx topology DC-DC boost converter (MTBC) is proposed with the parallel-connection of several capacitors at the input side and then the series connection of the same stage capacitors at the output side are applied. In this chapter, the authors have discussed (i) the fundamental circuit operation confirmation of the three-stage MTBC, (ii) the design principle of the input inductors and stage capacitors, and (iii) the mathematical expression for loss calculation and analysis (iv) the interleaved operation on the three-stage MTCB.

The principals of designing the inductance of the input inductor and the capacitance of the stage capacitors according to the number of stage were explained. As a result, the inductance of the input inductor and stage capacitor voltages stress on each stage is reduced by the increasing the number of stage. The input inductor current ripple on each stage is designed and it confirmed by the experimental results. Moreover, mathematical expressions of the conduction and switching losses are derived and were confirmed by the simulation results. The maximum efficiency of the prototype converter was 94.5% at the output power of 500

W. From the loss analysis, it is confirmed that the efficiency is increased by optimizing inductor design.

Then, the prototype circuits with the interleaved and synchronized switching schemes were experimentally confirmed by the three-stage MTBC. As a result, the maximum current stress at the bottom switch of the first stage at the output side was reduced half by the interleaved switching scheme. Furthermore, in the interleaved switching scheme, the equivalent frequency at the output side becomes twice of the switching frequency. As a result, it is experimentally confirmed that the inductance and core volume of the output inductor are reduced. In addition power density comparison between three-stage MTBC and other topologies are conducted theoretically.

Chapter 6

Conclusion

6.1 Discussion

The importance of renewable energy (RE) sources in supplying electricity energy cannot be denied nowadays due to the climate change and global warming concerns, especially solar PV system and wind turbine system. Generally, power converters play an important role as an interface for energy conversion between RE sources and electrical loads. Moreover, DC-DC power converters are become widely used especially in micro-grid system, data center system and electric vehicle system due to the good performance and more reliable.

The motivation of this study is to develop DC-DC power converters based on hybrid-based configuration in order to achieve weight and size reductions with high efficiency and good performance for the applications

of micro-grid system. Based on literature review of DC-DC boost converters, the converters can be categorized based on three main perspectives, i.e., magnetic-based, capacitor-based and hybrid-based configurations. Hybrid-based configuration is defined as a combination of inductor and capacitor components in a DC-DC converter. Meanwhile, the magnetic-based configuration usually refers to the conventional two-level DC-DC converter. This matter is discussed in Chapter 2. In addition, Chapter 2 also discusses the important feature of the hybrid-based configuration in DC-DC boost converters. Then the good features of the multilevel and multistage structures when it coupled with the hybrid-based configuration of DC-DC converters. Specifically, with these combinations the passive components, current stress and voltage stress reductions are achieved. Consequently, high efficiency and high power of DC-DC boost converters can be realized with the advantages of weight, size and volume reductions.

The first proposed converter, which is described in Chapter 3, has multilevel structure and based on flying capacitor DC-DC boost converter (FCBC) configuration. Specifically, the three-level FCBC has developed

with the reduced of input inductor and used the small capacitance of the flying capacitor. As a result, the inductance and inductor core volume of the input inductor were reduced by approximately 25% and 35%, respectively by considering the optimum point product of $V_L \times T_L$ parameter, whereby V_L is the inductor voltage and T_L is the charging time of the inductor. In addition the relationship between the capacitance of the flying capacitor and the output voltage ripple is experimentally confirmed to be independent of each other. Thus based on this relationship, the capacitance of the flying capacitor can be designed regardless of output voltage ripple. Therefore the findings show that high efficiency of the three-level FCBC is achieved with reduced of weight, size and volume. In addition power density comparison between two-level CBC and three-level FCBC are conducted theoretically.

Chapter 4 analyzed the effectiveness of the small capacitance of the multilevel FCBC. Specifically, the three-level and five-level FCBCs have constructed and developed with the small capacitance of the flying capacitors. In addition, based on the relationship between the capacitance of the flying capacitor and the output voltage ripple is independent of each

other principle as described in Chapter 3, the minimum capacitance based on the maximum voltage rating of switching devices was confirmed by the experimental results in the three-level and five-level FCBCs. Besides the expressions clarification in order to design minimum capacitance of the flying capacitor in the n -level FCBC is also illustrated. Moreover, the distortion of the voltage across the input voltage source and the input inductor and the distortion of the current to the output side which is the output capacitor and the load are analyzed experimentally. As a result, the small capacitance of the flying capacitors can be used in the three-level, five-level and n -level FCBCs. Therefore the effectiveness the small capacitance of the flying capacitor in the multilevel FCBC is experimentally confirmed.

The second proposed converter is based on Marx pulse generator topology for high boost ratio achievement with multistage structure which is described in Chapter 5. Specifically, the three-stage Marx topology DC-DC boost converter (MTBC) has developed in order to confirm the converter operation experimentally. The circuit structure is based on parallel connection of the stage capacitors at the low voltage side and then

series connection is applied with the same stage capacitors at the high voltage side. Hence, with this structure a high boost ratio can be achieved. Fundamentally the proposed converter consists of a two-level DC-DC boost converter with additional two switching devices for each stage. In addition the benefits of this proposed converter are current stress at the low voltage side and voltage stress on switching devices at the high voltage side are reduced, respectively due to series and parallel connections structures. Furthermore an interleaved operation is introduced in the proposed converter for the maximum bottom switching current reduction and the output inductor component reduction. The interleaved operation with those benefits is experimentally confirmed. Besides, in order to expanding the converter application, a bi-directional operation is also introduced and it is confirmed by the simulation results. Therefore the second proposed converter has achieved the high boost ratio feature capability with interleaved operations experimentally. In addition power density comparison between three-stage MTBC and other topologies are conducted theoretically.

6.2 Future Works

This thesis has demonstrated that the proposed converters are achieved the passive components reduction in multilevel and multistage structures. However, the proposed converters are still having several drawbacks for practical product implementation due to the following uncertain issues.

6.2.1 Inductor core loss reduction

The volume and power density features are not seriously taken into a consideration for both converters. Both converters used inductors and capacitors as energy storages. Inductor is considered as one of a major contributor to the size and weight although it gives advantages on the converters. The used inductor core material for the proposed converter is from ferrite material whereby this material has low saturation flux density. Higher flux density of an inductor core is needed with small size feature when a high current application is considered in order to reduce the core loss.

The second proposed converter is a high boost ratio type whereby at the low voltage side the DC current is high and one of major losses is

contributed by the core loss. Thus, an inductor core with high flux density, low hysteresis loss and low eddy-current loss features is needed for core loss reduction. In the future this core might be considered in order to reduce core loss especially for a high boost ratio DC-DC converter. On the other hand, at the high voltage side, the inductor voltage ripple V_{Lout} is very high, thus it is also contributes to the core loss. Due to low current at the high voltage side, an inductor with air core is suitable although the copper loss will be slightly increased. These solutions are suggested to the second proposed converter, three-stage multi-stage Marx topology boost converter (MTBC).

6.2.2 Circuit structure improvement

In the second proposed three-stage MTBC circuit structure, every stage has a conventional two-level boost converter and additional two switches. Due to limitation of the passive component reduction in a two-level boost converter, a new structure of the three-stage MTBC can be improved by introducing a three-level FCBC with additional switches. Although the switching devices are increased, the passive components will be reduced

and these passive components will give a significant impact on converter weight and size. Especially on the inductance and core volume of the input inductor and the small capacitance of the flying capacitor can be used.

6.2.3 Zero voltage switching (ZVS)

In the first proposed converter, i.e, the three-stage FCBC, the zero voltage switching (ZVS) feature can be introduced in the hard switching environment. This method can be implemented by introducing the correct dead-time T_d in the switching scheme. Ideally, the dead-time should be determined by considering two parameters, the inductance of the input inductor and the parasitic capacitance of switching devices. By controlling the charging energy of the parasitic capacitance of switching devices the ZVS can be achieved during turn-off period of switching devices. As a result switching loss can be reduced. However this method will affect the inductor current ripple design. A details clarification is required in order to realize this principle idea.

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