Design of an Nth Order Dickson Voltage Multiplier

Giuseppe Di Cataldo and Gaetano Palumbo

Abstract—**In this brief we propose a simple dynamic model of a Dickson voltage multiplier with N stages, which is obtained starting from the models previously proposed for less than 5 stages. The model allows increased insight into the dynamic behavior of these circuits and provides a valuable tool for determining a first version design.**

I. Introduction

A requirement of Power IC's [1]–[6] and EEPROM's [7]–[10] is a voltage higher than the power supply. Moreover, due to the reduction of the power supply to values lower than 5 V, a voltage higher than the power supply may also be necessary in signal processing IC's (in continuous time filters, for example, it optimizes the dynamic range [11]).

Most high-voltage multiplier circuits for IC circuits are based on the circuit proposed by Schenkel in 1917 [12], which was first realized in the form of an integrated circuit by Luscher in 1972 [13] and then by Dickson [14]. These circuits make use of capacitors which are interconnected by diodes and coupled in parallel with two noninterleaving clock signals, and thanks to their topology, unlike other voltage multipliers such as the one proposed by Cockcroft-Walton [15], they are quite insensitive to parasitic capacitances.

Dickson published the first static analysis of the circuit [14], which was then improved in [16]. However, there is no general dynamic model of the Dickson voltage multiplier, so the speed response cannot be simply used as a design constraint unless many circuit simulations are performed. We have already proposed dynamic models for a voltage multiplier having up to 4 stages [17]–[19], but due to the lowering of the power supply, voltage multipliers with more than four stages are used.

In this brief, we present a dynamic model for an N-stage Dickson voltage multiplier. The model is obtained starting from previously proposed models, and has a simple form which allows it to be used for a pencil and paper design.

To reach a more realistic circuit model we have added both parasitic capacitances between the top plate of the capacitor and the ground [17], and a constant current generator at the output node which takes into account a maximum current load [18].

II. N-Stage Voltage Multiplier

A. Fundamental Parameter

We start by assuming the operation of the Dickson voltage multiplier to be well known, since a qualitative description of the N-stage Dickson voltage multiplier is given in [14], and the intuitive dynamic behavior for the 2-stage multiplier can be found in [17]. Let us consider the N-stage voltage multiplier shown in Fig. 1, in which V_{ck} is the clock signal of Fig. 1(b), with a period of T. In real applications the clock signal, which has nonoverlapping phases, is sometimes in the range of $[V_{cc}, V_{cc} - V^*]$, where V^* is slightly smaller than V_{cc}, and represents the amplitude of the clock signal. Moreover, since in real circuits the reverse recovery time and forward recovery time of the diodes are much lower than the clock period, we will assume ideal diodes with a threshold voltage other than zero ($V_\gamma \neq 0$).

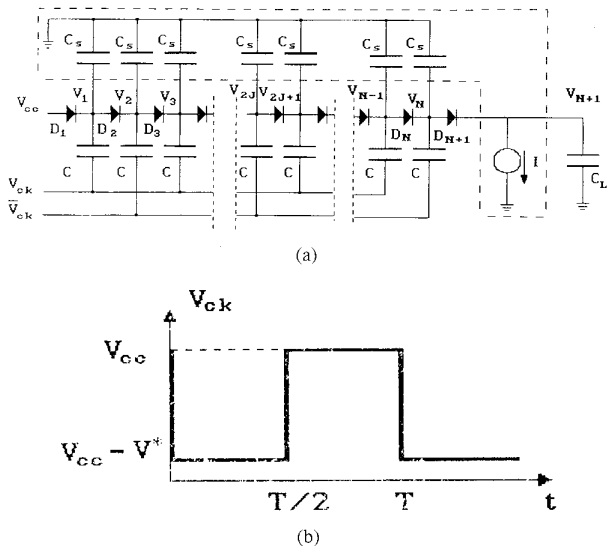

Fig. 1. (a) N-stage voltage multiplier (the circuit outside the dashed box represents an ideal N-stage voltage multiplier and (b) clock signal.

A fundamental parameter of the charge pump is the ratio K between the load capacitor C_L and the stage capacitor C with its parasitic capacitance C_s [Fig. 1(a)]

$$K = \frac{C_L}{C + C_s} \tag{1}$$

K is independent of the number of stages, and does not influence the steady state of the voltage multiplier, but only characterizes its dynamic behavior. Since $C_s \ll C$, the value of K gives an idea of the ratio between the silicon area of the load capacitor and that of each voltage multiplier stage.

Two parameters which represent the degree of ideality of the voltage multiplier are ε' and ε''. The first is the ratio between the parasitic capacitance and the whole capacitance of a stage

$$\varepsilon' = \frac{C_s}{C + C_s}. \tag{2}$$

The second is a function of the maximum output current I[1] which is supplied by the voltage multiplier [Fig. 1(a)] [18]

$$\varepsilon'' = \frac{T}{C + C_s}\frac{I}{V^*}. \tag{3}$$

Both ε' and ε'' are independent of the number of stages.

As shown in [17], the capacitance C_s and the current I lead to a reduction in the clock amplitude that can be estimated as

$$V' = (1 - \varepsilon' - \varepsilon'')V^*. \tag{4}$$

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[1] Since an increase in the load current determines a reduction on the effective clock amplitude [given below by (4)], and an increase of the output ripple [given below by (5)], we consider the more pessimistic case assuming a constant load current of a maximum value I.

Moreover, current I determines an output ripple, V_R[2]

$$V_R = \frac{T}{C_L} I. \tag{5}$$

To conclude the parameter definition, we introduce the "*jth Voltage Increment*," $\Delta V_j(n)$, as the voltage growth over the initial value of the jth node after the nth clock period

$$\Delta V_j(n) = V_j(n) - V_j(0). \tag{6}$$

The "*Output Maximum Voltage Increment*," $\Delta V_{N+1}(\infty)$, as the maximum voltage increment in the output node

$$\begin{aligned}\Delta V_{N+1}(\infty) &= \lim_{n\to\infty} \Delta V_{N+1}(n) \\ &= \lim_{n\to\infty} [V_{N+1}(n) - V_{N+1}(0)]\end{aligned} \tag{7a}$$

which according to [14] is given by

$$\begin{aligned}\Delta V_{N+1}(\infty) &= V_{cc} - (N+1)V_\gamma \\ &\quad + N(1-\varepsilon' - \varepsilon'')V^* - V_{N+1}(0) \\ &= NV'.\end{aligned} \tag{7b}$$

The "*Increase factor*," α, as the ratio between the *Voltage Increment* at the output after n clock period and the *Output Maximum Voltage Increment*

$$\alpha = \frac{\Delta V_{N+1}(n)}{\Delta V_{N+1}(\infty)}. \tag{8}$$

B. Fundamental Equation

As follows from the Appendix I, a representation in the z-domain of an N-stage voltage multiplier is given below

$$\mathbf{A} \cdot \mathbf{V} = \mathbf{C} \tag{9}$$

where (see matrix below). In (9) z represents the time $T/2$. In fact, the voltage variations on each node (except the output) change in each half clock period. Moreover, it is worth noting that since the variables of (9) are the voltage growth of nodes, they have a zero initial condition.

[2]In practical voltage multipliers there will also be an additional ripple component due to capacitance coupling from the clocks through the diodes. It is given by $V_R = [TI + \kappa C_D(1-\varepsilon')V^*]/C_L$, where C_D is the capacitance across each diode and κ is equal to 1 and 2 for nonoverlapping and overlapping clock, respectively [14].

TABLE I

N	X_N	$\frac{1}{\ln(X_N)}$
1	$\frac{K}{1+K}$	$-(K+0.5)$
2	$\frac{1+2K}{2+2K}$	$-(2K+1.5)$
3	$\frac{5K+3+\sqrt{9K^2+14K+9}}{8(K+1)}$	$-(3K+3.4)$
4	$\frac{3K+2+\sqrt{K^2+2K+2}}{4(K+1)}$	$-(4K+6.2)$

III. Simplified Voltage Multiplier Model

A Simplified Model and Design Equations

To obtain the dynamic model in the time domain of a Dickson voltage multiplier with N stages versus the parameter K, we must symbolically solve (9) and seek the inverse z-transform of the voltage $\Delta V_{N+1}(z)$. In the following we refer to the clock period T, because the output voltage changes once for each clock period.

The exact solutions of (9) up to N equal to 4 can be obtained by [17] and [19], and by adopting some mathematical simplifications for a 3- and 4-stage multiplier they can be represented

$$\Delta V_{N+1}(n) = N(1 - X_N^n)V' \tag{10}$$

where X_N is a function of K which changes with N, as shown in Table I. However, (9) cannot be solved to have a symbolic model for a number of stages greater than 4.

In order to obtain useful equations, we can state from (10) the number of cycles required to reach a fixed output voltage versus the capacitor ratio K. Substituting (8) in (10) we have

$$(1 - X_N^n) = \alpha \tag{11}$$

$$\mathbf{V} = \begin{bmatrix} \Delta V_1(z) \\ \Delta V_2(z) \\ \vdots \\ \Delta V_N(z) \\ \Delta V_{N+1}(z) \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ \dfrac{z}{z-1} V' \end{bmatrix}$$

$$\mathbf{A} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & \dots & 0 & 0 & 0 & 0 \\ -1 & 2z & -1 & 0 & 0 & \dots & 0 & 0 & 0 & 0 \\ 0 & -1 & 2z & -1 & 0 & \dots & 0 & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & 0 & \dots & -1 & 2z & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & \dots & 0 & -1 & 2z & -1 \\ 0 & 0 & 0 & 0 & 0 & \dots & 0 & 0 & -z & (K+1)z - Kz^{-1} \end{bmatrix}$$

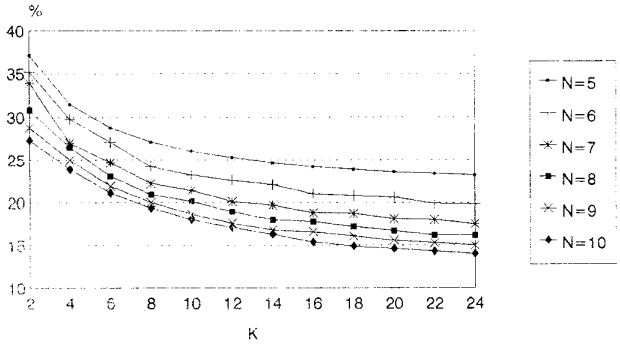

Fig. 2. Errors between exact model and (14) with $\alpha = 0.8$.

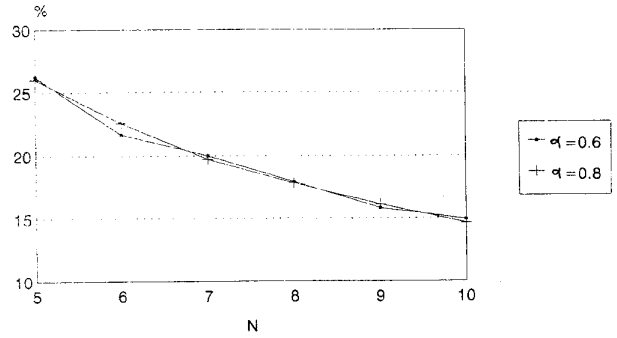

Fig. 3. Errors between exact model and (14) with $K/N = 2$.

which leads to

$$n = \frac{\ln(1-\alpha)}{\ln(X_N)}. \tag{12}$$

To have more simple equations to manage, we can develop $1/\ln(X_N)$ in a Taylor series around the point $K = 1$ assuming α to be constant. The results are given in the last column of Table I, and for $K \geq 1$ have an error of less than 4%.

An analysis of the developments in Table I (last column) and their substitution in (12), allows the model below to be extracted

$$n = -N(K + 0.4N)\ln(1-\alpha). \tag{13}$$

Hence, parameter K versus the number of clock periods required to have a voltage increment of α is given by

$$K = -\frac{n}{N\ln(1-\alpha)} - 0.4N. \tag{14}$$

The simple form of (13) and (14) leads us to think that they also hold for a number of stages greater than 4. This is true and we will show it in the next section. Hence, (13) and (14) represent a simplified dynamic model for an N-stage voltage multiplier.

B. Model Validation

To validate the dynamic model given by (13) for a voltage multiplier with more than 4 stages, we compare it with the exact solution given by (9). More specifically, by normalizing the solution of (9) to the *Maximum Output Voltage Increment* (i.e., to value NV_γ), choosing the number of stages N and the parameter K, we solve the system numerically and seek the number of clock periods required for a specified value of α. This number is then compared with that given by (13).

The results of the comparison for a voltage multiplier with a number of stages ranging from 5–10, and assuming $\alpha = 0.8$ are shown in Fig. 2. It is apparent that the error decreases with an increase in both the number of stages and the parameter K. Moreover it is positive, i.e., the number of clock periods given by (13) is greater than that found by solving (9).

Since we are often interested in the area utilized in the voltage multiplier, and knowing that the area is proportional to the sum of the capacitors in the multiplier, in Fig. 3 the error for a value of K/N equal to 2 versus the number of stages is reported (K/N is the ratio between the load capacitor C_L and the whole capacitance of the voltage multiplier). This error decreases as the number of stages increases, and, as can be seen from Fig. 2, it decreases as the value of K/N increases.

C. Design Example

To understand the pencil and paper design procedure better, we consider, for example, a power MOS which needs a voltage of 8–10 V to work in the triode region with a C_L of about 1 nF. The circuit has a power supply of 2.5 V and a clock amplitude equal to about 2.1 V. For the sake of clarity, we consider an application in which no current is supplied at the output, and so a 5-stage voltage multiplier is needed. Observe that the diodes have a very low V_γ ($V_\gamma < 0.3$ V) since out of the commutation they are biased in the subthreshold region. For applications in which the voltage multiplier supplies a maximum current I, the number of stages can be obtained using the equations in Appendix II.

Assuming a clock period of 2 μs (i.e., a frequency of 500 kHz) and searching for 80% of the Maximum Voltage Increment in 0.2 ms (i.e., a charge pump output voltage of about 8 V in 100 clock periods), from (2) and (14), we found a value of K equal to 10.4. Hence, a charge pump capacitor C of about 100 pF is needed. Simulation of the designed circuit with SPICE and the model parameters of a Smart Power IC (used by ST-Microelectronics to build the VM 205), and implementing the diodes with bipolar transistors, gives a number of 86 clock periods to allow the desired output value to be reached [i.e., an error of about 18% as compared with that given by (14)].

IV. Conclusion

In this brief, we have proposed a simple dynamic model for Dickson voltage multipliers made up of any number of stages, which is useful for a pencil and paper design with an acceptable safety margin. The importance of having a model like this is not only because it increases understanding of the dynamic behavior of these circuits, but, as shown above, it also helps in the design procedure, giving an initial estimate of the silicon area required for the circuit to be used.

The model can also be adopted for voltage multipliers with MOS switches by properly setting the parasitic capacitance C_s which can be assumed as the largest source-bulk or drain-bulk capacitances of MOS switches, and setting $V_\gamma = 0$. Otherwise, the model is not appropriate for voltage multiplier with MOS diodes, because the increasing voltage across the reverse-biased source-substrate junction will lead to a continuous variation in the threshold voltage of the MOS diodes which affect both the *Output Maximum Voltage Increment* [16] and the dynamic behavior in a nonnegligible way [20].

Appendix I

Without loss of generality we assume N to be an even integer, and analyze the N-stage circuit in the two timeframes in which the clock signal is low or high. The voltage variations on each node (except the output) change in each timeframe, and to simplify the mathematical

representation, we introduce a time variable T' which is half of the clock period T. The two time frames under consideration are $]2nT', 2nT'+T'[$, and $]2nT'+T', 2nT'+2T'[$. We point out that the last node (i.e., the output node of the circuit) is the $(N+1)$th node.

In the first timeframe V_{ck} is low (i.e., $V_{ck} = V_{cc} - V^*$). As a consequence the diodes D_{2j-1} (j being a positive integer) are in forward bias, and the diodes D_{2j} are in reverse bias [Fig. 4(a)]. From charge conservation we have

$$\begin{aligned}
&V_1(2nT') \cdot \\
&\quad = V_{cc} - V_\gamma \\
&V_2(2nT') + V_3(2nT') \\
&\quad = V_2(2nT' - T') + V_3(2nT' - T') \\
&\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
&V_{2j}(2nT') + V_{2j+1}(2nT') \\
&\quad = V_{2j}(2nT' - T') + V_{2j+1}(2nT' - T') \\
&\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
&V_N(2nT') + KV_{N+1}(2nT') + \frac{\varepsilon''}{2} V^* \\
&\quad = V_N(2nT' - T') + (1 - \varepsilon')V^* \\
&\qquad + KV_{N+1}(2nT' - T') \qquad \text{(A1.1)}
\end{aligned}$$

In the second timeframe V_{ck} is high (i.e., $V_{ck} = V_{cc}$). As a consequence the diodes D_{2j} are in forward bias, and the diodes D_{2j-1} are in reverse bias [Fig. 4(b)]. This leads to

$$\begin{aligned}
&V_1(2nT' + T') + V_2(2nT' + T') \\
&\quad = V_1(2nT') + V_2(2nT') \\
&\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
&V_{2j+1}(2nT' + T') + V_{2j+2}(2nT' + T') \\
&\quad = V_{2j+1}(2nT') + V_{2j+2}(2nT') \\
&\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
&V_{N-1}(2nT' + T') + V_N(2nT' + T') \\
&\quad = V_{N-1}(2nT') + V_N(2nT'). \qquad \text{(A1.2)}
\end{aligned}$$

Observing that for $t \in]2nT', 2nT' + T'[$ is

$$V_{2j}(2nT') = V_{2j+1}(2nT') + V_\gamma \qquad \text{(A1.3)}$$

and for $t \in](2n+1)T', (2n+1)T' + T'[$ is

$$V_{2j+1}(2nT' + T') = V_{2j}(2nT' + T') + V_\gamma \qquad \text{(A1.4)}$$

moreover, using the voltage increments $\Delta V_j(n)$ as variables and assuming the initial condition given by

$$V_j(0) = V_{cc} - j \cdot V_\gamma \quad j \in [1,\ N+1]. \qquad \text{(A1.5)}$$

Equations (A1.1) and (A1.2) become

$$\begin{aligned}
\Delta V_1(2nT') &= 0 \\
2\Delta V_2(2nT' + T') &= \Delta V_1(2nT') + \Delta V_3(2nT') \\
2\Delta V_3(2nT') &= \Delta V_2(2nT' - T') \\
&\quad + \Delta V_4(2nT' - T') \\
&\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
2\Delta V_{2j}(2nT' + T') &= \Delta V_{2j-1}(2nT') + \Delta V_{2j+1}(2nT')
\end{aligned}$$

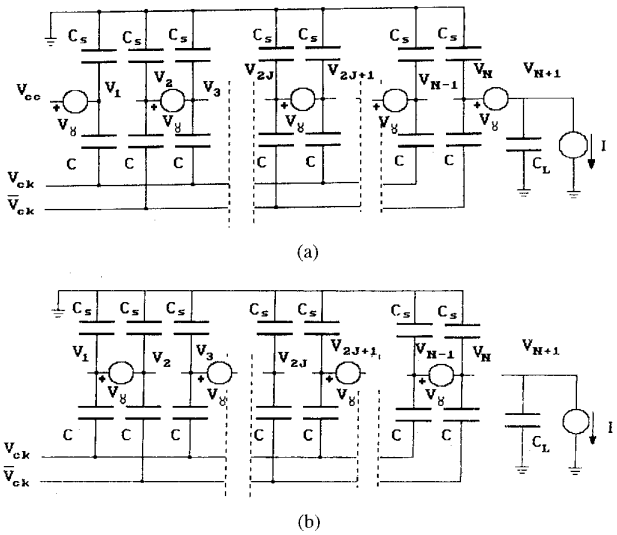

Fig. 4. N-stage voltage multiplier. (a) V_{ck} low (i.e., $V_{ck} = V_{cc} - V^*$); and (b) V_{ck} high (i.e., $V_{ck} = V_{cc}$).

$$\begin{aligned}
2\Delta V_{2j+1}(2nT') &= \Delta V_{2j}(2nT' - T') \\
&\quad + \Delta V_{2j+2}(2nT' - T') \\
&\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \\
2\Delta V_N(2nT' + T') &= \Delta V_{N-1}(2nT') + \Delta V_{N+1}(2nT') \\
(K+1)\Delta V_{N+1}(2nT') &= \Delta V_N(2nT' - T') \\
&\quad + K\Delta V_{N+1}(2nT' - T') \\
&\quad + \left(1 - \varepsilon' - \frac{\varepsilon''}{2}\right) V^*. \qquad \text{(A1.6)}
\end{aligned}$$

Let us observe that V_{N+1} changes its value only in one of the time frames considered. As a consequence

$$V_{N+1}(2nT' - T') = V_{N+1}(2nT' - 2T') - \frac{\varepsilon''}{2K} V^*. \qquad \text{(A1.7)}$$

by z-transforming (A1.6) with (A1.7) we can express it by the matrix in (9).

Appendix II

The desired voltage increment ΔV_w must be greater than $\Delta V_{N+1}(\infty)$. Thus, from (5) and (7b) the number of stages is given by

$$N \geq \frac{\Delta V_w}{(1 - \varepsilon')V^* - KV_R}. \qquad \text{(A2.1)}$$

Substituting (14) in (A2.1) and solving for N, we have (A2.2) shown at the bottom of the page. A simplified solution can be found by neglecting the constant term $0.4N$ in (14), and then substituting in (A2.1). Now, the solution is given by

$$N \geq \frac{\Delta V_w}{(1 - \varepsilon')V^*} \frac{n}{-\ln(1 - \alpha)} \frac{V_R}{(1 - \varepsilon')V^*}. \qquad \text{(A2.3)}$$

$$N \geq \frac{(1 - \varepsilon')V^*}{0.4V_R} \left[\sqrt{1 + 1.6 \frac{V_R \Delta V_w}{(1 - \varepsilon')^2 V^{*2}} + 1.6 \frac{n}{-\ln(1 - \alpha)} \frac{V_R^2}{(1 - \varepsilon')^2 V^{*2}}} - 1 \right]. \qquad \text{(A2.2)}$$

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The Influence of the Reverse Early Effect on the Performance of Bandgap References

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***Abstract*— In the literature three key-parameters are commonly used for the design of bipolar bandgap references: E_G (bandgap energy), I_S (saturation current) and X_{TI} (exponent of the temperature behavior of I_S). This paper shows that four key parameters exist: these three and V_{AR}, the reverse Early voltage. This parameter models the influence of the base-width modulation at the base-emitter junction on the collector current. A general expression for the error in the output voltage caused by the reverse Early effect is derived and a comparison is made with other errors.**

I. INTRODUCTION

The design of an electronic circuit starts with the mathematical description of the desired function. Several basic operations can be distinguished in this mathematical description. For accurate prediction and optimal performance of the electronic implemented operation and for minimizing the *systematic* errors, the behavior of these basic blocks must be known extensively. A systematic design theory for each of these basic blocks will provide the required knowledge [1].

An important aspect of a design theory is the identification of the key parameters. This is the minimal set of parameters that has to be known for an accurate design of the circuit.

One of the basic blocks is the bandgap reference. This paper shows that four key parameters exist for the design of bandgap references:

E_G bandgap energy
I_S saturation current
X_{TI} exponent of the temperature behavior of I_S
V_{AR} reverse Early voltage

In the literature [2], [3], and [4] the first three parameters are well known. The fourth parameter V_{AR} is not well known. Its influence is generally accounted for by the fitting of I_S. The drawback of this method is that two different physical phenomena, saturation current and base-width modulation, are modeled with one parameter and this parameter looses thereby its physical meaning. Further, for the transistor parameters for the design of bandgap references a dedicated parameter extraction needs to be done.

This brief describes the influence of the V_{AR} on the behavior of bandgap references, so that the standard extracted parameters of a process can be used.

The starting point is the Gummel and Poon model from which a minimal set of parameters is deduced for the design of bandgap references. The influence of the reverse Early effect on the temperature behavior is calculated. Finally, the error due to the Early effect is compared with other errors, e.g., absolute and matching errors of base-emitter junctions, absolute, and matching errors of resistors and amplifier offset.

II. THE FIRST-ORDER COMPENSATED BANDGAP REFERENCE

The first-order temperature behavior of a first-order compensated bandgap reference should ideally be zero. A first-order compensated

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