高雄工專學報

JOURNAL OF KAOHSIUNG INSTITUTE OF TECHNOLOGY

第十七期
VOLUME XVII

中華民國七十六年十二月

DECEMBER 1987

目　錄　CONTENTS

ANALYSIS AND DESIGN OF SWITCHING POWER AMPLIFIERS

Chin-Yuan Hsu

ABSTRACT

A push-pull switching power amplifier is proposed which is a four-quadrant converter, capable of having bipolar voltages and currents on its output. At any moment, one constituent converter of the amplifier is processing power from dc to ac side, while the other converter does the reverse. If the output is attached to a passive load, then the direction of the net power is from the dc side to the ac side. This is because more power is processed toward the ac side than the returning power and the difference is dissipated by the load. All of the advantages of the constiuttent converter, such as high efficiency, small size and weight are present in the amplifier. However, design of a linear switching amplifier is different from that of a dc converter, owing to different constraints (such as power bandwidth) and continuous large-signal variation of the states of the system. These differences, along with the low frequency distortion caused by the nonlineear gain of some dc converters, are discussed. Regulation of the output allows tight control of the harmonics and therefore distortion of the output. Also it desensitizes the output to variations of the supply voltage, load, or other parameters of the system. Thus, control aspects are analyzed next. The results of control techniques are demonstrated, through analysis and construction of a push-pull power amplifier comprising two 'Cuk converters. The design includes the analysis of the complete anplifier. A feedback loop is placed around the system and the placement of the poles and zeros of the loop gain at the two extremes of duty ratio are examined to ensure the stability of the amplifier.

1. Introduction

Switching power amplifiers are counterparts of linear amplifiers, and have an ideal efficiency of 100%. Therefore they can find attrative applications in high efficiency, low cost, small size and weight servo power amplifiers, and also in low cost, high performance audio power amplifiers.

Since the principles of operation of switching power amplifiers are not widely known, a brief discussion of their operation is included in Section 2. The problem is approached by generalization of a dc-to-dc converter, in which the limitation imposed by the unidirectional switehes is eliminated by a bidirectional switch. Then, the dc converter alone can process current and therefore power in both directions. Still, the output voltage is unipolar and techniques to generate bipolar output voltage are examined. Finally, the push-pull method is introduced which used a single voltage source and two current-bidirectional dc-to-dc converters to power a load which is differentially connected to the outputs of the converters. Full four quadrant ac operation is obtained which is capalbe of driving general load, including reactive load. Commonly, it is desired to regulate the output of the amplifier and so feedback loop(s) are placed around the system. Regulation of the output allows tight control of the harmonics and therefore disortion of the output.

However, design of a linear switching amplifier is different from that of a dc converter, owing to different constraints and continuous large-signal variation of the states of the system. Section 3 elaborates these differences, along with the low-frequency distortion caused by the nonlinear gain of some dc converters. Also, control aspects are discussed in this section.

The results of control technigues are demonstrated in Section 4, through analysis and construction of a push-pull power amplifier comprising two 'Cuk converters. The design includes the analysis of the complete amplifier. Finally, a feedback loop is placed around the system and the placement of the poles and zeros of the loop gain are examined to ensure the stability of the closed-loop system.

2. Configuration of Switching Amplifier

2.1 Two-Quadrant Converter and Push-Pull Configuration

An ordinary switched-mode dc-to-dc converter, illustrated by a 'Cuk converter [1] in Fig. 2.1a is considered a one-quadrant converter. The unidirectional capability is imposed upon the converter by the actual transistor-diode implementation of the switch. A unidirectional switch limits the operation to one direction of current, and because the unit is also capable of production of only unipolar voltages, the converter is limited to one quadrant. By a simple addition of another transistor Q_2, as shown in Fig. 2.1b, the switch and therefore the converter becomes current-bidirectional. A simple change of the duty ratio makes the converter look either as a current source or as a current sink.

The problem of the generation of a bipolar voltages at the output is solved by the symmetrical push-pull method shown in Fig. 2.1c. The inverter comprises two current-bidirectional dc converters driven by a modulator with complementary outputs. At duty ratio D=0.5 both converters are driven with the same pulse trains (despite the out of phase drive). Thus, the output voltages of the two converters with respect to ground are the same. The load is differentially placed across the outputs and therefore sees zero voltage. Now, if the duty ratio of one converter is increased, its output voltage increases. However, by the complementary nature of the drive, the duty ratio of the other converter, and consequently its output voltage, decreases. Therefore, there is a net voltage across the load. By symmetry, reduction of duty ratio of the first converter from 0.5 causes the voltage across the load to reverse its polarity. Also, when the load draws current, one converter sources the current while the other sinks the current. For the other direction of current, the roles of the converters reverse, calling for current-bidirectional converters. Hence the name push-pull truly reflects its operation.

The push-pull structure of Fig. 2.1c is not limited to the particular converter, but is general and can be implemented with a bidirectional version of any dc-to-dc converter. Fig. 2.2 shows the general push-pull amplifier where the blocks with double-headed arrows indicate bidirectional dc-to-dc converters. If an ac voltage is applied to the input of the modulator, the output is an ac voltage whose amplitude and phase depends on the specific converter and its dynamics. Therefore two dc-to-dc switching converters and a modulator with complementary outputs are constituent parts of a switching push-pull amplifier, and Fig. 2.3 shows push-pull amplifiers employing basic converters [2].

2.2 Regulated Push-Pull Switching Amplifier

Commonly, it is desired to regulate the output of the amplifier

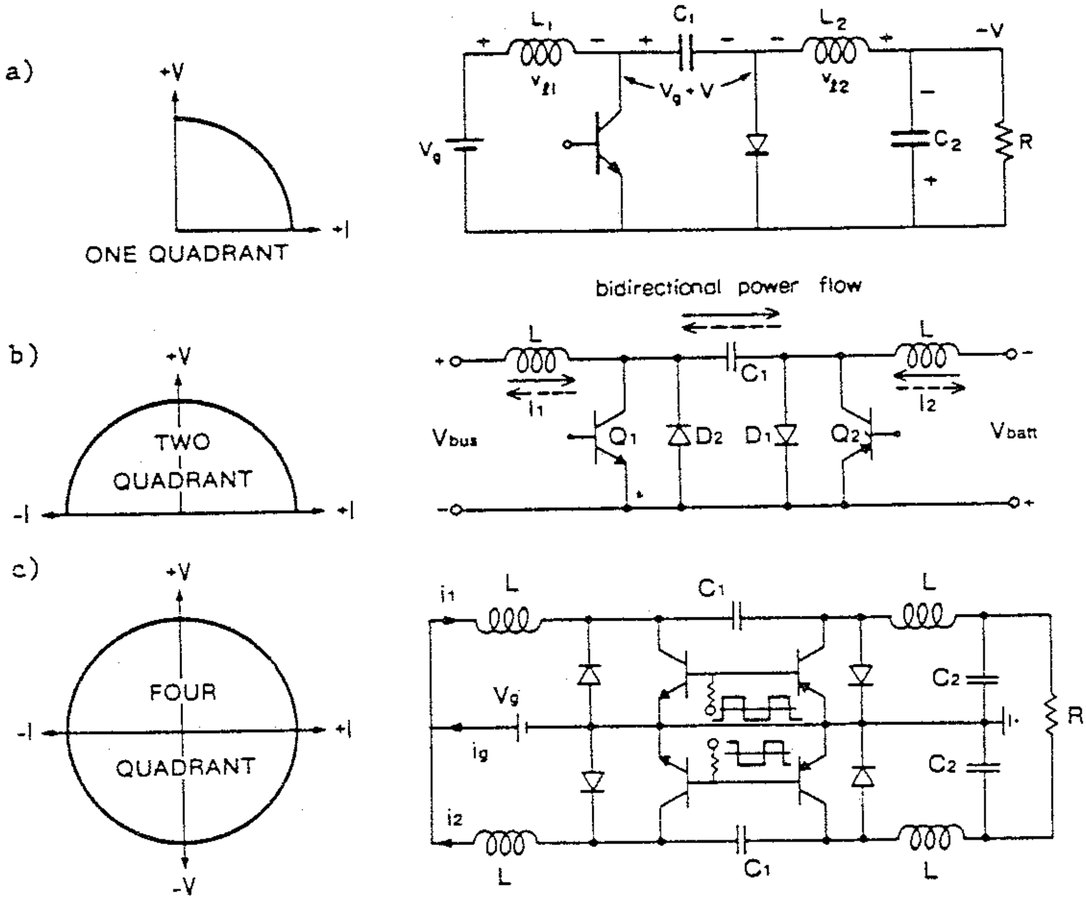


Fig. 2.1 Generalization of dc-to-dc converters. (a) Single-quadrant, (b) current-bidirectional (2-quadrant), (c) push-pull amplifier (4-quadrant).

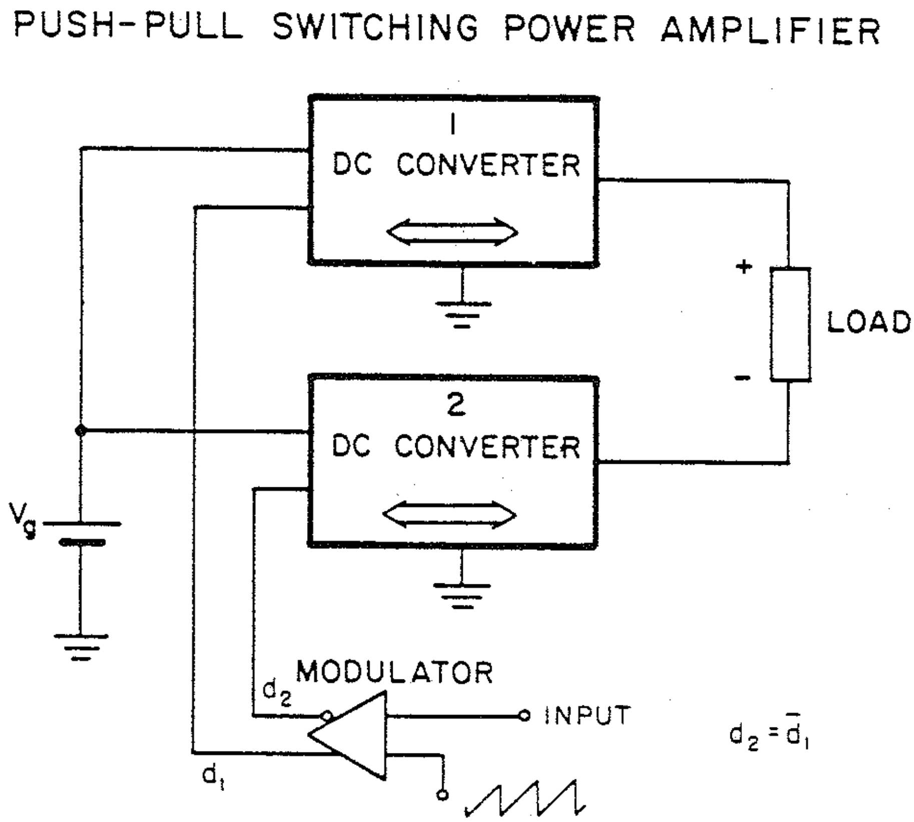


Fig. 2.2 A general push-pull switching power amplifier. Arrows denote current-bidirectionality.

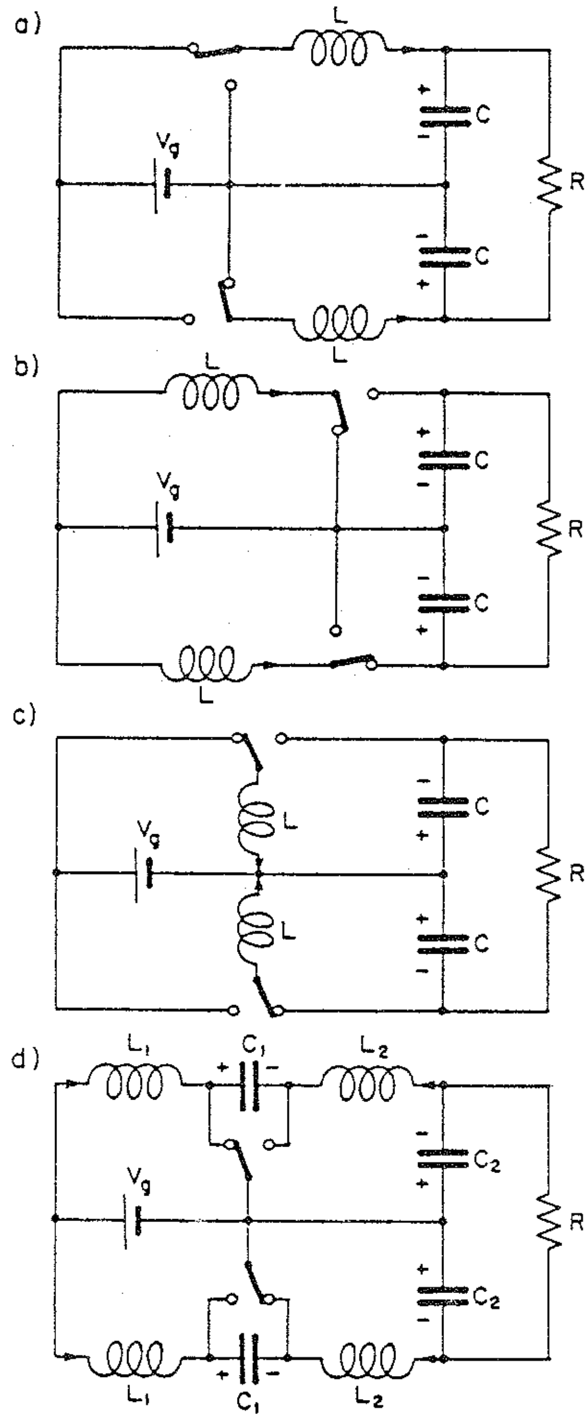


Fig. 2.3 Four push-pull switching amplifiers each consisting of two current-bidirectional converters.

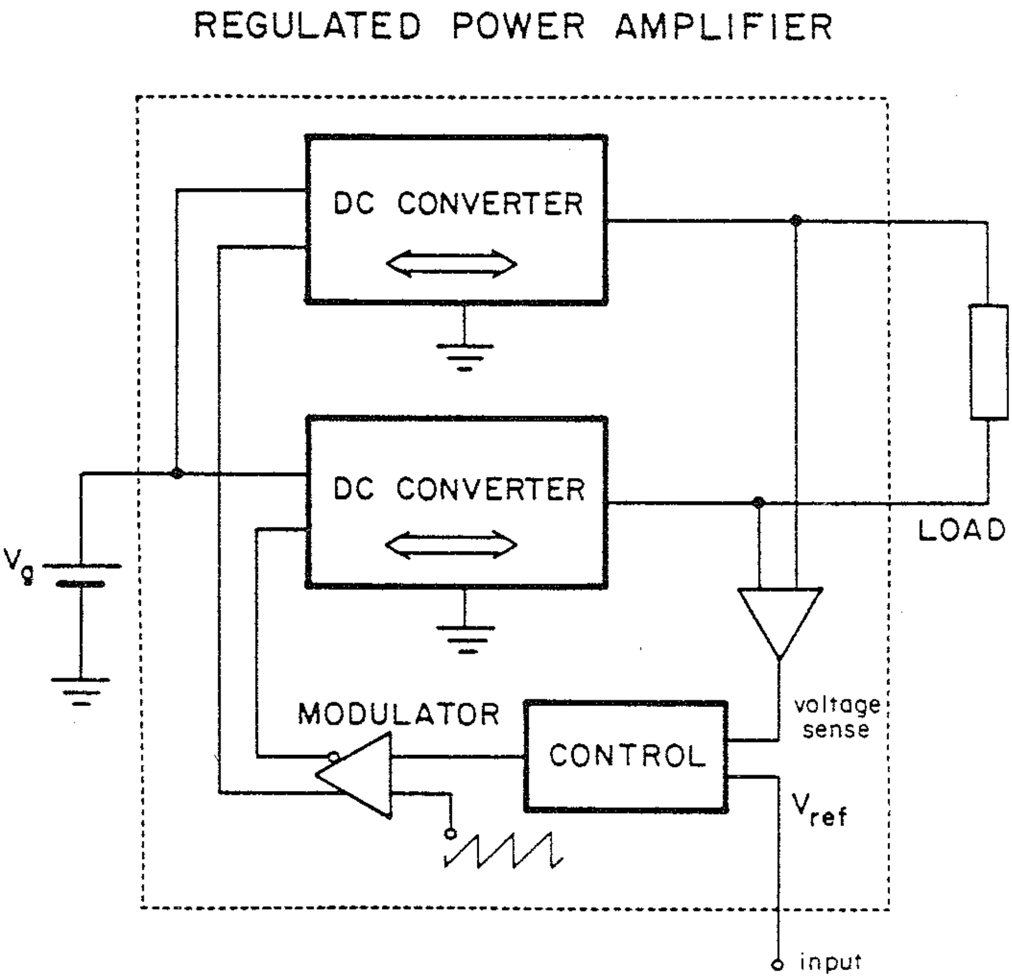


Fig. 2.4　Output voltage regulation of a push-pull amplifier. The sensed output voltage is compared with the reference voltage and the error is kept minimal by the feedback loop.

and so feedback loop(s) are placed around the system, as in Fig. 2.4 The output voltage is sensed (and other states if necessary), and then compared with a reference signal. The error signal is processed through the compensation network and is used to keep the output as close to the reference as possible. If the reference signal is an audio signal and the converters have sufficient bandwidth, the system becomes a switched-mode audio amplifier.

3. Analysis of Switching Amplifier

3.1 Differences Between Dc and Ac Systems (considerations of freq. response and linearity)

The fundamental difference between a dc and ac system is that, in a dc system, the operating point is set at a fixed point, except upon occasional disturbances when it changes to accommodate regulation (closed-loop); while, in an ac system, by its nature, the operating point experiences regular large variations. The ac system, therefore, must be able to tolerate these large variations.

These variations are not just in duty ratio and, for example in the case of the output voltage, the states of the system must handle a full scale variation over the desired frequency range. This immediately puts a constraint on the amplifier: the open-loop duty ratio-to-output frequency response must have a bandwidth at least as large as the maximum output frequency. Otherwise, if frequencies higher than the bandwidth of the open-loop system are imposed on the duty ratio, the output cannot follow the maximum peak variation owing to the filtering effect of the converters. That is, the power bandwidth is less than the small-signal bandwidth. This is analogous to slew rate limit of conventional linear operational amplifiers.

If a feedback loop is placed around the amplifier, the crossover frequency may be set at a high frequency, but the full power bandwidth of the amplifier remains at the open-loop value. For applications such as audio amplifiers, the corner-frequency is placed at the maximum audible frequency ($\simeq$ 20 KHz). While frequencies up to this limit must pass through the filter unaffected, the switching frequency must be attenuated as much as possible, and therefore the switching frequency must be much higher than the maximum bandwidth. Also, in order to lighten the task of the feedback loop around the complete amplifier, it is desired to make the open-loop system as close to ideal as possible.

Another difference between dc and ac system is in the "transfer ratio" from input to output of the amplifier. For an accurate large signal reproduction of a signal at the output of an amplifier, the gain characteristic (transfer ratio) must be linear. The transfer ratio is the dc gain (duty ratio-to-output) of the amplifier. Any nonlinearity of this characteristic is irrelevant in case of dc outputs, since the system is linearized around any operating point (for small perturbations), while in the case of the large variations in an ac system, it can cause severe distortion problems.

The calculation of the dc gain is simplified if all the parasitics of the circuit are neglected, whereby the dc loading effect of one stage upon the other becomes negligible. In the ideal case, One writes the output voltage as

$$\frac{V_o}{V_g} = M(D) - M(D') \tag{3.1}$$

where M is the ideal gain of one dc converter. At D=D'=0.5, the output has zero voltage. The duty ratio is determined by the modulator, and with the normal linear sawtooth input, the duty ratio is directly proportional to the input voltage [3]:

$$D=\frac{V_i}{V_{ramp}} \tag{3.2}$$

The transfer ratio V_o/V_i can be linear if the individual gains are formed such that Eq. (3.1) is linear versus D. This happens in the case of a buck converter

$$M(D)= D \qquad \frac{V_o}{V_g} = D-D' = 2D-1 \tag{3.3}$$

In the case of other basic converters [2], the individual and thus the overall gain is nonlinear

$$\text{boost:} \quad \frac{V_o}{V_g} = \frac{1}{D'} - \frac{1}{D} = \frac{D-D'}{DD'} \tag{3.4}$$

$$\begin{array}{c}\text{buck-boost}\\ \&\\ \text{Cuk}\end{array} \quad \frac{V_o}{V_g} = \frac{D}{D'} - \frac{D'}{D} = \frac{D-D'}{DD'} \tag{3.5}$$

However, as was mentioned before, Eq. (3.1) does not apply to nonideal cases. The loading effect of one converter in series with the load upon the other converter causes each dc gain to be different from that of a single, nonideal converter. For this reason, in general, the complete amplifier must be analyzed to find the input-to-output relationship. Consider the case of the boost amplifier of Fig. 3.1 with parasitic inductor resistance included. If one calculates the overall gain from the individual converter gains. the following incorrect result is obtained by use of Eq. (3.1):

$$\frac{V_o}{V_g} = \frac{1}{D'}\,\frac{1}{(1+\alpha/D'^2)} - \frac{1}{D}\,\frac{1}{(1+\alpha/D^2)}$$

$$= \frac{D-D'}{DD'}\,\frac{1-\dfrac{\alpha}{DD'}}{1+\alpha\left(\dfrac{1}{D^2}+\dfrac{1}{D'^2}\right)+\alpha^2\left(\dfrac{1}{DD'}\right)^2} \qquad (3.6)$$

where $\alpha \equiv \dfrac{R_\ell}{R}$

However, if we calculate the dc gain of the complete amplifier, the correct expression is obtained as follows. We write the state-space equations during each switching interval.

during dT_s:

$$P\dot{x} = \begin{bmatrix} L\dfrac{di_1}{dt} \\ L\dfrac{di_2}{dt} \\ L\dfrac{dv_1}{dt} \\ L\dfrac{dv_2}{dt} \end{bmatrix} = \underbrace{\begin{bmatrix} -R_\ell & 0 & 0 & 0 \\ 0 & -R_\ell & 0 & -1 \\ 0 & 0 & -\dfrac{1}{R} & \dfrac{1}{R} \\ 0 & 0 & \dfrac{1}{R} & -\dfrac{1}{R} \end{bmatrix}}_{A_{11}} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix}}_{b_{11}} \underbrace{v_g}_{v_g} \qquad (3.7)$$

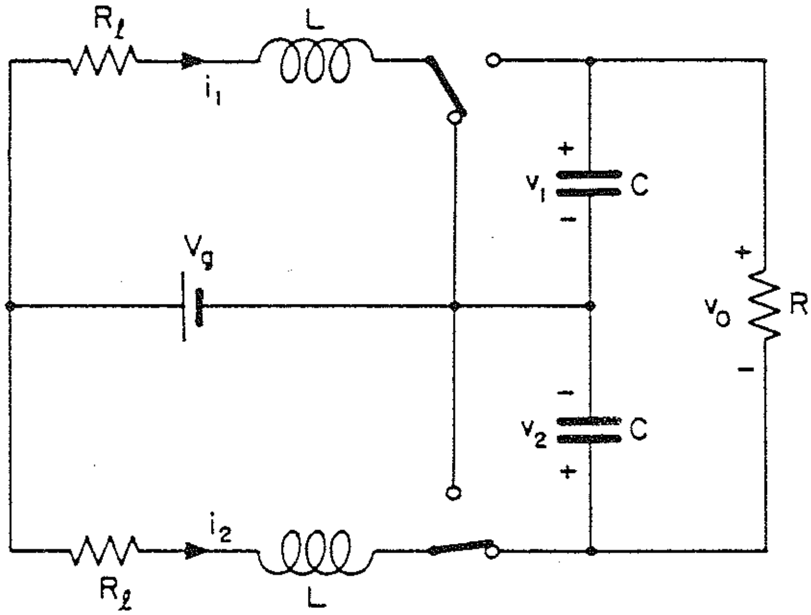


Fig. 3.1 Boost amplifier example with parasitics inductor resistances included.

Similarly during $d'T_s$:

$$P\dot{x}=\underbrace{\begin{pmatrix} -R_\ell & 0 & 1 & 0 \\ 0 & -R_\ell & 0 & 0 \\ 1 & 0 & -\frac{1}{R} & \frac{1}{R} \\ 0 & 0 & \frac{1}{R} & -\frac{1}{R} \end{pmatrix}}_{A_{22}} \underbrace{\begin{pmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{pmatrix}}_{x} + \underbrace{\begin{pmatrix} 1 \\ 1 \\ 0 \\ 0 \end{pmatrix}}_{b_{22}} \underbrace{v_g}_{v_g} \tag{3.8}$$

Notice that the equations are kept in the form $P\dot{x}= Ax + Bu$ by the averaging method, whereby the dc solution immediately eliminates the reactive elements $P\dot{x} = 0$. Now we apply the averaging method to Eqs. (3.7) and (3.8) to obtain:

$$0 = \begin{pmatrix} -R_\ell & 0 & -D' & 0 \\ 0 & -R_\ell & 0 & -D \\ D' & 0 & -\frac{1}{R} & \frac{1}{R} \\ 0 & 0 & \frac{1}{R} & -\frac{1}{R} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \\ V_1 \\ V_2 \end{pmatrix} + \begin{pmatrix} 1 \\ 1 \\ 0 \\ 0 \end{pmatrix} V_g \tag{3.9}$$

Solution of Eq. (3.9) for the output voltage, that is V_1-V_2, results in

$$\frac{V_o}{V_g} = \frac{D-D'}{DD'} \; \frac{1}{1+\alpha\left(\frac{1}{D^2}+\frac{1}{D'^2}\right)} \tag{3.10}$$

This is the general result, and its comparison with Eq. (3.6) shows that the magnitude of the true output voltage is always larger than predicted by Eq. (3.1) and, depending on the values of the X vector and D, and the difference between the two equations may be large.

The same procedure may be applied to other amplifier configurations of Fig. 2.3 and the following results are obtained

$$\text{buck}: \frac{V_o}{V_g} = (D - D') \frac{1}{1 + 2\alpha} \qquad \text{linear}$$

$$\text{boost}: \frac{V_o}{V_g} = \frac{D - D'}{DD'} \frac{1}{1 + \alpha\left(\frac{1}{D^2} + \frac{1}{D'^2}\right)} \tag{3.11}$$

$$\text{buck boost}: \frac{V_o}{V_g} = \frac{D - D'}{DD'} \frac{1}{1 + \alpha\left(\frac{1}{D^2} + \frac{1}{D'^2}\right)}$$

$$\text{Cuk}: \frac{V_o}{V_g} = \frac{D - D'}{DD'} \frac{1}{1 + \left(\frac{D^2}{D'^2} + \frac{D'^2}{D^2}\right) + 2\beta},$$

$$\alpha = \frac{R_{\ell_1}}{R} \qquad \beta = \frac{R_{\ell_2}}{R}$$

Equations (3.11) show that the gain functions of the nonlinear amplifiers are still nonlinear, except that the additional degree of freedom α may be used to shape the characteristic. The gain of the boost, buck-boost, and 'Cuk amplifiers is considerably higher than that of the buck amplifier. Therefore, much less duty ratio variation is needed to produce a specific amplitude at the output. Also, α may be selected to produce a flat region on the gain curve to ensure minimum distortion. For example, for the same boost converter of Fig. 3.1 the gain is calculated by the substitution D=0.5+a, where a is the variation of the duty ratio from the quiescent operation point of 0.5. We get:

$$\frac{V_o}{V_g} \quad \frac{8a}{1-4a^2+8\alpha\frac{1+4a^2}{1-4a^2}} \tag{3.12}$$

Selection of α =1/16 causes the first order nonlinearity (coefficient of a^2) to vanish, and the gain becomes

$$\frac{V_o}{V_g} = \frac{8a}{1.5 + 16a^4 + \cdots\cdots} \tag{3.12}$$

Following similar steps for the 'Cuk amplifier shows that $\beta \triangleq \frac{R_{\ell_2}}{R}$ is not important and maximum linearity is obtained at α =1/14. Of course, a β of zero yields the best efficiency. Fig. 3.2 shows

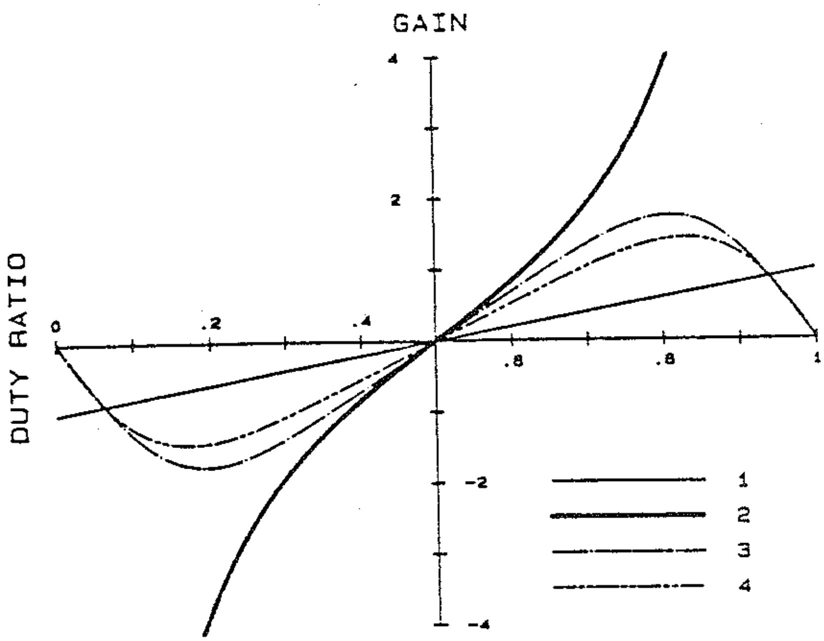


Fig. 3.2 Dc gain characteristics of various push-pull amplifiers. (1) Ideal buck, (2) ideal others, (3) linearized 'Cuk, and (4) linearized boost and buck-boost.

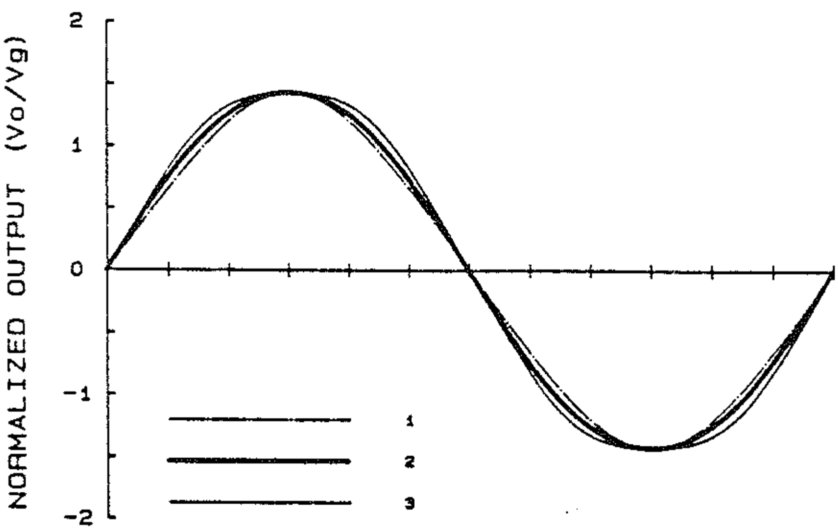


Fig. 3.3 Low frequency sine waves generated by nonlinear amplifiers. (1) Ideal (all), (2) linearized 'Cuk, and (3) linearized boost and buck-boost.

the dc gain characteristics of the basic converters. The initial gains of the ideal buck amplifier, ideal nonlinear amplifiers (described by Eqs. (3.4) and (3.5)), linearized boost and buck-boost, and the linearized 'Cuk amplifier are 2, 8, 5.33, and 7 respectively. The sine waves of Fig. 3.3 are generated by a lossless boost, a linearized boost, and a linearized 'Cuk amplifier. Table 3.1 contains pertinent results of these outputs.

Table 3.1

	ideal boost	linearized boost	linearized 'Cuk
Duty ration excursion	0.160	0.310	0.212
Peak gain	1.42	1.42	1.42
% Total harmonic distortion	2.70	4.90	1.25

3.2 Control Aspcets

Analysis of an amplifier involves an understanding of the dynamics of the two consitituent converters and their interactions with each othr and the load. However, the main difference is the regular larger variation of the operating point versus only occasional perturbation in dc-to-dc converters. The system is nonlinear and its dynamic is related to the operating point and duty ratio; hence the dynamic also experiences large variations. The control system must be designed in such a way as to consider all these facts.

As with the dc gain, in order to correctly include effects of all interactions of the various elements on the dynamics of the system, one must analyze the converter as a whole. The small-signal analysis verifies stability of the system at each operating point.

This is the case if the bandwidth of the converter is much larger than the large signal injection frequencies, whereby the output and the states of the system are on a trajectory corresponding to steady-state solutions of various duty ratios. At each duty ratio and its corresponding steady-state vector, the system may be analyzed by finding the associated small-signal dynamics. If the localized set of the resultant system is stable, then the design is complete. Therefore, the loop is designed for the small-signal amplifier model around the duty ratio of 0.5 for high performance, and then is checked to be acceptable at other duty ratios. In case of unacceptable performances, the original design is modified and the process continues until a satisfactory result is obtained.

There still are unmentioned a few fundamental differences between the dc and ac systems. In a dc system incorporating feedback loop(s), the output can be regulated to be very close to some preset value. This is possible by use of very high loop gains. One way of obtaining very high gains is to have an integrator in the feedback loop. For dc systems, the regulation is mainly at low frequencies and the integrator has an infinite ideal gain at dc. Therefore such a dc system can have a theoretically perfect dc regulation. However, in an ac system, the output of interest contains frequencies other than zero, where the integrator has a finite gain. Therefore, a perfect regulation is not possible, but the error may be kept to a satisfactorily low level by proper design. A dc component on the output of an ac system is prohibited, and therefore use of an integrator is highly desirable in order to ensure a zero dc level at the output.

With these constraints in mind, one can start to analyze the system. As mentioned earlier, the analysis is performed around the quiescent point and then checked for other operating points. In push-pull amplifiers the quiescent point is at duty ratio D=0.5 where the system is symmetric. That is, owing to the complete symmetry, one may be able to analyze the complete circuit by considering only one converter. However, at other duty ratios the loading of one converter by the other is such that the two cases are not exactly the same. Therefore, in order fully to understand the dynamics of the amplifier, the total system must be considered.

The procedure is clarified by the example of the boost amplifier introduced in Section 3.1. The state equations are repeated here for convenience:

$$Px = Ax + Bu$$

where

$$P = \begin{bmatrix} L & 0 & 0 & 0 \\ 0 & L & 0 & 0 \\ 0 & 0 & C & 0 \\ 0 & 0 & 0 & C \end{bmatrix}, \quad A = DA_{11} + D'A_{22} = \begin{bmatrix} -R & 0 & -D' & 0 \\ 0 & -R & 0 & -D \\ D' & 0 & -\frac{1}{R} & \frac{1}{R} \\ 0 & D & \frac{1}{R} & -\frac{1}{R} \end{bmatrix}$$

$$B = \begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \end{bmatrix} \qquad (3.14)$$

$$x = \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix}, \quad u = V_g, \quad A_{11} - A_{22} = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & -1 \\ -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}$$

$$B_{11} - B_{22} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Perturbation and linearization of the first equation results in:

$$P\,\dot{\hat{x}} = A\,\hat{x} + B\,\hat{u} + [(A_{11}-A_{22})X + (B_{11}-B_{22})U]\,\hat{d} \qquad (3.15)$$

and

$$(sP-A)\,\hat{x}(s) = B\,\hat{u}\,(s) + [(A_{11}-A_{22})X+(B_{11}-B_{22})U]\hat{d}(s) \qquad (3.16)$$

Substitute Eq. (3.14) into Eq. (3.16) to find the control-to-output transfer functions

$$\begin{bmatrix} sL+R_\ell & 0 & D' & 0 \\ 0 & sL+R_\ell & 0 & 0 \\ -D' & 0 & sC+\frac{1}{R} & -\frac{1}{R} \\ 0 & -D & -\frac{1}{R} & sC+\frac{1}{R} \end{bmatrix} \begin{bmatrix} i_2(s) \\ i_2(s) \\ v_1(s) \\ v_2(s) \end{bmatrix} = \begin{bmatrix} V_1 \\ -V_2 \\ -I_1 \\ I_2 \end{bmatrix} \hat{d}(s) \qquad (3.17)$$

At duty ratio D=0.5, the steady state values are as follows:

$$I_1 = I_2 = 0 \qquad (3.18\,a)$$

$$V_1 = V_2 = \frac{V_g}{D} = 2V_g \qquad (3.18b)$$

The duty ratio-to-output transfer function $H(s)=(\hat{v}_1(s)-\hat{v}_2(s))/\hat{d}(s)$ is then derived from Eg. (3.17) in which Eg. (3.18) is substituted

$$H(s) = 8V_g\,\frac{1 + 4R_\ell\,Cs + 4\,LCs^2}{\Delta} \qquad (3.19\,a)$$

and

$$\Delta = (1+8\frac{R_\ell}{R}) + [\,8\,\frac{L}{R} + R_\ell C\,(32\frac{R_\ell}{R} + 8\,)]\,s + [\,LC\,(8+64\frac{R_\ell}{R}) +$$

$$16\,R_\ell^2\,C^2\,]\,s^2 + 32\,LC\,(\,\frac{L}{R} + R_\ell\,C\,)\,s^3 + 16\,L^2C^2s^4 \qquad (3.19\,b)$$

Notice that the denominator of Eq. (3.19) can be factorized as follows:

$$\Delta = (1+4R_\ell Cs+4LCs^2)\left[1+8\frac{R_\ell}{R}+\left(8\frac{L}{R}+4R_\ell C\right)s+4LCs^2\right] \tag{3.20}$$

in which the first term exactly cancels out the numerator of Eq. (3.19a), resulting in

$$H(s) = 8V_g \frac{1}{1+8\frac{R_\ell}{R}+\left(8\frac{L}{R}+4R_\ell C\right)s+4LCs^2} \tag{3.21}$$

The cancellation of numerator may seem coincidental at first, but it is explained by the symmetry of the circuit and the fact that at duty ratio D=0.5 the two converters do not load each other.

Although this simplifies the design phase of the system, a complete analysis requires verification of the dynamics around each duty ratio. The general analysis cannot be simplified because the converters have different dynamics at different duty ratios and each imposes its response on the load. Consequently, the complete amplifier must be considered. For example, at D=0.5, Eq. (3.19), shows two poles and zeros which are exactly on top of each other and thus cancel. However, at duty ratios other than 0.5, the poles and zeros move to different locations. Since they are high Q pole and zero pairs, this movement causes a glitch in the response. Furthermore, at duty ratios other than 0.5, another zero appears in the response whose position is again related to duty ratio. As excursion of duty ratio from 0.5 increases, one of these zeros may enter the right half-plane. If the feedback circuitry is not designed for this movement, the system may go unstable.

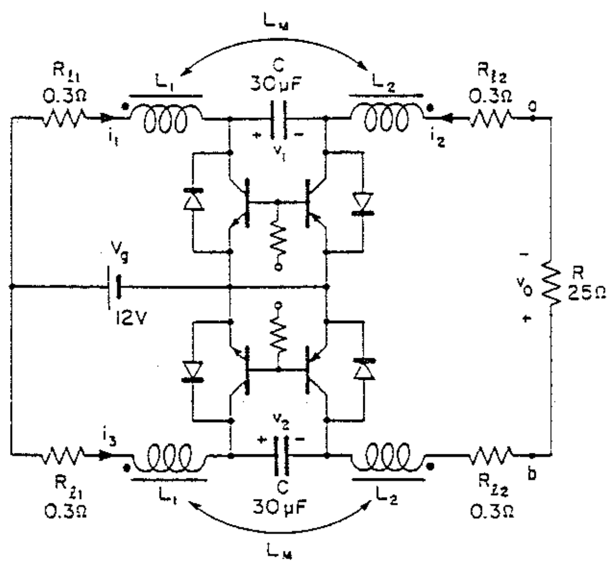
It must be noticed that the above discussion refers to nonlinear gain ampolifiers. The buck amplifier is a simple case in which the positions of neither the poles nor the zeros are dependent on duty ratio or steady-state conditions. Therefore, the design, once made, is final and no further verification are required. This, along with the linear dc gain characteristic of the power stage, makes the buck amplifier an attractive choice. Nontheless, the nonlinear amplifiers have higher gains to allow reproduction of a certain output with much lower duty ratio excursions. With small excursions, the position of poles do not changes considerably, while the zeros still can move in the s-plane over a wide range. To design the loop, one may first try an ordinary single loop system. If unsuccessful, multiple-loop feed-back can be the answers.

4. Design-Oriented Example of Push-Pull Amplifier

The design of a coupled-inductor 'Cuk amplifier [4,5,6,7] is reviewed in this section. The topology is a nonlinear one and the coupled-inductor version provides a very low ripple on the output current. In fact, with proper design, one can completely cancel the output ripple, and with such a configuration one may eliminate all the capacitors on the output ports. Fig. 4.1 shows the basic amlifier section with the output capacitors removed.

Despite the coupling of inductors, to first order, the dc analyses of this amplifier and the uncoupled version are the same (since for dc calculations, the ripples are generally ignored). For this reason, the dc analysis done in Section 3.1 is still valid and shows that for a maximally expanded region of linearity in the dc gain characteristics, one needs a total of 1/14 of the load resistance in series with the input inductance ($R_\ell /R=1/14$). This approach, while improving the distortion problem, has an undesirable effect on efficiency. So, we must make a compromise between distortion and efficiency. One way to minimize the problem is to keep the resistance R_{ℓ_1} as low as possible for better efficiency and stable dynamics and transfer the correction of distortion to the feedback loop.

Analysis of the control-to-output transfer function of the amplifier starts with the state-space equations in each switching interval. When the upper npn transistor in Fig. 4.1 is on, it represents the DTs interval while an inverse situation represents the D'Ts interval. Each converter has three states, but owing to cancellation of one state at the output circuit, the amplifier has only



$$L_1 = L_M = 1\,\text{mH}$$

$$L_2 = 1.05\,\text{mH}$$

Fig. 4.1 Coupled-inductor 'Cuk amplifier.

five independent states. After writing state equations in each position of the switch and performing the averaging process, one obtains the following:

$$
\begin{bmatrix} L_1 & L_M & 0 & 0 & 0 \\ 0 & -L_M & L_1 & 0 & 0 \\ L_M & 2L_2 & -L_M & 0 & 0 \\ 0 & 0 & 0 & C & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix}
\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{bmatrix}
=
\begin{bmatrix} -R_{\ell_1} & 0 & 0 & -D' & 0 \\ 0 & 0 & -R_{\ell_1} & 0 & -D \\ 0 & -R-2R_{\ell_2} & 0 & D & -D' \\ D' & -D & 0 & 0 & 0 \\ 0 & D' & D & 0 & 0 \end{bmatrix}
\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ v_1 \\ v_2 \end{bmatrix}
+
\begin{bmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_g
$$

$$
P \qquad \dot{x} \quad = \qquad A \qquad x \; + Bu \tag{4.1}
$$

We take the Laplace transform, and substitute the steady-state conditions (D=0.5) for the vector $[(A_{11}-A_{22})X+(B_{11}-B_{22})U]$ as in Eq. (3.15). Aslo, for simplicity, we absorb $R_{\ell 1}$ and $R_{\ell 2}$ into $L_1 s$ and R respectively, that is, substitute $L_1 S$ for $L_1 S+R_{\ell 1}$ and R for $R+2R_{\ell 2}$. Later in this section we recover the full result by making the reverse substitution. Through these process, one gets:

$$
\begin{bmatrix} sL_1 & sL_M & 0 & 0.5 & 0 \\ 0 & -sL_M & sL_1 & 0 & 0.5 \\ sL_M & 2sL_2+R & -sL_M & -0.5 & 0.5 \\ -0.5 & 0.5 & 0 & sC & 0 \\ 0 & -0.5 & -0.5 & 0 & sC \end{bmatrix}
\begin{bmatrix} \hat{i}_1(s) \\ \hat{i}_2(s) \\ \hat{i}_3(s) \\ \hat{v}_1(s) \\ \hat{v}_2(s) \end{bmatrix}
=
\begin{bmatrix} 2 \\ -2 \\ 4 \\ 0 \\ 0 \end{bmatrix} Vg\hat{d}(s) \tag{4.2}
$$

One may find the control transfer function $H(s)=R\hat{i}_2(s)/\hat{d}(s)$ by use of Cramer's rule. The following is obtained:

$$H(s)=8V_g\frac{1+2C(L_1-L_M)s^2}{1+2\frac{L_1+2L_M+L_2}{R}s+4L_1Cs^2+8\frac{C(L_1L_2-L_M^2)}{R}s^3} \qquad (4.3)$$

in which the common factor $(1+4L_1Cs^2)$ in numerator and denominator has been cancelled.

It turns out that the matching condition under which the zero ripple condition exists [1] can be modelled by $L_1=L_M$. Then, with the definition $L_2=L_M+L_e$, substitution into Eq. (4.3) resutls in

$$H(s)=\frac{8V_g}{1+2\frac{4L_M+L_e}{R}s+4L_MCs^2+8\frac{CL_ML_e}{R}s^3} \qquad (4.4)$$

Provided that $R >> 2\sqrt{L_e/C}$, the denominator can be further approximated into two factors

$$H(s)\cong\frac{8V_g}{(1+2\frac{L_e}{R}s)(1+8\frac{L_M}{R}s+4L_MCs^2)} \qquad (4.5)$$

This shows the presence of a complex pole pair at moderate frequencies with another real pole at high frequencies. There are no zeros, and with the real pole being at high frequencies, the circuit behaves essentially as a two-pole system which can be regulated by use of classical control theory. With the actual values shown on Fig. 4.1, the approximate poles are found to be

f_{p1} = 39.8 KHz (39.4 KHz)

f_{p2} = 459 Hz (462 Hz) Q_{p2} = 1.08 (1.08)

The exact poles directly calculated from Eq. (4.4) are shown in parentheses beside each value to confirm the accuracy of the approximate results.

The calculations carried out so far neglect the parasitics. However, parasitics can be included by simple resubstitutions of $L_1s + R_{\ell_1}$ for L_1s and $R+2R_{\ell_2}$ for R in Eq. (4.3):

$$H(s) = H_o \frac{1 + 2R_{\ell_1} Cs}{1 + \frac{2R_{\ell_1}}{R+2R_{\ell_2}} + \left(\frac{4L_M+L_e}{R+2R_{\ell_2}} + 4R_{\ell_1} C\right) s + \left(4L_M + 8\frac{R_{\ell_1}}{R+2R_{\ell_2}} L_2\right) Cs^2 + 8\frac{CL_M L_e}{R+2R_{\ell_2}} s^3}$$

where

$$H_o = 8V_g \frac{R}{R+2R_{\ell_2}} \qquad (4.6)$$

Comparison of Eq. (4.6) with the previous result of Eq. (4.4) shows that the parasitics have lowered the gain, slightly modified the position of the poles and their Q, and finally have created a new zero by interaction with the energy transfer capacitor C. Also, change of R only modifies the Q of the resonance. Fig. 4.2 shows the control-to-output transfer function of Eq. (4.6). Since the system is essentially second order, design of the feedback loop is simple and is done by insertion of a zero in the loop. Fig. 4.3 shows the simple compensation network used in the control circuit, in which V_e is the error which passes through the compensation network to the modulator, V_c. The lead-lag network comprised of R_1, R_2, and C_1 generates a zero and a pole for phase correction purposes, and C_2 is the integrator capacitor. The resistor around C_2 is for simulation of the limited gain of the operational amplifier and is not physically present. Although there wil be some output error owing to the finite loop gain, the integrator can null the dc component of the output voltage completely. The integrator can also be used to boost the loop gain at low frequencies to reduce the error and thus improve th distortion problem. However, in this case, the duty ratio deviation from the quiescent value of 0.5 must be small (0.1max).

The addition of a moderate amount of loop gain improves the distortion to an acceptable point, and the integrator in this case was used solely for dc cancellation. Fig. 4.4 shows the result of theoretical calculations of loop gain. The calculated phase margin is 67 degrees.

All that remains to be checked is the sensitivity of the loop gain to the operating point. In this case, only the control-to-output transfer function need be checked, because the remaining poles and zeros are due to the compensation network and not duty ratio dependent. The calculation shows a strong dependence of the control-to-output transfer function zeros upon the parasitics. For example, at duty ratio of 0.5, Eq. (4.3) shows a pair of zeros on the imaginary axis if $R_{\ell 1}$ and $R_{\ell 2}$ are ignored. At any duty ratio

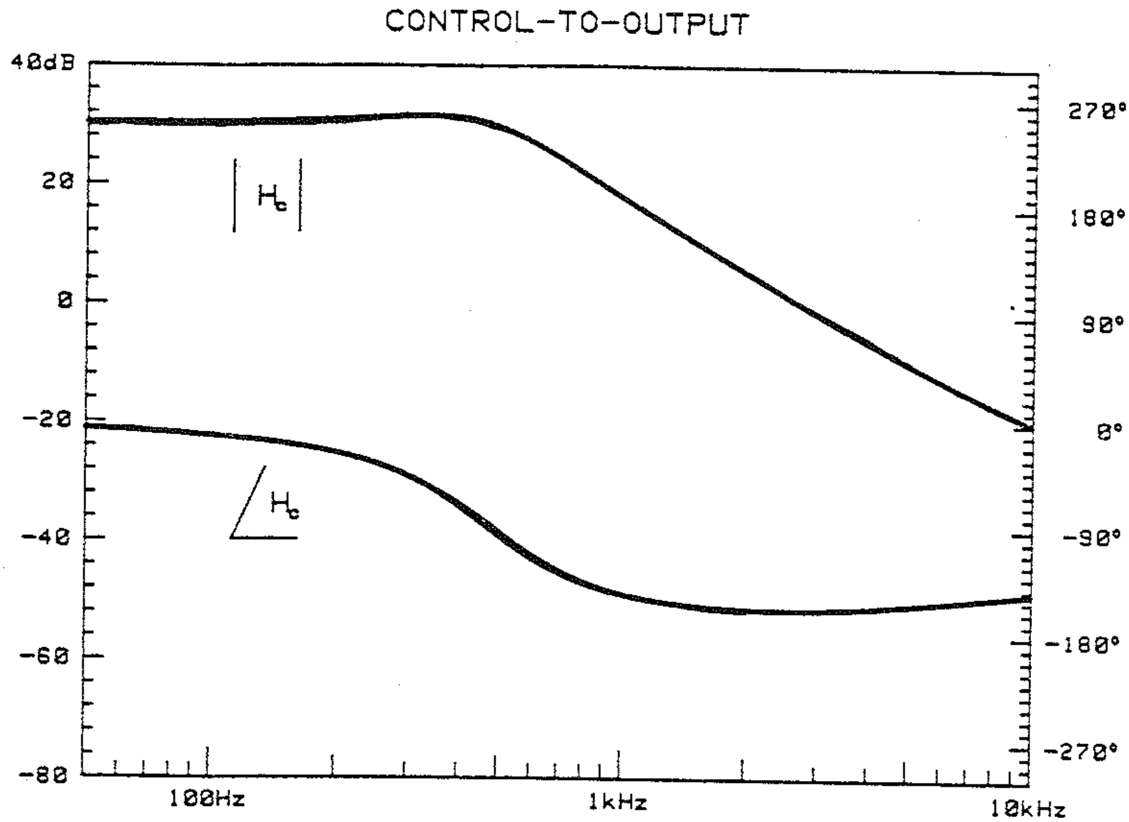


Fig. 4.2 Predicted control-to-output transfer function of the 'Cuk amplifier.

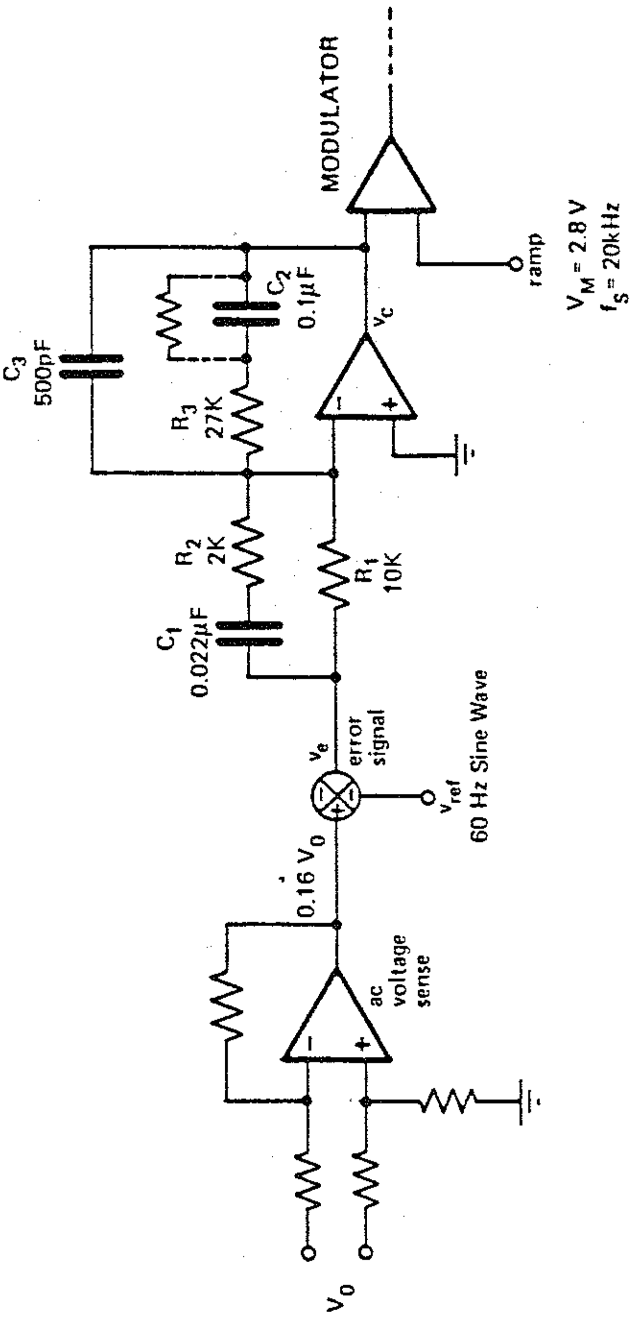


Fig. 4.3 Complete control circuitry of the 'Cuk amplifier.

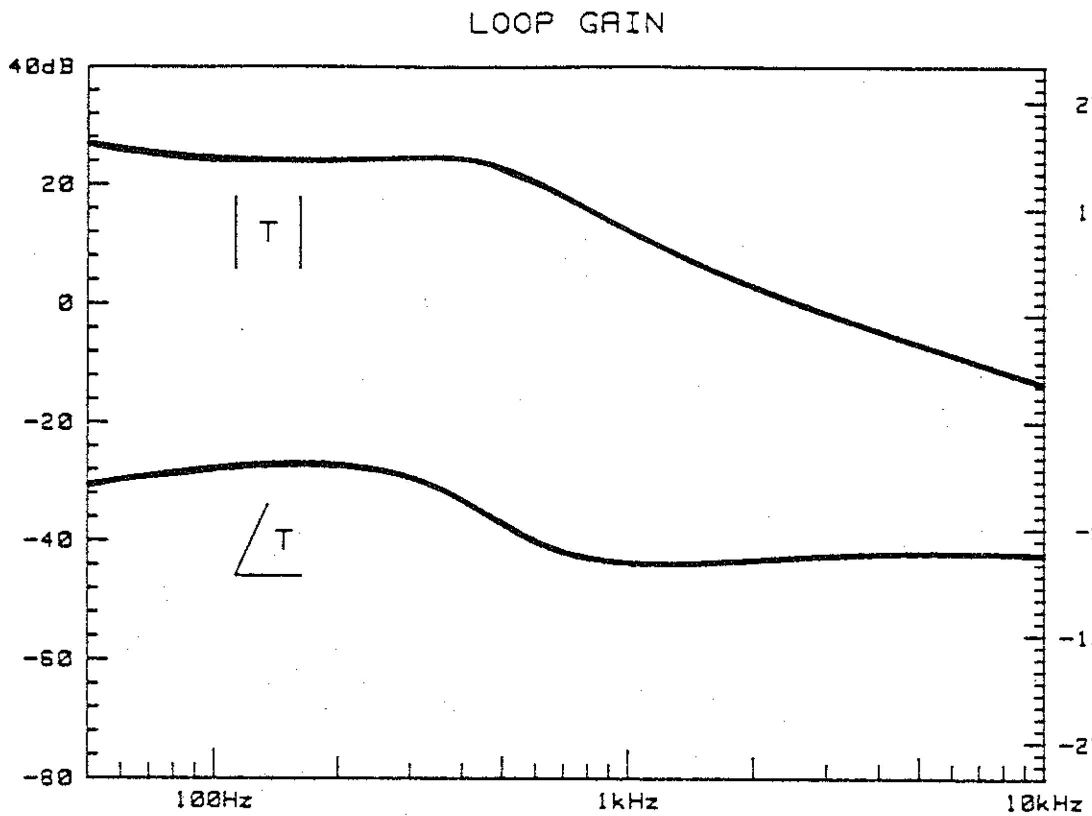


Fig. 4.4 Predicted loop gain.

other than 0.5, these zeros move to the right half-plane, which makes design of the control much more difficult. However, this movement is very small, and addition of a very small amount of parasitic $R_{\ell 1}$ solves the problem. The common factor in the numerator and denominator, $1+4L_1Cs^2$, changes to $1+4R_{\ell 1}Cs+4L_1Cs^2$, giving a negative real part to poles and zeros. If $R_{\ell 1}$ is large enough, the changes of duty ratio over the whole range can bring the zeros closer to the imaginary axis, but the zeros will never cross it. In the present example, the inherent parasitics of the circuit $R_{\ell 1} = R_{\ell 2} = 0.3\ \Omega$ were enough to keep the zeros in the left half-plane. Owing to symmetry of the amplifier around duty ratio of 0.5, the conditions at duty ratios of D=0.5+a and D=0.5-a are the same, so excursions on only one side need be considered. Table 4.1 shows the placement of the poles and zeros of the loop gain at the two extremes of duty ratio. Calculation of the loop gain at duty ratio of 0.6 (D_{max}) shows a phase margin of 56 degrees. Therefore, all the design steps have been corect and the design of the amplifier is complete.

Table 4.1

D = 0.5			D = 0.6		
$i_1 = 0$			$i_1 = 0.568$ A		
$i_2 = 0$			$i_2 = 0.377$ A		
$i_3 = 0$			$i_3 = -0.252$ A		
$v_1 = 24$ V			$v_1 = 29.6$ V		
$v_2 = 24$ V			$v_2 = 20.1$ V		
Poles					
459	Hz	Q = 9.62	485	Hz	Q = 3.56
461	Hz	Q = 1.01	421	Hz	Q = 1.15
41.3	KHz	Real	41.3	KHz	Real
Zeros					
459	Hz	Q = 9.62	466	Hz	Q = 32
8.84	KHz	Real	28.8	KHz	Real

5. Conclusions

A fundamental difference exists between the switching amplifier and the switching power supply: amplifier must reproduce continual large-signal variations of a control signal, whereas the power supply need only regulate a dc output against the occasional external perturbations which may occur. Consequently, there is a need to identify the features of the switching amplifier which limit its large-signal performance, and then formulate a tractable procedure for its large-signal analysis and design.

A general switch-mode push-pull power amplifiers are discussed in detail. The amplifier module contains two current-bidirectional dc-to-dc converters and a modulator with complementary outputs. The load is placed differentially on the outputs of the converters. The ideal 100% efficiency is not the only difference between switching amplifiers and their linear counterparts. A full-power sine wave can be generated at the load as long as the open-loop amplifier is capable of doing so. That is, the power bandwidth of the system is equal to its open-loop bandwidth. Furthermore, a system with a power bandwidth much larger than its input signal frequency, is assumed to pass through a series of steady-state conditons. It was shown that except for the buck amplifier, the other types of converters have nonlinear dc gain characteristics which produce an overall nonlinear gain. However, the gain is much higher, and addition of small parasitics was shown to linearize the dc gain characteristic to a considerable extent. Furthermore, the large-signal variations of duty ratio and states of the system results in movement of the poles and zeros of the control-to-output transfer function. As an analogy to the linear amplifiers, the feedback loop is designed around a nominal quiescent operating point and then is checked for stability at the maximum excursions. At a duty ratio of 0.5 (the quiescent operating point) the two constituent converters of the systme are exactly at the same conditions. And the usual right half-plane zeros of the converters do not appear in the response since they are generated by currents which are in this case zero. Since no dc is allowed in the ac output, a very high loop-gain at dc is mandatory. The feedback design is performed following the preceding simplifications and guidelines. Then, the loop gain is checked for possible variations caused by the dependence of the amplifier dynamics on the operating point.

Finally, these points were demonstrated by an amplifier composed of two coupled-inductor 'Cuk converters. A thorough examination of the dynamics showed an effective two-pole resonse for the control characteristic of the amplifier, and the feedback loop was then easily designed. The importance of the parasitic shows up in analysis of the system at non-quiescent operating conditions. It was shown that even small values of parasitic resistances are enough to prevent movement of some zeros to the right half-plane. Thus the parasitics, even though undesirable from the efficiency point of view, can improve both the dc and ac performances of an amoplifier. This completes the analysis of the switching amplifier.

REFERENCES

[1] Slobodan 'Cuk and R. D. Middlebrook, "A New Optimum Topology Switching Dc-to-Dc Converter," IEEE Power Electronics Specialists Conference, 1977 Record, pp. 160-179 (IEEE Publication, 77CH1213-8 AES).

[2] R. D. Middlebrook and Slobodan 'Cuk "A General Unified Approach to Modeling Switching-converter Power Stages," IEEE Power Electronics Specialists Conference, 1976 Record, pp. 18-34, Cleveland, OH, June 8-10, 1976.

[3] R. D. Middlebrook "Predicting Modulator Phase Lag in PWM Converter Feedback Loops, " Proc. Eighth International Solid-State Power Conversion Conference (Powercon 8), pp. H4.1-H4.6, April 1981.

[4] Slobodan 'Cuk and R. D. Middlebrook, "Coupled-Inductor and Other Extensions of a New Optimum Topology Switching Dc-to-Dc Converter," IEEE Industry Applications Society Annual Meeting, 1977 Record, pp.1110-1126 (IEEE Publication 77CH1246-8-IA).

[5] Slobodan 'Cuk and Robert W. Erickson, "A Conceptually New High-Frequency Switched-Mode Amplifier Techniqure Eliminates Current Ripple," Proc. Fifth National Solid-State Power Conversion Conference (Powercon 5), pp. G3.2-G3.22, May 1978.

[6] Slobodan 'Cuk and R. D. Middlebrook, "Advances in Switched-Mode Power Conversion," Robotics Age, Vol. 1, no. 2, pp. 6-18, Winter 1979.

[7] Slobodan 'Cuk "A New Zero-Ripple Switching Dc-to-Dc Converter" IEEE Power Electronics Specialists Conference, 1980 Record, pp. 12-32, Atlanta, GA, June 16-20, 1980.

交換式功率放大器之分析和設計

徐 晋 元

摘 要

本文提出一個推挽型交換式功率放大器，它是一個四象限（four quadrant）轉換器，在輸出端，有雙極性（Bipolar）的電壓和電流關係。在任何瞬間，此放大器中的一個轉換器將功率從直流（DC）側輸送到交流（AC）側，同時，其另一個轉換器做反方向的功率傳送。如果輸出端加上一個被動負載，則淨功率的方向將從直流側到交流側。這是因爲，傳送到交流側的功率比其反方向回來的功率較多，而此功率之差則被負載所消耗。因此，所有組成轉換器的優點，如高效率、小體積和重量等均表現於此放大器。然而，線性交換式放大器的設計是不同於直流轉換器的設計，這是由於有不同的限制（例如功率頻寬）和連續的系統狀態之大訊號變動。這些差異點，以及由一些直流轉換器的非線性增益所造成的低頻失眞，將於本文中加以討論。對輸出電壓的調整可嚴密控制輸出諧波和失眞的發生。同時，它也會減低電源電壓、負載、或其他系統參數的變動對輸出電壓的影響。因此，〞控制細節〞將分析於後。這些控制技術的結果，將以由兩個 'Cuk Converter 組成的放大器之分析加以證示。此設計將包括整體放大器的分析。最後在此系統上，加上一個授回路（feed back loop），然後再檢查回路增益（loop gain）在工作週期比（Duty ratio）之兩端點時的極點（Poles）和零點（Zeros）位置，以確保此放大器的穩定。

國立高雄工專學報第十七期

Journal of
National Kaohsiung Institute of Technology
Volume X VII

發 行 人：吳　建　國

Publisher: Wu Chien-Kuo

校　　址：高雄市三民區建工路415號

Address: 415 Chien-Kung Road, Kaohsiung (80782) Republic of China

電　　話：(07)3814526(5)

T E L：(07)3814526(5)

印 刷 所：正合印刷有限公司

電　　話：2319705，2718635

中 華 民 國 七 十 六 年 十 二 月