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Analog Dialogue

Op Amp Input Overvoltage Protection: Clamping vs. Integrated

by **Daniel Burton**

Introduction

High precision op amps enable system designers to create circuits that condition signals (amplify, filter, and buffer) while maintaining the precision of the original signal. When information is contained in very small variations of the signal, it is critical that op amps in the signal path perform their operation while contributing very little dc and ac error. The precision of the total system depends on maintaining the precision of the signal path.

In some applications, a situation may occur in which the inputs of the op amp get driven by voltages outside the level of the supply voltages—this is called an overvoltage condition. For example, if an op amp is configured to run with its positive supply at +15 V and its negative supply at -15 V, any time an input pin goes more than one diode drop beyond those supply rails (such as ± 15.7 V), the op amp's internal ESD protection diodes can be forward-biased and start conducting current. Excessive input current over long periods of time or even short periods of time, if the current is high enough, can damage the op amp. This damage can result in a shift in the electrical specification parameters beyond the data sheet's guaranteed limits; it can even cause a permanent failure of the op amp. When system designers are faced with this possible situation, they often add overvoltage protection (OVP) circuits at the inputs to the amplifier. The challenge then is to add OVP circuitry without adding errors (loss of system precision).

How Overvoltage Conditions Occur

Overvoltage Protection Method Overvoltage conditions can be caused by a number of different situations. Consider a system where a remote sensor is located in the field—for example, measuring fluid flow in a refinery and sending its signal through a cable to data acquisition electronics that reside at a different physical location. The first stage in the data acquisition electronics signal path can often be an op amp configured as a buffer or a gain amplifier. The input to that op amp is exposed to the outside world and therefore can be subjected to overvoltage

incidents, like a short circuit from a damaged cable or incorrectly connecting the cable to the data acquisition electronics.

Similarly, a situation that can cause an overvoltage condition is when an input signal that is usually within the input voltage range of the amplifier suddenly receives an external stimulus causing a transient spike that exceeds the op amp's supply voltages.

A third scenario that can result in an input overvoltage condition comes from the power-on sequence of the op amp and other components in the signal path. For example, if the signal source, such as a sensor, gets powered up before the op amp does, the output of the source can start to output a voltage that will then be applied to the input of the op amp even though the op amp supply pins have no power yet and are essentially at ground. This will create an overvoltage situation and likely force excessive current through the input of the op amp to ground (the unpowered supply pins).

Clamping: a Classic Overvoltage Protection Technique

A very popular way to add OVP is shown in Figure 1. When the amplitude of the input signal (V_{IN}) exceeds one of the supply voltages plus the forward voltage of a diode, the diode (D_{OVPP} or D_{OVPN}) will forward bias and send the current to the supply rails rather than into the op amp inputs where the excess current could damage the op amp. In this application, we are using an [ADA4077](#), an extremely high precision op amp with a maximum power supply range of 30 V (or ± 15 V).

The clamping diodes are 1N5177 Schottky diodes because they have a forward voltage of approximately 0.4 V, which is less than the forward voltage of the of the op amp's input electrostatic discharge (ESD) protection diodes; thus, the clamping diodes will start conducting current before the ESD diodes do. The overvoltage protection resistor, R_{OVP} , limits the forward current through the clamping diodes to keep them under their maximum current rating, preventing them from being damaged by excessive current. The resistor R_{FB} in the feedback loop is there because any input bias current on the noninverting input can cause an input voltage error across R_{OVP} —adding R_{FB} will null out the error by generating a similar voltage on the inverting input.



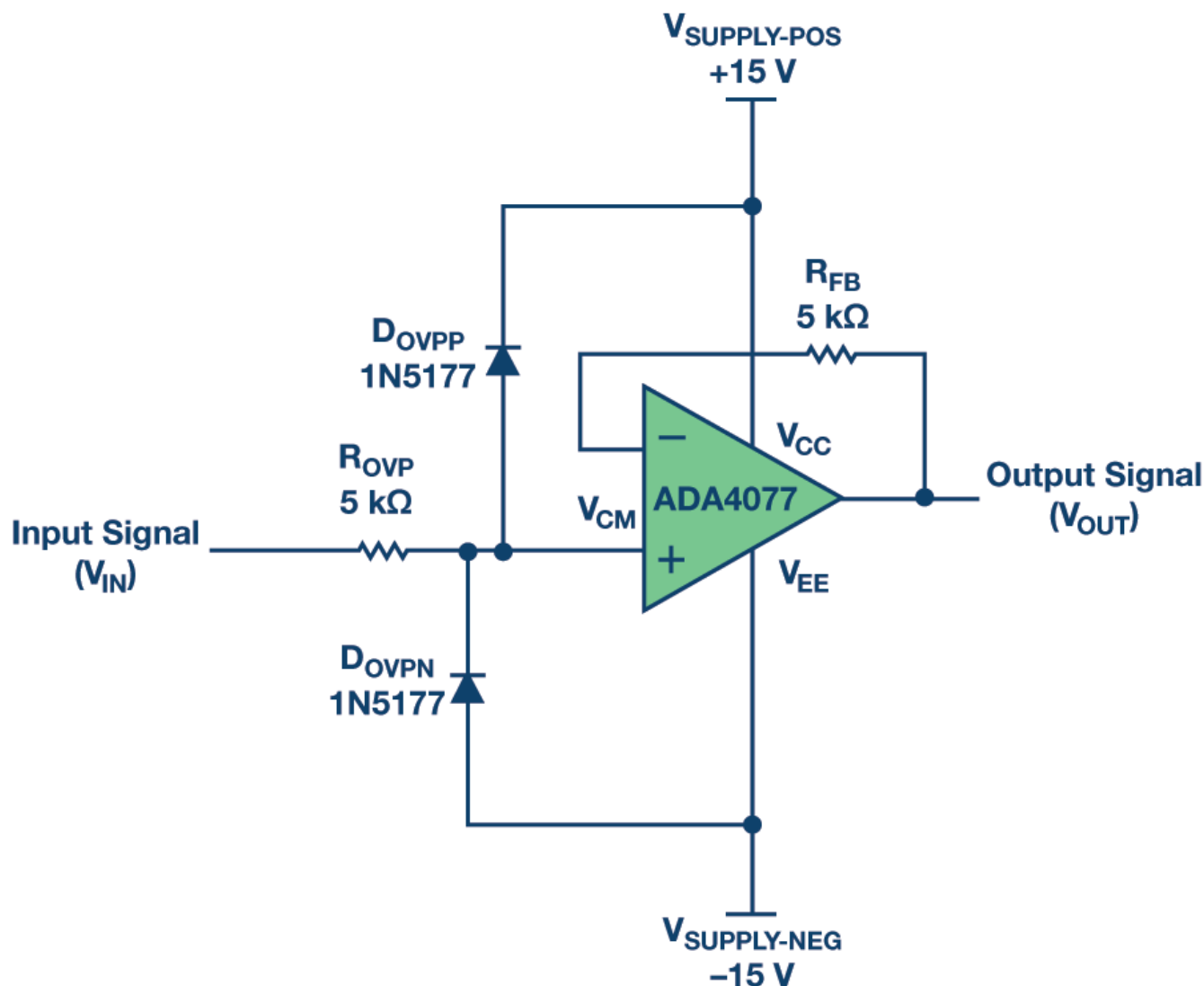


Figure 1. Classic clamping circuit for overvoltage protection.

The Trade-Off of a Diode Clamping Circuit—Reduced Precision

Although the classic circuit in Figure 1 protects the op amp inputs, it contributes a significant amount of error to the signal path. Precision amps generally have input offset voltages (V_{OS}) in the microvolts range. For example, the maximum V_{OS} for an ADA4077 is 35 μ V over the full operating temperature range of -40°C to $+125^{\circ}\text{C}$. Adding the external diodes and an overvoltage resistor contributes an input offset error that can be many times greater than the low offset inherent to the precision op amp.

Reverse-biased diodes exhibit a reverse leakage current that flows from the cathode through the anode to the supply. When the input signal voltage (V_{IN}) is between the supply rails, the diodes D_{OVPP} and D_{OVPN} have a reverse voltage on them. With V_{IN} at ground (the middle of the input voltage range), the reverse current through D_{OVPN} is approximately equal to the reverse leakage current through D_{OVPP} . However, when V_{CM} moves above or below ground, a larger reverse current flows through one diode than the other. For example, when V_{CM} is at the top of the op amp's input voltage range, which is 2 V from the positive supply or 13 V in this circuit, diode D_{OVPN} will have a reverse voltage of 28 V across it. According to the 1N5177 diode's data sheet, this can cause a reverse leakage current of close to 100 nA. As reverse leakage current flows from the

input signal (V_{IN}) through R_{OVP} , it will create a voltage drop across R_{OVP} that looks exactly like an increased input offset voltage to the signal path.

Of additional concern is that diode reverse leakage current increases exponentially with an increase in temperature, causing an increase in the offset voltage penalty of the clamping O_{VP} circuit. As a baseline of comparison for op amp precision with no external overvoltage circuitry, Figure 2 shows the measured offset voltage of the ADA4077 over an input voltage range from -13 V to $+13$ V. The measurements were performed at three temperatures: 25°C , 85°C , and 125°C . Note that at 25°C , the V_{OS} of the ADA4077 used in this test reached only $6\text{ }\mu\text{V}$; even at 125°C , the V_{OS} is only approximately $20\text{ }\mu\text{V}$. When we add the external clamping OVP circuit to the same ADA4077 device and apply the input at V_{IN} , we see the results shown in Figure 3. At room temperature, the V_{OS} jumps to $30\text{ }\mu\text{V}$ —five times the signal path error of the ADA4077 alone. At 125°C , V_{OS} goes to over 15 mV —an increase of 750 times the $20\text{ }\mu\text{V}$ of the ADA4077! Precision is gone.

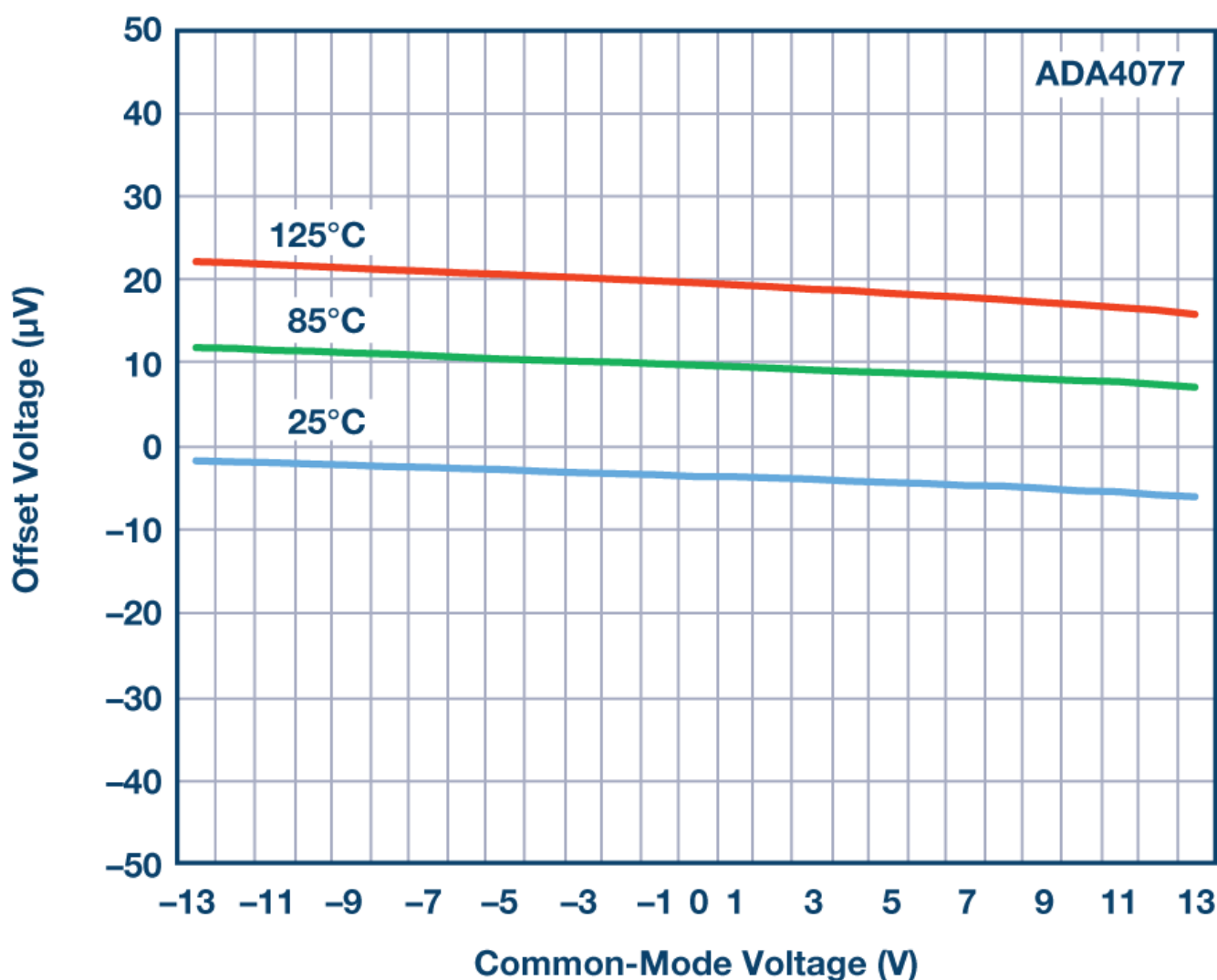


Figure 2. Input offset voltage vs. input voltage for ADA4077.

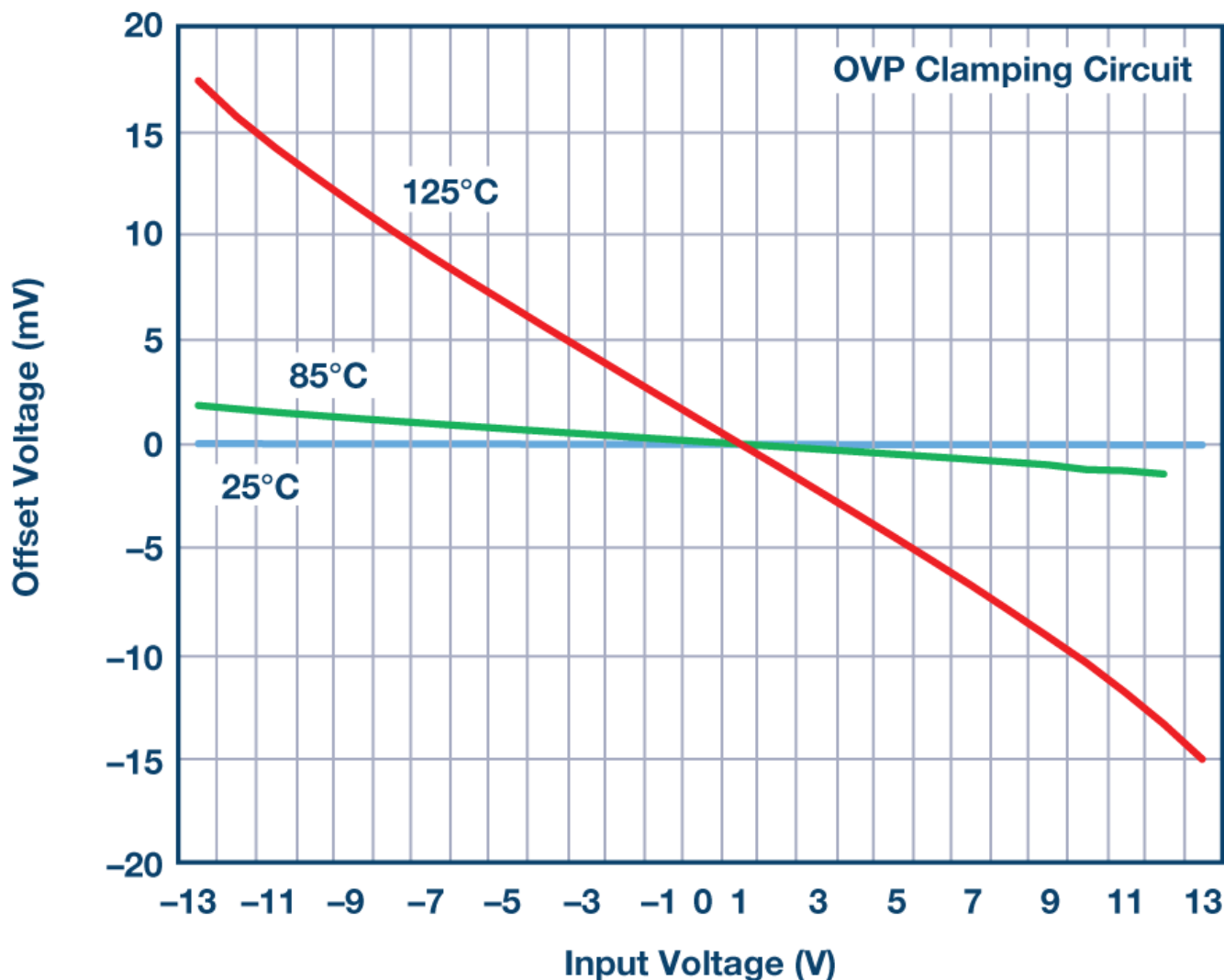


Figure 3. Input offset voltage vs. input voltage for an OVP clamping circuit added to ADA4077.

The 5 k Ω resistor does a great job protecting the clamping diodes as well as the op amp during an overvoltage condition but it adds quite a bit of offset error during normal operation when the diodes are leaking current across it (not to mention Johnson noise from the resistor). What we would like is a dynamic input resistance that has low resistance during operation within the specified input voltage range but high resistance during overvoltage conditions.

An Integrated Solution Provides the Answer

The [ADA4177](#) is a high precision op amp that includes integrated overvoltage protection. The integrated ESD diodes act as overvoltage clamps to protect the part. Depletion mode FETs are in series at each input before the ESD diodes. They provide the dynamic resistance, which increases when the input voltage (V_{CM}) exceeds the supply voltages. As input voltage increases, the drain-to-source resistance ($R_{DS(on)}$) of an internal FET increases, thus restricting the current flow exponentially with the increased voltage (shown in Figure 4). Because the ADA4177 uses depletion mode FETs on the inputs and not a series protection resistor, the op amp doesn't suffer the offset voltage penalty across the resistor that the clamping OVP circuit does.

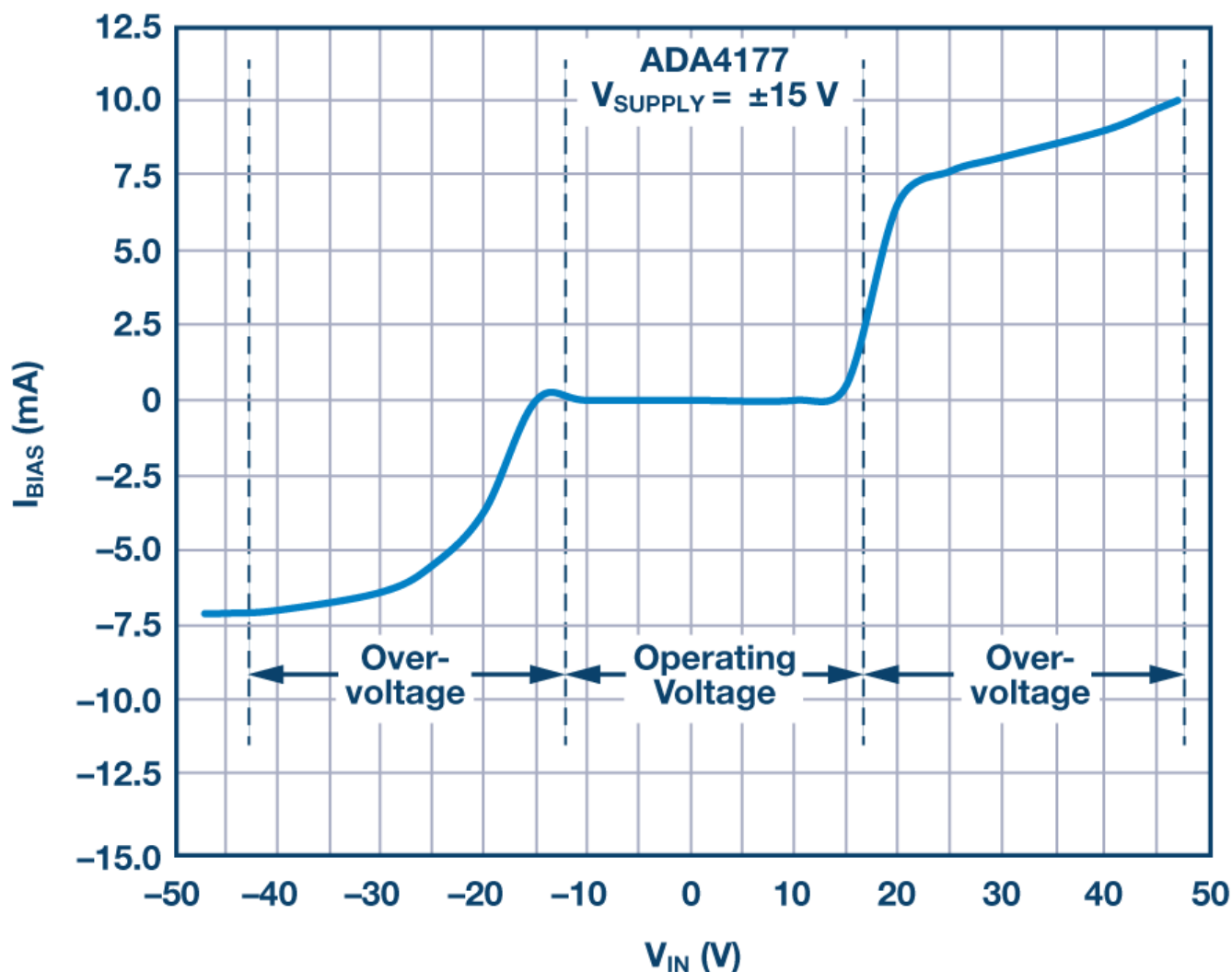


Figure 4. ADA4177 input bias current is restricted as overvoltage increases.

The ADA4177 can withstand voltages on its inputs of up to 32 V beyond the supply voltage. It limits overvoltage current to a typical 10 mA to 12 mA, protecting the op amp without the use of any external components. As shown in Figure 5, even at 125°C this tested unit is showing an offset voltage of only 40 μV . That's less than 3% of the error that the clamping circuit showed at that temperature. Precision is maintained!

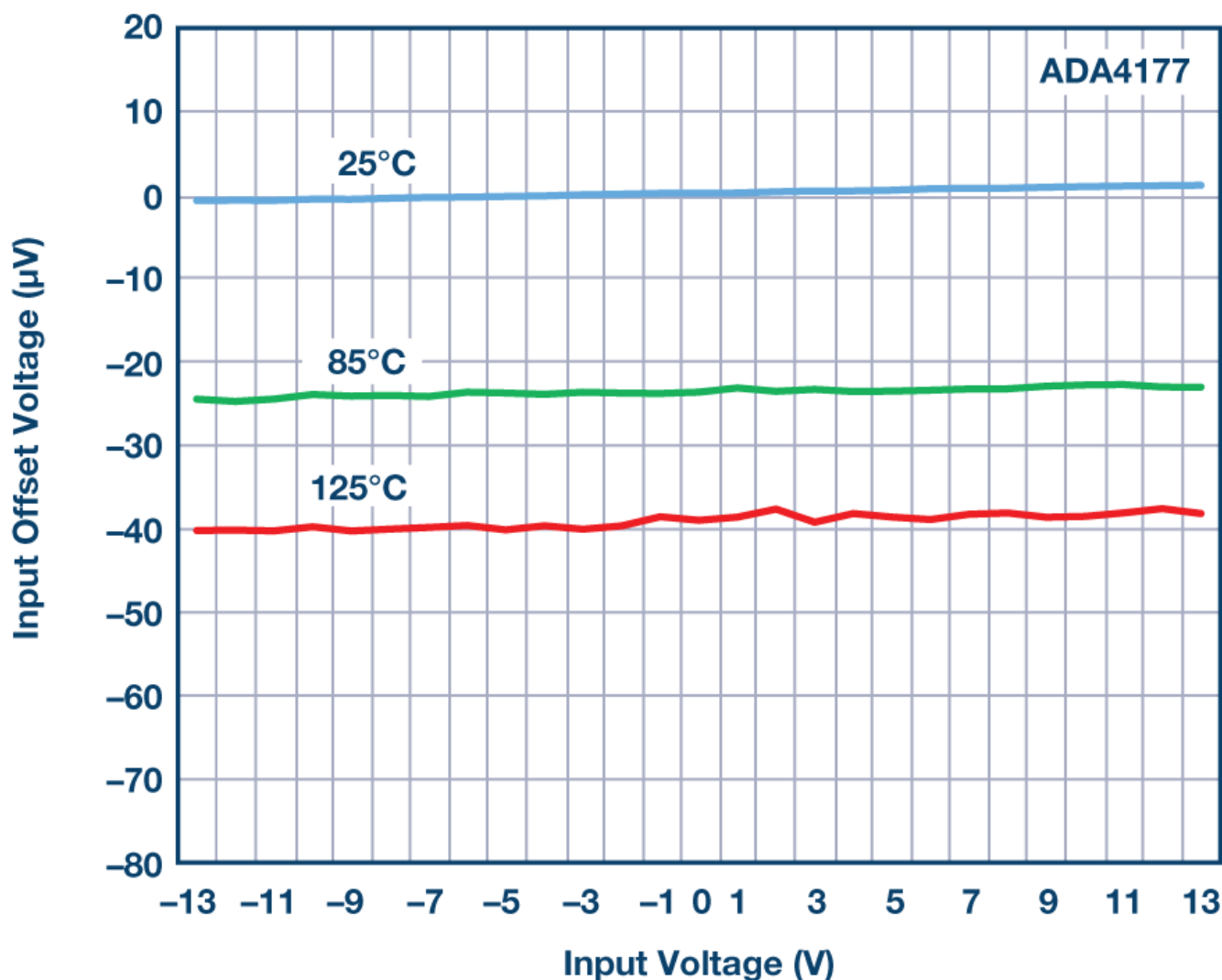


Figure 5. Input offset voltage vs. input voltage for ADA4177 with its integrated OVP.

What This Means to System Performance

When analyzing the effect of varying input voltage on the precision of the signal path, a system designer will consider the amplifier's common-mode rejection ratio (CMRR). This is a measure of how much of the common-mode input voltage is rejected from showing up on the output (or how little gets through). Since op amps are often configured to provide gain between the input and the output, we normalize the CMRR specification by referring to change in the input offset voltage, which is the change in output divided by the amplifier's closed-loop gain. The common-mode rejection ratio is a positive value expressed in dB and is calculated by the following formula:

$$\text{CMRR} = 20 \log (\Delta V_{\text{CM}} / \Delta V_{\text{OS}})$$

From this ratio, we see it is clearly desirable to keep the VOS as small as possible. The ADA4177 is specified to have a guaranteed minimum CMRR limit of 125 dB over full operating temperature. Using the test results from the units measured in this experiment, we can calculate and compare the CMRR of the clamping circuit and the ADA4177. Table 1 shows the extreme loss of precision when using the classic clamping diode circuit and the excellent CMRR of the ADA4177 with its integrated FET overvoltage protection.

Table 1. CMRR Comparison of ADA4177 to Discrete OVP with Clamping Diodes

Overvoltage Protection Method	25°C	85°C	125°C
ADA4177	143 dB	145 dB	142 dB
ADA4077 and Clamping OVP	113 dB	78 dB	58 dB

References

Arkin, Michael and Eric Modica. "[Robust Amplifiers Provide Integrated Overvoltage Protection.](#)" Analog Dialogue, Volume 46, Number 1, 2012.

Video: "[ADA4096-2 Input Overvoltage Protection Amplifier.](#)" Analog Devices, Inc.

Video: "[ADA4177: Op Amp with OVP and EMI Provides Robustness and Precision.](#)" Analog Devices, Inc.

For more information on the ADA4177 and ADA4077, see the product pages and data sheets here: [ADA4177](#) and [ADA4077](#).

Author



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Daniel Burton is an applications engineer at Analog Devices. He acquired his B.S.E.E. from San Jose State University and he has worked on sensing and precision linear signal paths for much of his career. Dan has been with Analog

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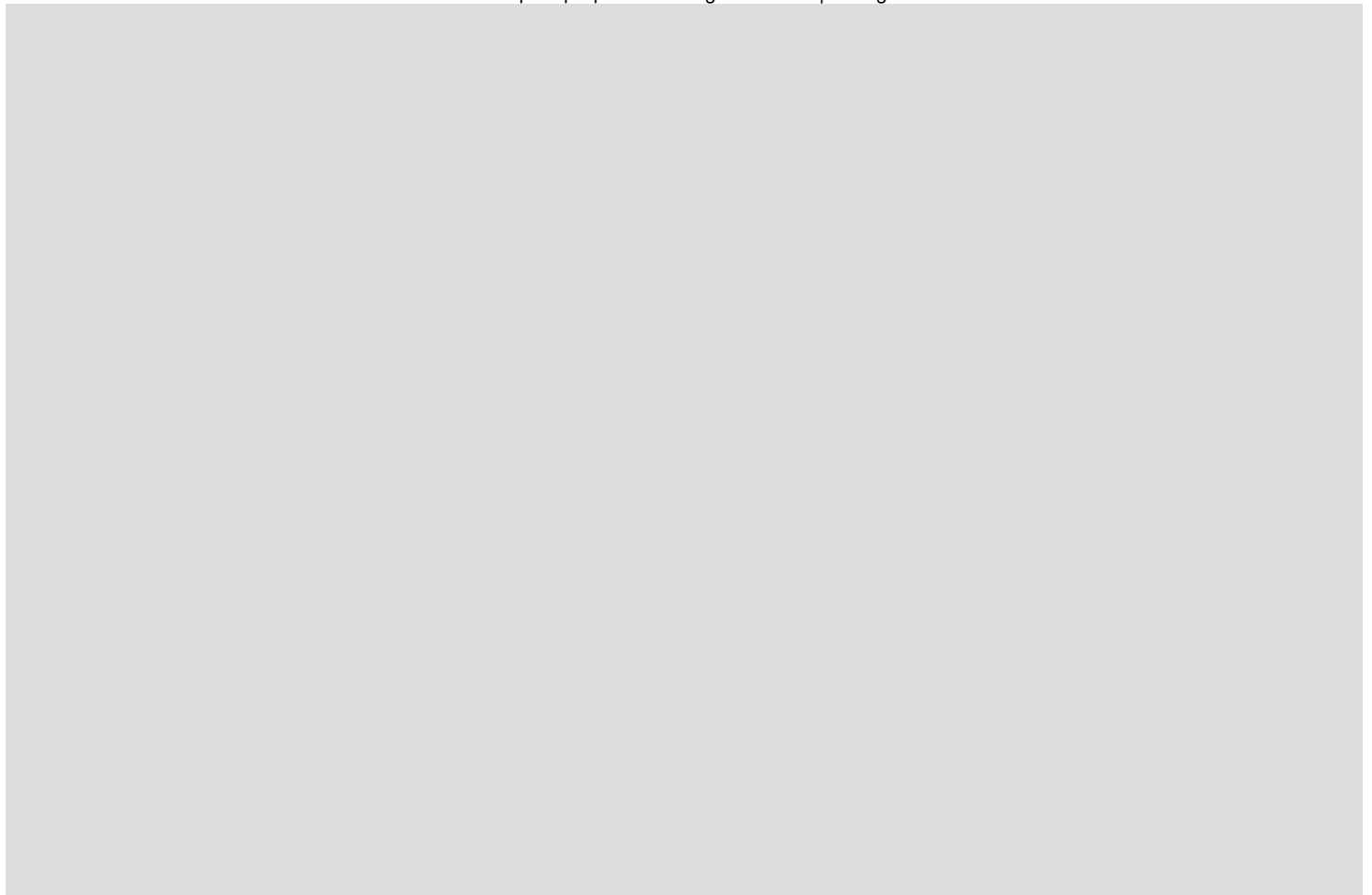
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