# Analysis and Design of Weighted Voltage-Mode Control

# for a Multiple-Output Forward Converter

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*Abstract* - A power stage model of a multiple-output forward converter with weighted voltage-mode control is derived incorporating all the major parasitics. The model is employed to identify the feasible region of the weighting factors to meet given dc regulation specifications. A design procedure that determines the optimal selection of the weighting factors is also proposed. Finally, the dc model and the design procedure are verified on an experimental two-output forward converter.

## I. INTRODUCTION

Voltage regulation of a multiple-output dc-dc converter is typically done with only one control variable, the duty cycle $d$. From the control point of view, duty cycle alone cannot accurately control several independent outputs. Therefore there always exists a dc regulation error in one or several of the outputs.

The most commonly used regulation method is to sense one output and leave the other outputs unattended. The sensed output is accurately controlled while the unsensed outputs are cross regulated. The cross-regulation range depends on the load conditions and the power stage parameters. Several papers discussing various issues of the cross-regulation were published in the past [1] - [4].

Another method of regulating a multiple-output converter is to sense two or more outputs simultaneously and feed back the sum of the weighted outputs as illustrated in Fig. 1. This is herein referred to as *weighted voltage-mode control*. Because the feedback signal is derived from several outputs, none of them can be precisely regulated . Compared to the conventional method, the weighted control redistributes the error among the outputs, and the regulation error can be adjusted by varying the weighting factors.

Although the weighted voltage-mode control has been used on many occasions, there is no systematic analysis and design procedure for this control. Most designs are performed on the trial and error basis, and the results were rather inconsistent. The purpose of this study is to develop an analytical model, and based upon that provide design insight for multiple-output forward converters employing the weighted voltage-mode control. Specifically, the paper
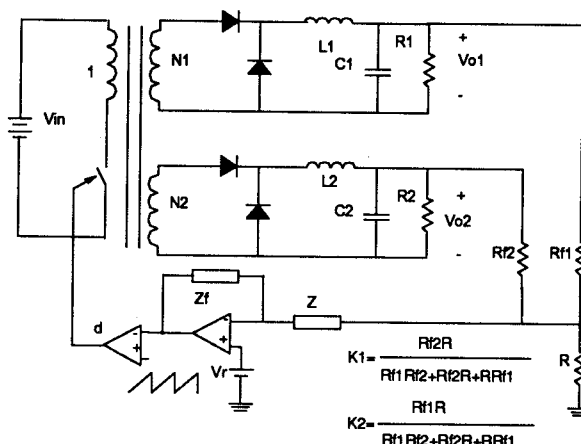
Fig.1 A dual-output forward converter with weighted voltage-mode control. The transformer reset circuitry is not shown here.

focuses on the determination of the weighting factors to meet the desired dc regulation specifications. The stability analysis and the control-loop compensator design to meet dynamic requirements are beyond the scope of this paper. The latter issue will be addressed in a follow-up paper which is being prepared.

First a power stage model including the effects of all the major parasitics is derived, revealing the critical parameters which affect the dc regulation. Then the closed-loop dc regulation is calculated. From the design specifications, the feasible range of the weighting factors $\{K_i\}$ is identified. Finally a forward converter is used to demonstrate how to apply the proposed design procedure to solve a practical design problem.

It should be noted that although only the analysis and design of a dual-output forward converter are presented in the paper, the same approach can be easily extended to virtually any converter topology with an arbitrary number of outputs.

## II. DC MODEL OF POWER STAGE

Generally, the tightness of cross-regulation is dependent on a number of the circuit parasitics. The major parasitics

are the winding resistances of the transformer and the output filter inductors, the leakage inductances of the transformer, and the forward voltage drop of the diodes. In this section, the effects of the major parasitics on dc output voltages are derived.

## 2.1 Modeling of Major Components

The output circuit (drain-to-source) of a MOSFET switch is modeled as an ideal switch in series with a resistor whose value is equal to the on-resistance $R_{ds}$ of the MOSFET. The parasitic output capacitance of the MOSFET is modeled by a capacitor $C_{ds}$ placed in parallel with the ideal switch and the resistor, as shown in Fig. 2.

The diode can be modeled as an ideal diode in series with a voltage source and a resistor, Fig. 2, i.e.,

$$V_D = V_d + I_D R_d \qquad (1)$$

where $V_d$ is the threshold voltage and $R_d$ is the on-resistance of the diode.

Since the output filter inductor essentially carries a dc current, it can be modeled as an ideal inductor in series with a dc resistor.

The transformer is modeled as an ideal transformer plus its parasitics. Each winding resistance includes both ac and dc resistance. By using the structure where the transformer primary winding is sandwitched between the secondary windings, the leakage inductance can be lumped on the secondary sides and the magnetizing inductance is located on the primary.

## 2.2 Simplified Power Stage

Replacing each component with the corresponding model, a simplified power stage model is obtained, Fig. 2.

When the switch is on, the current flowing through the active switch and the primary winding consists of two parts: reflected load currents and the magnetizing current. For a properly designed transformer, the magnetizing current is small compared with the reflected load currents, so it can be

assumed zero. As a result, the voltage across the primary winding is the line voltage $V_{in}$ reduced by the voltage drops across the primary winding resistance, and the channel resistance of the switch. Since the primary carries a pulsating current, the calculation of the voltage drop across the winding resistance should take into account of both dc and ac resistance. The value of the primary voltage is

$$V_p = V_{in} - I_p R_{on} - D I_p R_{pdc} - \sum_i I_{pac}^i R_{pac}^i \qquad (2)$$

where

$V_{in}$ - line voltage,
$R_{pdc}$ - dc resistance of the primary winding,
$R_{pac}^i$ - i-th harmonic of ac resistance of the primary winding,
$R_{on}$ - on-resistance of the switch,
$I_p$ - magnitude of the current in the primary,
$\qquad I_p = N_1 I_{o1} + N_2 I_{o2}$,
$I_{pac}^i$ - i-th harmonic of the primary current.

As the switch turns off, the reversal of the transformer voltage takes a finite time $\Delta t_p$ in order to charge the parasitic capacitance $C_{ds}$ and any other capacitance connected to the drain of the MOSFET (e.g., the capacitance of the transformer and the reset circuitry, etc.) As a result, the voltage across the primary winding of the transformer does not drop to zero till $t_2$, Fig. 3. This charging process causes the effective duty ycle extension $\Delta D_p$. Generally, the rigorous calculation of the duty cycle extension is extremely involving. However, the analysis can be simplified by assuming a large magnetizing inductance of the transformer so that the primary current can be modeled as a constant current source with the value equal to the sum of the reflected output currents. In this case, the time needed to charge the parasitic capacitances is

$$\Delta t_p = t_2 - t_1 = \frac{C_t V_{in} + 10 C_o \sqrt{V_{in}}}{I_p}, \qquad (3)$$

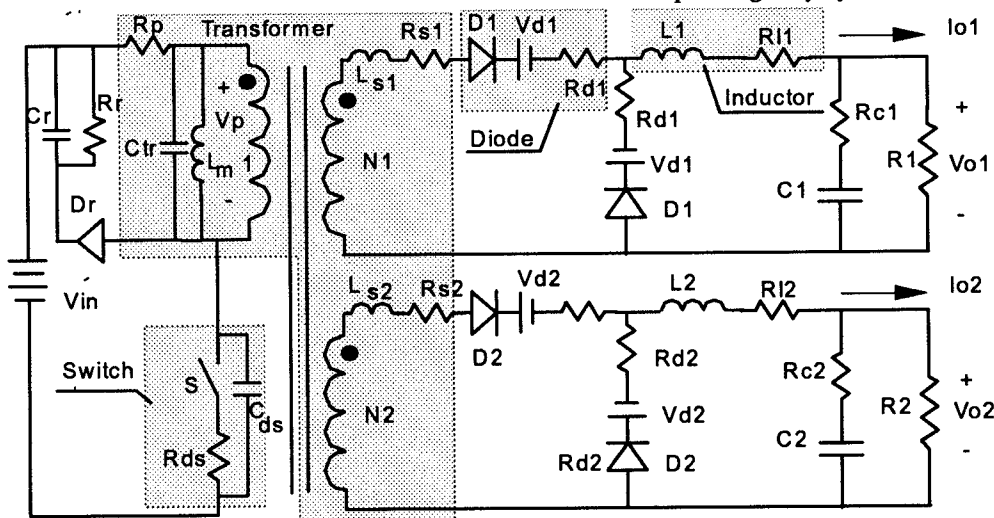and the corresponding duty cycle extension can be calculated



Fig. 2 The simplified power stage model.

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based on the equivalent volt-second product, Fig. 3(b),

$$\Delta D_p = \frac{\Delta t_p}{2T} = \frac{C_t V_{in} + 10 C_o \sqrt{V_{in}}}{2 I_p} f_s. \qquad (4)$$

where

$C_t$ - total capacitance of the transformer and the reset circuitry,

$C_o$ - junction capacitance of the MOSFET when $V_{ds}=25$ V,

$f_s$ - switching frequency.

The voltages across the transformer windings (both primary and secondary sides) have an effective duty cycle

$$D_e = D + \Delta D_p \qquad (5)$$

The reset voltage can also be represented by a square wave obtained from volt-second product, Fig. 3.



(a) The primary waveforms.

(b) Magnification of Vprim waveform during time interval t1-t2.
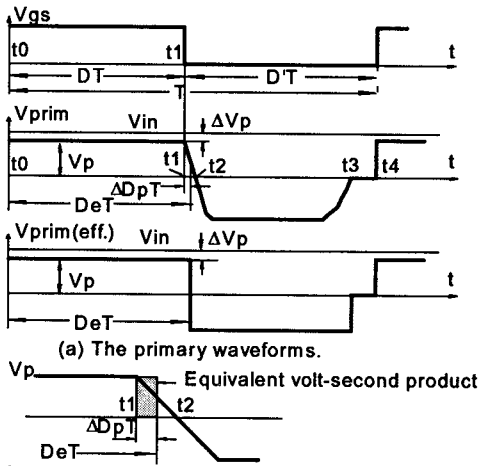
Fig. 3 The primary voltages in one switching period.

The secondary of the transformer can be modeled by a voltage source with the magnitude equal to the reflected primary voltage, or $V_s=NV_p$, and the effective duty cycle $D_e$. To simplify analysis, the current through the output filter inductor is assumed constant equal to the load current. Because the load current goes through either diode $D_A$ or diode $D_B$, and the diodes $D_A$ and $D_B$ are usually of the same type, the voltage source and the resistor of the diodes $D_A$ and $D_B$ can be shifted to the branch in series with the output filter. Figure 4 shows the simplified secondary circuit diagram and waveforms in one complete switching cycle.

When the active switch in the primary is turned on at $t=t_o$, voltage is induced immediately on the secondary windings. During time interval $t_o$ - $t_1$, $D_B$ is till contucting and the current commutating from $D_B$ to $D_A$, Fig. 4(1). As long as $D_B$ is conducting, the voltage at node J, $V_J$, is equal to zero. During t1- t2, $D_B$ is cut off and $D_A$ carries all the load current, Fig. 4(2). During t2 - t3, the switch is turned off, and the voltage $V_J$ becomes zero again since the load current is commutating from $D_A$ to $D_B$, Fig. 4(3). During t3 -t4, only $D_B$ is conducting, and $V_J$ is zero, Fig. 4(4). $V_J$ is a

square wave with a duty cycle loss caused by the leakage inductance. The duty-cycle loss at node J is

$$\Delta D_s = \frac{L_s}{V_s} f_s I_o, \qquad (6)$$

where

$V_s$ - secondary voltage,

$L_s$ - leakage inductance,

$I_o$ - load current.

The voltage drop caused by the secondary winding resistance is given by:

$$\Delta V_{scu} = D_e I_o R_{sdc} + \sum_i I^i_{sac} R^i_{sac}, \qquad (7)$$

where

$R_{sdc}$ - dc resistance of the secondary winding,

$R^i_{ac}$ - i-th harmonic of the ac resistance of the secondary winding,

$I_o$ - magnitude of the load current,

$I^i_{ac}$ - i-th harmonic of the secondary current.



(1) t0 - t1, S on, DA satrting on but DB not cut off yet, iL=iA+iB

(2) t1 - t2, S still on, DB cut off, iL=iA

(3) t2 - t3, S off, DA still on due to Ls, DB starting on, iL=iA+iB
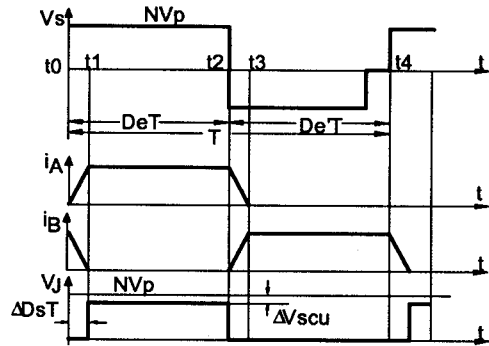
(4) t3 - t4, S still off, DA cut off, DB on, iL=iA

Fig. 4 The secondary circuit diagram in one complete duty cycle.

The total voltage drop across the diodes equals

$$V_D = V_d + I_o R_d. \tag{8}$$

The output voltage $V_o$ can be calculated by averaging $V_J$, which is a square wave with the magnitude equal to the secondary voltage minus the voltage drop across the secondary winding and the duty cycle $D_e$-$\Delta D_s$, over a switching period:

$$V_o = (D_e - \Delta D_s)(V_s - \Delta D_{scu}) - V_D - I_o R_L. \tag{9}$$

By neglecting the second order term, the output voltage in Eq. (9) can be written as:

$$V_o = D_e V_A - V_B. \tag{10}$$

where

$$V_A = V_s - \Delta V_{scu} = N V_p - \Delta V_{scu}. \tag{11}$$

$$V_B = V_d + I_o(f_s L_s + R_d + R_L) = V_d + I_o Z_B. \tag{12}$$

where

$$Z_B = f_s L_s + R_d + R_L. \tag{13}$$

$V_A$ quantifies the effect of input voltage, the transformer turns ratio, winding resistance, and the on-resistance of the active switch. $V_B$ describes the voltage variation induced by the leakage inductance of the transformer, the rectifier diodes, and the resistance of the output filter inductor. As can be seen from Fig. 5, the output voltage level depends on $V_A$ and the voltage variation range on $V_B$. These two quantities, therefore, provide useful information for design. Improper centering can be improved by adjusting $V_A$ whereas large voltage variation can be improved by refining the term $V_B$.

The quality of cross-regulation is decided by the combined effect of the forward voltage drop of the rectifier diodes, the inductor winding resistors, and the leakage inductances. To improve the cross regulation, it is important to decrease the total value of the internal impedance, rather than the value of the individual parasitic parameter.
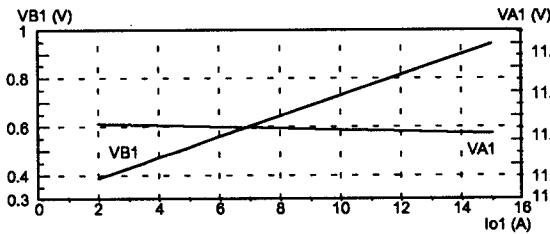


Fig. 5 Dependency of $V_A$ and $V_B$ on load $I_{o1}$.

## III. SELECTION OF WEIGHTING FACTORS

For a multiple-output dc-dc converter with weighted voltage-mode control, each output is not only related to the circuit parameters, but also to the weighting factors, $\{K_i\}$. In this section the relationship between the output voltages and the weighting factors for a dual-output converter, as shown in Fig. 1, is derived. The similar procedure can be applied to the converters with more than two outputs.

As derived in Sec. 2, the output voltages can be expressed as:

$$V_{o1} = D_e V_{A1} - V_{B1}. \tag{14}$$

and

$$V_{o2} = D_e V_{A2} - V_{B2}. \tag{15}$$

where $\{V_{Ai}\}$ and $\{V_{Bi}\}$ are defined in Eqs. (11) and (12) for output 1 and output 2 respectively.

In the steady state, the feedback renders the sum of the weighted output voltages equal to the reference voltage, Fig. 6, i.e.,

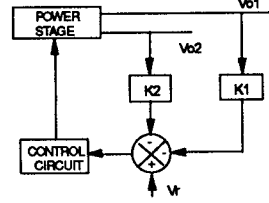$$V_r = K_1(D_e V_{A1} - V_{B1}) + K_2(D_e V_{A2} - V_{B2}). \tag{16}$$



Fig. 6 Control block diagram.

Solving Eq. (16) for $D_e$

$$D_e = \frac{V_r + K_1 V_{B1} + K_2 V_{B2}}{K_1 V_{A1} + K_2 V_{A2}}, \tag{17}$$

and substituting $D_e$ into Eqs. (14) and (15) yields the closed-loop output voltages:

$$V_{o1} = \frac{V_r + K_1 V_{B1} + K_2 V_{B2}}{K_1 V_{A1} + K_2 V_{A2}} V_{A1} - V_{B1}, \tag{18}$$

and

$$V_{o2} = \frac{V_r + K_1 V_{B1} + K_2 V_{B2}}{K_1 V_{A1} + K_2 V_{A2}} V_{A2} - V_{B2}. \tag{19}$$

For a given power stage (given $L_s$, $R_L$, $V_d$, $R_d$ etc.) the output voltages calculated from Eqs. (18) and (19) are only functions of input voltage, load currents and weighting factors, i.e.,

$$V_{oi} = f(I_{o1}, I_{o2}, V_{in}, K_1, K_2). \tag{20}$$

The output voltages reach their extremes at low line when one output is at the full load and the other at light load, i.e.,

$$V_{o1}^{max} = f_1(I_{o1}^{min}, I_{o2}^{max}, V_{in}^{min}, K_1, K_2), \tag{21}$$

$$V_{o2}^{min} = f_2(I_{o1}^{min}, I_{o2}^{max}, V_{in}^{min}, K_1, K_2), \tag{22}$$

$$V_{o1}^{min} = f_1(I_{o1}^{max}, I_{o2}^{min}, V_{in}^{min}, K_1, K_2), \tag{23}$$

$$V_{o2}^{max} = f_2(I_{o1}^{max}, I_{o2}^{min}, V_{in}^{min}, K_1, K_2). \tag{24}$$

The design objective is to keep the output voltages within the dc specifications for any load and line conditions,

$$V_{o1}^{min} \geq V_{o1(spec)}^{min}, \tag{25}$$

$$V_{o1}^{max} \leq V_{o1(spec)}^{max}, \tag{26}$$

$$V_{o2}^{min} \geq V_{o2(spec)}^{min}, \tag{27}$$

$$V_{o2}^{max} \leq V_{o2(spec)}^{max}. \tag{28}$$

Depending on the design specifications, Eqs. (25) - (28) define different regions of feasible values of $K_1$ and $K_2$. The following scenarios are discussed.

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1. Inequalities (25) - (28) specify a closed region in the first quadrant, Fig. 7(a).

2. Inequalities (25) - (28), with K1 and K2 axes together, specify a closed region in the first quadrant, Fig. 7(b). Usually, this is the case for loose regulation. It is observed that even if one weighting factor assumes the value of zero, the dc regulation specifications can still be met. Therefore, the cross-regulation through single feedback can be viewed as a special case of weighted voltage-mode control.

3. Inequalities (25) - (28) do not specify a common region in the first quadrant, Fig. 7(c). This situation implies that the design specifications are too tight for the given power stage parameters. Under this scenario, the design specifications must be relaxed, or else the power stage must be redesigned to accommodate the specifications.
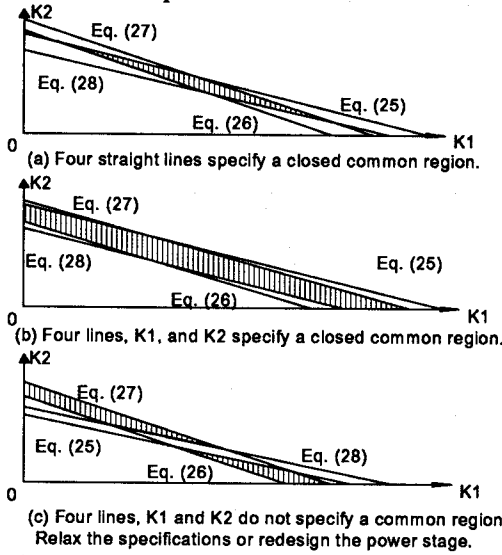


(a) Four straight lines specify a closed common region.

(b) Four lines, K1, and K2 specify a closed common region.

(c) Four lines, K1 and K2 do not specify a common region. Relax the specifications or redesign the power stage.

Fig. 7 The region of {Ki} specified by different design specifications.

Once the weighting factors {$K_i$} are selected, the parameters of the voltage divider network in Fig. 1 can be easily calculated. Assuming R has been chosen, then $R_{f1}$ and $R_{f2}$ are

$$R_{f1} = \frac{1 - (K_1 + K_2)}{K_1} R, \qquad (29)$$

$$R_{f2} = \frac{1 - (K_1 + K_2)}{K_2} R. \qquad (30)$$

## IV. DESIGN ILLUSTRATION

The design of a dual output dc-dc converter with weighted voltage-mode control is an iterative process which is shown in Fig. 8.

To verify the results of the described dc analysis and the proposed method of weighting factor selection, a dual-output forward converter was designed with following dc specifications:

- input line voltage $V_g$, 170 V - 270 V
- 5 V output: $4.8V \leq V_{o1} \leq 5.2V$, $2A \leq I_{o1} \leq 15A$
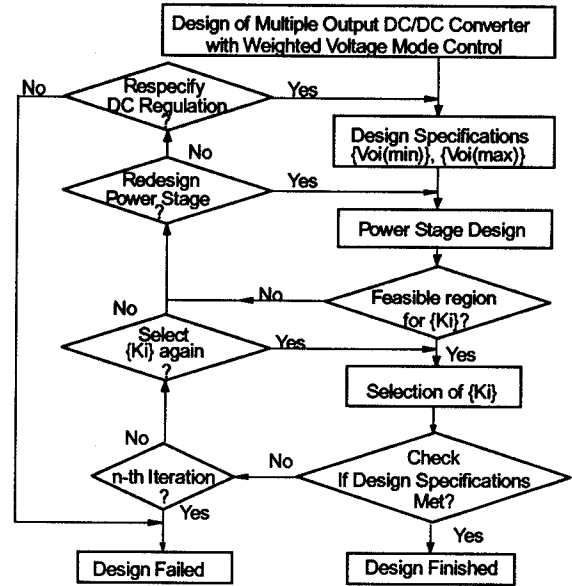


Fig. 8 The design procedure for a dual-output converter with weighted voltage-mode control.

- 12 V output: $11.5V \leq V_{o2} \leq 12.7V$, $0.5A \leq I_{o2} \leq 3A$

Following the well-established design procedure for the forward converter power stage [8], the experimental forward converter operating at 50 kHz was built with the following components:

- active switch, IRFP450,
- 5 V output rectifier diodes, IR60CNQ035,
- 12 V output rectifier diodes, IR8T100,
- power transformer,
  - core TDK PC40ER40,
  - primary winding, 45 turns AWG23 wire,
  - 5 V secondary, 3 turns 0.005x1" copper foil,
  - 12 V secondary, 7 turns 4xAWG23 wire.

The circuit parameters are listed in Table 1

By substituting the power stage parameters listed in Table 1 into Eqs. (25) - (28), the following inequalities are obtained:

$$54.22K_1 + 146.07K_2 \leq 28.41, \qquad (31)$$

Table 1 The list of the circuit parameters.

| $R_{ds}$ ($\Omega$) | 0.4 | $C_{ds}$ (pF) | 350 |
|---|---|---|---|
| $V_{d1}$ (V) | 0.301 | $R_{d1}$ ($\Omega$) | 0.012 |
| $V_{d2}$ (V) | 0.377 | $R_{d2}$ ($\Omega$) | 0.063 |
| $L_1$ ($\mu$H) | 154 | $R_{L1}$ ($\Omega$) | 0.028 |
| $L_2$ ($\mu$H) | 637 | $R_{L2}$ ($\Omega$) | 0.123 |
| $R_{odc}$ ($\Omega$) | 0.104 | $R^{(1)}_{Dac}$($\Omega$) | 0.268 |
| $R_{s1dc}$ ($\Omega$) | 0.0012 | $R^{(1)}_{s2ac}$ ($\Omega$) | 0.0057 |
| $R_{s2dc}$ ($\Omega$) | 0.0082 | $R^{(1)}_{s2ac}$ ($\Omega$) | 0.028 |
| $L_{s1}$ (nH) | 48.56 | $L_{s2}$ (nH) | 170.7 |

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$$58.87K_1 + 136.42K_2 \geq 28.47, \tag{32}$$

$$130.82K_1 + 303.08K_2 \leq 66.28, \tag{33}$$

$$123.95K_1 + 334.90K_2 \geq 66.32. \tag{34}$$

Plotting the boundary lines defined by Eqs. (31) - (34) in Fig. 9, it can be seen that they do not define a common region. This means that either the power stage is not properly designed or the design specifications are too tight. Assuming the design specifications are not allowed to be relaxed, then the only way to find feasible weighting factors $\{K_i\}$ is to redesign the power stage.
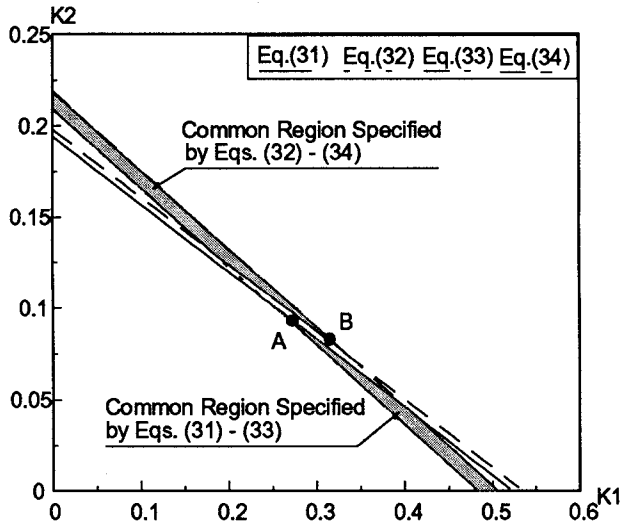
Fig. 9 Four inequalities do not specify a common region in the primary design.

Typically, the improper design of the power stage results from two aspects: (1) the secondary sides are not appropriately centered; (2) the internal impedance $Z_B$ is too large. It is important to pinpoint the cause before starting to redesign the power stage,

In Fig. 9, Eqs. (31) - (33) define a common region for $\{K_i\}$ which make the 5 V output meet the design specifications Similarly, Eqs. (32) - (34) define another region for $\{K_i\}$ which make the 12 V output meet the design specifications. Assume the 5 V output is more tightly regulated and its design is not going to be changed. Choose a set of $\{K_i\}$ such that the 5 V output just meets the regulation requirement while the 12 V output has the minimum regulation error. The cross section of Eqs. (31) and (32), which is point A as shown in Fig. 9, defines such $\{K_i\}$, where $K_1=0.288$ and $K_2=0.0872$. Using this set of $\{K_i\}$, the calculated $V_{o1}$ just falls into the design specification whereas the calculated $V_{o2}$ falls outside the design specification. Figure 10 shows the range of the output voltages variation. One can easily identify if improper centering or large internal impedance causes unsatisfactory dc regulation. For this specific design, it is obvious what the problem is -- voltage centering. The

difference between the maximum and minimum output voltages are within the specified values. The 12 V output
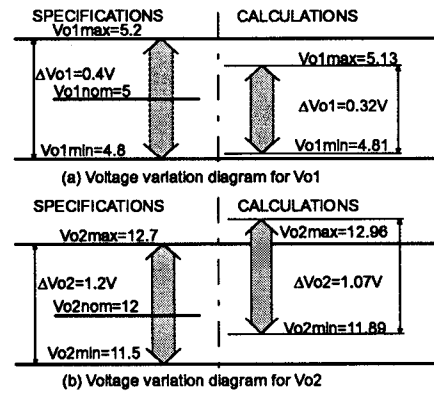
Fig. 10 Voltage variation diagram.

voltage, however, is off the center. Therefore, the voltage for 12 V secondary needs to be down shifted.

There are several possible ways to center the secondary voltages. In this work, an autotransformer with a turns ratio of 40/41 is inserted between the secondary winding and the rectifiers in 12 V output, Fig. 11, thereby changing the effective turns ratio of 12 V output from 0.156 to 0.152. Applying Eqs. (25) - (28) again, after this modification, another set of inequalities is obtained:

$$54.22K_1 + 142.34K_2 \leq 28.41, \tag{35}$$

$$58.67K_1 + 136.37K_2 \geq 28.47, \tag{36}$$

$$131.07K_1 + 295.70K_2 \leq 64.67, \tag{37}$$
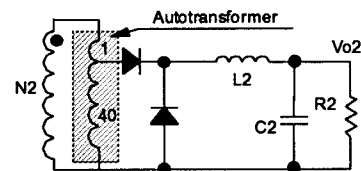
$$124.56K_1 + 326.73K_2 \geq 64.7. \tag{38}$$

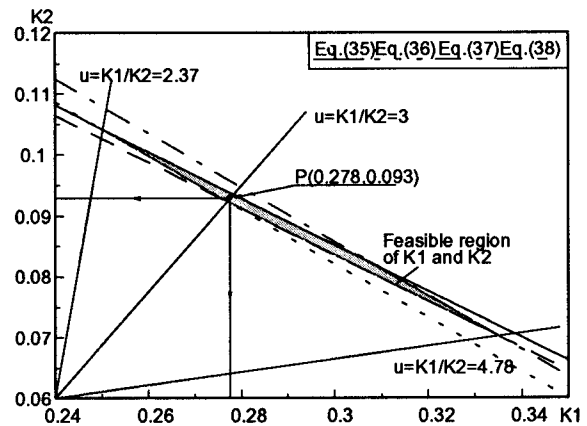Fig. 11. An autotransformer is employed in second output.

Fig. 12. Four inequalities define a common region after an autotransformer is employed.

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These four inequalities do specify a common region in the first quadrant, as shown in Fig. 12.

The shadowed area in Fig. 12 defines the feasible region for the weighting factors $\{K_i\}$. Two straight lines through the origin and two ends of the shadowed area specify the allowed ratio of $K_1/K_2$, which varies from 2.37 to 4.78 for this design. To meet the regulation specifications, the ratio of $K_1/K_2$ should fall into this range. At point P, which gives $K_1=0.278$ and $K_2=0.093$, the ratio of $K_1/K_2=3$. If R is chosen as 1 k$\Omega$, the feedback network is calculated as $R_{f1}=1.156$ k$\Omega$ and $R_{f2}=3.468$ k$\Omega$. With these values each output should meet its required regulation. Fig. 13 shows the measured and calculated output voltages.
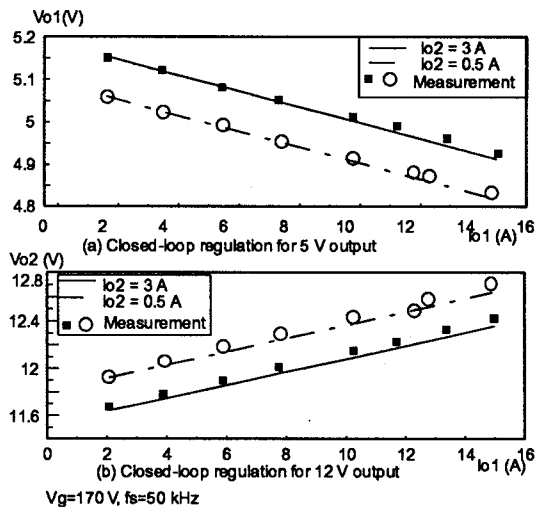


Fig. 13 The closed-loop output voltages $V_{o1}$ and $V_{o2}$.

Although the choice of $\{K_i\}$ can be any values as long as they fall into the shadowed area in Fig. 11, it is preferred to choose $\{K_i\}$ in the middle of the area to provide certain design margin. If the $\{K_i\}$ are chosen near the edges of the area, the output voltages may be easily out of the specifications because there are always some unmodeled factors, or the component values may deviate from the nominal ones somehow.

## V. CONCLUSIONS

A dc model incorporaing all major parasitics is derived for a forward dc-dc converter with multiple outputs. The model reveals that dc regulation is dependent, to a large extent, on the internal impedance which is the sum of the equivalent resistance of the rectifier diodes, the winding resistance of the output filter inductor, and the product of the leakage inductance and the switching frequency in each output. In addition, the winding resistors of the transformer, the parasitic output capacitance and the on-resistance of the active switch also affect the dc output voltage. The parasitics affect the output voltages in different ways: the resistors cause internal voltage drops while the parasitic capacitance

and the leakage inductance cause some modification of the effective duty cycle on the secondary side of the transformer. To improve the dc regulation, it is important to decrease the internal impedance for each output.

The cross-regulation is the result of the interaction between the outputs. Unsatisfactory dc regulation often is a result of improper centering, which makes the output voltages off the center, or large internal impedance, which causes the output voltages varying over a wide range.

The closed-loop output voltages are decided by the weighting factors in addition to the power stage parameters. By applying the dc regulation specifications, a set of inequalities is obtained, which specify the region for $\{K_i\}$. For some cases, it is possible to find a set $\{K_i\}$ to achieve desired dc regulation for all outputs. For other cases, the required regulation may not be met by simply choosing $\{K_i\}$. Either relaxation of the design specifications or redesign of the power stage may have to be invoked.

A design procedure for weighting factors is established. An off-line forward dc-dc converter is used as an example to demonstrate how to use the proposed design procedure. A good agreement is achieved between the measured output voltages and the predicted values.

## VI. REFERENCES

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