ACTIVE POWER DECOUPLING FOR A BOOST POWER FACTOR CORRECTION CIRCUIT

by

David Williams

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The undersigned certify that they have read, and recommend to the College of Graduate Studies for acceptance, a thesis entitled:

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submitted by David Williams in partial fulfilment of the requirements

of the degree of Master of Applied Science.

Dr. Wilson Eberle Faculty of Applied Science/School of Engineering

Supervisor, Professor (please print name and faculty/school above the line)

Dr. Thomas Johnson Faculty of Applied Science/School of Engineering

Supervisory Committee Member, Professor (please print name and faculty/school in the line above)

Dr. Liwei Wang Faculty of Applied Science/School of Engineering

Supervisory Committee Member, Professor (please print name and faculty/school in the line above)

Dr. Zheng Liu Faculty of Applied Science/School of Engineering

University Examiner, Professor (please print name and faculty/school in the line above)

External Examiner, Professor (please print name and university in the line above)

September 2016

(Date Submitted to Grad Studies)

Additional Committee Members include:

(please print name and faculty/school in the line above)

(please print name and faculty/school in the line above)

Abstract

During AC-DC conversion, the ripple power at the input of the converter must be filtered from the output. This filtering can be easily done by placing a capacitor on the DC bus. For systems with power output of hundreds of Watts or more, this capacitor must be quite high to effectively perform the filtering, and in order to be cost effective, an aluminum electrolytic capacitor (Al e-caps) needs to be used. The lifespan of Al e-caps is notoriously short, so for long lifespan systems, their use is not advisable.

Film capacitors have longer lifespans than Al e-caps but are more expensive on a cost per Farad basis. Methods have been proposed to reduce the required capacitance so that film capacitors can be cost effectively used. One of these methods is to use a separate decoupling port in the circuit that can filter the ripple power without the limitation of being connected directly to the DC bus. The first contribution is a method of using an active power decoupling (APD) port with a buck-based circuit that does not require direct measurement of the AC input signal for controlling the ripple power to the port. This APD port requires only two extra switches and some simple signal processing circuitry to generate a reference signal and control the voltage to the APD port capacitor.

The second contribution is a design guide for a sliding mode control (SMC) system for the APD port. SMC shows promise as a control system for power electronics circuits and has never been demonstrated on an APD port before.

The proposed circuit and control system is used in a 700 Watt AC-DC converter with power factor correction and is compared in simulation to a benchmark converter using a passive capacitor on the DC bus. The capacitance is reduced from $300\mu F$ to a $35\mu F$ and a $75\mu F$ capacitor without any effect on performance as indicated by measures of the voltage ripple,

power factor and total harmonic distortion. The capacitance reduction results in a cost savings of $175 on capacitors when using prices that were current at time of publication.

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List of Symbols

C	Capacitor
C_r	Ripple (APD) port capacitor
d	Duty cycle
D	Diode
DF	Dissipation factor of capacitor
f_{line}	Line frequency in Hertz
f_{sw}	Switching frequency
$H_R(s)$	Transfer function for resonant compensator
i_{ac}	AC line current
I_{ac_scaled}	A scaled version of the AC line current (for better visualization on graph)
i_c/i_{rc}	Current to ripple (APD) port
i_L	Inductor current
I_{LD}	DC Load Current
I_r	Peak ripple current
I_p	Peak AC current
K_{p1}	Current gain for SMC
K_{p2}	Voltage error gain for SMC
Kr	Gain of resonant compensator transfer function
L	Inductor
L_{ac}	AC portion of coupled inductor
LC	Inductor-capacitor circuit

L_{dc}	DC portion of coupled inductor
L_r	Inductor in ripple (APD) port
$Life$	Life expectancy of device
$Life_b$	Base life expectancy of device at rated temperature and voltage
M_v	Voltage derating multiplier for calculating life expectancy of device
N_{ac}	Turns on AC portion of coupled inductor
N_{dc}	Turns on DC portion of coupled inductor
p_{ac}	Power AC side
P_o	Output power
PO	Percent overshoot
P_r/P_{ripple}	Ripple power
Q	Quality factor of filter
S	Sliding mode state variable trajectory
R_{ESR}	Equivalent series resistance
t	Time
$T_{s(1\%)}$	One percent settling time
$tan(\delta)$	Dissipation factor of capacitor
T_c	Operating temperature used in life expectancy calculation
T_m	Rated temperature used in life expectancy calculation
u	Control variable for SMC (0 or 1)
u_{eq}	Control variable for SMC; equivalent to duty cycle
u_{eq}^*	Scaled control variable for SMC

V_a	Operating voltage used in life expectancy calculation
v_{ac}	AC line voltage
v_{acN}	Scaled AC neutral line voltage
v_{aux}	Auxiliary inductor winding voltage
v_c	Voltage across APD capacitor
V_C	Peak voltage across APD capacitor
V_{DC}	DC output voltage
v_i	Input voltage
V_{LD}	Load voltage
$V_r \ or \ \Delta V$	Ripple voltage
V_p	Peak AC Voltage
V_r	Rated voltage used in life expectancy calculation
v_{rc}	Voltage across APD capacitor
V_{RC}	Average voltage across APD capacitor
ΔV_{RC}	Ripple voltage across APD capacitor
V_{ref}	Reference voltage
v_L	Inductor voltage
V_o	Output voltage
W_c	Energy stored in capacitor
W_{min}	Minimum required energy stored in capacitor
δ	Defect angle of capacitor
ε	Permittivity of dielectric

θ	Phase shift between v_{ac} and v_{rc}
φ	Phase shift between v_{ac} and i_{ac}
λ	Failures in Time
ω_{line}	Line frequency (in rad/sec)
ω_o	Resonant Frequency (in rad/sec)

List of Abbreviations

AC	Alternating current
Al e-cap	Aluminum electrolytic capacitor
APD	Active Power Decoupling
BJT	Bipolar junction transistor
BPF	Bandpass filter
DC	Direct current
DF	Dissipation factor
ESL	Equivalent series inductance
ESR	Equivalent series resistance
FET	Field effect transistor
FIT	Failures in time
IGBT	Insulated gate bipolar junction transistor
LED	Light emitting diode
MTBF	Mean time between failures
MTTF	Mean time to failure
PF	Power factor
PFC	Power factor correction
PI	Proportional Integral
PID	Proportional Integral Differential
PR	Proportional Resonant
PWM	Pulse-width modulation

SMC	Sliding Mode Control
THD	Total harmonic distortion

Acknowledgements

First and foremost, I would like to thank my supervisor, Dr. Wilson Eberle, for both his technical support and moral support during my extended time as a graduate student. His understanding of balancing family, work, and studies helped me persevere.

I would also like to thank my parents Maury and Linda. They not only provided many hours of babysitting while I worked away, but they were also fantastic cheerleaders who helped keep me on track.

Chapter 1: Introduction

All AC-DC converters require a way to convert the varying power on the AC side into a constant power on the DC side. In order to do this conversion, an intermediate energy storage mechanism (a filter) is required. This filter is typically implemented using a large capacitor on the DC side to absorb energy when the AC power is higher than what is needed and to provide energy when the AC power is lower than what is needed. Because of the size of the capacitance required for this filter, an electrolytic capacitor is usually used because they can very easily and cost effectively provide the needed capacitance. Electrolytic capacitors have some drawbacks though and the biggest drawback is that their life expectancy is quite low - lower than any other electrical or electronic component. Low power systems that require long life, such as consumer style LED light bulbs can possibly still use electrolytic capacitors because the low power requirements result in lifespan de-rating that will likely meet lifespan requirements. High power systems (e.g., a few hundred Watts and up) will typically have higher operating temperatures meaning the lifespan will not be de-rated as much as low power systems.

In high power systems such as photovoltaic micro-inverters and industrial scale LED lighting systems where operating temperatures are high and long life is required, electrolytic capacitors should not be used because they simply do not have a long enough life expectancy.

1.1 AC-DC Converters

This section identifies some of the common AC-DC converter topologies, briefly outlines their benefits and drawbacks, and highlights the commonalities amongst them. All AC-DC converters have a means of rectifying the AC voltage and a means of filtering the ripple power. Optional stages of AC-DC converters are a transformer to step down the AC voltage, a linear or switching regulator to maintain the voltage at a constant value and a power factor correction stage.

Figure 1.1 is one of the most basic AC-DC conversion topologies. It has a low component count but is unregulated so the voltage will vary somewhat with the load. The charging/discharging cycle of the capacitor also makes the power factor of this topology very low.

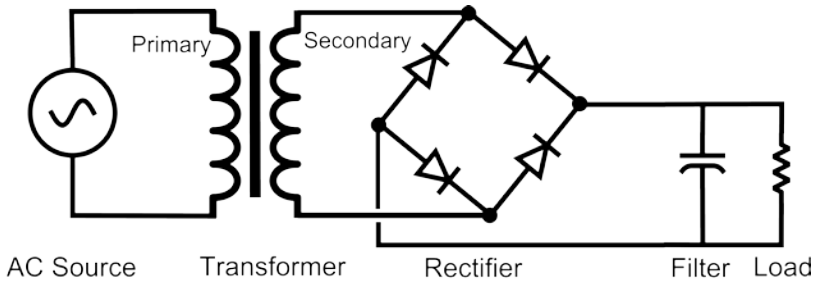

Figure 1.1 Full Wave Rectifier with Capacitive Filtering

Figure 1.2 adds an inductor to the output filter. This inductor removes large current spikes and forces the input current to be continuous over each cycle. The inductor improves the power factor but due to the low frequency of the AC source, it may be physically too large and expensive for practical applications.

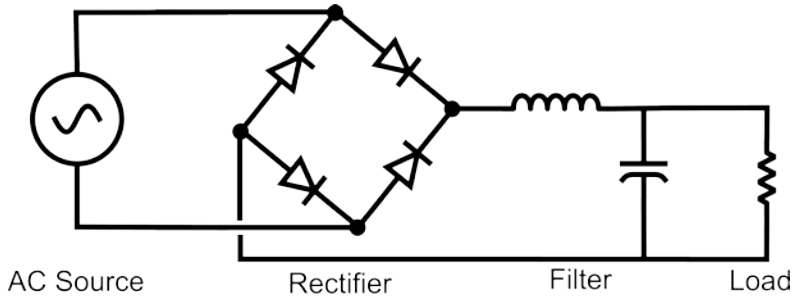

Figure 1.2 Full Wave Rectifier with Capacitive and Inductive Filtering

Figure 1.3 features a regulator for controlling the output voltage. This regulator could be a linear regulator or a switching regulator. Switching regulators are much more common because they are nearly as cheap and easy to use as linear regulators, but offer much higher efficiency.

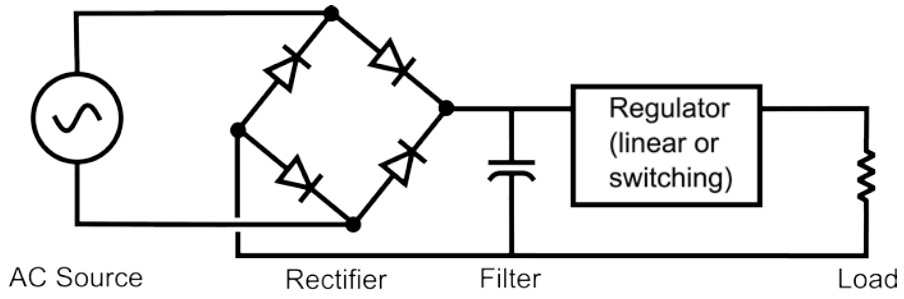

Figure 1.3 Full Wave Rectifier with Regulated Output

Figure 1.4 includes a boost regulator at the output of the rectifier. The purpose of this switching regulator is to control the current so that it is in phase with the AC voltage to maximize power factor. Also, depending on the control loops used, the boost regulator can also regulate the voltage to the load. There are obvious increases in the complexity of this topology compared to the original topology of Figure 1.1 which has only capacitive filtering, but the significant improvement in power factor is typically worth it, especially for converters operating at higher powers that must meet total harmonic distortion (THD) and power factor standards such as IEC-61000-3-2 [1].

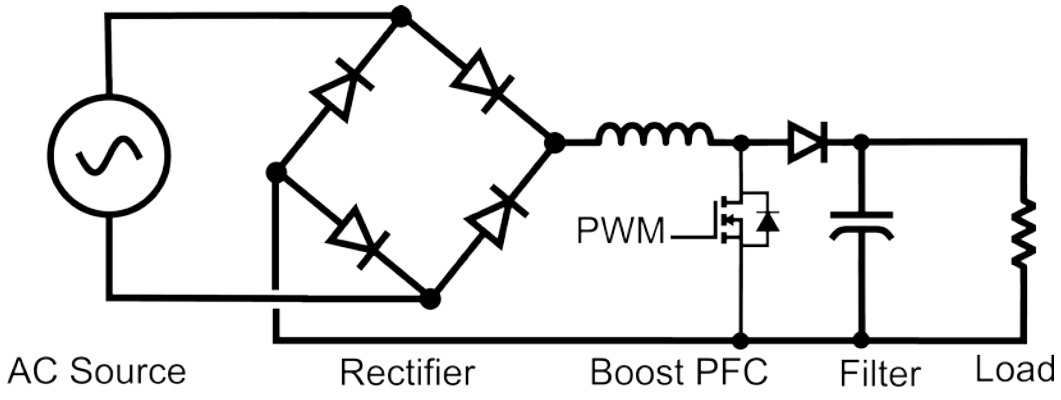

Figure 1.4 Full Wave Rectifier with Boost Power Factor Correction and Regulation Circuit

These example topologies progressed from very simple to somewhat more complicated, but all topologies have two things in common, the rectifier and the filter. The rectifier performs AC-DC

conversion in the strictest definition of the term (i.e., it forces current to go through the load in one direction only), and the filter minimizes the transfer of the ripple power from the AC input to the DC output. The next section provides some more details about the specifics of the ripple power.

1.2 Double Line Frequency Ripple

The power ripple that must be filtered is often called the double line frequency ripple because the frequency of the ripple is at two times the frequency of the line (AC) voltage.

The power delivered by the AC side can be determined from the sinusoidal voltage ($v_{ac}(t)$) and current ($i_{ac}(t)$) on the AC side where the voltage and current are given by:

$$v_{ac}(t) = V_p \cos(\omega t)\ V \quad \textbf{(1-1)}$$

$$i_{ac}(t) = I_p \cos(\omega t - \varphi)\ A \quad \textbf{(1-2)}$$

The peak voltage is V_p, the peak current is I_p, the frequency of the voltage and current is ω radians per second, and the phase difference between the voltage and current is φ radians.

Multiplying the sinusoidal voltage by the sinusoidal current gives the time varying power

$$p_{ac}(t) = v_{ac}(t) i_{ac}(t) = V_p \cos(\omega t) I_p \cos(\omega t - \varphi) \quad \textbf{(1-3)}$$

Expanding (1-3) gives

$$p_{ac}(t) = V_p I_p \cos(\omega t) \cos(\omega t - \varphi)$$

$$p_{ac}(t) = \frac{V_p I_p}{2}[cos(\omega t - \omega t + \varphi) + cos(\omega t + \omega t - \varphi)]$$

$$p_{ac}(t) = \frac{V_p I_p}{2}[cos(\varphi) + cos(2\omega t - \varphi)]$$

$$p_{ac}(t) = \frac{V_p I_p}{2} cos(\varphi) + \frac{V_p I_p}{2} cos(2\omega t - \varphi) \quad \textbf{(1-4)}$$

The term $\frac{V_p I_p}{2} cos(\varphi)$ is the average power on the AC side and is also the power delivered to the DC side so it can be designated as

$$P_o = \frac{V_p I_p}{2} cos(\varphi) \quad \textbf{(1-5)}$$

When the power factor is 1, the phase difference between the AC voltage and current is 0 so the average power is simply $\frac{V_p I_p}{2}$.

The term $\frac{V_p I_p}{2} cos(2\omega t - \varphi)$ from eqn (1-4) represents the ripple power. In order to deliver ripple free power to the DC side, this ripple power needs to be decoupled from the average power. To accomplish this decoupling, the energy must be stored in a filter when the instantaneous value of the ripple power is positive, and must be released by the filter when the instantaneous value is negative. Figure 1.5 highlights the periods of time when energy must be stored by the filter and when energy must be released by the filter.

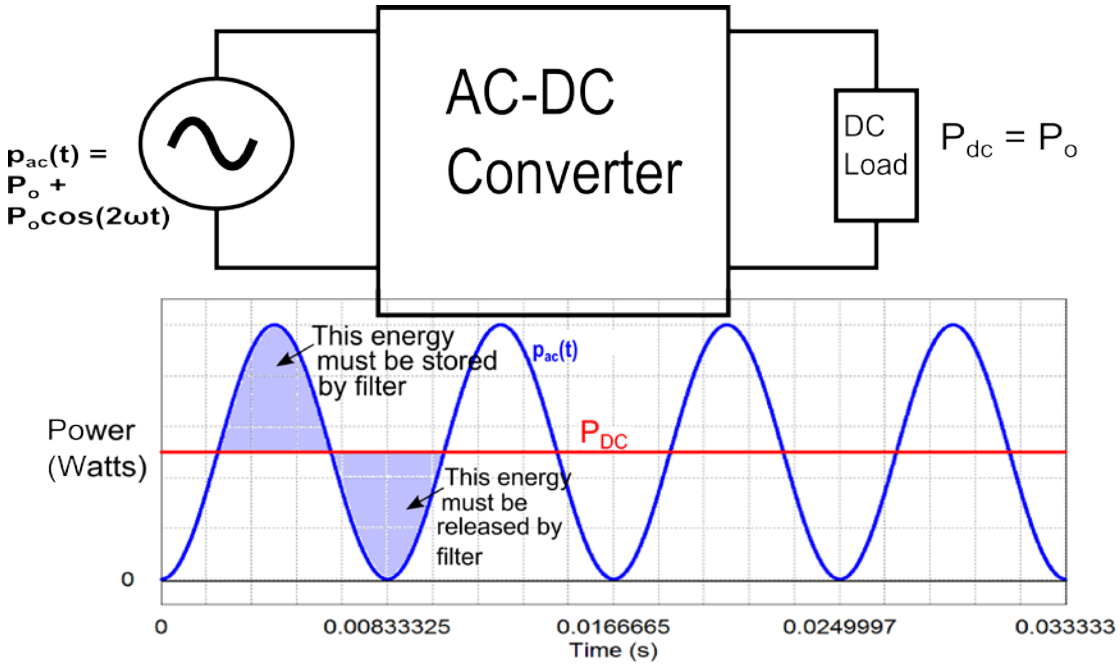

Figure 1.5 Power transfer in AC-DC Converter

1.3 Double Line Frequency Ripple Filter

The most common way to implement a double line frequency filter is to place a large capacitor across the output as shown in Figure 1.6.

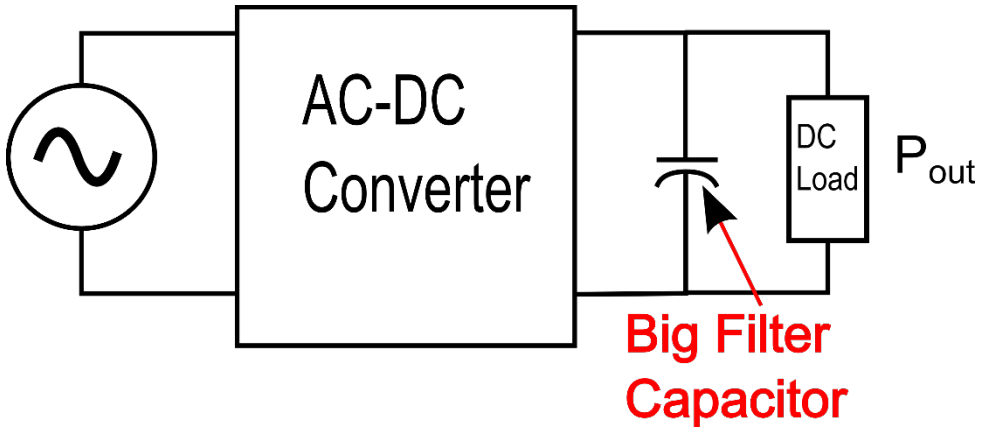

Figure 1.6. AC-DC Converter with Ripple Filter Capacitor

The required capacitance for the filter is derived in [2] and can be determined from the output power (P_o), the line frequency in radians per second (ω_{line}), the output voltage (V_o) and the allowable voltage ripple at the output (ΔV)

$$C = \frac{P_o}{2\omega_{line} V_o \Delta V} \quad \textbf{(1-6)}$$

Table 1.1 shows the required ripple filter capacitance for two example AC-DC converter systems (for both of these examples, the line frequency is assumed to be 60Hz):

Table 1.1 Capacitance Requirements for Example AC-DC Converters

Output Power	Output Voltage	Ripple %	Filter Capacitance
700W	400V	1	580μF
1.5kW	110V	5	17.2mF

To minimize cost and space, capacitors of the sizes indicated in Table 1.1 will need to be electrolytic capacitors. In almost all AC-DC converter systems electrolytic capacitors are used as the double line frequency ripple filter because of their relatively low cost and small footprint. The downside to using electrolytic capacitors is that their expected lifespan is relatively short. Film capacitors are an alternative to electrolytic capacitors; they are more robust and long lasting but for the same capacitance, they are larger and considerably more expensive.

Table 1.2 shows a comparison between electrolytic capacitors and film capacitors with similar ratings that would more or less meet the needs of the systems from Table 1.1. Note that these costs are for orders of 100 units and were current at time of writing.

Table 1.2. Comparison Between Electrolytic and Film Capacitors [3]

Electrolytic Capacitors				**Film Capacitors**			
Man. and Part #	**Rated Voltage**	**Capacitance**	**Cost**	**Man. and Part #**	**Rated Voltage**	**Capacitance**	**Cost**
United Chemi-con E36D451LPN611TAE3N	600V (DC)	610µF	$15.38	CDE 947D581K901BFMSN	900V (DC)	580 µF	$119.03
CDE 382LX222M400B092VS	400V (DC)	22mF	$20.73	AVX FFLI6B1607K--	800V (DC)	16mF	$278.17

1.4 Minimizing Required Capacitance

The double line frequency ripple filter capacitor of Figure 1.6 is performing two competing but simultaneous functions. It is maintaining a constant DC output voltage, but it is doing this by absorbing and releasing energy. The result is that the voltage is mostly constant but it is varying a little bit in the form of a ripple. In order to maintain the constant DC voltage and have the relatively small power ripple, the capacitance needs to quite high. In fact, it needs to be much higher than the minimum capacitance that could filter the power ripple. An alternative method to the typical, parallel capacitor is to add to the circuit a separate port whose only purpose is to match the power ripple of the AC side of the converter. This separate port could operate at any voltage since it is not tied to either the input or the output. The only requirement for the port would be that the power into the port must match the power ripple from the AC side of the

converter. If such a ripple port were implemented with a capacitor, the voltage, current and power signals to the port would look like this:

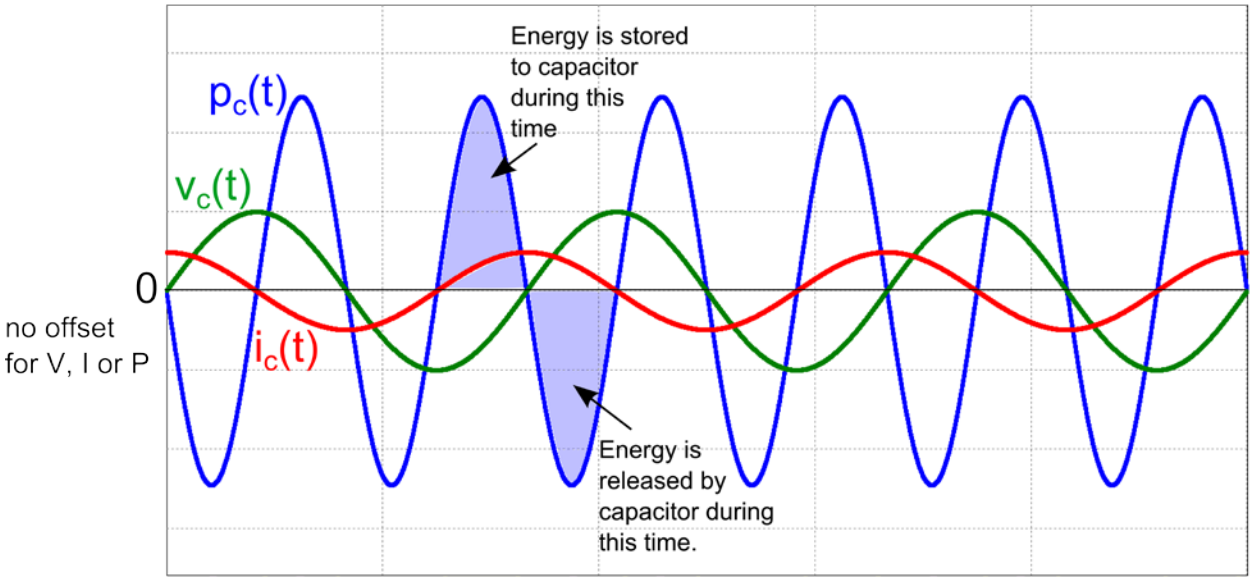

Figure 1.7 Voltage, Current and Power Waveforms to Ripple Port Circuit

Two significant advantages come from using a ripple port like this that is not directly tied to either the input or the output. First, the ripple port does not need to have a DC offset so the capacitor can be minimally sized. Second, the peak voltage across the ripple port capacitor can theoretically be set to any value and the higher the voltage, the more energy that can be stored in the capacitor for a given capacitance.

1.5 Research Motivation

Any AC-DC converter will benefit from having a longer life expectancy and some AC-DC converters, such as those in LED lighting systems are **required** to have a long life to meet market demands. LED lights which typically include the LEDs as well as the DC power supplies are often warrantied for up to ten years [4]. The system stresses in higher power (hundreds of Watts) industrial scale lighting systems mean that electrolytic capacitors cannot be used if long

life is required [5] so industrial scale/high power LED lighting systems should be built without them. The AC-DC converters of these systems must still filter the double line frequency ripple but doing so will require the use of expensive film capacitors or the use of an alternative ripple filter mechanism.

The objective of this thesis is to realize an alternative ripple filter (power decoupling) mechanism with applications in isolated AC-DC boost PFC converters. The alternative ripple filter mechanism will use a ripple port which is also known as an active power decoupling (APD) port), which is a circuit separate from both the AC and the DC parts of the converter [6]. The APD port design of this thesis yields improvements over existing techniques because it does not require direct measurement of the AC voltage or current to generate the control signals for the APD port. This improvement allows the AC side and the DC side of the converter to be electrically isolated from each other.

A secondary objective of this thesis is to introduce a new control methodology for the APD port.

1.6 Thesis Organization

This thesis is organized into five chapters. Chapter 1 introduces the necessity of double line frequency filters on AC-DC converters and outlines the differences between electrolytic and film capacitors. It also presents the idea of a ripple or active power decoupling port as an alternative way to eliminate double line frequency ripple.

Chapter 2 provides an in-depth literature review of the reliability and life expectancy of electrolytic capacitors and film capacitors as well proposed topologies and control methods for implementing active power decoupling in AC-DC and DC-AC converters.

Chapter 3 presents a new design for an active power decoupling system including the topology, reference signal generation and control methodology. The active power decoupling system is designed for a 700W/400V AC-DC converter with boost power factor correction (PFC). The APD system uses a buck converter based topology, sliding mode control and generates the control system's reference signal from the DC voltage. The theory behind the design as well as design choices are described in this section.

In Chapter 4, the effectiveness of the new system is verified in simulation by comparing it to the original boost PFC circuit. The performance metrics compared include total harmonic distortion, power factor, voltage ripple, and capacitance required.

Chapter 5 is a summary of the contributions of this thesis and outlines potential areas for future work and improvements.

Chapter 2: Literature Review

This chapter starts by detailing the characteristics of and differences between electrolytic and film capacitors and then describes the tradeoffs that must be made when choosing between the two types of capacitors for a circuit. Next, this chapter reviews methods used to reduce the capacitance required for ripple power decoupling. By reducing the required capacitance, the more reliable film capacitor can then be cost effectively used for ripple power decoupling. Different aspects of capacitance reduction strategies will be analyzed including common topologies and control methods used.

2.1 Capacitor Overview

Capacitors are energy storage devices which store energy in the form of charges separated by an insulating barrier. The basic model of a capacitor consists of two overlapping parallel plates that are separated by a thin dielectric or insulating barrier. The capacitance of a capacitor refers to the ability of these parallel plates to hold charge when some voltage is applied across the two plates. In equation form, this relationship between capacitance, charge and voltage is

$$C = \frac{Q}{V} \qquad \textbf{(2-1)}$$

where C is the capacitance in Farads, Q is the charge in Coulombs and V is the applied voltage in Volts.

In this parallel plate configuration, capacitance is determined by three factors. The first factor is the area of overlap between the parallel plates. The larger the area of overlap the more “room”

there is for charge to build up on the plates for a given voltage. The second factor for determining capacitance is the distance between the plates. The closer the plates are, the stronger the electric field between the plates is. This stronger electric field draws in more electrons to the negative side and pushes away more electrons on the positive side which means more charge is able to build up on the plates for a given voltage. The final factor that determines the capacitance of a capacitor is the dielectric material between the plates. A good dielectric material is one that is a good insulator but whose molecules can be strongly polarized by the applied electric field. The dipoles created have an attractive effect on electrons to the negative side and a repulsive effect on electrons on the positive side of the capacitor. This also allows more electrons to build up for a given voltage thus increasing the capacitance. Figure 2.1 illustrates the effect of a dielectric on the electric field in a capacitor.

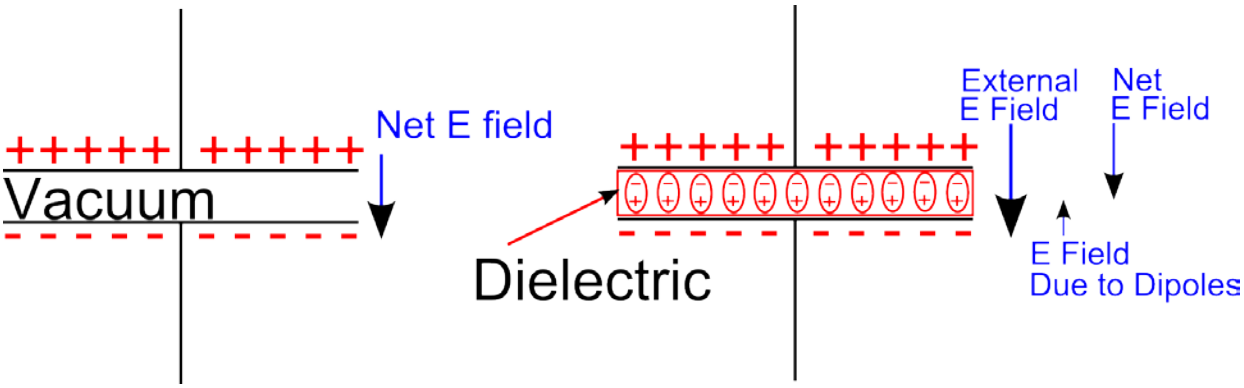

Figure 2.1 Electric fields in capacitors comparing vacuum between plates to a dielectric between plates

Combining these three factors, the capacitance of a parallel plate capacitor can be calculated as

$$C = \frac{\epsilon A}{d} \qquad \textbf{(2-2)}$$

Where ϵ is the permittivity of the dielectric (in $\frac{F}{m}$), A is the overlapping area of the parallel plates (in square meters), and d is the distance between the two plates (in meters).

Capacitors can be manufactured in different ways using different materials, but they all use the 3 general ways of setting the capacitance for a given capacitor: create overlapping surface area for charges to be stored on, place those surface areas close together, and provide a dielectric material between the surfaces.

2.1.1 Non-ideal Characteristics of Capacitors

Real capacitors have many non-ideal characteristics and this section outlines the most important ones. It is important to understand the effect these characteristics have in a circuit because the quantity of effect varies depending on the type of capacitor and this therefore informs the decision of what kind of capacitor to use for the circuit.

Equivalent Circuit Diagram

The model of a physical capacitor must include a few non-ideal properties because of resistance and inductance in the leads as well as conductance between the two insulating plates which causes charge leakage. Figure 2.2 is an equivalent circuit diagram of a physical capacitor:

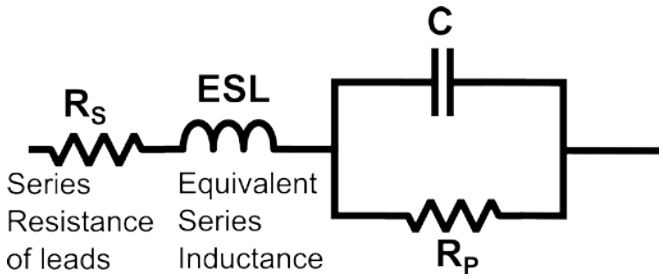

Figure 2.2. Equivalent Circuit of a Physical Capacitor

The equivalent series inductance (*ESL*) is the inductance introduced by the leads of the capacitor. C is the capacitance while R_p is the resistance between the two "plates" of the capacitor. In other words, it is the insulation or dielectric resistance. This resistance is large but not infinite, so will allow some charge leakage between the plates. R_S is the resistance introduced by the leads and connections in the capacitor. Combining R_s and the series equivalent of R_P gives the equivalent

series resistance (ESR) which is a frequency dependent value that causes power loss during flow of AC current.

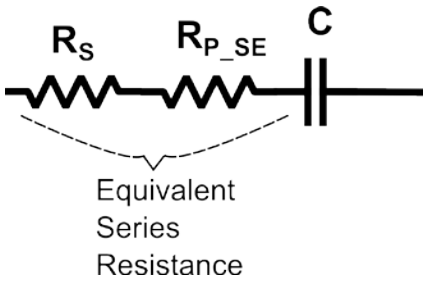

Figure 2.3 Equivalent Circuit of Capacitor showing ESR.

Just like in Figure 2.2, R_S is the resistance introduced by the leads and connections in the capacitor and generally this value is so small that it can be ignored. R_{p_SE} is the series equivalent of R_P from Figure 2.2.

Capacitance Tolerance: Is the maximum allowable deviation from the rated value that a capacitor can vary (given in percent).

Temperature Coefficient: A property of capacitors that indicates how capacitance changes with temperature. This capacitance change is usually temporary, although extreme temperatures can damage the capacitor and cause permanent changes. The temperature coefficient is mostly determined by the type of dielectric so different types of capacitors will have radically different temperature coefficients. For example, polypropylene film capacitors have negative temperature coefficients while polyester film capacitors have positive temperature coefficients [7].

Humidity Coefficient – A measurement of how much the relative capacitance will change for a 1% change in humidity. At a humidity less than 30%, the humidity coefficient is very small and at humidity above 85%, the humidity coefficient is large and unpredictable [8]. High humidity for extended periods of time can cause permanent damage to capacitors by removing the film metallization. [8]

Capacitor Frequency Dependence – Some types of capacitors are more sensitive to frequency than others. Polypropylene capacitors experience little change in capacitance up to 1MHz, while polyester capacitors experience a decrease in capacitance with increasing frequency. [8]

Dissipation Factor – Under an AC voltage, the magnitude of the phase difference between the voltage across and current through a capacitor should be 90°. Because of the ESR, the phase difference will be something less than 90°. The difference between 90° and the actual voltage to current phase angle is the defect angle, δ. The measurement of $\tan(\delta)$ is called the dissipation factor which can also be determined by the ratio of the ESR to the capacitive reactance: [8]

$$dissipation\ factor = tan(\delta) = \frac{ESR}{X_C} = \frac{ESR}{1/\omega C} = ESR \times \omega C \quad \textbf{(2-3)}$$

Dissipation factor is usually the parameter provided on capacitor data sheets, but the ESR and power dissipated through the ESR (i.e., self-heating) can be determined from it.

Insulation Resistance – is the resistance between the plates of a capacitor under DC voltage. This resistance should be very high, but varies with temperature (peak at around 15°C) and decreases over time.

Category Temperature Range – The range of temperatures in which the capacitor is able to operate from the minimum (T_{min}) to the maximum (T_{max}).

Rated DC Voltage – This is the maximum voltage that the capacitor is designed to continuously withstand at any temperature within the category temperature range.

Rated AC Voltage – This is the maximum RMS voltage at a specific frequency that the capacitor is designed to continuously withstand at any temperature within the category temperature range

The bottom line when it comes to all of these capacitor parameters is that the choice of capacitor for a given application requires much more consideration than just the cost and the capacitance. Specific applications will put more or less weighting on different parameters. Similarly the environment in which the capacitor will be operating will also be a factor in capacitor choice. When the conditions of the environment cannot be easily controlled, selection of capacitor should be done in a way that minimizes the effects of the conditions (e.g., heat and humidity). Power converters potentially need to operate in extreme environments, and if so, attention would need to be paid to temperature range, temperature coefficient as well as humidity coefficient. In applications where high efficiency is important, ESR and ESL would also need consideration.

2.2 Electrolytic Capacitors

2.2.1 Overview of Electrolytic Capacitors

Electrolytic capacitors are a variation of the parallel plate capacitor where the anode and the cathode are rolled together to create the overlapping surface area as shown in Figure 2.3. The figure indicates etching on the anode foil and the purpose of the etching is to increase the surface area and therefore increase the capacitance.

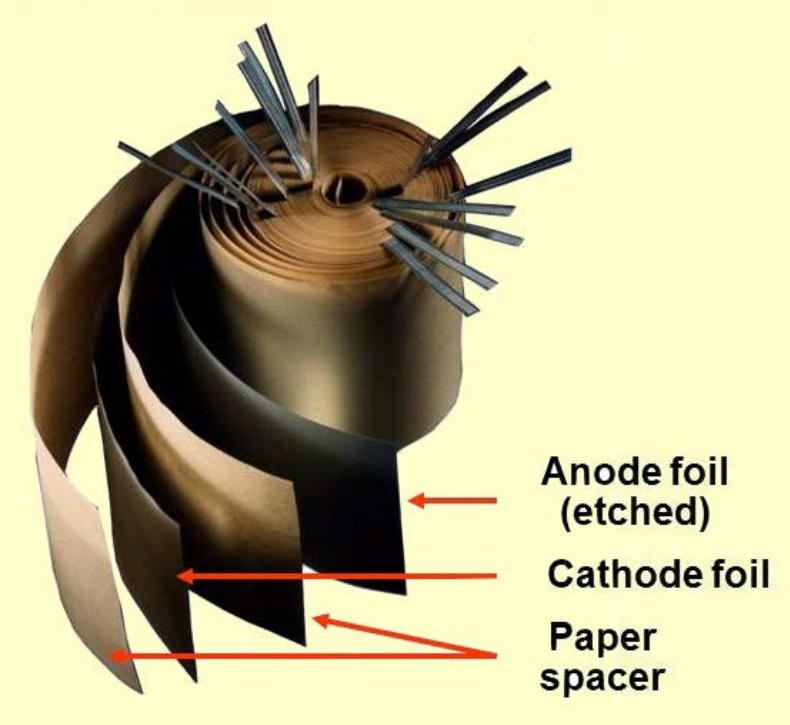

Figure 2.4 Anode and Cathode Rolls of opened Electrolytic Capacitor [9] CC0 1.0

Zooming in on the interface between anode and cathode as in Figure 2.4 allows a good view into how the overlap creates the capacitance.

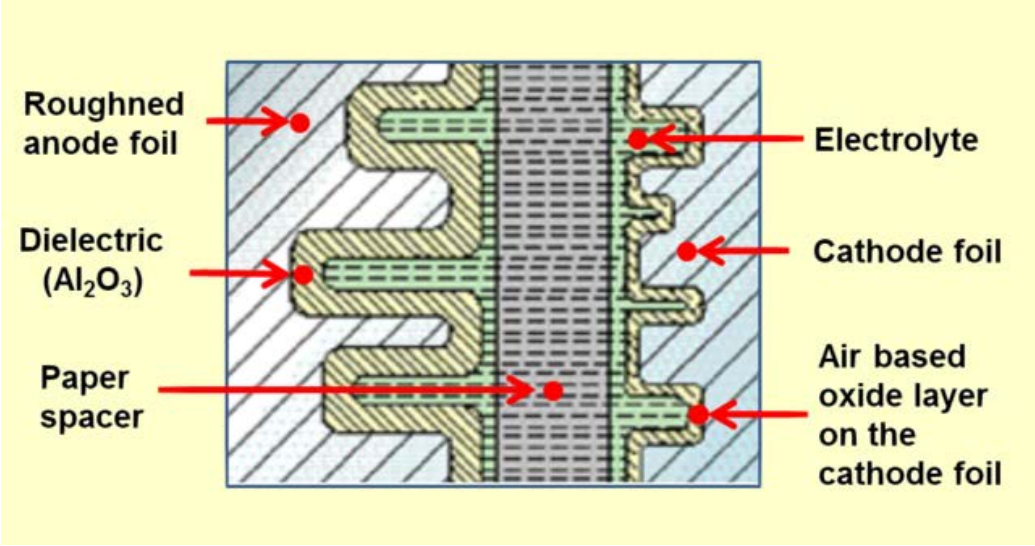

Figure 2.5. Cut through of Inner Construction of Electrolytic Capacitor [10] CC0 1.0

The capacitance is created between the roughened anode foil (roughened to increase surface area by more than 100 fold) and the electrolyte. The aluminum oxide on the anode foil acts as the dielectric between anode and the electrolyte. The large surface area and the extremely thin dielectric (less than a micrometer) results in electrolytic capacitors that can vary from 0.1μF to 3F with voltage ratings from 5V to 700V [5].

The electrolyte in these capacitors is a blend of different formulations depending on the rated voltage and operating temperature. It is made up of a solvent (such as ethylene glycol, dimethylformamide or gamma-butyrolactone) and a conductive salt solute such as ammonium borate or other ammonium salt. Water is also added to the electrolyte to increase the conductivity and to help seal leakage points in the dielectric. This self-healing occurs when leakage current causes hydrolysis of the water and the oxygen generated causes aluminum oxide to grow and seal the leakage. The negative side effect is that hydrogen gas is also created and must be vented. The venting occurs out of a specially designed seal that must be loose enough to allow H_2 gas to escape but tight enough to minimize the drying out of the electrolyte [5].

Hydrogen gas can also build up quickly if too much voltage is applied to the capacitor or if voltage is applied in the reverse direction. If the gas is generated too quickly, the seal will burst, often in an explosive manner. If sparking occurs at any time when hydrogen is being expelled, the hydrogen might actually be ignited. [5]

Aluminum Electrolytic Capacitors can provide high capacitance for a relatively low cost and so they excel in short term energy storage in application such as filtering for AC power supplies, switch mode power supplies, and power factor correction circuits [11]. Al e-caps have a few shortcomings. One of these shortcomings is that they have a relatively high ESR, which can contribute to wasted energy and cause self-heating to occur. Another shortcoming that will be

discussed in the next section is that they have a shorter lifetime and lower reliability than most other electronic components (including other types of capacitors).

2.2.2 Lifetime and Reliability of Electrolytic Capacitors

Expected lifetime and reliability are similar factors that are both related to component failures, but they have some significant differences. Expected life (which is also known as Wear-out Life, Operating Life, or Useful Life) tells how long a component will last under specific operating conditions (applied voltage, current and operating temperature). The expected life is typically a result of the component wearing out. An electrolytic capacitor is considered to have reached the end of its life when it no longer functions as intended in its application. This reduction of function can be due to a decrease in the capacitance, an increase in the ESR or an increase in the dissipation factor (DF) [11]. Various international standards are available that define the failure criteria for electrolytic capacitors Two of these standards are outlined in Table 2.1.

Table 2.1. Failure Standards for Capacitors

Type of Test	Standard	Test Conditions	Failure Criteria
Endurance	IEC 60068-2	Test at maximum temperature and rated voltage	• DF > 1.3 × $stated\ limit$ • Impedance > 2 × $stated\ limit$ • Change in capacitance more than 10%
Useful Life	CECC 30301	Test at maximum temperature, rated voltage, and rated ripple current	• DF > 3 × $stated\ limit$ • Impedance > 3 × $stated\ limit$ Change in capacitance more than 30%

Reliability, on the other hand, is a statistical measure of the number of expected random failures (typically due to a latent weakness in a particular component) when given a large number of devices operating over a long period of time.

2.2.2.1 Lifetime Estimation

The lifetime estimation of capacitors provides an estimate as to how long the capacitor will function before there are significant changes in its characteristics (failure criteria examples are provided in Table 2.1). The lifetime estimation is based on electrical stress, mechanical stress and temperature. Capacitor manufacturers will usually publish lifetime estimation test results at a certain temperature, voltage and ripple current. Design engineers can then use this data to determine the expected life under the expected operating conditions. The process of adjusting the expected life based on operating conditions is called de-rating, and this de-rating calculation uses a version of the Arrhenius Equation which is a formula used to calculate reaction rates when the reaction rates are temperature dependent [12]. The specific equation is typically provided by the capacitor manufacturer.

If the lifetime is going to be de-rated due to temperature, the de-rating equation looks like this [12]

$$Life = Life_b \times 2^{0.1(T_m - T_c)} \quad \textbf{(2-4)}$$

$Life$ is the expected life
$Life_b$ is the base life at an elevated temperature (determined by the manufacturer)
T_m is the elevated temperature used for establishing the base life
T_c is operating temperature of the application

If the lifetime is also going to be de-rated for operating voltage, the de-rating equation will have an additional factor of M_v

$$Life = L_b \times M_v \times 2^{0.1(T_m - T_c)} \quad \textbf{(2-5)}$$

M_v is a voltage multiplier equal to 1 when the capacitor is operated at the rated DC voltage and greater than 1 when the capacitor is operated at less than the rated voltage. For determining the voltage multiplier (M_v), Cornell Dubilier [12] uses

$$M_v = 4.3 - 3.3\frac{V_a}{V_r} \quad \textbf{(2-6)}$$

V_a is the applied voltage
V_r is the rated voltage

The lifetime can also be affected by the ripple current. Ripple current in a capacitor can be fairly significant and since the ESR of electrolytic capacitors is relatively high, there can also be some temperature rise in the capacitor due to ripple current ($I_{ripple}^2 ESR$) heating. The rise of temperature will be offset somewhat by the capability of the capacitor to dissipate the heat and this capability to dissipate heat depends on the heat radiation constant β (which is measured in $\frac{W}{°C \times cm^2}$) and the surface area of the capacitor (A in cm^2). The temperature rise (ΔT) can be most reliably obtained by directly measuring it, but it can also be approximated by the following equation [13]

$$\Delta T = \frac{I_{ripple}^2 R_{ESR}}{\beta \times A} \quad \textbf{(2-7)}$$

The value of β will change from device to device and from circuit to circuit, but a good estimate can come from Table 2.2. The surface area for a cylindrical capacitor can be calculated by [13]

$$A = \frac{\pi}{4} D(D + 4L) \quad \textbf{(2-8)}$$

Where D is the diameter of the cylinder and L is its length.

Table 2.2 Heat Radiation Constants for Various Electrolytic Capacitor Case Diameters

Case Dia (mm)	5 or less	6.3	8	10	12.5	16	18	20	22	25	30	35	40
$\beta(\frac{W}{^{\circ}C \times cm^2})$	2.18	2.16	2.13	2.10	2.05	2.00	1.96	1.93	1.88	1.84	1.75	1.66	1.58

To estimate the overall lifetime of the capacitor factoring in the operating temperature, operating voltage and ripple current requires the following equation:

$$Life = Life_b \times M_v \times 2^{0.1(T_m - T_c)} \times 2^{\left(\frac{\Delta T_0 - \Delta T}{\Delta T_0}\right)} \quad \textbf{(2-9)}$$

ΔT_0 is the only expression not in this equation that has not yet been defined. It is the temperature rise due to the rated ripple current.

Example Lifetime Calculation

The following is an example lifetime estimation calculation for a 100μF capacitor from Nippon Chemi-con with the part number EKXG451ELL101MM40S [14]. This capacitor is operating as the DC bus ripple filter in the system shown in Figure 3.2. Table 2.3 shows its rated characteristics as well as its operating characteristics.

Table 2.3. Characteristics for Calculating Expected Life of Al e-cap

Characteristic	Value
Base Expected Life (L_b)	10000 hours
Rated Voltage (V_r)	450V
Operating Voltage (V_a)	400V
Base Temperature (T_m)	105℃
Operating Temp (T_C)	85℃ [15]
Rated Ripple Current (I_{rr})	0.8A
Operating Ripple Current (I_r)	0.96A
Equivalent Series Resistance (R_{esr})	3.18Ω
Heat Radiation Constant (β)	1.96
Surface Area (A)	$A = \frac{\pi}{4} D(D + 4L) = 25.16$

$$M_v = 4.3 - 3.3\frac{V_a}{V_r} = 4.3 - 3.3\frac{400}{450} = 1.37$$

$$\Delta T_0 = \frac{I_{rr}^2 R_{ESR}}{\beta \times A} = \frac{(0.8A)^2\left(\frac{0.24}{2 * \pi * 120Hz * 100\mu F}\right)}{1.96 \times \frac{\pi}{4} 1.8(1.8 + 4 \times 4)} = \frac{(0.64)(3.18)}{1.96 \times 25.16} = 0.041℃$$

$$\Delta T = \frac{I_r^2 R_{ESR}}{\beta \times A} = \frac{(0.96A)^2 \left(\frac{0.24}{2 * \pi * 120Hz * 100\mu F}\right)}{1.96 \times \frac{\pi}{4} 1.8(1.8 + 4 \times 4)} = 0.059℃$$

$$Life = Life_b M_v 2^{0.1(T_m - T_c)} \times 2^{\left(\frac{\Delta T_0 - \Delta T}{\Delta T_0}\right)} = 10000 \times 1.37 \times 2^2 \times 2^{-0.44} = 40{,}388\ hours\ (4.6\ years)$$

2.2.2.2 Capacitor Reliability

While the lifetime of a capacitor is determined by the predictable electrochemical degradation of the capacitor over time (accelerated by temperature, voltage and current stress), the reliability of a group of capacitors is determined by random failures of capacitors within the population. These random failures are due to unpredictable weaknesses in the paper, foil or connections of some capacitors. The failure rate of a group of components over the expected lifetime follows the well-known bathtub curve [16] where a large but decreasing number of failures occur in the beginning of use ("infant mortality" failures) followed by a period of constant failure rate (random failures) and ending with an increasing failure rate due the devices wearing out and reaching the end of their lives.

The initial failures are typically due to failures in manufacturing that are discovered shortly after the devices are put in to use. The end of life failures are due to the wear-out processes described earlier in sub-section 2.2.2.1. The constant failure rate period is determined by a statistical analysis and is the subject of the rest of this sub-section.

Methods such as MIL-HDBK-217 [17], Telcordia SR332 [18] and others (including manufacturer specific methods) are used to predict the failure rates during the lifetime of capacitors. Failure rate, is denoted as λ or FIT (Failures In Time) and is typically measured as the number of expected failures per billion hours of operation. Alternatively, the Mean Time

Between Failures (MTBF) can be used to quantify reliability. A component with a failure rate of 1 FIT will have a MTBF of one billion hours ($MTBF = FIT \times 10^9$).

MIL-HDBK-217 uses historical data plus various stress factors to allow calculation of the failure rate. The capacitor failure rate model is [17]

$$\lambda_p = \lambda_b \pi_T \pi_C \pi_V \pi_{SR} \pi_Q \pi_E \quad \textbf{(2-10)}$$

[1]

λ_p is the failure rate in $\frac{failures}{10^6 hours}$
λ_b is the base failure rate
π_T is the temperature scaling factor
π_C is the capacitance scaling factor
π_V is the voltage stress factor
π_{SR} is the series resistance factor
π_Q is the quality factor
π_E is the environment factor

All of the various scaling factors are available from the MIL-HDBK-217 specification. Some organizations consider the MIL-HDBK-217 specification out of date for capacitors; it gives failure rates that do not match the latest failure data [12]. Because of this, some organizations create their own failure rate equations. For example Cornell-Dubilier uses the equation [7]

$$\lambda_p = \frac{400000}{Life_b}\left(\frac{V_a^3}{V_r^2}\right)(C^{0.5})\left(2^{\left(T_c - T_m/10\right)}\right) \quad \textbf{(2-11)}$$

Designers who are using electrolytic capacitors in their design, do not, in general, need to know exactly how to calculate FIT or MTBF, but should be aware of which method was used to allow for easier comparisons between devices. For example, an electrolytic capacitor with a FIT calculated using MIL-HDBK-217 will have a more conservative (i.e., higher) value than an e-cap with a FIT calculated using the equation from Cornell-Dubilier.

[1] An online failure rate calculator is available at: http://www.sqconline.com/mil-hdbk-217-capacitor-tables

2.3 Film Capacitors

Film capacitors (film caps) are distinguished by the presence of a plastic film acting as the dielectric between the metal electrodes. Film caps come in two general types, metal foil (also known as film/foil) capacitors and metallized film capacitors. Metal foil capacitors have two metal foil electrodes with terminals attached to them separated by an insulating plastic film and wound into a cylindrical shape [19]. Metallized film capacitors consist of a plastic film onto which aluminum or zinc metal is vacuum deposited through a process called schooping [20]. The deposited metal is very thin which results in a lower current capability than metal foil capacitors. However, the metal thinness allows for self-healing capability; when a short develops across the dielectric, the thin metallized films touch and the high energy density causes them to vapourize at the points of contact removing the short. [19]

Film capacitors are capable of handling high RMS and peak currents, high voltage, bipolar voltage and high levels of shock and vibration [22]. A wide variety of dielectrics are available to allow for selection of a film capacitor based on a specific need. For power electronics applications, polypropylene is the best choice because of its low dissipation factor and ability to perform well over the temperatures and frequencies encountered in power electronics applications [7]. Also, film capacitors do not fail explosively and tend to last much longer than electrolytic capacitors. This last characteristic (long life) is explored in the next section.

2.3.1 Useful Life

Film capacitors can fail outright by failing open or failing short, but most film capacitors reach their end of life due to incremental changes in capacitance, dissipation factor and insulation

resistance that add up over time. When those characteristics fall below a certain predetermined limit, the capacitor is considered to have reached the end of its life [7].

The typical changes that occur in a film capacitor that lead to the aging process are plastic film shrinkage which decreases the capacitance, and moisture absorption which increases dissipation factor and decreases insulation resistance.

While the end of life of a film capacitor does not occur by same mechanism as an Al e-cap, the expected life of a film capacitor is negatively impacted by both higher voltage and temperature just like it is for an Al e-cap. Ripple current is not as much of a factor for film capacitors because the ESR of a film capacitor is much lower. The equation for the expected life of a film capacitor is similar to the Al e-cap equation, except that voltage has a much larger contribution to the useful life in a film than an e-cap [21]

$$Life = Life_b \times \left(\frac{V_r F}{V_a}\right)^8 \times 2^{0.1(T_m - T_c)} \quad \textbf{(2-12)}$$

$Life$ is application service life
$Life_b$ is the base service life at rated temperature and voltage
V_r is the rated voltage
V_a is the application voltage
F is the voltage factor (default value is 1)
T_m is the rated temperature
T_c is the application temperature

Example Lifetime Calculation

The following is an example lifetime estimation calculation for a 35μF capacitor from EPCOS with the part number B32798G8356K [22]. This capacitor is operating as the energy storage device in the APD circuit in the system shown later in Figure 3.15. Table 2.3 shows its rated characteristics as well as its operating characteristics.

Table 2.4 Operating Data for Example Film Capacitor for Estimating End of Life

Characteristic	Value
Base Expected Life (L_b)	60000 hours
Rated Voltage (V_r)	375V
Operating Voltage (V_a)	325V
Base Temperature (T_m)	105℃
Operating Temp (T_C)	85℃ [15]

This capacitor is considered to have failed if the capacitance changes by +/-10%, if the dissipation factor changes to more than four times the upper limit, or if the insulation resistance drops below 1500 MΩ [22]. The time to failure can be estimated using the data from Table 2.4 and eqn (2-11):

$$Life = 60000 \times \left(\frac{375 \times 1}{325}\right)^{8} \times 2^{0.1(105-85)} = 754{,}040\ hours$$

The estimated service life is over 700,000 hours which is more than 86 years. or about 19 times longer than the expected service life of the Al e-cap example in section 2.2.2.1. This example illustrates the significant difference in expected life between an Al e-cap and a film capacitor.

2.3.2 Film Capacitor Reliability

The reliability of a film capacitor is determined in a similar manner as it is for an electrolytic capacitor. Again, since FIT, MTBF and/or MTTF values are given by the manufacturer, there is usually no reason for the user of the capacitor to do their own reliability testing on stand-alone capacitors. The important thing that designers need to keep in mind when comparing capacitors for reliability is that there are different methods for determining FIT, MTBF and MTTF. In order to directly compare reliability data, the methods ideally should be the same and if not, the comparison may require adjustments of the reliability data.

2.4 Film and Aluminum Electrolytic Capacitor Comparison

This section is a summary of the comparison between an Al e-cap and a film capacitor. The reason these two particular capacitors are being compared is because they are the two energy storage capacitors that are used in the benchmark AC-DC converter system (Al e-cap) and the AC-DC converter system (film cap) proposed in this thesis. The data indicates that the reliability of the two devices is about the same but the lifetime of the film capacitor is much longer than the Al electrolytic capacitor.

Table 2.5. Comparison of Al e-cap and Film Capacitor

Properties	Film Capacitor	Al Electrolytic Capacitor
Manufacturer and Part #	EPCOS AG (TDK) B32798G8356K	Nippon Chemi-Con EKXG451ELL101MM40S
Capacitance	35μF	100μF
DC Voltage	875V	450 V
AC Voltage	350V	n/a
Current (RMS)	22A @ 10kHz	800mA @ 120Hz 1800mA @ 100kHz
ESR	250mΩ @ 120Hz	2.7Ω @ 120Hz
Useful Life 1 (Voltage/Temp)	60,000 Hours (875V/105°C)	10,000 Hours (450V/105°C)
Useful Life 2 (Voltage/Temp)	968,000 Hours ($315V_{ac}$/85°C)	40,000 Hours ($400V_{DC}$/85°C)
FIT	$300 \times 10^{-9} \frac{failures}{hour}$ (875V/105°C)	$300 \times 10^{-9} \frac{failures}{hour}$ [2] [12] (450V/85°C)

[2] This value is not from the datasheet for the capacitor, but is a general FIT rate for Al e-caps

2.5 Methods to Reduce Capacitance in AC-DC and DC-AC Circuits

Eliminating double frequency ripple in AC-DC and DC-AC circuits is a well-known and unavoidable requirement. Methods to eliminate or reduce the double frequency ripple can be split into two broad categories, passive decoupling and active decoupling. Passive decoupling uses a circuit made solely of passive components (capacitors, inductors, transformers), while active decoupling requires not only passive components but also a means to actively control the current, voltage, and power to those components. In some of the literature, the term *active filter* is used to refer to the circuits that perform active decoupling. Because of the potential confusion of the term active filter with other types of active filters (e.g. filters built using operational amplifiers), the term *active decoupling* or *active power decoupling* will be used instead.

2.5.1 Passive Decoupling

2.5.1.1 Capacitor on DC Port

The simplest of all passive decoupling methods is shown in Figure 2.5. It involves placing a large (usually) aluminum electrolytic capacitor across the DC load in AC-DC converters and across the DC source in DC-AC converters.

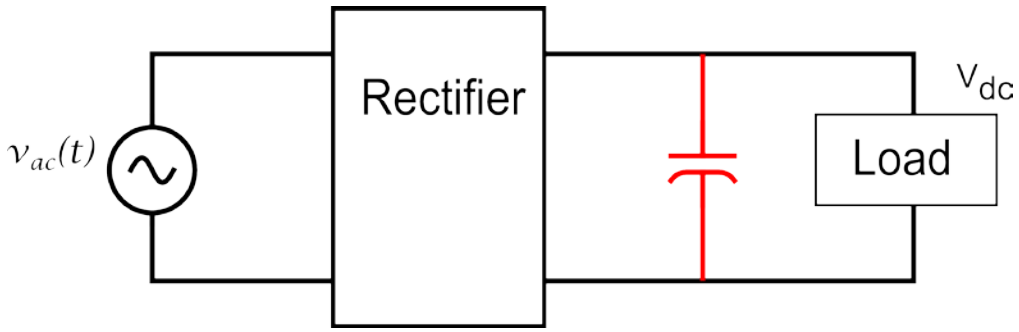

Figure 2.6 AC-DC Circuit with Passive Capacitor Filter

The required capacitance of the filter capacitor is determined in [6] and is

$$C = \frac{P_o}{2\pi f_{line} V_{DC} \Delta V} \quad \textbf{(2-13)}$$

where P_o is the average DC power, f_{line} is the mains frequency, V_{DC} is the DC output voltage and ΔV is the maximum allowable peak-to-peak voltage ripple.

The disadvantage of using a passive capacitor at the DC port is that most of the energy stored in the capacitor is not being used because of the need to keep the voltage across the capacitor at the DC voltage. So to ensure that the voltage ripple is as small as possible, the capacitance must be large. To cost effectively use a large capacitor in the system, an aluminum electrolytic capacitor must be used.

To see how much energy is stored in the capacitor, multiply both sides of eqn (2-13) by $\frac{1}{2}{V_{DC}}^2$ to determine the energy stored in the capacitor

$$W_C = \frac{P_o V_{DC}}{4\pi f_{line} \Delta V} \quad \textbf{(2-14)}$$

Then, to determine the **minimum** energy storage requirement, integrate the ripple power over half of the ripple power cycle to get [6]:

$$W_{min} = \frac{P_o}{4\pi f_{line}} \quad \textbf{(2-15)}$$

Combining (2-14) and (2-15) indicates that the ratio of the DC bus capacitor energy storage requirement to the actual minimum energy storage requirement is

$$\frac{W_c}{W_{min}} = \frac{V_{DC}}{\Delta V} \quad \textbf{(2-16)}$$

In other words, the energy stored in the DC bus capacitor is $\left(\frac{V_{DC}}{\Delta V}\right)$ times more than it needs to be. Of course to reduce the capacitance requires changing the decoupling topology.

2.5.1.2 Coupled Inductor Filter

A coupled inductor filter is another passive circuit that can reduce some of the output ripple by diverting ripple away from the DC port through the coupled inductor into a capacitor. The coupled inductor is a two port system that can be configured to act as one of several different types of filters including low pass and notch filters. Of particular interest is the ability to create a notch filter (at the ripple frequency) by selecting appropriate inductor and capacitor values for L_{dc}, L_{ac}, and C [26]. Figure 2.6 illustrates an AC-DC converter with a coupled inductor filter circuit.

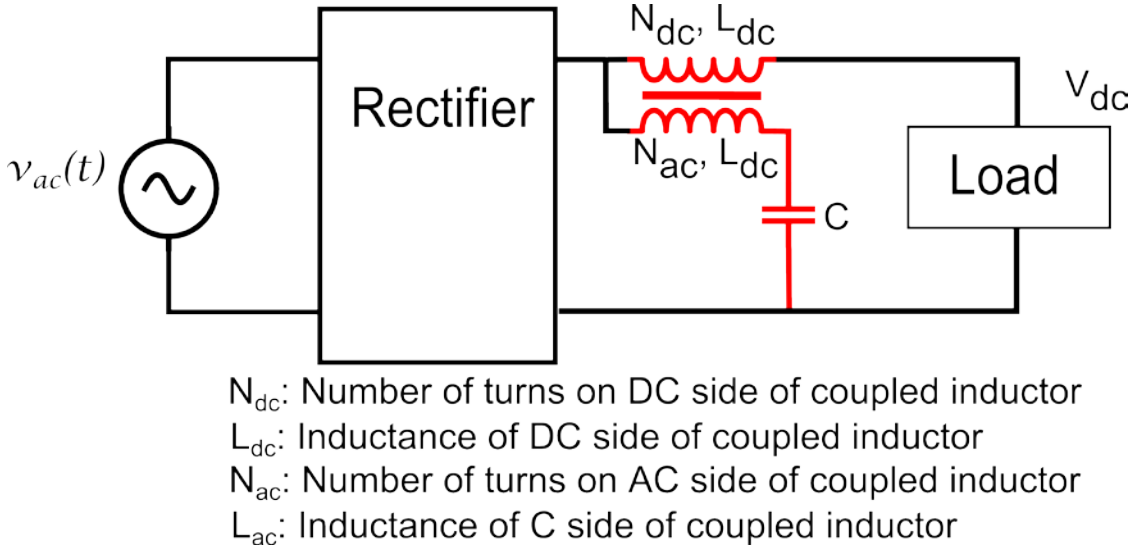

Figure 2.7 AC-DC Converter with Coupled Inductor Filter

This circuit has potential as an improvement over the DC capacitor filter. It still requires only passive components and can in theory pass the entire ripple to the capacitor. In practice though this circuit requires an in depth understanding of magnetics that most designers do not have and

because of its complexity, history has shown that this method gets reinvented and then forgotten over and over again [26]. The filter design must also be very precise and so requires careful accounting of non-idealities such as winding capacitances, parasitic resistances, and capacitor size restrictions otherwise the design won't filter as expected. In [27], an automatic tuning method is proposed, but it requires a control system that is as complicated as any active power decoupling system.

2.5.2 Active Power Decoupling

The general idea of active power decoupling (APD) is to actively channel the ripple power away from the DC load to an energy storage device (capacitor or inductor). With a separate port dedicated to active power decoupling, the voltage of the separate port can be independent of the load voltage and therefore the power decoupling voltage and current can vary with time to match the ripple power. Since the voltage and current can vary with time, the energy storage capability of the capacitor and/or inductor can be fully utilized. This full utilization alone allows for a lower capacitance/inductance to be used. In some cases, the energy storage device can be made even smaller by increasing the voltage to the decoupling port beyond the voltage of the DC load.
The multiple benefits of reducing capacitance include being able to cost effectively use the more reliable film capacitors as well as reducing the size and weight of the filter circuit. Because of these benefits, active decoupling methods have recently been the focus of many researchers [6] , [28]-[41].

Active power decoupling does come with drawbacks and the main ones are that extra components (switches) need to be added and a control system of some kind needs to be implemented. An analysis of the system needs must be undertaken to determine if the increased reliability and extended life of an APD system is worth the added complexity.

El-Habrouk et al. [42] propose that several different aspects or categories should be evaluated when determining what kind of active filter to utilize. Their focus is on active filters for power systems, but the same categories can be applied for active decoupling of power converters. These categories are as follows:

1. **Circuit topology**

   Two broad categorizations of active power decoupling topologies have been proposed [28]. The first categorization uses independent decoupling ports where the energy storage components as well as the switches for controlling the flow of energy are additional to the components used for the converter. The second categorization uses dependent decoupling ports where the energy storage components are separate from the converter but the switches for controlling energy flow to the decoupling port are shared with the converter. The advantage of using an independent port is that it is essentially a stand-alone circuit that can be dropped in to the converter circuit. The advantage of using a dependent port is that fewer components are required.

2. **Energy storage device used**

   The two primary energy storage devices that can be used in power decoupling circuits are inductors and capacitors. Circuits using inductors will not be analyzed because they are generally not practical to use. The high ESR of inductors can significantly reduce the system efficiency, they reach saturation in a non-linear manner making it important to size them correctly, and when acting as energy storage devices, they are physically far bulkier and heavier than capacitors. The literature [28], [29] indicates that other researchers have come to the same conclusion.

3. **Control method used.**

   The two broad categories of control methods are open-loop control and closed-loop control. Within closed-loop control, there are many methods proposed ([6], [29], [30], [32], [33], [36]), but in general, closed loop control systems use a feedback loop to sense and then control the compensation parameter which is usually the voltage to a capacitor, but is sometimes the current to an inductor. Open-loop control methods calculate the control parameters based on system measurements, but do not use feedback from the output to adjust the control parameters.

4. **Reference signal generation**

   For APD systems, it is always the ripple power that is being compensated, but the ripple power is typically not tracked directly. It is usually tracked via measuring the ripple voltage, ripple current, AC voltage, AC current, or some combination of these. The general idea behind the reference signal generation is to recreate the harmonic(s) that are to be filtered out. Harmonic re-creation can be done directly by filtering one of the signals of interest or indirectly by calculating the harmonics based on other measurements in the system.

This section has provided a general overview of the considerations to address when designing an APD system. The following subsections will provide more details on different APD topologies, methods of reference signal generation, and methods of control.

2.5.3 Active Power Decoupling Topologies

This section will describe the various active decoupling topologies. The specific trade-offs that are necessary for each of the different methods of active decoupling will also be discussed.

2.5.3.1 Full Bridge Decoupling Ports

Double line frequency ripple power is sinusoidal and therefore the voltage and current are sinusoidal too. The most straightforward way to create an independent decoupling port is to create a full bridge circuit to control sinusoidal voltage/current to the energy storage device [6]. Figure 2.7 shows a full bridge decoupling port consisting of the four switches controlling the voltage to an LC circuit. The capacitor is the energy storage device while the small inductor ensures a smoother current. This circuit is essentially an inverter with a DC voltage (plus ripple) input and an AC voltage to the capacitor load. The difference is that the load does not use the energy, but stores it and releases it to counter the power ripple from the AC source of the AC-DC converter. The full bridge switches need to be controlled to match the power ripple; when the AC input power is positive, the decoupling port needs to accept and store the energy and when the AC input power is negative, the decoupling port needs to return energy to the DC load.

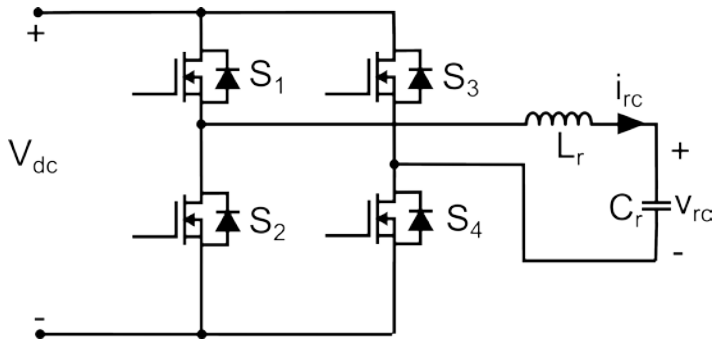

Figure 2.8. Full Bridge Decoupling Port

The switches (S1-S4) indicated in the diagram are shown as FETs, but could be any kind of controllable electronic switch (e.g., BJTs, or IGBTs).

Figure 2.8 shows the relationship between the power ripple and the (ideal) voltage and current to the decoupling port (note that this is a generalized relationship, so no values are used). The control system can be designed to directly follow the ripple power, or (more commonly) indirectly follow the ripple power by following the expected capacitor voltage (or current) that would match the capacitor power to the ripple power.

A limitation of this system is that the magnitude of the voltage to the decoupling port must be less than DC voltage in. This limitation is generally acceptable because if the DC voltage is high, the voltage to the decoupling port should not be higher for safety reasons. However, since being able to have a higher voltage means that the capacitance can be reduced even further, having an upper voltage limitation creates a lower capacitance limitation for the system.

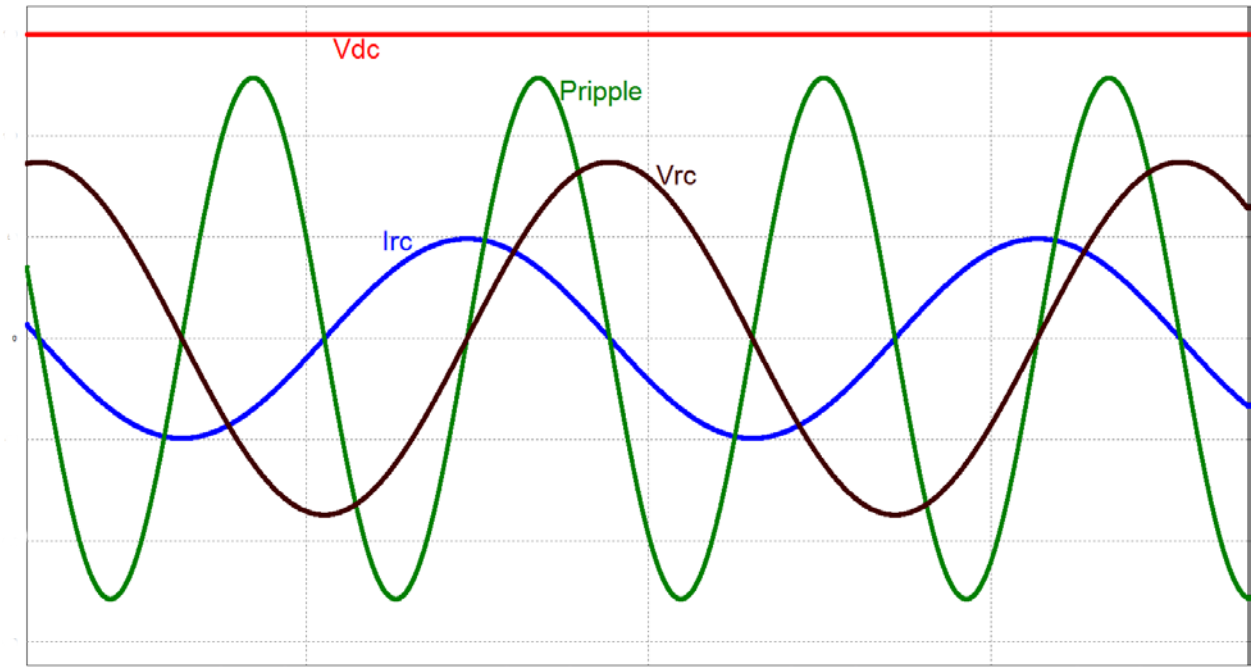

Figure 2.9. Full bridge decoupling port ripple power, decoupling port voltage and current

2.5.3.2 Buck, Boost and Buck-Boost Decoupling Ports

The operation of the full bridge decoupling port is fairly straightforward and simple to implement. The primary disadvantage of the circuit is that several new components are required, including four switches. These four switches introduce extra cost, require more space, and cause more power loss in the system. Several DC/DC converter structures for the decoupling port have been introduced [32], [43], [41] that follow the buck, boost and buck-boost converter configurations. These configurations also require extra switches, but the number of switches is reduced from four down to two. Just like the full bridge decoupling port, these decoupling ports store energy in a capacitor. Unlike the full bridge circuit, the voltage across the capacitor in these circuits is unipolar.

The buck decoupling port, as shown in Figure 2.9, requires that the magnitude of the voltage across the capacitor (v_{rc}) be less than the DC bus voltage (V_{dc}). The system will need to control the power to the decoupling port to match and cancel the ripple power, but must do so while keeping v_{rc} positive and less than V_{dc}. The resulting waveforms are shown in Figure 2.10 and indicate that voltage is always positive, but current flows in both directions. There are also discontinuities in the current and voltage flow which may contribute higher order harmonics to the system. The advantage of using only 2 switches instead of 4 will trump the discontinuity if the harmonics can be kept low enough to meet target specifications.

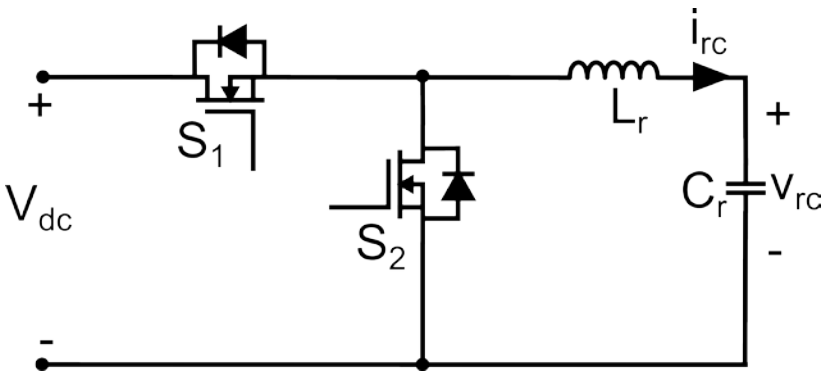

Figure 2.10. Buck Converter Based Decoupling Port

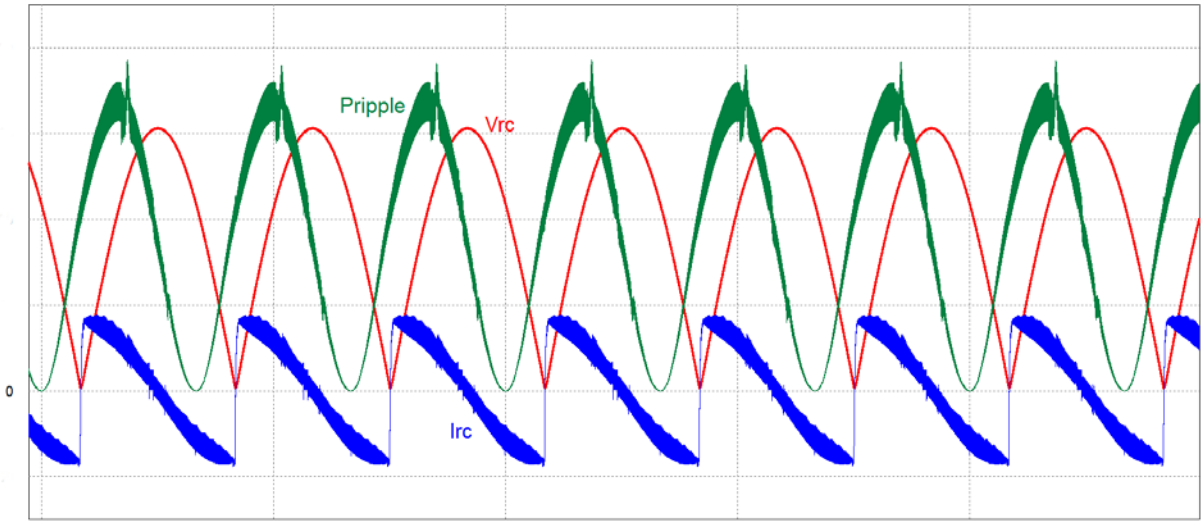

Figure 2.11 - Waveforms to Buck Based Decoupling Port

Boost converter based decoupling ports (shown in Figure 2.11) require the ripple port capacitor voltage (v_{rc}) to be higher than the DC bus voltage (V_{dc}) in order to operate correctly. This means that there will be extra, unused energy stored in the ripple port capacitor just like when using a DC bus capacitor. The difference in the boost converter decoupling port case is that because of the high voltage across the capacitor as well as the high ripple voltage allowed across the capacitor, the overall capacitance can be reduced.

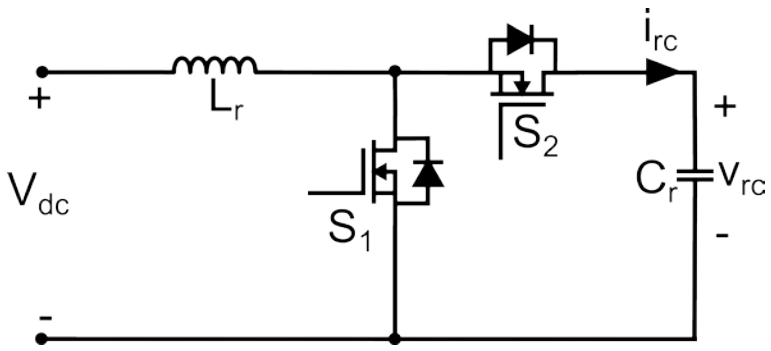

Figure 2.12. Boost Converter Based Decoupling Port

To show how the overall capacitance can be reduced, recall from (2-13) that the required capacitance for filtering double line frequency power ripple is approximately

$$C = \frac{P}{\omega V \Delta V}$$

Therefore the required DC bus capacitance would be:

$$C_{dc} = \frac{P_o}{\omega_{line} V_{dc} \Delta V_{dc}}$$

Similarly, the required ripple port bus capacitance would be:

$$C_r = \frac{P_o}{\omega_{line} V_{rc} \Delta V_{rc}}$$

Since the output power to be filtered, P_o, is the same in both equations, the capacitance reduction ratio would be

$$\frac{C_{dc}}{C_r} = \frac{V_{rc}\Delta V_{rc}}{V_{dc}\Delta V_{dc}} \quad \textbf{(2-17)}$$

For a DC bus capacitor, the value of V_{dc} is set by the required DC bus voltage and the value of ΔV_{dc} will be determined by the system requirements (and will typically need to be low: 1-10% of V_{dc}). Since those two values are set, there is no flexibility in selecting the capacitance.

On the other hand, if a boost converter based APD port is used, there is a lot of flexibility in selecting the average voltage (V_{rc}) and the ripple voltage (ΔV_{rc}) of the APD port. As long as $V_{rc} - \frac{\Delta V_{rc}}{2} > V_{dc}$, then the APD port will function correctly. At the same time, as long as V_{rc} and ΔV_{rc} are selected properly, a significant capacitance reduction can be obtained. For example, a 700W, 400V system operating at 60Hz that allows 2.5% peak-to-peak ripple would require a DC bus capacitor of 464μF. If a boost ripple port operating at an average voltage of 500V with a ripple of 100V peak-to-peak was used instead, then the capacitance could be reduced to 37.1uF. Using a boost converter based ripple port in this example, will reduce the required capacitance by a factor of 12.5.

The significant drawback is that the lowest voltage allowed at the ripple port must be higher than the DC voltage, (i.e., $V_{rc} - \frac{\Delta V_{rc}}{2} > V_{dc}$). Therefore, V_{rc} may be at such a high voltage as to make the ripple port a potential safety hazard and also put higher voltage stress on the decoupling components.

Figure 2.12 shows the voltage, current and power waveforms for a boost converter based ripple port. Note that the ripple voltage is always higher than the DC voltage. Also, note that the ripple current and power flow in both directions.

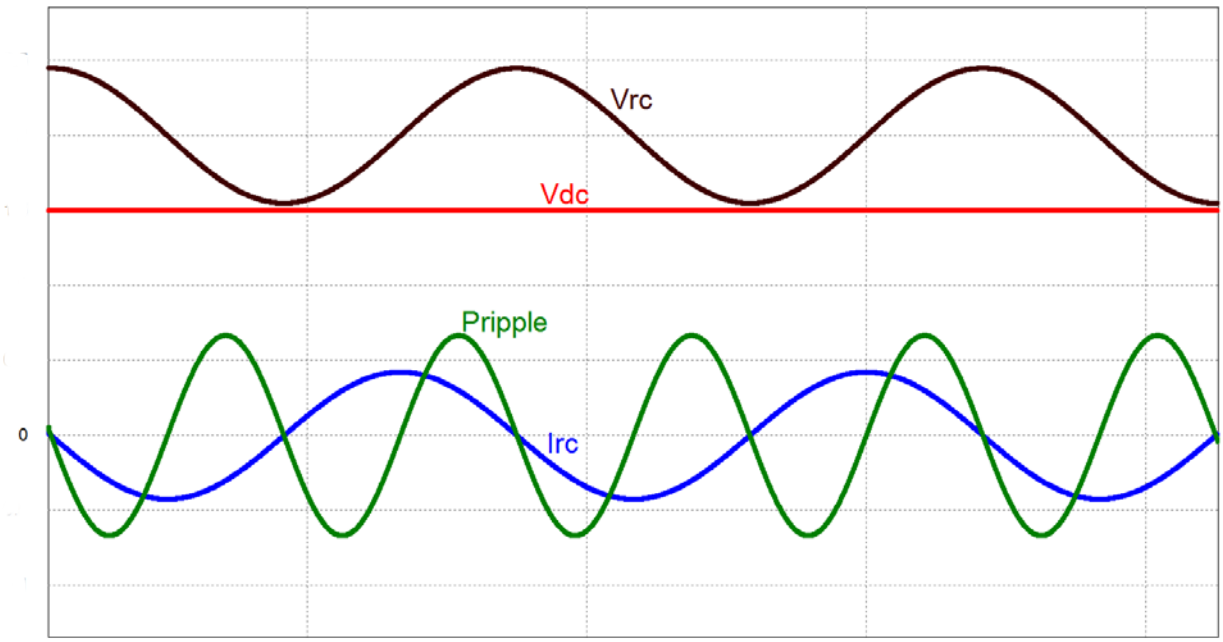

Figure 2.13 Waveforms to Boost Converter Based Decoupling Port

Buck-boost converter based decoupling ports (Figure 2.13) allow the ripple voltage to fluctuate above and/or below the DC voltage. This configuration can allow for further capacitance reduction when compared to either the buck based or the boost based decoupling ports because it can allow for an arbitrarily high average voltage while simultaneously allowing the instantaneous voltage to drop below the DC voltage. When referring back to eqn (2-13) , it can be noted that a high average voltage coupled with a high ripple voltage allows for high capacitance reduction. The buck-boost based decoupling ports do face the significant drawback of having discontinuous input and output currents so the reactive power is transferred indirectly from input to output.

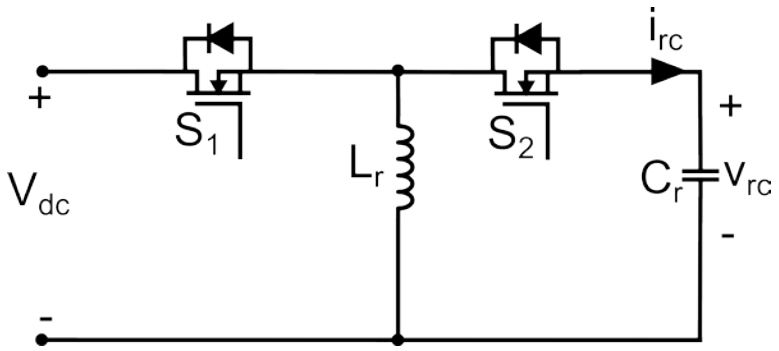

Figure 2.14. Buck-Boost Converter Based Decoupling Port

2.5.3.3 Split Capacitor Decoupling Ports

All of the circuits proposed in sections 2.6.3.1 and 2.6.3.2 reduce the required capacitance, but still require a DC bus capacitor to filter ripple with frequencies higher than twice the line frequency. The use of the DC bus capacitor indicates that decoupling is not fulfilled entirely by the decoupling port [43]. The decoupling port proposed in [44] uses split-capacitors in a symmetrical half-bridge circuit shown in Figure 2.14. This decoupling port not only supports the DC bus (so no extra DC bus capacitors are required), but also can be controlled to effectively absorb the ripple power.

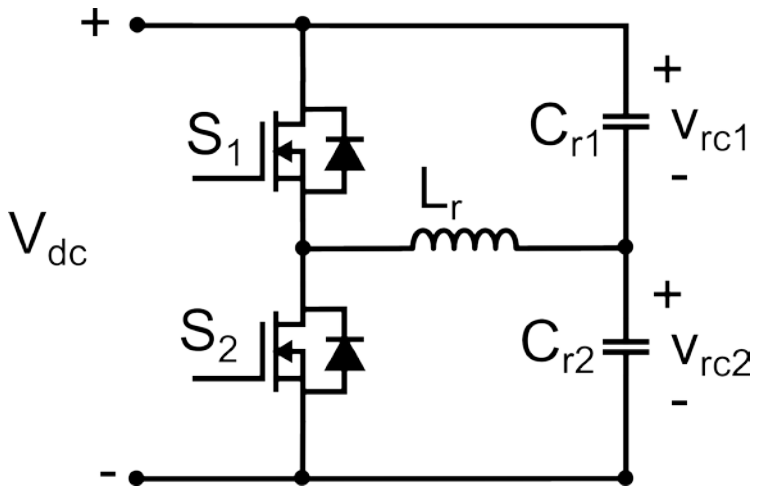

Figure 2.15 Split Capacitor Decoupling Port

As long as the two capacitor voltages are controlled according to these equations:

$$v_{rc1}(t) = \frac{V_{dc}}{2} + V_c sin(\omega t + \theta) \qquad \textbf{(2-18)}$$

$$v_{rc2}(t) = \frac{V_{dc}}{2} - V_c sin(\omega t + \theta)$$

the ripple power will be decoupled from the DC bus. Since each capacitor can be discharged to 0, energy storage capability of the capacitors can be maximized and capacitance can be minimized.

The control of this system requires that capacitors C_1 and C_2 be identical in value, otherwise tweaking of control parameters is required for each individual system. Also, the literature does not indicate the effectiveness of this system in filtering high frequency ripple. Considering that the voltage to the filtering capacitors is controlled to follow the double line frequency ripple, it seems likely that filtering of higher frequencies is limited.

2.5.3.4 Series Voltage Compensators

Wang et al. [30] proposed a series voltage compensator (Figure 2.15) to reduce the required decoupling capacitance. This compensator should not be considered a “port” since it is connected in series between the rectifier and load, but performs the same function as the previously discussed ports. The series compensator essentially creates a voltage to counter the voltage ripple and provide a ripple free DC voltage. The advantage of this system is that the voltage stresses will be very low when compared to the parallel decoupling ports. The proposal of Wang does have some significant disadvantages though, including high current stress, a requirement of four switches, two capacitors and two inductors, as well as DC offset to the capacitor resulting in limited capacitance reduction capability.

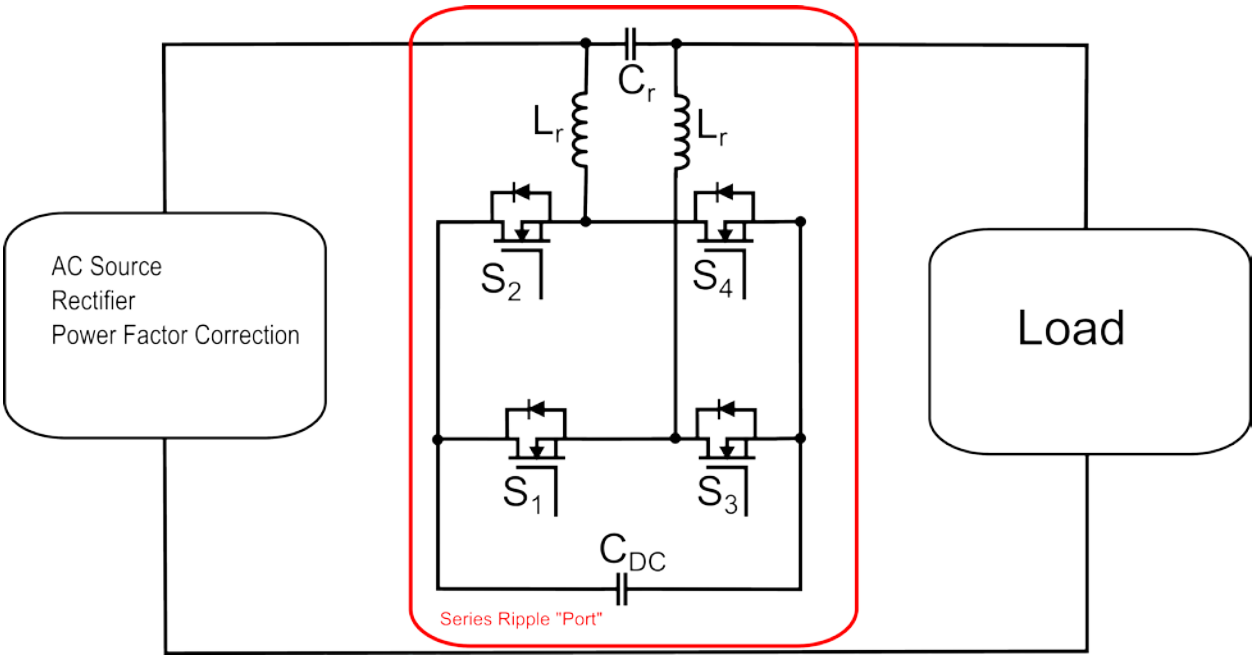

Figure 2.16. Series Decoupling Port

2.5.3.5 Dependent Decoupling Ports

Dependent decoupling ports can significantly reduce the required component count. Dependent decoupling ports have independent storage devices, but the control of energy flow to the storage devices is done using switches shared with the rectifier. Figure 2.16 shows an example dependent decoupling port circuit which includes the H-bridge rectifier. Switches S_1, S_2, S_3 and S_4 are the switches for the H-bridge rectifier to perform AC-DC conversion and power factor correction [45]. At the same time, switches S_3 and S_4 control the ripple power to C_{r1} and C_{r2} [28].

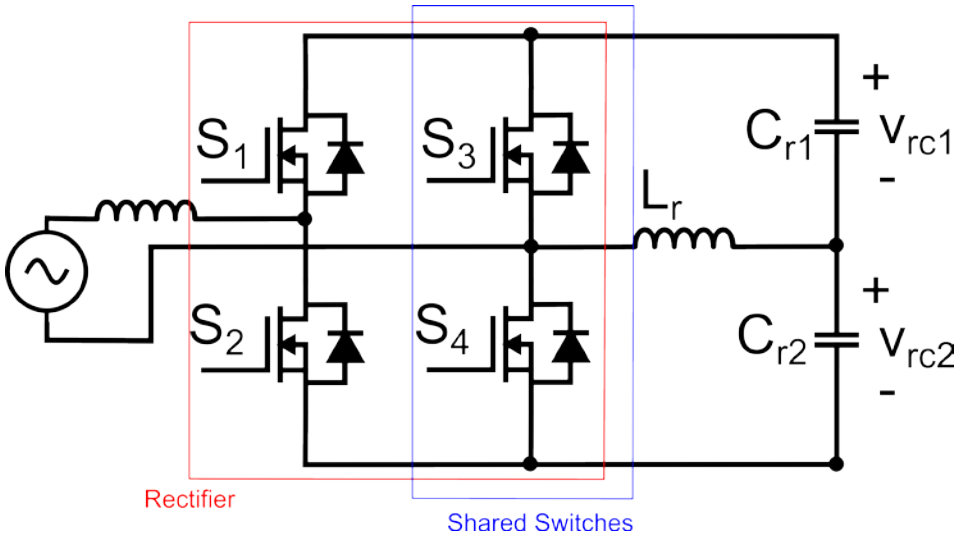

Figure 2.17. Dependent Split-Capacitor Decoupling Port

The obvious savings is that another set of switches is no longer required, so compared to the independent split-capacitor decoupling port, this circuit needs two fewer switches. On the other hand, because some of the switches are fulfilling two simultaneous functions, the control algorithms required can be significantly more complicated than independent decoupling ports.

2.5.4 Control Strategies for Active Power Decoupling

The purpose of this section is to discuss some of the strategies used to control the power to active power decoupling ports with the assumption that the control of the active power decoupling is done using active switches in the circuit. The two general methods of controlling power are open-loop control and closed-loop control. Open-loop control uses a calculation which may be predetermined or may be based on system parameter measurements to determine the switching (duty cycle, duration) of the control switches. Open-loop control is simple to implement because it does not use feedback from the decoupling circuit to ensure that the power is being decoupled correctly. Because of this simplicity, some of the literature ([31]) uses open-loop control to prove

the effectiveness of a topology. Closed-loop control systems use negative feedback loops and direct or indirect measurements of the active power to the decoupling port to control the decoupling port switches ensuring that the APD power matches the ripple power. Because of the superior performance and adaptability to changes in the system, most APD systems use closed loop control [6] , [28] - [41].

Open loop methods

Wang et al. in [31] split the ripple power cycle into charging (buck) and discharging (boost) phases and calculate a duty cycle based on measurements of the storage capacitor voltage and current, and DC voltage and current. In [47] a phase shifted version of the output AC voltage is created in an H bridge inverter ripple port which creates a simple system without feedback control.

Processing requirements may be reduced somewhat when compared to closed loop methods, but may still be significant. For example, in [31] a square root needs to be calculated every switching cycle. Also, while the control may be simpler, the required hardware is not; the number of sensors required often matches what would be needed in a closed loop system.

Closed Loop Methods

Closed loop control methods range from simple proportional control methods [48] to complicated multiple control loops with feed forward loops and specialized blocks (e.g., repetitive control) [47]. Some of the literature, such as [32] (which measures the ripple power and uses a PI controller to track it), simply uses a control method without justifying it (often because the focus of the paper is on topology, not control). Some of the literature does compare control methods. For example, [33] and [46] use a proportional resonant (PR) controller to get high gain at the resonant frequencies in order to minimize the steady state error. They also show

that PI control would not do this. Repetitive controllers [34], [47] are also shown to reduce steady-state error and do so with a limited bandwidth. The limitation of repetitive control is that it does not respond well to strong transients, but it has a strong advantage of being a plug-in solution [48]. In other words, it can be added to an already existing control system (e.g., PI controller).

More exotic control methods such as sliding mode control (SMC) have been shown to work effectively in AC-DC and DC-DC converters [49]-[51] due to their robustness in the presence of disturbances, fast dynamic response, wide operating range and simplicity of design. SMC has not yet been demonstrated in APD circuits, and since APD circuits can be based on DC-DC converters, there appears to be strong potential for investigation into using SMC in APD circuits.

2.5.5 Reference Signal Generation

Reference signal generation is required for closed-loop systems to give those systems a signal to track. The reference signal is typically the voltage and/or current harmonic(s) that need to be eliminated. This paper is only concerned with double-line frequency ripple[3], so it is only the second harmonic (of the input voltage or current) that needs to be eliminated. The second harmonic can be obtained by directly measuring the input AC voltage and/or current [36], by measuring and filtering the DC voltage and/or current [37], or by using some combination of AC and DC signals [52]. An alternative to calculating the second harmonic is proposed in [38] where the input AC voltage is measured and used directly as a reference. Instead of calculating the second harmonic, an analysis of the power flow to the energy storage capacitor indicates that to

[3] Higher frequency ripple will be handled by a small DC bus capacitor

decouple power, the capacitor voltage can track a phase shifted version of the AC voltage (see section 3.1 for more details).

2.5.6 Summary of Active Power Decoupling Considerations

Section 2.6.2 presents the motivation behind using an APD port in AC-DC converter circuits. Sections 2.6.3 to 2.6.5 discuss the advantages, disadvantages, and tradeoffs, necessary when deciding on a topology and control system for designing an APD port. To summarize the tradeoffs in topology selection, it is clear that unless there is a compelling reason, a full bridge APD port should be avoided to minimize component count. Going to the component count minimization extreme involves using a dependent port. Unless the designer has significant expertise with multi-modal control systems, dependent ports should also be avoided. Of the other three types of switch independent APD ports, the boost-based converter should be avoided unless high voltages are acceptable in the system and the buck-boost-based converter should be avoided unless it can be determined that the efficiency decrease is not significant. This summary suggests that the best choice for an APD port is a buck-based converter.

There is no clear specific winner when it comes to selecting a control system. The control should be closed loop for best performance, but there may be a trade-off between steady state error and circuit complexity.

A good compromise that features simplicity and performance is the control system proposed in [38]. The control is not discussed in detail, but the method of reference signal generation is simple and straight forward – the voltage of the APD port should follow a phase shifted version of the AC voltage. One thing that is required for that system though is direct measurement of the AC input voltage and current. In some systems, those signals would not be directly measurable.

The next section proposes a new APD methodology that allows control of an APD port in the manner of [38] and [39] while not requiring direct measurement of the AC voltage or current. The proposed system not only does not require direct measurement of the AC signals, but it can also relatively easily be dropped in to existing AC-DC converters.

The purpose of the proposed system in the next section is to create an APD port that does not require direct measurement of the AC voltage or current; the purpose is not to investigate the ideal control system. However, the next section does explore the possibility of using sliding mode control (which has not been investigated for APD circuits before) because of its potential as a simple and robust closed loop control methodology.

Chapter 3: Design of Active Power Decoupling System

As discussed in Chapter 2:, active power decoupling circuits can be effectively used to reduce or eliminate double-line frequency ripple while significantly reducing the required capacitance for energy storage. The active power decoupling circuit and control methodology proposed in [39] for a single phase PWM rectifier with PFC requires few components, a simple control system, has a power factor of 0.99, THD of less than 4% and voltage ripple of about 5%. It does require four switches though because it uses a full-bridge based power decoupling port. It is also limited to applications where the control system can directly measure the input AC voltage and current. If the AC and DC sides of the rectifier are isolated, or the AC side is not easily accessible, the system would not work because the control system on the DC side needs to measure the voltage and current on the AC side.

The purpose of this chapter is to first describe the theory behind the design of the APD system from [39], and second to explain how to improve that system by reducing component count, obtaining reference control signals without monitoring the AC side of the converter, and simplifying the control system. It should be noted that component count reduction was already described in [6] and in section 2.6.3.2, but has not been applied to AC-DC converters using the power decoupling method of [39].

The design of the proposed ripple port system requires designing the following three blocks:

1) The active power decoupling port which will consist of an energy storage capacitor and a buck based converter for managing energy flow to and from the capacitor
2) A bandpass filter for obtaining the voltage ripple from the DC side of the circuit
3) A control system for controlling the energy flow to and from the capacitor

3.1 Active Power Decoupling Theory

Section 1.2 describes the theory behind the need for a double line frequency filter, and eqn (1-3), which is repeated here, shows mathematically the split of the AC power into average power plus ripple power:

$$p_{ac}(t) = \frac{V_p I_p}{2} cos(\varphi) + \frac{V_p I_p}{2} cos(2\omega t - \varphi)$$

V_p and I_p represent the peak voltage and current of the AC signal, φ represents the phase difference between AC voltage and current and ω represents the frequency of the AC voltage in radians/second. For simplicity, the output power (i.e., the power to DC load which is the same as the average power) is designated as P_o and is set to

$$P_o = \frac{V_p I_p}{2} \quad \textbf{(3-1)}$$

So eqn (1-4) can be re-written as

$$p_{ac}(t) = P_o cos(\varphi) + P_o cos(2\omega t - \varphi) \quad \textbf{(3-2)}$$

The physical manifestation of eqn (3-2) in an AC-DC converter with an APD port, is illustrated in Figure 3.1 (this figure assumes that the power factor is 1 (so φ is 0)). The power produced by that AC source is $p_{ac}(t)$ and ideally, the DC load will receive the average power $\left(P_o cos(\varphi)\right)$ while the APD port will receive the ripple power $\left(P_o cos(2\omega t - \varphi)\right)$.

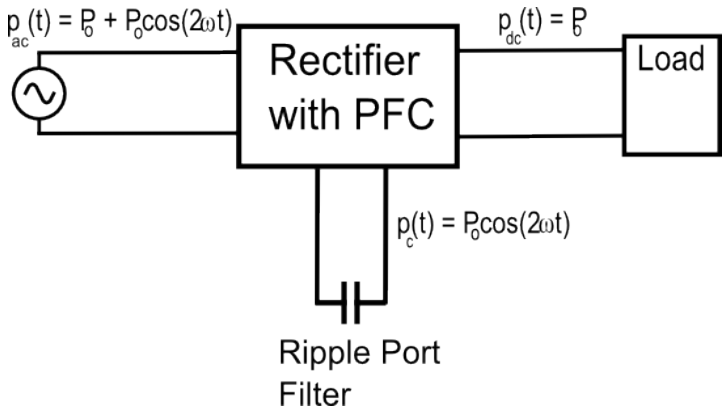

Figure 3.1. Power in AC-DC Converter with Ripple Port

When the APD port uses a capacitor for energy storage/filtering, the time varying power to the capacitor can be determined from the voltage across $\left(v_c(t)\right)$ and current through $\left(i_c(t)\right)$ the capacitor as illustrated in the following equations [6]:

$$v_c(t) = V_c cos(\omega t + \theta) \quad \textbf{(3-3)}$$

$$i_c(t) = C\frac{dv_c(t)}{dt} = -C\omega V_c sin(\omega t + \theta) \quad \textbf{(3-4)}$$

$$p_c(t) = v_c(t)i_c(t) = -\frac{\omega C{V_c}^2}{2} sin(2\omega t + 2\theta) \quad \textbf{(3-5)}$$

For the APD port to work perfectly, the power to the capacitor needs to be equal to the ripple power of eqn. (3-2):

$$p_c(t) = -\frac{\omega C{V_c}^2}{2} sin(2\omega t + 2\theta) = P_o cos(2\omega t - \varphi) \quad \textbf{(3-6)}$$

Eqn (3-6) can be split into the magnitude portion and the time varying portion and as long as the two magnitude portions are equal and the two time varying portions are equal, the capacitor power will match the ripple power.

First, examining the magnitude portions of eqn (3-6) requires

$$\frac{\omega C {V_c}^2}{2} = P_o \quad \textbf{(3-7)}$$

Since the capacitor voltage will be the characteristic to control, V_c, needs to be

$$V_c = \sqrt{\frac{2P_o}{\omega C}} \quad \textbf{(3-8)}$$

Second, examining the time varying portions of eqn (3-6) requires

$$-sin(2\omega t + 2\theta) = cos(2\omega t - \varphi) \quad \textbf{(3-9)}$$

The only unknown in eqn (3-9) is θ, which is the phase shift of the capacitor voltage with respect to the AC voltage. Solving eqn (3-9) for θ gives:

$$sin(-2\omega t - 2\theta) = \cos(2\omega t - \varphi)$$

$$cos\left(-2\omega t - 2\theta - \frac{\pi}{2}\right) = \cos(2\omega t - \varphi)$$

$$cos\left(2\omega t + 2\theta + \frac{\pi}{2}\right) = \cos(2\omega t - \varphi)$$

$$2\omega t + 2\theta + \frac{\pi}{2} = 2\omega t - \varphi$$

$$\theta = -\frac{\varphi}{2} - \frac{\pi}{4} \quad \textbf{(3-10)}$$

And if the power factor is 1:

$$\theta = -\frac{\pi}{4} \quad \textbf{(3-11)}$$

Equations (3-8) and (3-11) indicate that if the voltage across the ripple port capacitor is maintained at an amplitude of $\sqrt{\frac{2P_o}{\omega C}}$ and is phase shifted by -45° with respect to the AC voltage, then the APD port will fully decouple the ripple power from the DC load.

$$v_c(t) = \sqrt{\frac{2P_o}{\omega C}} cos\left(\omega t - \frac{\pi}{4}\right) \quad \textbf{(3-12)}$$

This APD method was first proposed in [40] and then expanded upon in [6], [39] and [38]. Harb and Balog in [39] use a full-bridge APD port (like the one in Figure 2.7) on a PFC AC-DC converter and control the voltage to the APD port according to eqn (3-12).

A simple improvement to this circuit is to replace the four switch full-bridge circuit with a two switch buck-based converter (see Figure 2.9). The voltage to the capacitor of the APD port will no longer be able to go negative, which means that the capacitor voltage will no longer follow eqn (3-12). However, modifying the control signal ($v_c(t)$) by rectifying it allows for the power to the APD to still match the ripple power.

$$v_c(t) = \left|\sqrt{\frac{2P_o}{\omega C}} cos\left(\omega t - \frac{\pi}{4}\right)\right| \quad \textbf{(3-13)}$$

3.2 The Benchmark Boost Power Factor Correction Circuit

A benchmark system is required against which the proposed system can be judged. The benchmark PFC circuit for this project is a 700W, 400V system with 170V_p input. The schematic of this circuit can be seen in Figure 3.2. One important thing of note is that the ripple capacitor in the DC output is a 300uF capacitor, and it is this capacitor that will be replaced by the proposed ripple port circuit.

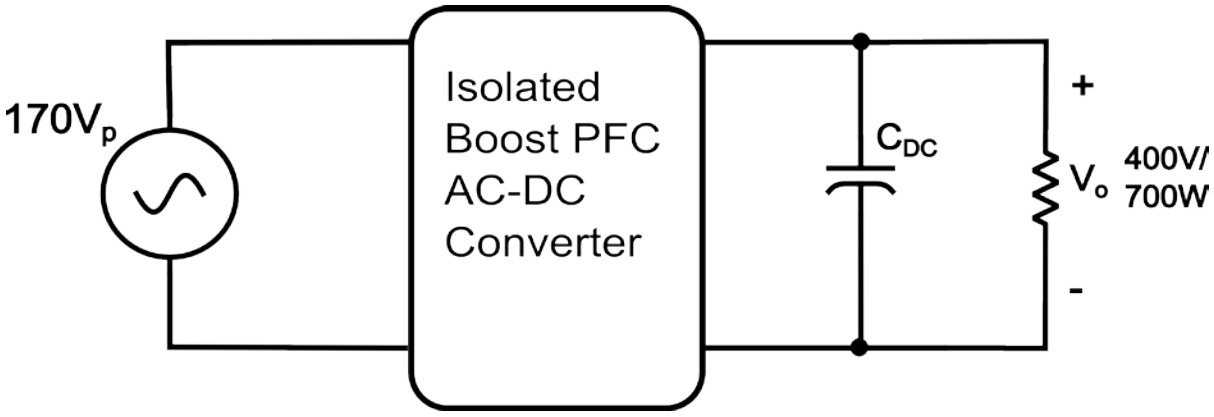

Figure 3.2 Nominal Boost PFC AC-DC Converter

3.3 Active Power Decoupling Port Circuit

The proposed power decoupling port circuit is a buck-based port placed in parallel with the DC bus. A buck converter based circuit was chosen to minimize the number of switches required and it was chosen over a boost-converter based system to keep the voltage of the decoupling port less than the voltage of the DC bus. The DC bus is at 400V, so if a boost-converter based system was used, the average voltage would need to be higher than 400V and the peak voltage would need to be much higher. Voltages that high would require safety considerations beyond what is needed for the 400V bus. The trade-off with using a buck-converter based system is that the capacitance cannot be reduced as low as it could be with a boost converter based circuit. The higher voltage of the boost based system allows capacitance to be reduced even more than what a buck based system can do.

The buck-based system is essentially a buck converter without a resistive load. The load is instead a capacitor which acts as the energy storage device. Other components required are synchronous switches for controlling current to the capacitor, and an inductor for keeping current flow continuous. The circuit schematic is shown in Figure 3.3.

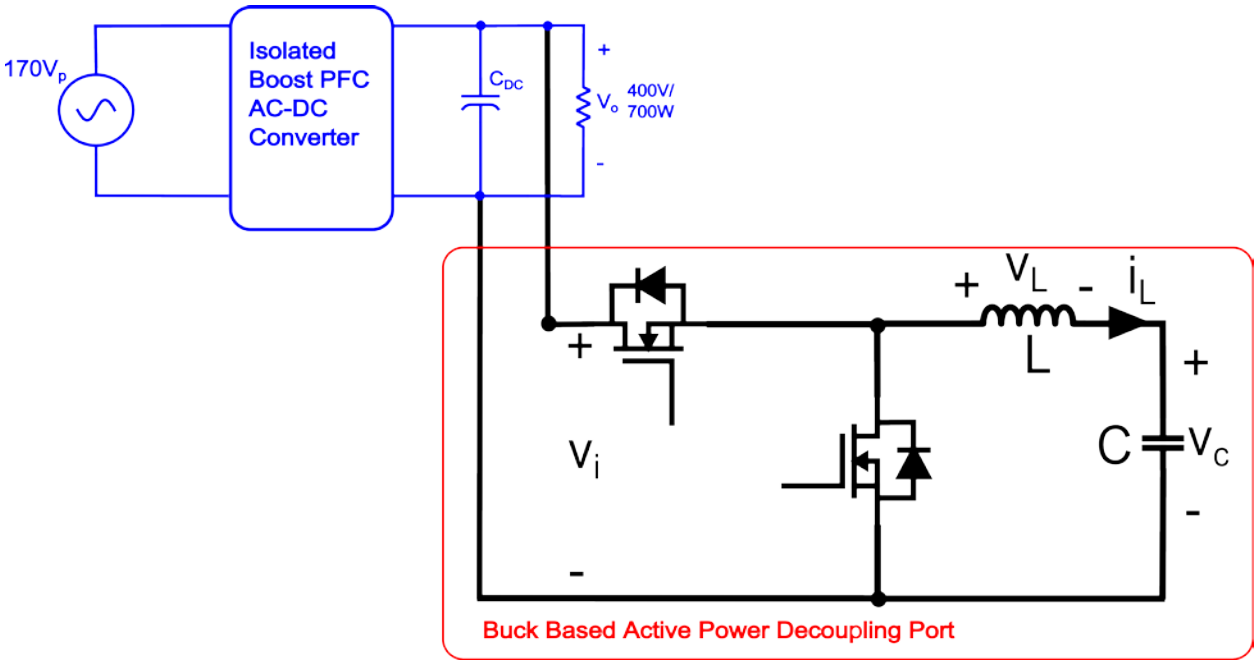

Figure 3.3 Ripple Port Connected to Boost PFC AC-DC Converter

Figure 3.3 shows the topology of the active power decoupling port circuit, but two design criteria that still need to be considered are the capacitance required for the capacitor and the inductance required for the inductor.

3.3.1 Capacitance Selection

As derived in section 3.1, the double line frequency ripple will be filtered by the ripple port when the peak of the ripple power and the peak of the power to the ripple port capacitor are equal. This relationship gives the relationship between capacitance, capacitor voltage and output power as follows:

$$C = \frac{2P_o}{\omega V_c^2} \quad \textbf{(3-14)}$$

where C is the capacitance, P_o is the peak ripple power (also the DC power), ω is the line frequency (not the double-line frequency), and V_C is the peak capacitor voltage. Assuming the

peak output power is 700W and the line frequency is $120\pi\ {}^{rad}/_{s}$, then the relationship between capacitance and peak capacitor voltage that would, in theory, fully decouple the ripple power is

$$C = \frac{3.71}{V_c^2} \quad \textbf{(3-15)}$$

This relationship is plotted in Figure 3.4.

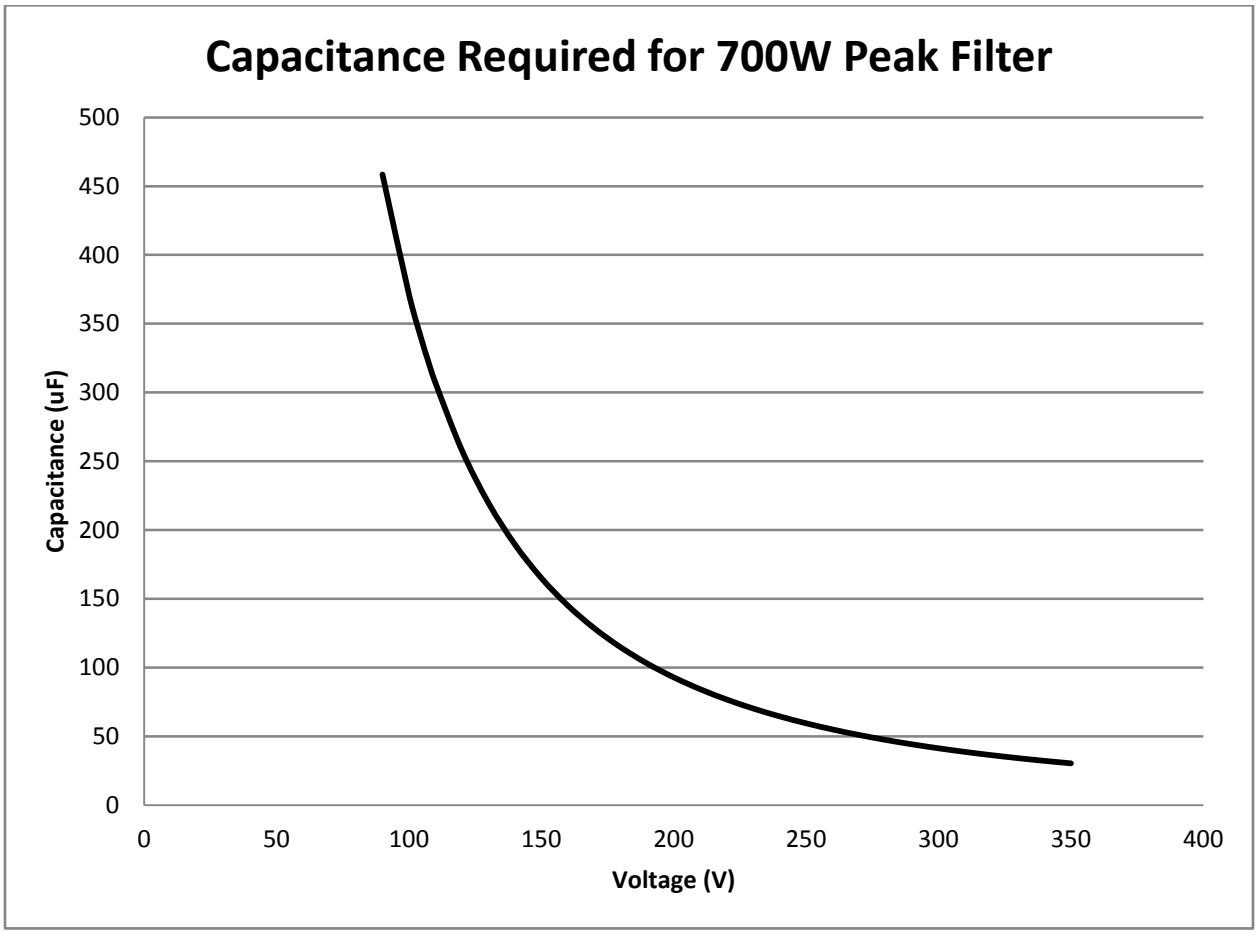

Figure 3.4 Capacitance Required as a Function of Capacitor Voltage

This graph shows that the higher voltage across the capacitor is, the lower the required capacitance is. There are diminishing returns though; as the voltage increases, the rate of

decrease in capacitance goes down. A balance must be struck between a low enough capacitance to justify changing from an Al e-cap to a film cap and a low enough voltage to keep the system safe. Since the ripple port is based on a buck converter circuit, the maximum voltage to the capacitor is always going to be lower than the DC bus voltage.

A voltage of 325V for the peak capacitor voltage is a good maximum to set because it allows for 75V of voltage margin from the maximum allowable (~400V). Using this maximum suggested voltage of 325V allows for a fairly low capacitance of 35 μF to be used. This is a reduction in capacitance by a factor of 8.6 compared to the nominal circuit with the DC filter capacitor. While 35 μF is the lowest the capacitance will be able to go in this system, other capacitances will also be tested to compare the effects.

Table 3.1 selects a few specific points based on eqn (3-12)

Table 3.1. Voltage-Capacitance Relationship for Active Decoupling Port

Capacitance	Voltage Peak Required
35uF	325V
40uF	300V
55uF	260V
75uF	222V
80uF	215V

3.3.2 Inductance Selection

While this design is for simulation only, some attention should be paid to real world factors such as the maximum and RMS current that will go through the inductor. In simulation, these

parameters will not have an effect on inductor selection, but could limit the selection of off-the-shelf inductors that could be used for a real system. Custom inductors could be designed, but that would increase the cost of this cost sensitive system.

The maximum inductor current of the system is important to know because the rated saturation current of the chosen inductor must be higher than the maximum inductor current to prevent the inductor core from reaching saturation. The RMS inductor current is also important to know in order to calculate power dissipated by the inductor through I^2R heating. Several inductances were tested in simulation to determine maximum and RMS current through the inductor as the ripple port was in operation. The maximum current and the RMS current were measured in the simulation with several different values of inductance and Table 3.2 shows the results of these tests.

Table 3.2 Maximum and RMS Inductor Currents using Different Inductances

Inductance	Max Current (Sim)	RMS Current (Sim)
100μH	6A	3.3A
200μH	5.25A	2.86A
300μH	4.6A	2.83A
400μH	4.5A	2.8A
470μH	4.25A	2.8A

Performing a cursory component search on Digikey's website indicates that there are 2 or 3 families of inductors that would fit the inductance and current requirements indicated by Table 3.2. A 470uH inductor will be used for the ripple port because it gives a lower maximum and RMS current and would be easy to obtain for a physical circuit if required.

3.3.3 Active Power Decoupling Port Circuit Design Summary

In summary, a buck converter based active power decoupling port will be designed and added to a 700W/400V AC-DC converter with Boost PFC. The APD port will use a 470µH inductor and a 35-75µF capacitor for energy storage. The overall circuit appears in Figure 3.5.

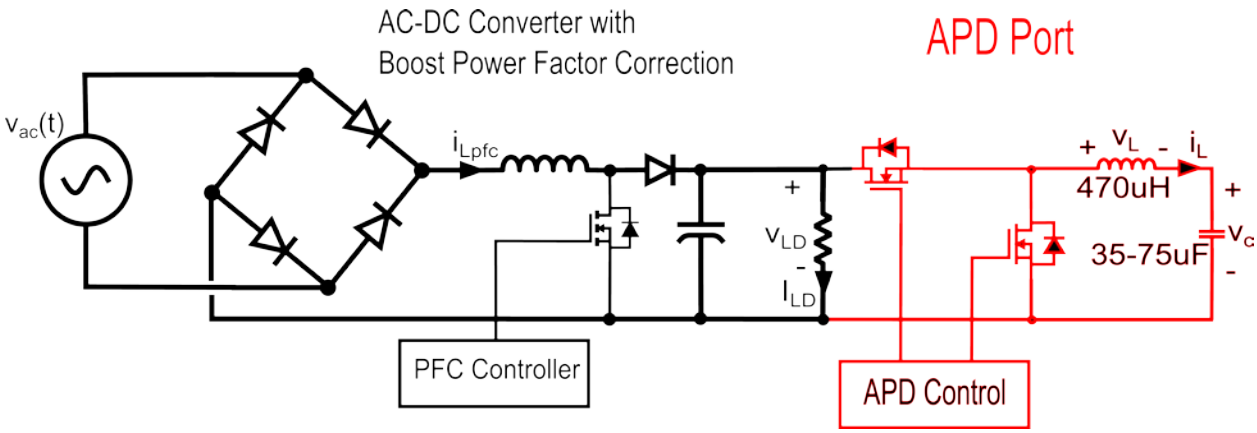

Figure 3.5 Boost PFC Circuit with APD Port

The next step in the system design process is to determine and create a method to control the voltage (and power ripple) to the APD. The following sections will describe how the reference signal for the control will be generated and how the voltage to the APD port will be controlled to match the reference.

3.4 Reference Signal Generation

The control system needs to track a phase shifted version of the input AC voltage. The simplest way to do this is to measure the input voltage directly. If the AC voltage is as shown in figure Figure 3.6, then the system could measure that signal and generate the reference signal which is phase shifted by 45° from the AC voltage (*Vshifted*) as shown in Figure 3.7.

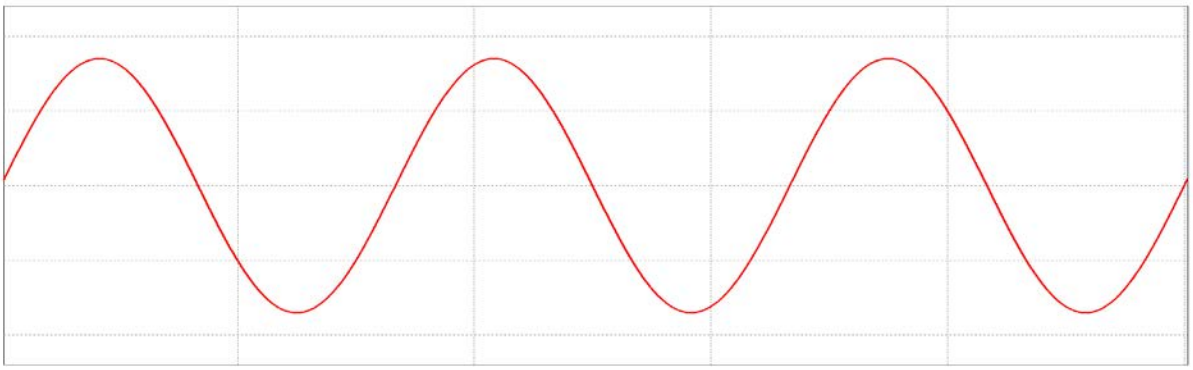

Figure 3.6 Vac

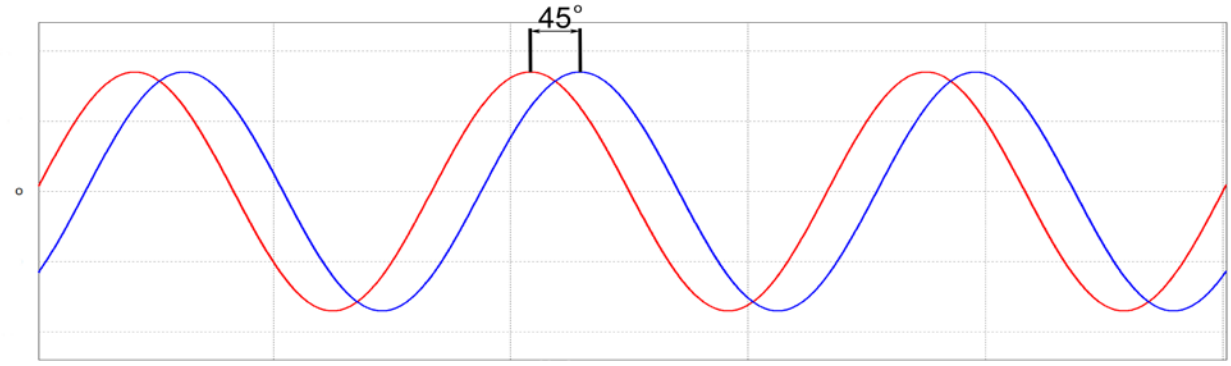

Figure 3.7 Vac plus Signal Phase Shifted By 45°

A limitation on the proposed system is that it cannot directly measure the AC voltage. Instead of measuring the AC voltage directly, the frequency and phase of the input voltage must be obtained indirectly from the ripple in the DC voltage.

Figure 3.8 shows the DC output of a boost power factor correction circuit. The output voltage is at 400V and includes the double line frequency ripple (in the figure, the scale is arbitrary to allow for better illustration of the ripple).

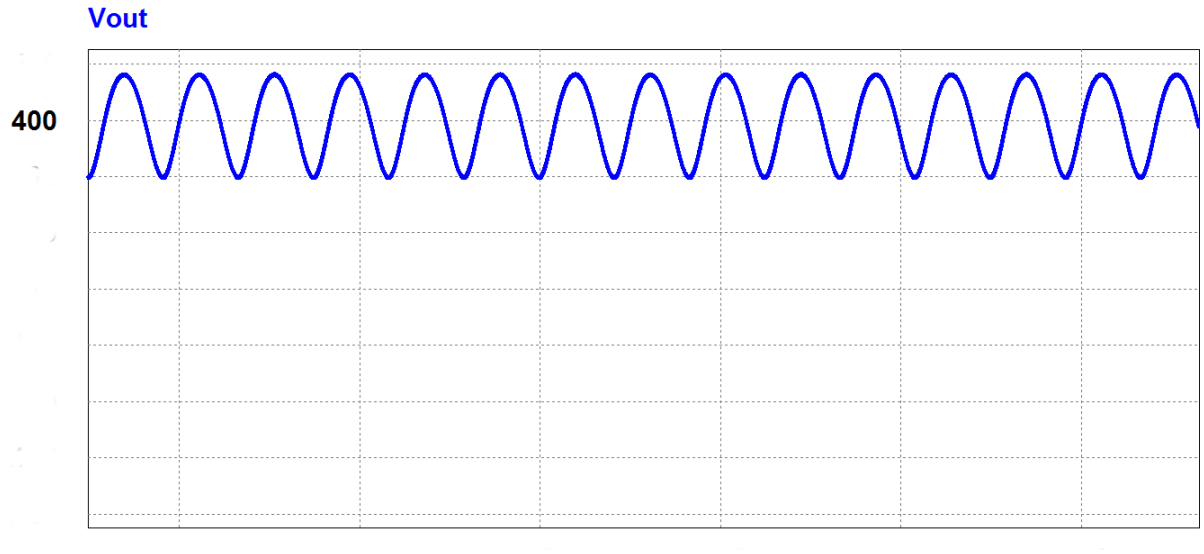

Figure 3.8. DC Voltage with Ripple

This voltage will be used to generate the reference signal by filtering it to obtain the 120Hz double line frequency signal, dividing the frequency in half to recreate the 60 Hz signal, phase shifting the signal the appropriate amount, and then multiplying the new 60 Hz sine wave by the required amplitude. The functional blocks to create the reference signal from the DC output are illustrated in Figure 3.9.

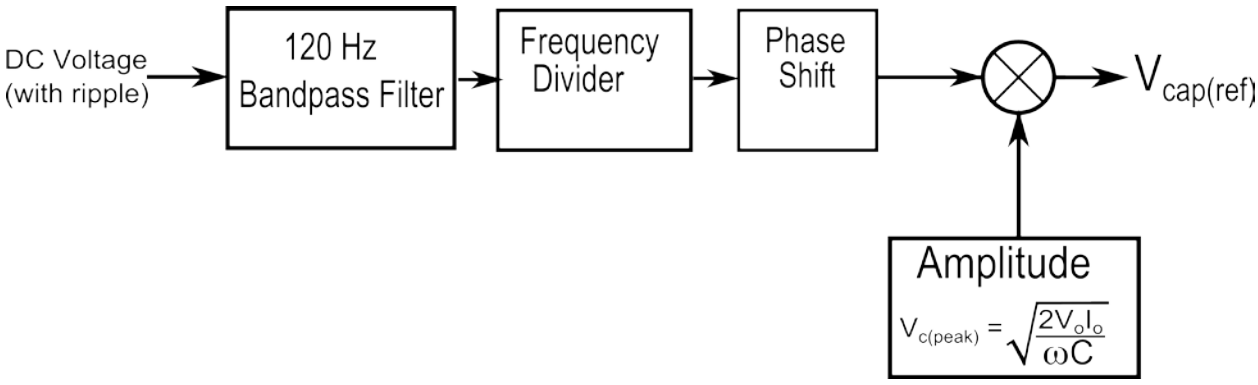

Figure 3.9. Block Diagram for Creation of Capacitor Voltage Reference

The next subsections, 3.4.1 and 3.4.2 provide details about each of the blocks from Figure 3.9.

3.4.1 120 Hertz Bandpass Filter

The center frequency of the bandpass filter is set at the double-line frequency. For this system, the line frequency will be be 60 Hz, so the double-line frequency will be 120 Hz. The bandpass filter is intended to be implemented in the digital realm, and for simulation purposes is done in PSIM. The bandpass filter only needs to generate a sine wave that has consistent zero crossings because these zero crossings are what will be used by the frequency divider to recreate the 60Hz signal. A simple filter that will generate consistent zero crossings can be created from a resonant filter [41].

The general form of the transfer function of a resonant filter is shown in eqn (3-16)

$$H_R(s) = \frac{K_r \frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + {\omega_0}^2} \quad \textbf{(3-16)}$$

K_r is the gain of the transfer function, ω_0 is the resonant frequency, and Q is the quality factor. The quality factor is defined as

$$Q = \frac{\omega_0}{Bandwidth} \quad \textbf{(3-17)}$$

In order to select for only the frequency of interest, Q should be set as high as possible. Lenwari et al [53] suggest using a Q greater than 7000 to ensure zero steady state error, however, that application was to use the resonant filter as part of a PR compensator where it was required to make steady state error as low as possible. Cao et al [41] suggest using a Q between 25 and 50 and a gain (K_r) of 1 for filtering ripple current for an APD of an AC-DC converter. Using $Q = 50$, $K_r = 1$ at the resonant frequency of 120Hz creates a resonant bandpass filter transfer function of

$$H_R(s) = \frac{30.16s}{s^2 + 15.08s + 568490} \quad \textbf{(3-18)}$$

A filter with the transfer function of eqn (3-18) will be used to obtain the 120 Hz ripple.

3.4.2 Frequency Divider, Phase Shift and Reference Sinusoid Generation

The frequency divider is used to regenerate a sinusoidal signal that is phase matched to the original AC voltage. The frequency divider accepts the ripple signal from the bandpass filter and detects positive to negative zero crossings using a comparator and D flip flop set up in toggle mode. The result is a 60 Hz square wave.

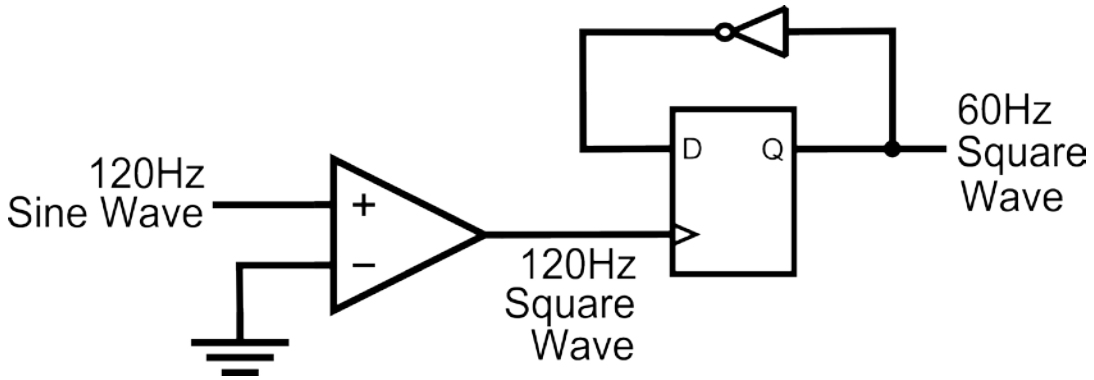

Figure 3.10 Frequency Divider Circuit

This square wave is used to regenerate the 60 Hz sine wave by triggering the generation of a sine wave from a wavetable. An arbitrary phase shift is added to the generated sine wave to create the reference sinusoid with the required phase shift.

The amplitude of the reference sinusoid is determined from the output power, the line frequency and the ripple port capacitor size as described by eqn (3-14) which is rearranged here so that it is in terms of the capacitor voltage:

$$V_{cap(ref)} = \sqrt{\frac{V_o I_o}{\omega C}}$$

This voltage is the peak of the reference voltage, and since it varies with power, it needs to be recalculated periodically based on the sampled output voltage (V_o) and current (I_o). The sample period can be the same sample period as the other sensor values.

3.5 Controller Design

Conventional pulse width modulation (PWM) controllers used in power electronics operate on a small-signal model of the plant and therefore operate most effectively within a small operating range [54]. Since the voltage to the energy storage capacitor of the ripple port will vary widely and continuously, a control system that tolerates a wide range of system values should be used. Sliding mode controllers (SMC) are non-linear controllers which have high levels of stability, are robust in system uncertainties (e.g., changing line and load) and are relatively easy to implement [55]. SMCs operate very well on systems whose structures are variable and DC-DC converters have inherently variable structures as the switches open and close which make them good candidates for SMC. The ripple port described in section 3.5.1 illustrates the variable structure of DC-DC converters quite well. The structure of the system alternates between two forms; one when switch S1 is closed and S2 is open and the one when switch S1 is open and S2 is closed. Conventional design attempts to take an average of the system states when developing the system model, but SMCs use the two individual states directly in the model. The following sections develop the equations that represent the two states of the ripple port filter, outline the general principles of SMC, and then show how to design a sliding mode controlled PID system for an APD port.

3.5.1 Buck-Based Active Power Decoupling Port Equations

In order to design the control system, a mathematical model of the system being controlled needs to be created. Creation of the mathematical model begins by analyzing the circuit, and in this case, the circuit to be controlled is the APD circuit shown in Figure 3.11:

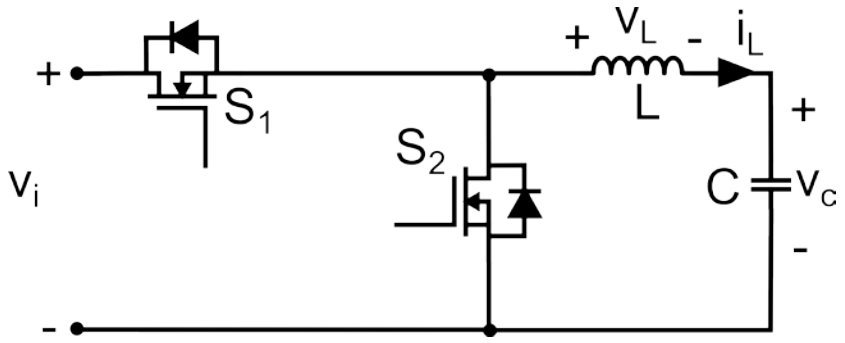

Figure 3.11 Ripple Port Circuit

This APD circuit is like a buck converter except that the load is the capacitor. The state space equations for the APD circuit are derived next.

S1 Closed/S2 Open:

The first state for the ripple port circuit occurs when S_1 is closed and S_2 is open as shown in Figure 3.12. In this state, the input voltage (v_i) is applied across the inductor and the capacitor $(v_L + v_c)$.

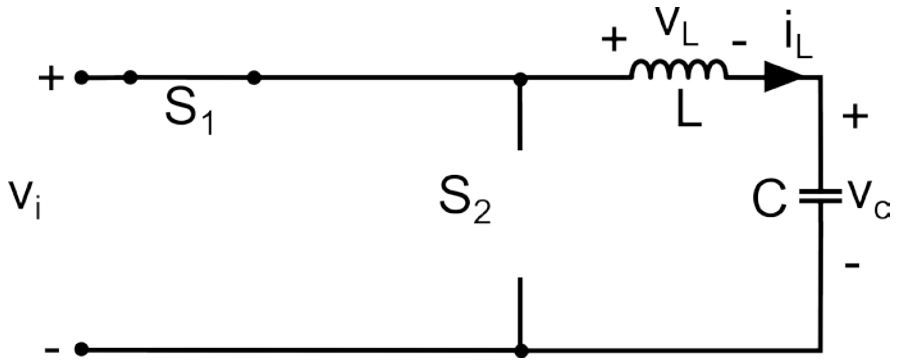

Figure 3.12 Ripple Port Circuit. S_1 Closed, S_2 Open

The equations for inductor voltage and capacitor current in this circuit state are as follows:

$$v_L = v_i - v_c = L\frac{di_L}{dt} \quad \textbf{(3-19)}$$

Rearranging to solve for $\frac{di_L}{dt}$ gives;

$$\frac{di_L}{dt} = \frac{V_i}{L} - \frac{v_c}{L} \quad \textbf{(3-20)}$$

The current through the capacitor is the same as the current through the inductor:

$$i_C = i_L = C\frac{dv_c}{dt} \quad \textbf{(3-21)}$$

Rearranging to solve for $\frac{dv_c}{dt}$ gives:

$$\frac{dv_c}{dt} = \frac{i_L}{C} \quad \textbf{(3-22)}$$

Combining equations (3-20) and (3-22) into matrix form gives

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{V_i}{L} \end{bmatrix} \quad \textbf{(3-23)}$$

S2 Closed/S1 Open:

The second state of the ripple port circuit occurs when S2 is closed and S1 is open as shown in Figure 3.13.

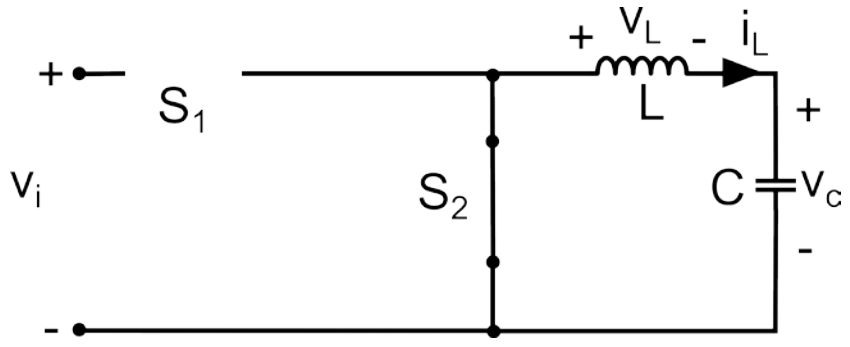

Figure 3.13 Ripple Port Circuit. S1 Open, S2 Closed

The voltage across the capacitor can be described by equation (3-24):

$$v_L = -v_c = L\frac{di_L}{dt} \quad \textbf{(3-24)}$$

Rearranging for $\frac{di_L}{dt}$ gives:

$$\frac{di_L}{dt} = -\frac{v_c}{L} \quad \textbf{(3-25)}$$

The current through the inductor can be described by equation (3-26)

$$i_C = i_L = C\frac{dv_c}{dt} \quad \textbf{(3-26)}$$

Rearranging for $\frac{dv_c}{dt}$ gives:

$$\frac{dv_c}{dt} = \frac{i_L}{C} \quad \textbf{(3-27)}$$

Combining equations (3-25) and (3-27) into matrix form gives

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \quad \textbf{(3-28)}$$

As the ripple port operates, it switches between the states described by equation (3-23) and equation (3-28). The two equations can be combined by adding the variable u which is equal to 1 for the state described by equation (3-23) and is equal to 0 for the state described by equation (3-28). The resulting equation is then:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{V_i}{L} \end{bmatrix} u \quad \textbf{(3-29)}$$

which describes the operation of the ripple port circuit in both switching states.

The goal now is to control the system, specifically v_c in this case, so that it actively removes the double line frequency ripple from the DC side of the PFC circuit. Sliding mode control has been chosen for this task for the reasons outlined in the beginning of section 3.5.The next sections will describe the basic ideas of sliding mode control and then develop the sliding mode control system for controlling the v_c of the ripple port circuit.

3.5.2 General Sliding Mode Control Principles

The basic principle of SMC is to define the system in terms of state variables of the system, develop a control law that will direct the state variables towards the desired point (i.e., capacitor voltage tracking the reference), and then combine these two elements into an equation defining the trajectory of the state variables of the system. The equation for the state variable trajectory of a second order system is given by:

$$S = \alpha_1 x_1 + \alpha_2 x_2 + a_3 x_3 \quad \textbf{(3-30)}$$

where x_1, x_2, and x_3 are the state feedback variables to be controlled and α_1, α_2, and α_3 are the control parameters and are generally referred to as the sliding coefficients. Control of the system is obtained by forcing S toward 0 which mathematically creates a sliding plane, or sliding surface along which the feedback variables can move to force S toward 0.

In two state systems (such as the buck-based ripple port), the control law is

$$u = \frac{1}{2}[1 + sign(S)] \quad \textbf{(3-31)}$$

where u (which is the same u as in eqn (3-29)) determines which state the system is in. In an ideal SMC system, the switching frequency for u would approach infinity to ensure that S is always at 0, however since power electronic circuits have a finite switching frequency, sliding

mode controllers for DC-DC converters are considered quasi-SMC. The nature of SMC systems causes the switching frequency to be variable, but this variable switching frequency makes the design of input and output filters in power electronic systems complicated [50]. In order to make the frequency fixed, the design method discussed in [56] will be used to create a PWM controller based on sliding mode voltage control.

The design of a sliding mode controller involves selection of the sliding coefficients so that a number of conditions are met [57]. The first condition is called the hitting condition which states that regardless of the initial values of the state variables, the system will move towards the sliding surface. In [51] it is shown that the hitting condition is met for all basic DC-DC converters using sliding surface and the control law defined in equations (3-30) and (3-31). The second condition to be met is the existence condition which states that when the state variables are very close to the sliding surface then the state trajectory must be directed toward the sliding surface. In other words, the existence condition states that the system must be directed towards equilibrium when it is close to equilibrium. The existence condition is met by selecting the appropriate sliding coefficients to ensure that:

$$\lim_{S \to 0} S \cdot \dot{S} < 0 \qquad \textbf{(3-32)}$$

where $\dot{S}$ is the time derivative of S.

The final condition that must be met is the stability condition and this condition is easily met if the designer selects the sliding coefficients to not only meet the existence condition but to also meet specific system responses (i.e., underdamped, critically damped or overdamped with specific desired convergence rate) [51].

Section 3.5.3 will show how to derive the sliding coefficients in order to meet the existence and stability conditions.

3.5.3 Designing a Sliding Mode Voltage Controlled PID

The purpose of the control system for the ripple port circuit is to control the voltage across the capacitor so that it follows a phase shifted version of the AC input voltage. The SMC based controller will be a PID sliding mode voltage controller like in [56], and as such, the state variables are:

$$\begin{aligned} x_1 &= V_{ref} - \beta v_c \\ x_2 &= \frac{dx_1}{dt} = \frac{d(V_{ref} - \beta v_c)}{dt} = -\beta \frac{dv_c}{dt} = \frac{-\beta}{C} i_L \\ x_3 &= \int x_1 dt \end{aligned} \quad \textbf{(3-33)}$$

Where x_1 is the voltage error, x_2 is the rate of change of the error, x_3 is the integral of the voltage error, and β is the scaling factor applied to the output/capacitor voltage (v_c)

Creating a vector, $\vec{x}$, using the state variables from eqn 3-33 gives:

$$\vec{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} V_{ref} - \beta v_c \\ \dfrac{d(V_{ref} - \beta v_c)}{dt} \\ \int x_1 dt \end{bmatrix} = \begin{bmatrix} V_{ref} - \beta v_c \\ \dfrac{-\beta}{C} i_L \\ \int x_1 dt \end{bmatrix} \quad \textbf{(3-34)}$$

To create the state space matrix equation, take the time differentiation of the vector $\vec{x}$:

$$\dot{\vec{x}} = \begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \end{bmatrix} = \begin{bmatrix} x_2 \\ \dfrac{-\beta}{C} \dfrac{di_L(t)}{dt} \\ x_1 \end{bmatrix} \quad \textbf{(3-35)}$$

The value of $\frac{di_L(t)}{dt}$ depends on the state of the circuit, and according to eqns (3-20) and (3-25):

$\frac{di_L(t)}{dt} = \frac{V_i}{L} - \frac{v_c}{L}$ when u=1 and

$\frac{di_L(t)}{dt} = -\frac{v_c}{L}$ when u=0.

Combining these equations into one state space matrix equation gives:

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{-\beta}{LC} V_i \\ 0 \end{bmatrix} u + \begin{bmatrix} 0 \\ \frac{\beta}{LC} v_c \\ 0 \end{bmatrix} \quad \textbf{(3-36)}$$

The reachability condition requires that

$$\lim_{S \to 0} S\dot{S} < 0$$

This limit needs to hold true for both states of the system. So it needs to be true when S is greater than 0 and S is moving towards 0 (i.e., when *u*=1) and when S is less than 0 and S is moving towards 0 (i.e. when *u*=0).

When *u*=1, S will be positive as it approaches 0 so it is required that $\dot{S}$ be less than 0

$$\dot{S}_{(S \to 0^+)} = \alpha_1 \dot{x_1} + \alpha_2 \dot{x_2} + a_3 \dot{x_3} < 0$$

or

$$\dot{S}_{(S \to 0^+)} = \alpha_1 (\frac{-\beta}{C} i_L) + \alpha_2 \frac{\beta}{LC} (v_c - V_i) + a_3 (V_{ref} - \beta v_c) < 0 \quad \textbf{(3-37)}$$

In the second case, when *u*=0, S will be negative as it approaches 0, so it is required that $\dot{S}$ be greater than 0

$$\dot{S}_{(S \to 0^-)} = \alpha_1 \dot{x_1} + \alpha_2 \dot{x_2} + a_3 \dot{x_3} > 0$$

or

$$\dot{S}_{(S \to 0^-)} = \alpha_1 (\frac{-\beta}{C} i_L) + \alpha_2 \frac{\beta}{LC} v_c + a_3 (V_{ref} - \beta v_c) > 0 \quad \textbf{(3-38)}$$

Combining equations (3-37) and (3-38) gives the existence condition:

$$0 < \frac{\alpha_1}{\alpha_2} (-\beta L i_L) + \beta v_c + \frac{\alpha_3}{\alpha_2} (V_{ref} - \beta v_c) LC < \beta V_i \quad \textbf{(3-39)}$$

The existence condition can be obtained by the proper selection of $\frac{\alpha_1}{\alpha_2}$ and $\frac{\alpha_3}{\alpha_2}$.

The next section describes how to select the sliding coefficients to obtain the desired dynamic behaviour. Once the desired dynamic behaviour is obtained, the coefficients should be put back into equation (3-39) to ensure that the existence condition is met. If it is not met, then the desired dynamic behaviour needs to be adjusted to obtain coefficients that do meet the existence condition.

3.5.3.1 Selection of Sliding Coefficients

Equation (3-39) describes what is required for the existence condition to be met but does not give information on how to select the sliding coefficients to obtain the desired dynamic behaviour of the system. Ackermann's formula can be used to obtain a state feedback control law for any arbitrary dynamic behavior of a feedback system; [58] shows how Ackermann's formula can be used in a general SMC system and [50] shows how Ackermann's formula can specifically be used in the feedback of DC-DC converters using SMC. Using Ackermann's formula to give the desired dynamic behavior of the system ensures that the stability condition of the SMC is met.

In SMC systems, the point of stability occurs when S= 0.

$$S = \alpha_1 x_1 + \alpha_2 \frac{dx_2}{dt} + \alpha_3 \int x_3 dt = 0 \quad \textbf{(3-40)}$$

The equation for S can be rearranged into the standard 2nd order system equation by taking the derivative of $\vec{x}$ with respect to time, and dividing both sides of the equation by α_2

$$\frac{\alpha_2}{\alpha_2}\frac{d^2x_1}{dt^2} + \frac{\alpha_1}{\alpha_2}\frac{dx_1}{dt} + \frac{\alpha_3}{\alpha_2}x_1 = \frac{0}{\alpha_2}$$

$$\frac{d^2x_1}{dt^2} + \frac{\alpha_1}{\alpha_2}\frac{dx_1}{dt} + \frac{\alpha_3}{\alpha_2}x_1 = 0$$

$$\frac{d^2x_1}{dt^2} + 2\xi\omega_n\frac{dx_1}{dt} + \omega_n^2 x_1 = 0 \quad \textbf{(3-41)}$$

which allows for easy identification of the natural frequency (ω_n) and damping ratio (ξ) of the system

$$\omega_n = \sqrt{\frac{\alpha_3}{\alpha_2}} \tag{3-42}$$

$$\xi = \frac{\alpha_1}{2\alpha_2\omega_n} = \frac{\alpha_1}{2\sqrt{\alpha_2\alpha_3}} \tag{3-43}$$

Then by selecting the desired damping ratio and natural response, values for α_1, α_2, and α_3 can be determined.

Selection of the damping ratio, ξ, can give three broad (stable) response categories [59]:

1. $\xi > 1$ gives an overdamped response which is one that has the slowest response, but no overshoot
2. $\xi = 1$ gives a critically damped response which has the fastest response with no overshoot
3. $0 < \xi < 1$ gives an underdamped response which has the fastest response but the response will also have an overshoot.

A standard pole placement design method [59] is to choose a 1% settling time of the system which occurs at 5τ where τ is the time constant of the system. In terms of the damping ratio and natural response of the system

$$\tau = \frac{1}{\xi\omega_n} \tag{3-44}$$

Substituting equations (3-42) and (3-43) into (3-44) gives τ in terms of the sliding coefficients:

$$\tau = 2\frac{\alpha_2}{\alpha_1} \quad \textbf{(3-45)}$$

So the 1% settling time ($T_{s(1\%)}$) is

$$T_{s(1\%)} = 5\tau = 10\frac{\alpha_2}{\alpha_1} \quad \textbf{(3-46)}$$

The second system response characteristic is the peak overshoot (PO) which is dependent only on the damping ratio and is given by [59]:

$$PO = 100e^{-\xi\pi/\sqrt{1-\xi^2}} \quad \textbf{(3-47)}$$

Equation (3-47) can be rearranged in terms of ξ to give

$$\xi = \frac{\left|\ln\left(\frac{PO}{100}\right)\right|}{\sqrt{\pi^2 + \left[ln\left(\frac{PO}{100}\right)\right]^2}} \quad \textbf{(3-48)}$$

The design procedure then involves selecting the desired $T_{s(1\%)}$ and PO, then solving $\frac{\alpha_1}{\alpha_2}$ and $\frac{\alpha_3}{\alpha_2}$

$$\frac{\alpha_1}{\alpha_2} = \frac{10}{T_{s(1\%)}} = \frac{2}{\xi\omega_n} \quad \textbf{(3-49)}$$

$$\frac{\alpha_3}{\alpha_2} = \omega_n^2 \quad \textbf{(3-50)}$$

Values for $\frac{\alpha_1}{\alpha_2}$ and $\frac{\alpha_3}{\alpha_2}$ need to be put back in to equation (3-39) to ensure that the existence condition is met with the chosen sliding coefficients. If it is not, then the desired system dynamics must be adjusted.

This section concludes the derivation of the ratios $\frac{\alpha_1}{\alpha_2}$ and $\frac{\alpha_3}{\alpha_2}$ from the required system dynamics. The next sub-section will show how these ratios are used in creating the control law for the system.

3.5.3.2 Converting Sliding Mode Into PWM System

The next step in the SMC design is to calculate the control law and then determine how to use the control law in the quasi-SMC/PWM system. This control law derivation process is taken from [56].

Equation (3-37) is the value of $\dot{S}$ when u=1 and equation (3-38) is the value of $\dot{S}$ when u = 0. Combining the two equations gives

$$\dot{S} = \alpha_1\left(\frac{-\beta}{C} i_L\right) + \alpha_2 \frac{\beta}{LC} v_o - \left(u \times \alpha_2 \frac{\beta}{LC} V_i\right) + a_3(V_{ref} - \beta v_o) \quad \textbf{(3-51)}$$

Note that while the value of u is either 0 or 1, the average value of u can be determined by averaging the value of u over a period of time.

Setting $\dot{S} = 0$ and solving for u creates the control law for the feedback system:

$$0 < u_{eq} = -\frac{\alpha_1}{\alpha_2}\left(\frac{\beta L i_L}{\beta v_i}\right) + \frac{\beta v_o}{\beta v_i} + \frac{a_3 LC}{\alpha_2 \beta v_i}\left(V_{ref} - \beta v_o\right) < 1 \quad \textbf{(3-52)}$$

Multiplying the inequality by βv_i simplifies the control law to:

$$0 < u^*_{eq} = \frac{\alpha_1}{\alpha_2}(-\beta L i_L) + \beta v_o + \frac{a_3 LC}{\alpha_2}\left(V_{ref} - \beta v_o\right) < \beta v_i \quad \textbf{(3-53)}$$

This control law can be converted into a PWM system by generating the u^*_{eq} value from the system (and the predetermined $\frac{\alpha_1}{\alpha_2}$ and $\frac{\alpha_3}{\alpha_2}$) and comparing it to a ramp with a peak of βv_i to generate the PWM to the switches of the ripple port.

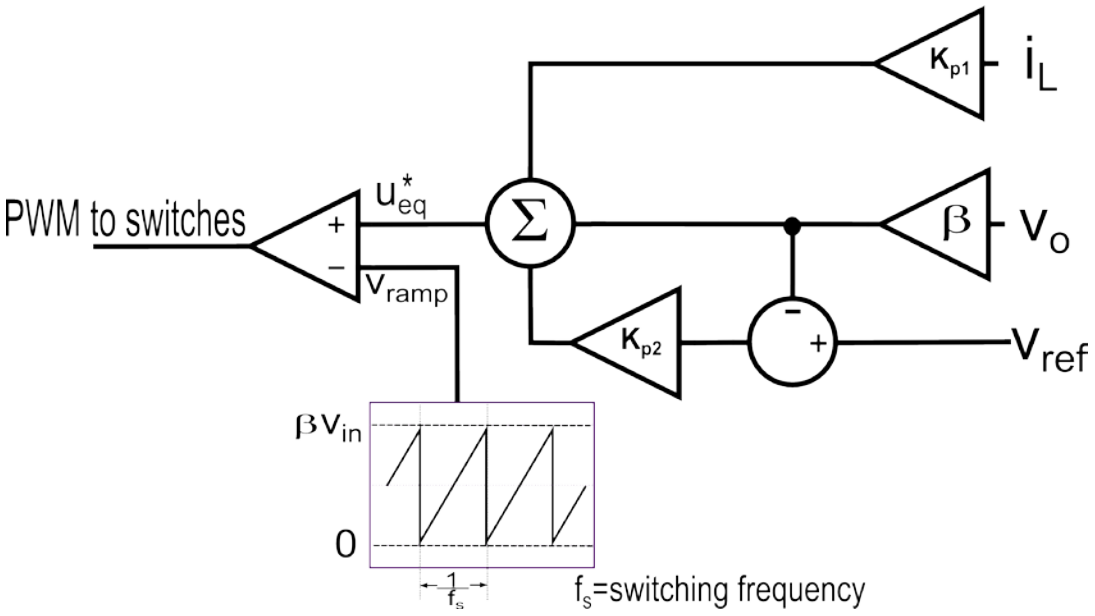

Figure 3.14 PWM Generation from Control Law

In the diagram:

$$K_{p1} = -\frac{\alpha_1}{\alpha_2}(\beta L) \quad \textbf{(3-54)}$$

$$K_{p2} = \frac{\alpha_3}{\alpha_2}(LC) \quad \textbf{(3-55)}$$

Now combining the control system circuitry with the APD port topology gives the entire system as shown in Figure 3.15.

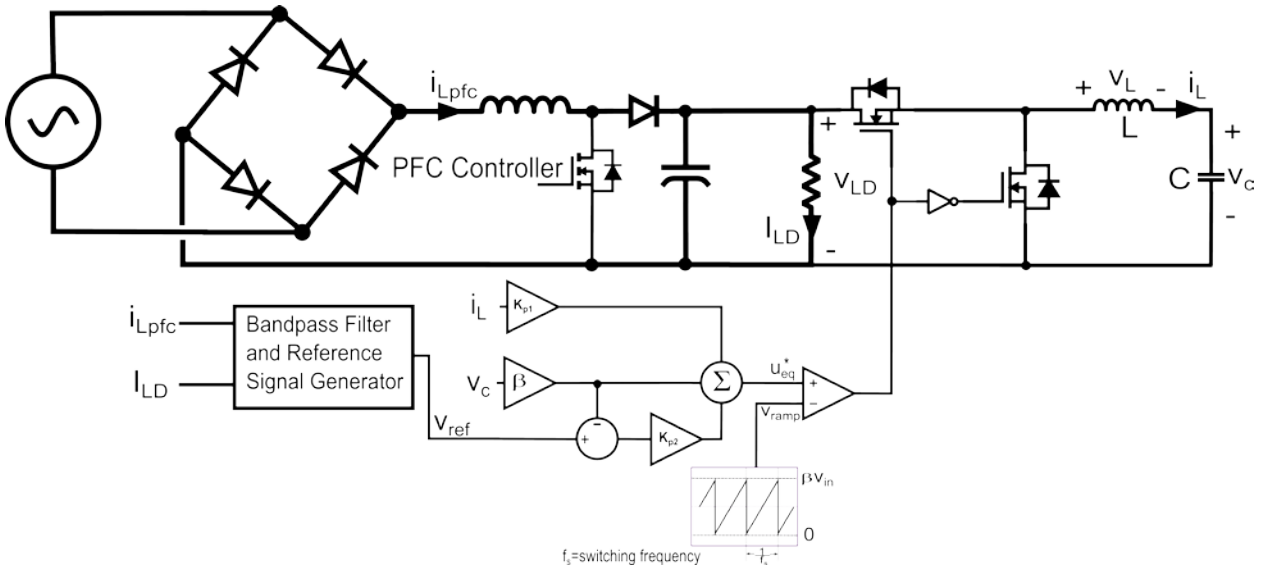

Figure 3.15 Active Power Decoupling Circuit in Boost PFC

Chapter 4:

Simulation Results of Active Power Decoupling Circuit

4.1 Overview of Results

A boost PFC circuit requires power decoupling to eliminate power ripple at the DC load. This power decoupling is typically achieved by using large electrolytic capacitors on the DC bus (i.e., at the load). The proposed power decoupling method in Chapter 3: uses an active power decoupling port to decouple the input AC power from the output DC power. This chapter provides a comparison between a boost PFC circuit using a large electrolytic capacitor (the benchmark) and a boost PFC circuit using the proposed power decoupling method. The performance metrics for this comparison will include power factor, total harmonic distortion, voltage ripple and capacitance required.

4.2 Benchmark System

The boost PFC system that will be used as a benchmark is a simulation of a 400V, 700 watt system. This system is based on a boost PFC system from Texas Instruments. The benchmark system simulation circuit is shown in Figure 4.1

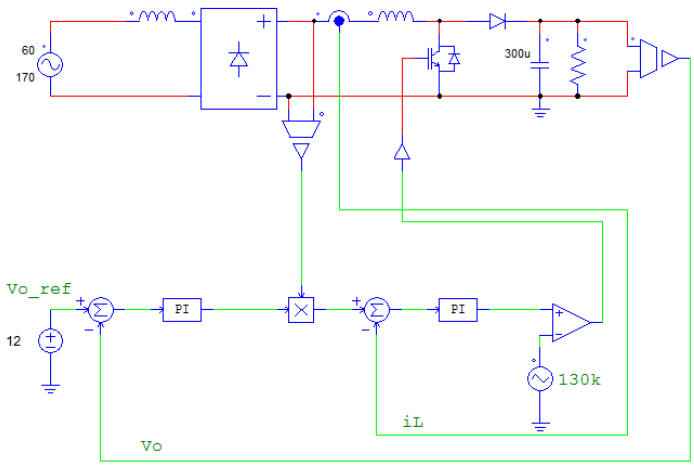

Figure 4.1. PSIM Simulation Schematic for Benchmark System

4.3 Active Power Decoupling Port System

The active power decoupling port system uses the same starting system as the benchmark, but the 300 µF capacitor is replaced with a 47uF capacitor (for high frequency filtering) and the APD circuit. The APD portion of the simulation circuit is shown in Figure 4.2

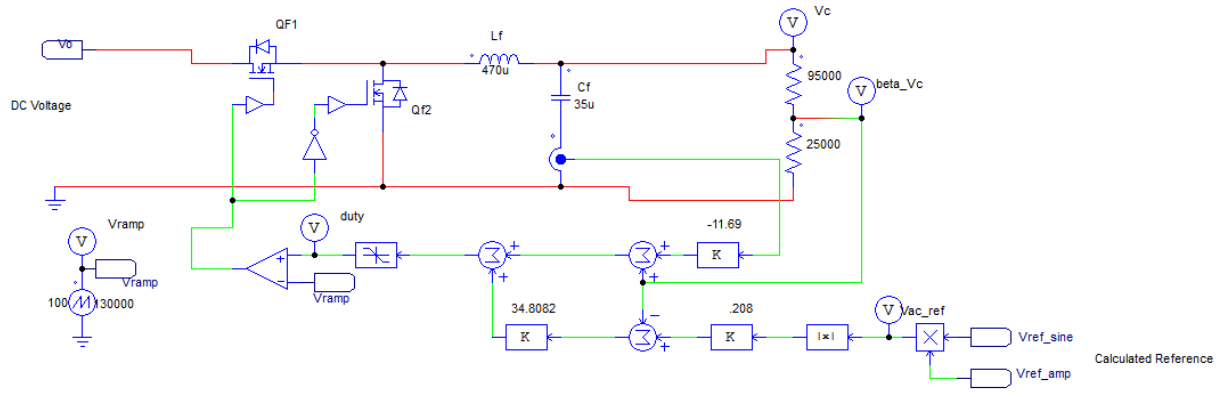

Figure 4.2 APD Port in PSIM

Note that the capacitor in the APD circuit is labelled as 35µF. Testing results shown in section 4.4 used both a 75µF and a 35µF capacitor.

4.4 Results

This section presents the simulation results for both the benchmark and the proposed systems. Simulations were run for both systems with various constant and changing loads. The most significant metric is the voltage ripple (and corresponding power ripple) at the output because it is the system characteristic the APD system must reduce. The power factor (PF) and total harmonic (THD) are also measured to ensure that other characteristics of the APD system are not detrimentally affected when compared to the benchmark system.

4.4.1 Steady State Operation

Figure 4.3 and Figure 4.4 show a comparison between the voltage ripple in the benchmark system and the voltage ripple in the APD system. In both of these cases, the load was the maximum of 700 W. The ripple for the benchmark circuit is 15V peak to peak (3.75% of V_{DC}) and the ripple for the APD circuit is 9V (2.25% of V_{DC}).

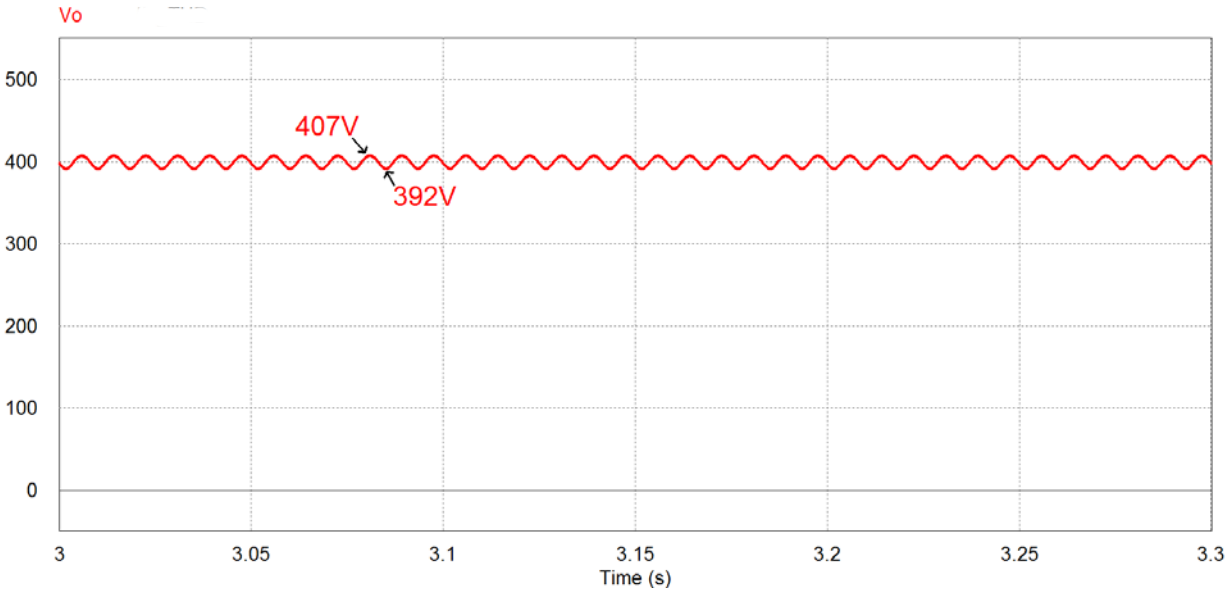

Figure 4.3. Voltage Ripple in Benchmark System

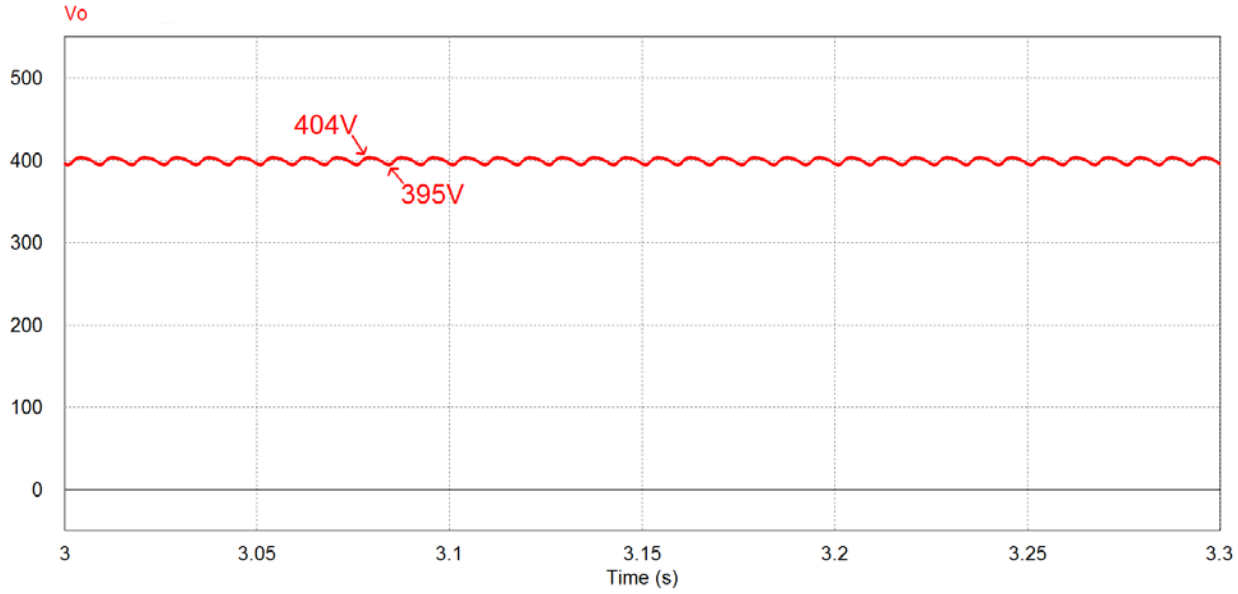

Figure 4.4 Voltage Ripple in APD System

The voltage ripple in the two systems is fairly similar and it can be seen in Table 4.1, which is a summary of the voltage ripple measurements for both systems under different loads, that the ripple voltage is fairly similar under all tested loads. One interesting characteristic that stands out

is that the APD circuit gives better results with high loads and the benchmark circuit gives better results with low loads.

Table 4.1 Voltage Ripple for Benchmark and APD Systems Under Various Loads

Load	System	Vripple (p-p)	Vripple (%)
700 W	Benchmark	15V	3.75%
	APD	9V	2.25%
350 W	Benchmark	9V	2.25%
	APD	6V	1.5%
175 W	Benchmark	3V	0.75%
	APD	4.3V	1%
100 W	Benchmark	2V	0.5%
	APD	3.6V	0.9%
50 W	Benchmark	1.3V	0.3%
	APD	2.7V	0.7%

The ripple voltage at the output is an important measurement for comparison between the two circuits, distortion at the input is another important consideration. If the input of the APD circuit is significantly more distorted than the input of the benchmark circuit, then the APD solution will not work. Figure 4.5 and Figure 4.6 show the input (AC) voltages and currents of the benchmark circuit and APD circuit respectively.

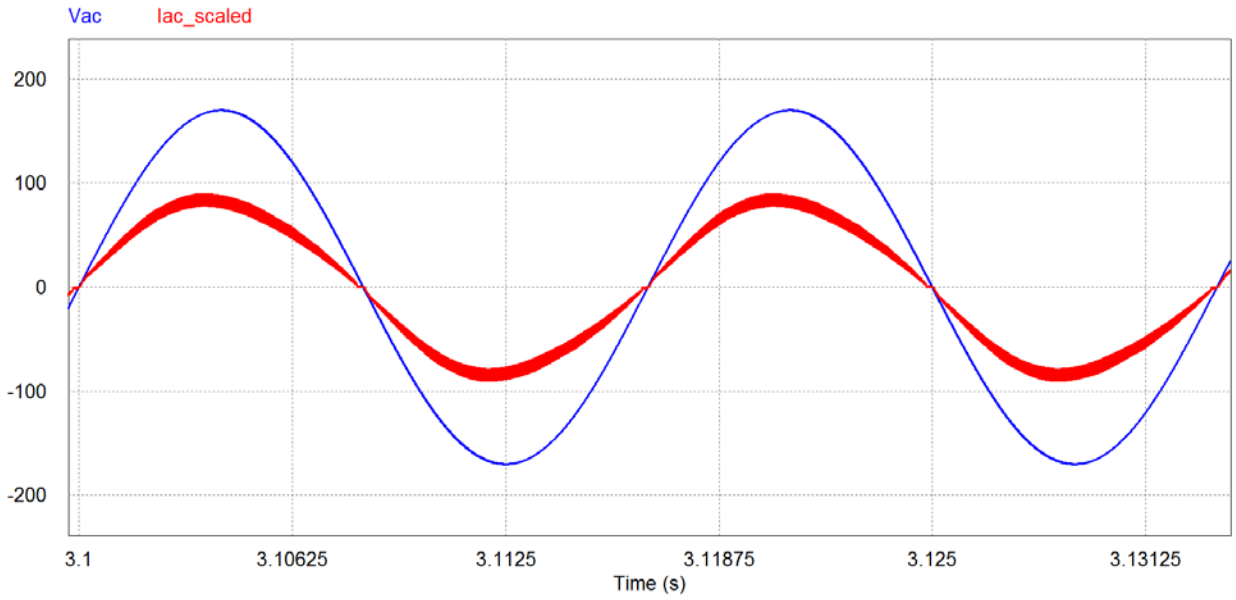

Figure 4.5. Relationship betwen Vac and Iac in Benchmark Circuit

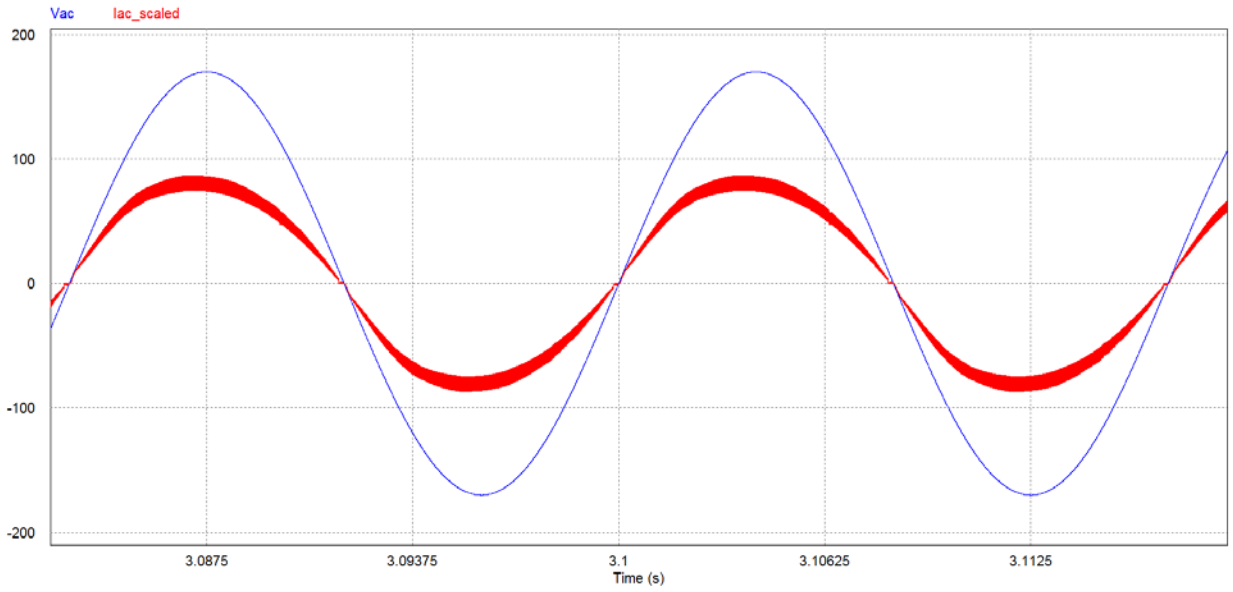

Figure 4.6. Relationship between Vac and Iac in APD Circuit

The AC voltage shown is from a voltage source and the AC current shown is the resulting current into the system. It should be noted that the current signal is labeled ***Iac_scaled*** because it

is the AC current scaled up by a factor of 10 to make it more visible on the graph. In other words, the peak appears to be 83A when in fact, the peak current is actually 8.3A.

When comparing the two sets of signals, it is apparent that there are differences in the shapes of the current waveforms, but it is more useful to make a quantitative comparison between the two by measuring the power factor and the THD of the current. These characteristics were measured under the same loads as in Table 4.1 and these measurements are shown in Table 4.2.

Table 4.2 Voltage Ripple for Benchmark and APD Systems Under Various Loads

Load	System	Power Factor	THD
700 W	Benchmark	0.995	6%
	APD	0.995	7%
350 W	Benchmark	0.989	10.5%
	APD	0.990	11.7%
175 W	Benchmark	0.966	19.7%
	APD	0.966	20.5%
100 W	Benchmark	0.92	34.4%
	APD	0.92	33.3%
50 W	Benchmark	0.84	61.3%
	APD	0.84	58.4%

The primary take-away from this comparison between the benchmark and APD circuits is that the results are quite similar which indicates that using the APD system does not detrimentally affect the performance of the system.

A more rigorous analysis of the harmonic content involves analyzing the currents at specific harmonics. This kind of analysis is important in order to meet international specifications such as the IEC-1000-3-2 [1] which regulates allowable amount of harmonic content generated by electronic devices connected to the electrical grid. IEC-1000-3-2 (also known as EN-61000-3-2) specifies several different classes of equipment and harmonic content limits for each of the

classes. The systems used in this paper fall under either Class A or Class D. Class D devices are devices with AC input to a DC load that are under 600W, while Class A categorization includes AC-DC converters with loads over 600W. This test system is on the border between Class A and Class D because it can consume/output up to 700W but can also have loads less than 600 W. Since it is capable of being a Class A device, it should probably be evaluated as a Class A device. However, for completeness Class D parameters will also be examined.

Table 4.3 IEC-1000-3-2 Specifications plus harmonic content in I_{ac} of APD circuit

Harmonic Hz (order)	Class A Maximum permissible harmonic current (A)	Class D Maximum permissible harmonic current per watt (at 700W) (A)	Class D Maximum permissible harmonic current per watt (at 175W) (A)	Harmonic Content of I_{ac} APD Circuit (700W Load) (A)	Harmonic Content of I_{ac} APD Circuit (175W Load) (A)
120 (2)	1.08	-	-	~0	~0
180 (3)	2.3	2.38	0.60	0.43	0.2
240 (4)	0.43	-	-	~0	~0
300 (5)	1.14	1.33	0.33	0.124	0.08
360 (6)	0.3	-	-	~0	~0
420 (7)	0.77	0.7	0.18	0.043	0.04
480 (8)	0.23	-	-	~0	~0
540 (9)	0.4	0.350	0.088	0.028	0.034
660 (11)	0.33	0.175	0.061	0.025	0.03
780 (13)	0.21	0.203	0.051	0.0122	0.021
900 (15)	0.15	0.182	0.045	0.01	0.014

The data in Table 4.3 lists the maximum permissible harmonic currents for Class A devices and Class D devices for both 700W and 175W loads. The last two columns of the table list the measured (from simulation) harmonic content of the current in the APD circuit under full load (700W) and one quarter load (175W). It is clear from the data that the APD circuit meets the

IEC-1000-3-2 specifications for both of the loads regardless of if it is categorized as a Class A or a Class D device.

This subsection has shown that replacing the passive electrolytic capacitors of the benchmark circuit with active power decoupling has no detrimental effects on the steady state performance of the circuit. Voltage ripple, power factor, and THD are nearly identical between the two circuits. At the same time separate current harmonic measurements indicate that the APD circuit still meets the IEC-1000-3-2 specification.

The next section analyzes the dynamic operation of the benchmark and APD circuits to see how the circuits respond to changing loads.

4.4.2 Transient Response

When a system is in steady state and either the input or the output changes, there will be some kind of transient response. Specifically, if the load changes, the system will respond to try to return the output to the regulated value. This section describes the observations made when the load is stepped up to a greater load and stepped down to a lesser load. Specific measurements that will be obtained in these tests are how much the system overshoots while trying to compensate for the load change and the amount of time it takes to reach steady state conditions again.

Figure 4.7 shows several step changes in the load to the benchmark circuit. The change of load in each step is one quarter of the full load and the loads range in value from a full load (700W) down to one quarter of a full load (175 W).

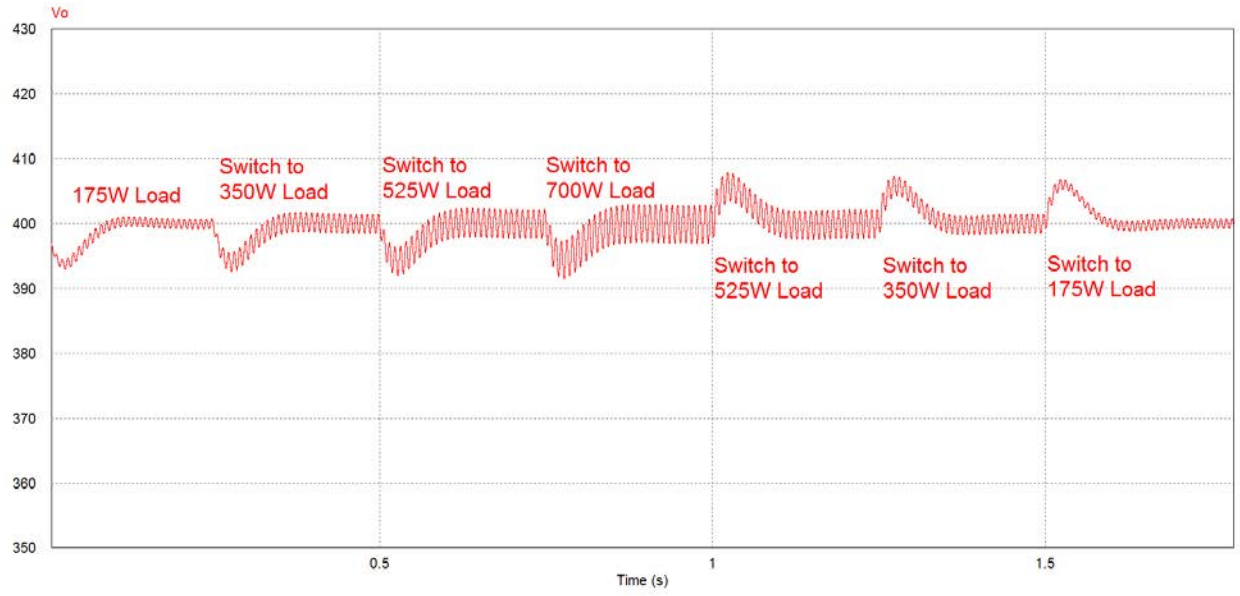

Figure 4.7 - Output Voltage Response to Changing Loads (Benchmark Circuit)

It can be seen in the figure that when the load is stepped up, there is a negative overshoot and when the load is stepped down, there is a positive overshoot. When stepping up the load, the voltage dips down to 393V and then takes about 0.125 seconds to return to steady state. When stepping down the load, the voltage jumps up to 408V and returns to steady state in approximately 0.125 seconds.

In comparison, Figure 4.8 shows the output voltage with the same output load step changes.

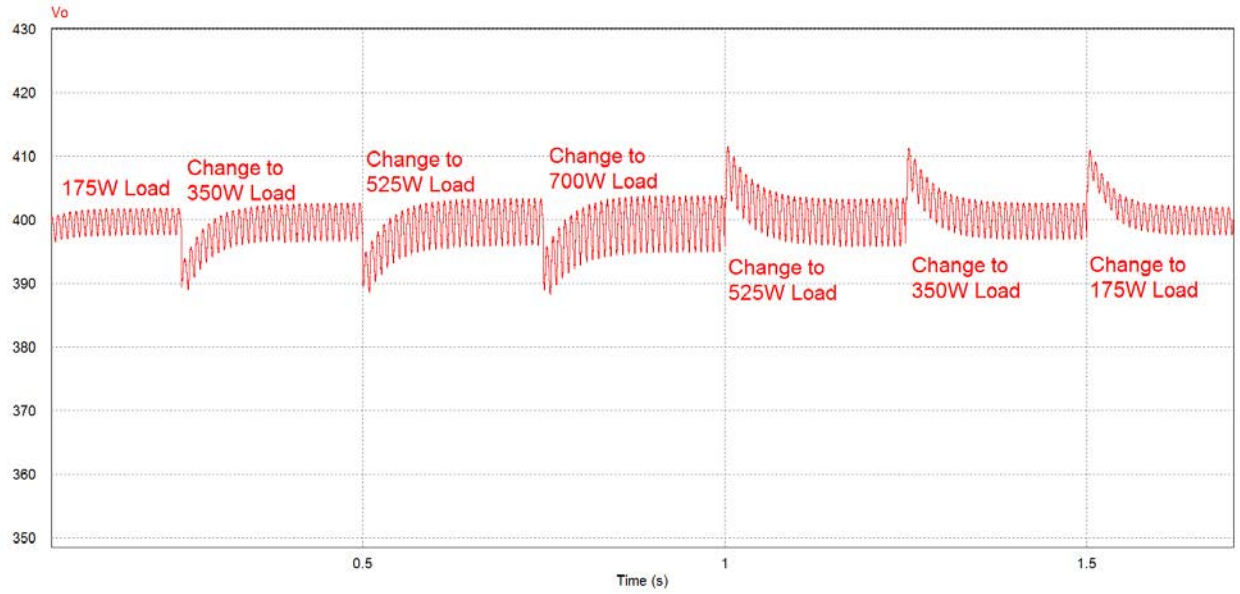

Figure 4.8 Output Voltage Response to Changing Loads (APD Circuit)

When stepping up the load, the voltage dips down to 389V and then takes about 0.18 seconds to return to steady state. When stepping down the load, the voltage jumps up to 411V and returns to steady state in approximately 0.16 seconds.

Figure 4.9 and Figure 4.10 also show step changes but with larger steps from quarter load (175W) to full load (700W) for both circuits.

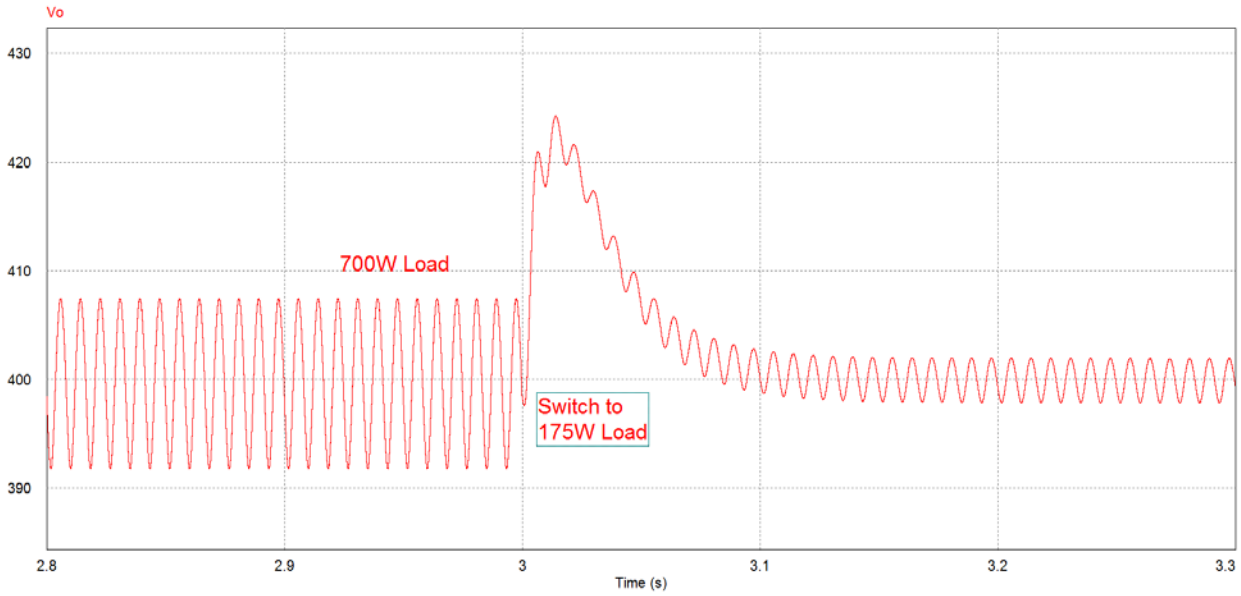

Figure 4.9 Output Voltage Response to Load Change (700W to 175W) (Benchmark Circuit)

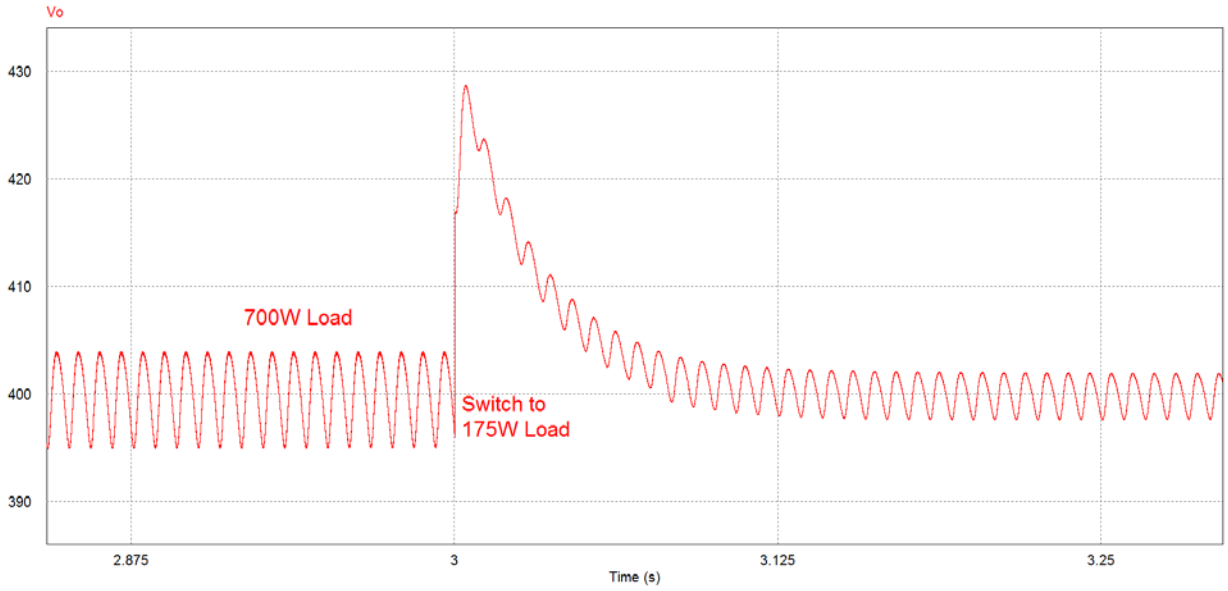

Figure 4.10 Output Voltage Response to Load Change (700W to 175W) (APD Circuit)

The benchmark circuit has less output voltage overshoot, going to a peak of 424V compared to 428V for the APD circuit. Both circuits have a settling time of about 0.15s.

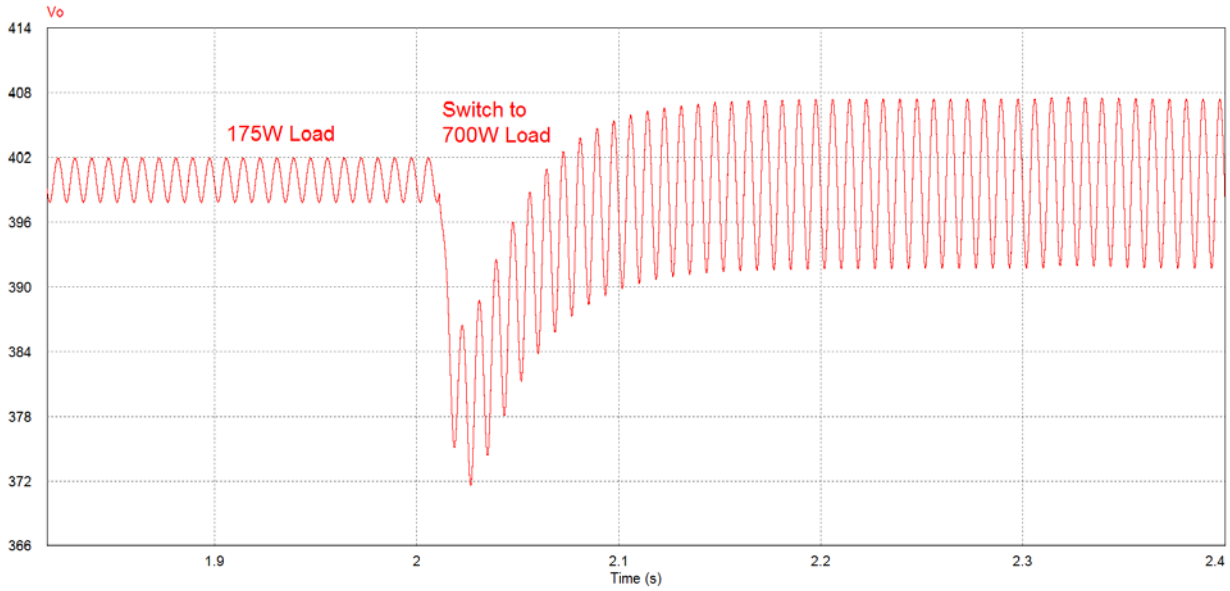

Figure 4.11 Output Voltage Response to Load Change (175W to 700W) (APD Circuit)

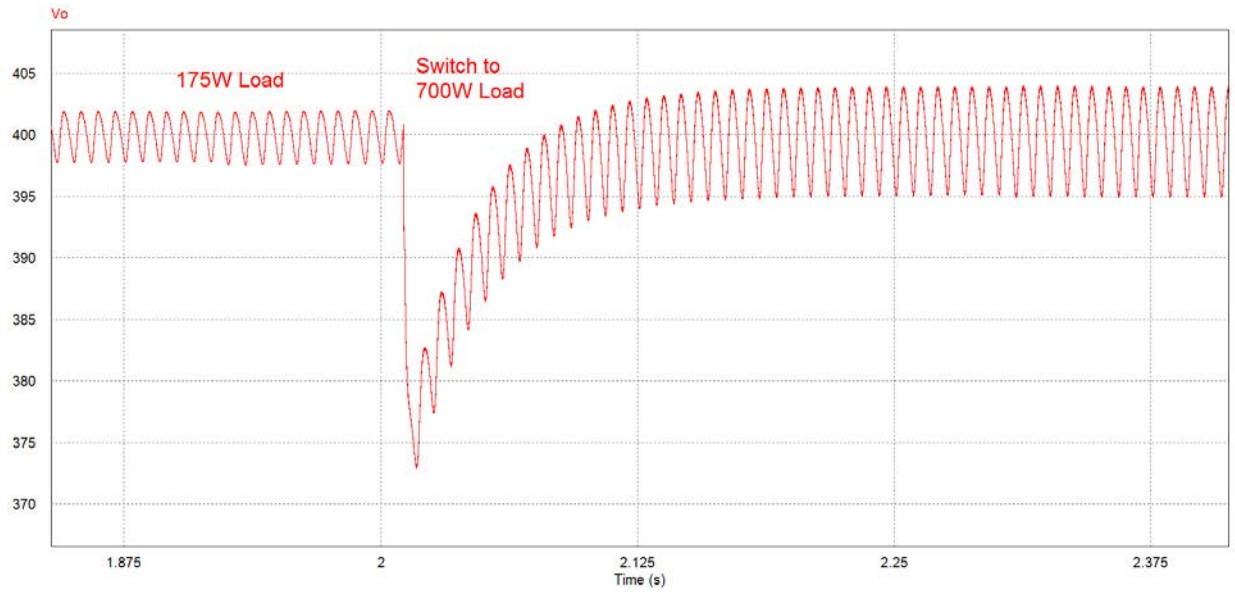

Figure 4.12 Output Voltage Response to Load Change (175W to 700W) (APD Circuit)

When the load steps up, the responses are fairly similar as well. Both circuits drop down to about 372V and return to steady state in approximately 0.15 seconds

4.4.3 Input AC Power vs. Power to APD port

If the power decoupling was perfect, then all of the ripple power would go to the APD port and the average power would go to the load, but of course voltage tracking will not be perfect. There will be switching noise, the phase shift between input voltage and APD port voltage may not be at the exact value required, and the response of the control system will not be instantaneous. This section will qualitatively analyze the relationship between the ripple power at the input and the power to the APD port by visually comparing the two power measurements.

The top half of Figure 4.13 shows the input AC power and the power to the APD port. The waveforms are very similar, but not identical; there is small phase shift between the two (~5°) and there is some distortion in the signals in part due to the switching and in part due to the nature of the current flow to the APD circuit which is somewhat discontinuous. The small spikes in the APD power that are visible around the zero crossing (when going positive to negative) occur when the APD current is transitioning from positive to negative. The bottom half of Figure 4.13 zooms in to APD current and power at that point in time. Inspection of these signals seems to indicate that the spikes are likely due to the inability of the control system to properly handle currents rapidly changing direction.

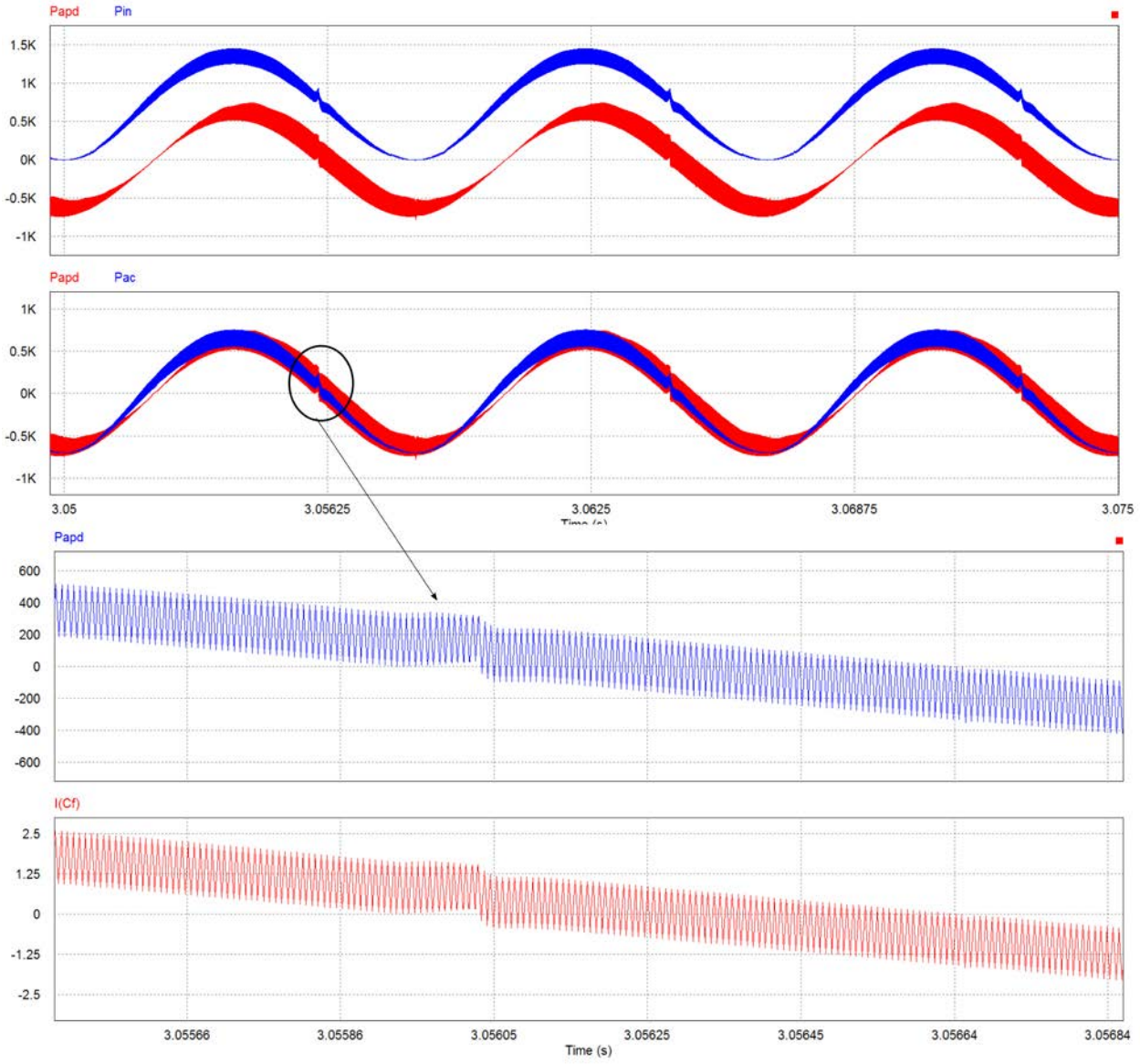

Figure 4.13 Input Power and Ripple Port Power

4.4.4 Discussion of Capacitor Reduction

The tests in the previous subsection were all done with a capacitance value of 75uF in the APD port. It is possible to reduce this capacitance even more as long as the voltage (V_c) is increased according to eqn (3-14) which is duplicated here:

$$C = \frac{2P_o}{\omega V_c^2} \quad \text{or} \quad V_c = \sqrt{\frac{2P_o}{\omega C}}$$

Since the voltage in to the APD is 400V (plus some ripple) and there are diminishing returns (in terms of capacitance reduction) as the voltage increases due to the voltage being proportional to the **square root** of the capacitance. A maximum APD voltage of around 325V is advisable. At a peak of 325V to the APD, the capacitance required would be 35µF.

Figure 4.14 shows the voltage ripple with the 35µF capacitor in the APD. The ripple is nearly identical to the ripple with the 75µF capacitor. This result is expected since the power ripple is controlled to be the same. THD and power factor measurements also give similar values of 7% and 0.995 respectively.

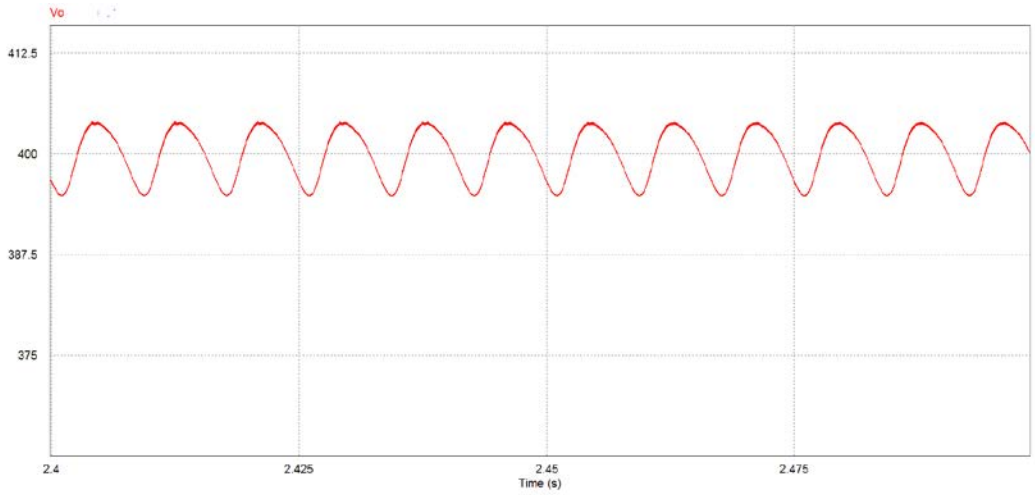

Figure 4.14 Output Voltage Ripple with 35µF Capacitor

The transient response with the 35µF is also very similar to the transient response with the 75µF capacitor as can be seen in Figure 4.15

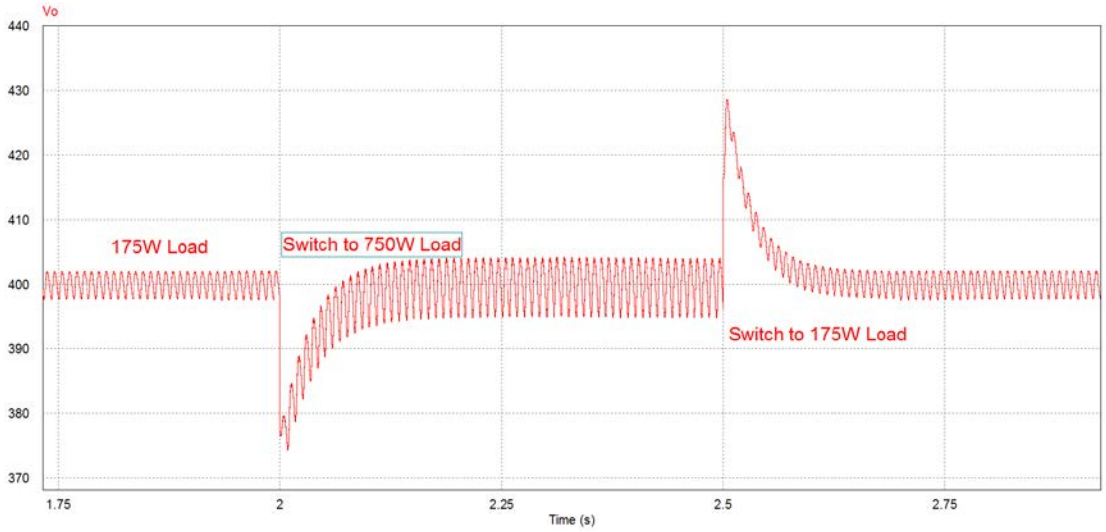

Figure 4.15 Response to Changing Load (APD with 35µF cap)

The overshoot goes down to 375V and up to 428V while the settling time is about 0.19s.

Based on the fact that the 35µF capacitor and the 75µF capacitor give nearly identical results, the recommended capacitance in the APD is 35µF. Further capacitance reduction is likely possible, but then the capacitor voltage would need to approach the DC bus voltage and a safety margin of 50-75V is recommended.

4.4.4.1 DC Bus Capacitor

The capacitor in the DC bus is still required for filtering higher frequency noise. In the previous experiments it was kept at 75 µF. In this set of experiments, it was reduced to 35µF to see what the effect would be on the voltage ripple, power factor and THD. With this reduction, the voltage ripple was 15V peak-peak, the power factor was 0.994 and the THD of the current was 9.2% with a load of 700W.

These results indicate that the DC bus capacitor does have an impact on the overall results and for this particular system it is necessary to keep it at 75 µF to keep the results on par with the benchmark system. In support of this conclusion, the transient response also worsens. When

stepping up the load, the voltage spikes down to 355V and when stepping down the load, the voltage spikes up to 434V. These values are 15-20 V more than when the 75 µF capacitor is used.

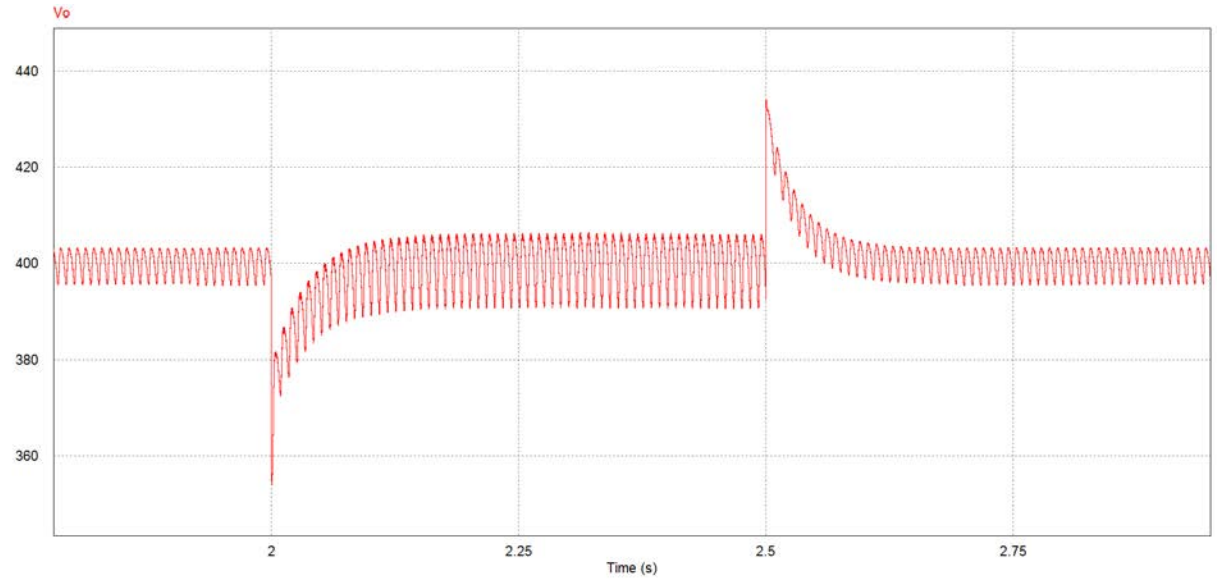

Figure 4.16 DC Bus Voltage Transients With 35 µF Capacitor on DC Bus

4.4.4.2 Capacitor Costs

Evidence from simulation indicates that performance would not be affected by replacing the 300µF capacitor in the benchmark system with a 75µF capacitor on the DC bus and a 35µF capacitor in an APD port. Assuming that long life capacitors are required in the system, the next question is "is it cost effective to use a lower capacitance on an APD port instead of a 300 µF film capacitor on the DC bus?"

The answer is not totally clear because it would depend on a full cost analysis of the system. What can be quickly done is compare the cost of the film capacitors. Table 4.4 shows cost, voltage rating and part numbers for the three capacitances under question. This data is taken from Mouser's website and is based on orders of 100 units which is the highest quantity price break quoted on the website for the 100µF capacitor.

Table 4.4 Film Capacitor Costs

Capacitance	Cost	Voltage Rating	Part #
100μF	$78.31	1100V	B25620B1107K101
75 μF	$32.63	630V	B32798G2756K
35 μF	$26.80	875V	B32798G8356K

If the benchmark system was to use film capacitors it would require 3 of the 100μF caps from Table 4.4 resulting in a cost of $234.93 for the capacitors. If the APD system was to use the 75μF and 35μF film capacitors, it would cost $59.43. Overall, it would cost about $175 more for the capacitors in the benchmark system. To determine if this would be cost effective, the cost of the balance of the APD system would need to be determined but that is an exercise to be saved for when the physical system is built.

4.4.5 Effect of Phase Difference Between Input AC Voltage and APD Voltage

The results discussed in the above subsections all use a phase difference between the input AC voltage (V_{ac}) and the APD voltage ($_{Vac\_ref}$) of 45°. This phase difference is shown in Figure 4.16.

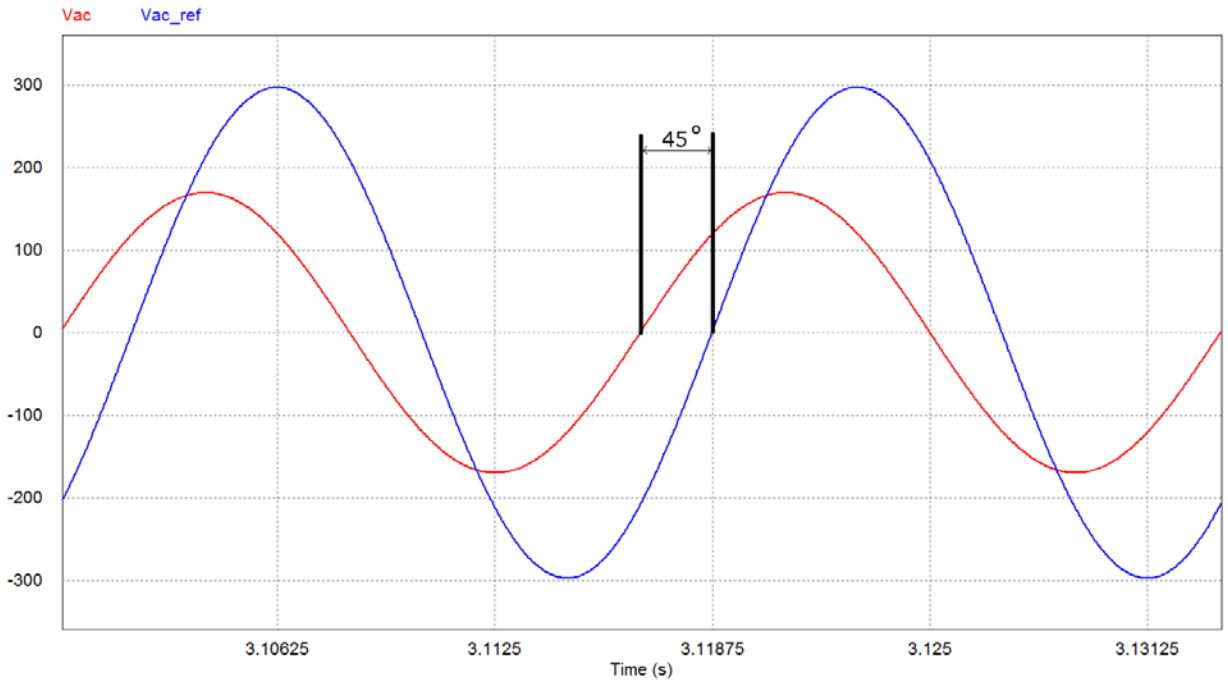

Figure 4.17. Phase Shift Between AC Voltage and Reference Signal

When the phase difference is varied from 45°, the effectiveness of the power decoupling circuit is reduced. To illustrate this reduction of effectiveness, a few different phase shifts were tested and the resulting output voltage ripple, power factor and THD for these tests is shown in Table 4.5

Table 4.5 Effect of Phase Shift on Voltage Ripple, Power Factor and THD

Phase Shift	Voltage Ripple (peak-peak)	Power Factor	THD
55	22V	0.989	13.7%
50	15V	0.994	10%
47	9V	0.995	8%
45	9V	0.996	7%
43	9V	0.994	7%
40	9V	0.994	7%
35	13V	0.990	9%

This table confirms that 45° is the optimal phase shift to use. It has the best voltage ripple, power factor and THD.

4.5 Summary of Results

Tests of voltage ripple, power factor, and THD under constant and varying loads show that the boost PFC circuit with APD performs as well as the benchmark PFC circuit with Al e-caps for power decoupling. The capacitance can be reduced from $3 \times 100\mu F$ capacitors to a 35μF cap and a 75μF capacitor. For systems where long life is a necessity, this capacitance reduction results in a cost savings on capacitors of $175. The overall cost savings needs to be determined when the hardware prototype is built.

Chapter 5: Conclusions and Future Work

5.1 Conclusions

It is obviously desirable to have a long life for electronic devices; for some types of devices, long life is absolutely critical. A primary feature of modern lighting is that they last for many tens of thousands of hours. This feature has been driven by the migration of lights from incandescent to compact fluorescent to LEDs. LEDs have very long lifespans and in order to create lights that last tens of thousands of hours, all components must at least match the lifespan of the LEDs. High power LED lighting systems used in industrial lighting settings can operate on the order of hundreds of watts. These high power lighting systems must meet several requirements simultaneously. They must be able to convert AC power to DC power (and therefore must filter double line frequency ripple), they must have a long life (tens of thousands of hours), and they must be affordable. The standard method of filtering the double-line frequency ripple involves putting a large Al e-cap at the DC bus, but because of the high output power of industrial LED lighting systems, operating temperatures are too high to support the required lifespan of the capacitor. Putting a film capacitor in as a direct replacement for the electrolytic capacitor is not cost effective because on a $\$/_F$ basis, film capacitors are far more expensive than Al e-caps.

Much research has gone into developing ways to reduce the required capacitance for the filter by actively decoupling the ripple power from the DC power. Doing this allows film capacitors to be cost effectively used in place of Al e-caps in AC-DC converters. This thesis has investigated that research and then contributed a method, including topology and a control system for reducing the capacitance required for filtering the double-line frequency ripple. This method provides active power decoupling without the need to directly measure the AC input. It allows for the reduction

of the capacitance by a factor of 8.5 without affecting the performance of the circuit as measured by the voltage ripple, power factor, and THD of the input current.

5.1.1 Active Power Decoupling Without Directly Measuring AC Input

Active power decoupling is a well-researched method to decouple double-line frequency ripple from the DC output of an AC-DC converter. The elegant APD solution proposed by Krein and Balog allows for flexibility in topology selection and ease of controlling the APD circuit. What that solution requires though is direct measurement of the AC mains voltage and current. The method proposed in this thesis removes the requirement of directly measuring the line voltage or current and the simulation results indicate that required capacitance can be significantly reduced while having no effect on the performance of the system.

5.1.2 Sliding Mode Control for APD Circuit

Sliding mode control is a natural fit for controlling power electronic circuits which have multiple states that are the result of the switches. These multiple states lend themselves well to SMC. The literature showing the use of SMC in power electronics is growing, but it has never been used in APD circuits. While this thesis does not compare SMC to other modes of control, it does show how to design SMC for an APD circuit and proves that SMC can be an effective control solution for APD circuits.

5.2 Future Work

This section contains recommendations for possible future work to keep the project moving forward.

5.2.1 Board Design

An APD board should be created to test active power decoupling in hardware. This board would consist of the buck-based active power decoupling port and associated control system for managing power flow to and from the APD port. The APD board would be connected to an AC-DC converter with power factor correction. A good candidate for the AC-DC converter is the 400V, 700W TMDSILPFCKIT board from Texas Instruments [62].

5.2.2 Digital Controller

Most, if not all of the signal processing done in the simulations are intended to be implemented on the digital controller. The list of digital controller blocks that needs to be created includes

1. 120Hz Bandpass filter
2. 60 Hz reference signal re-generation
3. Sliding Mode Control Calculations

Alternatively, it is possible to build the control system in hardware. The 120Hz bandpass filter and the 60Hz reference signal re-generation could be built using operational amplifiers, flip-flops and a simple microcontroller. The SMC circuit needs sensors and multipliers, so it could also be easily created using operational amplifiers.

5.2.3 Experimentation in Hardware

Once a new board is built and the digital controller software is written, the obvious next step is to test the new APD system and compare it to the original system without APD as well as to simulation. Testing in hardware would involve comparing similar metrics as was done in

simulation (i.e., voltage ripple, power factor, total harmonic distortion, effect of phase shift), but would also include testing the efficiency of the APD system versus the benchmark system.

5.2.4 Adaptive Phase Shifting

The phase difference between the AC voltage source and the APD capacitor voltage needs to be maintained at 45° when the power factor is 1. For this experiment, the power factor was assumed to be 1, but if the power factor is not unity and/or changes during operation as the load changes, the phase shift should be adjusted to minimize power ripple to the load. An adaptive phase shifting scheme could be adopted either based on direct power factor measurements, or using a Maximum Power Point Tracking (MPPT) type algorithm such as the hill-climbing technique discussed in [61].

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