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## High Efficiency Power Supply using new SiC devices

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## **Zusammenfassung**

Neuartige Siliziumkarbid (SiC) Bauelemente und dessen Nutzung in Schaltnetzteilen ist der Gegenstand dieser Arbeit. Wie sind die Eigenschaften des SiC Leistungsbauteils optimal auszunutzen um die Topologien der Schaltnetzteile zu vereinfachen und die Leistungsdichte zu steigern.

Die SiC Schottky Dioden sind am Markt, aber auch die SiC Transistoren sind seit kurzem verfügbar als FuE Muster. Dennoch, die Verbreitung und der Einsatz in den herkömmlichen Topologien findet sehr langsam statt. Einerseits die hohen Produktionskosten des Halbleiters und dementsprechend hohe Preisverhältnis gegenüber Si Bauteilen, andererseits unbekannte Eigenschaften des SiC Transistors (SiC JFET) verzögern die breite Marktakzeptanz. Offensichtlich ist, dass ein einfacher Umtausch der Si Leistungsschaltern mit den entsprechenden SiC Bauteilen in den herkömmlichen Schaltnetzteilen würde nicht die erwartete Effizienz - und Leistungserhöhung ermöglichen.

Ausgezeichnete Eigenschaften von SiC Halbleiter sind seit Jahren gut bekannt. Was nicht eindeutig ist, und das ist die Zielsetzung dieser Arbeit, in welcher Weise sind diese Eigenschaften auszunutzen um die maximalen Vorteile für die Endanwendung zu einzubringen.

Anhand der Beispielanwendung der Telekomstromversorgung wurde vorgeschlagen das Vorgehen in der Topologieauswahl zu ändern und für einen Leistungsbereich von 1kW-1.5 kW anstatt Mehrschaltertopologien eine Einschaltertopologie mit SiC Transistor zu verwenden. In der entstandenen Anwendung ist der Einsatz des SiC Junction Field Effect Transistors (JFET) notwendig und dessen Potenzial ist voll ausgenutzt, wobei die Probleme bezüglich der Mehrschaltertopologien beseitigt sind.

Um die Schaltfrequenz zu erhöhen und die Leistungsdichte weiter zu verbessern, wurde ein weiches Schalten von Resonant Reset Converter verwendet, die die parasitäre Elemente der Schaltung nutzt. Gleichzeitig ermöglicht die höhere Sperrspannungsfähigkeit des SiC Schalters eine schnellere Entmagnetisierung des Leistungstransformators.

Die SiC JFET Transistoren sind detailliert analysiert und die spezifischen Eigenschaften sind festgestellt, welche eine neuartige und einfache Gateansteuerung ermöglichen.

Die bekannte Lösung für Normally-ON Problematik – „Baliga Pair“ wurde erweitert, um zusätzliche Stabilität zu erhalten, was sich besonders bei Schaltfrequenzen über 200kHz bemerkbar macht.

*To my family, with much love and gratitude for  
loving care and support during all these years*

*January, 2007*

## **Summary**

New Silicon Carbide (SiC) power devices and their usage in the switch mode power supply (SMPS) circuits is the subject of this thesis, - how to fully exploit the potential of SiC devices in switch mode converters while simplifying their topologies and increasing power density and efficiency.

Although the excellent properties of the SiC semiconductor and its superior features compared with silicon (Si) are recognized for many years and long-awaited SiC power devices are now available, their practical application in power supplies is still seems to take time. Obviously, simple replacement of the Si power transistors in commonly used topologies, which are not originally designed to exploit all futures of SiC devices, will not give the expected efficiency increase and cost advantages. The SiC power devices set another dimension in designing process of the switch mode power converters. It becomes necessary to develop a new, system relevant approach in the power supply design.

Currently in the 1.0kW -1.5kW power supplies (e.g. for telecom applications) multi-switch Half-Bridge or Full-Bridge topologies are used. Having the advantage of limited voltage stress on the switches, (app. 600V-800V), these topologies incorporate external isolated high-side gate drive circuits, have to maintain appropriate dead times to prevent shoot trough conditions and have to deal with inherent magnetic flux imbalance in the transformer core.

It is suggested to change the settled hierarchy in the converter topologies used in the mentioned power range and replace the Si-based multi-switch converters by a SiC single-switch converter. In the proposed single-switch resonant reset forward converter, the specific properties of SiC Junction Field Effect Transistor (JFET) are necessarily used and its potential is fully utilized, while the challenges associated with multi-switch topologies are basically eliminated. The comparative analysis also shows minimal differences between passive components of the single-switch, single-ended and double-switch, double-ended converters.

Proposed zero voltage switching (ZVS) approach in the adopted converter enables further increase of the switching frequency while utilizing the circuit parasitics and increasing the power density. The circuit is analyzed over the complete power and voltage

range. Special attention is paid for parasitics, possible overvoltages, ZVS operation and switching losses.

However, the SiC JFET is a normally ON transistor and requires relatively high negative voltage for switching OFF, which makes its utilization in many applications difficult. The new and simple driving circuit, based on DC voltage bias is suggested as a gate driver for SiC JFET.

Another known way out from normally ON behavior is the “Baliga Pair” or combined “Cascode” circuit, where the JFET-MOSFET pair can operate in normally OFF mode. However, in such circuitry, because of limited reverse recovery capability of the body diode, a parasitic oscillation could occur if very fast switching is performed. Also the direct switching speed adjustment by means of gate resistors is not possible. For eliminating these limitations a modification of the “Cascode” is proposed, where the SiC device can be driven with its own gate, yet remaining normally OFF in case of failure or power down.

Although the SiC wafer quality is increasing gradually, large chip areas are not feasible in near future. Logical solution for increasing device current capability is the parallel connection of the small chips. Investigations on the SiC JFET samples have shown different punch-trough gate currents. This fact should be taken into account, for the gate drive circuit designs if parallel driving of the SiC JFETs is necessary, especially for circuits with avalanche or current source driving methods.

Mentioned proposals are investigated and implemented in practical hardware design.

## Preface

This thesis project has been jointly supported by Infineon Technologies and Siemens AG.

The steering group consists of:

Prof. Dr. Jürgen Schmid

Prof. Dr. Eckhard Wolfgang

Prof. Dr. Peter Zacharias

Prof. Dr. Leo Lorenz

The following parts of the thesis are original work:

- ✓ SiC devices are implemented in the Resonant Reset Forward converter, its output power range has been extended up to 1kW and zero voltage switching (ZVS) operation is realized.
- ✓ SiC JFET transistors are analyzed and tested under high temperature conditions (250°C) and investigations are carried out for possible parallel connection of the chips.
- ✓ Alternative gate driver circuit for SiC JFET transistors is proposed.
- ✓ SiC JFET Cascode (Baliga Pair) circuit is investigated at higher switching voltage slew rates and modification is proposed for minimizing the influence of packaging parasitics
- ✓ A practical 1 kW prototype of single switch resonant reset converter is realized, where the active switch operates at 200-300 kHz frequency. High temperature operation capability (app. 250°C) is tested under light load operation.

The research project is partially published in the following publications:

1. European Power Electronics Conference EPE'03, September 2003, Toulouse, France
2. Power Control and Intelligent Motion PCIM-Europe'04, May 2004, Nürnberg, Germany
3. IEEE Power Electronics Specialist Conference PESC'04, June 2004, Aachen, Germany
4. Power Electronics and Motion Control EPE-PEMC'04, September 2004, Riga, Latvia
5. IEEE Industrial Applications Society IAS'04, October 2004, Seattle, Washington, USA
6. VDE-ETG Schlüsseltechnologie für nachhaltiger Energietechnik, 2004, Berlin, Germany
7. European Power Electronics Conference EPE'05, September 2005, Dresden, Germany

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I am grateful to my co-advisors Prof Eckhard Wolfgang and Prof. Leo Lorenz for leading me to the industrial world of power electronics and giving me an opportunity to accomplish this PhD work in industry. Especially I want to thank Prof. Wolfgang for technical supervision and enabling me to accomplish this thesis despite of many other projects and limited time.

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## Used abbreviations

AC	Alternative Current
AC/DC	AC to DC Converter
A/D	Analogue to Digital
AlGaN	Aluminum Gallium Nitride
APS	Auxiliary Power Supply
APS	Autonomous Power Station
BIFET	Bipolar Injection Field Effect Transistor
CCM	Continues Current Mode
CMOS	Complementary Metal Oxide Semiconductor technology
DC	Direct Current
DC/DC	DC to DC converter
DCM	Discontinues Current Mode
DPS	Distributed Power System
DoE	Department of Energy
DSP	Digital Signal Processor
ESR	Equivalent Series Resistance
ESL	Equivalent Series Inductance
FET	Field Effect Transistor
FB	Full Bridge also H-Bridge
GaN	Gallium Nitride
GTO	Gate Turn Off switch
H-Bridge	Full Bridge converter topology consisting of 4 switches
HB	Half Bridge converter topology consisting of 2 switches
HF	High Frequency
HV	High Voltage
ICE	Internal Combustion Engine
IEEE	Institute of Electrical and Electronics Engineering
IGBT	Insulated Gate Bipolar Transistor
IPM	Integrated power modules
IPEM	Integrated power electronics modules (future integrated systems)
JFET	Junction Field Effect Transistor

LF	Low Frequency
LV	Low voltage
MCT	MOS Controlled Thyristors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTBF	Mean Time between Failures
P-N	PN Junction
PE	Power Electronics
PFC	Power Factor Corrector circuit
PiN	P intrinsic zone N diode
PSPICE	PC Simulation Program with Integrated Circuit Emphasis
PWM	Pulse Width Modulation
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SIT	Static Induction Transistor
SMPS	Switch Mode Power Supply
SOI	Silicon On Isolator
UPS	Uninterruptible Power Supply
VLSI	Very Large Scale Integration circuit
WBG	Wide-Band-Gap
WWW	World Wide Web
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching

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# 1 Introduction

## 1.1 Background and Motivation

The most important tasks in any power supply design procedure are:

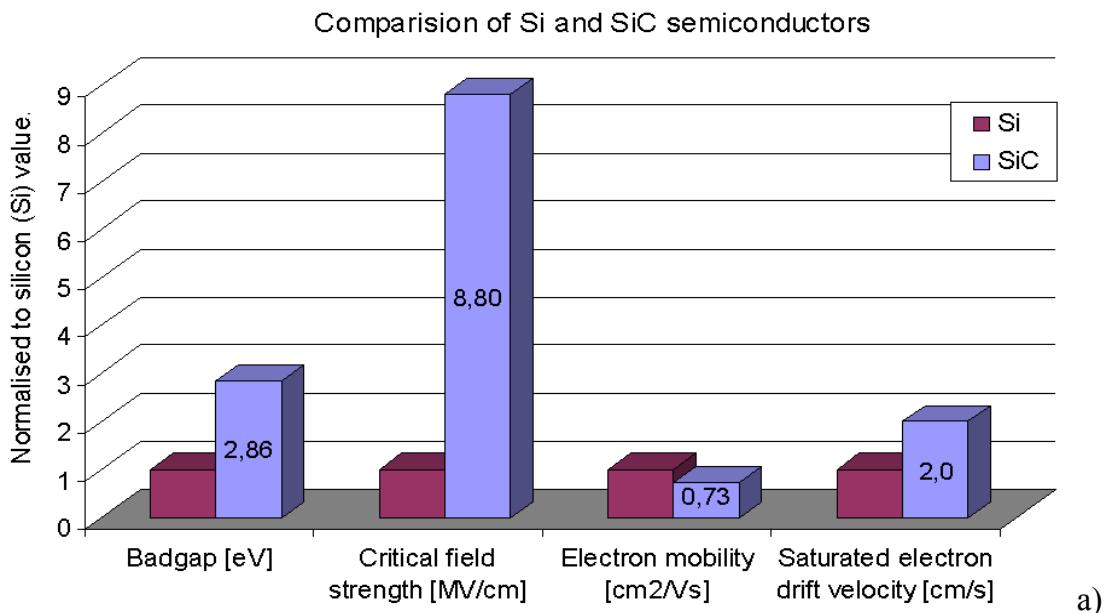
- ✓ reduction of the power losses – efficiency improvement and
- ✓ reduction of the size and weight together with increasing of the output power - hence increase of power density.

However, there is no single solution for both tasks. The trade off between size, cost, weight and efficiency can not be exactly determined and is usually driven by market requirements. Finding a solution for one parameter is usually accompanied by shifting the problem to other parameters. For instance an improvement in secondary switch mode power supplies (SMPS) towards higher power density can be achieved mainly by reducing their passive components (transformers, inductances, capacitors, filters etc.), which is possible by increasing the switching frequency. Increase of the frequency is basically restricted by the limited high frequency capabilities of the switching devices leading to increased switching losses and, eventually, to decreasing of the efficiency. Although some known techniques allow further increase of frequencies in the common circuits (e.g. resonant converters), the resulting converter topologies become in many cases more complicated and for large input / load variations sometimes difficult to control and stabilize. In such cases increase of power density becomes less evident, because during comparisons all the peripheral components, like control circuitry, snubbers, input and output filters, heatsinks etc. should be taken into account. Complex, sometimes with DSP controlled power converter systems are becoming increasingly costly.

Control and topology simplicity are the product differentiators of today's power converters and for mission critical, high temperature and harsh environment applications these properties are mandatory.

In contrast, reduction of the switching losses can be achieved also with lower switching frequencies and utilizing novel multilevel topological solutions, which can additionally increase the system reliability [62], [95]. Nevertheless, extremely reduced switching frequency could impact the overall power density, making such converters suitable for specific applications only

On the other hand, the power semiconductor development has recently shown big achievements in wide band-gap (WBG) technology and in related power devices [11]. Silicon carbide, being the most feasible semiconductor for power devices, has received a lot of attention during the last decade. The very high electric breakdown field makes it most suitable semiconductor for using in high power devices (Figure 1-1). Because of



**Figure 1-1 Electrical properties of the SiC compared to the Si; values are normalized**

much higher allowable electrical field, active devices like rectifiers and switches can be designed with more than ten times thinner and shorter semiconductor structures (drift layers) resulting in very much lower specific on-state resistance. In principle, SiC offers not only higher breakdown voltage, but also higher thermal conductivity, higher saturated electron drift velocity and inherent ability to operate at much higher junction temperatures because of the low intrinsic carrier concentration associated with the wide band-gap (WBG) [65], [77], [98]. All of these is well known and widely documented in the recent literature. What is less documented, is how these properties transform into device or system benefits that silicon power electronics can not realize, – this is the main subject of this thesis. Among already commercially available SiC Schottky barrier diodes (SBD) from Infineon [107] and Cree [107], within past two years also SiC power transistors - SiC

JFETs from SiCED [14]<sup>1</sup> became available as samples for research and development. However, due to technological constraints the price and production cost of SiC devices will remain always higher than the production costs of Si counterparts [6]. Additionally the unknown properties of the SiC transistors slow down the expected large and fast market acceptance. After replacing the Si power transistors and diodes in the commonly used SMPS topologies by high speed, high voltage, high temperature but also rather expensive SiC counterparts, designers were not able to see “the big” efficiency or power density improvements. Moreover, the higher cost and complexity of the resulting converters were dominant.

A question rises – how and in which power converter topologies the SiC power devices can be effectively utilized? Which properties of SiC devices allow increasing the power supply performance?

It becomes necessary to find out another approach in the design procedure of the well adopted converter topologies: - settled hierarchies of the applicable power ranges in the different topologies and design selection decisive factors are less suitable for the implementation of the new power devices like SiC JFETs. Many simple, single-switch topological solutions had been considered in former time as “not applicable” for higher<sup>2</sup> power ranges because of lack in fast, high frequency and high voltage power transistors. In order to overcome the maximum allowable drain voltage limitations of existing MOSFETs, so called multi-switch topologies are utilized, where the applied voltage is blocked by either series connected lower voltage transistors or by clamping the drain voltage to the input voltage level. Today, when the SiC devices are available, it should be verified, whether the single switch topologies can be revived and favorably used. With putting them in practice, the overall power system will become simpler and, despite of used expensive SiC device, can be more economical. By using system relevant approach for the power supply design the system efficiency as well as reliability could be drastically increased.

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<sup>1</sup> As of February 2002 to December 2003 the SiC JFETs from SiCED GmbH, were only available silicon carbide transistors for R&D in Europe

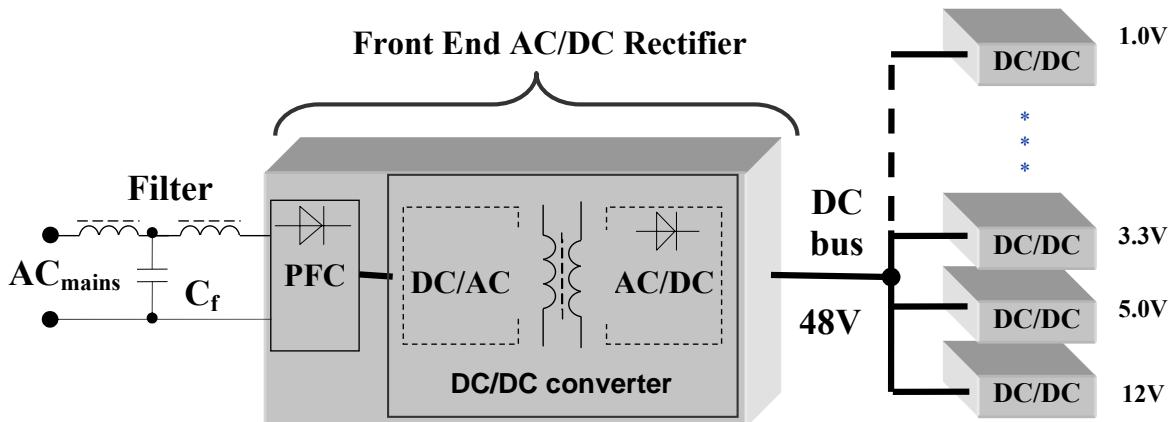
<sup>2</sup> “high” is considered as over 500W. The separation of switch mode power supplies in “low” power and “high” power in this thesis is given informally.

## 1.2 Application requirements & trends

Among the main requirements, such as high efficiency and power density, every electrical or electronic application has its own, specific requirements to the power supply. Targeting to general switch mode power supplies, in the following we will shortly review some challenging application areas like telecom, automotive, energy applications and point out whether and how SiC devices can be used for their performance increase.

### 1.2.1 Telecom application requirements

In the vast variety of server or telecom power supplies, the so called Distribute Power System (DPS) are widely adopted. In such systems, power is processed by two stages. Firstly the mains AC input is rectified, boosted up to 400V DC level then converted back and regulated to 48V intermediate DC bus by front end converter. In the second stage this DC voltage is distributed to the loads by the DC/DC non-isolated converters. The simplified block diagram of the commonly used DPS is illustrated in Figure 1-2

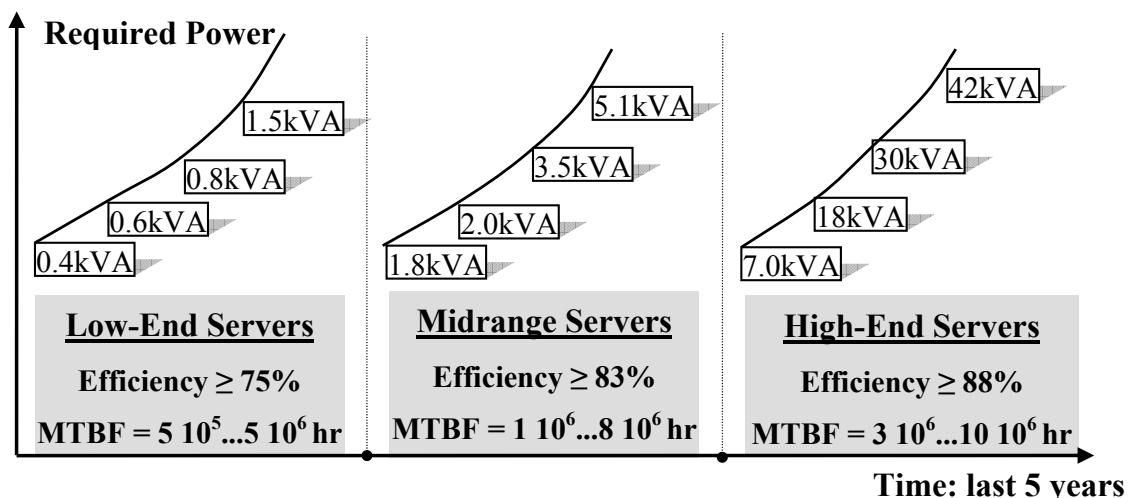


**Figure 1-2 Distributed power system architecture with isolated AC/DC rectifier providing 48V DC bus, which is loaded with DC/DC non-isolated point of load (POL) converters**

The main challenges in this application are following:

Firstly, by increasing of integration degree in digital electronic, more and more transistors are integrated to the system with faster switching frequency (VLSI). The power demand of digital system is increasing dramatically. The power supply, as a supporting subsystem, also expected to be less expensive and provide more power with smaller volume – increase of power density becomes essential part of any new development of power converter for telecom applications.

With integration of digital electronics, the profiles of the systems which are to be installed in racks are becoming another driving tendency in industry. More and more digital systems becoming highly integrated and, therefore, can be built with very low profiles. Consequently it is intended to have the system power supplies in low profile too in order to be mechanically compatible with digital components and systems. Nowadays the systems normally have a profile of 1.5U (1U ~ 4cm), and the tendency is moving towards 1U power systems [85]. In Figure 1-3, the trends for output power density,



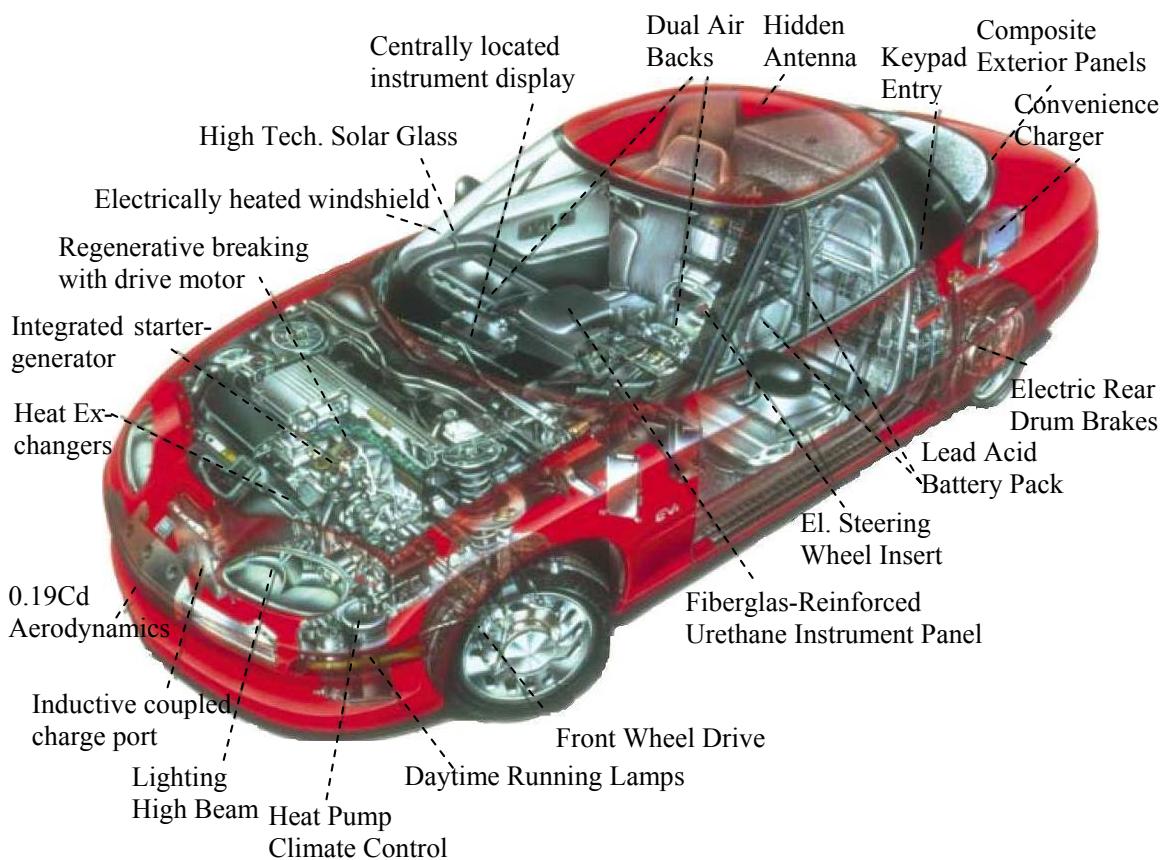
**Figure 1-3 Trends for AC/DC rectifiers: During the last 5 years the power demands in each server category are increased 4-6 times accompanied with 5% efficiency increase.**

efficiency and lifetime (MTBF) are shown over the past 5 years. For each server category the power demand has increased almost 4 times, for high-end servers even 6 times. The efficiency needs to be increased by more than 5%. To achieve this improvement 30% to 50% reduction of system power loss is required [85]. From above discussions can be concluded, that the trend for power supplies depends from digital system evolutions. During last few years, the digital systems shrunk more then tenfold. However miniaturization and integration of the power supplies for server/telecom applications with currently available technologies is hardly possible. Shrinking the volume and space will cause an increase of environmental and operating temperatures of the components. There is an obvious need of new semiconductor technology, which is inherently suited for elevated temperature operation. Correspondingly, new cooling or temperature management systems together with high temperature packaging are becoming mandatory. Important to note, that an integration and tight packaging of today's complex converters is hardly possible. The simplification of the topologies should be the first step towards integrated power electronics modules - IPEM [59]. This aspect will be discussed in Chapter 5.1. The

issues with high temperature passive components and packaging will be briefly reviewed in Chapter 3.

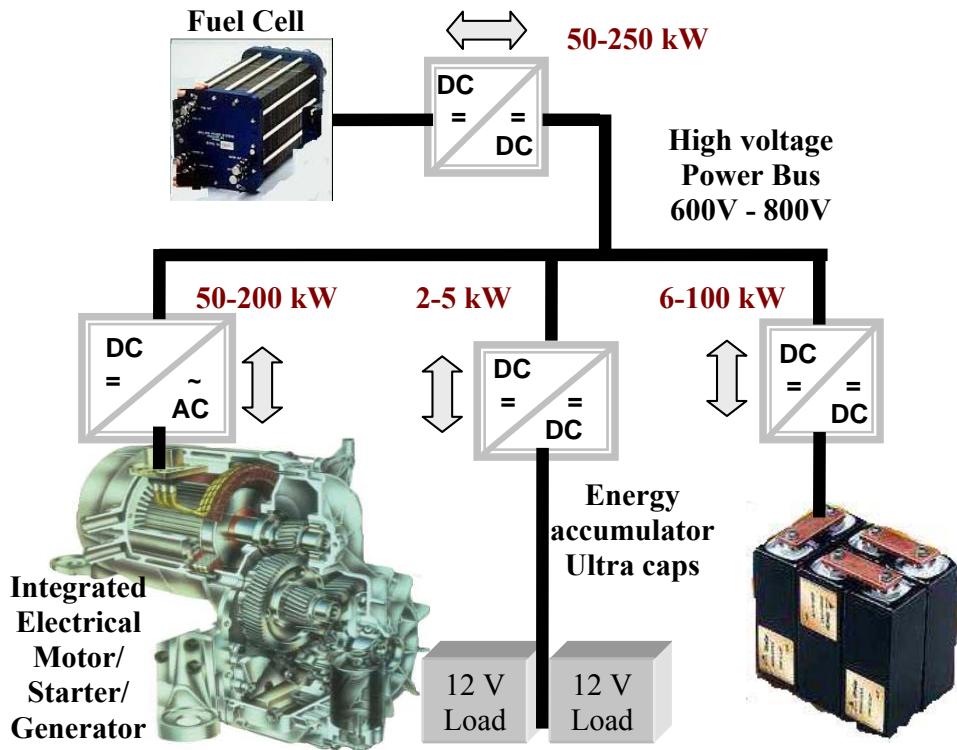
### 1.2.2 Automotive application requirements

During the last few years the requirements for transportation electronics have been drastically changed, attracting the automotive industry towards mechatronics (integration of electronics and mechanical systems, e.g. electronics in transmission). Figure 1-4 [General Motors] illustrates the emergence of electronics in automotive branch, where the DC/DC and DC/AC power converters are becoming inevitable part of present and future vehicles. On the other hand, they are also considered as one of the critical parts, which contribute to the mass and volume of the vehicle, and correspondingly have the direct influence on the acceleration and overall efficiency of the vehicle.



**Figure 1-4 GM EV<sub>1</sub> - The Power Electronics in Hybrid Vehicles [GM]**

The schematic diagram illustrated in Figure 1-5 shows where in vehicle the electrical power conversion takes place, as well as installed type and power levels of the converters. High temperature power electronics rated at temperatures well above 125 °C would eliminate present-day box placement design constraints.



**Figure 1-5 Schematic diagram of high voltage power bus and installed DC-DC and DC-AC converters for different power levels in hybrid electrical vehicle**

This will reduce the number of wires and connectors in the engine, which can improve long-term reliability. X-by-wire systems (X- throttle, steer, shift, brake etc.) are under development, and will dominate in future vehicles [74]. Also elevating the operating temperature of power devices up to 150°C will simplify the temperature management by using common cooling systems both for power electronic (PE) and internal combustion engine (ICE). Table 1-1 shows some ambient temperature ranges in automotive applications [25], [83]. The major source of heat affecting the vehicular electronics is the heat generated by the active devices, especially by the power semiconductors themselves.

Under -hood	100-125 °C	On Wheel	150-250°C
On-Engine (ICE)	150-200°C	Cylinder	200-300°C
In-Transmission	150-175°C	Exhaust	850°C, ambi. 300°C

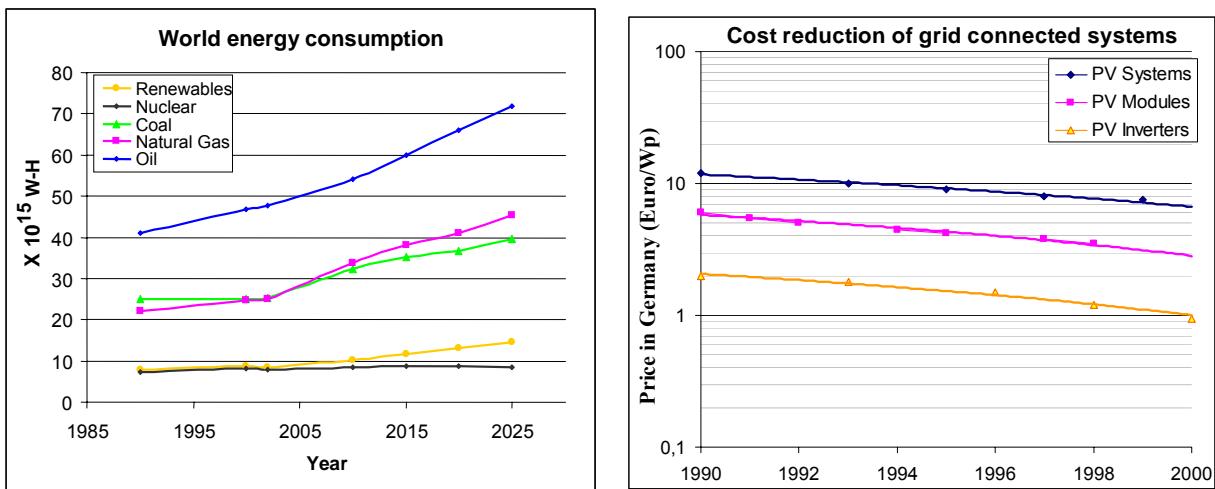
**Table 1-1 Automotive maximum ambient temperatures**

Because of high currents and high frequencies both the conducting and the switching losses are contributing to the overall temperature increase. The amount of losses depends mostly on the type of power devices used. Due to limited power capability, the unipolar MOSFETs are not used in today's traction drives, but IGBT and PiN diodes.

However, bipolar devices have limited switching frequency range and generally higher switching losses compared to the MOSFETs and Schottky diodes. Having high breakdown voltages (over 1200V) and high switching frequencies yet keeping ON-state resistance very low in Si MOSFET is hardly possible, - a material with a higher electric breakdown field is required. The SiC could be the best suited semiconductor, where its inherently high operating temperature capability together with high breakdown voltage and switching frequency can be advantageously utilized.

### 1.2.3 Requirements in energy and in harsh environment applications

Energy is the most important aspect for economic and national security. The worldwide energy demand will continue to rise. According to Department of Energy projections (DoE) [38], next twenty years the natural gas and oil will be still the dominant source of energy, despite of alternate energy sources: Figure 1-6. However, the easy recoverable oil and gas will be diminishing in supply, and their recovery will be from deep wells. In the well with hundreds of kilometers depth, the temperature is varying from 180 °C to 450 °C and more (180° C is considered minimal for direct electric power generation.).

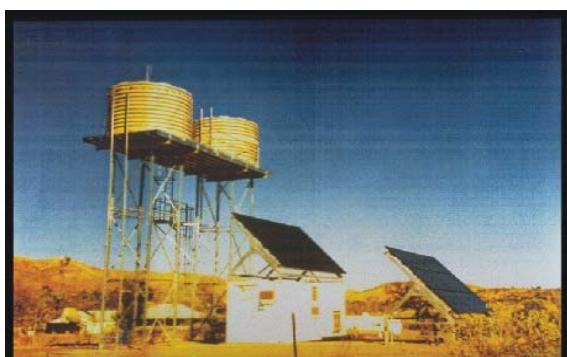


**Figure 1-6 a)** Next years the oil and natural gas will remain as dominant source of energy [38].  
**b)** The cost reduction of PV converters shows the same tendencies as for PV modules, making power converter developers to find out simple and cost competitive solutions [96].

Presently, there is no any electronic hardware system or module that can survive in such a harsh, high temperature and high pressure environment and the drillers have to explore these depths without an appropriate instrumentation. Drilling in this manner is very costly, slow and inaccurate. Currently geothermal industry uses a Dewar-flask a (double-walled evacuated housing) that protects the internal electronic power supplies and sensors for

approximately 10 hrs within a 300° C. Taking in account that the voltage references are limited today up to 150 °C and most passive devices up to 180 °C, the power supply with less components and simplest topology together with high temperature active devices can gradually improve the situation.

Power electronics converters are already an integrated part of the whole renewable energy system. The accelerated growth of energy development from renewable sources sets increased demand on the high efficiency, reliable and high power density converters. The learning curve of the converter cost reduction Figure 1-6 b) [96], shows the same tendencies as for PV modules, which stimulate designers to find out innovative, simple and cost effective power supply solutions. In rural and hard accessible regions the solution for 1kW power supply is the autonomous photovoltaic station [80]. In these regions, such systems are mostly installed for public live supply and medical care net, therefore only reliable and maintenance free uninterruptible electrical power systems (UPS) can be used.



a)



b)

**Figure 1-7 Solar energy applications, where the maintenance cost of any component can be unacceptable high. A) Alpine cot Ponti in Italy and b) Water supply station in Australia [80]**

Figure 1-7a) shows the water supply station (part of a 4kWp hybrid system) for a small commune in central Australia located some hundred kilometers far from the next town Alice Springs. Some places are so hard to access, that every visit for maintenance is extreme cost-intensive Figure 1-7 b) shows the PV supplied Alpine cot Ponti in Italy, which is possible to reach only with helicopter. In such systems additional investment in compact, highly integrated autonomous power supplies, which are free from the regular upholding, is beneficial. The power converters realized with SiC, which can be integrated in future high temperature robust modules, will allow eliminating the mechanical moving parts such as fan cooling. Resulting converter will be maintenance-free, with increased reliability, and better suited for mentioned renewable energy applications.

### **1.3 Thesis objective**

The objective of this thesis is to investigate the new SiC devices and find out a suitable topology, where the specific properties of the SiC devices are fully utilized.

After building a prototype converter with implemented SiC devices, the topology simplification, higher efficiency and higher power density should be obtained, which will provide a solution for future integration of the converters into high temperature integrated power electronics modules.

The following aspects should be studied:

1. Evaluation and characterization of the SiC JFET transistors to find out the properties which allow increasing power converter performance.
2. Determination of the SiC converter design technique - how to fully utilize the potential of SiC semiconductor in power converters while simplifying their topology
3. Investigate possible driving approaches of the SiC JFET in suitable topologies
4. Build up a prototype converter with silicon carbide power devices for performance evaluation and verification.

## 1.4 Outline of the thesis

The dissertation is organized as following:

**Chapter 1** has reviewed 3 challenging applications backgrounds:- Telecom, automotive and harsh environment energy applications. Their issues and specific requirements are identified.

**Chapter 2** will review the development roadmaps both for the semiconductor technology and for power converters. Classification of converter topologies and power losses which can be reduced by means of SiC devices will be studied.

In **Chapter 3** the vision towards miniaturization, integration and high temperature operation in power electronics and main obstacles to achieve this target will be presented.

**Chapter 4** will introduce the new SiC vertical junction field effect power transistor (SiC VJFET) and will investigate its specific properties.

In **Chapter 5**, the implementation of the SiC transistor in the power converters will be investigated, and possible simplification of the existing topologies will be proposed. This chapter examines some suitable topologies in order to fully exploit the possibilities of SiC transistors and diodes, especially towards operation with higher voltages and higher frequencies.

**Chapter 6** describes the realization of two new gate drive circuits for driving SiC JFETs

**Chapter 7** concentrates on the practical design, dimensioning and experimental results of the prototype converter

**Chapter 8** summarizes the most important findings in this thesis and concludes the work with suggestions for future investigations.

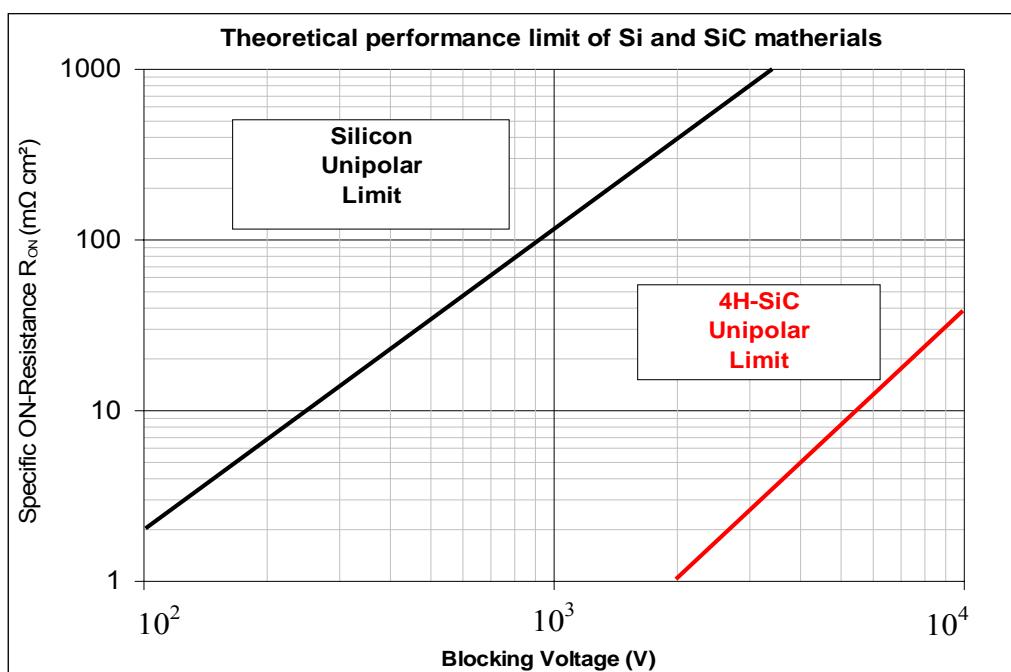
## 2 State of the Art

### 2.1 Roadmap of power semiconductor devices

#### 2.1.1 Wide band-gap semiconductors

*Silicon power devices are reaching their fundamental limits of performance  
J. Baliga, 1992.*

Imposed by the low breakdown field of silicon, power switching devices have reached their fundamental limits: Figure 2-1. Significant improvements can only be achieved by going to semiconductors with higher breakdown fields – wide band-gap semiconductors. Recent progress in a manufacturability of WBG power device technology shows that within the next 2 years two families can be available: SiC and GaN, whereas the SiC is the most mature and the closest to market. GaN and AlGaN also have high breakdown field and high carrier mobility, and could be ideally suited for power device implementation. However, the II-V nitride compounds do not possess a native oxide similar to  $\text{SiO}_2$ ,



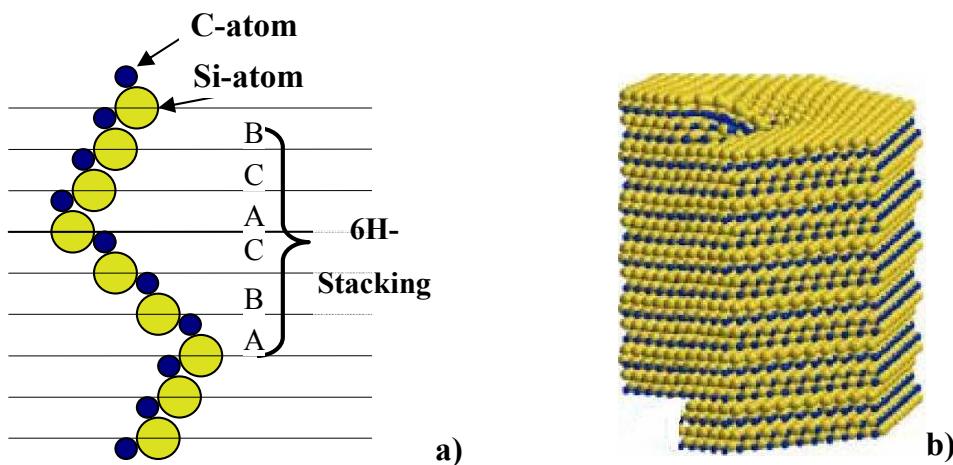
**Figure 2-1 Area specific ON resistance of SiC unipolar device, as figure of merit, shows theoretically 400 times better voltage breakdown capability than Si counterpart [11]**

therefore true MOS devices will not be feasible in near future [9]<sup>3</sup>. A good overview of the wide-band-gap (WBG) materials and the latest devices based on them including SiC transistors can be found in [11]. Numerous studies are carried out by NASA Glenn SiC Research Group and reported in e.g. [8], [109].

### 2.1.2 SiC technology and properties of the SiC

The SiC crystals chemically consist of 50% carbon atoms covalently bonded with 50% silicon atoms. There are over 100 different crystal structures (polytypes), each SiC polytype has its own distinct set of electrical semiconductor properties. However, only few polytypes are used for semiconductor production, - the cubic 3C-SiC, hexagonal 4H-SiC and 6H-SiC. The letter indicates the geometrical form of the crystal structure and the number shows the stacking sequence (see Figure 2-2a).

For example the 15R-SiC is the most common of many possible SiC types with a rhombohedral crystal structure.



**Figure 2-2 a)** Schematic cross section of the SiC polytype and **b)** its 3D image [8]

The most important electrical and thermal properties of SiC together with other common semiconductor materials, summarized from [9], [19] and [36] are given in the comparison Table 2-1. The SiC's superior properties have been known for decades; however, only reproducible wafers of reasonable size, quality and price are important for mass-production of semiconductor electronics. Si can be easily melted and again recrystallized, e.g. by Czochralski method, whereas the SiC sublimes instead of melting. This was the

<sup>3</sup> The literature survey of WBG semiconductor technology was carried out during 2002-2004. Recent publications have shown devices having quasi MOSFET behavior and normally off condition in certain operating ranges.

major obstacle for mass production. The first breakthrough technology for reproducible 6H-SiC crystal growth was established by Tairov and Tzvetkov in 1970's, called modified seeded sublimation growth [15]. Though the first 1-inch 6H-SiC wafer became commercially available already in 1989, the 4H-SiC with its substantially higher carrier mobility is the favourable choice for today's devices. Furthermore, 6H-SiC shows an inherent electron mobility anisotropy, which degrades the conduction parallel to the crystallographic c-axis, consequently for vertical power devices the 4H-SiC is the best choice. In 1993 the Cree Research LTD (D. J. Larkin, and J. A. Powell under NASA funding) first provided to market 2.5cm diameter 4H-SiC wafers. Same time T. Urushidani et. al. have presented in [52] a high voltage Schottky barrier diode blocking 1100V. This was the first milestone which increased the pace of industrial utilisation of SiC.

<b>Electrical Property</b>	<b>Si</b>	<b>GaAs</b>	<b>SiC (4H)</b>	<b>SiC (6H)</b>	<b>GaN (2H)</b>	<b>Diamond</b>
Band-gap Eg [eV]	1.12	1.42	3.28	2.96	3.4	5.5
Critical electrical field E <sub>Cr</sub> [MV/cm]	0.29	0.3	2.5	3.2	3.3	20
Relative dielectric constant [E]	11.9	13.1	9.7	9.7	8.9	5.7
Electron mobility $\mu_n$ [cm <sup>2</sup> /Vs]	1200	8500	800	370	1000	2200
Hole mobility $\mu_p$ [cm <sup>2</sup> /Vs]	490	320	115	90	30	1800
Thermal conductivity $\lambda$ [W/cmK]	1.5	0.5	3.8	3.8	1.3	20
T <sub>max</sub> [K]	400	460	873	873	900	2200
Commercial wafer diameter [cm]	30	15.4	7.62	x	5.0	1.2

**Table 2-1 Comparison of the silicon (Si) and wide band-gap power semiconductors: Gallium Arsenide (GaAs), Silicon Carbide (SiC), Gallium Nitride (GaN) and Diamond.**

Unfortunately, being a very "hard" semiconductor material, SiC often contains several crystal defects, whereas the most harming is the "micropipe" defect. It prevents the increase of defect-free wafer diameter, which directly affects the SiC electronics capability. A micropipe is a screw dislocation with a hollow core (a cave diameter on the order of micrometers) in the SiC wafer that extends roughly parallel to the crystallographic c-axis [7]. SiC wafers also contain high density of closed-core defects, which like micropipes, cause a localized strain and SiC lattice deformation [7], [13]. In addition to micropipe defects, there are also non-hollow core (elementary) screw dislocation defects in SiC wafers and epilayers.

While these defects are not considered as fatal as micropipes<sup>4</sup>, recent experiments have shown that they degrade the leakage and breakdown characteristics of P-N junctions: [10], [50] and [86]. Considering permanent defect density reduction, overall wafer quality improvement and consequent increase of device chip area, the power handling capability will grow exponentially until 2010 and, according to Ohashi [87], can reach 500kVA by 2018 (see Figure 2-3).

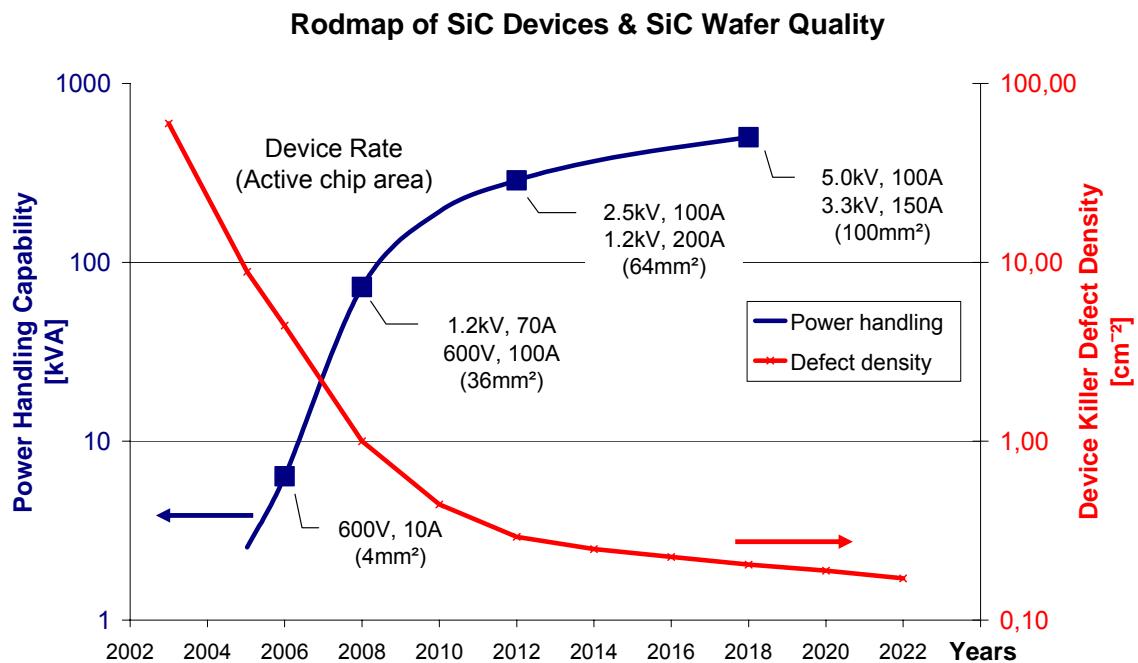


Figure 2-3 Progress in SiC Devices related to SiC material progress as enabling technology [87]

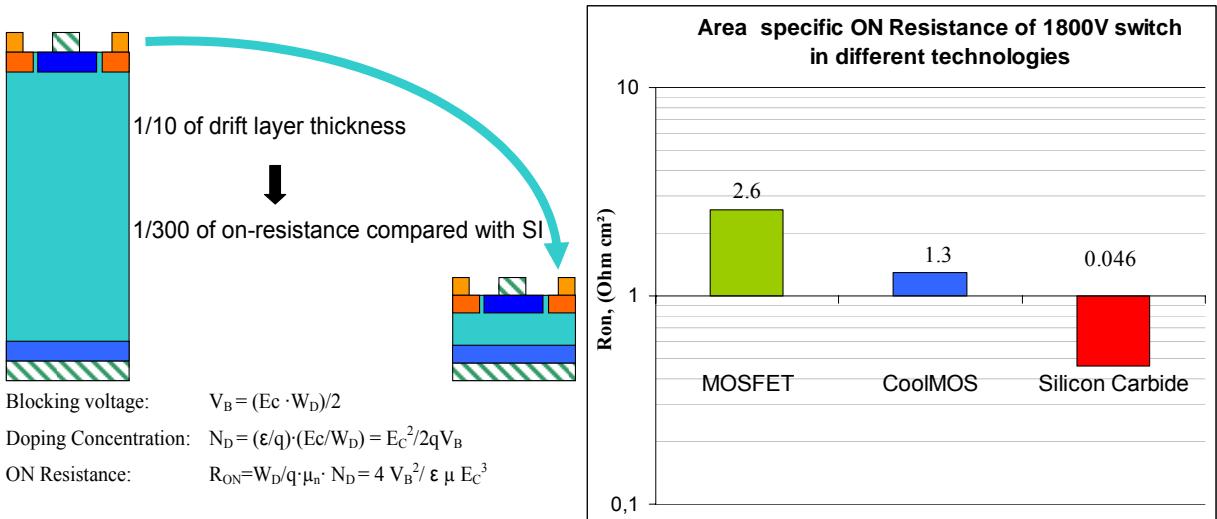
### 2.1.3 Power switching devices based on SiC semiconductor

#### MOS Devices

SiC is the most attractive compound semiconductor, because of its native oxide is  $\text{SiO}_2$  – comparable to oxides used in Si MOSFETs [4]. This means that the main power devices made-up in silicon, i.e. the power MOSFET, insulated gate bipolar transistor (IGBT), and MOS-controlled thyristor (MCT) can be fabricated in SiC too. However, because of technological differences, power devices in SiC will be very different from silicon devices, and a direct translation of silicon concepts to SiC is not always possible. As can be seen from Table 2-1 the SiC has a breakdown field app.10x higher than silicon,

<sup>4</sup> As of 2003 the micropipe crystal defects were biggest challenging task in SiC production. Recently Japan researches (H. Ohashi) have shown virtually defect free SiC wafers (EPE2005, CIPS 2006).

resulting to SiC power devices with very short depletion width  $W_D$  (Figure 2-4a) and with practically 50 lower specific on resistance (Figure 2-4 b) than similar devices in silicon.



**Figure 2-4 a)** Much shorter drift layer thickness in the SiC devices leads to the ultra low (theor.300 times) ON-state resistance. **b)** Area specific resistance of the SiC switch compared to the conventional and charge compensated Si MOSFETs shows 50 times improvement

A drawback of SiC is that the voltage of P-N junction is higher because of higher energy gap. This means that SiC diodes will have generally higher ON state voltages. The carrier mobility is also lower than in Si, consequently the inversion channel mobility in SiC MOSFET is much lower ( $<90 \text{ cm}^2/\text{Vs}$  for inversion electrons), which means that in lower voltage range the MOSFET devices will have lower gain and current carrying capability. Since the thin drift regions can not be utilized due to limited minimum achievable channel thickness, the higher ON-state resistance is expected.

The main advantage of the SiC MOSFET would be obvious only at medium to high voltage ranges 3...5 kV. Above these voltages the SiC IGBT could be better choice. Moreover, SiC oxides are not showing the same reliability as in Si MOSFETs. They have higher threshold voltage shifts, gate leakage, and oxide failures than comparably biased silicon MOSFET's, [47]. In [12] differences between the basic electrical properties of n-type versus p-type SiC MOS devices are discussed. One of the obvious differences between thermal oxidations of Si and SiC to form  $\text{SiO}_2$  is the presence of carbon (C) in SiC. While most of the C in SiC converts to gaseous CO and  $\text{CO}_2$  and evaporates from the oxide layer during thermal oxidation, remaining C resides near the SiC- $\text{SiO}_2$  interface. This has detrimental impact on  $\text{SiO}_2$  electrical quality [1]. Consequently much longer and higher temperature maintenance (annealing) is required to improve the SiC oxide quality.

## JFET Devices

Alok and Baliga [18] presented a high voltage 6H-SiC JFET for 450V. A buried gate JFET transistor is reported in [29]. In [35] Konstantinov et. al. have presented buried gate JFET with blocking voltages up to 600-700. Though there are many reports about different possibilities to realize SiC JFET, the only device available today, which can be practically implemented in the power converter circuits is the SiC VJFET from SiCED GmbH (available as engineering samples) [14].

## Other Devices

There are also reports about other emerging devices in development and their possible applications like:

SiC Metal Semiconductor Field Effect Transistor – MESFET: [44], [49]

Gate Turn OFF Switches – GTO: [17], [23] and

SiC Thyristors - [16], [48] .

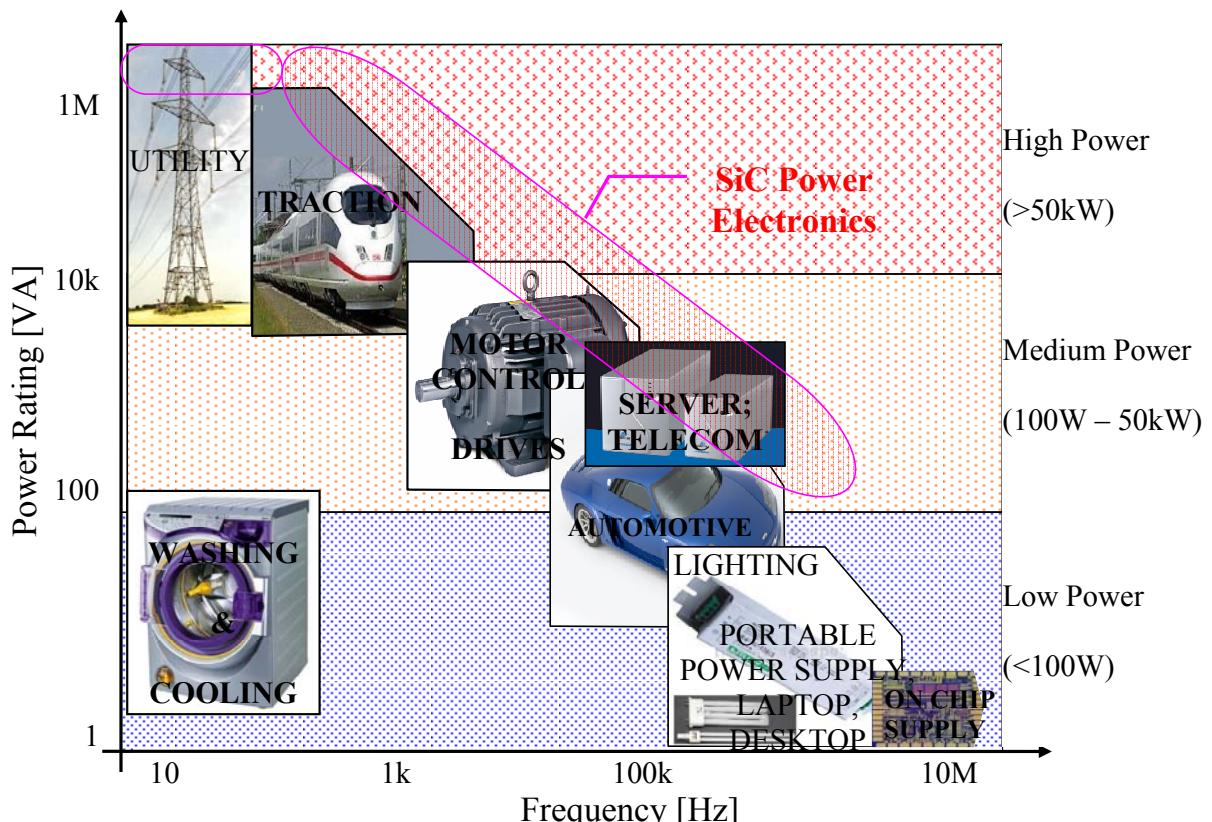
Japan researches have recently reported about laboratory samples of SiC bipolar transistors and IGBTs [Ohashi 2005]. There are also recent reports about bipolar transistors [24] with acceptable current gain [37]. Friedrichs [28] has recently reported that with heterojunction bipolar SiC transistor - Bipolar Injection Field Effect Transistor (BIFET) basically higher current gain is achievable. However some aspects should be studied, before the Bipolar Junction Transistors (BJT) can be reliably manufactured: 1) Identify the causes of limitations in minority carrier life time.2) How to create highly conductive and high quality p type wafers 3) How to manage the difficulties for paralleling of dies to get higher current [101].

Technology	Transistor Type	Operating Voltage [V]	Frequency Limit [MHz]	Possible Temperature [°C]	Integration Scale
SiC	Normally ON	> 1200	200	500	Discrete
GaN	Normally ON	> 15	100	300	Small
Vacuum Trans	Normally ON	> 500	2000	500	Discrete
SOI CMOS	Normally OFF	5V	20	300	Medium

**Table 2-2 Summary of the currently known high temperature transistor technologies**

Summarizing the given overview of the state of the art SiC semiconductor and emerging power devices based on it, we can state, that by means of SiC the application fields of currently known power semiconductors can be significantly widened. Of the many conceivable device benefits, the key one from the perspective of this study is the ability to meet system conditions with one device when silicon technology requires several. For example, the high voltage and switching speed of SiC diodes and transistors allow reducing the dynamic losses same way as Si Schottky diodes can do, however only for lower voltage levels. Based on above mentioned we will focus on those system aspects, that substantially reduce the size or complexity of the circuit in which SiC device is mounted. For example, by keeping all other boundary parameters constant, and by increasing the switching frequency of the high voltage power field effect transistors from 80 kHz up to 300-400 kHz, the volume and weight associated with passive devices can be drastically reduced. All this aspects will be discussed in details in next chapters.

Figure 2-5 shows the step by step emergence of the SiC devices in different applications: Switch mode power supplies → Industrial Drives and Motor Control → Traction → Utility and Megawatt applications



**Figure 2-5 Related voltage, current and frequency ranges for different power devices and their application range extension by means of SiC semiconductor**

## 2.2 Roadmap of power converters

*Today only 12% of the world electricity is switched by power semiconductors. This will change...  
Steffen Inc. 2002*

Nowadays, Switch Mode Power Supplies (SMPS) have to fulfil many end-application requirements like industrial, automotive, telecom etc. Power converters, being the most material- and energy- demanding parts in electronic equipment, often define their size-weight, exploitation, reliability and cost factors. Due to different nature of application requirements, especially the nominal power level of an end-user, there is a set of commonly used converter topologies for different products. Usually, in power supplies dedicated for power levels from 700W and higher, the multi-switch double-ended topologies are chosen [57].

### 2.2.1 Classification of main topologies

General secondary power supplies tree is illustrated in the following chart: Figure 2-6

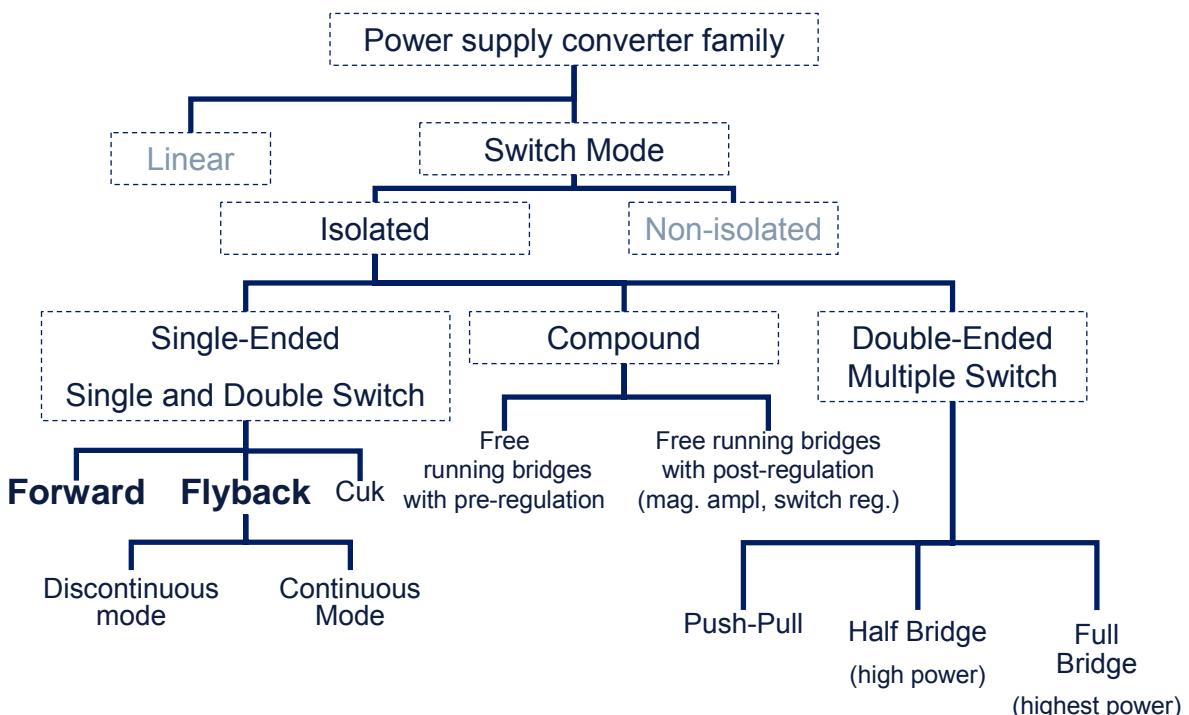
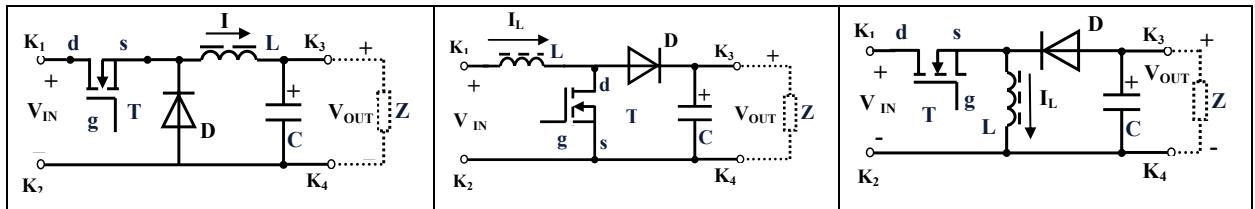


Figure 2-6 The secondary power supply converter tree

Assuming all components as well as the input power source ideal, two classes can be separated out from all possible converter topologies depicted in the Figure 2-6:- converters with finite energy accumulation (Buck Converter) and converters with infinite energy accumulation (Boost Converters) [86]. Designing and use of the power converters requires understanding of their main characteristics. The majority of the converter topologies are derived from 3 fundamental types: I- Buck, II -Boost and III- Inverting (Table 2-3). Though being a basic topology, the Inverting converter (Buck-Boost) is not fundamental, since its characteristics can be obtained with series connection of two previous fundamental converters. Basically these three topologies have the same components (Switch, Diode, Inductor, and Capacitor), but differently connected to the load side (Table 2-3). It is this “outer” side of the converter that classify the converters to the mentioned types.



**Table 2-3 Fundamental topologies: Buck, Boost and Inverting converters**

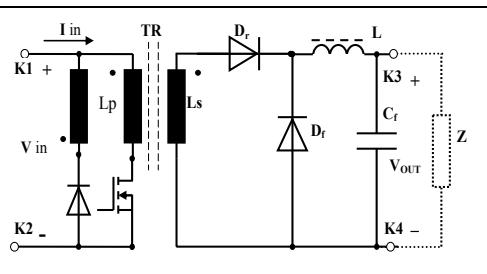
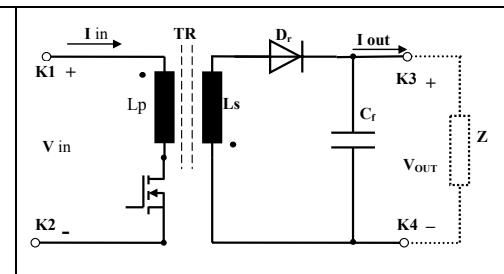
There are 3 different operation modes in that the power converter can operate:

- Continues Conduction Mode (CCM) – operation with continues magnetic flux in inductive components
- Discontinues Conduction Mode (DCM) - operation with discontinuous magnetic flux in inductive components
- Critical conduction mode (BCM) – boundary operation between two modes

Regarding the way how the energy is taken from source and provided to load, converters can be classified as:

- Pulsed energy consumption from source and continues energy output to the load (I)
- Continues energy consumption from source and pulsed energy output to the load (II)
- Pulsed energy consumption from source and pulsed energy output to the load (III)

Further investigation of the converters in this thesis is based on two isolated “Forward” and “Flyback” converters, which can be derived from the fundamental converters [90]. Their basic characteristics and main relationships between input, output and regulation parameters are derived in [A1] and summarized in the Table 2-4. Due to isolation transformer the output voltage and current are recalculated to the primary side.

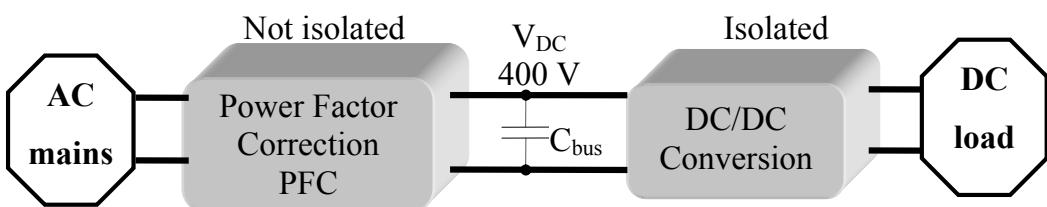
Topology		
Regulation characteristics CCM	$U_{Load} = D \cdot U_{IN} \frac{n_s}{n_p}; D = \frac{t_{ON}}{T}$	$U_{Load} = \frac{D}{1-D} U_{IN} \frac{n_s}{n_p}; D = \frac{t_{ON}}{T}$
Regulation characteristics DCM	$U_{load} = U_{IN} \cdot \frac{n_p}{n_s} \frac{D^2}{4 \cdot \tau_{LR} \cdot f} \cdot \sqrt{1 + \frac{8\tau_{LR} \cdot f}{D^2}}$ $\tau_{RL} = \frac{L_p}{R_{Load}}$	$U_{load} = U_{IN} \cdot D \cdot \sqrt{\frac{1}{2 \cdot \tau_{LR} \cdot f}},$ $\tau_{RL} = \frac{L_p}{R_{Load}}$
BCM Boundary operation	$I_{load} = U_{IN} \cdot \frac{n_p}{n_s} \frac{D \cdot (1-D)}{2 \cdot L \cdot f}$	$I_{load} = U_{IN} \cdot \frac{D \cdot (1-D)}{2 \cdot L_p \cdot f} \frac{n_p}{n_s}$
Ideal output characteristics	$U_{load} = U_{IN} \cdot \frac{n_p}{n_s} \frac{D^2}{D^2 - \frac{2 \cdot L \cdot I_{Load} \cdot f}{U_{IN}}}$	$U_{load} = U_{IN} \cdot \left( \frac{D^2}{2 \cdot L_p \cdot I_{Load} \cdot f} \right)$
Real output characteristics	$U_{Load} = U_{IN} \cdot \left( D - \frac{I_{Load} \cdot r}{U_{IN}} \right)$	$U_{Load} = U_{IN} \cdot \left( \frac{\frac{n_s}{n_p} \frac{D}{1-D} - D \cdot r_p \left( \frac{n_s}{n_p} \right)^2 + r_s (1-D)}{U_{IN} \cdot (1-D)} \right)$
Switch min and max currents	$I_{\frac{min}{max}} = I_{Load} \mp \frac{U_{IN} \cdot D \cdot (1-D) n_p}{2 \cdot L \cdot f} \frac{n_p}{n_s}$	$I_{\frac{min}{max}} = \frac{n_s}{n_p} \frac{I_{Load}}{1-D} \mp U_{IN} \frac{D}{2 \cdot L_p \cdot f}$
Switch maximum voltages	$U_T = V_{IN} \cdot \left( 1 + \frac{n_p}{n_{aux}} \right)$	$U_T = U_{IN} + U_{Load} \frac{n_p}{n_s} = \frac{U_{IN}}{1-D}$ $U_D = \frac{n_s}{n_p} \frac{U_{IN}}{1-D}$

Switch current (ave.)	$I_T^{ave} = \frac{n_s}{n_p} I_{Load} D$	$I_T^{ave} = \frac{n_s}{n_p} I_{Load} \frac{D}{1-D}$
Switch current (RMS.)	$I_T^{RMS} = \frac{P_{Load}}{U_{IN} \sqrt{D}}$	$I_T^{RMS} = I \cdot \sqrt{D} = \frac{P_{Load}}{U_{IN} \sqrt{D}}$
Switch power stress	$P_S = \frac{P_{out}}{D}$	$P_S = \frac{P_{out}}{D \cdot (1-D)}$
Output voltage ripple	$\Delta U_{CF} = \frac{U_{IN} \cdot D \cdot (1-D)}{8 \cdot L \cdot C_F \cdot f^2}$	$\Delta U_{CF} = \frac{I_{Load} \cdot D}{C_F \cdot f}$
Output impedance in CCM	$R_{OUT} = r$ , where $r$ is overall active ohmic resistance of the windings and interconnections	$R_{OUT} = \frac{r_s}{(1-D)^2}$ , where $r$ is overall active ohmic resistance of the secondary winding and interconnections
Graphical form of regulation characteristics		
Graphical form of output characteristics		

**Table 2-4 The main characteristics of the Forward and Flyback topologies for all operating modes with ideal and real components**

### 2.2.2 State of the art topologies

Converters become more specialized, standardized and modulised. Basically, similar results can be achieved with different converter topologies if we perfect them. Therefore this dissertation is targeted to general power supply converters. However, as an example, the challenges, issues and solutions will be given for 1kW DC/DC converter, which is a part of AC/DC rectifier. The so called “Front End AC/DC Rectifier” is usually the first power conversion step in distributed power systems (DPS), described in Chapter 1.2. The simplified block diagram of front-end converter is shown in Figure 2-7

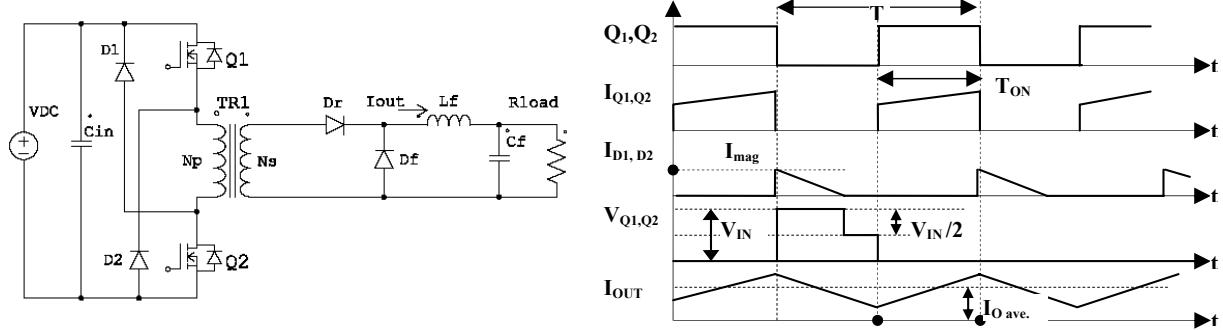


**Figure 2-7 Two stage architecture of front end rectifier**

The power factor correction stage (PFC) converts the rectified input AC line voltage to standard  $400V_{dc}$  and the DC/DC converter converts this  $400V_{dc}$  into regulated  $48V_{dc}$ . While the PFC, as single-switch boost converter, can be realised with high performance devices like CoolMOS™ and SiC Diodes for power ranges 1-2 kW [91] and with frequencies up to 400kHz [82], the DC/DC stage needs careful design considerations to obtain the same performance in the given power range. For a single-phase system, the power level of DC/DC converters typically lies in range of 1kW. For higher power levels the parallel connection of the converters can be used. Today's industrialized designs of front-end DC/DC converters evolve usually full-bridge, two switch forward and half-bridge converters. Next, these topologies will be reviewed and their main issues will be discussed for the given application.

#### Two switch forward converter

The schematic and corresponding waveforms of the double-switch forward converter are shown in Figure 2-8 [61], [73] and [102]. The big advantage of this topology is its robustness. Since two switches are connected in series with transformer, the shoot trough problem, which exists in other totem poll configurations, is solved. During OFF time the transformer is demagnetized by reversed input voltage applied to the primary through two clamp diodes.



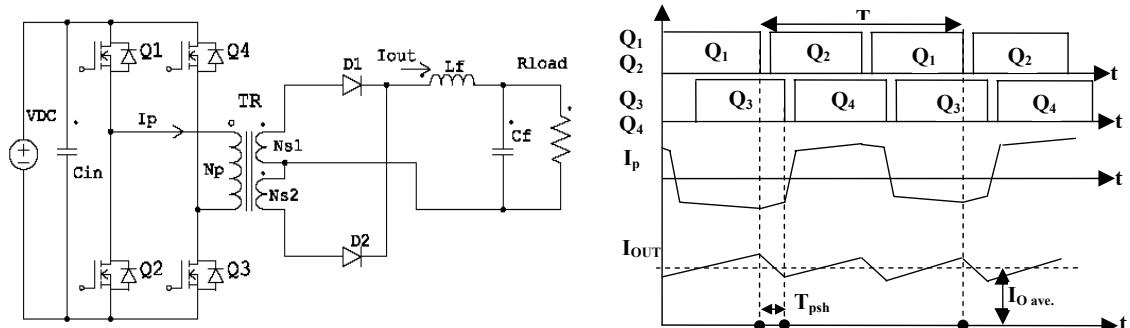
**Figure 2-8 Double switch forward converter and its switching waveforms**

After demagnetization, in the dwell stage, there is no current in primary side, while secondary side is freewheeling. Because of clamped drain voltages on the switches and the inherent robustness of the topology, it is often implemented in aerospace power supplies, where they are additionally exposed to high energy radiation.

The major disadvantage of the double switch forward converter is the hard switching (has higher switching losses) and despite of using two switches, it has rather high output voltage modulation depth – and therefore needs larger output inductor. Because of series connected switches during energy transfer period, the conduction losses are also higher compared to single transistor topologies. Due to transformer reset requirement, the maximum duty cycle is limited to 0.5. Therefore the energy transfer can take place as maximum during half of the switching period. This leads to the increased RMS current through the power switches.

### Phase shifted full bridge converter

The full bridge and its operating waveforms are depicted in Figure 2-9 [58], [93]. Phase shift full bridge converter is one of the most popular topology for high power application. It can operate as soft switching converter. All four switches on primary side can achieve

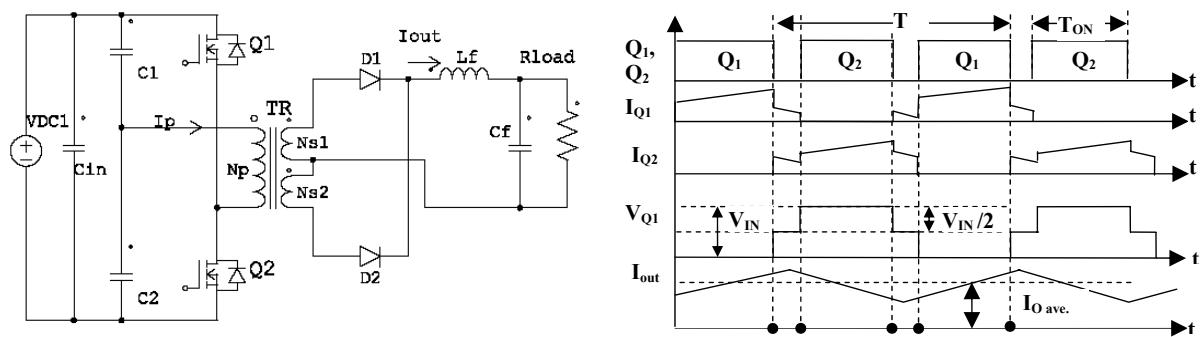


**Figure 2-9 Full bridge phase shift converter and operating waveforms**

Zero Voltage Switching (ZVS), therefore high frequency operation is possible. On the output filter the twice switching frequency and therefore lower volt-sec is applied. Though, there are several disadvantages for phase shift full bridge topology. The biggest one is the complexity. The high and low side switches should be appropriately controlled and unavoidable dead time issues must be considered. With large leakage inductance, which is necessary for ZVS, the duty cycle loss due to charge and discharge of leakage inductance will be significant. This limit the choice of transformer turns ratio and decrease the performance of whole converter. In light load operation ZVS can be lost. The second drawback is the circulating reactive current. From waveforms we can see, that in every switching cycle during “OFF” time, the transformer primary side shorted with two upper or lower transistors. It will increase the conduction loss. The smaller the duty cycle, the more circulating current will be.

### Half bridge converter

The next common topology, used in midrange telecom power supplies, is the balanced version of the forward converter – the Half Bridge converter. Since both transistors are effectively in series, they never see greater voltage than the supply voltage  $V_{in}$ . When both are OFF, their voltages reach an equilibrium point of  $V_{in}/2$ . The biggest disadvantage of this topology is the need for two low frequency input capacitors (lowest possible). Furthermore, if snubbers are used across the power transistors (during dead time), great care must be taken in their design, since the symmetrical action means that the snubbers can interact with one another. The circuit cost and complexity have clearly increased, and this must be weighted up against the advantages gained. The Table 2-5 summarizes the main advantages and limitations of the common topologies used SMPS.



**Figure 2-10 The half bridge converter and its switching waveforms**

Topology	Advantages	Disadvantages
<b>Flyback*</b> <sup>f</sup>	No output filter inductor is needed Low cost multiple output voltages Suited for high voltage outputs ZVS is possible	Coupled inductor transformer Higher core size and costs Unidirectional core excursion Much higher output ripples Large output filter capacitor Higher peak drain current Double drain voltage ( $>2V_{\text{input}}$ )
<b>Single Transistor Forward *</b> <sup>b</sup>	Continuous output inductor current Lower output voltage ripple Smaller peak current handling No air gap - true transformer Smaller transformer Smaller output filter capacitor	Additional reset winding Additional reset diode Unidirectional core excursion Max. practical duty cycle = 0.5 Double drain voltage ( $>2V_{\text{input}}$ ) Hard switching
<b>Push-Pull</b>	Bidirectional transformer excitation Leakage and magnetisation energy are recuperated	Flux symmetry imbalance Centre-taped transformer Interaction between snubbers Shoot trough problem Double drain voltage ( $>2V_{\text{input}}$ ) Hard switching
<b>Two Transistor Forward</b>	Drain voltage is clamped to $V_{\text{in}}$ No demagnetising winding No shoot trough problem Bidirectional transformer excitation Robust	Limited duty cycle ( $< 0.5$ ) Higher RMS current* <sup>H</sup> Unidirectional core excursion Lower efficiency (2 in series) Isolated high side driver Hard switching
<b>Half Bridge</b>	Drain voltage is $V_{\text{in}}$ Leakage and magnetisation energies are dumped into input capacitors Bidirectional transformer excitation	Two bulky input capacitors Interaction between snubbers Isolated high side driver Increased circuit cost and complexity Higher primary RMS current Shoot trough problem Flux symmetry imbalance
<b>Full Bridge</b>	Drain voltage is clamped to $V_{\text{in}}$ Bidirectional transformer excitation Low output ripple Highest output power capabilities ZVS possible Bidirectional transformer excitation	Highest circuit cost and complexity Four transistors are needed Two isolated high side drivers Reactive circulating power if ZVS realised Shoot trough problem Flux symmetry imbalance
<b>*Comments</b>	compared to: * <sup>f</sup> –Forward, * <sup>b</sup> –Flyback, * <sup>H</sup> – Half and Full bridges	
<b>Table 2-5 Main advantages and limitations of the common topologies used SMPS</b>		

## 2.3 Power losses in SMPS

In order to be able to increase the efficiency of the converter, it is important to identify how the losses appear and where the energy is dissipated.

From many different types of losses, originating from almost every component installed in the converter, in this thesis we will discuss only that loss sources which are relevant to the projected topology and can be minimized through the implementation of SiC devices.

### 2.3.1 Losses in active devices

Generally the losses in power switching devices can be separated to dynamic – hence switching transient losses and static – hence conduction losses.

#### Diode static losses

The conduction loss of the diode is directly proportional to its forward voltage drop and series resistance. Ideal diode characteristics can generally be presented by the following equation:

$$I = I_S \cdot \left( e^{\frac{q(V - I \cdot R_S)}{nKT}} - 1 \right), \text{ where} \quad (2-1)$$

$I_S$  - is the saturation current,  $q$  - is the magnitude of electron charge ( $1.601 \times 10^{-19}$  C),  $k$  - is the Boltzmann's constant ( $1.3805 \times 10^{23}$  J/K),  $T$  - is the temperature in Kelvins,  $n$  - is the ideality factor,  $V$  is the voltage across the diode,  $I$  is the current through the diode, and  $R_S$  – is the diode series resistance.

The PWL models are already supplied by SiC diode manufacturers (Infineon [108], Cree Research [107]). Their parameters in this work are obtained from I-V characteristics. The conduction losses can be expressed as:

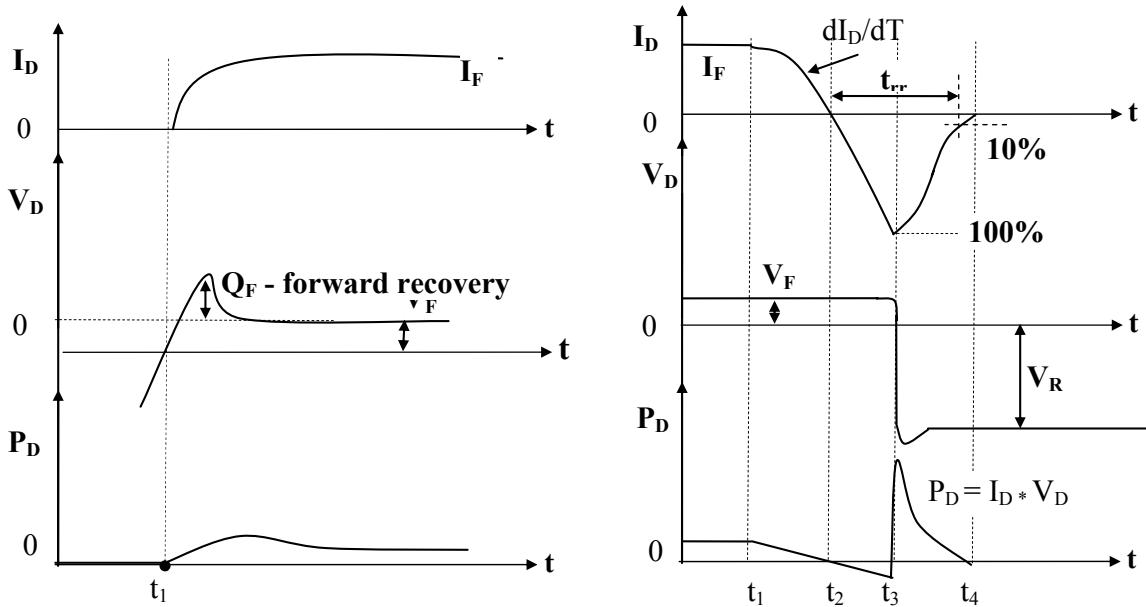
$$P_{cond} = I_{DC} \cdot V_D + I_{DC}^2 \cdot R_S \quad (2-2)$$

The  $V_D$  and  $R_D$  values are temperature dependent, and should be taken into account during loss calculation. It is important to note that Si and SiC diodes have different temperature dependences. The SiC has positive temperature coefficient (until certain current level), whereas the Si diode  $R_S$  is decreasing with temperature.

#### Diode switching losses

The switching losses are the sum of turn ON, turn OFF and reverse recovery losses. For turning ON a bipolar power diode, the depletion layer of the P-N junction has to be flooded with charge. This slightly lifts the voltage drop and consequently the forward

recovery losses. At high switching frequencies the turning OFF process is more critical. The diode can not support reverse voltage until the reverse current reaches its peak. Only when the stored space charge  $Q_R$  is swept out from depletion region, the diode can be turned OFF. This accounts for the pulse of energy dissipation shown in Figure 2-11 b)



**Figure 2-11 Switching waveform of power diode: a)  $P_D$  conduction loss is due to forward voltage drop. b) Pulse  $P_D$  is caused by stored charge remaining after peak of reverse voltage**

The reverse recovery current pulse has ramifications also on the power switches. In single-ended applications, where the diodes are connected on the secondary side for rectification, the transformer winding is effectively short circuited by the diode in the first part of the  $t_{rr}$ . The current pulse is reflected through to the main switch (described later for transistor losses) and increases power losses there.

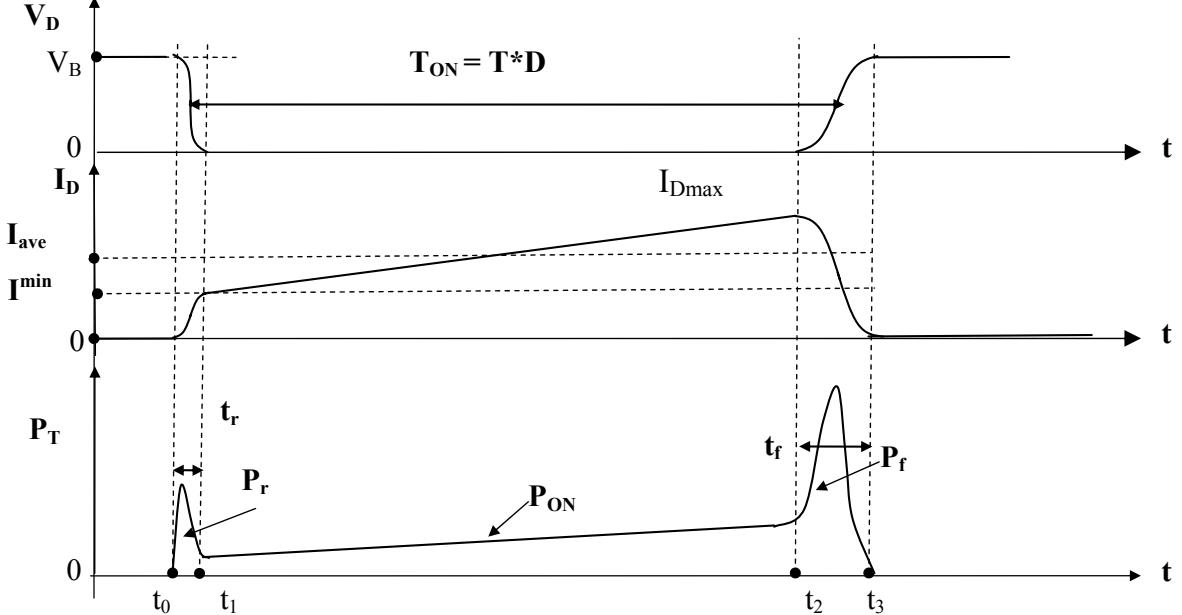
In this thesis therefore, SiC Schottky diodes will be chosen which are free from the mentioned drawback. However as it will be shown in practical results, the SiC diodes experience a capacitive displacement reverse current during hard switching and higher  $V_F$ .

### Transistor losses

Switching losses in transistors discussed here will be based on power MOSFET transistor and generalized for FET switching devices. However, where applicable the specific differences related to JFET switches will be mentioned explicitly. Like in diodes, in power transistors also two types of losses can be identified: switching losses and conduction losses. The static losses occur due to not zero drain to source resistance of the switch. The “ON” state loss can be expressed through the well known product of this on-state resistance and drain current:

$$P_{cond} = I_D^2 \cdot R_{DS}^{ON}, \text{ where } I_D - \text{ is the RMS current through the switch.} \quad (2-3)$$

From the simplified switching waveform depicted in Figure 2-12, we can see that the short time for edges taken for switching is increasing with increase of switching frequency. At low frequencies the static conduction losses are dominating and can be averaged over the whole period T:  $P_{ON} = D \cdot \left( \frac{I_{D\min} + I_{D\max}}{2} \right)^2 \cdot R_{DS}^{ON}$ . The  $R_{DS}$  depends on specific ON resistance of the material discussed in Chapter 2.1.



**Figure 2-12 Power transistor losses due to finite switching times and  $R_{DS}(ON)$**

The switching losses can be calculated using piece-wise integration of the switching curves during turn ON and turn OFF:  $V_{DS} = -\frac{V_{IN}}{t_r} \cdot t + V_{IN}$  and  $I_D = \frac{I_{D\min} t}{t_r}$ ,

The energy dissipated and over period T is:

$$P_r = \frac{1}{T} \int_0^{t_r} v_{DS} \cdot i_D dt = \frac{1}{T} \int_0^{t_r} V_{IN} I_{D\min} \cdot \left( 1 - \frac{t}{t_r} \right) \cdot \frac{t}{t_r} dt = \frac{V_{IN} \cdot I_{D\min} \cdot t_r}{6T} \quad (2-4)$$

and for turn OFF:

$$P_f = \frac{1}{T} \int_0^{t_f} v_{DS} \cdot i_D dt = \frac{1}{T} \int_0^{t_f} V_{IN} I_{D\max} \cdot \left( 1 - \frac{t}{t_f} \right) \cdot \frac{t}{t_f} dt = \frac{V_{IN} \cdot I_{D\max} \cdot t_f}{6T} \quad (2-5)$$

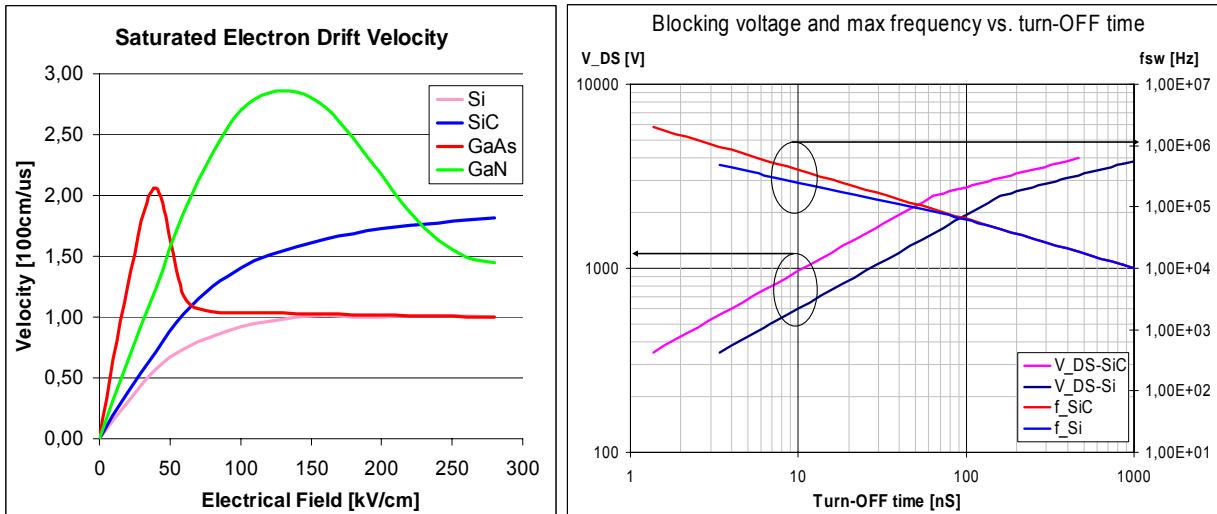
The overall power loss will be the sum of turn ON, turn OFF and static losses

$$P = P_{ON} + P_r + P_f = D \cdot \left( \frac{I_{D\min} + I_{D\max}}{2} \right)^2 \cdot R_{DS}^{ON} + \frac{V_{IN}}{6} \cdot (I_{D\min} t_r + I_{D\max} t_f) \cdot f_{sw} \quad (2-6)$$

As we can see from Figure 2-12 and from expressions above, the losses are increasing and efficiency is decreasing with increase of switching frequency. Thus for minimizing  $P_r$  and  $P_f$ , fast rise and fall times ( $t_r$ ,  $t_f$ ) are required. Unfortunately the high voltage Si MOSFETs can not offer required high switching speeds, whereas SiC devices, thanks to the double of the saturated electron drift velocity and smaller semiconductor structures, have much higher switching speed and high voltage capability (Figure 2-13a). To further quantify these losses, we can take the loss terms associated with switching of inductive or capacitive loads. E.g. for large inductive loads, the voltage is turned ON and OFF very rapidly while the current remains practically constant. Generally, the turn-on time ( $t_r$ ) is much shorter than the turn-off time ( $t_f$ ), consistent with the behavior of most semiconductor switches. It can be approximated that the drain voltage first increases linearly over time  $t_f$  to the bus voltage  $V_B$ , while the drain current is fixed. Then the current decreases linearly to zero in time  $t_f$ , while the voltage remains fixed. Under this assumption and with taking the duty cycle DC=50%, the total power dissipation can be approximated as:  $P_D = \frac{1}{2} I_{ON} \cdot V_{ON} + I_{ON} \cdot V_B \cdot t_f \cdot f_{sw}$ . By limiting the turn-OFF loss level  $P_s = \frac{1}{2} (V_B - V_{ON}) \cdot I_{ON}$

to  $P_{lim}$  the maximum frequency can be found as:  $f_{sw}^{\max} = P_{lim} \cdot \left( \frac{(V_B - V_{ON})}{V_{ON}} - 1 \right) / 2 \cdot t_f$ . The reduced

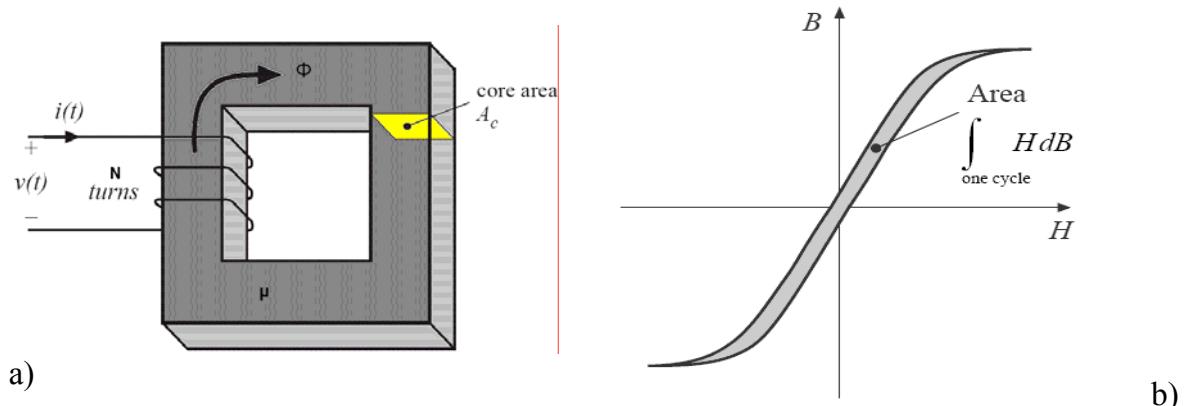
$t_f$  by SiC switches leads to an increase in  $f_{\max}$  in the manner shown in Figure 2-13b) E.g. for blocking voltage 1000V the  $t_f$  is equal to 25ns for Si and 10ns for SiC. This corresponds respectively to 100 kHz for Si and app 800 kHz for SiC (values for Si are experimental, values SiC are projected).



**Figure 2-13 a)** High saturated electron drift velocity enables high speed SiC switching devices with **b)** drastically decreased switching times and at higher blocking Drain-Source voltages

### 2.3.2 Losses in magnetic devices

By introducing SiC devices in power converters, their switching frequency can be drastically increased. The increase of power density however is possible as far as the volumes of passive magnetic components can be decreased. Therefore, development of high frequency, high power density and high temperature magnetic components together with higher efficiency is of paramount importance. Because of excessive losses in transformers an optimal frequency is approached, beyond which no appreciable gain in transformer power density can be realized. For currently available magnetic core materials mentioned optimum frequency upper limit is located app. at 250 – 300 kHz (found experimentally). Generally in magnetic components two types of losses can take place: low frequency or DC losses and high frequency losses. DC losses appear only in windings due to copper active resistance, whereas high frequency losses can appear both in magnetic core, as hysteretic and eddy-current losses, and in windings, as skin and proximity effects. Noticeable, that to the high frequency losses in the core contributes not only main switching frequency, but also effects of PWM waveform harmonics and DC flux bias.



**Figure 2-14 a)** Magnetic core model with flux  $\Phi$  flowing through area  $A_c$ ; **b)** Core loss is proportional to the Hysteresis integral area. Minimization of the losses leads to reduction of the core volume max flux level

## Hysteretic losses

Core energy per cycle W flowing into N-turn winding of an inductor, excited by periodic waveforms of frequency f:

$$W = \int_0^T v(t) \cdot i(t) \, dt \quad (2-7)$$

Faraday's law for induced voltage and Ampere's law for induced current are correspondingly:

$$v(t) = n \cdot A_C \cdot \frac{dB(t)}{dt} \text{ and } H(t) \cdot l_m = n \cdot i(t) \quad (2-8)$$

Substituting (2-8) into (2-7) integral will result:

$$W = \int_0^T \left( n \cdot A_C \cdot \frac{dB(t)}{dt} \right) \cdot \left( \frac{H(t) \cdot l_m}{n} \right) \cdot dt = A_c \cdot l_m \int H \cdot dB \quad (2-9)$$

The term  $A_C * l_m$  is the volume of the core, while the integral is the area of the B-H loop

$$P_H = f \cdot (A_c \cdot l_m) \cdot \int_{\text{one cycle}} H \cdot dB \quad 2-10$$

Hysteretic loss is directly proportional to applied frequency. Both hysteretic and eddy-current losses arise from complicated processes inside the magnetic material [70]. Hysteretic losses can be estimated using an empirical equation predicted by the theory of magnetic domains: The parameters  $K_H$  are determined experimentally

$$P_H = K_H \cdot f \cdot B_{\max}^\alpha \cdot (\text{core volume}), \quad 2-11$$

## Eddy-current losses

Eddy-current losses are due to the finite conductivity of the magnetic material and have a non-integer power dependence on the frequency of excitation over the useful range of frequency of operation of the material. From provided total core loss curves and specified values for  $K$ ,  $a$  and  $b$ , following empiric (Steinmetz equation) can be used:

$$P_E = K_E \cdot f^a \cdot B_{\max}^b \cdot (\text{core volume}) \quad 2-12$$

In these equations,  $B_{\max}$  is the peak flux density and  $f$  is the frequency of core excitation. The exponents "a" and "b" are non-integers so that  $K$  has very cumbersome and meaningless units. A better, physically understandable approach, "a fractal model" can be used, where magnetization process and the eddy currents are regarded as not uniformly distributed, but very localized in the core [103].

### 3 Miniaturization and integration in power electronics

Previous chapter has shown that modern power electronics requirements are more than that, what the Si-based semiconductor technologies can offer today. Requirements in automotive, telecom, energy and other applications show clear needs of high temperature, high power density, cost effective power supplies. A way out to achieve these target is to follow the digital system evolution (Moor's law) and make an integration in the power electronics. From the comparison of digital and analog (power supply) systems, it is possible to recognize some similarities between information and energy processing systems (Figure 3-1). In signal processing system the input analog signal is quantized with A/D converters and, after processing it, converted back to analog signal with D/A converters. Power systems also quantize the analog power with PWM converters or choppers and after filtering deliver the output analog power to the load. While digital systems need energy from power supply for information processing, power systems need controlling signals and information for power processing.

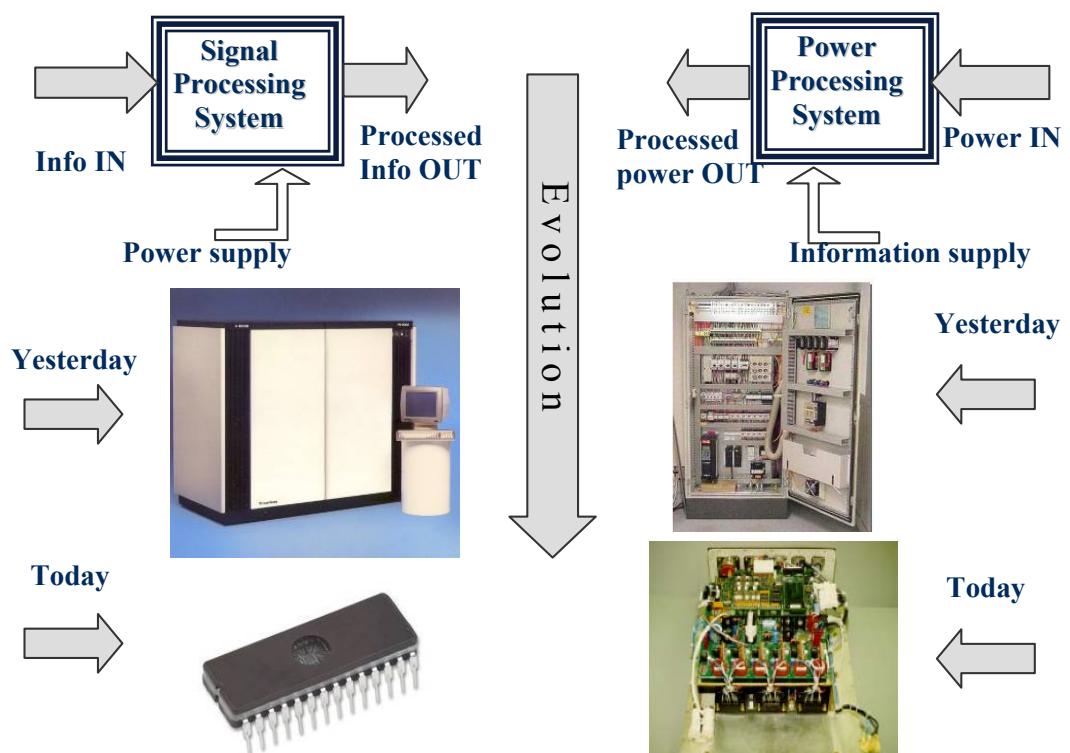
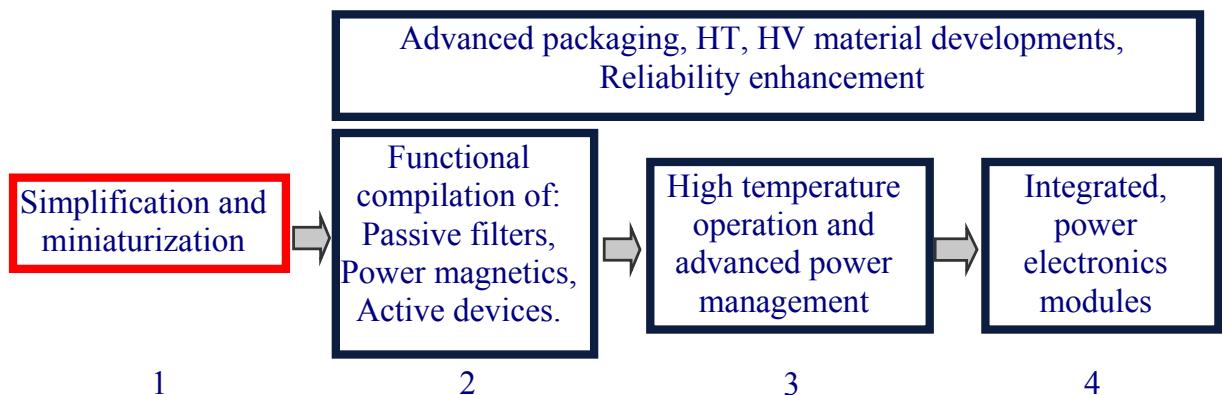


Figure 3-1 A signal processing system contrasted with a power processing system

However, the advancement towards integration of power systems was not as much as in digital one. The state-of-the-art converters still require lot of space for driving circuitry, for cooling and for passive components. Especially filter capacitances and inductors are very hard to miniaturize. For enabling the integration of power electronics modules, the standardization, modulisation is important. The goal is to obtain power electronics building blocks, which can be cascaded for any custom power demands. This approach can drastically reduce touch labor and production costs of power supplies. Following 4 steps are proposed (Figure 3-2) to achieve the mentioned target:



**Figure 3-2 A vision for integrated power electronics – 4 Steps towards high power density integrated power electronics modules:**

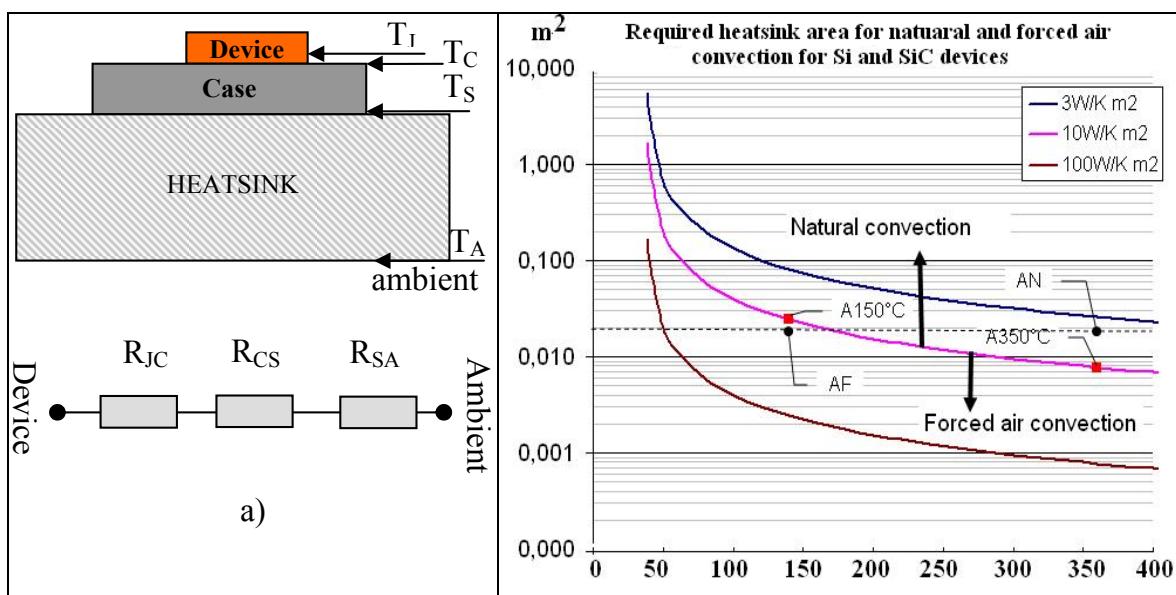
On top of all: high temperature, high voltage packaging and reliability enhancement should be incorporated at the beginning of integration process –see Figure 3-2

1. In order to be able to integrate power converters, its topology must be extremely simple and easy to control- this part is covered in this thesis. It will be shown that SiC allows the simplification of power converters.
2. The integration process itself should incorporate passive elements and combination of functionally different elements like capacitors and inductors in one device [59].
3. If all components are tightly packed in one module the temperature increase will be unavoidable – advanced power management and device cooling must be realized.

In the following it will be shown how the SiC technology can help to realize advanced power management.

### 3.1 Enhanced thermal management in SiC power converters

As already described in Chapter 2.1, SiC with its refractory nature gives inherent capability to operate at higher temperatures than traditional silicon at approximately the same level of electrical performance (i.e., efficiency, speed, etc.) To clarify the impact of higher junction temperature on device and system performance, assume that the device is packaged in the case shown in Figure 3-3a), soldered to a case and the case is bonded to a heatsink.



**Figure 3-3 a)**The simplified thermal model of the power chip packaged and attached to heatsink; **b)** Increased temperature of the SiC ( $350^\circ\text{C}$ ) vs. Si ( $150^\circ\text{C}$ ) chip allow changing the forced air cooling by the natural convection using the same heatsink surface area.

Further it is assumed that the heatsink can transport heat to the ambient environment by either conduction or convection. The package has 4 reference temperatures:  $T_J$  - semiconductor device junction,  $T_C$  – at device to case interface,  $T_S$  – at case to sink interface and in the ambient environment -  $T_A$ . Taking the whole energy to be dissipated to equal  $P_0$ , for this model the junction temperature is related to the ambient temperature as:

$$R_{JA} = \frac{T_J - T_A}{P_0} = R_{JC} + R_{CS} + R_{SA} \quad 3-1$$

As an example the widely used 5-A, 600V Si MOSFET packaged in TO-220 case is chosen. Assuming that the operating frequency is low enough it dissipates a static power of 25W. The maximum junction temperature of the device is limited to  $150^\circ\text{C}$  according datasheet. This will be compared to a SiC device having the same power characteristics, but a maximum junction temperature of  $350^\circ\text{C}$ . Both devices are assumed to have an

active area of  $0.15 \text{ cm}^2$ , consistent with the moderate current density of  $100 \text{ A/cm}^2$ . The thermal resistance from junction to case in TO220 according datasheet is  $T_{JC} \sim 1,4^\circ \text{ K/W}$  and from case to heat sink  $T_{CS} \sim 0,1\text{K/W}$ . The sink-to-ambient thermal resistance  $T_{SA}$  depends entirely on the sink area and the heat-removal strategy. For natural convection the heat flux capacity is in range of  $3-10 \text{ K/Wm}^2$  and for forced air it falls in the range  $10-100 \text{ K/Wm}^2$ . Putting these quantities into equation above, we can estimate the necessary sink area vs. the junction temperature rise  $\Delta T$ , which is presented in Figure 3-3 b) for the three boundary values of the sink-to-ambient heat-flux capacity. The upper curve defines the typical range of natural convection, while the lower curve defines the typical range of forced-air convection. These curves illustrate two important facts about higher operating temperature:

- ✓ The first is that the higher temperature will allow smaller heat-sink area for the same packaging technology. This is illustrated through the two operating points (A150) and (A350) for the Si and SiC device, located at  $150^\circ\text{C}$  and  $350^\circ\text{C}$ , respectively. Each point is located on the boundary curve, above which a natural and below which a forced-air convection must be maintained. The resulting sink areas are  $240 \text{ cm}^2$  and  $76 \text{ cm}^2$  for the Si and SiC devices, respectively. This results to heat-sink for SiC with app. 50% less dimensions then for Si devices.
- ✓ A second important fact is that by means of higher operating temperature in SiC a complete change in the thermal management approach for a given packaging area is possible: - This can be illustrated through the two operating points (AF) and (AN) in Figure 3-3 b) at  $150^\circ\text{C}$  and  $350^\circ\text{C}$ , respectively, and both fixed in area at  $0.02 \text{ m}^2$ . It is visible that point (AF) lies within the range of forced-air convection, while point (AN) is well within the range of natural convection. This means that the Si device would require a fan but the SiC device could operate without one. This will allow to eliminate the mechanical parts which are usually accompanied by mechanical vibrations, acoustic noise, and environmentally-dependent failure mechanisms that can limit the reliability of the overall power system. Hence, the higher operating temperature of SiC will provide a superior thermal management solution for the application cases mentioned in Chapter 1.2.3, where the system architecture does not allow forced-air convection or where the system environment (e.g., wet conditions, dust or pollution level etc.) impacts the reliability of a fan.

### 3.2 Passive components and packaging issues in high temperature power electronics

Today's commercially available power electronic devices have maximum rated operation temperature about 100°C (125°C junction) – far below those required in challenging applications and in high density power modules (Chapter 1.2). While at temperatures from 250°C to 300°C the leakage current and latch-up problems for low power, signal electronics can be solved with Silicon On Isolator technology (SOI), for high power electronics at temperatures over 300°C the solution can be found only in wide band-gap semiconductors, like SiC or GaN[38]. The theoretical temperature limits of various solid-state semiconductor technologies, derived from their band-gaps and carrier mobilities, are given in Table 3-1.

Technology	Theoretical limit [°C]	Practical limit [°C]
Si	400	225
SOI ( signal level only)	400	300
GaN	900	600
SiC	900	600
Thermionic vacuum devices	1000	600

**Table 3-1 Capability of high temperature semiconductor technologies: Theoretical temperature limit derived from band-gap and carrier mobility of the semiconductors, and practical limit achieved in experiments on unpackaged laboratory samples [38], [49], [109]**

It can be seen, that theoretical temperature limits are much higher than practically achievable device temperatures. They are mainly determined by:

- ✓ Metallurgical contacts of the devices
- ✓ Electromigration within metal traces
- ✓ Time dependent breakdown of the gate dielectrics
- ✓ Defects in semiconductor, which become fatal at elevated temperatures

Important to note, that the presented results of practical limits are valid for laboratory samples only. The real long-term, high temperature capabilities of the devices are much lower and limited by packaging, interconnect and die attach reliabilities. On the other hand, for complete integrated power electronics modules, the high temperature passive devices must be available too. Development of HT passive devices has had mixed success. Currently, thick film ruthenium oxide resistors are capable for long-term working under 500°C [46], [42]. In contrast, the general purpose ceramic capacitors have shown wide

variation in capacitance with increased temperature. Particularly, the leakage current of the capacitor increases so much, that the capacitor can not hold the charge anymore. Nowadays known most promising and stable capacitor for 500°C operation could be NP0 ceramic capacitor. Unfortunately its leakage current at 300°C is becoming very high. The piezoelectric capacitors can be designed for specific temperatures and have shown good dissipation stability, but the capacitance variation over temperature is very big. Various alternative dielectric materials like diamond, etc. are under research; however large capacitance values (over 1uF) and voltages (over 100V) for 300°C operation is not feasible in near future. The lifetime of the passive components for high temperature power electronics depends not only on the survivability of resistive elements, dielectrics or magnetic cores, but also on the component packaging, ohmic contact and soldering technology. These are most common failure sources in electronic devices which are not designed for high temperature applications.

High temperature packaging has following radical differences:

1. Decomposition or melting of materials
2. Coefficient of thermal expansion (CTE) mismatch
3. Interdiffusion of different metal layers or interconnects
4. Electromigration

A summary from [25], [26] of maximum allowable temperatures and limiting properties for selection of die bond-pad / wire bond combinations is given in Table 3-2

Metals: Pad-Wire	Max Temperature	Properties / Comments
Al-Au	175 °C	Forms brittle intermetallic phases which reduced bond strength and conductivity
Ni-Al	260 °C	Interdiffusion creates excessive voids that decrease bond area strength
Au-Au	500 °C	1 mil Au wire bond 5000hr in oxidizing air with 50mA DC; 500 thermal cycles

**Table 3-2: Maximum temperatures and limiting factors of the selected bondpad-wire metallurgical combinations [25], [26].**

Important to note, that some power electronics applications, like automotive, aerospace etc. beside the temperature are exposed to other extreme environmental conditions too, including wide thermal cycles, shock, vibration, fluids and corrosive gases.

## 4 State of the art SiC JFET power transistor

### 4.1 Overview

#### 4.1.1 Principle of operation

There are 2 different types of junction field effect transistors (JFETs): the N type and P type (Figure 4-1), which refer to the polarity of the majority charge carriers in the channel of semiconductor that connects the drain terminal D to the source terminal S. Since the channel is formed from a single-polarity material, its resistance is a function of the geometry of the conducting volume and the conductivity of the material only.

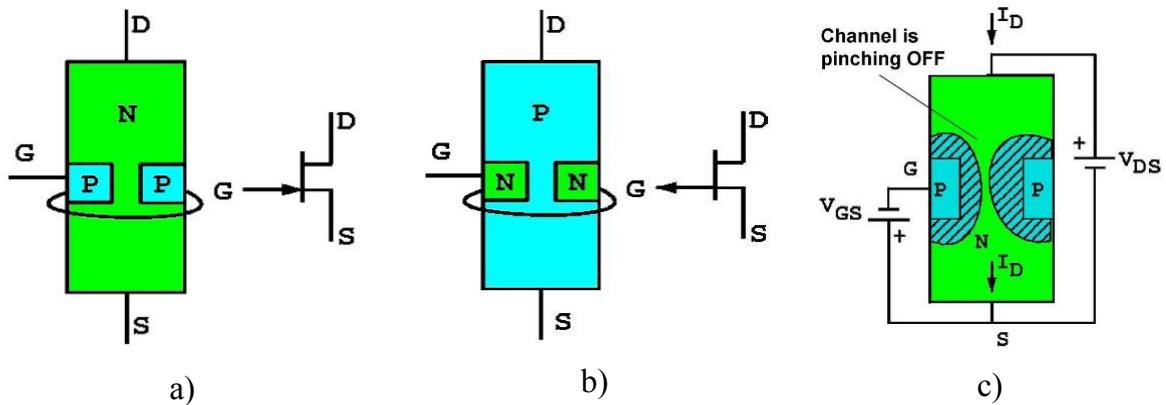


Figure 4-1 a) The N and b) P channel JFET transistors and their operation principle c)

The JFET has two modes of operation: the variable-resistance mode, and the pinch-off mode. In the variable-resistance mode the JFET behaves like a resistor whose value is controlled by its Gate to Source voltage  $V_{GS}$ . In the pinch-off mode, the channel is heavily constricted. The most of drain-source voltage drop is occurring along the high-resistance thin channel near the depletion regions. If  $V_{GS}$  voltage goes from negative to positive the JFET becomes just a forward-biased diode.

#### 4.1.2 Spice modeling of SiC JFETs

Spice models of SiC JFETs, firstly provided by Zappe et. al. in [53] and [54], can predict the JFET well, if model parameters are known. This model is realized for low voltage SiC buried-gate JFETs (SIT structures) and only partially applicable for high voltage vertical JFET devices used in this thesis. Similar buried gate SiC design was tested in [35] by Konstantinov. Allebrand [19], in his thesis has compared the Spice model with Kaminski's

[33] device level simulations and has found a good matching of the model. A vertical JFET, provided by SiCED [14] is also modeled by Griepentrog and Maier [30] and has been used for prediction of electrical and thermal behavior in current limiting applications using saturation property of the 1<sup>st</sup> generation SiC JFETs.

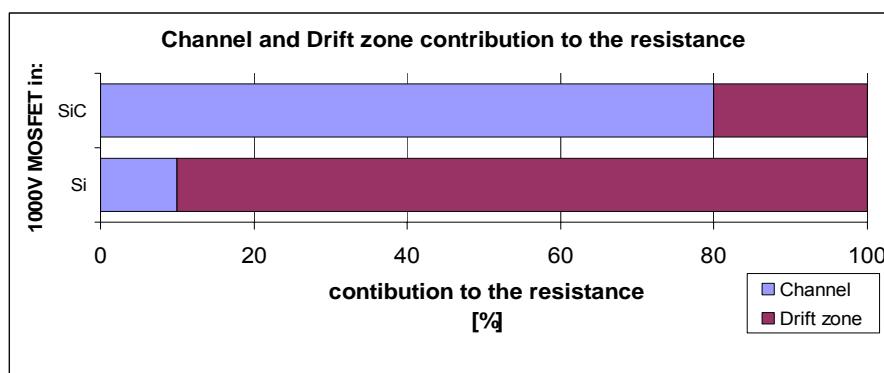
#### **4.1.3 High temperature operation**

Casady et. al [22] characterized a SiC JFET for use in temperature ranges from 293K to 773K. The RF performance of 4H SiC JFET at 500°C is predicted by Hatfeld et. al. in [31]. High temperature operation of SiC JFET for use in inverter phase leg is published by Morell in [41]. McLean et al. have fabricated 6H-SiC buried Gate JFET in epitaxial layer grown on wafers. Functionality has been measured from 218K to 773K.

A thermal cycling study has been provided by Rozario et. al.[43]. They have also implemented and tested SiC buried-gate JFETs in inverters for high temperature and high power applications. Prof. Shenai describes the performance, characterization, modeling and reliability of SiC devices in [97]. The high temperature operation (500hr life at 500°C) of normally OFF vertical trench JFET fabricated in 4H-SiC is presented by Mazolla et. all. in [76].

## 4.2 The SiC VJFET transistor

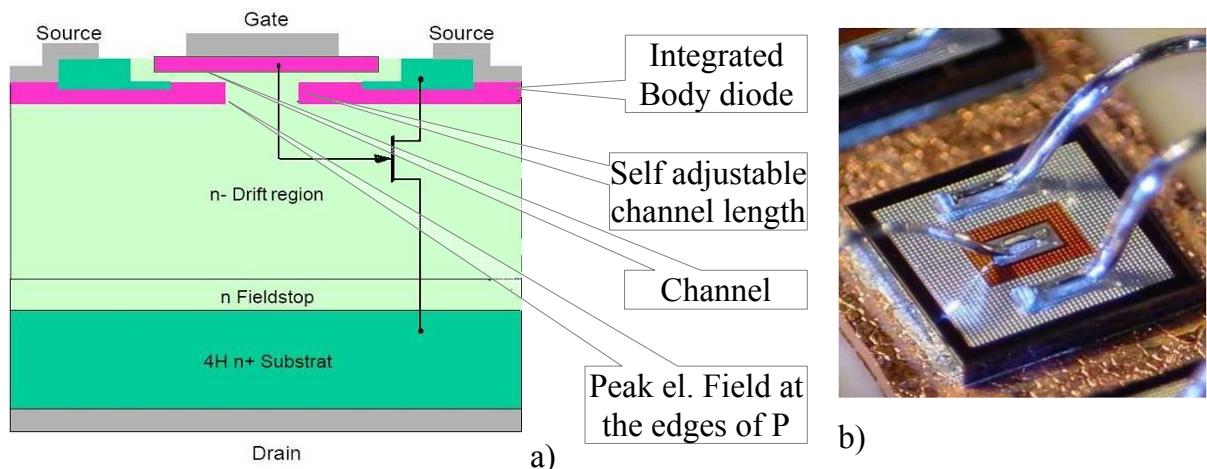
Almost all SiC switching devices described in today's publications use the vertical device structure. The reason is to exploit the drift region which has the main contribution to the ON-state resistance. In the volume a higher electron velocity can be achieved, which is only 20% less than by Si. Under the surface, however, the electron mobility of n-channel MOSFET is drastically reduced, because of rough channel layers and poor thermal oxides, to be grown on p-type SiC which exhibits higher fixed charge and interface state densities.



**Figure 4-2 The contribution to the ON-state resistance of MOS devices in Si and SiC**

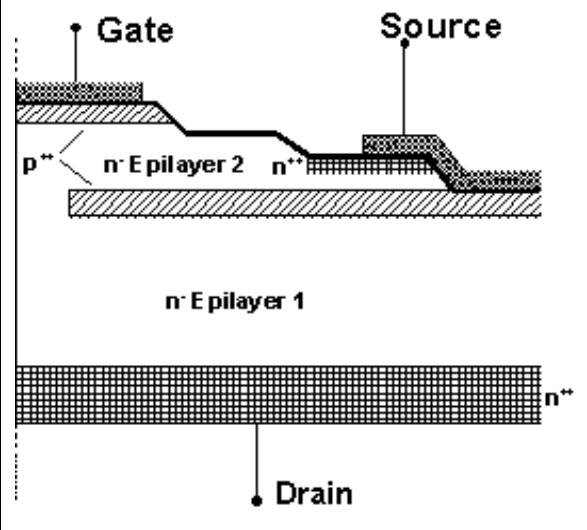
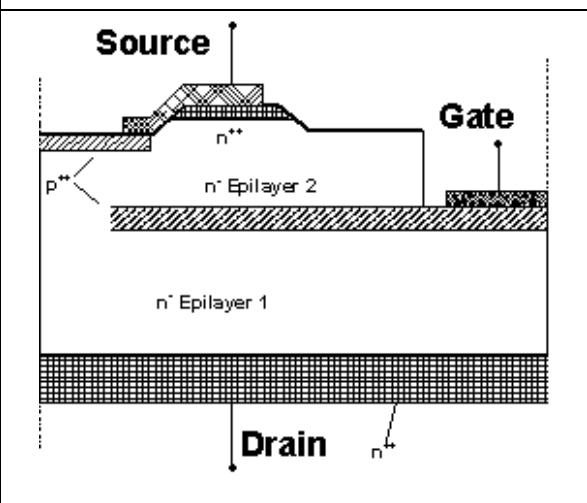
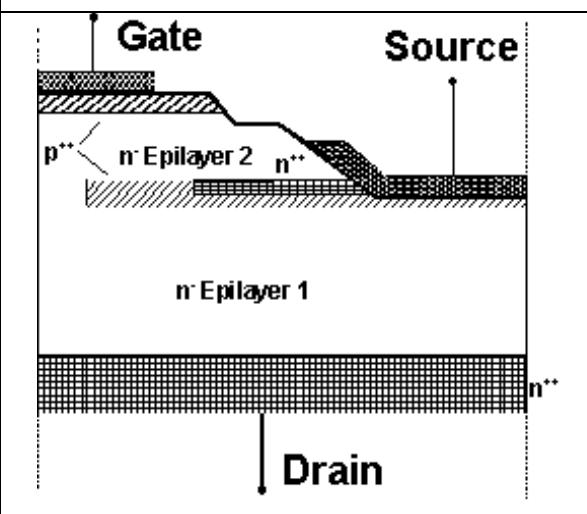
Consequently, the channel of SiC MOSFET's has more influence to the overall resistance than the Si counterpart (Figure 4-2). Therefore regarding ON state resistances and gate oxide stability, the JFET devices with lateral channel in SiC are more favourable.

Basic structure of Vertical Junction Field Effect Transistor (VJFET) is illustrated in Figure 4-3a. The device is controlled with top and buried gates. Picture provided by [14].



**Figure 4-3 a) The Basic structure of the SiC JFET. From bottom to top: Drain metallization, highly doped n+ contact layer, n Fieldstop and n- Drift layers, highly doped p Gates (Red), n Channel, p+ Source contacting layer, top metallization; b) The picture of the JFET [14]**

There were 3 generations of SiC-JFETs from SiCED GmbH, which are studied and implemented in target converter during this thesis work. Their main differences and improvement stages are summarized in Table 4-1. The latest release – 4 generation has an

	<b>1<sup>st</sup> Generation of SiC VJFETs</b> +Fast +Low Miller capacitance +Body-Diode under Source contact - Prechannel - $R_{ON}$ (app. $22\text{m}\Omega\text{cm}^2$ @ 1500V) - Low Source contact area - Low W/L ratio - Low $I_{SAT}$ (app. $200\text{A}/\text{cm}^2$ )
	<b>2<sup>nd</sup> Generation of SiC VJFETs</b> + Low $R_{ON}$ (app. $18\text{m}\Omega\text{cm}^2$ @ 1500V) + High cell density + Large Source contact area + High saturation current ( $\approx 320\text{A}/\text{cm}^2$ ) - Higher internal gate series resistance - Higher Miller capacitance - Body diode through Gate-contact
	<b>3<sup>rd</sup> Generation of SiC VJFETs</b> + Self adjustable channel length + Low internal gate series resistance + Low $R_{ON}$ ( $< 12\text{m}\Omega\text{cm}^2$ @ 1500V) + Low Miller capacitance - Cell density utilisation is not optimal - Smaller Source contacting area

**Table 4-1 The 3 generations of the SiC VJFET transistors and their main properties**

enhanced current capability and due to modified structure (increased N-doping immediately under the buried p-layer) better channel utilization and cell density.

#### 4.2.1 Static characteristics

From the 3<sup>rd</sup> generation JFET structure can be seen, that through the direct Gate connection from the topside of the chip, the big gate resistances can be eliminated.

Such a structure allows obtaining less than  $14\text{m}\Omega\text{cm}^2$  ON-state resistances at 1500V blocking voltage. Figure 4-4 a) illustrates the currently achievable ON-state resistances for different JFETs with  $4,1\text{mm}^2$  active die area.

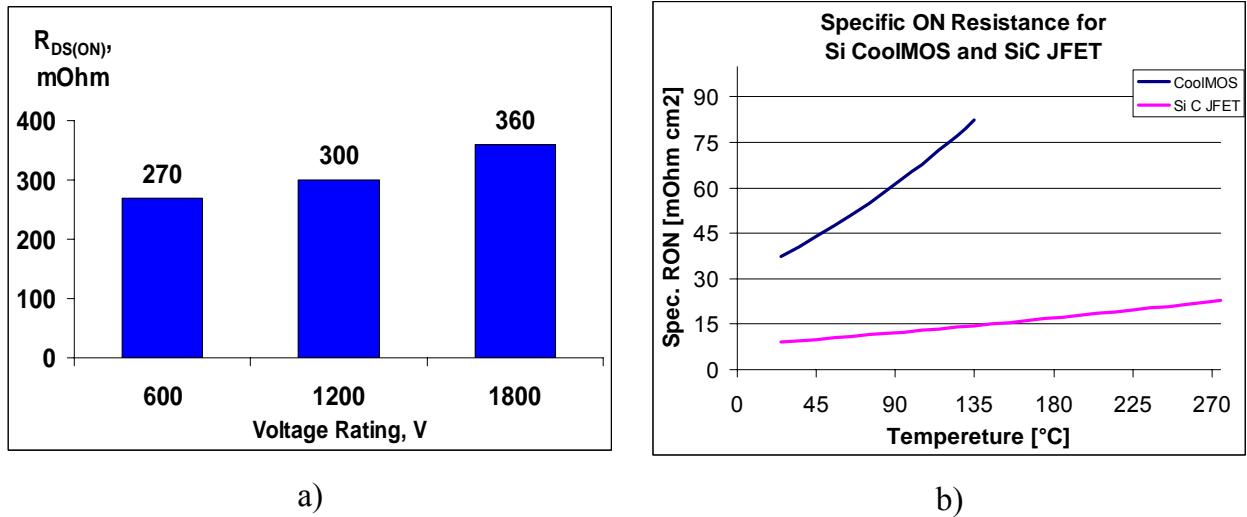


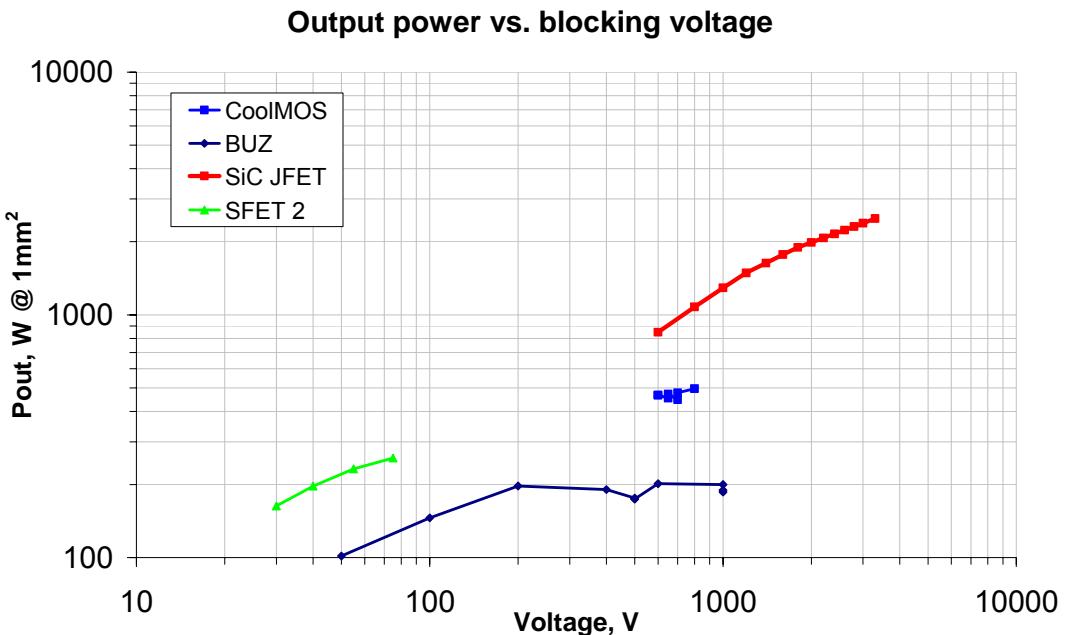
Figure 4-4 a) The ON state resistance of SiC VJFET for different blocking voltages b) specific ON resistance of the SiC JFET and Si CoolMOS vs. Temperature

Analysis of the scattering mechanism in SiC has shown following dependencies between doping density  $\mu$  and temperature coefficient  $\alpha$  [28]:  $\mu \sim T^{-\gamma} \Rightarrow R_{ON} \sim T^\alpha$ ;

Low doping  $\rightarrow \gamma$  very high; high doping  $\rightarrow \gamma$  decreases.

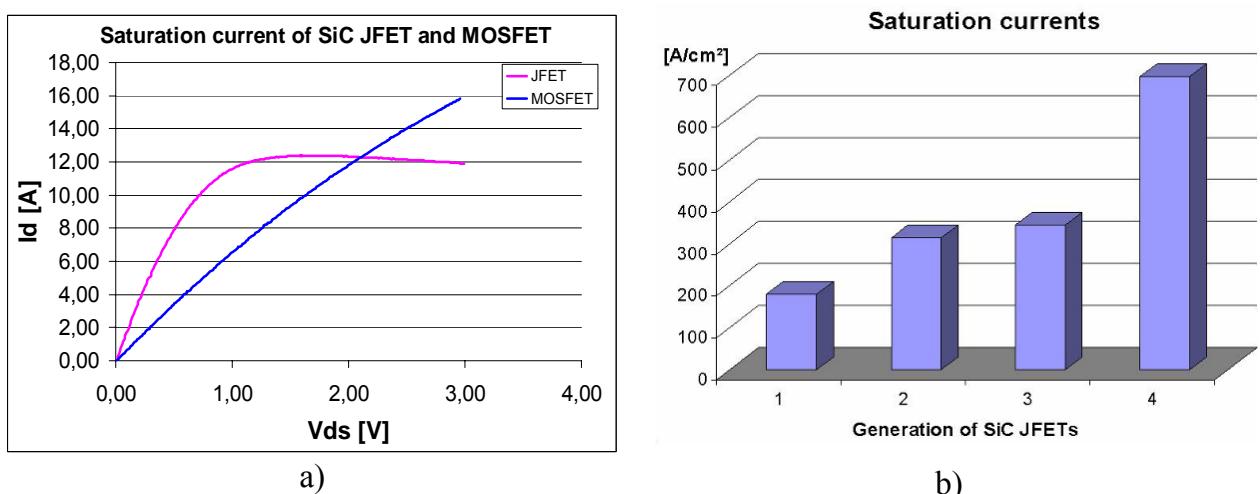
By doping in the channel region as high as possible the temperature dependency of the SiC JFET can be decreased up to  $(T(K)/298)^{1.6}$ , whereas for Si CoolMOS it is equal to  $(T(K)/298)^{2.7}$ . These curves are depicted in Figure 4-4b).

Based on the maximum available voltage and device power capability (e.g. for TO220  $\approx 2\text{W}$ ), it is possible to determine the RMS current through the device and the maximum output power. The output powers versus blocking voltages for CoolMOS (Different technologies 600V - 800V), BUZ (50 - 1000V), SFET (30 - 75V) as well as for SiC JFET are depicted in Figure 4-5. The specific ON resistances are normalised to unity chip area  $\Omega/1\text{mm}^2$ ,



**Figure 4-5 Output power vs. blocking voltage for different power FET technologies**

Interesting to note, that the first generation SiC JFETs have shown specifically low saturation current, which can be seen from Figure 4-6 a), where the measurement results of output characteristics of the JFET are compared with Si MOSFET. This property has been gradually improved in the next generations. The 3<sup>rd</sup> generation JFET has doubled it reaching almost 350A/cm<sup>2</sup>. The fourth generation shows excellent saturation current capability – 700 A/cm<sup>2</sup> Figure 4-6 b)



**Figure 4-6 The output characteristics of the Si MOSFET and SiC JFET. a) The first generation SiC JFET is showing relatively low saturation current. b) 4<sup>th</sup> generation has reached 700A/cm<sup>2</sup>**

## 4.2.2 Dynamic characteristics

### Reverse recovery characteristics of the SiC JFET in phase leg configuration

Although the switching speed of the SiC JFET is very high, in the phase leg operation the switching properties of its body diode are decisive. From the SiC JFET structure can be seen, that its body diode is a PN junction implemented under the source region. For characterization of the device a setup shown in Figure 4-7 a), b) has been built up.

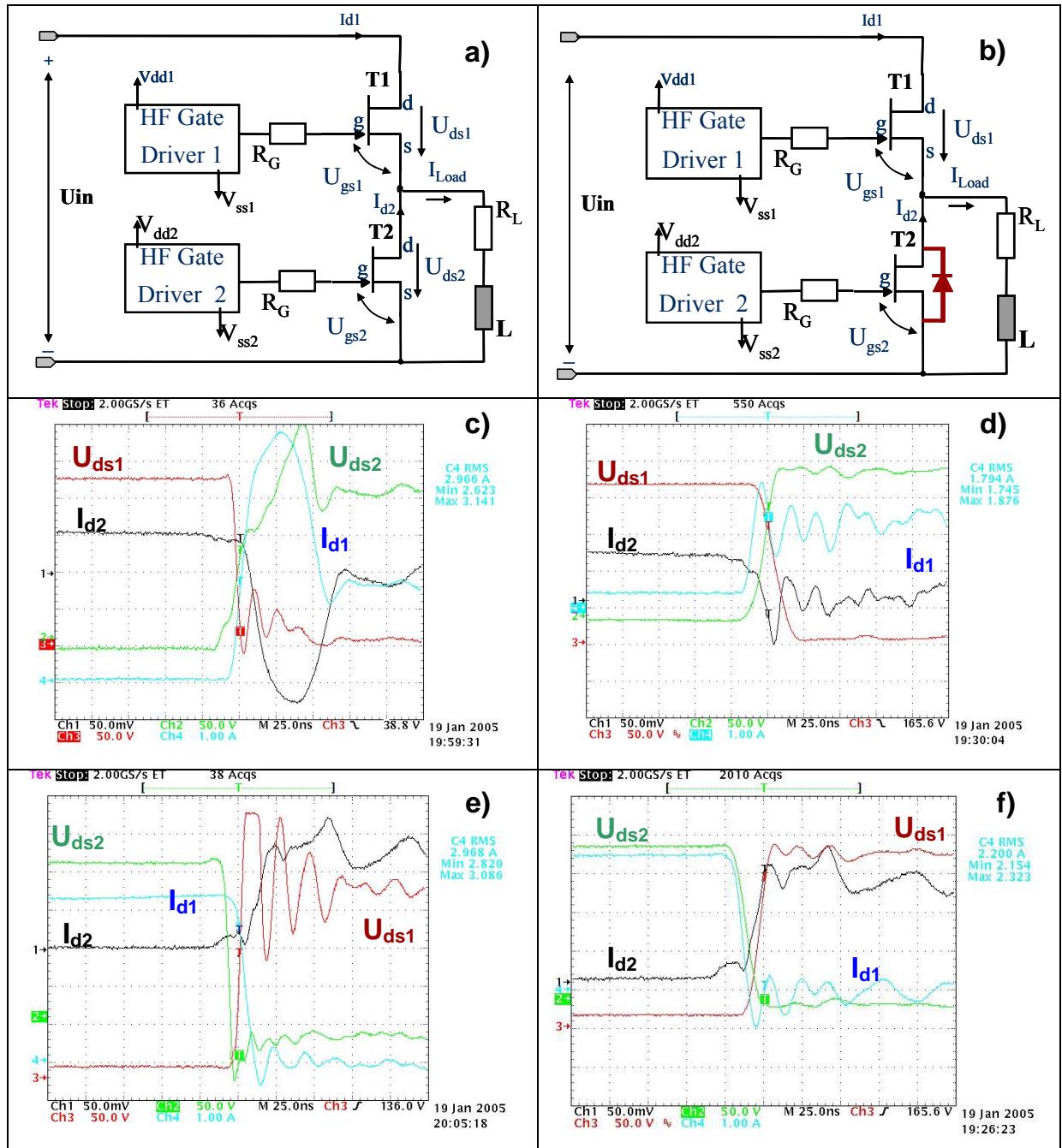


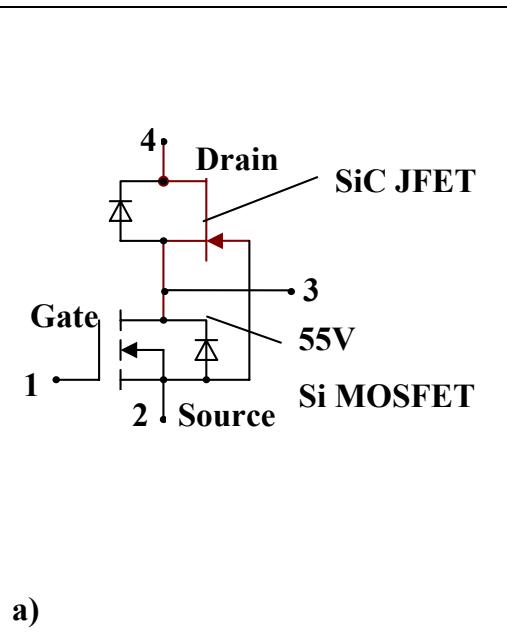
Figure 4-7 Phase leg setup with SiC JFETs only a),c),e) and with external SiC reverse diode b),d),f). Switching ON c),d) and switching OFF e),f) waveforms of the SiC JFET in phase leg.

Two cases were examined: The phase leg with external SiC reverse diode and without it, where the internal body diode is used for freewheeling. Important to note, that the switching characteristics of the body diode of SiC VJFET is comparable to ordinary Si diode. This is visible from the comparison of the switching ON transients given in Figure 4-7 c) and d). The drain current  $I_{d2}$  of the  $T_2$  has comparably large negative “reverse recovery” slope. Consequently if very fast switching is necessary an additional SiC diode should be connected in parallel to the SiC VJFET drain-source Figure 4-7 b.

#### 4.2.3 Normally ON problem and JFET-MOSFET Cascode circuit

A big advantage of the MOSFET devices against JFETs is that they are normally-OFF, whereas the JFETs are normally on devices. This means, that the JFET conducts if no voltage is applied to the gate. This is a drawback in many applications, where the suddenly loose of control can cause conduction of the switches and consequently can lead to short circuit. Also during system start-up, when the control circuitry has not yet fully powered, a high shoot-trough or transient currents can take place. Because of the normally-ON problem the Si power JFET are considered in many power electronics applications as an undesirable device. As it was shown in Chapter 4.1.1 in order to switch the JFET device OFF, a negative voltage applied to the gate of JFET will be needed. This voltage, called “pinch-off voltage” must be enough high in order to switch the JFET OFF, but also has to be limited in order to prevent the reverse biased junction of the Gate-Source diode from secondary breakdown. Due to different designs of currently available JFET devices the pinch-off voltage varies from -20V to -40V. Today it is important to design the right gate drive and precisely adjust the output negative voltage level. However, as the manufacturing technology of the SiC JFETs advances, the tight justification of the pinch-OFF voltages will be possible already in production, therefore this is not regarded as a drawback.

In fact, the problem is not the negative voltage necessary to drive the JFET, nor its relative high level, but merely the conducting of the JFET when the gate voltage is zero. One possibility to “make” the JFET normally OFF device is the “cascode” circuit or “Baliga Pair”. The “Baliga Pair” consist of low voltage normally OFF device, e.g. a low voltage high current MOSFET, connected in series with the high voltage JFET Figure 4-8. Controlling of the JFET is taking place using the MOSFET. When the MOSFET is switched OFF the voltage over its Drain-Source rises and applies as negative bias to the gate of the JFET. Now the JFET also switches OFF and blocks whole applied voltage.

 <b>a)</b>	 <b>b)</b>	<table border="1"> <tbody> <tr> <td><math>I_D</math></td><td>5</td><td>A</td></tr> <tr> <td><math>I_D(10\mu s)</math></td><td>8</td><td>A</td></tr> <tr> <td><math>E_{ON}</math></td><td>18</td><td><math>\mu J^{**}</math></td></tr> <tr> <td><math>E_{OFF}</math></td><td>32</td><td><math>\mu J^{**}</math></td></tr> <tr> <td><math>V_{GS(max)}</math></td><td><math>\pm 20</math></td><td>V*</td></tr> <tr> <td><math>V_{GS}</math> (threshold)</td><td>2.1 - 4</td><td>V*</td></tr> <tr> <td><math>I_{GSS}</math></td><td>&lt; 100</td><td>nA*</td></tr> <tr> <td><math>P_{tot}</math></td><td>40</td><td>W</td></tr> <tr> <td><math>T_{Op}</math></td><td>-25 .. +150</td><td>°C</td></tr> <tr> <td><math>R_{thjc}</math></td><td>3</td><td>K/W</td></tr> <tr> <td><math>V_{Bdss}</math></td><td>1.5..1.8</td><td>kV</td></tr> <tr> <td><math>I_{dss}(25^\circ C \text{ &amp; } 125^\circ C)</math></td><td>&lt;100</td><td><math>\mu A</math></td></tr> <tr> <td><math>I_{gss}</math></td><td>&lt;100</td><td>nA</td></tr> <tr> <td><math>R_{ds(on)}</math></td><td>0.5..0.8</td><td>Ohm</td></tr> <tr> <td><math>C_{ISS}</math></td><td>540</td><td>pF*</td></tr> <tr> <td><math>C_{OSS}</math></td><td>140</td><td>pF*</td></tr> <tr> <td><math>C_{RSS}</math></td><td>30</td><td>pF*</td></tr> </tbody> </table>	$I_D$	5	A	$I_D(10\mu s)$	8	A	$E_{ON}$	18	$\mu J^{**}$	$E_{OFF}$	32	$\mu J^{**}$	$V_{GS(max)}$	$\pm 20$	V*	$V_{GS}$ (threshold)	2.1 - 4	V*	$I_{GSS}$	< 100	nA*	$P_{tot}$	40	W	$T_{Op}$	-25 .. +150	°C	$R_{thjc}$	3	K/W	$V_{Bdss}$	1.5..1.8	kV	$I_{dss}(25^\circ C \text{ & } 125^\circ C)$	<100	$\mu A$	$I_{gss}$	<100	nA	$R_{ds(on)}$	0.5..0.8	Ohm	$C_{ISS}$	540	pF*	$C_{OSS}$	140	pF*	$C_{RSS}$	30	pF*
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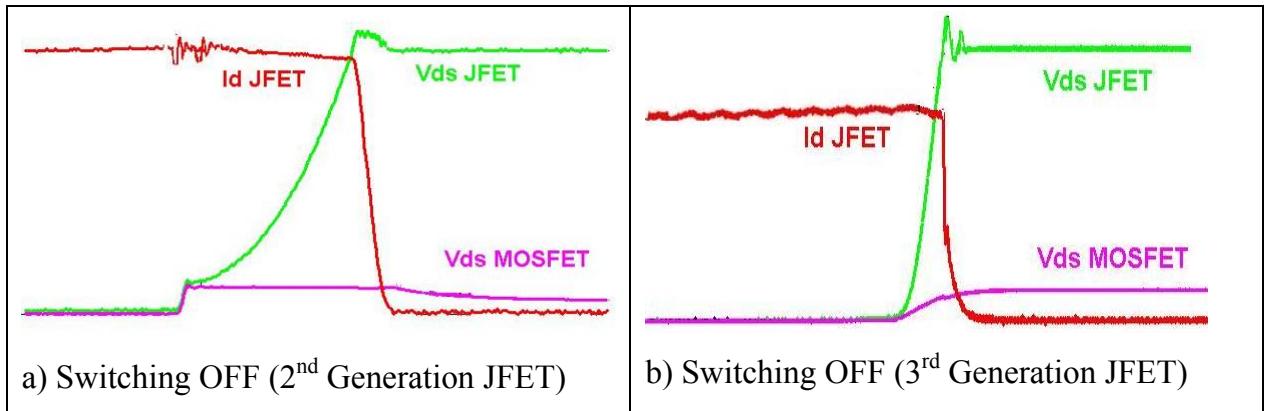
**Figure 4-8 a) SiC JFET in Cascode circuit, b) different high voltage and high temperature packaging approaches and c) Main characteristics. \*Values are defined by the LV MOSFET**

Although the MOSFET is always on the current path, its contribution to the actual ON-resistance is negligible. The 30V MOSFETs have usually 1.2-3.0mΩ Drain to Source resistance.

#### Dynamic behavior of the SiC VJFET in Cascode circuit

Like any conventional JFET, the SiC JFET switches are very similar to the MOSFETs as far as their switching characteristics are concerned. In general, all theoretical calculations done for MOSFET can be applied for JFETs too. Even though these similarities, dynamic behaviour in the Cascode circuit is somewhat more complicated than an ordinary MOSFET. For dynamic characterisation a test setup similar to the circuit illustrated in Figure 6-1 has been built up, where instead of JFET the Cascode device is installed. From the turn-OFF waveform of the Cascode circuit (Figure 4-9a) one major drawback in the dynamic behaviour can be observed. As soon as the drain voltage of the MOSFET rises, the drain voltage of the JFET rises as well. If the switching speed of the JFET is limited (this was inherently the case in 2<sup>nd</sup> generation devices) it takes rather long time until the applied voltage can be fully blocked by the JFET. During this time interval, the MOSFET must operate in avalanche mode, because being turned OFF, its drain voltage is at the maximum value and the current still must flow through its channel. For repetitive operation, this could damage the MOSFET. Also without any gate resistor in the JFET's gate path, the device showed an internal gate resistance, consisting of ohmic contact of the

gate electrode and the p-layer resistance of the gate region. In the next generation the switching speed was greatly improved, which can be seen from Figure 4-9b).

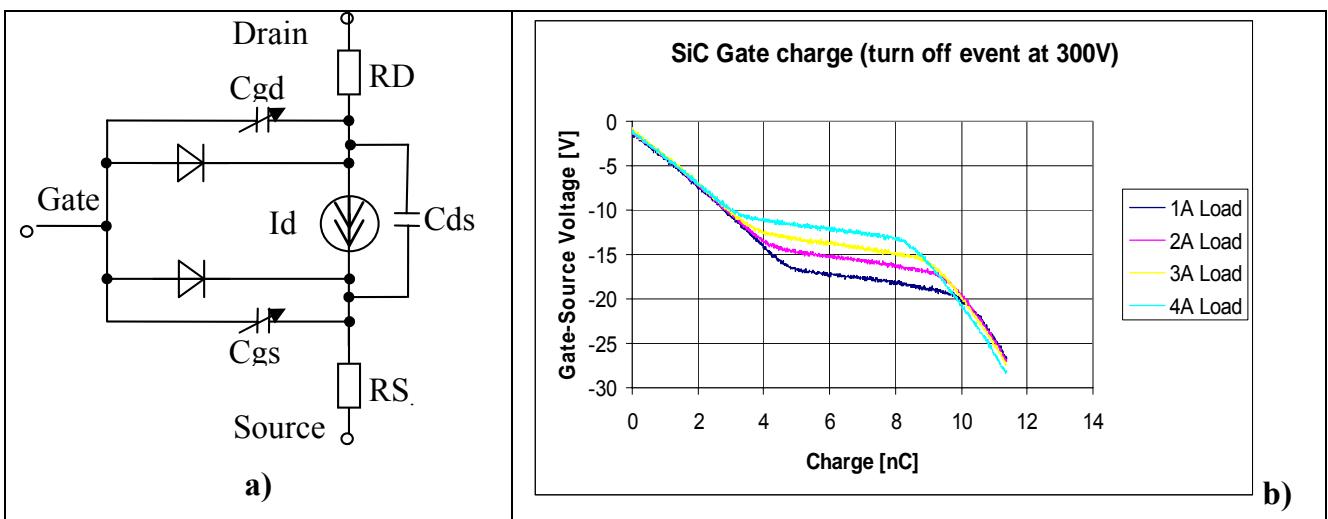


**Figure 4-9 Switching waveforms of the SiC JFET – Si MOSFET in Cascode configuration [71]**

The whole process is much quicker and finished in about 30ns. The MOSFET is never driven into avalanche, since its drain voltage is rising to the static value after the switching process of the SiC VJFET. If nevertheless the switching speed of the VJFET must be limited, than the Cascode configuration should be modified to be controllable from the VJFET gate directly, yet retain the normally OFF condition. This will be described in details later in Chapter 6, where the JFET alternative driving methods will be presented.

### 4.3 SiC VJFET model

For simulation of the power converter circuit the Saber™ metaphysics simulation software is used [112]. This software is provided with optional component library and templates, with predefined models of different components. The JFET model structure from the Saber™ library is shown in Figure 4-10 a).



**Figure 4-10 a) The SiC VJFET model equivalent circuit and b) its Gate charge characteristics**

The VJFET model was characterized based on the Berkeley JFET model incorporated into the generic JFET template and includes following required and optional parameters:

$\beta$ Beta transconductance coefficient	$V_{GS}$ gate-source voltage
$\lambda$ Lambda channel length modulation	$V_{GD}$ gate-drain voltage
$r_d, r_s$ drain and source resistances	$v_{ds}$ drain-source voltage
$r_{gs}, r_{gd}$ gate-source and gate-drain resistances	$I_{drain}$ drain current
$r_{ds}$ drain-source resistance	$I_{gate}$ gate current
$c_{gs}$ gate-source capacitance at zero bias	$I_{srce}$ source current
$c_{gd}$ gate-drain capacitance at zero bias	$V_{GF}$ Gate forward p-n potential
$v_{po}$ pinch OFF voltage	$M$ Gate p-n grading potential
	$K_{CF}$ Forward bias capacitance coefficient

Unfortunately not all parameters can be immediately found. Even for engineering samples, there was no any datasheet provided by the device supplier. Some necessary parameters are taken from PhD-Thesis of Nando Kaminski [33] and his semiconductor simulations. Very few parameters were obtainable from conference proceeding – whereas most of the data usually concerning different type of JFETs. Yet different generations of the same device have rather different parameters like: maximum saturation currents, pinch-off threshold voltage, punch-through and breakdown voltage levels etc.

Therefore, majority of the parameters had been extracted from experimental measurements. Firstly the static parameters are obtained; afterwards the gate charge and capacitances were extracted from measurements Figure 4-10b) [68]. These are voltage dependent and can be described by the following equations:

$$C_{GS} = cgs \left( 1 - \frac{V_{GS}}{V_{GF}} \right)^{-M} \quad \left| \begin{array}{l} \text{if } V_{GS} \leq K_{CF} \cdot V_{GF} \\ \text{if } V_{GS} > K_{CF} \cdot V_{GF} \end{array} \right. \quad 4-1$$

$$C_{GS} = cgs (1 - K_{CF})^{-(1+M)} \cdot \left[ 1 - K_{CF} \cdot (1 + M) + M \cdot \frac{V_{GS}}{V_{GF}} \right]$$

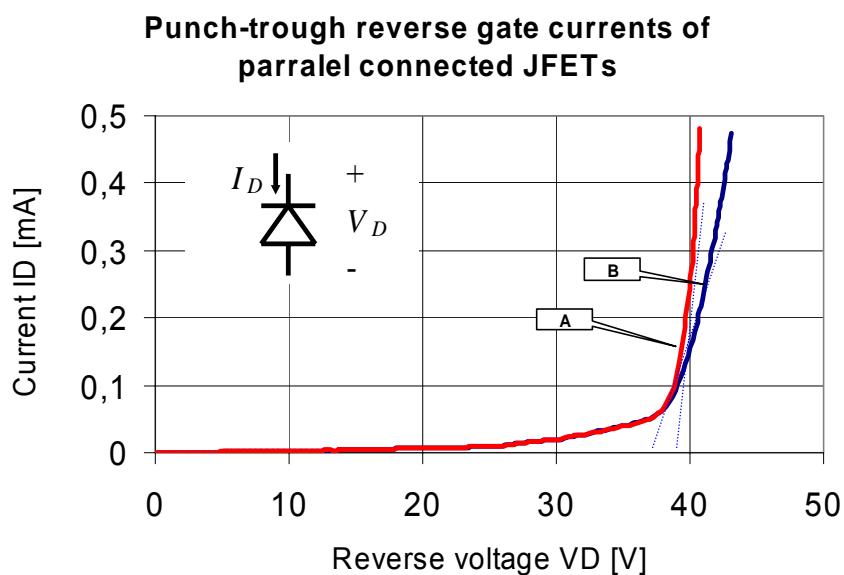
$$C_{GD} = cgd \left( 1 - \frac{V_{GD}}{V_{GF}} \right)^{-M} \quad \left| \begin{array}{l} \text{if } V_{GD} \leq K_{CF} \cdot V_{GF} \\ \text{if } V_{GD} > K_{CF} \cdot V_{GF} \end{array} \right. \quad 4-2$$

$$C_{GD} = cgd (1 - K_{CF})^{-(1+M)} \cdot \left[ 1 - K_{CF} \cdot (1 + M) + M \cdot \frac{V_{GD}}{V_{GF}} \right]$$

The pinch-OFF voltage  $V_{PO}$  is between -20 and -40V and varies from sample to sample. A mean value -30V is chosen. The channel length modulation Lambda is equal  $10^{-6}$  [19]

#### 4.4 Paralleling of the VJFET transistors

Because of positive temperature coefficient of the channel resistibility, the SiC VJFET can be paralleled as any other Si MOSFET transistor. For driving the parallel connected JFET however, more detailed investigations should be performed. As it was shown previously, the gate of the JFET transistor appears to be a pn-junction and in OFF state can be regarded as a reverse biased diode. During reverse biasing, the depletion layer of this diode grows and at breakdown voltage it can reach through or “punch-through” the short and lightly doped drift region. When this occurs (like in commonly termed punch-through diodes) further increase of reverse voltage will not cause the depletion region to widen any further and the field profile begins to flatten out. From the “outside” this can be noticed by significant increase of gate reverse current Figure 4-11.



**Figure 4-11 Reverse biased gate leakage and punch-trough currents of two JFET samples**

Figure 4-11 also shows that different samples of JFET's can have different punch-trough currents at the same reverse voltage level (curves A and B). This aspect sets a boundary over the current and voltage requirements of the parallel connected gates. The maximum allowable gate currents should be taken in account for designing the SiC JFET gate driver circuits.

## 5 Application and impact of the SiC devices on the power converters

In Chapter 2.2.2 an overview of the common converter topologies is presented and main properties are summarized in Table 2-4. This chapter will point out in which converter topologies the specific properties of SiC devices are essential for their efficient operation or, in other words, how the SiC devices can be optimally implemented in power converters.

### 5.1 Simplification of the topologies using SiC devices

From the wide choice of power converter topologies, with their particular advantages and disadvantages, making them suitable for certain power supply application, we can select two major groups: Single-ended and Double-ended (see Figure 2-6). The double ended, multi switch topologies like: symmetrical and asymmetrical half bridges, push-pull and phase shifted full bridge converters are commonly used in high power applications. However, the topology complexities of these converters are also significantly higher; see

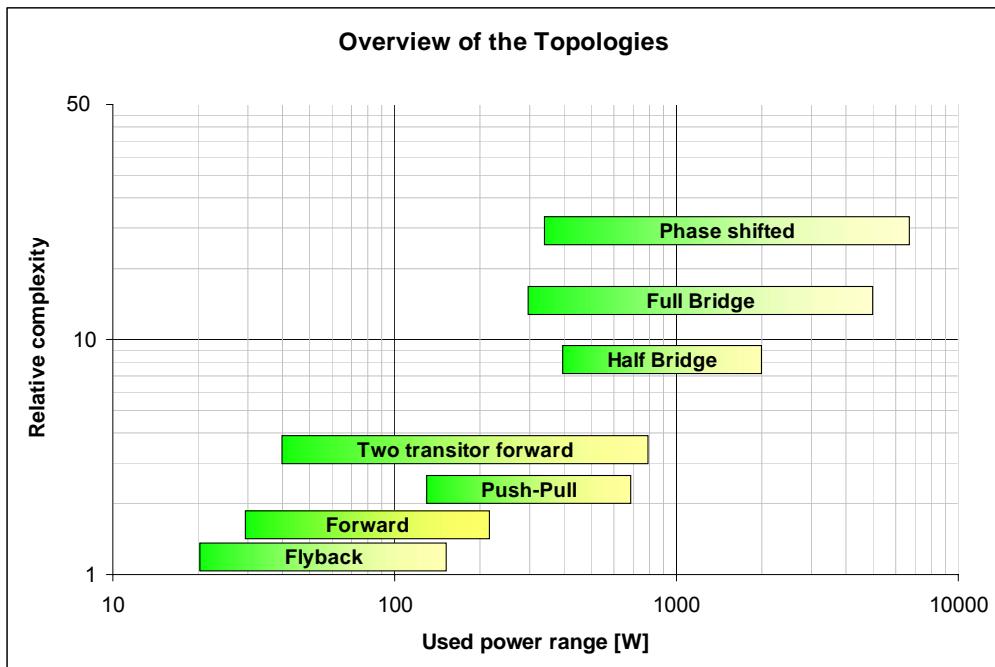


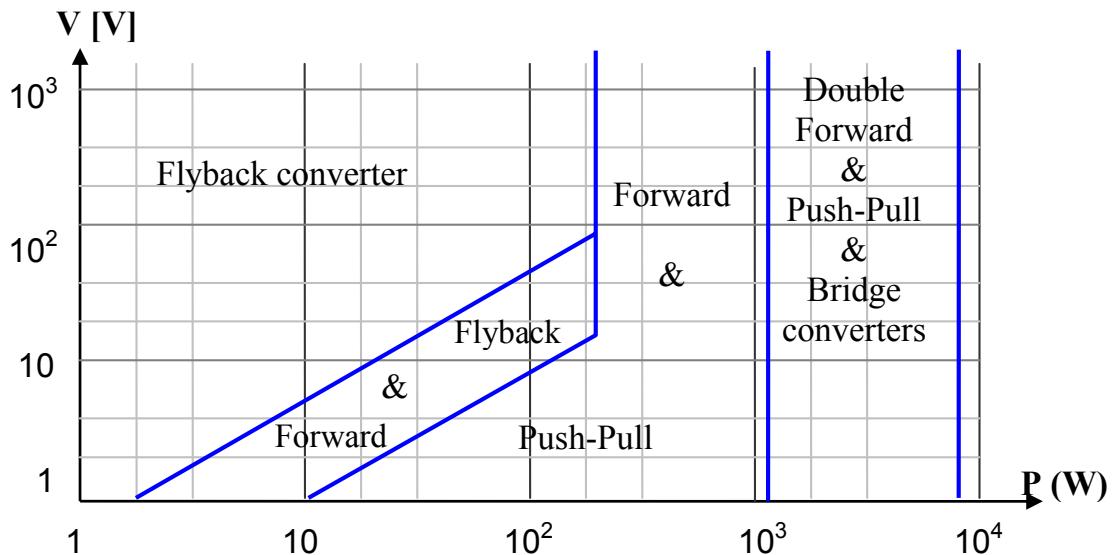
Figure 5-1 Commonly used topologies for different power levels & their complexity

Figure 5-1. They use 2 or 4 switches with issues to manage the reverse recovery of the body diodes, to prevent shoot through conditions, to maintain appropriate dead times

between switching the high side and low side switches. They usually incorporate external isolated high side gate drive circuits and have to deal with transformer core inherent flux imbalance.

Single-ended topologies like the Forward, Flyback, Double Switch Forward, SEPIC, etc. are often chosen for implementing simple, low cost and up to nowadays for low power converters. The use of only one active switch and the simple control circuit required are strong reasons for this choice. As we can see from Figure 5-2, for output voltages from few volts up to 1kV, and for output power up to 1kW, the single-ended topologies like forward converters are more preferable than double ended ones [100].

Topology overview (Chapter 2.2.2) shows that the main advantage of the multi-transistor topologies is the switch power stress, particularly the voltage stress, which, in half and full bridge topologies (e.g. for telecom applications) are about 600V-800V [55]. Considering the requirements given in Chapter 1.2 and targets discussed in Chapters 2 and 3, it can be easily concluded that the converter topology should be the simplest with minimal number of power switches. The single switch single-ended converters can meet these criteria.



**Figure 5-2 Output power and voltage ranges for different converter topologies. The forward converter can be applied for up to 1kW output power [100]**

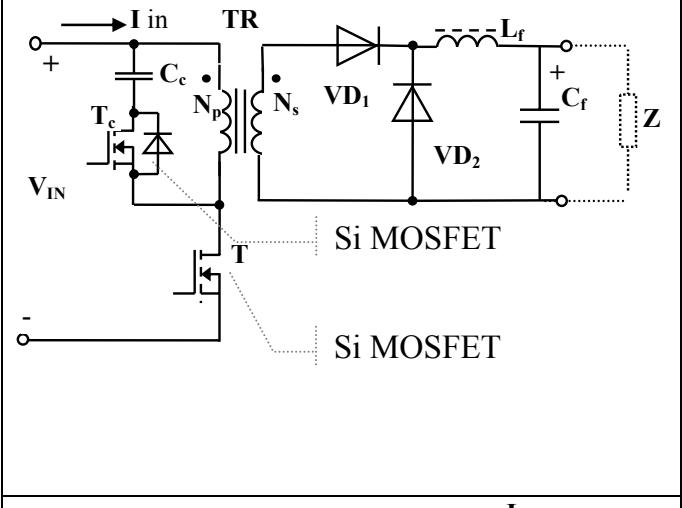
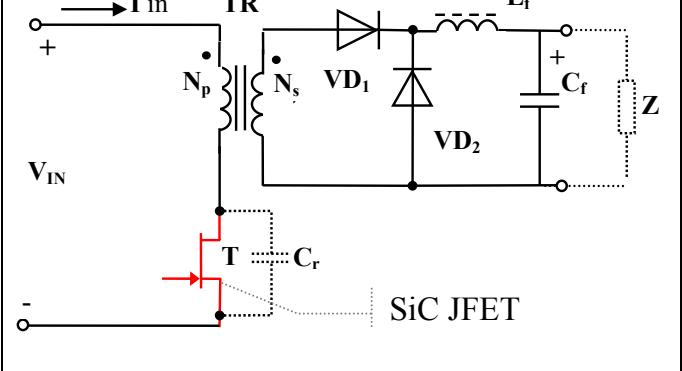
### 5.1.1 Choosing resonant reset forward converter

Generally increased switching frequencies in converters are possible, when quasi-resonant (e.g. ZVS) operation is realised, which greatly reduces the energy losses caused by discharging the capacitances [104]. Incorporating the ZVS function into Flyback converter operating in continues current mode is difficult, if not impossible. The Forward converter, in contrast, is better suited for ZVS, because the primary winding of the transformer during switch-OFF time is available as inductor of the resonant circuit. Additionally the transformer transfers the energy without storing it. Therefore higher power density and higher efficiency can be achieved with forward topologies.

Consequently in later discussions we will concentrate on Forward type single switch converter topologies only. One disadvantage of single-switch converters, especially of resonant reset forward converter against multi-switch topologies, is that the leakage inductance energy can, if not managed correctly, lead to voltage overshoot on the primary switching device.

Table 5-1 shows different possibilities for transformer core reset in forward converter topologies. It is obvious, that SiC power switch allows extremely simplifying the reset mechanism of the converter, by reducing needed external reset component count up to one reset capacitor. At higher frequencies 400kHz - 600kHz, even this capacitor can be eliminated, by substituting it with parasitic output capacitance of the JFET and/or by transformer internal windings capacitances.

Moreover, for comparable power handling and cost effective realisation of the single switch converter, its power switch should be able to withstander 2-3 fold input voltages and provide extremely low ON-state resistance. The ON-Sate resistance needed for possible replacement of the CoolMOS transistors in Bridge topologies by the single-transistor one in applications from 700W to 1000W is presented by T. Reinmann [91]. From Reinmann's calculations can be seen, that having a power SiC transistor with voltage ratings (1.5 -1.8kV) and with drain currents about 5A, together with given  $R_{DS\text{-ON}}$  resistance, the replacement of the multi-switch topologies in mentioned power range is theoretically possible already with today's SiC semiconductor technology. The possible application for replacement of the multi-switch topologies by the single-switch one is also presented in [78], [79], [82].

	<b>The Forward converter with active clamp reset</b> + Simple transformer + Limited voltage on the switches - Additional high-side reset switch - Additional high-side driver . Clamping capacitor - Complex control
	<b>The Forward converter with resonant reset</b> + Simple transformer + No need of external reset components + Simplest control - High voltage stress of the switch

**Table 5-1 Different possibilities for transformer reset in Forward converter:- the resonant reset is the simplest topology but needs very high voltage power transistor like SiC JFET**

From general SiC device overview (Chapter 2.1) and from SiC JFET specific properties (Chapter 4) we can see, that among other parameters, the SiC power devices have inherently higher temperature and power stress capability than Si counterparts, therefore it is expected to have much higher reliability of the system<sup>5</sup>. With less active elements in the design, the breakdown probability of the system is minimised.

<sup>5</sup> It is assumed that a SiC power device has at least the same quality and reliability level as the Si counterpart

## Simplification

Table 5-2 shows the parametric comparison of some forward topologies, where the switch voltage stresses include the effect of leakage inductances. We can see that having the highest voltage stress on the power switch, the Resonant Reset is the simplest forward topology.

<b>Forward Topologies</b>	<b>Efficiency</b>	<b>Voltage Stress</b>	<b>Sm.-Signal Dynamics</b>	<b>Noise EMI</b>	<b>Additional Parts Count</b>
Conventional, with. reset winding	Low	$2V_{inmax} + V_{leak}$	Buck-Like	High	3-Winding Transformer, Diode
Forward with RCD snubber	Low	$\sim 2 V_{inmax}$	Buck-Like	High	Dissipative resistor, C, D
Forward with LCDD snubber	Low	$\sim 2V_{inmax}$	Buck-Like	High	L,C,D,D
Forward with resonant reset	Medium	$2V_{inmax} + V_{rst} + V_{leak}$	Buck-Like	Low	Without any reset circuit
Forward with two switches	Medium	$\sim 1,0V_{inmax}$	Buck-Like	Medium	2 Large FET, HS gate drive, D,D
Forward with active clamp	Medium	$\sim 1,3V_{inmax}$	Buck-Like + additional dynamics	Low	Small FET&C, HS gate drive complex. cntrl
Double Forward	High	$\sim 1.3V_{inmax}$	Buck-Like add. dynamics	Low	Small FET, C,D 2 saturable reactors

Notes: D- Diode for clamp, demagnetization or snubber circuit, L – inductor, C - capacitor

**Table 5-2 Properties of different forward topologies included influence of parasitics, the resonant reset converter having highest voltage stress on the switch, is the simplest topology**

The simplification can be explained as following:

1. Because of single switch design, the topology needs only one low-side gate driver IC.
2. Having very small gate charge, the control and driving circuitry for SiC JFET can be also simpler.
3. Transformer core reset is accomplished in natural way, without any additional clamp circuitry or demagnetisation winding.

## Efficiency increase

Efficiency increase in resonant reset forward converter compared to the common topologies is obtained using several ways:

1. Reduction of the number of active component and elimination of the dissipative snubbers will lead obviously to reduced active loses compared to the multi-switch converters.
2. Increase of duty cycle limit will result to lower RMS current, hence to conduction loss reduction in the power switch. This can be seen from the calculations given in Chapter 2.3.1 with (2-6) and Table 2-4 respectively
3. Replacing dissipative transformer core reset circuitry with recuperative, resonant reset circuit will save the energy and can lead to efficiency increase
4. Practically, the frequency in single switch converters, compared to the half- or full-bridge converters can be increased, because of absence of dead time  $T_{dead}$  between switching the high and low side switches (Table 2-5). By utilising the high switching speed of the transistor and zero reverse recovery of the secondary side diodes, the switching losses will be minimised. Due to higher duty cycle and switching frequency, the smaller inductive filter will have also lower copper resistance. This will reduce the ohmic losses in the high current carrying inductor (2.3.2).

## Switch utilization factor and semiconductor cost in the resonant reset converter

Often the largest single cost in a converter is the cost of the active devices. Therefore it is useful to compare the candidate topologies for SiC application against the total active switch stress and active switch utilization. Every converter topology has an ultimate and physically limited power switch utilisation factor  $U$ .[55], which is defined as  $U = P_{Load} / S_{Total}$ , where  $S$  is the switch stress. At low duty cycle the transistor current stress becomes large; if the duty cycle is exceeding 0.5, then the transistor peak voltage is large. So the optimal selection of duty cycle is important in order to have minimal current-voltage product (see Figure 7-1). Incorporation of isolated transformer additionally reduces the switch utilisation. In general, the buck-derived converters should have as large duty cycle as possible. Even so, the switch utilisation factor is reduced showing that the switch peak voltage is increasing by factor 2.8. In contrast to conventional forward topology, in resonant reset converter the duty cycle is not limited to 0.5, therefore its switch utilisation factor can theoretically reach 0.32, see Table 5-3. The actual duty cycle limit depends on

the maximal allowable drain voltage on the switch. In practice, however, the maximum switch utilisation in phase leg of bridge converter is limited by its duty cycle -  $D = 0.45$  for each transistor. In resonant reset converter the maximum duty cycle is 0.65-0.7, whereas the switch voltage is 3 times higher.

Topology	$U(D)$	$U(D)_{MAX}$	max $U(D)$ at $D =$
Buck	$\sqrt{D}$	1	1
Boost	$\frac{(1-D)}{\sqrt{D}}$	$\infty$	0
Flyback	$(1-D) \cdot \sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward $n_1=n_2$	$\frac{1}{2} \cdot \sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Full Bridge (buck derived)	$\frac{\sqrt{D}}{2 \cdot \sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Resonant Reset Forward	$\frac{1}{3} \sqrt{D}$	$\frac{1}{3} = 0.333$	1

**Table 5-3 Active switch utilization of some common DC/DC converter**

The semiconductor cost in a given converter can be estimated using the switch utilisation:

$$\left( C_{semi} \left[ \frac{\$}{kW} \right] \right) = \left( \frac{C_{device} \left[ \frac{\$}{kVA} \right]}{V_{rate} I_{rate} U(D)} \right), \text{ where} \quad (5-1)$$

$C_{semi}$  - Is the semiconductor cost per kW output power

$P_{out}$  - Output power;  $C_{device}$  - Semiconductor device cost per rated kVA

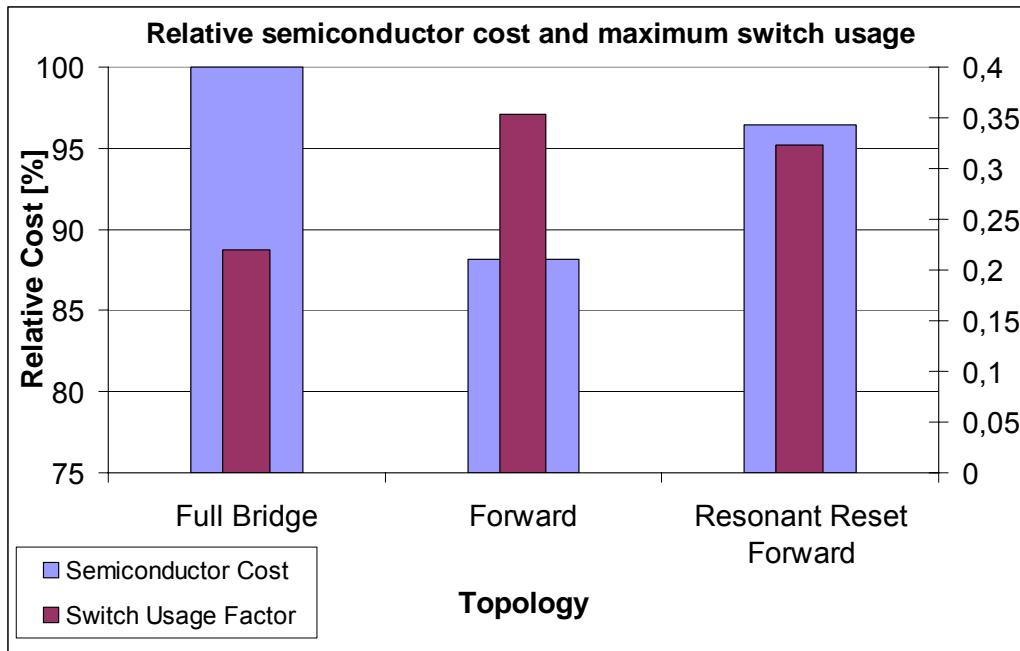
$V_{rate}$  - Voltage derating factor;  $I_{rate}$  - Current derating factor

$U(D)$  - Converter switch utilization

Figure 5-3 shows the relative overall power switch costs in different topologies. Here, the bridge converter with Si CoolMOS switches is compared with two single switch topologies with SiC. We can see, that the overall system cost of resonant reset converter with 4,3 € SiC Transistor<sup>6</sup> can be lower than a bridge with € 0,64 CoolMOS. The overall semiconductor cost is normalised to Si CoolMOS transistor.

<sup>6</sup> The estimated price of the SiC JFET Cascode (to be available by 2007-2008)

Overcoming 0.5% duty cycle limit will reduce the conduction loss of the primary side and will lower the voltage stress in secondary side. This in turn with high input voltages will lead to very high reset voltage stress on the drain of the switch. With the currently available SiC power JFET, it is possible to withstand voltages up to 1800V! Influence of the parasitic, voltage dependant capacitance can be minimized, with additional external capacitor connected in parallel to the drain-source of the transistor.



**Figure 5-3 Relative semiconductor cost and maximum switch utilization in different converter topologies.**

High switching frequency of the JFET allows minimizing the transformer size and necessary value of the reset capacitance. In this case, the windings capacitances of the transformer can be used for core reset purpose. The control of the JFET remains simple, because of very low gate charge.

It is important to notice, that at higher frequencies the copper resistances of the transformer and filter inductor windings will be minimised. However, active losses will not have a significant impact on the overall efficiency, but the switching and high frequency losses. In addition some fundamental limits start to show up, at higher operation frequency, when parasitic inductances on source path and in the switch commutation loop reduce the switching speed and increase the switching losses. The parasitic capacitances cause more switching ON losses. Therefore, in order to gain from frequency increase, the resonant or resonant transition converters with ZVS operation should be implemented.

## 5.2 Analysis of the resonant reset forward converter

*There is nothing more practical than a good theory.*  
-James C. Maxwell

### 5.2.1 Introduction

Chapter 0 has shown that the resonant reset converter is one of the most suitable topologies for entirely utilizing the specific properties of the SiC device and for realizing efficient and simple power supplies for 1-1.5kW applications. Although the prevailing property of the SiC JFET is the high breakdown drain voltage capability, in resonant reset converters, it can rise very high and, if not managed properly, can cause breakdown of the switch. Therefore proper design and good understanding of all the converter parameters which can have an influence on the overvoltages is important.

It is well understandable by the author, that high voltage ratings and high dV/dT slew rates are undesirable parameters in today's converter designs. They can accelerate the aging, can impact the isolation reliability of the packages and of the passive components like transformer and capacitors as well. It is believed, however, that the packaging technology and production quality of the passive components will reach the necessary levels for utilization of the SiC power semiconductors without restrictions.

In the following an analyses will be carried out with aim to define critical parameters and operating conditions of the topology

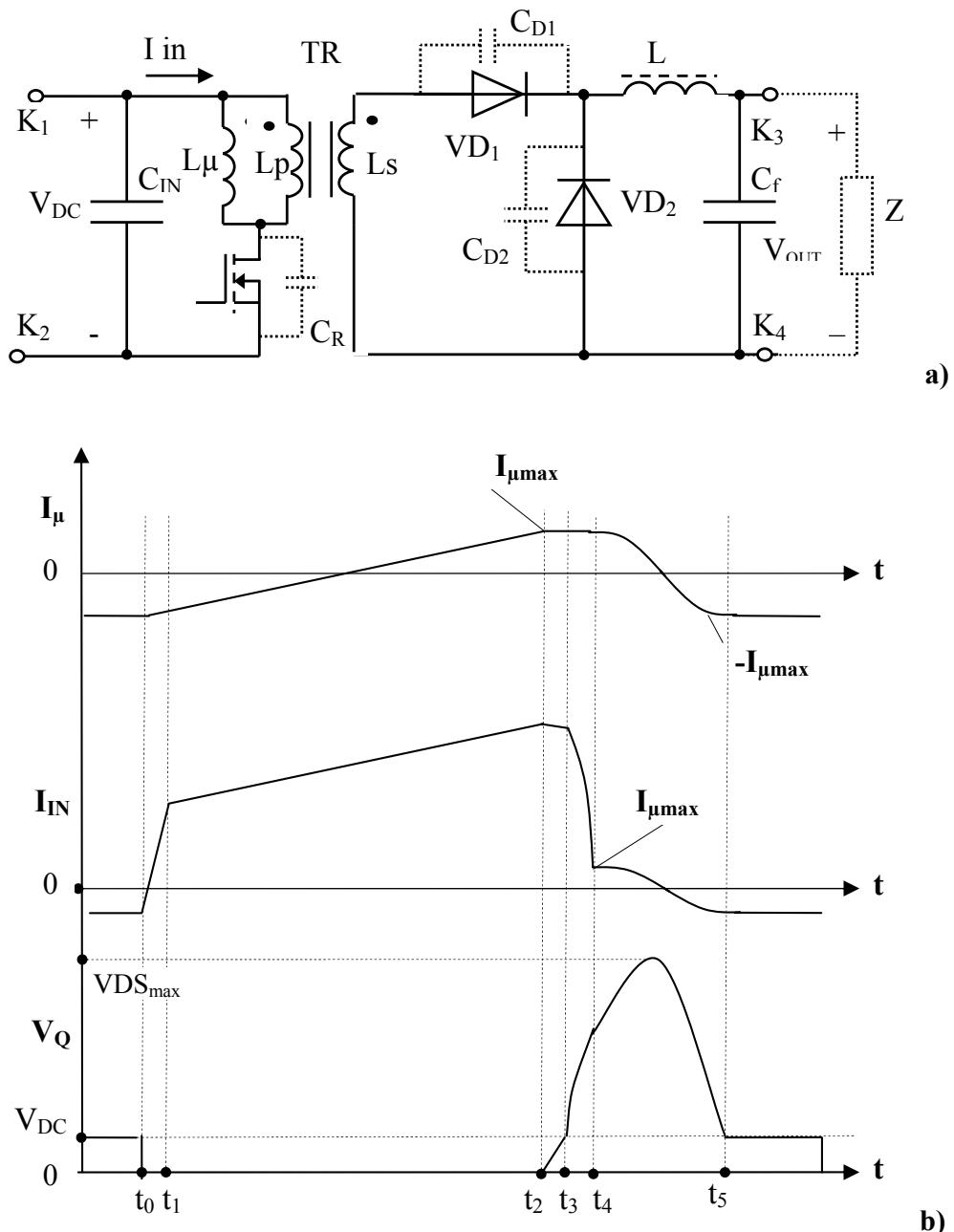
Influence of the parasitic parameters such as device capacitances and leakage inductances are reflected in all calculations

Resonant reset mode and relationship between reset time and device parameters are derived analytically

Operation under light load and short circuit conditions are investigated for proper transformer design

### 5.2.2 Analysis

The operation principle of the resonant reset converter is based on classical single switch forward converter with tertiary winding; therefore, more generally it can be analyzed as a buck converter. The difference is the transformer reset mechanism, which is accomplished with resonant circuit. The resonant reset forward converter and its switching waveforms are shown in Figure 5-4.



**Figure 5-4 Single-ended resonant reset forward converter and switching waveforms**

The resonance circuit consists of the  $C_R$  capacitor connected in series with resonance inductance  $L_p$ , which is the primary inductance of the transformer.

Analysis is performed under following assumptions:

- a) Parasitic capacitances are considered during OFF time of the switches.
- b) The diode reverse recovery time is neglected (assuming to use SiC diodes)
- c) Output current during switching periods is considered constant – the output inductance is large enough
- d) The transformer is considered as T model with equal distribution of parasitic leakage inductances
- e) Transformer winding capacitance has been recalculated and considered as output capacitance of the transistor. Winding resistances considered as negligible small

The circuit analysis can be divided into 4 time periods or phases. Results of detailed calculations and derivations of formulas, where all parasitic influences are considered are placed in Appendix [A2]

**Phase 1: ON time** - During the power transfer stage, when the power transistor is ON, the circuit behavior is the same as for classical forward converter. Equivalent circuit corresponding to this period:  $T_0-T_2$  is depicted in Figure 5-5 a). In this stage the current unity rise begins with minimum input level (which in CCM operating mode corresponds to minimum output current level) and has the following linear form:

$$\frac{\Delta i}{\Delta t_{on}} := \left[ \frac{(V_{in} - V_{out}) \cdot L_{\mu 1} + V_{in} \cdot L_{out}}{L_{\mu 1} \cdot L_{out}} \right] \quad (5-2)$$

**Phase 2: Switching OFF** - Next period is the transition from ON to OFF state. In this period:  $T_2-T_4$  the transistor is going into OFF state and the voltage on the transistor drain will start to rise. As long as on the transformer primary winding applied the positive voltage, the rectifying diode on the secondary side stays open. Therefore the full load current recalculated to the primary side together with magnetizing current will quickly charge the  $C_R$  resonance capacitance up to input voltage level during time interval  $T_2-T_3$ , according to the (5-3) system of differential equation At the same time the parasitic capacitance of the freewheeling diode will be discharged. If the reverse recovery time of the rectifier diode is not negligibly small, then during this time on the capacitor  $C_R$  a higher voltage spike can occur, until the freewheeling diode switches ON and takes the load current. The corresponding equivalent schematic is depicted in Figure 5-5 b)

$$\left\{ \begin{array}{l} L_\mu \cdot \left( \frac{d}{dt} i_\mu(t) \right) + v_c(t) = 0V_{in} \\ L_{out} \cdot \left( \frac{d}{dt} i_{out}(t) \right) + v_c(t) = 0V_{in} - V_{out} \\ C_r \frac{d^2}{dt^2} (v_c(t)) = \frac{d}{dt} i_\mu(t) + \frac{d}{dt} i_{out}(t) \end{array} \right. \quad (5-3)$$

This interval ends at  $t=T_3$ , when the voltage on the freewheeling diode  $V_{D2}$  decreases to zero and the parasitic capacitance of the diode is entirely discharged. Afterwards the voltage on the drain will continue to rise until the whole energy stored in the leakage inductances will be transferred to the capacitor  $C_R$ . Simultaneously the parasitic capacitance of the rectifier diode  $C_{D1}$  will be charged. This period is very short and in calculations [A2] the magnetising current is taken as constant. However the voltage continues to rise and can reach very high values (twice the input voltage e.g. for 400V input and drain voltage can reach 800V). The Phase 2 ends at  $t=T_4$ , when the  $i_2$  reaches zero and the load can be decoupled from the primary side.

**Phase 3: OFF State** - After transition period the circuit will enter in OFF-State:- Period  $T_4-T_5$  (see Figure 5-4). The voltage on the transformer primary is keeping negative and rectifier diode will start to switch OFF. Oscillation will occur caused by resonance circuit  $L_\mu$ ,  $C_R$ ,  $C_{D1}$ . Secondary current will freewheel through the freewheeling diode  $VD_2$ . The corresponding equivalent schematic is depicted in Figure 5-5c.

After some algebraic transformations [A2] the corresponding equation for magnetising current can be written as

$$i_\mu(t) := A_2 \cdot \cos[w_g \cdot (t - T_4) + B_2] \quad (5-4)$$

By integrating the both sides of the equation, with appropriate initial conditions ( $V_o = V_{off\_max}$  and  $I_o = I_{off\_max}$ ) we can find the voltage on the resonance capacitor  $C_R$

$$v_Q(t) := E_{in} + A_2 \cdot Z_2 \cdot \sin[w_g \cdot (t - T_4) + B_g], \text{ where}$$

$$w_g := \frac{1}{\sqrt{L_\mu \cdot (C_Q + C_{D1})}}, \quad (5-5)$$

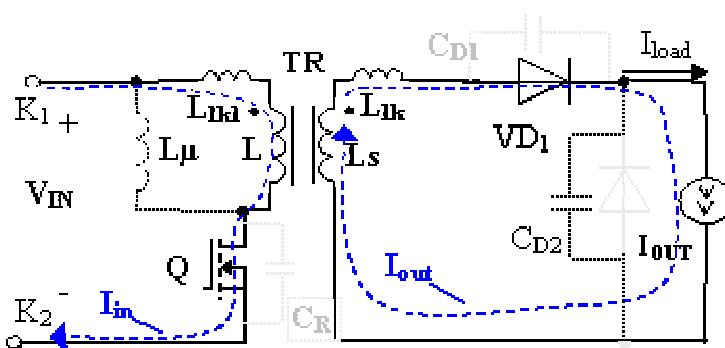
$$Z_2 := \sqrt{\frac{L_\mu}{C_Q + C_{D1}}},$$

$$Y_2 := \begin{cases} \text{atan}\left(\frac{v_{QT4} - E_{in}}{Z_2 \cdot i_{\mu T4}}\right) & \text{if } i_{\mu}(T_4) > 0 \\ \pi - \text{atan}\left(\frac{v_{QT4} - E_{in}}{-Z_2 \cdot i_{\mu T4}}\right) & \text{otherwise} \end{cases}$$

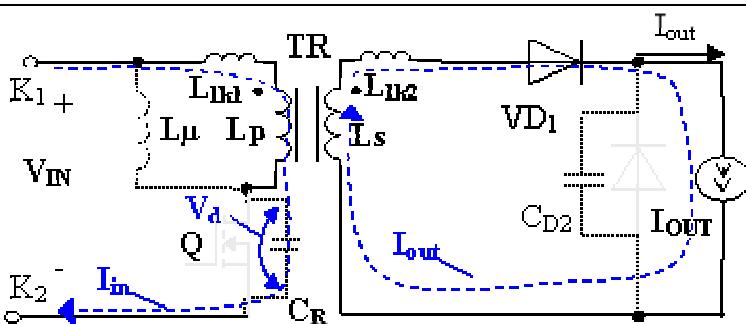
At the end of this phase ( $T_4-T_5$ ), the resonant circuit resets the core energy. It can be seen from calculation and from simulation results presented later, that in application with 1kW-1.5 kW and 0.75 Duty Cycle the power switch has to withstand at least 1500V drain voltage.

#### Phase 4: Secondary side short circuit

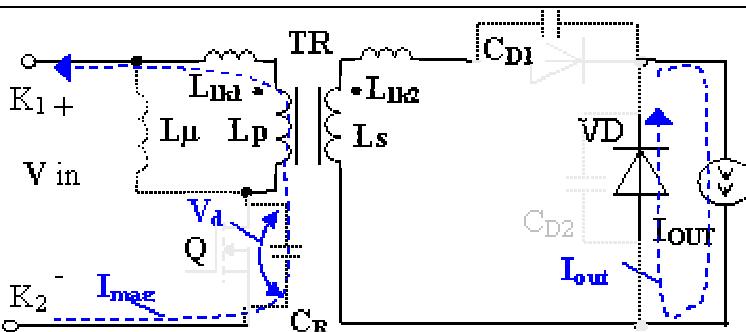
At  $t = T_5$ , rectifier diode  $VD_1$  turns ON again and the operation stage changes to the equivalent circuit shown in Figure 5-5 d). When the output capacitance  $C_R$  recharged back to input voltage level  $V_{IN}$ , the voltage drop on the primary winding will try to be positive again.  $VD_1$  will be positive biased and turns ON. But the secondary side freewheeling current is still flows through output inductor (CCM). Through the simultaneously opened  $VD_1$  and  $VD_2$  (marked red) the secondary transformer winding is shorted. The voltage on the primary winding could not be changed further. During this period the negative magnetising current will remain unchanged (theoretically), until the next cycle. In practice, due to leakage inductance and parasitic capacitance of the switch, the current will oscillate around the average magnetising current level. The oscillation will however decay rapidly due to winding resistances of the transformer. Also the circulating magnetizing current will slightly decrease. To have minimum switching ON losses, it is beneficial to catch the voltage downslip and switch ON at minimum of drain voltage. Practically it is possible to switch ON with drain voltages much lower than  $V_{IN}$ , by utilising the parasitic inductances and stray inductance of the transformer. In next section it will be shown, that by appropriate design it is possible to have ZVS operation in wide voltage range.



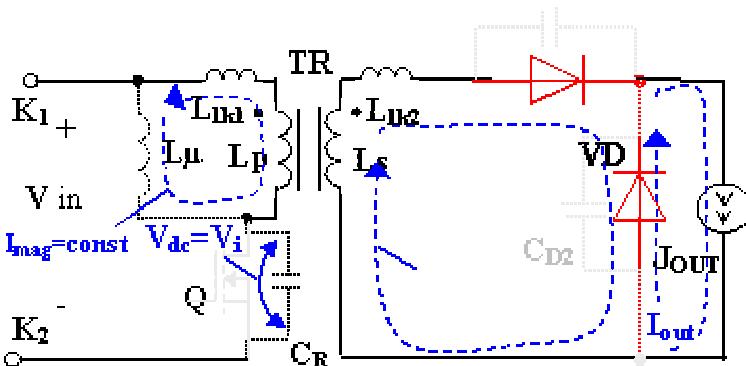
**A)** Phase I – the switch is switched ON and the current, flowing through the primary winding, transferred to the secondary side of the transformer and delivered to the load



**B)** Phase II – as soon as the switch is switched OFF, the magnetizing current will charge the drain-source. Eventually the voltage on the primary winding will be reversed. Simultaneously demagnetization of the transformer core will take place



**C)** Phase III Demagnetizations of the transformer will continue, the current will resonate, change its direction and discharge the capacitor  $C_R$  until the voltage on the primary winding of the transformer returns back to zero.



**D)** The voltage on the primary winding would oscillate further below zero level; however it will be clamped to zero level, because of shortened secondary winding – hence the transistor drain voltage will be clamped to input voltage level.

Figure 5-5 Equivalent circuits of resonant reset forward converter in different states

### 5.2.3 Operation at light-load and short-circuit condition

#### No load operation condition

In open load condition the converter will be able to operate always in ZVS mode due to zero output current and, therefore, zero clamping current (see phase 4 in topology analysis). The control circuit will detect the zero crossover and half-sine wave voltage oscillations will be applied on the transistor drain during OFF-time. Because of open load the overvoltage will be given only by magnetizing current energy which will be transferred into the equivalent drain capacitance according to

$$\frac{V_D^2 \cdot C_{RES}}{2} = \frac{L_\mu \cdot I_\mu^2}{2} \quad (5-6)$$

#### Light load operation condition

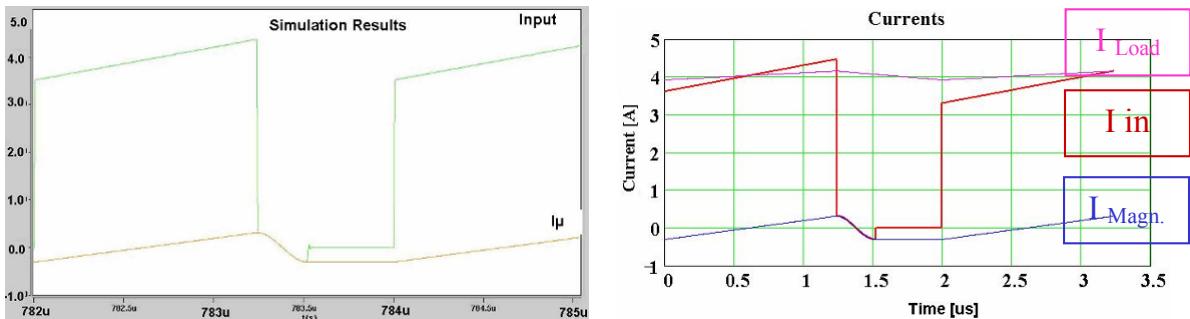
The absolute level of magnetizing current depends on output load. From Figure 5-4 is visible, that transformer flux excursions between first and third quadrant of the B-H plane. This is similar to a push-pull topology. The flux excursion at light load is always symmetrical at light load.

#### Heavy load or short circuit condition

As the load becomes heavy, the center of flux excursion is moving into the third quadrant Figure 5-4 b). When the converter is overloaded and the main switch ON-time is very short, the magnetizing current will remain below zero. This corresponds to the main transformer flux excursion only in third quadrant of B-H plane.

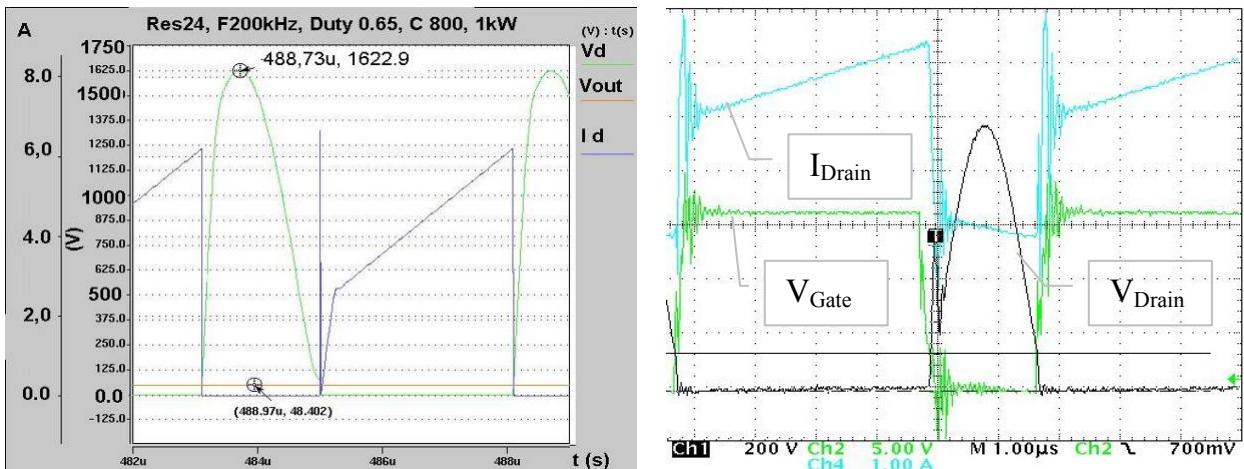
### 5.2.4 Simulations for higher power and higher voltage levels

Investigations on possible higher power levels and higher drain voltages are carried out with Saber™. Firstly, the simulation models of the components used in circuit are verified with calculations in given power and voltage ranges. Figure 5-6 shows a good match between simulation and mathematical results of the drain and magnetising currents.



**Figure 5-6 Model Verification Results of calculations with Mathcad™ and with Saber™**

Figure 5-7a) shows the possible drain overvoltage, which occurred during converter operation at higher duty cycle. Important to note that at 200 kHz switching frequency the overall resonance capacitance can be reduced down to 800pF if higher drain voltage e.g. 1650V can be tolerated. On the other hand, from the drain current waveform we can see that during switching ON the resonant capacitor (equivalent total capacitance) is discharging through the switch causing current spikes (Figure 5-7b blue trapezoidal curves). Even the discharge of the 800pF capacitances from the 400V can increase switching losses, which at frequencies above 200 kHz could be unacceptable high. Taking into account that the discharging energy is proportional to the square of voltage, the realization of the soft switching (ZVS) in our topology is highly desirable.

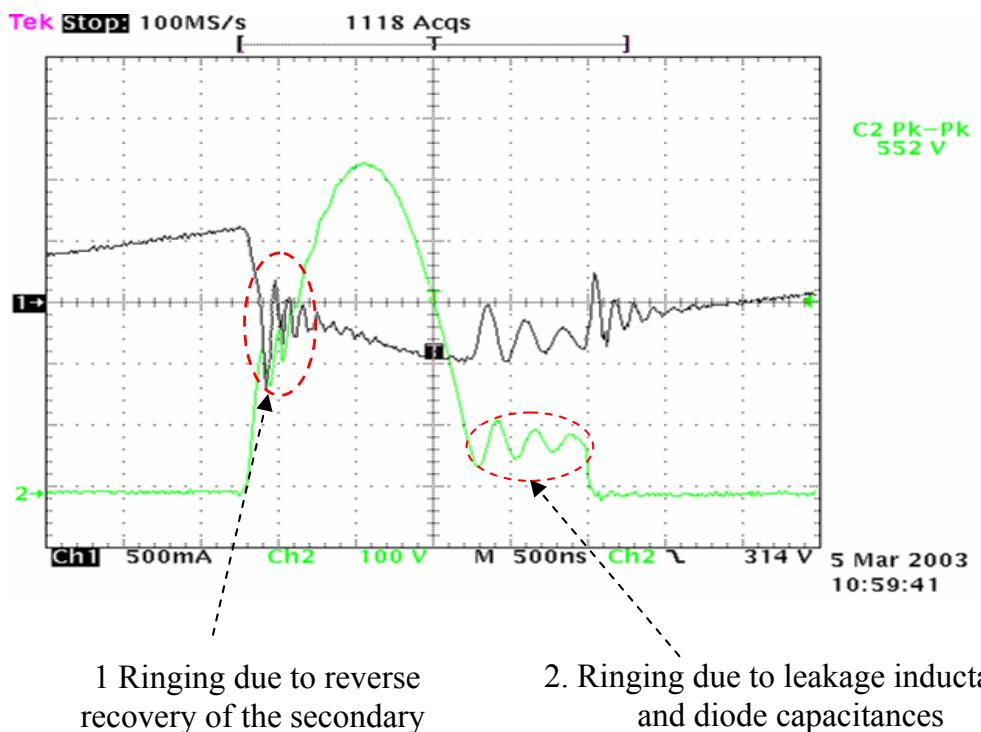


**Figure 5-7 a) Simulation results for higher drain voltages, b) switching losses and oscillations**

### 5.2.5 Obtaining Zero Voltage switching operation

One of the fundamental stumbling blocks in increasing the frequency is the parasitic elements in the circuit, therefore the solutions should be found to overcome this limitation. In the following, will be shown how the SiC devices can help to increase the switching frequency. Figure 5-8 shows two parasitic effects. Due to reverse recovery problem of the rectifier and freewheeling diodes, the overvoltage spikes and increased energy losses can take place. The secondary side reverse recovery effect can be fully eliminated by using SiC diodes see (Figure 5-9). Here the switching property of the SiC diodes is utilized for additional frequency increase. It should be mentioned, that only at higher frequencies (above 100 kHz) the advantage of SiC Power Schottky Diodes becomes evident [88].

From the Figure 5-8 we can see also the second problem - the leakage inductance rings with the secondary capacitances during dwell time. It also slows down the rise time of the primary current during turn-ON.

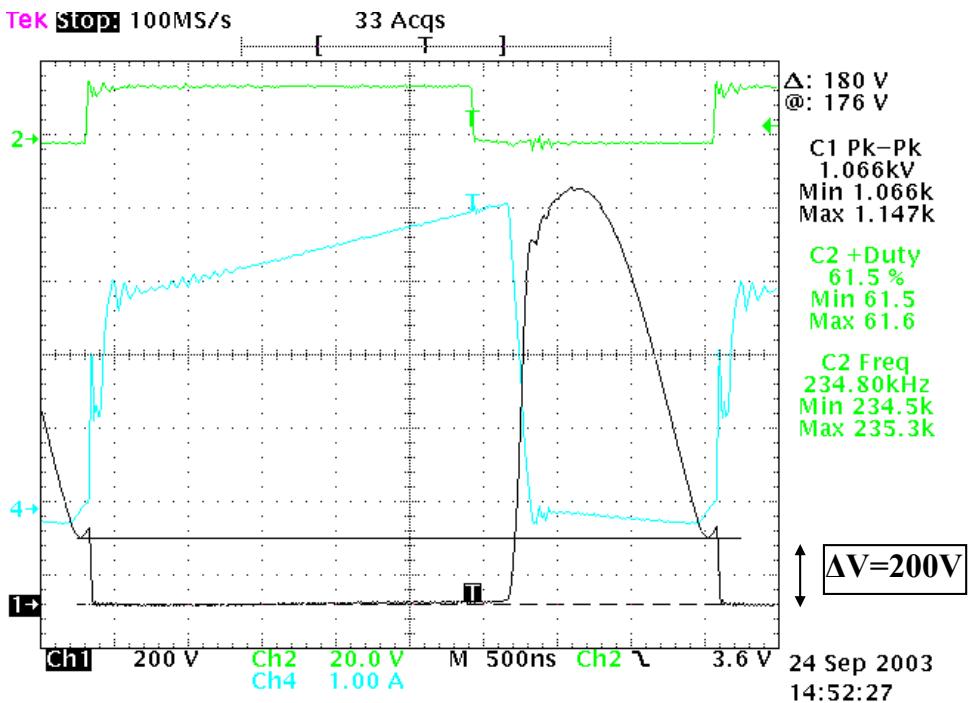


**Figure 5-8** Switching drain voltage (Ch 2 Green) and current (Ch 1 Black) under influence of parasitic elements. The ringing voltage amplitude depends on the output load and leakage inductance

There are two ways to deal with the problem of leakage inductance ringing with the secondary capacitance. The first is to minimize the stray inductances as much as possible, and just use snubbers to control the ringing, EMI, and corresponding component stress. Most of designers do this in designing conventional PWM converters. However, the

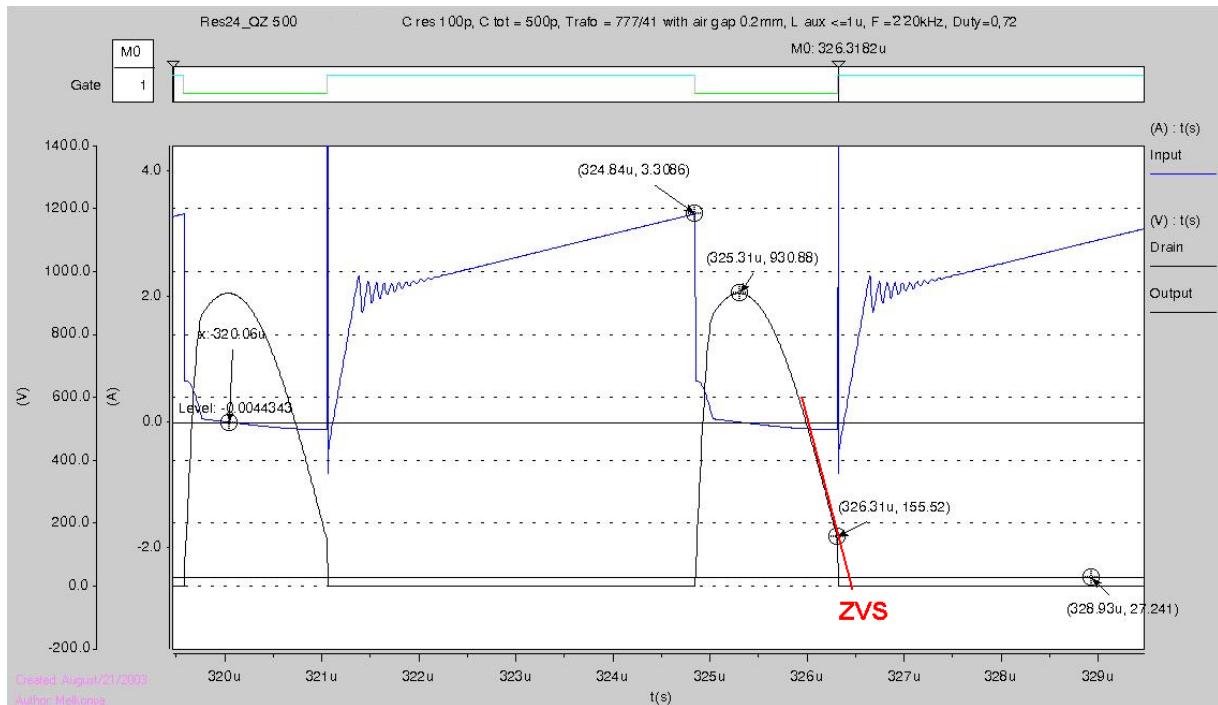
coupling between transformer winding is always not ideal, and for our converter, it is impossible to reduce the leakage beyond a certain minimum level because of isolation and safety requirements in high voltage transformer. Another approach is to actually increase the leakage inductance and provide a way to decouple the secondary side from the primary for a short while in the last stage of switching period (Phase 4 in Chapter 5.2). This solution will be presented in more details below.

The converter is utilizing the Drain to Source capacitance both for demagnetization purposes of the transformer and as lossless snubber. The high blocking voltage capability of the SiC JFET allows accelerated demagnetization of the transformer, increasing the duty cycle, frequency and reduction of the necessary snubber capacitance value. At higher frequencies, however, even discharging of the parasitic drain-source capacitance through FET presents a problem. From the MathCAD calculations and practical results Figure 5-9 we can see, that having enough stray inductances and higher magnetization current, the energy stored in parasitics will draw the drain voltage below the input voltage level. By designing proper control circuitry, it is possible to catch the minimum voltage and switch the transistor ON, always at minimum of the drain voltage. So the minimisation of the switching ON voltage is leading to the appropriate control technique. In this case the control method is fixed OFF time and variable on time -hence variable frequency control.



**Figure 5-9** Switching waveforms of the converter with SiC secondary side diodes. Drain voltage from input level (400V) is falling down to ~180V, where the switching ON takes place.

However, because of the small amount of energy stored in stray inductances, the voltage does not fall enough low, and real zero drain voltage is hardly obtainable in this way. Further increase of the stray inductances especially at high frequencies is not desirable. Therefore the drain voltage downswing should be tolerated further by the secondary side (see analysis Phase 4). Simulation results are illustrated in Figure 5-10. By extrapolating the drain voltage waveform, it can be seen, that after 100-200ns the voltage would reach the zero level.



**Figure 5-10 The simulation results at higher duty cycle and low output power. In order to obtain ZVS the drain voltage should be able to swing down during very short time.**

This brings us to the following – the ZVS condition in resonance reset forward converter can be realized by introducing a time delay between getting the positive voltage on the secondary winding and turning on the rectifier diode. The implementation of the idea is straightforward (Figure 5-11a) – replacing the rectifier diode with the high frequency thyristor (SiC Thyristor with  $t_q < T_{demag}$  ( $\sim 1\mu s$ )). Such a future SiC junction controlled thyristor is reported in [16].

The same result can be also achieved with the low  $R_{DS(on)}$  power MOSFET connecting in series with existing rectifier diode (Figure 5-11b). This, however, is applicable for relatively low output currents, because of additional on state power losses in the transistor.

For output currents above 5 A, the solution, which is actually implemented in experimental board, is a saturation reactor inserted between the rectifier diode and the secondary winding (Figure 5-11c). The tiny ferromagnetic choke serves as a decoupling element. It is designed such a way, that at the first moment, when the voltage on the secondary winding becomes positive, it has a big reactive resistance. It blocks the positive voltage applied to the rectifier and allows further voltage increase on the transformer windings. The voltage on the drain will decrease and after short time it will reach the zero point. The switch can be switched on, with the zero voltage on it. At that time the saturation reactor enters in saturation and after loosing all the energy has no any influence on the rest of the converter functionality until next switching cycle. This simple solution, compared to the previous two solutions does not require any control circuit and has lower energy losses. This solution is applicable for higher power and high output currents. The time delay (time elapsed before entering into the saturation) can be adjusted externally and combined with possible post-regulation with so called magamps or it can be fixed to maximal value by design.

The short time, during which the drain voltage swings down to zero, depends on resonant circuit parameters and the maximum allowable drain voltage. The higher the drain voltage the less time is to be blocked by saturable reactor.

Here again the high breakdown voltage capability of the SiC transistor is utilized to swing the voltage down to zero and realize ZVS operation. The high  $V_{DS}$  allows using very small saturable reactor having small cross-section area and volume, which has consequently lower losses.

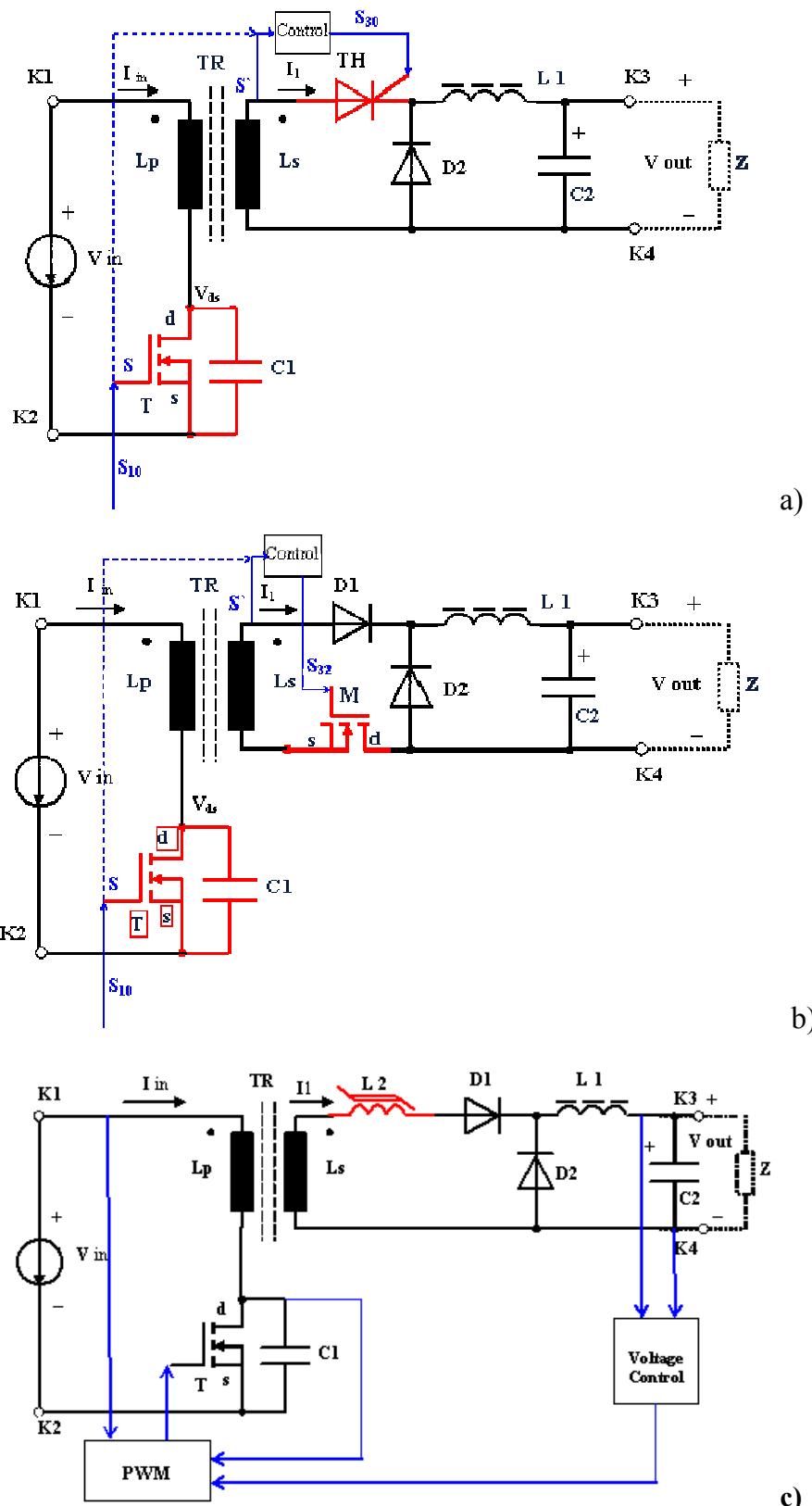


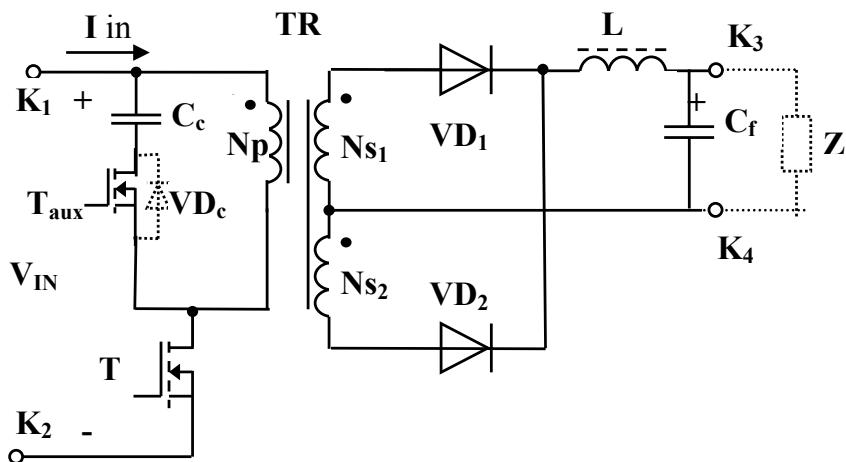
Figure 5-11 Realization of the ZVS in resonant reset forward converter using:

a) high frequency SiC Thyristor, b) low  $R_{ON}$  MOSFET and c) using saturation reactor

## 5.3 Application of the SiC devices in alternative topology

### 5.3.1 Single switch double-ended Forward-Flyback converter

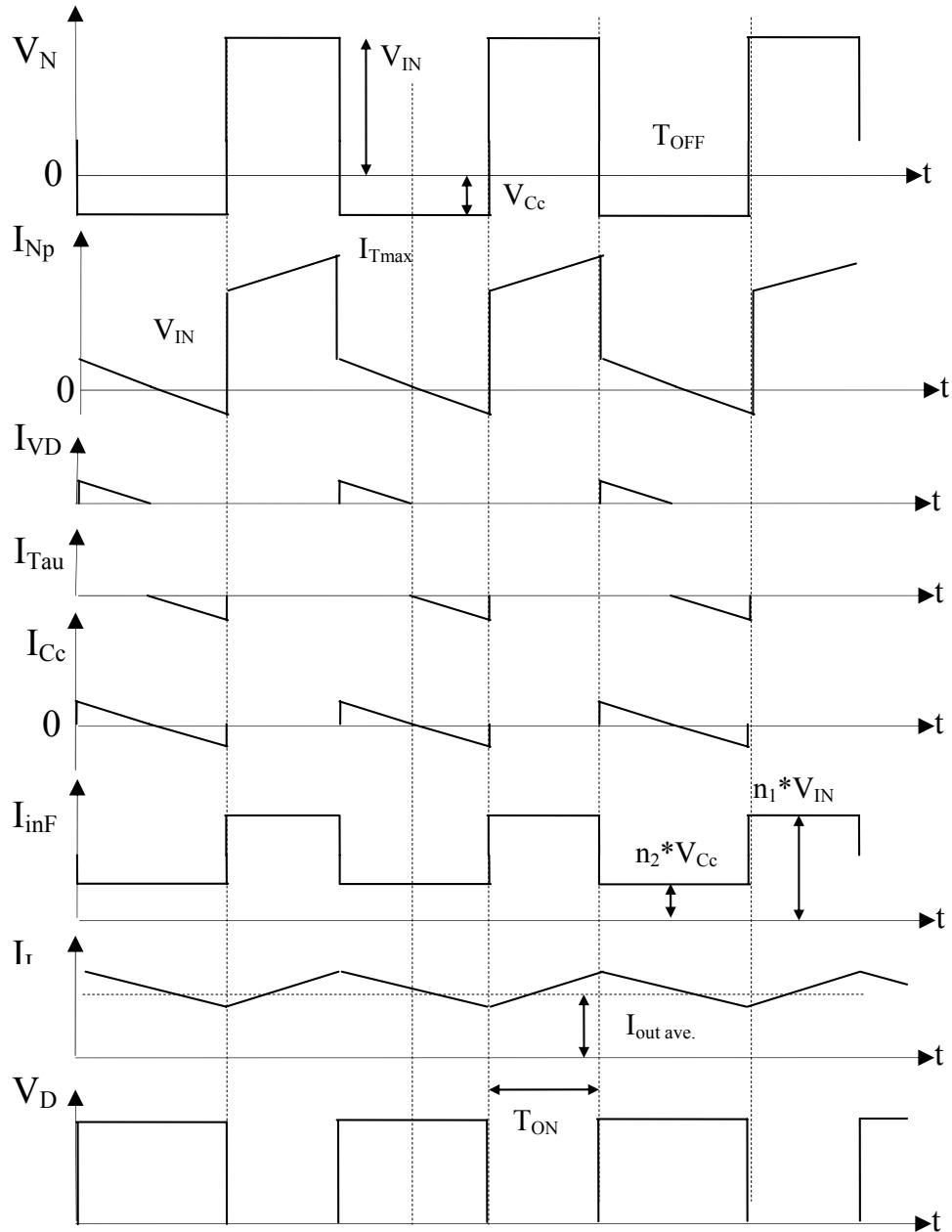
One interesting future provides converter illustrated in Figure 5-12. It is somewhat a combination of Flyback and Forward converters. The unique feature of this topology is that it can transfer energy both during OFF and during ON time of the main power switch. Therefore the modulation depth of the voltage on the output filter is much lower. This reduces the size of the output inductor drastically. In classical form [90], the topology has an active clamp circuitry realized with auxiliary transistor  $T_{AUX}$  and clamping capacitor  $C_c$  placed on the primary side.



**Figure 5-12 The double ended forward converter – it combines the Flyback and Forward converters by providing energy transfer both during switch ON and switch OFF time [90].**

The operation principle is clarified in switching waveforms illustrated in Figure 5-13. The main transistor  $T$  and auxiliary clamping transistor  $T_{aux}$  are controlled complementary. During switch ON time the auxiliary switch is in OFF state. The voltage polarity of the clamp capacitor  $C_c$  keeps the body diode of the transistor reverse biased. Also diode  $VD_2$  is switched OFF. In this stage (during  $t = D*T$ ) the operation principle is exactly same as in conventional forward converter with demagnetizing winding, which is presented in Table 2-4. After switching the main transistor OFF, the diode  $VD_1$  is closed and  $VD_2$  is forward biased. In this stage the equivalent circuit of the topology is becoming similar to the Flyback converter, comprising capacitor  $C_c$ , diode (body)  $VD_c$  and primary winding  $N_p$ . However the operation principle in this stage is different. The magnetizing energy of the transformer is provided to the load, and the capacitor  $C_c$  is taking only the difference between the current of output inductor ( $I'_L = I_L$  recalculated to the primary side) and the magnetizing current. During first half of switching OFF time ( $[1-D]*T/2$ ), this current

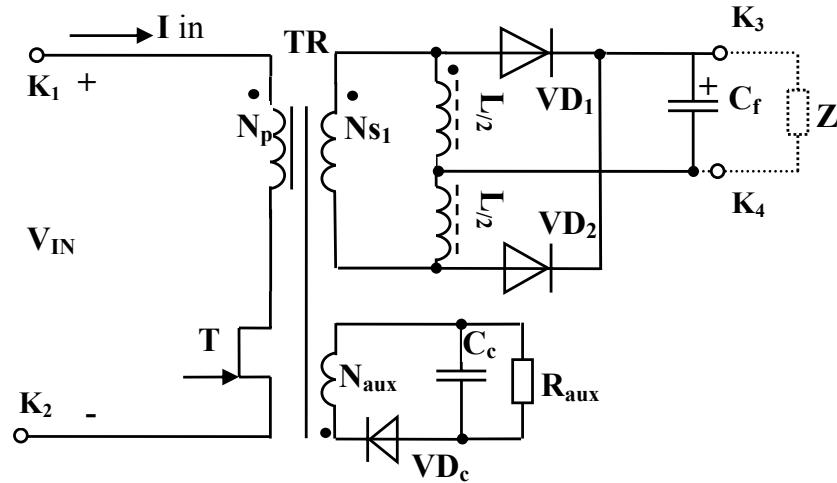
flows through the body diode  $VD_C$ , another half time - through the auxiliary switch  $T_{aux}$  in opposite direction. As we can see from switching waveforms Figure 5-13, the capacitor  $C_C$ , does not give its energy to the load like the Flyback converter does, but takes the current difference of the inductive elements connected in series during OFF time. The voltage of the capacitor  $C_C$  is applied to the secondary side during switch OFF time. The modulation depth of the voltage on the input of LC filter is consequently much lower. This can drastically reduce the volume of the needed filter components.



**Figure 5-13 Switching waveforms of the single switch double-ended forward converter**

This topology can be transformed to following equivalent topology, where the high side clamp transistor  $T_{aux}$  can be replaced by passive clamp Figure 5-14. The additional current for forward biasing the diode  $VD_C$  will obviously contribute to the overall magnetizing

current, however its contribution will be negligible compared to the overall current level. If the auxiliary winding  $N_{aux}$  is wound bifilar with the secondary, then the values for  $R_{aux}$  and  $I_{aux}$ , derived in [B1] should be correspondingly rescaled with transformation coefficient  $n_{aux} = N_p/N_{aux}$ . All other parameters and calculations from [B1] remain the same.



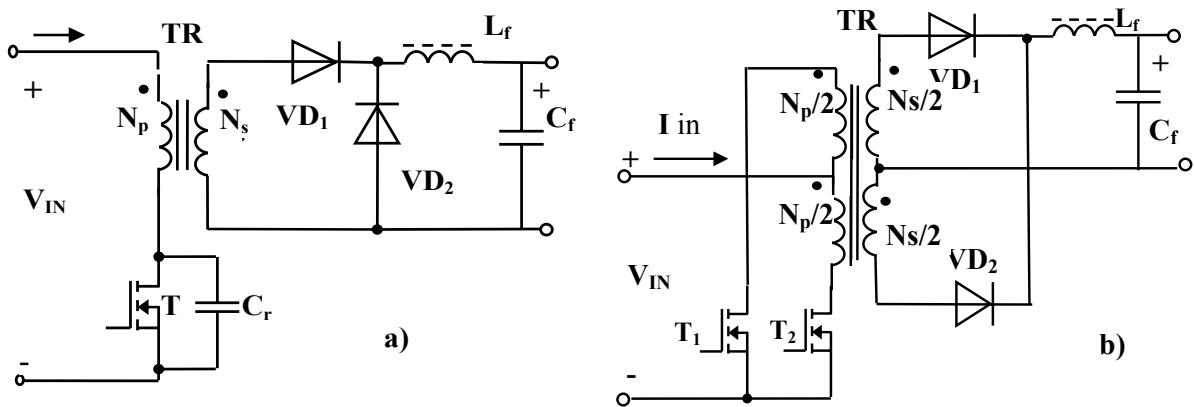
**Figure 5-14 Single switch double ended Forward –Flyback composite converter clamped through auxiliary winding**

The drawback of this topology is its high magnetizing current which is equal to the average load current recalculated to the primary winding. However, with using high voltage SiC transistor in this topology, it would be possible to realize high frequency simple auxiliary power supply, e.g. for high voltage motor drive applications, where input voltage rail is very high (800-1000V), and no MOSFETs are available for single switch low power converter realization.

## 5.4 Comparative study of the single switch and multi-switch topologies

As it is shown in previous chapters, the single switch resonant reset converter can provide better utilization of the specific properties of SiC power transistor. However, there is a settled opinion, that any single-ended topology, despite of its very simple configuration, has worse mass and volume factors than their double ended counterparts. Therefore, up to nowadays, the converters with single-ended topologies are rated as inherently lower power density converters. To find out the influence of the SiC switch on the power density of the converter, single-ended and double-ended topologies will be analyzed and compared towards volume-weight parameters of their passive components – (filters, transformer), which are primarily defining the power density of the converters.

Figure 5-15 shows a push-pull converter b) with center-tapped transformer, which can be realized with conventional Si MOSFETs and the single switch forward converter a) with resonant reset which needs a high voltage SiC device. In both of these configurations the energy transfer is taking place during switch ON time.



**Figure 5-15 Single-ended (resonant reset forward) and double-ended (push-pull) converter**

Chapter 2.2.1 shows that the single switch forward topology (derived from buck converter), in continuous current operation mode (CCM) has a “hard” output transfer characteristics same as in double ended topologies (see also Appendix A1). The transformer demagnetization in this converter is accomplished by means of resonant capacitor. It was also shown, that at higher frequencies this capacitor can be replaced by the sum of distributed capacitance of the windings and parasitic output capacitance of the switch.

The comparative analysis is carried out with equal for both topologies commutation conditions. That is for push-pull converter at switching frequency  $f$ , and for forward converter at switching frequency  $2f$ .

In resonant reset converters the current modulation depth on the magnetic components, corresponding the maximum duty cycle can reach 0.65-0.8. In the push-pull converter, in contrast, the maximum modulation depth can reach 0.9 taking in account the delay time  $T_d$ , which is an unavoidable dead time in all multi-switch topologies. In the analysis the

coefficient  $D_{\max} = \frac{t_{ON}}{t_{ON} + t_{OFF}} = 0.7$  for resonant reset forward converter will be chosen

with assumption that the overvoltage on the main switch will reach 2.7-3.0 times the input voltage:  $V_{D\max} = 2.7..3.0 \cdot V_{IN}$ . The coefficient  $D_{\max} = 0.9$  for push-pull converter can be obviously chosen as maximum value, in order to be able to prevent the possible shoot-

through during the switching transient in the power switches. The analysis is carried out with following steps:

- ✓ The switch ON time duration for double ended topologies:  $t_{ON} = D / 2 \cdot f$ , and the ON time duration for single-ended topologies:  $t_{ON} = D / F$ . The average input current of the converters is equal to

$$I_{IN}^{ave} = \frac{P_{load}}{U_{in} \cdot \eta}, \text{ where} \quad (5-7)$$

$U_{in}$  - is the input voltage of the converter,  $P_{load}$  - is the output power,  $\eta$  - is the converter efficiency app. 85-93%.

- ✓ The maximum input current can be defined as:  $I_{IN}^{\max} = \frac{I_{IN}^{ave}}{D}$ , and the effective value of the transformer current is  $I_{IN}^{RMS} = I_{IN}^{\max} \cdot \sqrt{D}$ . The capacitance of the input filter is calculated according recommendation for using electrolyte capacitors  $I_C^{RMS} \leq 0.5A$  per capacitor [89]. Having the equivalent series resistance and input current of the electrolyte capacitor the ripple voltage on it will be  $U_{C_{in}}^p = 0.5 * I_{IN}^{\max} \cdot ESR_{C_{in}}$ ;

For the input capacitance the maximum voltage ripple will be:

$$U_{C_{in}}^R = \frac{I_{IN}^{ave} \cdot t_{OFF}}{2 \cdot C_{in} \cdot K\phi} \quad (5-8)$$

where  $K\phi$  is showing the dependency of the capacitor from the frequency, for 200kHz the  $K\phi \approx 0,3$  [89]

The total input voltage ripple on the capacitor is the sum of (5-7) and (5-8):

$$U_{C_{in}} = U_{C_{in}}^p + U_{C_{in}}^R \quad (5-9)$$

- ✓ Inductance value of the output filter is given as  $L_{out} = \frac{U_{load} \cdot t_{ON}^{\max}}{\Delta I_{load}} \frac{1}{1-D}$ , where

$\Delta I_{load} = 0.1 \cdot I_{load}$  - is the maximal allowable ripple current,

$t_{ON}$  - is the maximal pulse duration.

The number of turns in output filter is equal to  $w_{Lout} = \sqrt{\frac{10^8 \cdot L_{out} \cdot l_{mag}}{1,26 \cdot S \cdot \mu}}$ , where  $l_{mag}$  is the average flux path length of magnetic core; S is the cross section area of the magnetic core. In the prototype design the ring MP3310 with distributed air gap is used.

This metal-powder magnetic material allows the maximum flux of 1,56T. The output

$$\text{capacitors ESR for the given output ripple voltage will be } ESR_{Cout} = 2.5 \frac{f \cdot L_{out} \cdot U_{Cout}}{U_{load}}$$

$$\text{The number of turns of primary winding is equal to } w_{prim} = \frac{10^4 \cdot U_{IN} \cdot t_{ON}}{K1 \cdot B_{max} \cdot S}, \text{ where}$$

$B_{max}$  - is the maximum flux (for frequencies over 50 kHz should be limited to 0.2...0.25T

K1 is equal to one for single-ended converters and to 2 for double ended converters.

- ✓ The maximum drain voltage can be roughly estimated as  $U_D^{max} = U_{IN} \left( 1 + \frac{D}{f} \sqrt{\frac{1}{L_\mu \cdot C_R}} \right)$ ,

where  $L_\mu$  - is the magnetizing primary inductance,  $C_R$  - resonance capacitance.

In Chapter 5.2 possible maximum drain overvoltage is analyzed in details. However, it is very important to mention here, that at the given maximum “duty cycle” the resonant reset duration must be at least the quarter of the  $L_\mu C_r$  oscillations.

As we can see from the results listed in Table 5-4, both push-pull and resonant reset converter have the same output capacitors and the same number of transformer windings. The input filter capacitance in worst case is equal 22.8uF and 30uF for Push-Pull and Resonant Reset converters respectively. However from practical point of view for both cases two 15uF parallel connected capacitors will be selected.

The slightly increased output filter inductance value from 264 to 312 uH is the only difference between passive components of the converters.

The comparison results of the converters are listed below in the Table 5-4 for the following input parameters:

$$\begin{array}{lll}
 U_{IN} = 200 - 340 \text{ V} & \text{- Input voltage} & V_{IN}^{Ripple} = 2.5 \text{ V} \\
 U_{out} = 48 \text{ V} & \text{- Output voltage} & V_{OUT}^{Ripple} = 0.5 \text{ V} \\
 I_{out} = 20 \text{ A} & \text{- Output current} &
 \end{array}$$

Parameter	Double-ended topology			Single-ended topology		
U <sub>in</sub> [V]	300	370	440	300	370	440
D	0.9	0.59	0.45	0.7	0.5	0.35
F [kHz]		100		-	200	-
T <sub>ON</sub> [us]	4.5	2.95	2.25	3.5	2.5	1.75
T <sub>OFF</sub> [us]	0.5	2.05	2.75	1.5	2.5	3.25
I <sub>in average</sub> [A]	2.38	1.93	1.78	2.38	1.93	1.78
I <sub>in max</sub> [A]	2.64	3.27	3.97	3.04	3.86	5.1
I <sub>in RMS</sub> [A]	-	2.51	-	-	2.73	-
C <sub>IN</sub> [uF]	3	10	22.8 (2X15)	8.4	17.4	30 (2X15)
U <sub>Cin~</sub> [V]	0.86	1.06	1.99	1.1	1.85	1.95
U <sub>CinR</sub> [V]	1.64	1.43	0.50	1.40	0,65	0.57
U <sub>CinP</sub> [V]	-	-	2.5	-	-	2.5
U <sub>out</sub> [V]	-	48	-	-	48	-
L <sub>out</sub> [uH]	-	-	264	-	-	312
W <sub>Lout</sub> [turns]	-	30	-	-	33	-
C <sub>out</sub> [uF]	-	65	-	-	65	-
ESR <sub>Cout</sub> [Ohm]		1			1	
B <sub>max</sub> [T]	-	0.27	-	-	0.2	-
W <sub>prim</sub> [turns]	-	25X2	-	-	50	-
W <sub>sec</sub> [turns]	-	9X2	-	-	23	-

**Table 5-4 Different comparative parameters of the double and single-ended converters**

## 5.5 Summary

In this chapter the most suitable topology for implementing the SiC devices is selected and its main characteristics were determined analytically.

- ✓ The single-ended and double-ended topologies are examined, and the main advantages of the multi-switch double-ended topologies over the single switch topologies are identified. It was shown that the biggest drawback – high voltage stress in single switch converters can be overcome with SiC high voltage JFET.
- ✓ From vast variety of single switch topologies the resonant reset converter is selected as most favorable due to following reasons:
  - a) It does not need external reset circuit and it is the simplest isolated converter topology
  - b) Generally has no problems with magnetic flux symmetry imbalance in transformer core
  - c) It has a bi-directional magnetic flux excursion in the transformer core (symmetrical at nominal, light load and no-load operation )
  - d) It recuperates demagnetising energy by means of storing it in resonant tank
  - e) It has basically not limited duty cycle ( over 0.5 is possible)
  - f) Thanks higher switch utilisation the overall semiconductor cost can be decreased
- To the less desired features of the converter can be considered:
  - g) Relatively high peak reset voltage accelerate demagnetisation of the core, and very high voltage switches are necessary
  - h) Reset dynamics depends on overall circuit parasitics, particularly drain-source capacitance of main switch.
  - i) The switching frequency can be additionally increased only if ZVS is realised
- ✓ Operation at open circuit, light load and short circuit conditions are outlined where transformer flux excursion is examined.
- ✓ Simulation for higher power and voltage levels is carried out.
- ✓ It was shown how the specific properties of the SiC devices can be further utilized for realizing zero voltage switching (ZVS) operation of the converter.
- ✓ Another single switch topology is examined towards optimal implementation of SiC transistor. The converter's operation characteristics, specific properties, advantages and drawbacks were analytically determined. Possible application as supporting low power auxiliary power supply for motor drive is proposed.
- ✓ Comparative analysis is provided showing minimal (15%) increase of output filter inductor value compared to the two switch push-pull converter.

## 6 Gate driver for the SiC VJFET

### 6.1 Introduction

For using the SiC JFET switch in Resonant Reset Forward converter an appropriate gate driving circuit (GDU) should be designed. Such GDU circuitry should provide a negative voltage to turn-OFF the JFET and zero volts for turning it ON. In this chapter two different novel approaches are proposed. However, these are not supposed to be complete solution for series production, rather than for trial purposes. Their expanded versions, which can include adaptive current source or controlled voltage loop, are subject for future investigations. There are also other experimental works about possibilities for realizing a GDU for JFET published by ETH Zürich [84], [67]. These gate drivers are also realized and experimentally compared with proposed driver circuits.

### 6.2 Current and voltage requirements

For designing a gate drive circuit, the gate requirements of the transistor should be specified. The main parts can be specified as:

- a) Gate voltage - the maximum and minimum threshold voltage levels when the transistor is switched OFF and ON
- a) Gate power
- a) Signal isolation and transmission if required
- a) Negative and positive voltage overshoot protection
- a) Short circuit and overcurrent protection

#### Gate voltage

Turn ON – at the 0V gate voltage the channel of the JFET is fully conducting (Normally ON). The output voltage rise time of the gate driver should be as fast as possible. However in order to prevent the parasitic oscillations, the drain voltage rise time should be limited to 50-60ns (obtained experimentally).

Turn OFF –The voltage needed to pinch the channel OFF is dependable and varies from sample to sample. In “pentode like” JFETs it depends mostly from the voltage blocking gain  $\mu$ . From the experience on the samples provided so far, some 600V JFET has required about -23V gate voltage, others needed as high as -40V to be fully switched OFF. By constant blocking gain  $\mu$ , the required turn OFF voltage is equal to  $V_{\text{Gate}} = - V_{\text{DSmax}} / \mu$ .

Note that for minimizing the oscillations the switching speed should be limited. In case of provided JFET, where the gate capacitance is the reverse biased pn-junction, the recommended gate resistance can be in range of 10-30 Ohm. The maximum drain voltage fall time should be also limited to 40ns (obtained experimentally and application dependent)

### **Gate power**

The gate driver must deliver enough power for switching the JFET transistor ON and OFF with any possible voltage levels and switching frequencies and under worst case gate capacitance. According the measured gate charge in some samples and needed voltage levels the gate power should be about 8Watts.

### **Signal isolation and transmission**

There are different ways to transmit the gate signals. In proper design the gate drive units should be located next to the power switches. Therefore the input signals must be transmitted from controller to GDU. Depending whether high switching speed and /or high temperature is needed or not, the optocouplers, magnetic, magneto-resistive or capacitive galvanic isolators can be used. It is important to note, that SiC JFET devices can have switching times less than 40-30ns. In such cases the driver coupling capacitance and common mode noise rejection can be critical, therefore careful gate driver design is mandatory.

### **Negative and positive voltage overshoot protection**

As it was shown previously, the gate of JFET is just a diode junction, which is reverse biased when JFET turned OFF. This means, that the excessive gate voltages should be avoided in order to prevent secondary breakdown. It must be noted, that the minimum voltage required for switching OFF can be rather high. And in some cases the gap between secondary breakdown level and pinch-off voltage is rather narrow – about 3-8V.

For this reason the current limiting future could be advantageous, which will also limit the current in case of positive biasing of the gate diode.

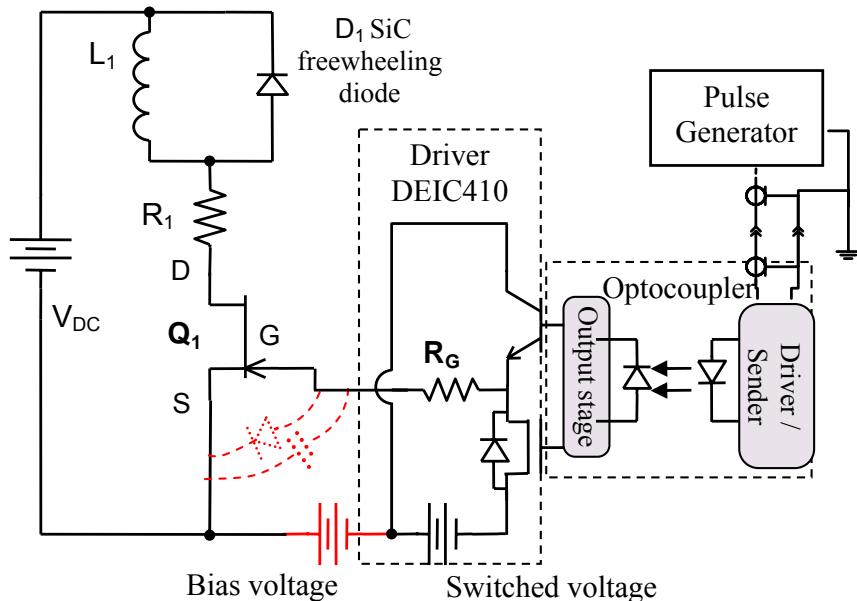
### **Short circuit and overcurrent protection**

Also the JFETs are rather robust against short circuit and showed self current limiting capability, it is recommended to include in gate driver a short-circuit protection, that turns OFF the JFET if the ON state voltage becomes too high.

### 6.3 Driving with negative voltage bias

While the JFET switch exhibits all the advantages of silicon carbide, it has the drawback that it is normally ON and requires a relatively high negative gate voltage to turn it OFF. This problem can be overcome by the use of the so-called “Cascode” configuration [92], where low-voltage silicon MOSFET is the primary driving circuit. The “Cascode” configuration, however, has the conventional silicon device in close proximity to the silicon carbide device and as such the Cascode configuration is limited to the same temperature constraints as conventional silicon. The application of the Cascode configuration is well documented in [92].

It is therefore very desirable to be able to drive the JFET directly, without the accompanying silicon MOSFET device. From a driving perspective the silicon carbide JFET can be considered similar to any other Si JFET. The equivalent circuit between the gate and source appears to be a diode junction orientated as shown in Figure 6-1



**Figure 6-1 Test setup with JFET gate junction diode and capacitance equivalent circuit**

This pn junction is normally never forward biased. With no bias on the pn junction, the main conduction channel is also normally unconstricted and exhibits a low resistance. In order to turn OFF the transistor, and close the channel by pinching it off, it is necessary to apply a negative bias to the pn junction between the gate and the source. For the different versions of the devices currently available, this pinch-off voltage varies between -23V and -40V. A complication arises due to the fact that at a voltage approximately 8V lower than the pinch-off voltage, the reverse biased pn junction will undergo breakdown and start to

rapidly conduct current. The reverse biased gate-source pn junction has a similar capacitive impedance characteristic as a conventional MOSFET. Turning the device ON and OFF requires charging and discharging this capacitance typically from zero to a voltage below the pinch-off voltage. This may be accomplished in a similar manner as for a conventional MOSFET and a typical drive circuit is shown conceptually in Figure 6-1. The only difference is a negative gate voltage with amplitude somewhat larger than that of a conventional MOSFET. A problem that arises is that due to the relatively high voltages involved, it is not possible to make use of conventionally available driver circuits that are low cost and well proven. In general a discrete solution for the final gate drive stage is necessary [84], [67]. This solution may be completely discrete in nature, or consist of a conventional driver circuit followed by a high voltage buffer.

Again it should be investigated the possibility of making use of some of the unique transfer characteristics of the JFET to ease the gate drive requirements. With no gate voltage applied, the drain-source channel exhibits a low conduction resistance. As a progressively larger negative gate voltage is applied, the channel starts to narrow until eventually blocking current totally. For a large portion of the range however the drain-source voltage is very low (the JFET is on) and therefore the internal electric field from drain to source is negligible. The channel remains in the linear region. This can be best illustrated in Figure 6-2, where the on-state drain-source voltage of the JFET is plotted as a function of the negative bias on the gate.

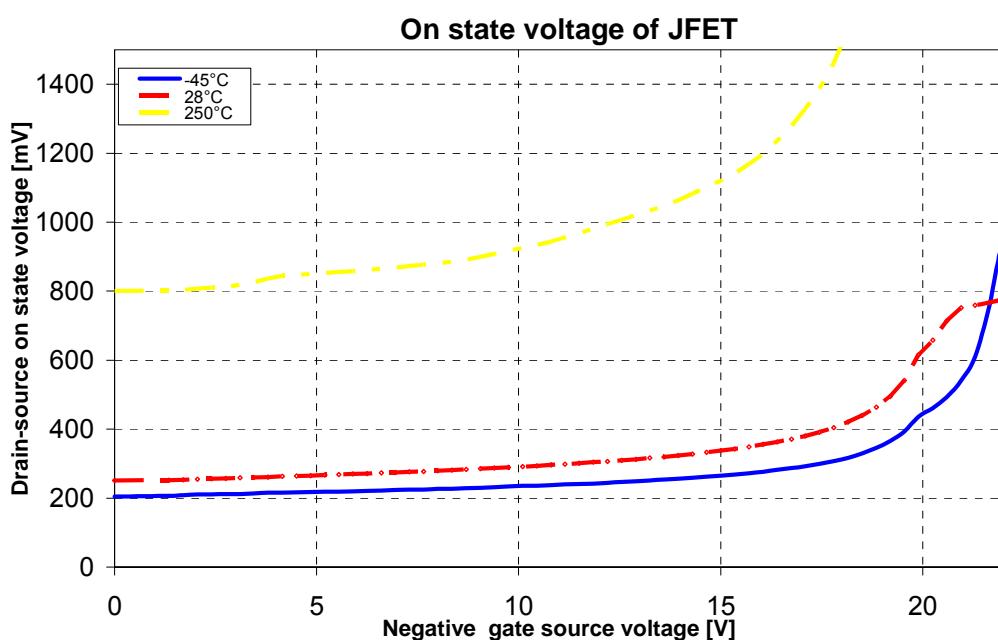


Figure 6-2 On state voltage of the JFET vs.  $V_{GS}$  @ constant drain current 4.8A

As can be seen from Figure 6-2, at gate voltages below app. 10V, the on state voltage of the device varies linearly as a function of the negative gate bias. It can be seen that the transistor remains on with a low conduction voltage even for a considerable negative drive voltage. As the gate voltage approaches the pinch-off voltage the resistance rises rapidly and the device turns OFF. It is this property of the device that is to be utilized to aid in the simplification of the gate drive. It is possible to place a constant negative bias on the gate of the JFET and then to pulse the gate negative past the pinch-off voltage to switch it OFF:  $V_{PinchOFF} = V_{bias} + V_{drive}$ . The excursion from the constant negative bias to a point past pinch off is not so large and can be accomplished with a conventional monolithic gate driver. If for example the pinch-OFF voltage for JFET is  $V_{pinchOFF} = 42V$  and the maximum driving voltage can reach  $V_{drive}=20V$ , then the  $V_{bias} = V_{pinchOFF} - V_{drive} = 42V - 20V = 22V$ . In this case any commercially available drivers can be used. Clearly if the pinch-off voltage of the JFET is changed, then only negative DC bias should be adjusted. Moreover because of the

much less voltage needed to charge the gate -  $P_{Gate} = \frac{C_{Gate} \cdot \Delta U_{Gate}^2}{2}$ , the overall gate power

can be reduced.

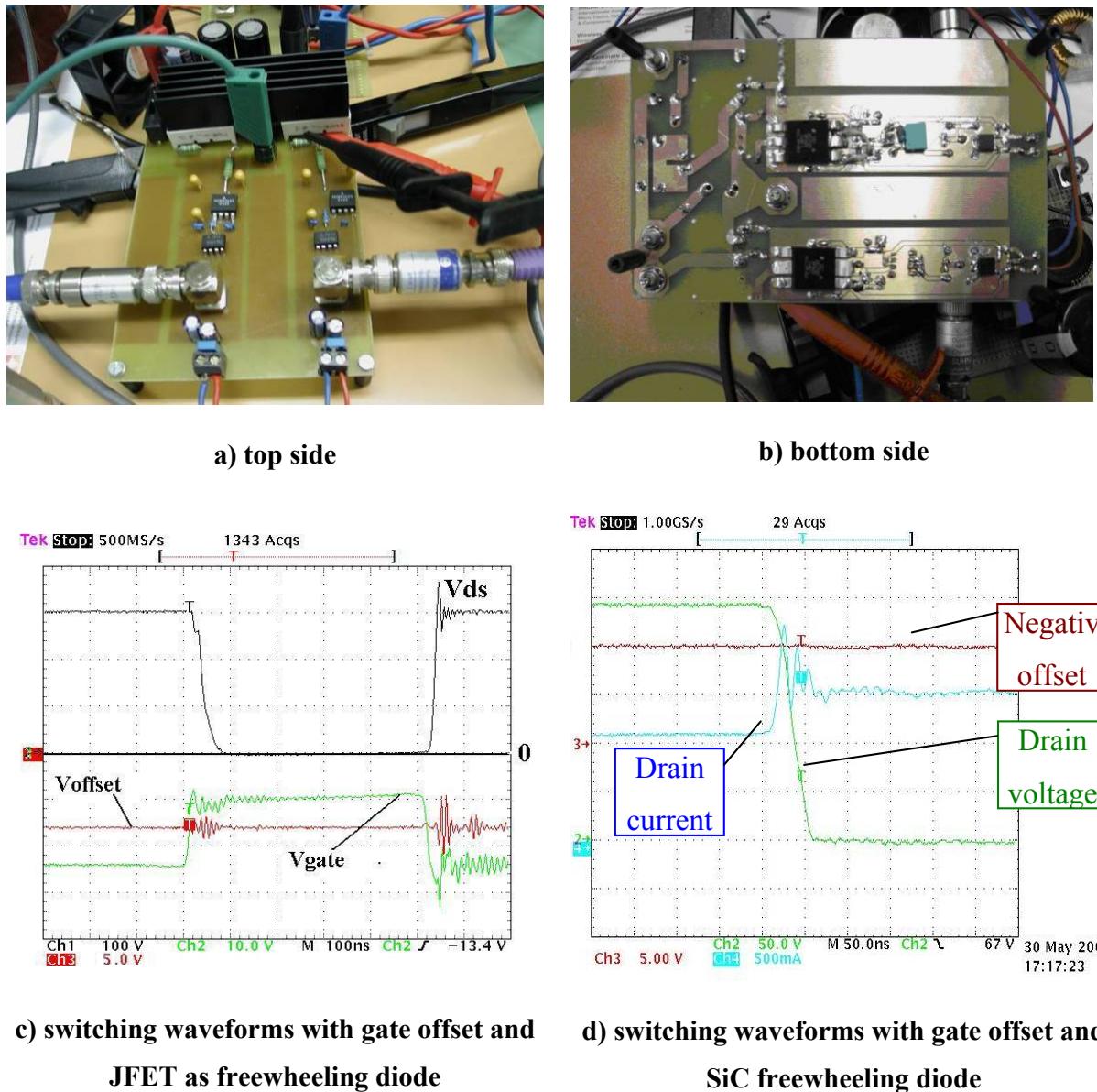
### Practical realization of the new gate driving circuit

The experimental results are obtained by using a low parasitic test circuit realized as a chopper Figure 6-1. The circuit is realized using the HCPL high-speed, high-voltage optocoupler together with IXYS gate driver DEIC420 and 1 Ohm gate resistance. The Silicon Carbide devices is the 3rd generation JFET Transistor with  $V_{PinchOFF} = 22V$  packaged in a Semitop™ package. It has 1200V Drain-Source blocking voltages and 5A Drain current capability.

The test circuit was operated at a nominal switching frequency of 200 kHz. Two cases are tested. The SiC Transistor and it's body diode as freewheeling diode and with SiC Schottky diode. The switching waveforms of the circuit are shown in Figure 6-3 c) d). The zero line of all three traces in the figure is the thick center line. The gate voltage is clearly being pulsed negative, however the more positive level of the gate signal is at approximately -9V.

As can be seen from switching waveforms the -9V gate voltage offset remains constant whereas the only addition - 13V driving voltage is used to switch the device OFF. In this case any commercially available drivers can be used.

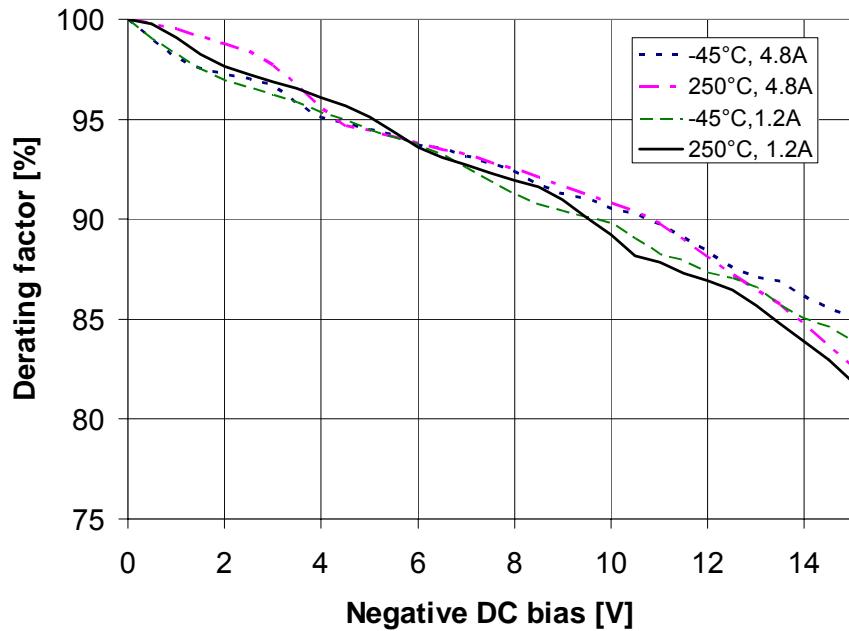
This leads immediately to the question of the effect of the constant gate bias on the conduction losses of the device. The on state voltage and therefore the conduction losses are increased by this driving method. However the device will switch faster and there are lower gate charge demands on the driver circuit.



**Figure 6-3 The test board switching waveforms with offset voltage on the gate**

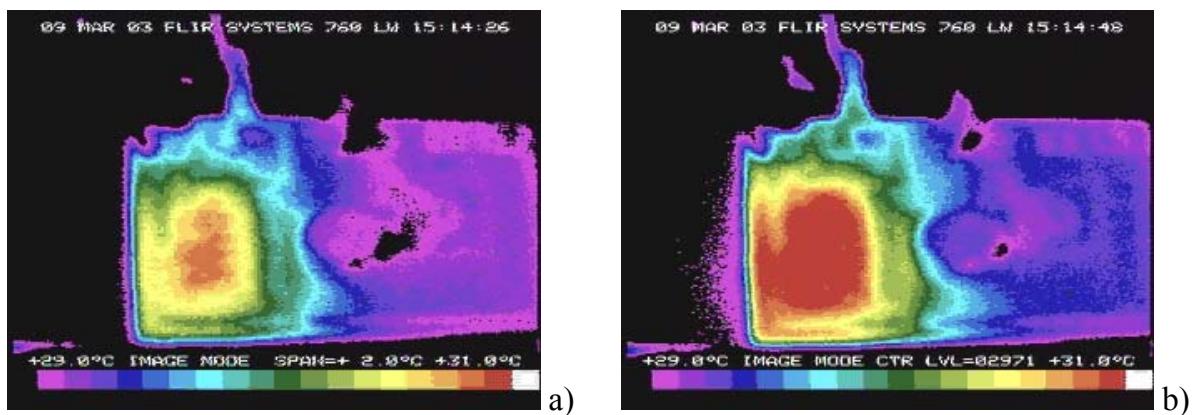
The reduction in performance of the JFET with this type of driving scheme needs to be controlled. A derating factor can be defined that will keep the losses in the device constant at the same level that exists when there is zero bias. In case of zero bias the whole pinch-OFF voltage should be supported by driver IC. This derating factor is shown in Figure 6-4 for constant negative DC bias voltages up to 15V. The derating factor is shown for both

high and low temperatures and high and low currents. It remains relatively constant at all these extremes. Derating of approximately 1% per volt of negative DC bias is required.



**Figure 6-4 Derating factor of the proposed driving scheme**

In order to further demonstrate the low additional losses that are introduced due to the constant negative bias, thermal images of open die devices were taken during switching conditions. These results are shown in Figure 6-5. Clearly the device on the left with a conventional full voltage swing on the gate has a smaller hot spot. However the maximum temperature of the two devices appears to be very closely matched. The new proposed gate drive does however lead to a larger hot spot due to a small increase in losses.



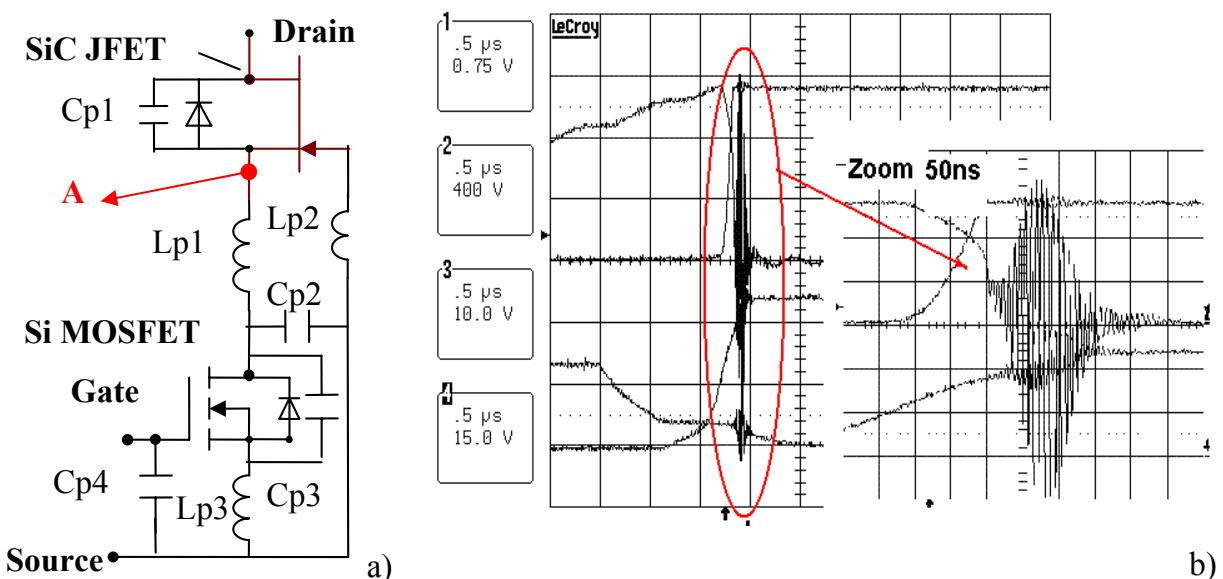
**Figure 6-5 Thermal image of the JFET die under switching conditions a) conventional, b) with offset on gate**

## 6.4 Driving JFETs in Cascode circuit

The driver circuit discussed before can be applied to any JFET for different pinch-off voltages. Applying an appropriate negative voltage is not a drawback, the problem is merely the conduction of the JFET when its gate voltage is zero. This can happen during start up or mains voltage slugs, etc., when the gate driver's auxiliary power supply can not maintain the necessary pinch-off voltage or when the voltage suddenly disappears. The “Baliga Pair” or Cascode circuitry, briefly discussed in Chapter 4.2.3 is a simple solution for this problem [56]. It can be applied for many high voltage, high power normally-ON devices in lower frequency range, where the switching speeds of the devices are moderate. Further investigations, however, have shown some limitations in Cascode circuit:

1. At higher switching frequencies, especially at higher switching voltage slew rates, significant parasitic oscillations can occur (Figure 6-6b provided by Reinmann [91]).

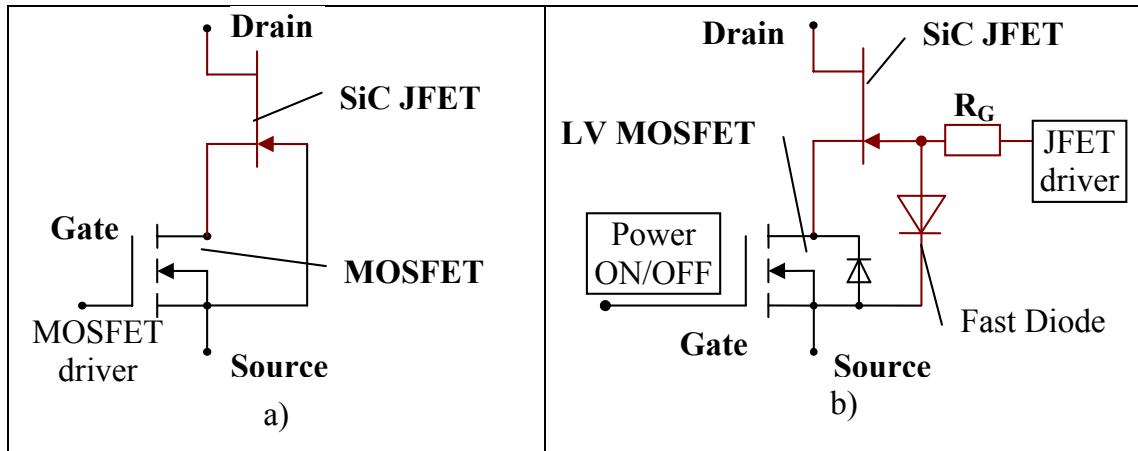
This can be explained as following: When the MOSFET is switched OFF the voltage on its drain rises quickly up to JFET's pinch-off level (Figure 6-6a Point A). At that moment the JFET switches OFF. Due to parasitic packaging inductances this voltage (Point A) does not remain constant, but continues to oscillate in series resonant circuit  $C_{p1}-L_{p1}-C_{p2}$ . The drain voltage of the MOSFET is directly applied to the gate, therefore the same oscillations will “see” the gate of the JFET and accordingly will modulate its channel.



**Figure 6-6 The SiC JFET in Cascode configuration with LV Si MOSFET, together with parasitics a) and oscillations caused during switching OFF process b) [91]**

During downswing of the voltage at point A, the negatively applied voltage to the gate can initiate positive feedback and consequently produce oscillations, which in some cases can

be destructive. Therefore it is desirable to slow down the switching process of the JFET. As it was mentioned previously, a rather high gate resistance compared to the MOSFETs is necessary to decrease the switching speed of the JFET. However in classical “Cascode” circuit the control is realized by means of MOSFET and not by the gate of the JFET.



**Figure 6-7 The classical Cascode circuit a) and modified Cascode b)**

2. It is obvious that inserting of the pre-resistance in series with the Gate of JFET will slow down it, but in this case the LV MOSFET will be drown to the avalanche with every switching cycle, which can cause tremendous energy losses and to possible destructive operation of the Cascode.
3. In order to reach the pinch-off voltage of the SiC JFET, the LV MOSFET Drain-Source breakdown voltage must be at least the JFET's pinch-off level. On the other hand, (when the switching speed of JFET is low) in order to prevent the JFET gate from secondary breakdown, this voltage shouldn't be too high. Regarding the narrow gap between JFET gate breakdown voltage and its pinch-off voltage, finding out such a MOSFET is very difficult, if not impossible

In proposed simple extension of the “Baliga Pair” the JFET can be controlled independently, while allowing normally OFF mode (Figure 6-7b). During normal operation the MOSFET is permanently switched ON, and has minimal influence on the switching behavior of the JFET. Additional diode decouples the LV MOSFET, during driving the JFET with negative polarity gate driver and with adjustable speed by means of controlled current or gate resistance. In case of sudden voltage slugs or losing power of control and/or driver circuit the LV MOSFET switches automatically OFF (normally OFF), only once – hence preventing the short circuit in accident cases. Exact level of the applied voltage to the Gate of the JFET can be adjusted with diodes connected in series.

## 7 Prototype of 1kW resonant reset converter

To give an experimental verification of the operating concepts and theoretical expectations, a prototype breadboard of SiC Resonance Reset Forward converter is realised, which provides 48V DC at 1 kW output power.

### 7.1 Design and dimensioning of the converter

#### 7.1.1 Power stage

The converter is designed according following specifications:

Parameter	Symbol	Value	Unit
Input voltage range	$V_{IN}$	380-430	V <sub>DC</sub>
Output voltage	$V_{OUT}$	48	V
Output voltage ripple	$\Delta V_{OUT}$	< 0.1 V <sub>OUT</sub>	V
Nominal output power	$P_{OUT}$	1000	W
Switching frequency – Variable	$f_{sw}$	200 - 300	kHz
Efficiency	$\eta$	>90	%

The input voltage range is selected according to the output specification of typical off-line, universal input, power factor correction boost converter; the switching frequency is selected arbitrary about 200 kHz. The exact values of the input and output voltages are not important with respect to verifying the principles of operation of the converter in this thesis. They can be adopted later on to the specific applications.

#### Voltages and currents of the active switch

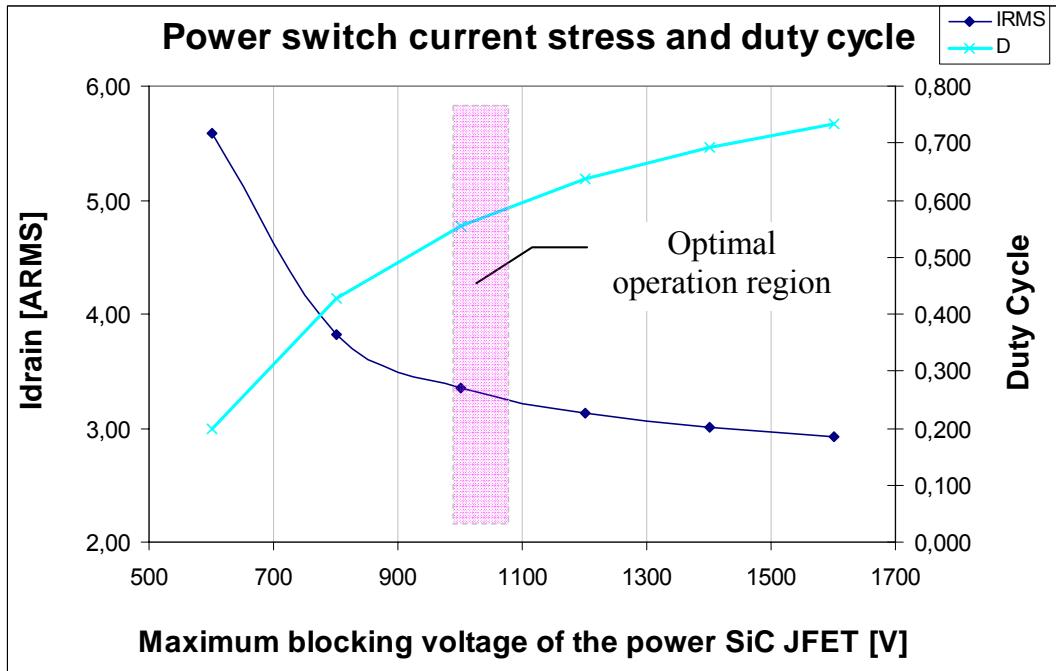
The current and voltage stresses of the active device can be found from the flux balance and energy balance equations of the converter. For initial calculation the resonant voltage swing on the transistors is approximated to the sinus waveform and allowed to rise up to 1600V. Afterwards, from the more detailed calculations (see Appendix [A2]), the influence of the parasitic components can be considered, and the real resonant peak voltages can be redefined. According energy balance, the optimal duty cycle and demagnetisation time can be determined – hence the drain overvoltage level can be found.

The magnetising current energy of the transformer is converted to the voltage potential of the resonant capacitor:

$$\frac{1}{2}L\mu \cdot I\mu^2 = \frac{1}{2} \cdot C_{RES} \cdot V_{RES}^2 \Rightarrow V_{RES} = \sqrt{\frac{L\mu \cdot I\mu^2}{C_{RES}}} - \text{therefore the resonant time is estimated as: } (7-1)$$

$$t_r = \left| \frac{\arcsin\left(-\frac{V_{LK}}{V_{RES}}\right)}{\omega} \right| + \pi, \text{ where } V_{LK} = \sqrt{\frac{L_{LK} \cdot I^2_{out}}{C_{RES}}} \quad (7-2)$$

From equation (7-2) we can estimate allowable reset times by constant ON time for different drain overvoltage levels hence for different  $V_{RES}$ . As we can see the higher the voltage that the transistor can withstand, the shorter reset times can be – also larger duty cycles can be allowed. From the RMS current definition for forward topology  $\frac{P_{OUT}}{U_{IN} \cdot \sqrt{D}}$  (see Appendix A1), the RMS current will be lowered too and for given specifications it varies from 5.59A to 2.92 A. For  $V_{RES}$  500V- to 1500V the reset time varies from 4us to 1.33us. The results of the calculations are graphically illustrated in the Figure 7-1.



**Figure 7-1 The optimal operating area according with RMS current and duty cycle dependencies from the maximum demagnetizing voltage applied to the transformer primary**

From the above given curves we can see, that the optimal design point with significant RMS current reduction is located at duty cycle 0.52-0.6. And the drain overvoltage for given specification will reach about 1000-1100V. Important to note, that these initial

estimations consider only rectangular waveform of the reset voltage, without taking into account any parasitic effects.

With today's available 1500V, 5A JFET in Cascode combination and with total device resistance of 380mOhm @ 25°C, the ON state losses can be directly estimated from the drain RMS current:  $P_{ON} = I_D^2 * R_{ON} = 3.65 \dots 4.13 \text{W}$ . The power losses on the secondary side

diodes will be  $\frac{P_{OUT}}{U_{OUT}} \cdot V_F = \frac{1000 \text{W}}{48 \text{V}} \cdot 1.5 \text{V} = 31.2 \text{W}$ . These DC losses are rather high

because of higher forward voltage drop of SiC diodes, however the switching losses in the primary switch are minimised, which is noticeable especially at higher frequencies.

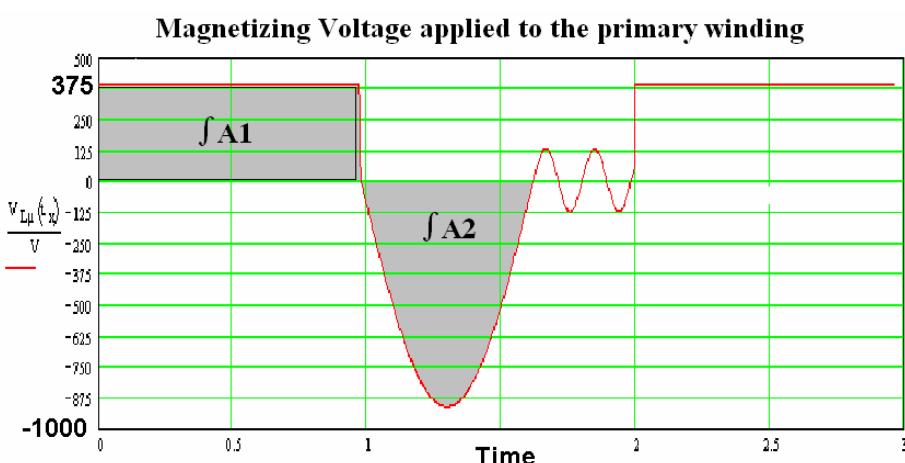
### Power transformer design

From the selected duty cycle range and with consideration of possible minimum input voltage, the power transformer winding ratio can be selected.

$$n = \frac{U_{IN}^{\min}}{U_{OUT}^{\max} + V_F} \cdot D \Rightarrow n = \frac{380 \text{V}}{48 \text{V} + 1.5 \text{V}} \cdot (0.52 \dots 0.6) = 3.96 \dots 4.62; \quad (7-3)$$

The transformation coefficient  $\bar{U}$  is therefore the mean value:  $\rightarrow \frac{3.96 + 4.57}{2} = 4.29$

The power transformer in this converter design is the most important part, which defines the main switching parameters and can have an influence on the overall converter performance. Because the transformer is demagnetized with a much higher reverse voltage than the magnetising DC bus (400V), the time needed for demagnetisation is much shorter than for magnetization. Reason for this is the needed flux balance – the equality of



**Figure 7-2 The volt-second balance of the transformer. The area A under magnetizing and demagnetizing voltages must be equal**

positive and negative volt-seconds on the transformer (see Figure 7-2). Therefore it is important to find a suitable transformer layout which allows the elimination of the demagnetization branch without saturation and allows secure operation of the converter without destruction of the power switch due to very high overvoltages.

**1.** For the prototype board the ETD transformer core will be selected. For the given switching frequency 200 kHz, the power transfer of the ETD39 transformer with N87 core material is equal to 1480W by 213mT Flux and 3.9A/mm<sup>2</sup> current density. For the first calculation therefore this core will be selected.

**2.** The number of turns for primary winding is given by:

$$\omega_1 = \frac{U_{IN} \cdot \Delta t}{B_{max}^{Fe} \cdot A_{min}^{Fe}}, \text{ where} \quad (7-4)$$

$U_{IN}$  – Peak voltage on the primary;  $T$  – The maximum time during which the voltage is applied to the primary winding;  $B_{max}$  – Maximum flux density in the ferrite core;

$A_{min}$  – is the minimum cross-section area of the transformer core. From (7-4) the primary winding turns can be estimated  $\omega_1 = \frac{400 \cdot 3.46us}{300mT \cdot 125mm^2} = 36.9 \cong 37$  windings, consequently for secondary winding  $w_2 = 37/n = 9, 2$  windings.

**3.** Calculation of the core losses involves the optimisation of the windings and core materials. To do this a transformer calculation tool based on [64] is used. The high number of turns reduces the magnetic flux density; however the winding resistance and therefore the losses are increasing. The optimisation steps are presented in [F1]

**4.** Minimisation of power losses in the windings consists of optimisation of the windings type their geometrical arrangements. The optimum winding selection procedure is also carried out with transformer calculation tool [F1]

**5.** The last check is the temperature rise, which should be limited to the given range. If the over temperature is unacceptably high, another core should be selected and the optimisation procedure should be repeated.

The resulting transformer design consists of the following:

Core: EPCOS ETD 44/ N87; Transformation coefficient 4.29

Primary winding: 30 turns of copper foil 21.5mm x 50μ

Secondary winding: 7 turn of 2 paralleled sheets of copper foil 21.5mm x 100μ.

Winding pattern: 8-7-14-7-8 (4x interleaved).

Magnetizing inductance: 3150 uH without air gap; Secondary inductance 171.5 uH

## Input and output filter design

Concerning the technical specifications and taking in account that DC-DC conversion usually follows after PFC stage, it is important to guarantee a minimum hold-up time 15ms. The required storage capacitance in case of mains fadeout is estimated from:

$$W = \frac{1}{2} \cdot C \cdot U^2 = P_{OUT} \cdot t_{Holdup} \quad (7-5)$$

Allowable minimum DC bus voltage:

$$U_{min} = 48 \cdot n \cdot \frac{1}{D_{max}} = 329V \quad (7-6)$$

And the resulting necessary capacitance is:

$$C_{in}^{DC} \geq \frac{2 \cdot P \cdot t_{Holdup}}{U_{IN}^2 - U_{min}^2} = 580\mu F \quad (7-7)$$

Two parallel connected capacitors (e.g. EPCOS 450V/ 330uF) are used.

The output LC filter is calculated with taking in account that the output voltage depends only on the duty cycle and the input voltage, - it is load independent (see Chapter 2.2). The inductor current  $I_L$  has a triangular shape and its average value is determined by the load:

$$\Delta I_L = \frac{1}{L_{out}} (U_{IN} \cdot n - U_{OUT}) \cdot \left( \frac{U_{OUT}}{U_{IN} \cdot n} \right) \frac{1}{f_{sw}}, \quad (7-8)$$

$$\text{and } I_{max} = I_{OUT} + \frac{1}{2} \Delta I_L$$

Allowing the output current ripple 40% of the load the maximum peak current is  $I_{max} \approx 1.4 \frac{P}{U_{OUT}} = 29A$ . Using the above described calculation and optimisation

procedure the filter inductance  $L_{OUT} = 29.2\mu H$ , is made on core KoolM $\mu$  Typ77259-A7 and 17 windings with 2x1.5mm diameter.

For choosing the output filter capacitor first the H(s) response of the low pass LC filter should be studied. It extracts the DC component of the modulated output voltage:

$\tilde{U}_{OUT}(t) = D \cdot U_{IN} + \tilde{U}'(t)$ , where  $\tilde{U}'(t)$  is the periodic waveform which contains only the fundamental and harmonics of  $\tilde{U}_{OUT}(t)$ . Since the output ripple voltage is given by the high-frequency response of transfer function H(s) to  $\tilde{U}'(t)$ , we can approximate H(s) as:

$H(s) \approx \omega_0^2 / s^2$ . This corresponds to following double integration:  $\tilde{U}_r(t) \approx \omega_0^2 \int \tilde{U}'(t) dt$

It can be shown that the peak-to-peak output voltage ripple is equal to

$$U_r^{p-p} = U_{OUT}^{DC} \cdot \frac{\pi^2}{2} (1-D) \cdot \left( \frac{f_0}{F_{sw}} \right)^2$$

By closed feedback the worse case normalised ripple  $\delta_r$  occurs at  $D_{min}$  so that

$$\delta_r = \frac{\pi^2}{1} (1-D_{min}) \cdot \left( \frac{f_0}{F_{sw}} \right)^2$$

Hence, the LC filter is designed with a resonant frequency  $f_0$  given by:

$$f_0 = \frac{F_{sw}}{\pi} \sqrt{\frac{2 \cdot \delta_r}{1 - D_{min}}}, \text{ and}$$

For the design specifications  $\delta_r = 100mV$ ,  $D_{min}=0,2$  and design parameter switching frequency 200kHz, the resulting corner frequency is 4,6 kHz. The corresponding filter capacitor value is 4,08e-5F (nearest available capacitor 40uF can be selected).

### 7.1.2 JFET gate driver for high temperature operation

The first generation SiC JFETs have relative high negative pinch-off voltage and their levels varied from sample to sample. Therefore the gate drivers should be redesigned or adjusted for every device individually. Moreover, due to Si MOSFET, the Cascode circuit is not applicable for high temperature operation. The discrete gate driver developed at ETH Zurich Figure 7-3 [84] is free from mentioned limitations, and therefore adopted for our high temperature tests. In this driver concept the output voltage is intentionally selected very high, and the gate of the JFET will be driven in avalanche during every switch-OFF process. In this case, the necessary pinch-off voltage will be covered for every chip variations. For increasing the switching speed, the driver provides high peak pulse

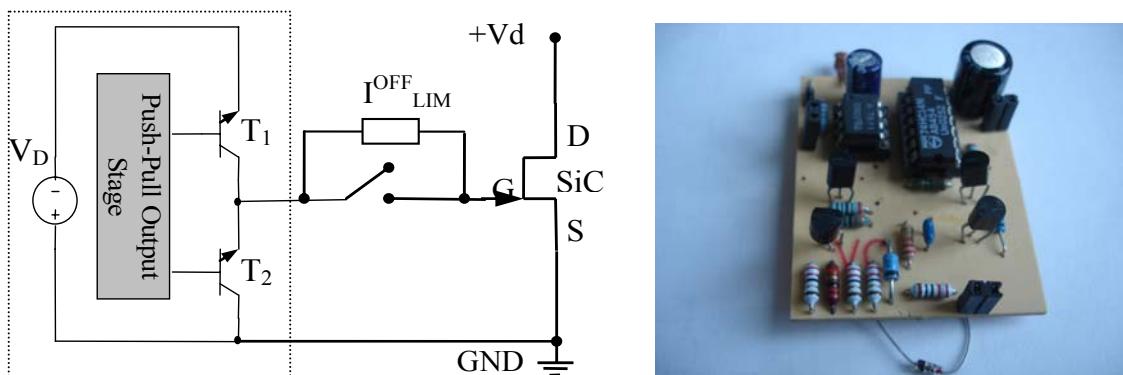
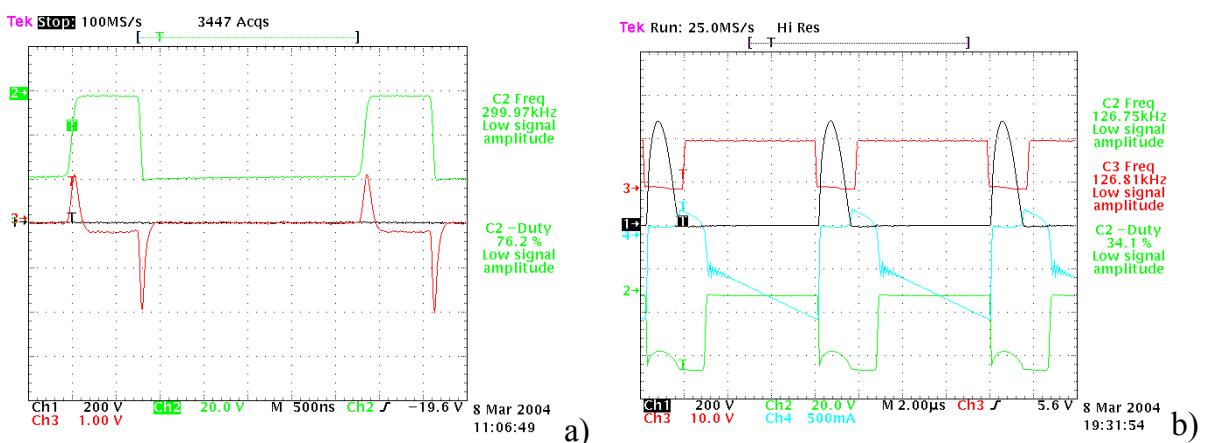


Figure 7-3 Principal diagram of the avalanche gate driver

currents at the beginning and limits it by additional high resistive gate network during OFF-state, in order to prevent the gate (reverse biased diode) from avalanche breakdown (see Figure 7-4 a; current scale 1V=200mA). In our realization it was possible to operate the JFET at app. 170 kHz regardless of actual pinch-off voltage and operation temperature. It can be seen from Figure 7-4 b), that due to rather high resistive gate path, the gate voltage (Green) can be affected by the drain voltage change through drain to source capacitance. In our case during the switch-OFF time, the gate voltage decreases from -40V to -35V, but the transistor remains in OFF state. Because of different avalanche currents flowing into gate, the parallel driving of many chips will be difficult. As it was presented in Chapter 4.4, the amount of gate current increase in one chip can be much higher then in other one. This avalanche breakdown property is technologically difficult to control in production, therefore avalanche driving can cause excessive power losses in high current applications, where many parallel connected chips are required.

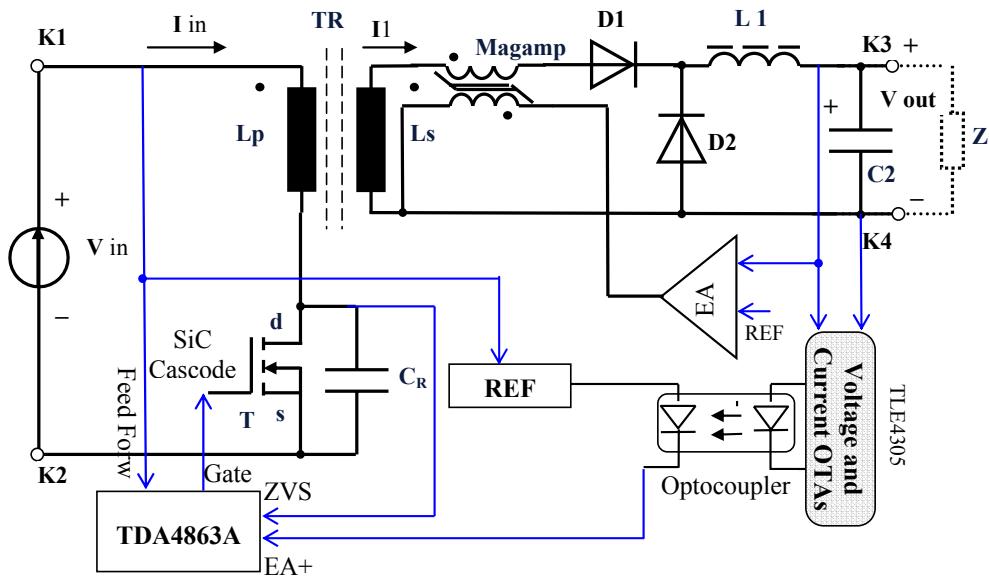


**Figure 7-4 Gate driver pulsed currents a) and switching waveforms resonant reset converter with implemented gate driver**

### 7.1.3 Saturable reactor and magnetic amplifier post-regulator

As it was discussed in Chapter 5.2.5, the saturable reactor is to be used in order to ensure ZVS operation of the converter over the wide input voltage and load range. In this chapter the saturable reactor will be implemented both for obtaining ZVS operation of the converter and for post-regulation purposes. Such postregulators (also known as magnetic amplifier or magamps) allow additional fine tuning and enable output voltage tight regulation because of a local feedback around the secondary side output. In this case multiple outputs can be obtained with less effort on the main output filter. It is well known that higher switching frequency (above 200 kHz) will cause excessive power dissipation

in the square-loop core of Magamp (see Chapter 2.3.2). Nevertheless, if the input voltage range is relatively narrow, the use of saturable reactor in medium to high power applications can be well suited, if the ways out to minimise the core losses can be found. Therefore tradeoffs between maximum used frequency and magamp losses should be considered. The general converter schematic with secondary-side magamp and control circuitry is shown below in Figure 7-5. The magamp is placed in series directly with secondary winding and physically arranged to be between transformer secondary and rectifier diode.



**Figure 7-5 The schematic diagram of the resonant reset forward converter, with secondary side magamp postregulator.**

The amplifier is driven by control loop and provides necessary voltage to magamp, which varies the blocking time in order to maintain output voltage regulation. Magamp reset current flows through output rectifier's parasitic capacitance and transformer secondary (not shown in Figure 7-5). As explained previously, the magamp core reset occurs during the OFF time, when the power transformer is also reset by resonant circuit. Generally, the magamp loss depends on the time required for blocking the secondary voltage – hence on regulation depth of the output voltage. However for only ZVS realisation, very small amount of blocking time needed. Regarding the high secondary current, the maximum number of primary turns is selected to be one in order to keep the core volume as small as possible. Additionally, to keep the magamp losses low, the output voltage is adjusted mainly from primary side by PWM, whereas only slight, postregulation is left for magamp. The maximum blocking time available from the core, is given by:

$$T_{bl} = \frac{N \cdot A_e \cdot (B_{SAT} - B_{RST})}{V_{bl}}, \quad (7-9)$$

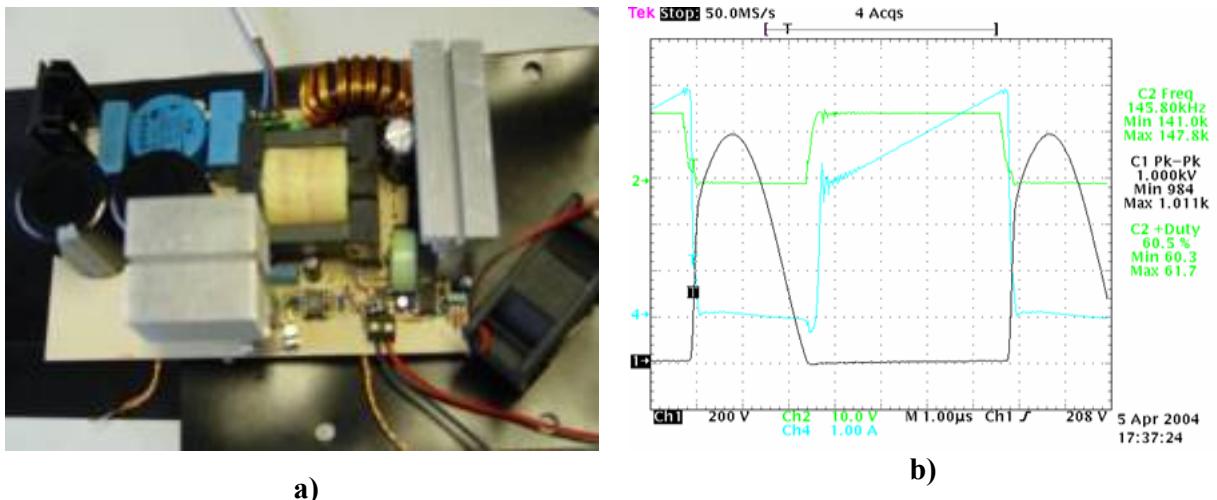
where  $A_e$  is the core cross-section and the  $B$  is flux density at forward and reset times respectively. Obviously, the maximum blocking time occurs at high-line, light load and is about 400ns in this application. Here also the maximum core loss takes place.

The magamp design implemented in the 1 kW breadboard is:

Core: Allied Signal METGLAS RM6 ring choke; Primary winding: 1 turns of Litz wire;  
Maximum core loss can be estimated from [106]:

$$P_{core} = 9.93 \cdot 10^{-6} \cdot F_S^{1.57} \cdot \left( \frac{B_{SAT} - B_{reset}}{2} \right)^{1.70} = 9.93 \cdot 10^{-6} \cdot 200^{1.57} \cdot \left( \frac{0.5 - 0.35}{2} \right)^{1.70} \approx 25.53 \left[ \frac{W}{kg} \right], \quad 7-10$$

where  $B$  is in Tesla and the switching frequency  $F_S$  is in Hz. The total loss of saturable reactor at 200 kHz and with minimum blocking time is about 1.2 W. The breadboard of the resonant reset power converter and its switching waveform are depicted in Figure 7-6.

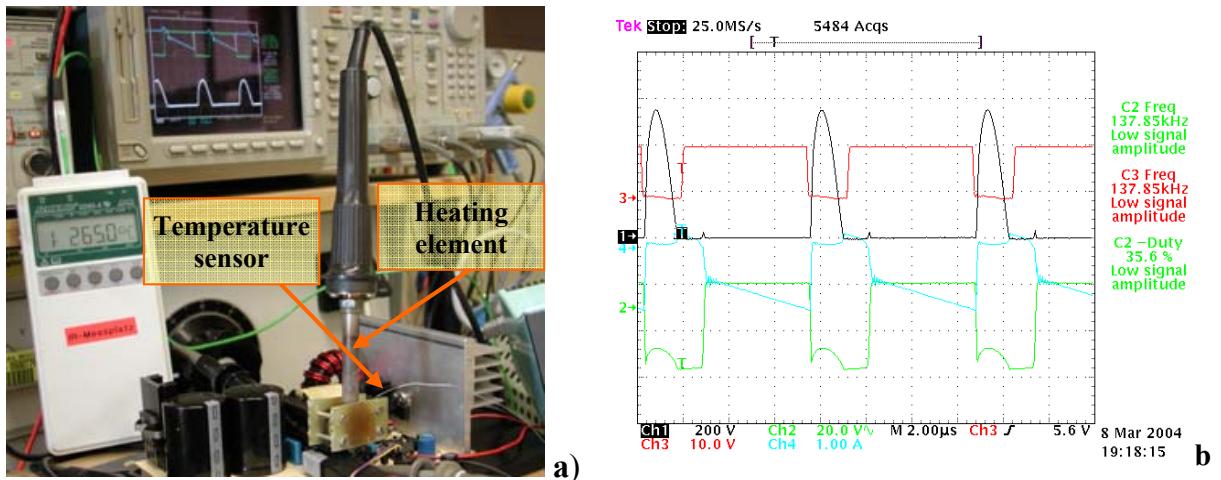


**Figure 7-6 a)** The prototype board of the 1kW Resonant Reset Forward Converter.  
**b)** Operation waveforms under ZVS condition. The drain voltage (black) is falling down to zero and then the gate signal (green) switches the transistor ON. The trapezoidal drain current (blue) has practically no spikes.

The board consists of the input filter with current compensated inductors, the power transformer, the SiC JFET Cascode as power switch and the secondary side forward rectification circuitry. Resonant circuit includes the output capacitance of the power switch and primary inductance of the transformer 640uH. Parallel to the switch additional 600pF x 2000V resonance capacitor is connected. The resonance polypropylene capacitor should be of high quality e.g. EPCOS MFP B32632, in order to process the high frequency high slew rate voltages. Overall resonant capacitance of the converter is app.

800pF which includes the parasitic capacitance of the transformer windings and secondary side diodes. As rectifier and freewheeling diodes two paralleled SiC SDP10S30 diodes 300V/12A are selected. The power switch is SiC JFET [40]. For controlling and primary regulation the output voltage, as well as for catching the minimum voltage the DCM PFC free running controller IC-TDA4863G is used. The saturation reactor is constructed on the small ring ferrite B64290-L38 with 15uH overall inductance, - value was arrived experimentally. The complete schematic circuit is attached in [G1]. From Figure 7-6 we can see that switching of the SiC JFET is taking place under zero drain voltage, which causes remarkably low ripple on the drain current.

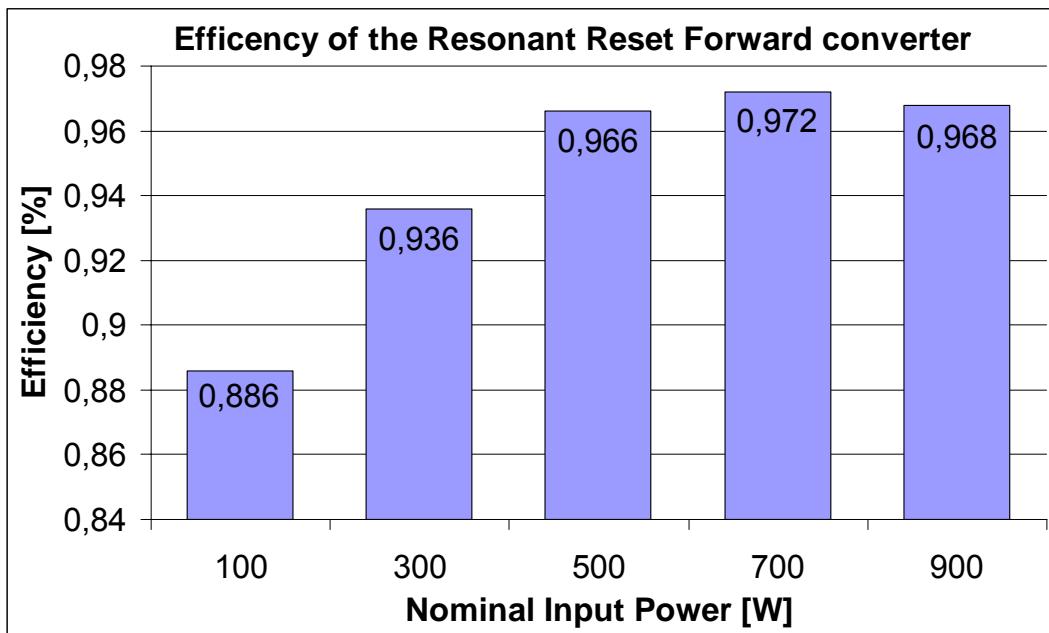
Finally, the converter operation was tested under high ambient temperature. The heatsink of the SiC JFET was replaced by heating element (the soldering bulb). Because of rather high junction temperatures the JFET was driven directly without Si MOSFET. The gate driver circuit purposed by [67] and explained in Chapter 7.1.2 is used.



**Figure 7-7. a)** Operation of the prototype converter under 260°C ambient temperature and **b)** switching waveforms: black - Drain voltage; blue – input current; green – gate signal

## 7.2 Efficiency

The obtained efficiency of the prototype converter for different input voltage levels is given below in Figure 7-8.

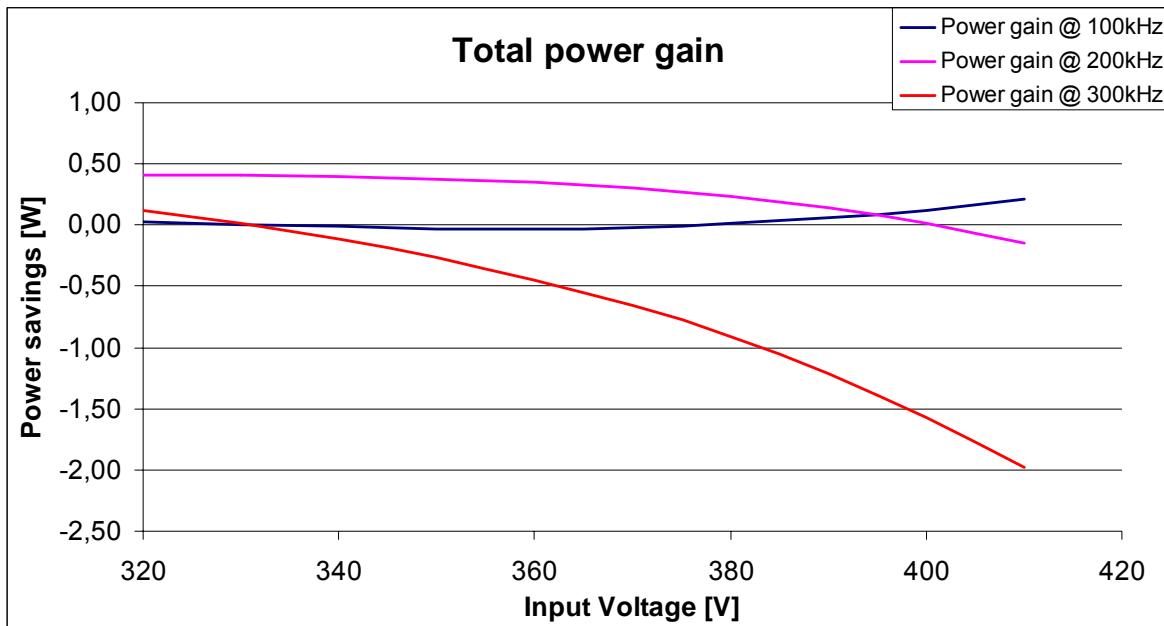


**Figure 7-8 Measured efficiency at 400V input and 48V output voltages**

The efficiency measurement results can be summarized as following:

- ✓ The most losses take place on the secondary side (over 70%), where SiC Diodes are used. Only at higher frequencies (over 200 kHz) the real advantage of the SiC rectifiers becomes evident.
- ✓ The over 0.5 duty cycle allows reduction of the RMS current to 4-5 Arms in the switch which results to app. 8-11W losses at  $520\text{m}\Omega @ 80^\circ\text{C}$
- ✓ Due to high switching speed (slew rates), the switching losses are minimized even at hard switching cases. Important to note that the optimal selection of the JFET's pinch-off voltage can have big influence on the efficiency.

As we can see the maximum efficiency is obtainable at 700W, - the reason is the relative high on state losses of the rectification diodes. Due to SiC the Schottky diodes have 1.5V forward voltage drop, which at 1000W and 48V output voltage causes over 31W power losses.



**Figure 7-9 Power loss savings vs, Input voltage by using saturable reactor at different switching frequencies.**

Figure 7-9 illustrates a comparison between the power dissipation savings incurred due to ZVS of the SiC JFET versus the core loss introduced by the saturable reactor used to realize the ZVS mechanism.

The output current is selected equal to 10A and used as the point of comparison. The induction level ( $\Delta B$ ) was held constant for the 100 kHz, 200kHz and 300kHz switching frequencies. It can be seen a positive net gain even until the switching frequency is increased up to 300 kHz. Behind this frequency the saturable reactor core loss will dominate.

However, at 200 kHz and at higher line voltages a significant reduction of power dissipation in power switch can be obtained by shifting the loss into saturable reactor. This is a desirable effect from thermal management and reliability point of view.

We can see that at low frequency range the DC losses are dominant and at higher current levels have more influence on the efficiency. By increasing the input voltage level current and therefore the DC losses too are decreasing. From Figure 7-9 it is also visible that the minimizing the volt-seconds the saturable reactor have to block, will decrease the core losses. Therefore is desirable to minimize the input voltage variation, which is the case if a PFC stage is preceded to the DC/DC conversion

## 8 Conclusion and future work

### 8.1 Summary

This thesis has combined two challenging technologies of power electronics in one solution: - from one hand the power semiconductor devices and from other hand the development of power converters.

The power semiconductor industry is moving towards wide-band-gap technology providing inherently high temperature, high voltage and high frequency capable devices. Power converters, imposed by high efficiency, high power density as well as by marketing demands are moving towards integrated, modulised and standardized systems.

The main aspects covered in this thesis can be summarized as following:

1. The properties of SiC semiconductor are presented and the VJFET power device based on SiC is investigated towards its optimal implementation into target power converter:
  - ✓ SiC has higher breakdown electrical field (eight times more than Si). This permits much smaller power device structures (drift regions). Short drift regions allow manufacturing SiC devices with very low drain-source resistance  $R_{DS(ON)}$  compared to Si devices. Implementation of the latest SiC high voltage JFET with less than  $400\text{m}\Omega R_{ON}$  and  $1500\text{V}_{DS} (\leq 12 \text{ m}\Omega\text{cm}^2 @ 1500\text{V})$  leads to reduced ON-state losses of the DC/DC converter (below  $35\text{W} @ 1\text{kW}$ ). Whereas the power switch losses are only 15W.
  - ✓ Higher thermal conductivity (three times more than Si) permits better heat dissipation and allows better cooling and temperature management. By optimal usage of high temperature gradient from the module to the environment, the power converter volume can be minimized and mechanical cooling fans can be eliminated.
  - ✓ Higher band-gap (three times more than by Si) enables higher junction temperatures and allows increasing current density through the SiC device. Realized resonant reset converter has shown high junction temperature operation capability of the device (over  $260 ^\circ\text{C}$ ), and possibility to replace several Si switches by single SiC switch. Suggested simplification approach can be considered as the first step towards integrated power electronics modules.
  - ✓ High saturated electron drift velocity (two times than Si) combined with very small die size (20 times smaller than correspondingly rated silicon-based devices) enables

✓ fabrication of ultrafast switching devices. SiC JFETs show very “light” gate driving possibility (less than 300pF @ 0-20V) and very high switching ON and OFF voltage slew rates (can reach 60kV/us). Implementation of the SiC JFET into adopted power converter reduces switching losses even in hard switching conditions. Overall switching losses are about 30W at full load and 200 kHz switching frequency.

2. A concept for utilizing the specific properties of the SiC devices has been found.

✓ It was shown that full utilization of superior features of SiC devices is possible if the target converter is explicitly designed for it. Simple replacement of the Si power switches by SiC counterpart will not bring expected advantages. Only system level optimization and comparison is relevant.

✓ From the wide choice of power converter topologies the resonant reset converter is selected as the most suitable one. From topological point of view it is the most simple and is free from known drawbacks of multi-switch topologies. Highest possible drain voltage for fast demagnetization of the transformer as well as for duty cycle increase and high switching frequency for minimization of required resonant capacitance are the specific requirement of this topology. The power switching devices to be implemented in the mentioned topology must have following properties: high switching frequency (app. 200 kHz), high breakdown voltage (over 1500V), high switching voltage slew rates (over 20kV/us) and high operation temperature (over 250 °C). The combination of these properties leads to the power switching device, which can be realized only in SiC.

3. Two new approaches for driving SiC JFETs:- the “constant DC bias” and “Cascode extension” are proposed for future integration into power modules and for high temperature and high frequency operation of the adopted power converter.

4. Prototype resonant reset converter board with implemented SiC VJFET and SiC rectifiers is designed and built for experimental verification. The all SiC DC/DC converter shows following improvements versus Si counterpart.

- ✓ Increase of power capability from 50..100W up to 1kW (ten times)
- ✓ Elimination of snubbers, demagnetization circuits and duty cycle extension (80% less components and complexity)
- ✓ Increase of switching frequency and obtaining zero voltage operation (ZVS)

## 8.2 Suggestions for future work

- ✓ The analysis of the high voltage operation is done under normal environmental conditions. The influence of the high temperature on the breakdown voltage and reliability of the overall converter should be studied further in details.
- ✓ Influence of the high voltage peaks not only on the SiC active devices but also on the power transformer should be analyzed. The high slew rate voltage applied on the transformer can drastically accelerate the isolation aging and reduce its reliability. Detailed analysis and possible implementation of planar transformers is a subject for further work.
- ✓ The high frequency operation of SiC JFET (over 300 kHz) was not fully utilized, because of absence of simple high frequency free running controller IC. It would be advantageous to push the switching frequency higher and observe the limiting factors of other (e.g. passive) components.
- ✓ If the normally-OFF and high temperature operation is mandatory, more sophisticated solution for gate driving circuitry should be found.
- ✓ The Silicon Carbide technology is in its infancy, and maximum voltage boundaries of the switching devices are open. The maximum drain voltage level of the converter, discussed in this thesis, is arbitrary not limited. Therefore any other novel topological solution for utilizing the unique properties of SiC devices while maintaining controllable or clamped voltage operation is a future research area.

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# Appendix

## A1 Derivation of the main characteristics for single switch Forward and Flyback converters

Derivation of the operation characteristics under following assumptions:

1. Input voltage source has zero internal resistance (ideal voltage source)
2. Switching time (rise and fall times) of the switches are neglected
3. ESR of the filter capacitances are equal to zero
4. Output voltage ripple is negligibly small compared to the average output voltage level
5. All switches are ideal

Main equations:

Volt-second integral on the winding of any inductor is equal to zero:

$$U_{ON}^L \cdot D \cdot T = U_{OFF}^L \cdot (1 - D) \cdot T \quad (9-1)$$

Amper-second integral on any capacitor is equal to zero:

$$I_{ON}^L \cdot D \cdot T = I_{OFF}^L \cdot (1 - D) \cdot T \quad (9-2)$$

Average current consumption of the converter from the source is:

$$I_{IN} = I_{ON} \cdot D + I_{OFF} \cdot (1 - D) \quad (9-3)$$

The average voltage on the load after LC filter is given:

$$U_{LOAD} = n_{ON} \cdot U_{ON} \cdot D + n_{OFF} \cdot U_{OFF} \cdot (1 - D) \quad (9-4)$$

, where  $n_{ON}, n_{OFF}$  are transformation coefficients and  $U_{ON}, U_{OFF}$  are voltages on the primary winding during switch ON and OFF time respectively. During the same time intervals the current through switch is changing according following:

$$i_{ON}(t) = I_{MIN} + \frac{U_{IN} - U'_{Load}}{L} t, \quad if \quad 0 \leq t \leq t_{ON} = D \cdot T \quad (9-5)$$

$$i_{OFF}(t) = I_{MAX} - \frac{U'_{Load}}{L} t, \quad if \quad 0 \leq t \leq t_{OFF} = (1-D) \cdot T$$

Taking into account that:  $i_{ON}(T_{ON}) = I_{MAX}$  and  $i_{OFF}(T_{OFF}) = I_{MIN}$ ,

and  $t_{ON} + t_{OFF} = T = 1/f$  from (9-56) we can find the regulation characteristics of the forward converter in CCM mode:

$$U_{Load} = D \cdot U_{IN}$$

The minimal and maximal currents through the switches can be found from the equation of energy balance:

$$U_{Load} \cdot I_{Load} \cdot T = \int_0^{T_{ON}} U_{IN} \cdot i_{ON}(t) dt, \quad (9-6)$$

Therefore

$$I_{MIN}^{MAX} = I_{Load} \mp \frac{D \cdot (U_{IN} - U_{Load})}{2 \cdot L_f \cdot f_{sw}} \quad (9-7)$$

From the (9-6) it is possible to find out the average current through the filter inductance:

$$I_L = (I_{MIN} + I_{MAX}) / 2 = I_{Load}$$

Average current through the power switch and freewheeling diode recalculated to the primary side can be found through the following relations:

$$I_{ave}^{Tr} = \frac{1}{T} \int_0^{T_{ON}} i_{ON}(t) dt = I_{Load} \cdot D \quad (9-8)$$

$$I_{ave}^{D_{FW}} = \frac{1}{T} \int_0^{T_{OFF}} i_{OFF}(t) dt = I_{Load} \cdot (1 - D)$$

The power rating of the switch  $P_{SW} = U_{SW} I_{SW}$  related to the output load power is given by

$$P_{SW} = \frac{P_{Load}}{D} \quad (9-9)$$

From the (9-9) follows the better power switch utilization is taking place if the  $D \rightarrow 1$   
(it is assumed that current ripple in the Inductor is negligible compared to the DC current)

To find out the voltage ripple on the output, the amount of charge through the filter capacitor should be determined. The current through the  $C_f$  is equal to  $I_{Cf} = I_{Load}(t) - I_{DC}$ .

$$\Delta Q = \frac{1}{2} \frac{(U_{IN} - U'_{Load}) \cdot T_{ON}}{2 \cdot L} \left( \frac{T_{ON}}{2} + \frac{T_{OFF}}{2} \right) \quad (9-10)$$

Given that  $\Delta Q = C_F \cdot \Delta U_C^{pk-pk}$ , we can obtain the output voltage ripple  $\Delta U_C^{pk-pk}$  as:

$$\Delta U_C^{pk-pk} = \frac{U_{IN} \cdot D \cdot (1-D)}{8 \cdot L_f \cdot C_f \cdot f_{sw}^2} \quad (9-11)$$

From the (9-11) we see that at the given voltage ripple  $U_r$ , the increase of switching frequency radically will decrease the needed filter mass and volume. In the real circuit however the voltage ripple is in most cases higher, because of not ideal capacitive filter components. Real electrolytic capacitors can be represented as series connected equivalent resistance ESR and inductance ESL. The additional output voltage ripple AC component with consideration of real components can be calculated as:

$$\Delta U_C^p = \frac{R_{ESR}^C \cdot U_{Load}' (1-D)}{L_f \cdot f_{sw}} + \frac{L_{ESL}^C \cdot U_{Load}'}{L_f \cdot D} \quad (9-12)$$

In most cases the above mentioned parasitic parameters are determining the output voltage ripple level.

The boundary operation condition at the given value of the output filter inductor or at the given load current is determined from (9-7) by:

$$I_{Load}^{BCM} = \frac{U_{IN} D \cdot (1-D)}{2 \cdot L \cdot f} \quad (9-13)$$

$$L_{Lf}^{BCM} = \frac{U_{IN} D \cdot (1-D)}{2 \cdot I_{Load} \cdot f}$$

The boundary operation condition is met if the load current is less than  $I_{Load}^{BCM}$  or if the output filter inductance is less than  $L_{Lf}^{BCM}$  at the given output current. Considering that the  $I_{min} = 0$ , and from (9-5) and taking the on time of the freewheeling diode equal to  $T_{OFF} = T_{ON} \cdot \frac{(U_{IN} - U_{Load}')}{U_{Load}'}$  we can find the average load current value by means of piece wise integration:

$$I_{Load} = \frac{1}{T} \int_0^{T_{ON}} \frac{U_{IN} - U_{Load}'}{L_f} t dt + \frac{1}{T} \int_0^{T_{OFF}} \left( \frac{U_{IN} - U_{Load}'}{L_f} T_{ON} - \frac{U_{Load}'}{L_f} t \right) dt$$

After multiplication of the both sides of the equation and some simplification procedures the regulation characteristics of the converter in DCM can be found:

$$\frac{U'_{Load}}{U_{IN}} = \frac{D^2}{4 \cdot \frac{L_f}{R_{Load}} \cdot f_{sw}} \left( \sqrt{1 + \frac{8 \cdot \frac{L_f}{R_{Load}} \cdot f_{sw}}{D}} - 1 \right) \quad (9-14)$$

After replacing load resistance by  $R_{Load} = U_{Load} / I_{Load}$  the equation (9-14) can be written as:

$$\frac{U'_{Load}}{U_{IN}} = \frac{D^2}{D^2 - \left( \frac{2 \cdot L_f \cdot I_{Load} \cdot f_{sw}}{U_{IN}} \right)} \quad (9-15)$$

The real characteristic of the converter is load-dependant even in CCM mode, due to active resistance of the not ideal components (e.g. winding resistance of the inductor).

From the volt-second equality the real characteristics can be found:

$$(U_{IN} - U'_{Load} - I_{Load} \cdot r) \cdot D \cdot T = (U'_{Load} + I_{Load} \cdot r) \cdot (1 - D) \cdot T, \text{ from which:}$$

$$\frac{U'_{Load}}{U_{IN}} = D - \frac{I_{Load} \cdot r}{U_{IN}} \quad (9-16)$$

In case of Flyback converter the left side of the equation (9-4) has to be set to zero, after which it will become equivalent to equation (9-1).

During ON states of the switch and the rectifier diode the currents in corresponding time intervals are given by following relations

$$i_p(t) = I_p^{MIN} + \frac{U_{IN}}{L_p} t, \quad \text{if } 0 \leq t \leq T_{ON} = D \cdot T \quad (9-17)$$

$$i_s(t) = I_s^{MAX} - \frac{U_{Load}}{L_s} t, \quad \text{if } 0 \leq t \leq T_{OFF} = (1 - D) \cdot T$$

At the commutation point the maximum and minimum currents are related as:

$$\omega_p I_{p MAX}^{MIN} = \omega_s I_{s MAX}^{MIN} \quad (9-18)$$

By the absolute coupling of the primary and secondary windings, the inductances are:

$$L_s = L_p \cdot \left( \frac{\omega_s}{\omega_p} \right)^2 \quad (9-19)$$

Solution of the equation (9-17) - (9-19) gives the regulation characteristic of the converter in CCM mode

$$\frac{U_{Load}}{U_{IN}} = \frac{\omega_s}{\omega_p} \frac{D}{(1 - D)} \quad (9-20)$$

From energetic balance equation for this converter  $U_{Load} \cdot I_{Load} \cdot T = \int_0^{T_{ON}} U_{IN} \cdot i_p(t) dt$ , the upper and lower limits of the switch current are:

$$I_{sw\ MAX} = \frac{\omega_s I_{Load}}{\omega_p (1-D)} \mp \frac{U_{IN} \cdot D}{2 \cdot L_p \cdot f_{sw}} \quad (9-21)$$

The average current through the switch and rectifier diode in the corresponding ON-state intervals are:

$$\begin{aligned} I_{sw} &= \frac{\omega_s \cdot I_{load}}{\omega_p (1-D)} \\ I_{VD} &= \frac{I_{Load}}{(1-D)} \end{aligned} \quad (9-22)$$

The average currents during switching period are equal:

$$I_{sw}^{ave} = \frac{\omega_s \cdot I_{Load} \cdot D}{\omega_p \cdot (1-D)} \quad (9-23)$$

$$I_{VD}^{ave} = I_{load}$$

The voltages on the switch and on the rectifier diode during corresponding OFF times are:

$$\begin{aligned} U_{sw} &= U_{IN} + \frac{\omega_p}{\omega_s} U_{Load} = \frac{U_{IN}}{1-D} \\ U_{VD} &= \frac{\omega_s}{\omega_p} U_{IN} + U_{Load} = \frac{\omega_s \cdot U_{IN}}{\omega_p \cdot (1-D)} \end{aligned} \quad (9-24)$$

The rated power of the switch is:

$$P_{sw} = \frac{P_{Load}}{D \cdot (1-D)} \quad (9-25)$$

If the  $I_p$  from the (9-21) becomes equal to 0, the converter enters in BCM mode. The boundary condition therefore is given as:

$$\begin{aligned} I_{Load}^{BCM} &= \frac{\omega_p \cdot U_{IN} \cdot D \cdot (1-D)}{2 \omega_s \cdot L_p \cdot f_{sw}} \\ L_f^{BCM} &= \frac{\omega_p \cdot U_{IN} \cdot D \cdot (1-D)}{2 \omega_s \cdot I_{Load} \cdot f_{sw}} \end{aligned} \quad (9-26)$$

The regulation characteristic can be found like for (9-14):

$$\frac{U_{Load}}{U_{IN}} = D \sqrt{\frac{1}{2 \cdot \frac{L_p}{R_{Load}} f_{sw}}} \quad (9-27)$$

By replacing the  $R_{Load}$  in (9-17) we can get the external characteristic of the converter in CCM mode:

$$\frac{U_{Load}}{U_{IN}} = \frac{D^2 \cdot U_{IN}}{2 \cdot L_p \cdot I_{Load} \cdot f_{sw}} \quad (9-28)$$

Considering the active copper resistance of the inductances the real characteristics can be found from the volt-second equality on the inductive elements

$$\frac{U_{Load}}{U_{IN}} = \frac{\omega_s D}{\omega_p (1 - D)} - \frac{D \cdot r_p \cdot \left( \frac{\omega_s}{\omega_p} \right)^2 + r_s \cdot (1 - D)}{U_{IN} \cdot (1 - D)^2} I_{Load} \quad (9-29)$$

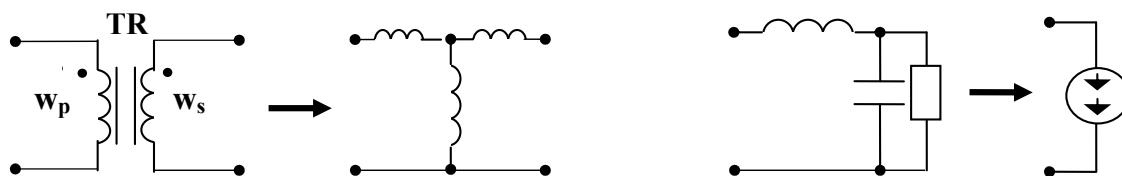
## A2 Detailed operation analysis of the resonant reset forward converter

In resonant reset converter, the transformer core is reset by the resonance of the transformer magnetizing inductance and parasitic capacitances of switching devices. However transformer Flyback voltage and reset time are strongly affected by device parameters e.g. main switch output capacitance, rectifier and freewheeling displacement capacitors etc. Therefore detailed analysis for reset time and possible overvoltage prediction is very important.

There are 5 operating states in resonant reset converter. The equivalent circuit diagrams for each state is presented in figure

The exact analysis is carried out under following assumptions:

1. The transformer is considered as T model with equal distribution of parasitic leakage inductances
2. The stray inductances of the transformer are much smaller than (main) magnetizing inductance.
3. Transformer winding capacitance is recalculated and considered as output capacitance of the transistor
4. The copper resistances of windings are neglected
5. Parasitic capacitances are considered during OFF time of the switches.
6. The diode reverse recovery time is neglected (assuming to use SiC diodes)
7. Output current during switching periods is considered constant – the output filter inductor is large enough
8. The converter is always operating in CCM mode – continues inductor current



**Equivalent circuits of the transformer and output filter**

## MathCAD Program listing with comments

### Resonant Reset Forward Converter Analysis

#### 1. Input parameters

Input Voltage	Output Voltage	Output Power	Output Current
$E_{in} := 400V$	$V_{out} := 48V$	$P_{out} := 1000W$	$I_{out} := \frac{P_{out}}{V_{out}}$
Switching Period		Duty cycle	Switch on time
$T_{sw} := 4\mu s$		$D := 0.5$	$T_{on} := D \cdot T_{sw}$

#### 2. Transformer

Winding turns ratio	Magnetising inductance	Prim. stray inductance	Sec.inductance
$N_{TR} := 20$	$L_\mu := 640 \cdot 10^{-6} H$	$L_{1S} := 30 \cdot 10^{-9} H$	$L_{2S} := 30 \cdot 10^{-9} H$

#### 3. Power stage defintions

Switch drain voltage	Rectifier diode voltage	Freewhiling diode voltage
$v_Q(t) := 0$	$v_{D1}(t) := 0$	$v_{D2}(t) := 0$
Switch output capacitance	Rectifier diode capacitance	Freewhiling diode voltage
$C_Q := 0.5 \cdot 10^{-9} F$	$C_{D1} := 30 \cdot 10^{-12} F$	$C_{D2} := 30 \cdot 10^{-12} F$
Switch drain source resistance	Diodes forward voltage	
$R_{DS} := 0.5 \times 10^{-3} \text{ ohm}$	$V_{DF} := 1.1V$	

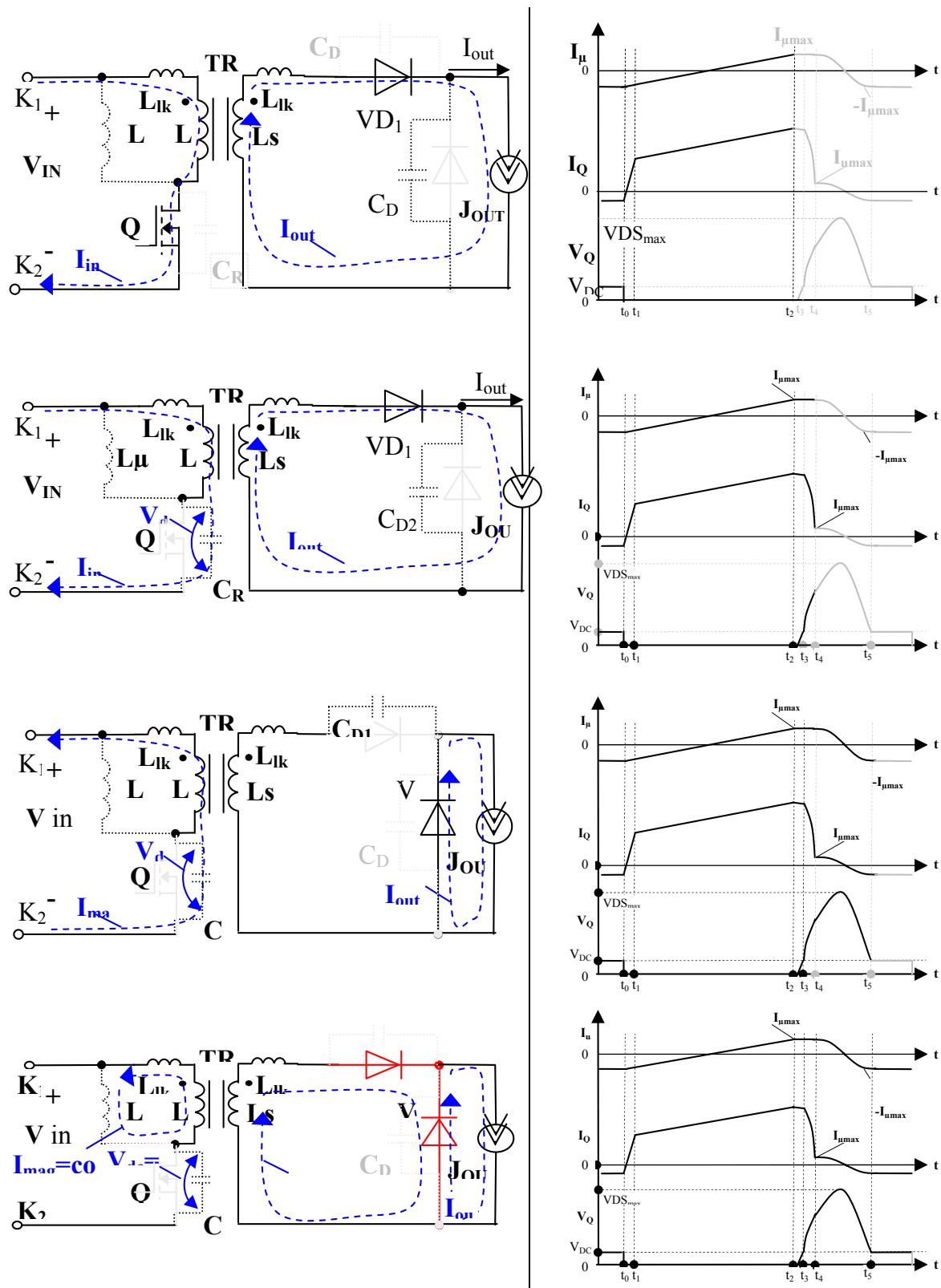


Figure 9-1 Equivalent circuits of resonant reset forward converter in different states

### Stage A

The overall stray inductance is:  $L_S := L_{1S} + L_{2S}$

During the time 0 to  $T_1 := \frac{L_S \cdot (I_{out} - i_{20})}{E_{in}}$  the magnetizing and output current will rise according:

$$i_2(t) := \frac{E_{in}}{L_S} \cdot t + i_{20} \quad i_\mu(t) := \frac{L_{2S}}{L_S \cdot L_\mu} \cdot E_{in} \cdot t + i_{\mu0}$$

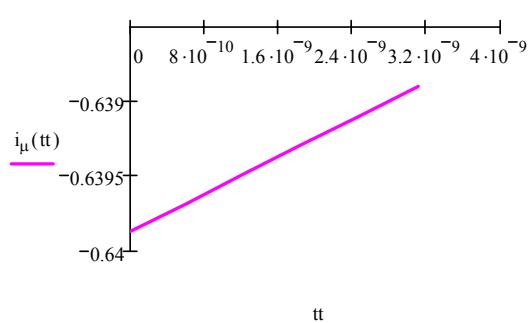
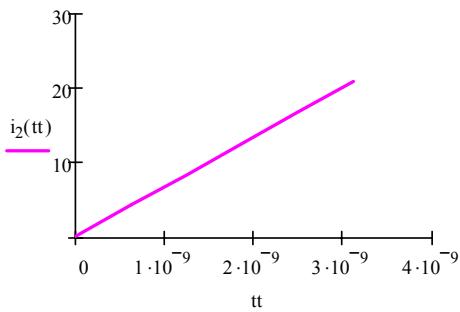
Initial voltage on the transistor is:

$$v_Q(t) := 0 \quad v_{QA}(t) := v_Q(0)$$

Currents levels at endtime of stage A is:

$$i_\mu(T_1) = -0.639 \text{ A} \quad i_2(T_1) = 20.833 \text{ A}$$

$$\text{time step: } tt := 0, \frac{T_1}{5} .. T_1$$



### Stage B

During the ON-time interval, the energy is transferred from input to output

The magnetising inductance current will rise according:  $i_{\mu T1} := \frac{L_{2S}}{L_S} \cdot E_{in} \cdot \frac{T_1}{L_\mu} + i_{\mu0}$

Due to parasitic capacitance of the freewheeling diode, the oscillation with resonant frequency

$$w_b := \frac{1}{\sqrt{L_S \cdot C_{D2}}} \quad w_b = 745.356 \text{ MHz}$$

The diode capacitance will be charged and the oscillations caused by  $L_{S1}$  and  $L_{S2}$  and  $C_{D2}$  will be relaxed to zero

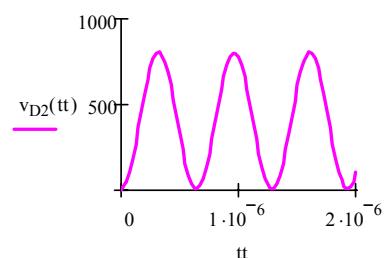
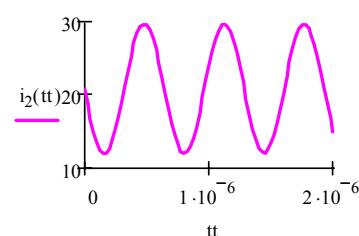
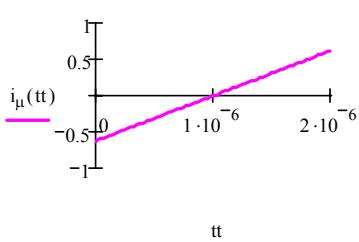
$$i_\mu(t) := I_{out} + E_{in} \cdot \sqrt{\frac{C_{D2}}{L_S}} \cdot \sin[w_b \cdot (t - T_1)] \quad i_2(t) := \frac{E_{in}}{L_\mu} \cdot (t - T_1) + i_{\mu0} + E_{in} \cdot \sqrt{\frac{L_{1S}}{L_S}} \cdot \sqrt{\frac{C_{D2}}{L_S}} \cdot \sin[w_b \cdot (t - T_1)]$$

The diode voltage will change according:  $v_{D2}(t) := E_{in} \cdot [1 - \cos[w_b \cdot (t - T_1)]]$

The transistor drain voltage is remaining:

$$v_Q(t) := 0 \quad v_{QB}(t) := v_Q(t)$$

$$\text{Time step: } tt := T_1, T_1 + \frac{T_2 - T_1}{80} .. T_2$$



**Stage F**

Stage F begins at time  $T_2$ , during this stage the output capacitance of the transistor  $C_Q$  is charged, whereas the  $C_{D2}$  is discharged

The resonant frequency of the charging process is equal to  $w_f := \frac{1}{\sqrt{L_\mu \cdot (C_Q + C_{D2})}}$   $w_f = 1.717 \times 10^3$  kHz

and the characteristic impedance of the  $L_\mu$  and parallel connected  $C_Q$  and  $C_{D2}$  is equal to  $Z_f := \sqrt{\frac{L_\mu}{C_Q + C_{D2}}}$

The magnetising current has reached at this moment the level  $i_{\mu T2} := \left( \frac{E_{in}}{L_\mu} \right) \cdot (T_2 - T_1) + i_{\mu T1} \quad i_{\mu T2} = 0.609$  A

$$X_f := \sqrt{\left( \frac{E_{in}}{Z_f} \right)^2 + (I_{out} + i_{\mu T2})^2} \quad Y_f := \tan\left( Z_f \frac{I_{out} + i_{\mu T2}}{E_{in}} \right)$$

During this interval the magnetising and secondary currents will change according to:

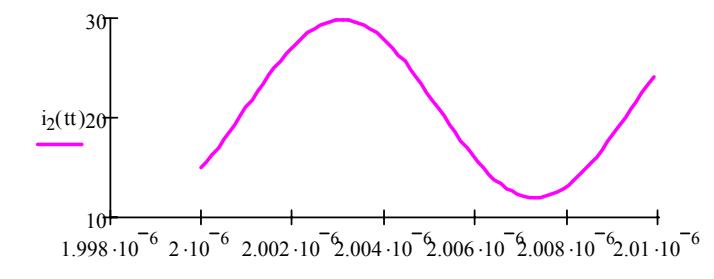
$$T_3 := \frac{\frac{\pi}{2} - Y_f}{w_f} + T_2 \quad tt := T_2, T_2 + \frac{T_3 - T_2}{80} \dots T_3$$

$$i_{\mu}(t) := I_{out} - \frac{C_{D2}}{C_Q + C_{D2}} \cdot X_f \sin[w_f(t - T_2) + Y_f]$$

$$i_{\mu}(t) := X_f \sin[w_f(t - T_2) + Y_f] - I_{out}$$

$$i_{\mu T3} := X_f - I_{out}$$

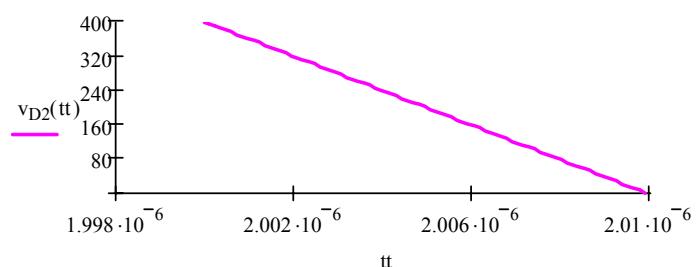
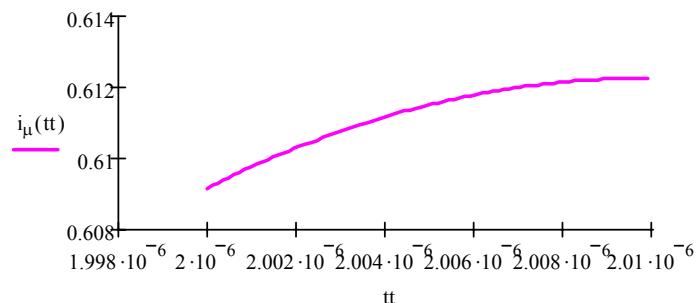
$$v_{D2}(t) := Z_f X_f \cos[w_f(t - T_2) + Y_f]$$



$$v_Q(t) := E_{in} - v_{D2}(t)$$

$$v_{QF}(t) := v_Q(t)$$

$$v_{D1} := 0$$



This interval ends at  $t=T_3$ , when  $V_{D2}$  reaches zero, and  $C_{D2}$  is entirely discharged

### Stage E

In this stage at  $T_3$  the freewheeling diode turns ON

The output capacitance of the transistor is charged by the remaining energy stored in stray inductances of the transformer

$$\text{The resonant frequency and characteristic impedance are: } w_e := \frac{1}{\sqrt{L_S \cdot C_Q}} \quad Z_e := \sqrt{\frac{L_S}{C_Q}} \quad w_e = 182.574 \text{ MHz}$$

$$\text{This interval is very short, therefore the magnetizing current can be assumed as constant} \quad Z_e = 10.954 \frac{\text{V}}{\text{A}}$$

$$i_{2T3} := I_{out} - \frac{C_{D2}}{C_Q + C_{D2}} \cdot X_f \quad i_2(t) := (i_{2T3} + i_{\mu T3}) \cdot \cos[w_e(t - T_3)] - i_{\mu T3}$$

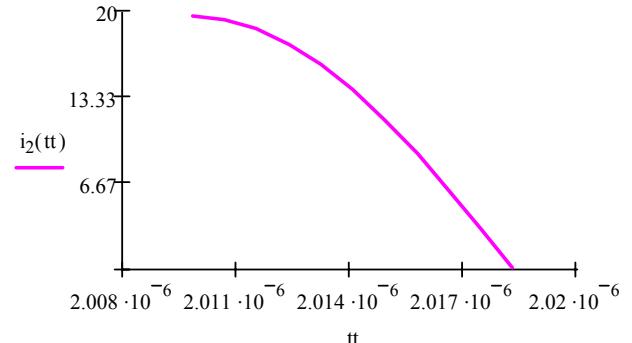
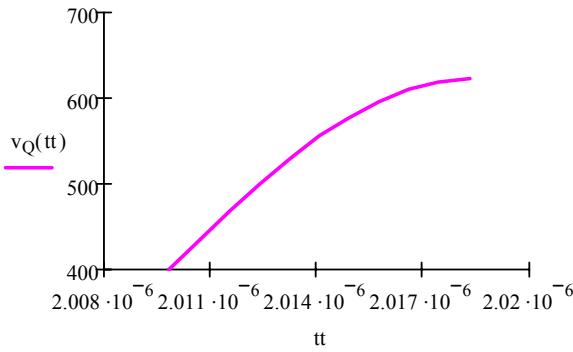
$$\text{The duration of this stage is equal to: } T_4 := \frac{1}{w_e} \cdot \arccos \left( \frac{i_{\mu}(T_3)}{i_2(T_3) + i_{\mu}(T_3)} \right) + T_3 \quad T_4 - T_3 = 8.438 \times 10^{-9} \text{ s}$$

$$i_{\mu}(t) := i_{\mu T3}$$

$$v_Q(t) := E_{in} + Z_e \cdot (i_{2T3} + i_{\mu T3}) \cdot \sin[w_e(t - T_3)]$$

$$\text{The drain voltage continues to rise: } v_{QT4} := E_{in} + Z_e \cdot \sqrt{\left( \frac{C_Q}{C_Q + C_{D2}} \right)^2 \cdot (I_{out} + i_{\mu T3})^2 - i_{\mu T3}^2} \quad \text{up to} \quad v_{QT4} = 621.525 \text{ V}$$

$$tt := T_3, T_3 + \frac{T_4 - T_3}{10} .. T_4$$



**Stage G**

At  $t=T_4$  the rectifier diode turns OFF, and oscillation caused by  $L_\mu$ ,  $C_Q$  and  $C_{D1}$  occurs

$$\text{The resonant frequency and characteristic impedance are: } w_g := \frac{1}{\sqrt{L_\mu \cdot (C_Q + C_{D1})}} \quad w_g = 1.717 \times 10^3 \text{ kHz}$$

$$i_{\mu T4} := i_\mu(T_3) \quad i_\mu(T_4) = 0.612 \text{ A}$$

$$Z_g := \sqrt{\frac{L_\mu}{C_Q + C_{D1}}}$$

$$X_g := \sqrt{i_{\mu T4}^2 + \frac{(v_{QT4} - E_{in})^2}{Z_g^2}}$$

$$Y_g := \begin{cases} \text{atan}\left(\frac{v_{QT4} - E_{in}}{Z_g \cdot i_{\mu T4}}\right) & \text{if } i_\mu(T_4) > 0 \\ \pi - \text{atan}\left(\frac{v_{QT4} - E_{in}}{-Z_g \cdot i_{\mu T4}}\right) & \text{otherwise} \end{cases}$$

The drain voltage will reach its maximum level afterwards will decay according the sinus form

$$v_Q(t) := E_{in} + X_g \cdot Z_g \cdot \sin[w_g \cdot (t - T_4) + Y_g]$$

The rectifier diode will see the same voltage form on the secondary side

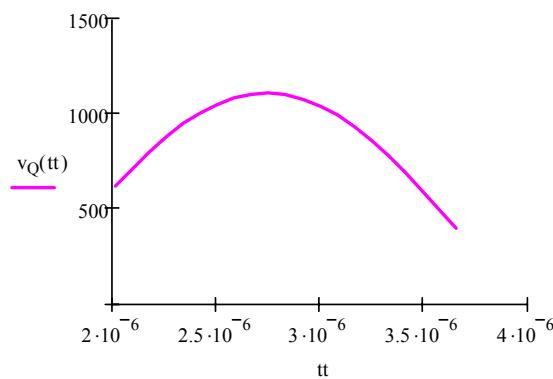
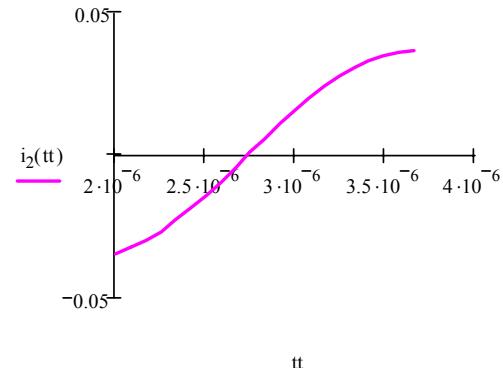
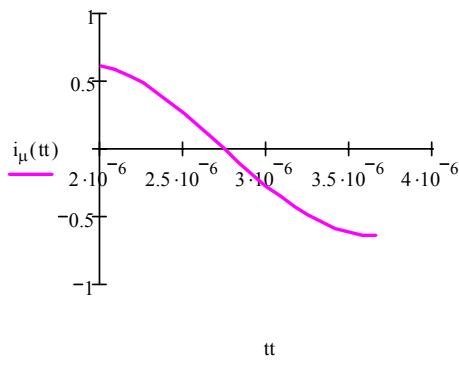
$$v_{D1}(t) := v_Q(t) - E_{in}$$

$$v_{D2}(t) := 0$$

$$T_5 := \frac{\pi - Y_g}{w_g} + T_4 \quad tt := T_4, T_4 + \frac{T_5 - T_4}{20} .. T_5$$

$$i_Q(t) := X_g \cdot \cos[w_g \cdot (t - T_4) + Y_g]$$

$$i_D(t) := -\frac{C_{D1}}{C_Q + C_{D1}} \cdot [X_g \cdot \cos[w_g \cdot (t - T_4) + Y_g]]$$



### Stage E short circuit

At  $t=T_5$ , D1 turns ON again, and during this interval the secondary winding of the transformer is shorted by D1 and D2

Magnetising current will circulate through the diodes and will remain almost constant until the power transistor turn ON again

$$w_{ec} := \frac{1}{\sqrt{L_s \cdot C_Q}} \quad w_{ec} = 218.218 \text{ MHz}$$

$$i_{2s}(t) := \frac{C_{D1}}{C_Q + C_{D1}} \cdot X_g \cdot \sin[w_{ec}(t - T_5)]$$

$$i_{2T5} := i_2(T_5) \quad i_{2T5} := \frac{C_{D1}}{C_Q + C_{D1}} \cdot X_g$$

$$i_{\mu}(t) := -X_g \quad i_{\mu T5} := -X_g$$

$$v_{Q4}(t) := E_{in} \quad V_{D1} := 0 \quad V_{D2} := 0$$

$$w_{es} := \frac{2w_{ec}}{\tau_{tot}}$$

$$w_{ec} = 36.37 \text{ MHz}$$

In a steady state the final values of the secondary and magnetizing current become the initial values for Stage A

By solving following system of linear equations the initial values for  $i_{\mu}(0)$  and  $i_2(0)$  can be found:

Vorgabe

$$i_{20} = \frac{L_s \cdot I_{out} - T_1 \cdot E_{in}}{L_s}$$

$$i_{\mu 0} = \frac{(-L_{2s}) \cdot E_{in} \cdot T_1 + i_{\mu T1} \cdot L_s \cdot L_{\mu}}{L_s \cdot L_{\mu}}$$

$$i_{\mu T1} = \frac{(-E_{in}) \cdot T_2 + T_1 \cdot E_{in} + i_{\mu T2} \cdot L_{\mu}}{L_{\mu}}$$

$$i_{\mu T3} = X_f - I_{out}$$

$$i_{\mu T4} = i_{\mu T3}$$

$$v_{QT4} = E_{in} + Z_g \cdot \sqrt{\left(\frac{C_Q}{C_Q + C_{D2}}\right)^2 \cdot (I_{out} + i_{\mu T3})^2 - i_{\mu T3}^2}$$

$$T_5 = \frac{\pi - \arctan\left(\frac{v_{QT4} - E_{in}}{Z_g \cdot i_{\mu T4}}\right)}{w_g} + T_4$$

$$i_{2T5} = \frac{C_{D1}}{C_Q + C_{D1}} \cdot X_g$$

$$i_{\mu T5} = -X_g$$

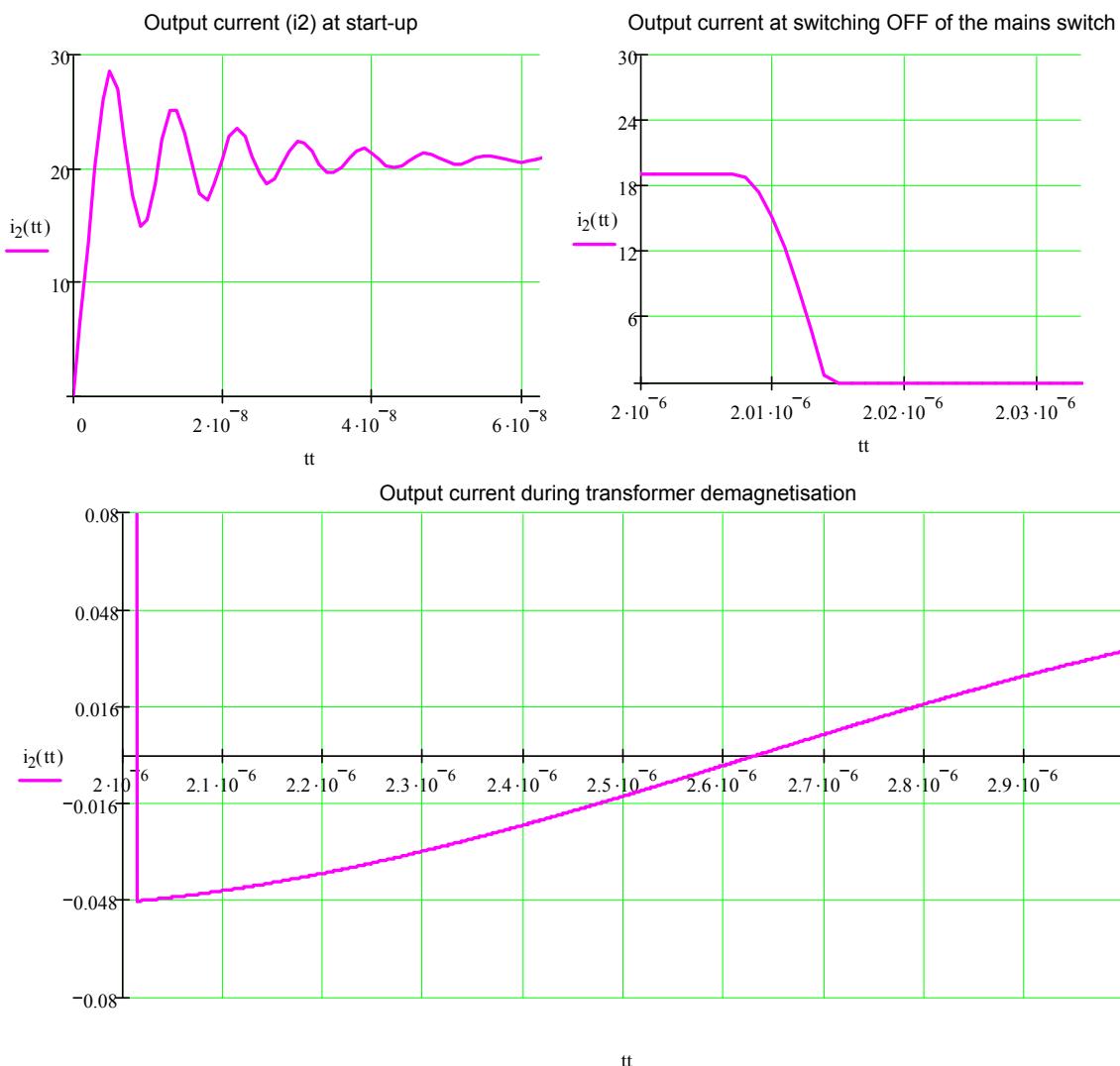
$$\text{Suchen } (i_{20}, i_{\mu 0}) \rightarrow i_{20} := \frac{-(E_{in} \cdot T_2 - L_{1s} \cdot I_{out})}{2 \cdot L_{\mu}} - \frac{C_Q + C_{D1}}{C_Q} \cdot \frac{\left(\frac{C_Q}{C_Q + C_{D1}}\right)^2 \cdot (L_{1s} + L_{2s}) \cdot I_{out}^2}{2 \cdot (E_{in} \cdot T_2 - L_{1s} \cdot I_{out})}$$

$$i_{20} := -\frac{C_{D1}}{C_Q + C_{D1}} \cdot i_{\mu 0}$$

### Resulting Current and Voltage Equations

*Secondary current:*

$$\dot{i}_2(tt) := \begin{cases} \frac{E_{in}}{L_S} \cdot tt + i_{20} & \text{if } 0 \leq tt < T_1 \\ I_{out} + E_{in} \cdot \sqrt{\frac{C_{D2}}{L_S}} \cdot \sin[w_b(t - T_1)] \cdot e^{\left[ \frac{-w_b}{\tau_{tot}}(t - T_1) \right]} & \text{if } T_1 \leq t < T_2 \\ I_{out} - \frac{C_{D2}}{C_Q + C_{D2}} \cdot X_f \sin[w_f(t - T_2) + Y_f] & \text{if } T_2 \leq t < T_3 \\ (i_{2T3} + i_{\mu T3}) \cdot \cos[w_e(t - T_3)] - i_{\mu T3} & \text{if } T_3 \leq t < T_4 \\ -\frac{C_{D1}}{C_Q + C_{D1}} \cdot [X_g \cos[w_g(t - T_4)] + Y_g] & \text{if } T_4 \leq t < T_5 \\ \frac{C_{D1}}{C_Q + C_{D1}} \cdot X_g & \text{if } T_5 \leq t < T_6 \end{cases}$$



For plotting complete waveforms corresponding equations for each operation stage following time intervals are introduced:

### Timing

$$T_{sw} = 4 \times 10^{-6} \text{ s} \quad \text{Period} \quad \text{Time step} \quad \text{step} := 10^{-9} \text{ s} \quad tt := 0, \text{step} .. T_{sw}$$

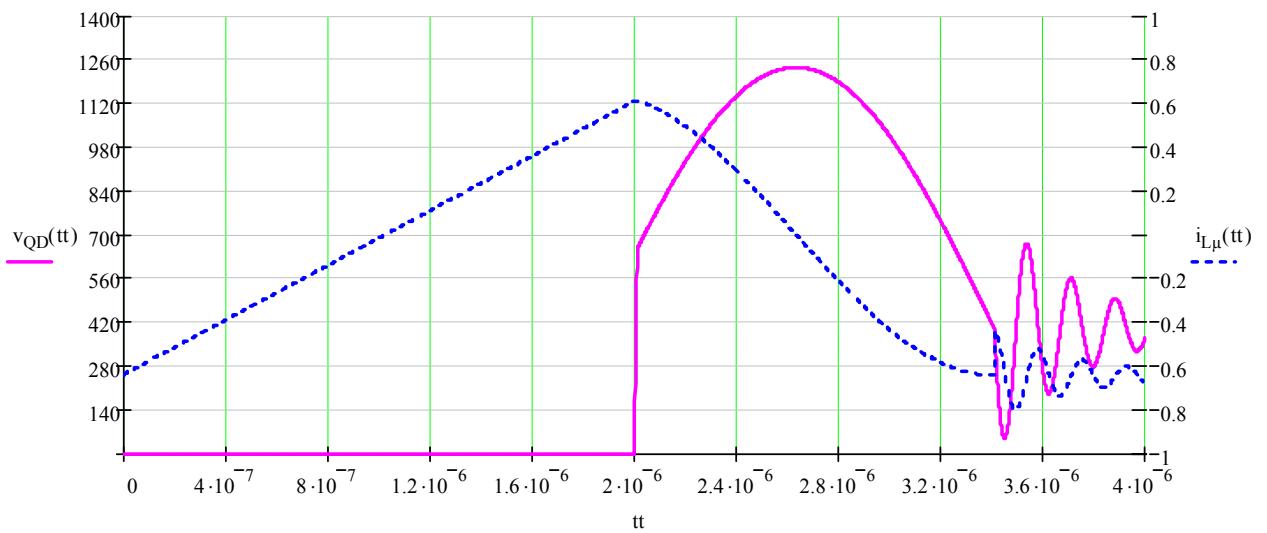
$$T_1 = 3.117 \times 10^{-9} \text{ s} \quad \text{Stage A} \quad T_4 = 2.014 \times 10^{-6} \text{ s} \quad \text{Stage E}$$

$$T_2 = 2 \times 10^{-6} \text{ s} \quad \text{Stage B} \quad T_5 = 3.408 \times 10^{-6} \text{ s} \quad \text{Stage G}$$

$$T_3 = 2.007 \times 10^{-6} \text{ s} \quad \text{Stage F} \quad T_6 := T_{sw} \quad \text{Stage E sc}$$

$$v_{QD}(tt) := \begin{cases} 0 \cdot V & \text{if } 0 \leq tt < T_1 \\ v_{QB}(tt) & \text{if } T_1 \leq tt < T_2 \\ v_{QF}(tt) & \text{if } T_2 \leq tt < T_3 \\ E_{in} + Z_e \cdot (i_{2T3} + i_{\mu T3}) \cdot \sin[w_e \cdot (tt - T_3)] & \text{if } T_3 \leq tt < T_4 \\ E_{in} + X_g \cdot Z_g \cdot \sin[w_g \cdot (tt - T_4) + Y_g] & \text{if } T_4 \leq tt < T_5 \\ E_{in} \left[ 1 - e^{-\left[ w_{ec} \frac{(tt-T_5)}{\tau_{tot}} \right]} \cdot \sin[w_{ec} \cdot (tt - T_5)] \right] & \text{if } T_5 \leq tt < T_6 \end{cases} \quad \text{Drain voltage}$$

$$i_{L\mu}(tt) := \begin{cases} \frac{L_{2S}}{L_S \cdot L_\mu} \cdot E_{in} \cdot tt + i_{\mu 0} & \text{if } 0 \leq tt < T_1 \\ \frac{E_{in}}{L_\mu} \cdot (tt - T_1) + i_{\mu 0} + E_{in} \cdot \frac{L_{1S}}{L_\mu} \cdot \sqrt{\frac{C_{D2}}{L_S}} \cdot \sin[w_b \cdot (tt - T_1)] & \text{if } T_1 \leq tt < T_2 \\ X_f \sin[w_f \cdot (tt - T_2) + Y_f] - I_{out} & \text{if } T_2 \leq tt < T_3 \\ i_{\mu T3} & \text{if } T_3 \leq tt < T_4 \\ X_g \cdot \cos[w_g \cdot (tt - T_4) + Y_g] & \text{if } T_4 \leq tt < T_5 \\ -X_g \left[ 1 - \frac{e^{-\left[ w_{ec} \frac{(tt-T_5)}{\tau_{tot}} \right]}}{\pi} \cdot \cos[w_{ec} \cdot (tt - T_5)] \right] & \text{if } T_5 \leq tt < T_6 \end{cases} \quad \text{Magnetizing current:}$$



## B1 Analysis of single switch double-ended composite Forward-Flyback converter

Derivation of the operation characteristics under following assumptions:

1. Input voltage source has zero internal resistance (ideal voltage source)
2. Switching time (rise and fall times) of the switches are neglected
3. ESR of the filter capacitances are equal to zero
4. Output voltage ripple is negligibly small compared to the average output voltage level
5. All switches are ideal

For the CCM operation mode, when the transformer and inductor currents are continuous, the energy balance equation results to following:

$$U_{IN} \cdot D \cdot T_{sw} = U_C \cdot (1-D) \cdot T \Leftrightarrow \frac{U_C}{U_{IN}} = \frac{D}{1-D} \quad (9-30)$$

The output characteristic is defined as

$$U_{Load} = n_1 \cdot U_{IN} \cdot D + n_2 \cdot U_C \cdot (1-D) \Leftrightarrow \frac{U_{Load}}{U_{IN}} = (n_1 + n_2) \cdot D \quad (9-31)$$

The absolute voltage values on transformer primary during ON (DT) and OFF (1-D)T time are respectively equal to  $U_{IN}$  and  $U_C$ .

Considering the magnetizing current that first increases from  $I_{\mu\min}$  and then decreases from  $I_{\mu\max}$ , the current changing can be described as:

$$\begin{aligned} I_{\mu 1}(t) &= I_{\mu}^{\min} + \frac{U_{IN}}{L_{\mu}} t; \quad \text{if } 0 \leq t \leq T_{ON} = D \cdot T_{sw} \\ I_{\mu 2}(t) &= I_{\mu}^{\max} - \frac{U_{IN} D}{(1-D) L_{\mu}} t; \quad \text{if } 0 \leq t \leq T_{OFF} = (1-D) \cdot T_{sw} \end{aligned} \quad (9-32)$$

On the output filter inductor during ON time the  $n_1 U_{IN} - U_{Load}$  is applied and during switch OFF time:  $U_{Load} - n_2 U_C$ . Therefore the currents through the inductor are:

$$\begin{aligned} i_L(t) &= I_L^{\min} + \frac{n_1 \cdot U_{IN} \cdot \left(1 - \frac{D \cdot (n_1 + n_2)}{n_1}\right)}{L_f} t; \quad \text{if } 0 \leq t \leq T_{ON} \\ i_{L2}(t) &= I_L^{\max} - \frac{n_1 \cdot U_{IN} \cdot D \cdot \left(1 - \frac{D \cdot (n_1 + n_2)}{n_1}\right)}{(1-D) \cdot L_f} t; \quad \text{if } 0 \leq t \leq T_{OFF} \end{aligned} \quad (9-33)$$

The maximum and minimum values of the currents can be found from the energy balance equation: During ON time on the LC filter input a voltage  $n_1 E$  is applied and current is changing according equation above, therefore:

$$I_{Load} \cdot n_1 \cdot U_{IN} \cdot D \cdot T = \int_0^{DT} n_1 \cdot U_{IN} \cdot i_{L1}(t) dt \quad (9-34)$$

Taking in account that  $i_{L1}(DT) = I_{max}$ , we get :

$$I_L^{\min} = I_{Load} \mp \frac{n_1 \cdot U_{IN} \cdot D \cdot \left(1 - \frac{D \cdot (n_1 + n_2)}{n_1}\right)}{2 \cdot L_f \cdot f_{sw}} \quad (9-35)$$

And for (1-D)T time:

$$I_{Load} \cdot n_2 \cdot U_{IN} \cdot D \cdot T = \int_0^{(1-D)T} \frac{U_{IN} D}{1-D} \cdot i_{\mu 2}(t) dt \quad (9-36)$$

Because at time  $t = (1-D) T$  the  $i_{\mu 2} = I_{\mu \min}$ , therefore:

$$I_{\mu}^{\min} = n_2 I_{Load} \mp \frac{U_{IN} D}{2 \cdot L_{\mu} \cdot f} \quad (9-37)$$

The current through the power transistor during ON time is defined by the sum of magnetizing and load currents:  $i_{VT1}(t) = i_{\mu 1}(t) + n_1 \cdot i_{L1}(t)$  according (9-32) and (9-33).

Therefore the minimum and maximum currents can be written as:

$$I_{VT1}^{\min} = I_m^{\min} + n_1 I_L^{\min} \quad (9-38)$$

From (9-35) is visible that if the condition  $D = \frac{n_1}{n_1 + n_2}$  is satisfied then

$$I_L^{\min} = I_L^{\max} = I_{Load} \quad (9-39)$$

In this case the load current does not change in time anymore (9-33). Obviously there is no need to use a filter in this case, because the applied voltages during both ON and OFF times are equal.

The current through the clamping capacitor C can be written as:

$$I_C(t) = I_C^{\max} \left(1 - \frac{2 \cdot f \cdot t}{1-D}\right) \mid 0 \leq t \leq (1-D) \cdot T \quad (9-40)$$

$$I_C^{\max} = \frac{U_{IN} \cdot D}{2f} \left( \frac{1}{L_{\mu}} - \frac{n_1 n_2 \left(1 - \frac{D \cdot (n_1 + n_2)}{n_1}\right)}{L} \right) \quad (9-41)$$

The voltages on the switches  $U_{VT1}$ ,  $U_{VT2}$ ,  $U_{VD3}$ ,  $U_{D1}$ , and  $U_{VD2}$  can be found as:

$$U_{VT1}^{DS} = U_{VT2}^{DS} = U_{VD3} = \frac{U_{IN}}{1-D}; U_{VD1} = \frac{(n_1 + n_2) \cdot U_{IN} \cdot D}{1-D}; U_{VD2} = (n_1 + n_2) \cdot U_{IN} \quad (9-42)$$

The rated power of the transistor is equal to:

$$P_{VT1} = \frac{P_{Load}}{D \cdot (1-D)} \quad (9-43)$$

Converter operates in boundary conduction mode (BCM) if the condition  $I_{\mu\min} = 0$  in equation (9-37) occurs. The critical values of the inductances, which are corresponding to discontinuous current conduction mode can be found from:

$$L_{\mu}^{BCM} = \frac{U_{IN} \cdot D}{2 \cdot I_{Load} \cdot n_2 \cdot f}; L_f^{BCM} = \frac{n_1 \cdot U_{IN} \cdot D \cdot \left(1 - \frac{D \cdot (n_1 + n_2)}{n_1}\right)}{2 \cdot I_{Load} \cdot f} \quad (9-44)$$

By using the body or external connected diode the DCM conduction mode can be eliminated allowing converter operating at open load condition.

Voltage ripples on the capacitors of the converter: The peak-to-peak voltage on the clamping capacitor is equal to:  $\Delta U_C^{pk-pk} = \frac{\Delta Q}{C_{cl}}$ , therefore

$$\Rightarrow \Delta U_{C_{cl}}^{pk-pk} = \frac{I_C^{\max} \cdot (1-D) \cdot T}{4C_{cl}} = \frac{U_{IN} \cdot D \cdot (1-D)}{8 \cdot f^2 \cdot C_{cl}} \left[ \frac{1}{L_{\mu}} - \frac{n_1 n_2 \left(1 - \frac{D \cdot (n_1 + n_2)}{n_1}\right)}{L_f} \right] \quad (9-45)$$

And the peak-to-peak voltage on the output filter capacitor is defined as:  $i_{C_f} = i_L(t) - I_{Load}$

$$\Rightarrow \Delta U_{C_f}^{pk-pk} = \frac{n_1 \cdot U_{IN} \cdot D \left(1 - \frac{D \cdot (n_1 + n_2)}{n_1}\right)}{8 \cdot L \cdot f^2 \cdot C_{cl}} \quad (9-46)$$

From (9-46) it is visible that  $\Delta U_{C_f} > 0$  if  $D < \frac{n_1}{(n_1 + n_2)}$ ,  $\Delta U_{C_f} = 0$  if  $D = \frac{n_1}{(n_1 + n_2)}$  and

$\Delta U_{C_f} < 0$  if  $D > \frac{n_1}{(n_1 + n_2)}$ . Comparing with conventional back or forward converters we

can see that with right selection of the transformer windings in this converter the ripple voltage can be drastically decreased.

The optimal transformation coefficient can be selected according:

$$n_1 = n_2 = n = \frac{U_{Load}}{2} \left( \frac{1}{U_{IN}^{\min}} + \frac{1}{U_{IN}^{\max}} \right) \quad (9-47)$$

## C1 Derivation of the VI characteristics of the $L_{\text{leak}}, C_{\text{DS}}, V_D$ resonance circuit during switching ON time

By using current and voltage laws on the inductive and capacitive elements following equations can be obtained:

$$\begin{cases} U_{IN} = L_s \frac{di_L}{dt} + u_C \\ i_L = I_{\text{Load}} + i_C \\ i_C = C_{DS+VD1} \frac{dU_C}{dt} \end{cases} \quad (9-48)$$

Using Laplace transformation on the equations above we can obtain:

$$\begin{cases} \frac{U_{IN}}{s} = L_s(sI_L) + u_C \\ I_L = \frac{I_{\text{Load}}}{s} + I_C \\ I_C = C_{DS+VD1} \cdot sU_C \end{cases} \quad (9-49)$$

By inserting last two equations of the system into the preceding one we obtain:

$$\frac{U_{IN}}{s} = L_s \cdot s \left( \frac{I_{\text{Load}}}{s} + C_{DS+VD1} \cdot s \cdot U_C \right) + U_C \quad (9-50)$$

From this equation the  $U_C$  can be found:

$$U_C = \frac{L_s \cdot I_{\text{Load}} \cdot s - U_{IN}}{s \cdot (s^2 \cdot L_s \cdot C_{DS+VD1} + 1)} \quad (9-51)$$

Using inverse Laplace gives the following equation:

$$u_C = U_{IN} \cdot \left[ 1 - \cos \left( \frac{t}{\sqrt{L_s C}} \right) \right] - I_{\text{Load}} \cdot \sqrt{\frac{L_s}{C}} \sin \left( \frac{t}{\sqrt{L_s C}} \right) \quad (9-52)$$

The current through the capacitance can be obtained from (9-51) and (9-49), which give the following equation:

$$I_C = U_{IN} \frac{\frac{1}{L_s}}{\left( s^2 + \frac{1}{L_s C} \right)} - I_{\text{Load}} \sqrt{L_s C} \frac{\frac{1}{s \sqrt{L_s C}}}{\left( s^2 + \frac{1}{L_s C} \right)}$$

$$I_L = \frac{I_{\text{Load}}}{s} + U_{IN} \sqrt{\frac{C}{L_s}} \frac{1}{\left( s^2 + \frac{1}{L_s C} \right)} - I_{\text{Load}} \frac{s}{s^2 + \frac{1}{L_s C}}$$

Using inverse Laplace transformation we obtain the current:

$$i_L(t) = I_{\text{Load}} \left[ 1 - \cos \left( \frac{t}{\sqrt{L_s C}} \right) \right] + U_{IN} \sqrt{\frac{C}{L_s}} \sin \left( \frac{t}{\sqrt{L_s C}} \right)$$

## D1 Derivation of the transfer function

The transfer function of the voltage on the inductance is given as:

$$G(s) = \frac{U_L(s)}{U_e(s)} = \frac{s \cdot L}{\frac{1}{sC} + sL} = \frac{L \cdot C}{1 + s^2 L \cdot C} \text{ and for half sinus voltage, it is given as:} \quad (9-53)$$

$$U_L(s) = \frac{U_i}{s^2 + \frac{1}{LC}} = U_i \cdot \sqrt{LC} \frac{\frac{1}{\sqrt{LC}}}{s^2 + \frac{1}{LC}}$$

The inverse Laplace transformation will give:

$$u_L(t) = U_i \cdot \sqrt{LC} \sin \frac{1}{LC} t, \text{ where } \frac{1}{\sqrt{LC}} = \omega \quad (9-54)$$

$$\text{This voltage will oscillate during half period to zero: } V_{Lk} + V_{RES} \cdot \sin(\omega \cdot t) = 0 \quad (9-55)$$

The transfer function of the voltage on the inductance is given as:

$$G(s) = \frac{U_L(s)}{U_e(s)} = \frac{s \cdot L}{\frac{1}{sC} + sL} = \frac{L \cdot C}{1 + s^2 L \cdot C} \text{ and for half sinus voltage, it is given as:} \quad (9-56)$$

$$U_L(s) = \frac{U_i}{s^2 + \frac{1}{LC}} = U_i \cdot \sqrt{LC} \frac{\frac{1}{\sqrt{LC}}}{s^2 + \frac{1}{LC}}$$

The inverse Laplace transformation will give:

$$u_L(t) = U_i \cdot \sqrt{LC} \sin \frac{1}{LC} t, \text{ where } \frac{1}{\sqrt{LC}} = \omega \quad (9-57)$$

This voltage will oscillate during half period to zero:

$$V_{Lk} + V_{RES} \cdot \sin(\omega \cdot t) = 0 \quad (9-58)$$

## E1 Power switching device voltage and current stresses

Semiconductors must be rated to carry the maximum peak current  $I_p$  and be capable to block the peak voltage  $V_p$ , which can occur in the circuit. Depending on the application, these factors can be crucial determining the switch parameters such as switching speed, reverse blocking and recovery time, current gain etc. Sometimes both parameters at the same time  $V_p$ , and  $I_p$  are used for the topology comparisons. For buck derived converters (Chapter 2.2.1), during switch OFF time  $(1 - D) \cdot T$  the current flowing into the output filter  $L$  will decrease by  $\Delta I$  peak-peak ripple current amount:

$$\Delta i_{out} = \frac{1}{L} \cdot \int_0^{(1-D)*T} V_{out} dt = \frac{V_{out} \cdot (1 - D) \cdot T}{L} \quad (9-59)$$

the voltage ripple at the same time duration will be defined as:

$$\Delta v_{in} = \frac{1}{C} \cdot \int_0^{(1-D)*T} I_{in} dt = \frac{I_{in} \cdot (1 - D) \cdot T}{C} \quad (9-60)$$

By defining the ripple ratios  $\mathfrak{R}_C = \frac{\Delta v_{in}}{V_{in}}$ ,  $\mathfrak{R}_L = \frac{\Delta i_{out}}{I_{out}}$ , from equations (9-59) and (9-60)

we can find the stress parameter for both switch and diode:

$$V_p \cdot I_p = V_{in} \cdot (1 + \mathfrak{R}_C) \cdot I_{out} \cdot (1 + \mathfrak{R}_L) = P_{out} \frac{(1 + \mathfrak{R}_C) \cdot (1 + \mathfrak{R}_L)}{D} \quad (9-61)$$

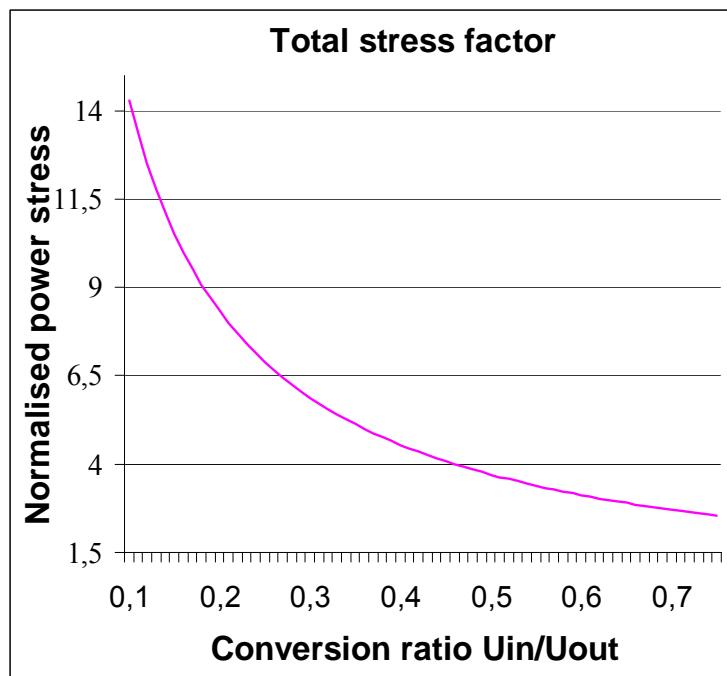


Figure 9-2 Power stress factor of the main switch in buck derived converters

## F1 Power Transformer Calculation

**Glättungsdrassel Infineon Reso 1kW 200kHz** c:\trafo ~

**Wicklung: Verlustleistung/Optimierung**

Hendx =  $w \cdot lwsx / bwx + ldfx / bwx$

Hendy =  $w \cdot lwsy / bwy + ldfy / bwy$

bwy/mm 0.750

mittl. 50.000

Lagenzahl 34.000

parallel(HF-Litz) 2

bwy/mm 0.750

ay/mm

ax/mm

ay/mm

dia/mm 1.500

bwx/mm 98.400

Hanfy =  $ldfy / bwy$

RHO/(Vmm/A) 0.000023

RHO(Cu 100 Grd C) 0.000023

Flachband/Runddraht

Flachband Runddraht

**Verlustleistung**

	X	Y
Pcu1/W	2,421	0,000
Pcu2/W	0,000	0,000
Pcu3/W	0,000	0,000
Pcu4/W	0,000	0,000
Pcu5/W	0,000	0,000
Pcu/x/y/gesamt/	2,421	0,000
Pcu gesamt/W	2,421	

Periodendauer/μs 5.000

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**Kern: Flußdichte-Eingabe/Verlustleistung** c:\trafo ~\1\inf\_reso.ini

Eingabe/Flußdichte

B/mT	304,200	361,500	304,200	0,000	0,000	0,000	0,000	0,000	0,000
Zeit/Tp/%	0,000	62,000	100,000	0,000	0,000	0,000	0,000	0,000	0,000
B/mT	0,000	0,000	0,000	0,000	0,000	0,000	0,000	0,000	0,000
Zeit/Tp/%	0,000	0,000	0,000	0,000	0,000	0,000	0,000	0,000	0,000

Löschen

**Kern-Werkstoff**

- N27
- N32
- 52M
- N67
- Kool μ
- C
- N87
- 26M

**Periodendauer/μs** 5.000

**Verlustleistung/W**

Magn.	Kernformkonstante
10500	1,000

Verlustleistung/W 1,808

1,808

1,000

Grafik

Drucken

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**B/mT**

+K

0

-K

0 50 100 Zeit/Tp/%

### **Selection of the transformer core**

Flusswandler: Grunddateneingabe/Kernauswahl					
<b>Typ</b>	<b>Infineon Reso 1kW 200kHz</b>				
<b>Uemax/V</b>	<b>410,000</b>		<b>Vtmax</b>	<b>0,620</b>	
<b>Uemin/V</b>	<b>390,000</b>		<b>Ktvar</b>	<b>1,000</b>	
<b>Uenenn/V</b>	<b>400,000</b>		<b>Ftakt/kHz</b>	<b>200,000</b>	
<b>Uanenn/V</b>	<b>48,000</b>		<b>Bsat/mT</b>	<b>320,000</b>	
<b>Ianenn/A</b>	<b>20,900</b>				
<b>Takt-Schema</b>	<b>Mittelpunkt-Wickl.</b>				
<input checked="" type="radio"/> Ein-Takt	<input type="radio"/> ohne	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
<input type="radio"/> Zwei-Tak	<input type="radio"/> primaer	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
<input type="checkbox"/> Phase-Shif	<input type="radio"/> sekundär	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
	<input type="radio"/> prim.+sek	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
<b>Kern-Reihe</b>					
<input checked="" type="radio"/> ETD	<input type="radio"/> EFD	<input type="radio"/> ELP	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
<input type="radio"/> ETD	<input type="radio"/> EFD	<input type="radio"/> ELP	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
<input type="radio"/> ETD	<input type="radio"/> EFD	<input type="radio"/> ELP	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
<b>Kern-Werkstoff</b>					
<input type="radio"/> N27	<input checked="" type="radio"/> N92	<input type="radio"/> N67	<input type="radio"/> Kool µ	<input type="radio"/> N87	<input type="radio"/>
<input type="radio"/> N27	<input type="radio"/> N92	<input type="radio"/> N67	<input type="radio"/> Kool µ	<input type="radio"/> N87	<input type="radio"/>
<b>Kernauswahl</b>					
<b>Kern</b>	<b>Pfe/W</b>	<b>Pcu/W</b>	<b>DTke/K</b>	<b>DTwi/K</b>	
ETD29	3,505	12,713	184,547	431,224	
ETD34	5,036	6,534	116,560	204,644	
ETD39	7,648	2,532	86,366	92,063	
CTD44	11,944	1,167	90,230	73,234	
ETD49	16,339	0,659	96,847	71,229	
ETD54	24,528	0,339	111,842	78,544	
ETD59	39,596	0,182	143,085	98,888	

frmWicklungsoptimierung

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Flusswandler: Wicklungsoptimierung						
Typ	Infineon Reso 1kW 200kHz					
Optimierung der Windungszahlen						
<b>Wp</b>		<b>Ws</b>				
23.092		5.258		11.944	1.167	90.238
30.000		7.000		5.326	2.018	47.552
<b>Übernahme Wdg.e!</b>		<b>Windungszahlen ne</b>				
		<b>Uemin/V</b>		<b>Vtnenn</b>	<b>DBmax/mT</b>	<b>DBnenn/mT</b>
		390.000		0.604	320.000	287.161
		380.574		0.590	246.318	215.698
Kern	Bwred/mm	Hw/mm	Lw/mm	Fm/mm <sup>2</sup>	Vm/mm <sup>3</sup>	Cm
ETD44	21.500	7.100	77.700	172.000	17800.000	1.117

Wirkungsoptimierung für Eintaktflusswandler							
Wp							
<input checked="" type="radio"/> Runddräh	Fbreite/mm	Fbreite/Mleit	Vgrad	Nparallel	Wp id	Fhöd/mm	Fhoehe/mm
<input type="radio"/> Flachban	21,500	1,000	4.000	1.000		0,055	0,050
					Pcup/W		1,033
Ws							
<input checked="" type="radio"/> Runddräh	Fbreite/mm	Fbreite/Mleit	Vgrad	Nparallel	Ws id	Fhöd/mm	Fhoehe/mm
<input type="radio"/> Flachban	21,500	1,000	4.000	2.000		0,114	0,100
					Pcus/W		1,143

Übertemperaturen		Entwicklungszeit optimieren	DTke/K	DTwi/K
Pfe/W	Pcu/W		40,327	53,003
5,326	2,176	Übertemperaturen		

#### **frmKernauswahl**

**Drucken**

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Drucken

Ende

### Transformer construction “Infineon/ Reso/ 1kW/ 200kHz”

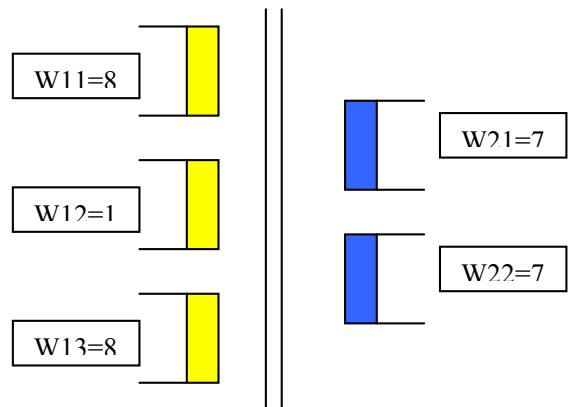
Core: ETD44/ N87

Airgap: 0mm

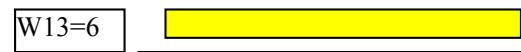
Transformation coefficient:  $\dot{U}=4,29$

Windungsverhältnis: 30:7

Circuit:



W1 (primary) series connection (on PCB)



W2 (secondary) parallel connection (on PCB)



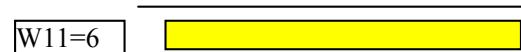
Windings: Copper - Foil, Width: b=21,5mm



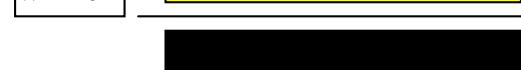
Thickness: W1: d=50 µm



Thickness: W2: d=100 µm



4 fold overlapping windings



Core

Layout:

Transformer bobbin (18 Pins), EPCOS-Nr. B66366-B1018-T1

Top View

Inductance:

$W_{11} = 224 \mu H$

$W_{12} = 686 \mu H$

$W_{13} = 224 \mu H$

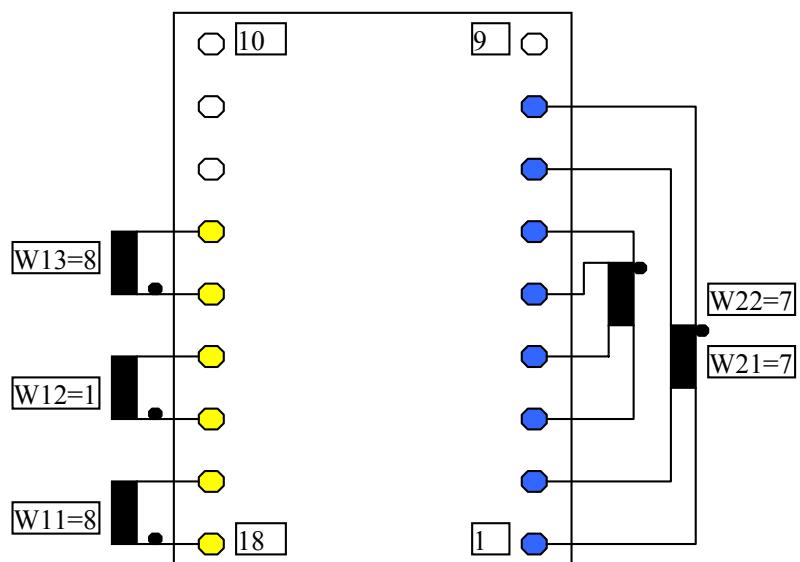
$W_{1\text{tot}} = 3150 \mu H$

$W_{21} = 171,5 \mu H$

$W_{22} = 171,5 \mu H$

$W_{2\text{tot}} = 171,5 \mu H$

Toleranz: +30/-20%



## G1 Schematics of the demo board

