Utilization Of An Active-Clamp Circuit To Achieve Soft Switching In Flyback Converters

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ABSTRACT - **Flyback derived topologies are attractive because of their relative simplicity when compared with other topologies used in low power applications. Incorporation of active-clamp circuitry into the flyback topology serves to recycle transformer leakage energy while minimizing switch voltage stress. The addition of the active-clamp circuit also provides a mechanism for achieving zero-voltage-switching (ZVS) of both the main and auxiliary switches. ZVS also limits the turn-off di/dt of the output rectifier, reducing rectifier switching losses and switching noise due to diode reverse recovery.**

I. INTRODUCTION

The flyback topology has long been attractive because of its relative simplicity when compared with other topologies used in low power (up to several hundred watts) applications. The flyback "transformer" serves the dual purpose of providing energy storage as well as converter isolation, theoretically minimizing the magnetic component count when compared with, for example, the forward converter. A drawback to the use of the flyback is the relatively high voltage and current stress suffered by its switching components. High peak and RMS current stress is a particular problem for flybacks when operating in discontinuous conduction mode (DCM) and is in fact a primary detriment to increasing output power. An addition, high turn-off voltage (caused by the parasitic oscillation between the transformer leakage inductance and the switch capacitance) seen by the primary switch traditionally requires the use of a RCD clamp to limit the switch voltage excursion. Unfortunately, in this scheme the energy stored in the transformer leakage is dissipated in the clamp resistor, resulting in a difficult design trade-off between clamping action and clamp circuit power dissipation.

The limitations presented by the RCD clamp can be largely overcome by replacing the passive clamp with an active-clamp circuit as shown in Figure 1. The active-clamp circuit provides the benefits of recycling the transformer leakage energy while minimizing turn-off voltage stress across the power switch. In addition, the active-clamp circuit provides a means of achieving zero-voltage-switching (ZVS) for the power switch and subsequent lowering of the output rectifier di/dt. This results in decreased rectifier switching loss and output switching noise. To achieve soft-switching characteristics over a useful operating range, the addition of a small resonant inductor in the active-clamp loop is usually necessary (see Fig. 1).

The use of the active-clamp circuit to achieve soft switching in DCM flybacks is well documented [1,2,3]. In DCM operation, the transformer magnetizing inductance (in conjunction with the active-clamp circuit) is used to discharge the primary switch capacitance and achieve ZVS. However, for higher output power operation, it is more desirable to operate in CCM to reduce device current stress [4,5]. As will be demonstrated, ZVS can still be realized in CCM by utilizing the energy stored in the resonant inductor. The presence of the resonant inductor also helps to softly commute the turn-off of the output rectifier, resulting in reduced output noise and rectifier switching losses. This would be a particular advantage in high output voltage applications where slower rectifiers are more likely to be used.

This paper presents evaluation of a constant-frequency, soft-switching, active-clamp flyback converter for DC/DC conversion applications. The basic principle of operation is analyzed and a design procedure is developed. Experimental results are then

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presented which illustrate converter function and verify the analysis presented.

II. ACTIVE-CLAMP FLYBACK CONVERTER OVERVIEW

The incorporation of an active-clamp circuit into the basic flyback topology is shown in Fig. 1. In the figure, the flyback transformer has been replaced with an equivalent circuit model showing the magnetizing and leakage inductances (L_r represents the total transformer leakage inductance reflected to the primary in addition to any external inductance). Switches S1 and S2 are shown with their associated body diodes. C_r represents the parallel combination of the parasitic capacitance of the two switches. It is this device capacitance resonating with L_r which enables ZVS for S1. With the active-clamp circuit, the transistor turn-off voltage spike is clamped, the transformer leakage energy is recycled, and zero-voltage-switching (ZVS) for both primary (S1) and auxiliary (S2) switches becomes a possibility. These advantages come at the expense of additional power stage components and increased control circuit complexity (two switches as opposed to the usual one switch).

Figure 2 illustrates the topological states and Fig. 3 the key waveforms for the active-clamp flyback converter. For this description of circuit operation (and for the subsequent development of a design procedure in the next section), the following assumptions are made:

- ideal switching components;
- steady-state CCM operation;
- L_r (includes the transformer leakage inductance) is much less than the transformer magnetizing inductance, L_m (typically 5% to 10% of L_m);
- sufficient energy is stored in L_r to completely discharge C_r and turn on S1's body diode;
- and, $\pi\sqrt{L_r C_{clamp}} >> T_{off}$.

The last assumption simply states that one-half the resonant period formed by L_r and C_{clamp} is much longer than the maximum off time of S1 ($T_{off} \cong (1-D)T_S$). The sequence of topological states

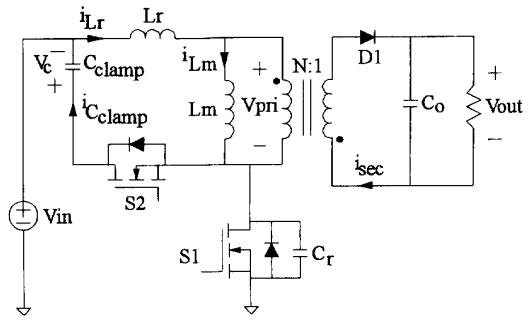

Fig. 1 Simplified schematic of the active-clamp flyback converter.

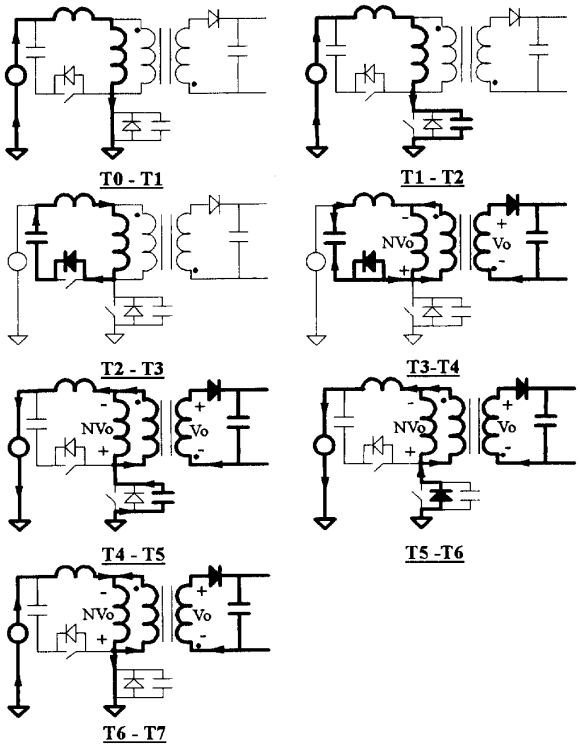

Fig. 2 Active-clamp flyback topological states.

is described below:

T0 - T1: At T_0, switch S1 is on, and the auxiliary switch, S2, is off. The output rectifier, D1, is reversed biased as is the anti-parallel diode of S2. The magnetizing inductance (along with the resonant

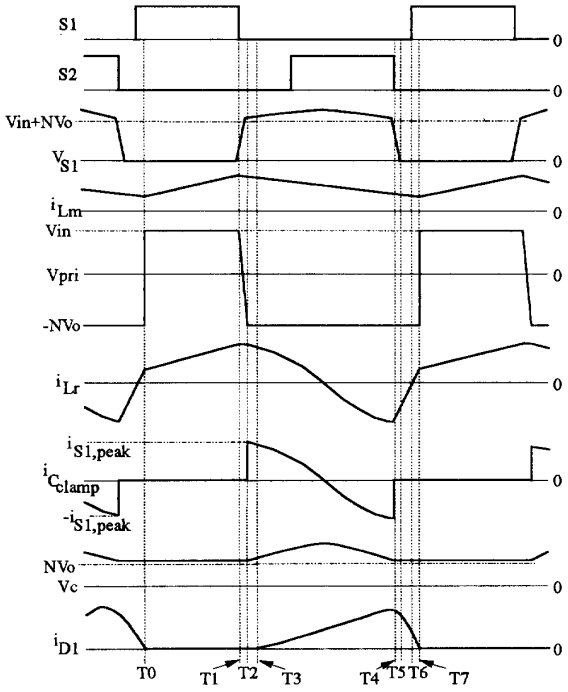

Fig. 3 Active-clamp flyback steady-state waveforms.

inductance) is being linearly charged just as it would be during the inductor charging phase in "normal" flyback operation.

T_1 - T_2: S1 is turned off at T_1. C_r is charged by the magnetizing current (which is also equal to the current through the resonant inductor). C_r is actually charged in a resonant manner, but the charge time is very brief, leading to an approximately linear charging characteristic.

T_2 - T_3: At T_2, C_r is charged ($V_{DS} = V_{in} + V_c$) to the point where the anti-parallel diode of S2 starts to conduct. The clamp capacitor fixes the voltage across L_r and the transformer magnetizing inductance to V_c ($\cong NV_o$), forming a voltage divider between the two inductances. Since C_{clamp} is much larger than C_r, nearly all of the magnetizing current is diverted through the diode to charge the clamp capacitor. Consequently, V_{pri} decreases according to:

$$V_{pri} = -V_c \frac{L_m}{L_r + L_m}. \qquad (1)$$

T_3 - T_4: At T_3, V_{pri} has decreased to the point where the secondary transformer voltage is sufficient to forward bias D1. The transformer primary voltage is then clamped by the (very large) output capacitance to approximately NV_o. L_r and C_{clamp} begin to resonate. In order for S2 to achieve ZVS, the device should be turned on before $i_{C_{clamp}}$ reverses direction.

T_4 - T_5: The auxiliary switch, S2, is turned off at T_4, effectively removing C_{clamp} from the circuit. A new resonant network is formed between the resonant inductor and the MOSFET parasitic capacitances. The transformer primary voltage remains clamped at NV_o as C_r is discharged.

T_5 - T_6: Assuming the energy stored in L_r is greater than the energy stored in C_r, at T_5 C_r will be sufficiently discharged to allow S1's body diode to start conducting. The voltage across the resonant inductor becomes clamped at $V_{in} + NV_o$. This also fixes the rate of decay of the output rectifier current to:

$$\frac{di_{D1}}{dt} = -N\left(\frac{NV_o}{L_m} + \frac{V_{in} + NV_o}{L_r}\right). \qquad (2)$$

For $L_m >> L_r$ Eq. (2) simplifies to:

$$\frac{di_{D1}}{dt} \cong -N\frac{V_{in} + NV_o}{L_r}. \qquad (3)$$

It is during this interval that switch S1 can be turned on under zero-voltage conditions.

T_6 - T_7: S1 is on, and the secondary current is decreasing as the resonant inductor current increases. At T_7, the secondary current decreases to zero (because the resonant inductor current has equaled the magnetizing current), and D1 reverse biases, allowing the polarity to reverse on the transformer primary. The magnetizing and resonant inductances begin to linearly charge again, starting another switching cycle ($T_7 = T_0$).

Note that the length of the time intervals T_1 to T_3 and T_4 to T_7 have been greatly exaggerated in Fig. 3 in order to more clearly show the transition periods.

III. SOFT-SWITCHING FLYBACK DESIGN CONSIDERATIONS

For the purposes of ZVS of S1, there must be assurance that the switch is turned on during the T_5 to T_6 time interval. If not, the resonant inductor current reverses (becoming positive again), recharging C_r, and ZVS is lost (or at least partially lost). Therefore, the delay time between the turn off of S2 and the turn on of S1 is critical to ZVS operation. The optimum value of this delay is one-quarter of the resonant period formed by L_r and C_r:

$$T_{delay} = \frac{\pi}{2}\sqrt{L_r C_r} \tag{4}$$

Strictly speaking, the value of C_r is a function of applied voltage (particularly at small drain-to-source voltages), but Eq. (4) simplifies matters by assuming that it is not.

In addition to the S1/S2 timing requirement there must also be sufficient energy stored in the resonant inductor to completely discharge the switch capacitance. This requirement is valid at time instant T_4 (when S2 is turned off):

$$E_{L_r} \geq E_{C_r}\Big|_{@\,S2\ turn\ off} \tag{5}$$

It should be noted that even if insufficient energy is stored in L_r to completely discharge the switch capacitance, meeting the timing requirement called for in Eq. (4) guarantees switching with the minimum possible voltage stress for the given operating condition.

Equation (5) can be used to develop a design equation determining an appropriate resonant inductor value that realizes ZVS at a desired operating point. This will be detailed in the section concerned with the design of L_r.

CCM-ZVS Active-Clamp Flyback Design Procedure:

1) Select flyback transformer inductance: The presence of the active-clamp circuit does not significantly alter the primary switch current waveform from that of a seen in standard CCM flyback designs. Therefore, the usual methods of determining the appropriate value of magnetizing inductance can be used. Of course, the peak switch current is heavily influenced by the amount of allowed inductor ripple current. This is usually expressed as some percentage of the maximum average inductor current (occurring at maximum load and minimum line) so as to limit peak switching currents. The value chosen for L_m also determines the CCM/DCM boundary operating point:

$$P_o^{CCM} \geq \frac{1}{2}\frac{\eta(V_{in}D)^2}{L_m F_S}, \tag{6}$$

where η is the converter efficiency and F_S is the switching frequency.

2) Select transformer turns ratio: The transformer turns ratio is chosen to accommodate as low a voltage rating for the switching devices as possible while still being able to realize a reasonable range of duty cycles over the input line range. Assuming that the active clamping provides for perfect voltage clamping across the primary switch (i.e., no overshoot), then the maximum off-state voltage appearing across S1 and S2 is given by:

$$V_{S1,S2}^{max} \approx V_{in}^{HL} + NV_o + \frac{2L_r F_S P_o^{max}}{\eta V_{in}^{HL} D^{HL}\left(1-D^{HL}\right)}. \tag{7}$$

The last part of the expression in Eq. (7) is the value of the voltage developed across L_r. Although an explicit value of the resonant inductor hasn't yet been determined, for the purposes of estimating the maximum voltage stress on S1 and S2 a value of $L_m/10$ can be used as a conservative design guideline. Also, the converter duty cycle is approximately the same as for a traditional flyback operating in CCM. However, with the addition of L_r the effective duty cycle (as defined by the charge and discharge cycle of the flyback inductor) is slightly less than switch S1's duty cycle:

$$D_{eff} = D_{S1} - \Delta D \cong D_{S1} - \frac{1}{D_{S1}}\frac{2L_r P_o F_S}{(V_{in}+NV_o)V_{in}}. \tag{8}$$

Eq. (8) is approximate in that it assumes lossless switching.

3) Design resonant inductor: After the value of L_m has been fixed the resonant inductor can be designed. As

mentioned previously, it is assumed its value will be a small fraction of L_m. For a given converter operating point and value of C_r, achieving ZVS requires that L_r be of sufficient size to completely discharge the switch capacitance. At time instant T_4, from Eq. (5):

$$I_{S1,peak} = I_{L_r,peak} \geq V_{C_r}\sqrt{\frac{C_r}{L_r}}, \qquad (9)$$

where the peak primary switch current is

$$I_{S1,peak} \cong \frac{P_o}{\eta V_{in} D} + \frac{1}{2}\frac{V_{in} D}{L_m F_S}. \qquad (10)$$

The difficulty in solving Eq. (9) for L_r is the fact that the resonant capacitor voltage (V_{Cr}) is a function of the value of L_r. However, in a practical design situation, the resonant inductor voltage at T_4 is relatively small (compared to $V_{in} + NV_o$) and Eq. (9) can be solved for an approximate minimum value of L_r necessary to achieve ZVS:

$$L_r|_{ZVS} \geq \frac{C_r(V_{in} + NV_o)^2}{I_{S1,peak}^2}. \qquad (11)$$

In applications requiring high output voltage, it may be more desirable to specifically tailor the soft-switching characteristics of the output rectifier than to necessarily realize ZVS of the primary switch. In this case Eq. (3) may be the more important design criteria for the resonant inductor.

The RMS current carried by L_r can be estimated from Eq. (12):

$$I_{L_r,RMS} \approx \sqrt{\frac{\left(\frac{P_o}{\eta V_{in} D}\right)^2 (2D+1) + \frac{P_o D}{\eta L_m F_S}(1-D) + \frac{1}{4}\left(\frac{V_{in} D}{L_m F_S}\right)^2}{3}}$$

The expression for this current is complicated by the fact that the resonant inductor carries both primary switch and circulating clamp current.

4) Select auxiliary switch: For the purposes of estimating the required current rating of S2, advantage is taken of the assumption that the L_r-C_{clamp} resonant period is much longer than the off time of S1. Under this assumption the current through S2 (same as $i_{C_{clamp}}$) approximates a sawtooth waveform with endpoint currents equal to the peak current through S1 (see Fig. 3). The MOSFET body diode conducts clamp current for half the S2 on time with the MOSFET itself conducting current for the remaining half of the cycle. Therefore, the worst case maximum currents seen by both the MOSFET and its body diode are approximately:

$$\underline{\text{S2 MOSFET}}: \quad I_{S2,RMS}^{max} \approx I_{S1,peak}^{max}\sqrt{\frac{1-D^{LL}}{6}}, \qquad (13)$$

and

$$\underline{\text{S2 body diode}}: \quad I_{S2,AVG}^{max} \approx I_{S1,peak}^{max}\frac{1-D^{LL}}{4}, \qquad (14)$$

where the peak primary switch current can be obtained from Eq. (10).

5) Select clamp capacitor: Choosing the value of clamp capacitance is done based on the design of L_r. The resonant frequency formed by the clamp capacitor and the resonant inductor should be sufficiently low so that there is not excessive resonant ringing (and hence voltage overshoot) across the power switch when the switch is turned off. However, using too large a value of clamp capacitance yields no improvement in clamping performance at the expense of a larger (more costly and bulky) capacitor. A good compromise for design purposes is to select the capacitor value so that one-half of the resonant period formed by the clamp capacitor and resonant inductance exceeds the maximum off time of S1. Therefore:

$$C_{clamp} >> \frac{(1-D^{HL})^2}{\pi^2 L_r F_S^2}. \qquad (15)$$

The capacitor voltage rating has to exceed NV_o by the amount of voltage dropped across L_r:

$$V_{C_{clamp}}^{max} \approx NV_o + \frac{2L_r F_S P_o^{max}}{\eta V_{in}^{HL} D^{HL}\left(1-D^{HL}\right)}. \qquad (16)$$

The required ripple current rating for the capacitor is:

$$I_{C_{clamp},RMS}^{max} \approx I_{S1,peak}^{max}\sqrt{\frac{1-D^{LL}}{3}} \qquad (17)$$

Eq. (17) was derived using the same simplifying assumption used to derive Eqs. (13) and (14).

6) Choose output rectifier: The maximum theoretical reverse voltage seen by the output rectifier in the active-clamp flyback is the same as for a standard flyback design. However, the rectifier current is another matter. Due to the presence of the clamp circuit, the secondary current is discontinuous in shape even though the flyback inductor is operating in CCM. This is illustrated in Fig. 3. The result is much higher peak secondary currents than would normally be expected in CCM operation:

$$I_{D1,peak}^{max} \approx \frac{2P_o^{max}}{V_o(1-D^{LL})}. \qquad (18)$$

The average rectifier current is just the load current. As was pointed out previously, the addition of L_r reduces the rate of diode turn-off di/dt. This improves rectifier switching losses and converter noise levels (see Figs. 6 through 8).

7) Select output capacitor(s): The principle factor affecting the value of output capacitance is utilization of enough capacitance to meet device ripple current ratings:

$$I_{C_o,RMS}^{max} \approx \frac{P_o^{max}}{V_o}\sqrt{\frac{1+3\left(D^{LL}\right)^2}{3\left(1-D^{LL}\right)}}. \qquad (19)$$

Theoretically, the capacitance value would be selected based on output voltage ripple specifications. However, in practice, meeting the RMS current rating called for in Eq. (19) sets a lower limit on an amount of capacitance that usually easily meets any ripple voltage specification.

8) Design flyback transformer: Still constrained by the assumption that $L_r << L_m$, the transformer design for the active-clamp flyback is no different than that for a traditional CCM flyback, except the primary and secondary RMS currents are somewhat different. The transformer secondary and output rectifier RMS currents are equivalent, so:

$$I_{sec,RMS}^{max} = I_{D1,RMS}^{max} \approx \frac{2P_o^{max}}{V_o\sqrt{3\left(1-D^{LL}\right)}}. \qquad (20)$$

The transformer primary current is identical to the resonant inductor current, consequently its RMS value is given by Eq. (12).

IV. EXPERIMENTAL RESULTS

To experimentally characterize the soft-switching properties of the active-clamp flyback converter, a breadboard was constructed to the specifications listed below:

- input voltage: 100 VDC
- output voltage: 48 VDC
- output power: 500 W maximum
- switching frequency: 100 KHz

Using the design procedure discussed in the previous section as a guide, the experimental converter was constructed using the following components:

- Transformer:
  core: Toshiba PC40ETD49-Z
  primary: 45T of 3 strands of 150/42 Litz wire
  secondary: 15T of 5 strands of 150/42 Litz wire
  L_m: 215 μH, L_{leak} (referred to primary): 2.3 μH
- Resonant inductor:
  core: MPP 55530
  winding: 8T of 10 strands of AWG 26
  L_r: 7 μH (with no bias)
- Clamp circuit:
  C_{clamp}: 2.2 μF, 250 V
  S2: IRFP360
- S1: IRFP360
- Output stage:
  D1: 2 x BYV44-500
  C_o: 3 x 2200 μF, 100 V Aluminum electrolytic

For the experimental circuit the DCM/CCM operating point boundary was about P_o = 84 W and ZVS was realized above 145 W. Fig. 4 compares experimental efficiencies using an RCD clamp with no resonant inductor and the active-clamp circuit with L_r = 7 μH (all

other circuit parameters are identical). It can be seen that the active-clamp circuit yields an improvement of at least 4% in power stage efficiency. Maximum output power for the RCD clamped power stage is about 200 W due to power dissipation limitations in the clamp resistor.

Figures 5 and 6 are experimental waveforms pertinent to illustrating the converter's soft-switching characteristics. Figure 5 displays S1's gate drive voltage, the resonant inductor current, and S1's drain-to-source voltage. Operation is at P_O = 300 W. Figure 6 compares the output rectifier current with and without L_r in the circuit. The operating point of the converter is identical for both cases (P_O = 300 W, ZVS with L_r, hard switching without it). As can be seen from the figure, with the resonant inductor the rectifier reverse recovery current characteristic is substantially improved. Not only is switching loss in the diode decreased, but the output voltage high-frequency (HF) noise is reduced. This is illustrated in Figs. 7 and 8 which show the output voltage noise spectrum with and without L_r. In particular, the noise levels in the frequency range of about 2.5 to 3 MHz show a reduction of nearly 20 dB between the two cases. Coincidentally, HF noise in the range of about 2 to 5 MHz is typically very difficult to filter because the frequency is somewhat low for effective use of ferrite beads and is too high for standard capacitive bypassing.

Another attractive usage for the active-clamp circuit is as a low-loss turn-off snubber when using an IGBT as

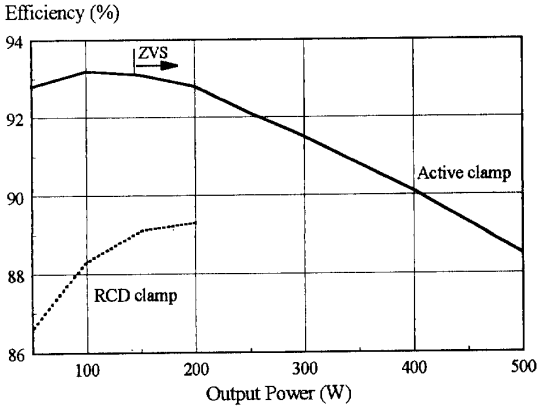

Fig. 4 Efficiency comparison between RCD and active-clamp configurations. For RCD clamp, R = 4.7 KΩ, 10 W and C = 2.2 μF.

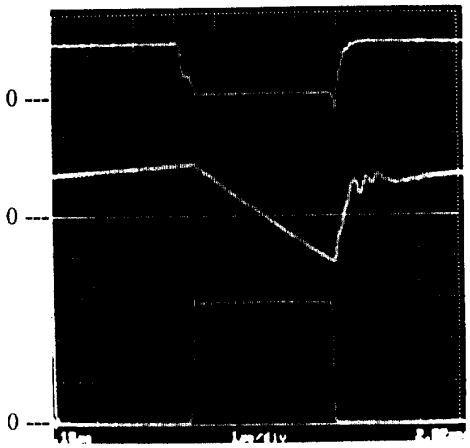

Fig. 5 ZVS active-clamp flyback experimental waveforms. Top trace: $V_{gs,S1}$ @ 15 V/div.; middle trace: I_{Lr} @ 5 A/div.; bottom trace: $V_{ds,S1}$ @ 100 V/div. Time scale is 1 μs/div.

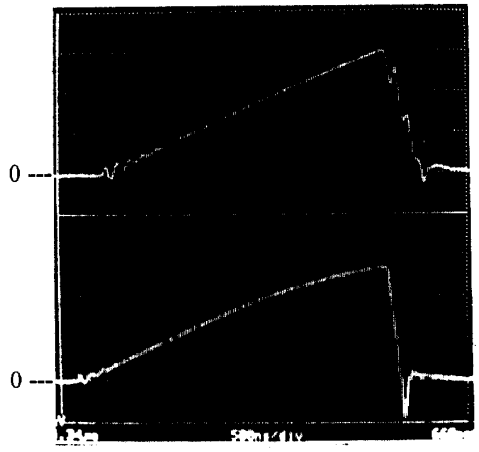

Fig. 6 Output rectifier current waveforms @ 10 A/div. Top trace: L_r = 7 μH; bottom trace: $L_r = L_{leak} \approx$ 2 μH. Time scale is 500 ns/div.

the primary switch device (S1). IGBTs have superior conduction characteristics compared to MOSFETs (of the same voltage rating). The drawback to the use of IGBTs is that they display excessive turn-off losses as their switching frequency is increased. The severity of this problem can be reduced by adding an external capacitor (C_r) from the collector to the emitter of the IGBT to slow down the rate of increase in collector

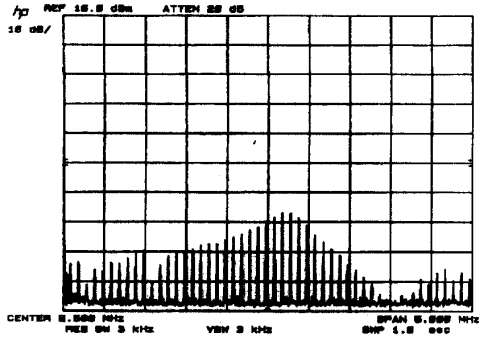

Fig. 7 Output voltage noise, $L_r = L_{leak}$.

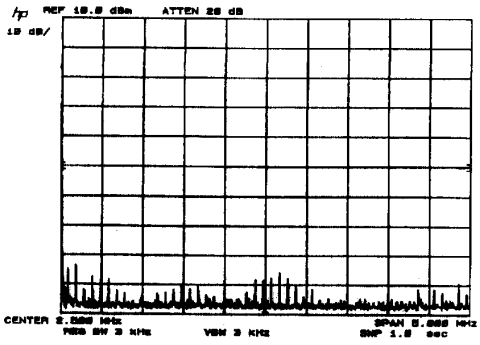

Fig. 8 Output voltage noise, $L_r = 7\ \mu H$.

voltage as the device turns off. This allows time for the device current to tail to zero without excessive device voltage being present. Subsequently, before S1 is turned on, the resonant inductor discharges C_r so that its stored energy is not dissipated in the IGBT at device turn on.

Experimental results comparing power stage efficiencies using an IGBT with and without external capacitance is shown in Fig. 9. With C_r = 3000 pF the efficiency is improved by about 1% over most of the load range. The ZVS range for each case is marked on the curves.

VI. CONCLUSION

This paper has presented the analysis, design, and experimental results for a high-efficiency 500 W flyback DC/DC converter employing active-clamp circuitry. The incorporation of the active-clamp circuit into the basic flyback topology provides a mechanism for

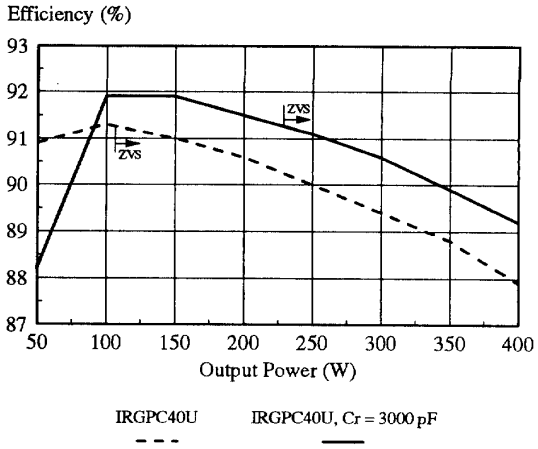

Fig. 9 Efficiency comparison using IGBT primary switch with and without turn-off capacitor.

achieving ZVS for both the primary and auxiliary switches and soft commutation of the output rectifier while operating in CCM. CCM operation is desirable as power levels of several hundred watts can realize higher efficiencies than when compared with DCM operation.

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