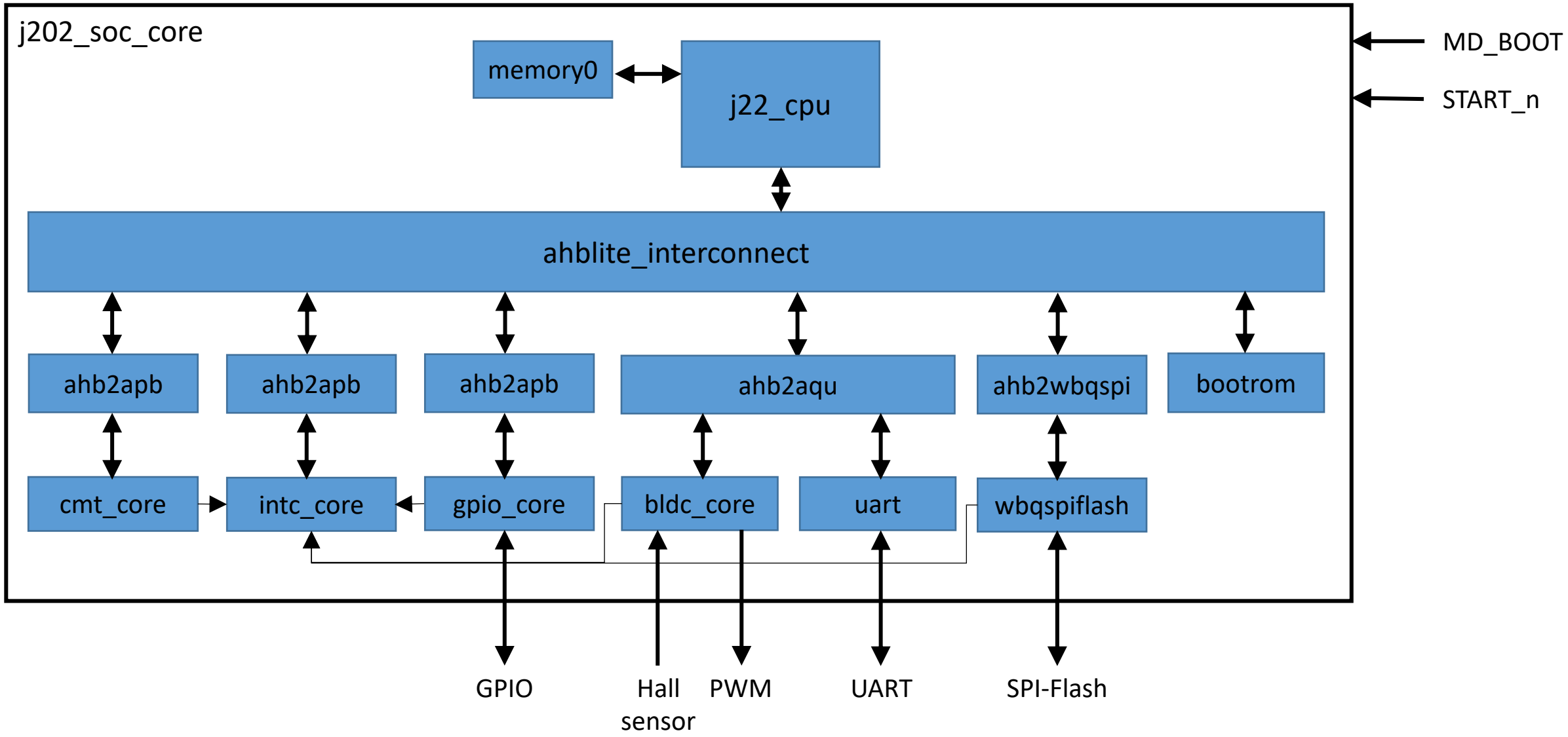
j202_soc_core
memory0
j22_cpu
MD_BOOT
START_n
ahblite_interconnect
ahb2apb
ahb2apb
ahb2apb
ahb2aqu
ahb2wbqspi
bootrom
cmt_core
intc_core
gpio_core
bldc_core
uart
wbqspiflash
GPIO
Hall sensor
PWM
UART
SPI-Flash

Address Map

md_boot[1:0] = 00, 11		01		10				
Start	End	Start	End	Start	End	Size	Peripheral / Memory	Comment
fff80000	fff87fff	00000000	0003ffff	fff80000	fff87fff	32KB	memory0	Local RAM(TCM0)
20000000	20ffffff	←	←	00000000	00ffffff	16MB	qspi_flash	SPI-Flash
21000000	2100000f	←	←	01000000	0100000f	16B	wbqspiflash	SPI-Flash Controller
00000000	0003ffff	30000000	3003ffff	←	←	256KB	bootrom	Boot-ROM
abcc0000	abcc0fff	←	←	←	←	4KB	cmt_core	Compare Match Timer
abcc1000	abcc1fff	←	←	←	←	4KB	intc_core	Interrupt Controller
abcc2000	abcc2fff	←	←	←	←	4KB	gpio_core	GPIO
abcd0000	abcd00ff	←	←	←	←	256B	bldc_core	PWM
abcd0100	abcd01ff	←	←	←	←	256B	uart	UART

IPs from other developers

- AHB to Wishbone Bridge

  https://opencores.org/projects/ahb2wishbone

- Quad SPI Flash Controller

  https://opencores.org/projects/qspiflash