Detailed Explanation of the hardware of the FPGA Student Development Board

The hardware of the development board kit is the basis for ensuring experimental learning. This part of the content is mainly for the hardware part.

A brief description, which can be read or checked appropriately, especially when it comes to information such as hardware interface definitions, to understand this

Part of the content is necessary. At the same time, it can be used with reference to the hardware schematic diagram included with the CD-ROM.

1. FPGA Student Development Board Hardware

1.1 General introduction

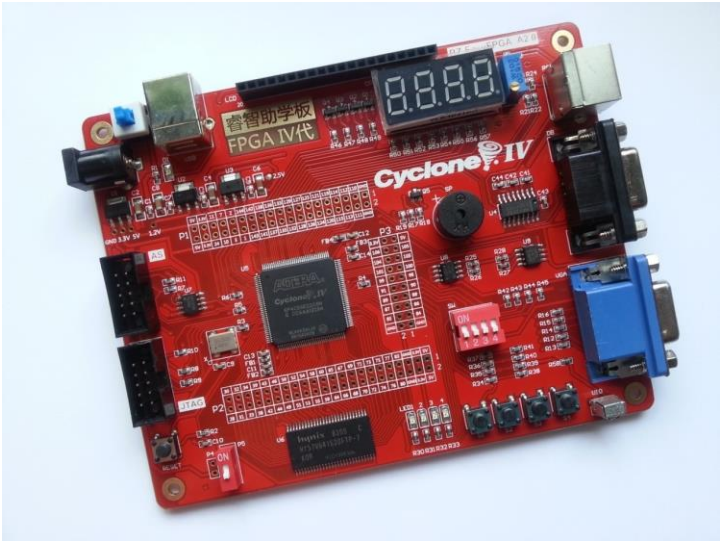


Figure 1 Real shot of the hardware of the student development board

Main hardware resources

1. The main chip adopts ALTERA's latest fourth-generation FPGA, CycloneIV series EP4CE6E22C8N
2. On-board EPCS4N/EPCS16 large-capacity serial configuration chip, support JTAG/AS mode
3. Onboard 64MbitSDRAM, support SOPC, NIOSII development (many low-priced boards do not have SDRAM, cannot support NIOS (SOPC development)
4. On-board 50MHz active crystal oscillator, which provides the system's working master clock
5. Adopts 1117-3.3V voltage stabilizer chip to provide 3.3V voltage output
6. Adopts 1117-1.2V voltage stabilized chip to provide FPGA core voltage
7. Adopts 1117-2.5V voltage stabilizer chip to provide PLL voltage
8. Careful decoupling design, using a large number of decoupling capacitors
9. Provide 5V DC power socket
10. Provide square port USB interface power socket
11. A system reset button, Reset, can also be used as a user input button

12. Self-locking button power switch
13. LED power indicator light
14. Well-designed allocated IO resources, all IO leads, 3 expansion interfaces, general 2.54mm spacing, you can expand by yourself
15. The corresponding downloaded file for the JTAG download interface is. SOF, fast speed, it is recommended to use this interface for normal learning
16. The file corresponding to the AS download interface is. POF, the speed is slow, and it is recommended to use it when curing procedures are required.

Enrich peripheral resources

1. There are 4 independent buttons on board, which can be used for button control, basic experiments in digital logic, etc.
2. Onboard 4-digit LED light-emitting diodes, which can be used for LED control, basic experiments in digital logic, etc.
3. Onboard 4-digit digital tube, frequency meter, stopwatch
4. Onboard 4-digit dip code switch, which can be used for experiments such as switch control
5. Equipped with 1X20 LCD screen row seat, support LCD1602, LCD12864, TFT LCD screen (not included LCD, need to be purchased separately)
6. Precision adjustable resistance to adjust the LCD backlight
7. Onboard 1 buzzer, which can be used for sound and music experiments
8. PS2 interface, PS/2 keyboard experiment can be done
9. Onboard brand new original imported temperature sensor chip LM75A, which can be used for thermometer experiments
10. RS232 serial port, serial communication experiment can be done
11. VGA interface, can do display experiments, etc.
12. I2C serial EEPROM AT24C08, do IIC bus experiment
13. Infrared receiving module

1.2 IO allocation of FPGA

The hardware design of FPGA is still different from that of single-chip microcomputer, ARM or DSP. The IO function of MCU is usually fixed, and the function of a certain pin is required by the Datasheet. But the FPGA is different. In comparison, its IO is more flexible and free. Of course, the dedicated pins of the FPGA should be in accordance with the datasheet standards, and the connection of the general IO can be defined by itself. For example: when assigning pin functions, the FPGA The definition of the general IO function can be determined by yourself. If you want this pin to be connected to the LED, then connect to the LED, and if you want to connect to the digital tube, then connect to the digital tube. The final solution may be based on the board PCB layout, functional compatibility, etc. Considering it comprehensively, it can also be properly adjusted during the PCB routing process.

If you look at our Wisdom Student Development Board, it is actually an example. We concentrated on using about 38 iOS for SDRAM, and all the other iOS were drawn out and made into expansion holes with standard spacing of 2.54mm. Through these holes, they were connected to other peripherals. If you want to build other peripherals by yourself, just solder the pins or sockets, and connect them to your peripherals with DuPont wires or other connectors. The picture below shows the real shots of the three extended IO (the white numbers are the corresponding IO pin numbers):

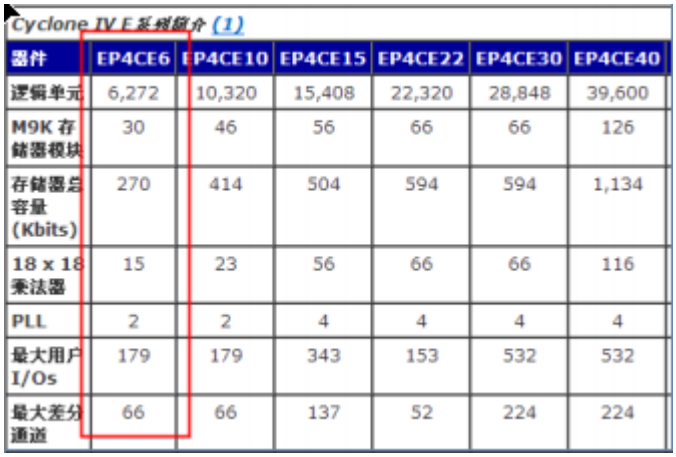
Figure 2 Real shot of the main chip IO expansion

2. Schematic diagram of Wisdom FPGA Student Development Board

2.1 FPGA Main Chip

The FPGA chip uses CycloneIV E series EP4CE6E22C8N, which is rich in resources and affordable. It is especially suitable for FPGA junior and senior learning. The on-board real shots and the internal resources of the chip are shown in Figure 3 and Figure 4 below.

Figure 3 Real shot of the main chip



Cyclone IV E 系列简介 (1)

器件	EP4CE6	EP4CE10	EP4CE15	EP4CE22	EP4CE30	EP4CE40
逻辑单元	6,272	10,320	15,408	22,320	28,848	39,600
M9K 存储器模块	30	46	56	66	66	126
存储器总容量 (Kbits)	270	414	504	594	594	1,134
18 x 18 乘法器	15	23	56	66	66	116
PLL	2	2	4	4	4	4
最大用户 I/Os	179	179	343	153	532	532
最大差分通道	66	66	137	52	224	224

Figure 4 Screenshot of EP4CE6 series chip resources

For more instructions and introductions about this chip, you can find it on Altera's official website.,

http://www.altera.com.cn/devices/fpga/cyclone-iv/overview/cyivoverview.html#table1

Usually, the number of logic units on the chip is an important reference index, and EP4CE6E22C8N is enough for beginners to use. For the schematic diagram of the main FPGA chip, please refer to the schematic diagram in PDF format on the supporting CD-ROM, which can be enlarged for reference.

2.2 Memory SDRAM circuit

The student development board comes with SDRAM, so the student development board fully supports SOPC and NIOSII development. If there is no SDRAM, it is very difficult to run a slightly larger NIOSII program. The selected SDRAM chip HY57V641620 has a capacity of 64Mbit. SDRAM is used for expansion. It can be used as the RAM of the NIOS II processor to run programs, or as other applications that require large amounts of real-time data storage. As long as the SDRAM circuit connects the address bus, data bus, and control bus to the I/O port of the FPGA, the power supply part of the SDRAM is filtered using multiple 104 capacitors to ensure the stability of the chip's working power supply.

The SDRAM schematic diagram is shown in Figure 5 ：

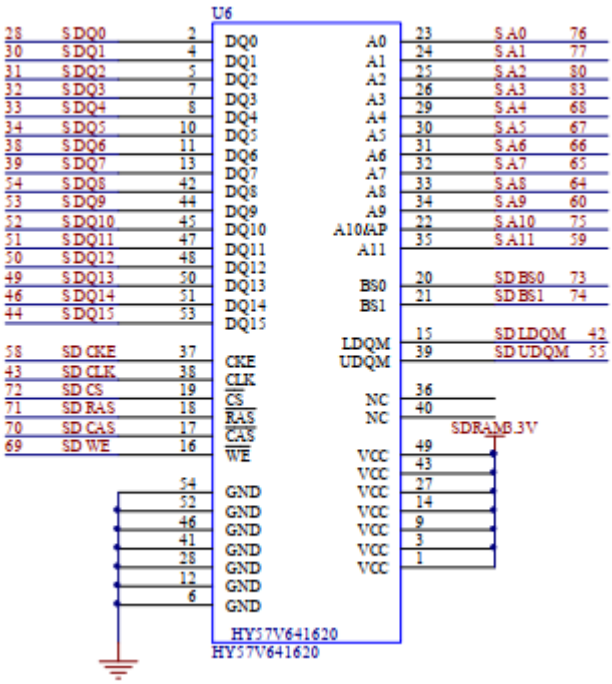


Figure 5 SDRAM schematic diagram

Reminder: On the old version of the PCB, there is a one-digit dial switch on the left side of the SDRAM chip. This function is to control the power supply of the SDRAM. See Figure 6 ：

Figure 6 SDRAM and power supply

Now in the newly released version, this dial switch has been removed.

2.3 Power supply circuit

The power supply is the most important part to ensure the normal operation of the entire development system. There are three types of power supplies for the student development board: 3.3V, 2.5V, and 1.2V

3.3V is mainly used to power all IO ports, memory circuits, serial configuration devices, reset circuits, and LEDs of FPGAs.

2.5V is required for the PLL power supply for JTAG circuits and FPGAs

1.2V provides the core operating voltage of the FPGA.

The power input can be powered by USB, or an external 5V power supply can be used. D1 is the working indicator light of the entire circuit board. In the upper left corner of the PCB board, the schematic diagram of the power supply part is shown in Figure 7, Figure 8 is a schematic diagram of the three voltages.

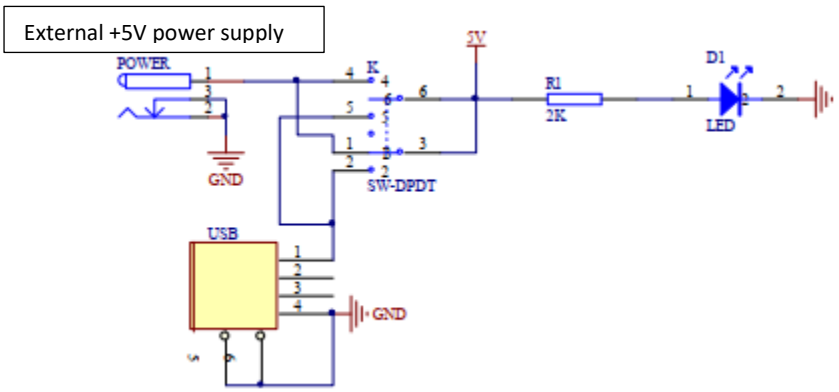


Figure 7 Schematic diagram of the power input part

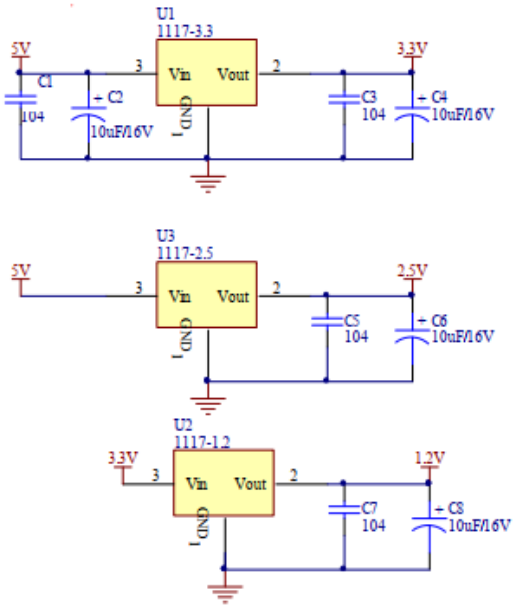


Figure 8 Three voltage circuits

2.4 JTAG download and configure circuit

There are three types of configuration download methods for FPGA devices: active configuration method (AS), passive configuration method (PS), and the most commonly used (JTAG) configuration method. Here we only discuss the JTAG and AS methods:

The JTAG mode is to directly put the program through the JTAG interface when it is powered on (under the Altera platform. sof file, SRAMObjectObjectFileFile) is downloaded to the FPGA. Because the FPGA is based on the SRAM structure, the program that was just downloaded after the power failure is lost, and the program must be downloaded again after power-on before it can be run. The JTAG download speed is very fast. When using usb blaster to download, everyone will observe that the download process is basically completed within 1-2 seconds.

AS programming mode is to compile the generated object file (under the Altera platform) through the Blaster cable

It is a .pof file, Programming Object File) programmed into the configuration chip. The configuration chip is usually a dedicated Flash used in conjunction with the FPGA, and the number after EPCS represents the bit width. Once the program is burned into the configuration chip, the FPGA will automatically download the program from the configuration chip when the board is powered on

According to the above statement, the size of the .sof file is related to the model of the FPGA, and the size of the .pof file is related to the model of the configuration chip.

In general circuits, the AS+JTAG method is usually used, so that the JTAG method can be used for debugging. Finally, after the program has been debugged correctly, the AS mode is used to burn the program to the configuration chip. In fact, JTAG can also complete the programming of EPCS chips, as long as you can use the tools that come with Quartus to generate JIC files that can be used in JTAG mode to download. In this way, we found a problem: when the AS mode cannot be downloaded, we can use the JIC file downloaded in JTAG mode to verify whether the configuration chip is damaged. Of course, there is another advantage that when mass-producing circuit boards, the AS interface download socket can be eliminated, leaving only the JTAG socket, which can save PCB area. Anyway, JTAG can also download POF files

The schematic diagrams of the JTAG and AS sockets are shown in Figure 9. It should be noted that the JTAG voltage of the Cyclone IV device must be 2.5V.

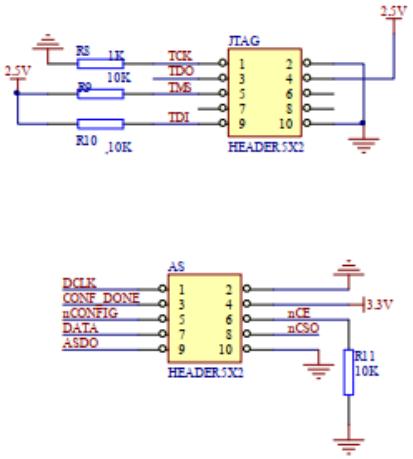


Figure 9 Schematic diagram of JTAG and AS socket parts

For the AS configuration part of the circuit, let's take a look at some reference designs given in the Cyclone IV Device Handbook, see Figure 10:

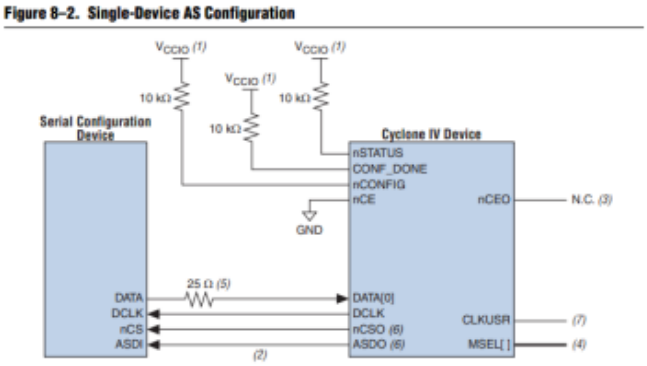


Figure 10 Reference design in Cyclone IV Device Handbook

Note that the main pins of the FPGA, nSTATUS\CONF_DONE\nCONFIG\, need to be pulled up with a 10K resistor, and nCE is grounded. The 4 pins of DATA\DCLK\NCSO\ASDO are SPI interfaces, which are connected to the configuration chip EPCS. Figure 11 is a schematic diagram of the AS part.

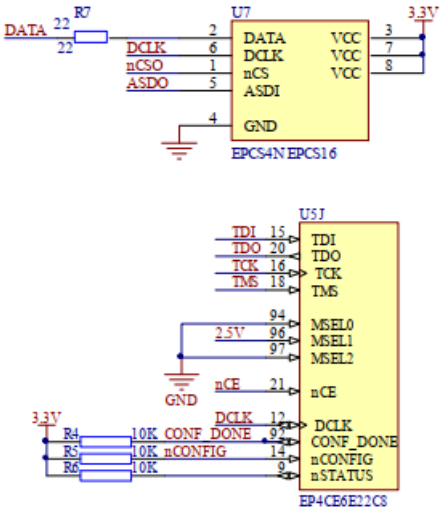


Figure 11 AS download configuration

2.5 Clock and Reset circuit

Unlike microcontrollers, FPGAs do not have a specific reset function pin. In theory, each IO can be used as a reset pin, but the reset function needs to be realized through programming. Figure 12 contains a simple low-level reset circuit. A good code style generally has reset statements in the design to ensure that the current state of each input/output is clear after the reset. After the system is running, press this key to input a low level to the FPGA, causing the system to enter a low-level reset state. The reset button can also be used as a stand-alone button, and users can use the reset button to do button input experiments.

The development board uses a 50M active SMD crystal to provide the system with a running clock. The clock and reset circuit circuits are shown in Figure 12. These clock pins are processed in the development board as follows：

a) CLK1 (PIN23) is used as the system working clock and is directly connected to the 50MHz crystal oscillator
b) CLK3 (PIN25) is used as the system reset pin, and the user can realize the reset function through programming.

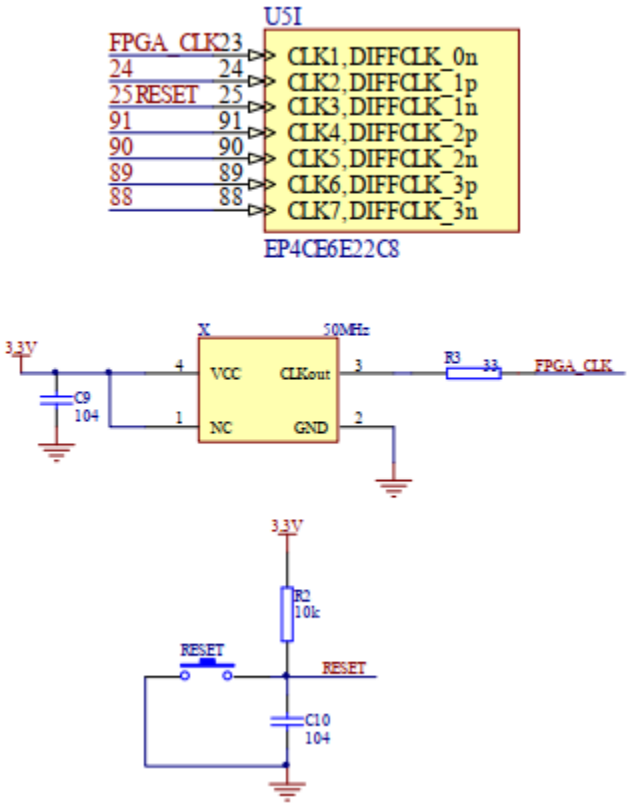


Figure 12 Clock and reset circuit

2.6 Extended IO distribution circuit

Each IO of the FPGA is drawn out, with a total of 3 expansion sockets, all of which are equipped with VCC5V, 3.3V, and GND power supplies, which are convenient for external connection. The schematic diagram of the expansion SOCKET is shown in Figure 13.

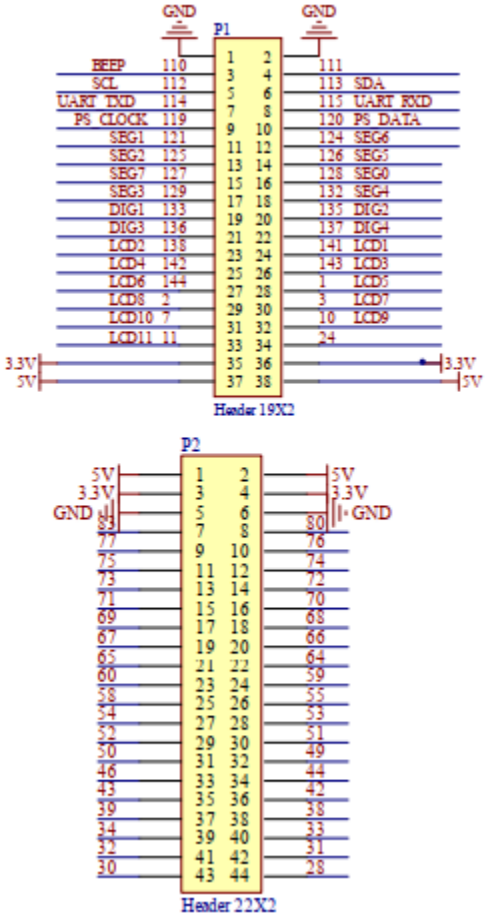


Figure 13 Schematic diagram of the expansion pack

2.7 Independent buttons and LEDS

There are 4 independent buttons and 4 independent LEDs on the student development board. The circuit is shown in Figure 14. For the button circuit part, if the output is low, it means that the button is pressed. The resistors R34-37 in the circuit are all protective to prevent the FPGA chip IO from shorting directly to ground when the button is pressed when it is set to output and high.

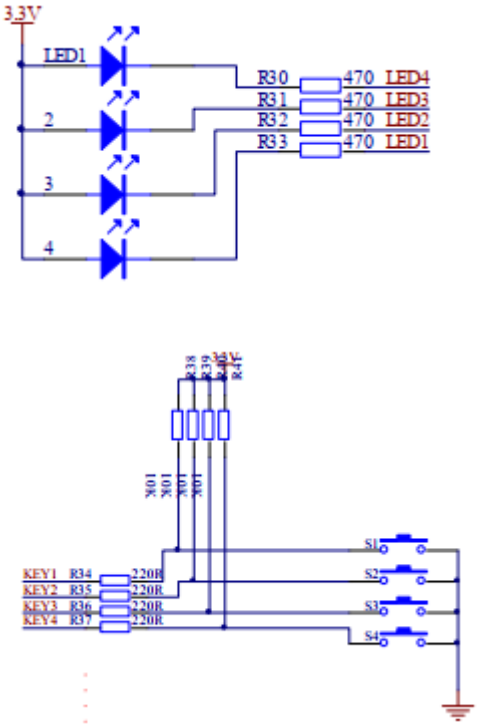


Figure 14 Independent buttons and LED circuits

2.8 Dip switch circuit

The dip switch is an input device. The circuit of the 4-digit dip switch is very simple. Note that it is multiplexed with the independent buttons. The circuit schematic diagram is shown in Figure 2.8.

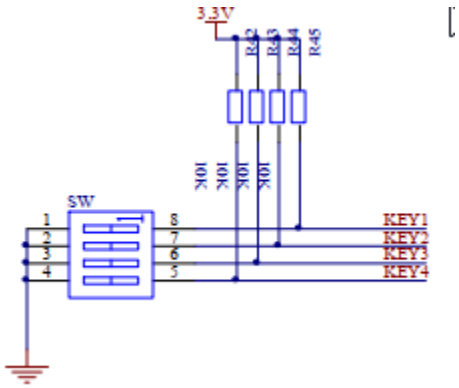


Figure 15 Dip switch circuit

2.9 Buzzer circuit

The buzzer is driven and controlled by a PNP transistor. If a certain frequency pulse is input to the BEEP, the buzzer will sound. Changing the input frequency can change the sound of the buzzer. The schematic diagram is shown in Figure 16.

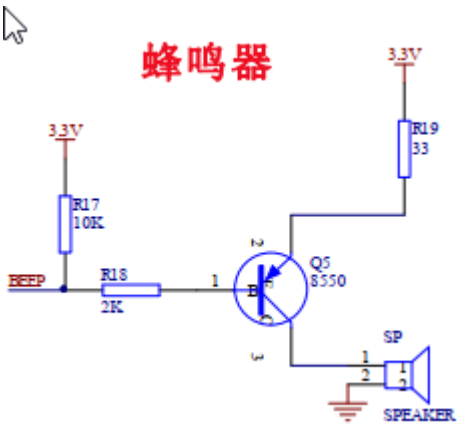


Figure 16 Buzzer circuit

2.10 Seven-segment digital tube display circuit

The seven-segment digital tube display circuit is shown in Figure 17. The digital tube is common anode. When the bit code drive signal is 0, the corresponding digital tube is operated; when the segment code drive signal is 0, the corresponding segment code lights up. The bit code is driven by a triode due to the large current

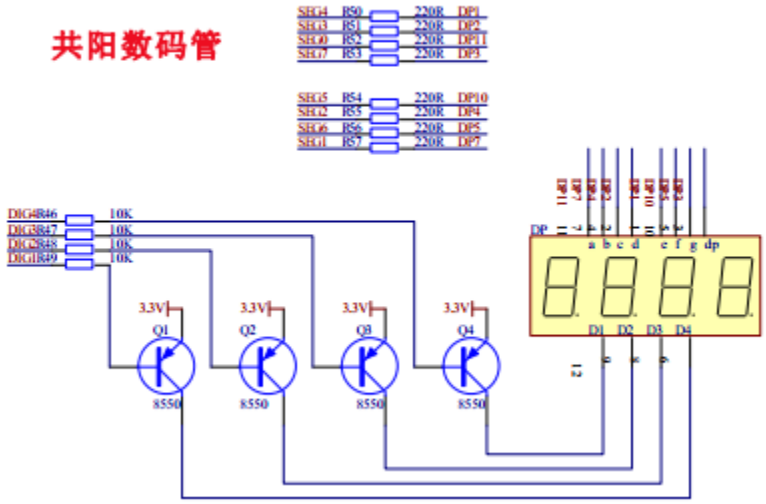


Figure 17 Seven-segment digital tube display circuit

2.11 LCD 1602, 12864, and TFT color screens

There is a 20-hole single-row seat on the board, which is shared by 1602 and 12864 and TFT color screen. When doing experiments, you need to install the optional liquid crystal device by yourself. Pay attention to the order of pins when installing. Figure 18 is the schematic diagram of the interface connection

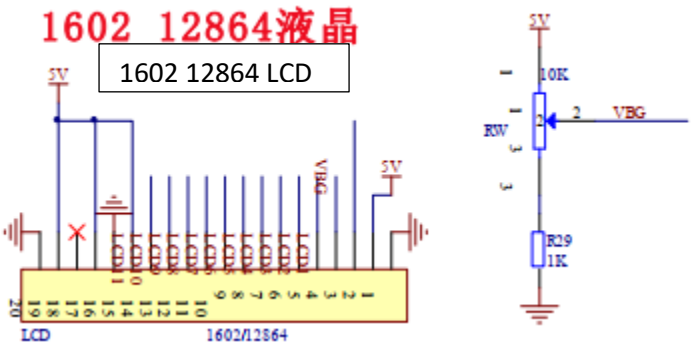


Figure 18 LCD 1602 and 12864 circuits

2.12 RS232 serial port

RS232 is one of the commonly used communication interfaces. It can be used for communication with peripheral equipment and system communication with the host. I believe that everyone is familiar with RS232 serial communication. Maybe you have played serial port with a single-chip microcomputer, or maybe you are also familiar with the hardware circuit of MAX232, but you may not be familiar with the serial port communication protocol. On the student development board, we can learn to design serial ports through FPGAs. This process is very helpful for familiarizing yourself with the protocol. The RS232 serial port circuit is shown in Figure 19. Since it is a 3.3V system, MAX3232 is used for RS232 level conversion.

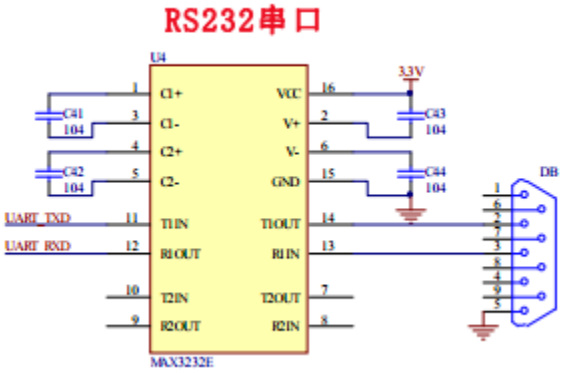


Figure 19 RS232 serial port circuit

2.13 VGA interface circuit

The interface circuit of VGA is shown in Figure 20. This circuit uses the method of resistor network to generate different voltage signals required by VGA. It is a simple 8-color generation circuit that can display characters, colors, etc. on the monitor.

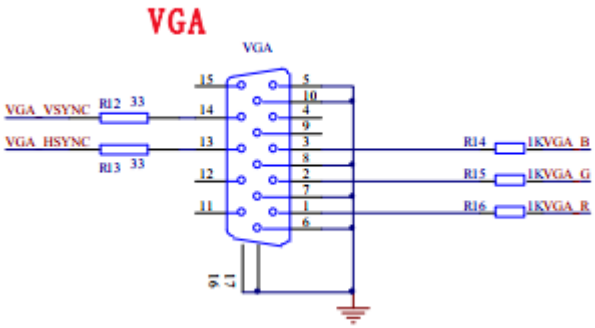


Figure 20 VGA interface circuit

2.14 PS/2 keyboard and mouse interface circuit

The PS/2 interface is a commonly used input device interface, which can use a mouse and keyboard as input for system data. The principle of the PS/2 keyboard and mouse interface circuit is shown in Figure 21. It is powered by a 5V power supply. Both the data cable and the clock cable of the interface must be connected with pull-up resistors.

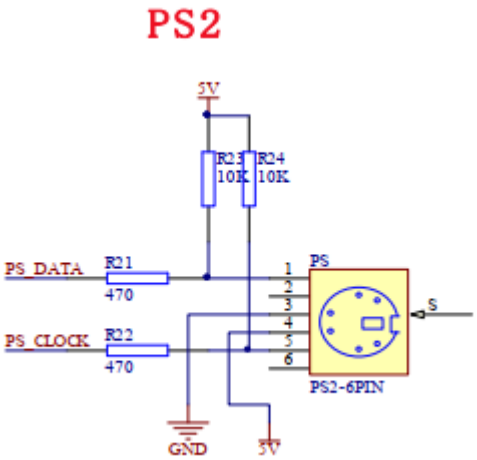


Figure 21 PS/2 keyboard and mouse interface circuit

2.15 Temperature sensor circuit

The digital temperature sensor circuit is shown in Figure 22. LM75A is a high-speed I2C interface temperature transfer device, which can directly convert the temperature into a digital signal in the temperature range of -55 to +125 degrees, with high accuracy.

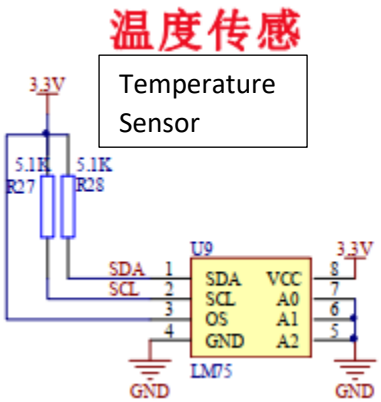


Figure 22 Temperature sensor circuit

2.16 IIC circuit

The I2C communication protocol is a serial bus standard. Although there is no data throughput capability of a parallel bus, I2C communication applications still have its vitality. The I2C bus uses the serial data line, SDA, and the serial clock line, SCL, to communicate information among devices connected to the bus. Each device has a unique address as an identification mark and can send and receive data. For more details, please refer to the I2C bus protocol specification. Figure 23 shows the circuit diagram

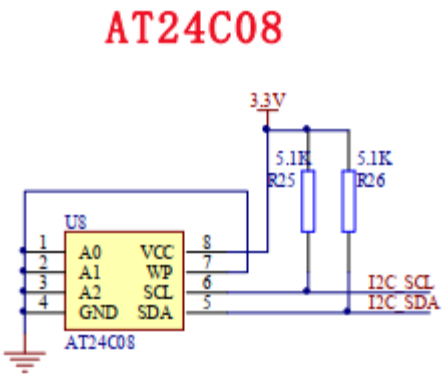


Figure 23 Temperature sensor circuit