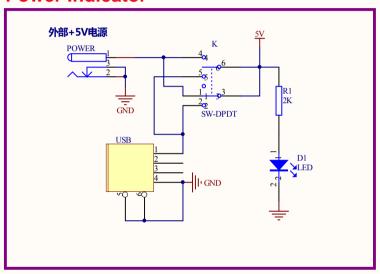
Power Indicator

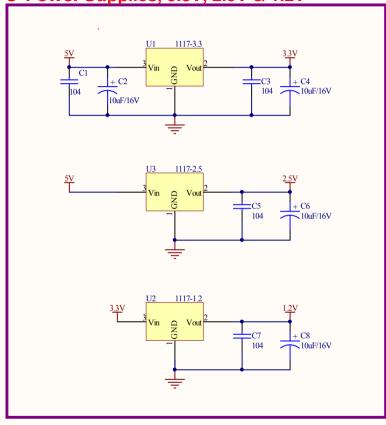


Notes on the schematic diagram:

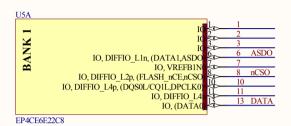
- 1. There are two ways to supply power to the development board, one is to connect the 5V power adapter externally or by connecting the USB B power supply. Only one can be connected, and the self-locking switch K can control two kinds of power supply switching
- 2. There are three kinds of onboard power supply

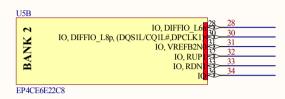
Power IC, respectively AMS1117-3.3V - IO voltage, AMS1117-2.5V - P AMS1117-1.2V - is

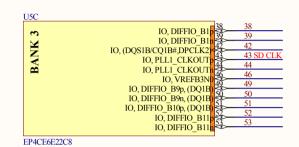
3-Power Supplies, 3.3V, 2.5V & 1.2V



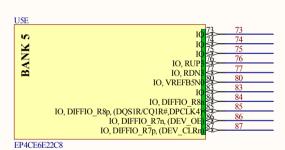
AMS1117-2.5V - PLL voltage, AMS1117-1.2V - is core voltage.								www.OurFPGA.com
Shanghai Weixin Technology Co.,	Drawing name	Power	Description	Different Development Bo	oard Power Supp	lies	Design	Smart R&D
Ltd.	Product Name	Altera Student Boart	Prod Num#	RZ-EasyFPGA A2.1	Drawing Version	2.1	Date	2017-2-1







U5D	
	IO, DIFFIO B125 54 54 55
4	IO, DIFFIO B12h
BANK	IO, DIFFIO B15p, (DQ1B)
Z	
₹	IO, DIFFIO BIG (DOID)
<u> </u>	IO, DIFFIO_B16n, (DQ1B)
	10 VPFFP 010 65 65
	IO, VREFB4N0 66 66
	IO, RUP2, (DQ1B) 67
	IO, RDN2, (DQ1B)
	IO, DIFFIO_B20n, (DQS0B/CQ1B,DPCLK3)
	TO DIFFIO POL
	IO, DIFFIO B21p 70
	IO, DIFFIO B21h 72 72
	IO, DIFFIO_B22p
EP4CE6E	22C8



BANK 6	IO, DIFFIO_R4n, (INIT_DONE IO, DIFFIO_R4p, (CRC_ERROR IO IO, DIFFIO_R3n, (nCEO) IO, DIFFIO_R3p, (CLKUSR) IO, (DQS0R/CQ1R,DPCLK5) IO, VREFB6N		98 99 100 101 103 104 105
	IO, VREFBOIND IO, DIFFIO R1	<u>6</u>	106

Schematic notes:

1. This page is the IO of the FPGA's BANK, the number marked on the pin, such as 98. It means the pin PIN98 of the FPGA chip If there are two network labels on the same connection, it means that these two networks are connected together. The pure digital network labels on the schematic diagram represent the corresponding pins of the FPGA, and this rule applies to the entire diagram.

							Tech Community	www.OurFPGA.com
Shanghai Weixin Technology Co.,		FPGA_BANK	Description	FPGA_BANK			De sign	Smart R&D
Ltd.	Prod. Name	Altera助学板	Prod Num#	RZ-EasyFPGA A2.1	Version	2.1	Date	2017-2-1

C15 C16 C17 C18 C19 C20 C21 C22

104 104

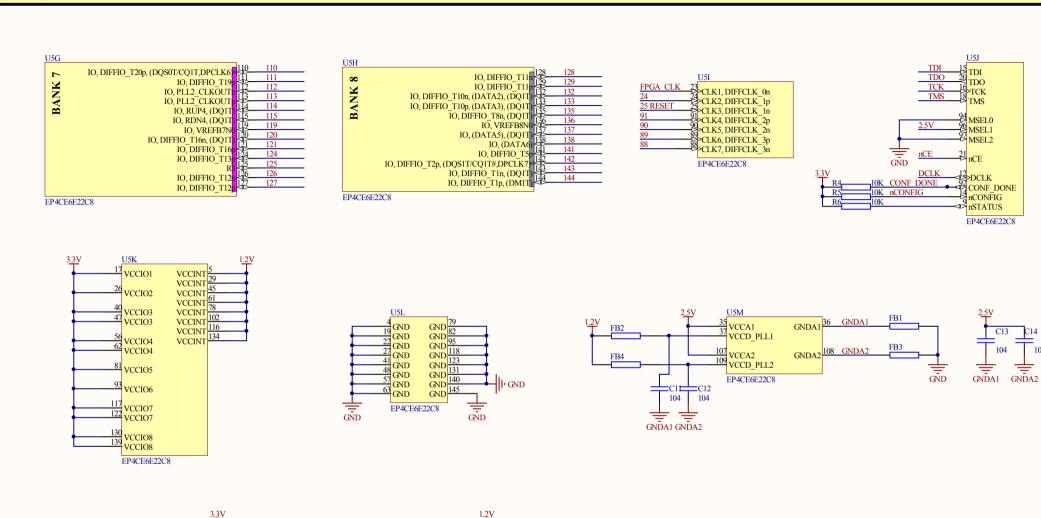
를 GND C23 C24 C25 C26

C27 C28

104

C29

₩ GND

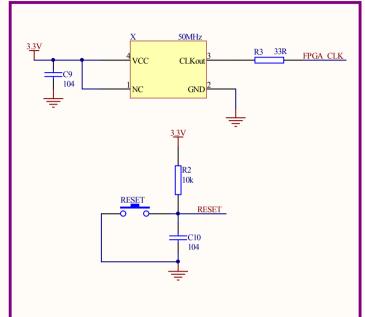


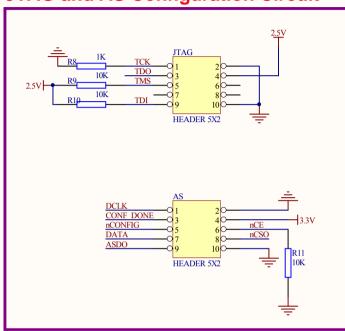
						Tech Community	www.OurFPGA.com
Shanghai Weixin Technology Co.,	Drawing NameFPGA_BANK	Description	FPGA_BANK			De sign	Smart R&D
Ltd.	Prod. Name Altera Student Boart	Prod Num#	RZ-EasyFPGA A2.1	Version	2.1	Date	2017-2-1

C32

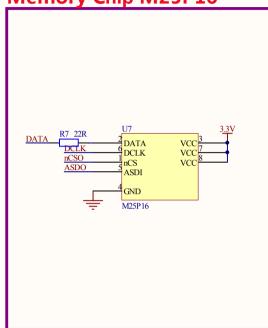
C30 C31

50M Crystal Oscillator and Reset Circuit JTAG and AS Configuration Circuit



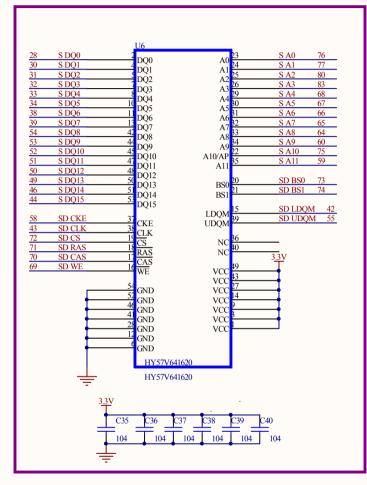


Memory Chip M25P16

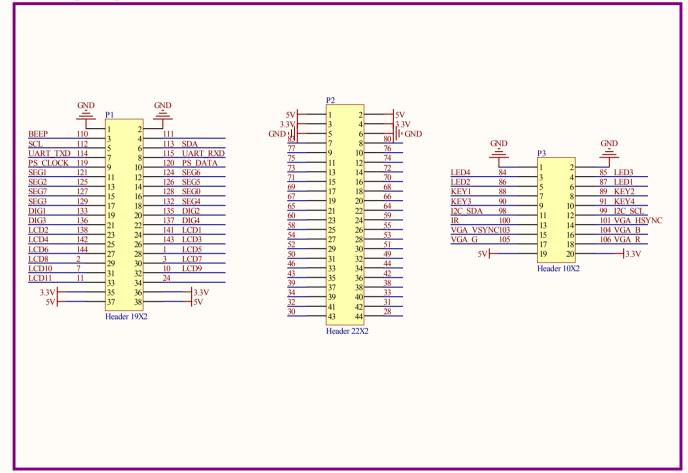


						Tech Community	www.OurFPGA.com
Shanghai Weixin Technology Co.,	Drawing NameCLK_JTAG_RST	Description	CLK_JTAG_RST			De sign	Smart R&D
Ltd.	Prod. Name Altera Student Boart	Prod Num#	RZ-EasyFPGA A2.1	Version	2.1	Date	2017-2-1

SDRAM Circuit



IO Outgoing Extensions



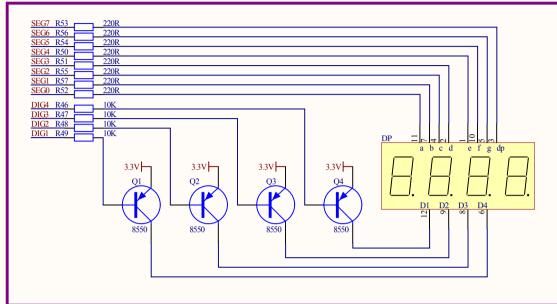
Schematic notes:

1. The number marked on the pin, such as 110. If the PIN110 pin of the FPGA chip has two network labels, it means that the two labels are connected together. For example, BEEP110 indicates that the PIN110 pin of the FPGA is connected to this expansion pin and is connected to the BEEP network.

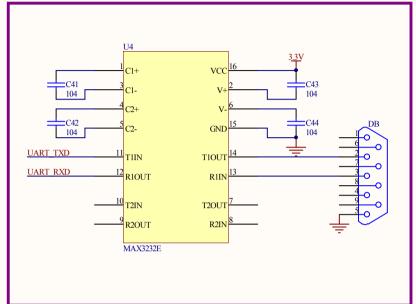
	expansion p	oni ana io oo	incoted to the BLEF hetwo	• • • • • • • • • • • • • • • • • • • •					
					<u></u>			Tech Community	www.OurFPGA.com
Shanghai Weixin Technolog	y Co.,	Drawing Na	meSDRAM_IO Extension	Description	SDRAM_IO Extension			De sign	Smart R&D
Ltd.		Prod. Name	Altera Student Boart	Prod Num#	RZ-EasyFPGA A2.1	Version	2.1	Date	2017-2-1

6_Peripherals& Interfaces.SchDoc

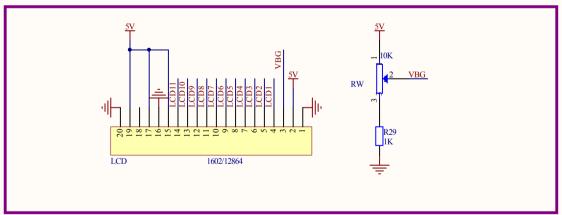
4 Digit - 7 Segment Display



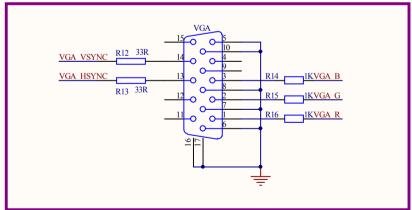
RS232 Serial Port



1602 12864 LCD

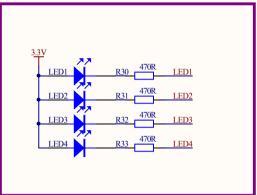


VGA Interface

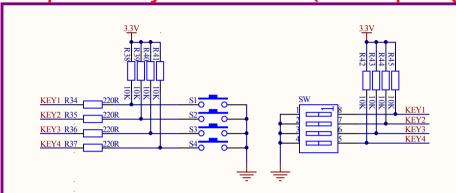


							Tech Community	www.OurFPGA.com
Shanghai Weixin Technology Co.,	Drawing Na	mePeripherals & Interfaces	Description	Peripherals & Interfaces			De sign	Smart R&D
Ltd.	Prod. Name	Altera Student Boart	Prod Num#	RZ-EasyFPGA A2.1	Version	2.1	Date	2017-2-1

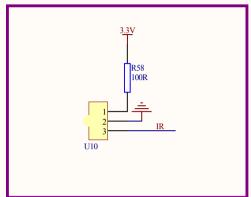
4 LEDs



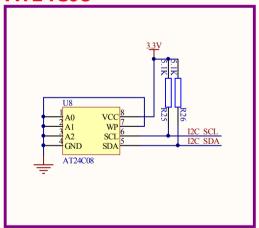
Independent key and DIP switch (IO multiplexing)



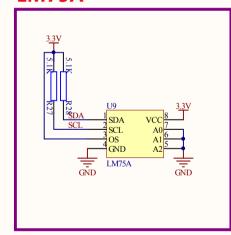
Infrared



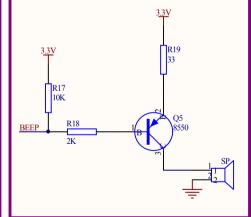
AT24C08



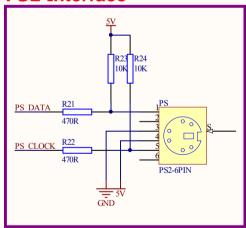
Temperature Sensor LM75A



Buzzer



PS2 Interface



							Tech Community	www.OurFPGA.com
Shanghai Weixin Technology Co.,	Drawing Na	mePeripherals & Interfaces	Description	Peripherals & Interfaces			De sign	Smart R&D
Ltd.	Prod. Name	Altera Student Boart	Prod Num#	RZ-EasyFPGA A2.1	Version	2.1	Date	2017-2-1