VLSI Circuits Design HW#3

Course	Name	Student ID
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● 1A - activity factors and probabilities of 8-input AND gate

Figure 1 shows an 8-input AND gate built by a tree of gates. If all of the input probabilities are 0.5, please determine the activity factors and probabilities at each node in the circuit.

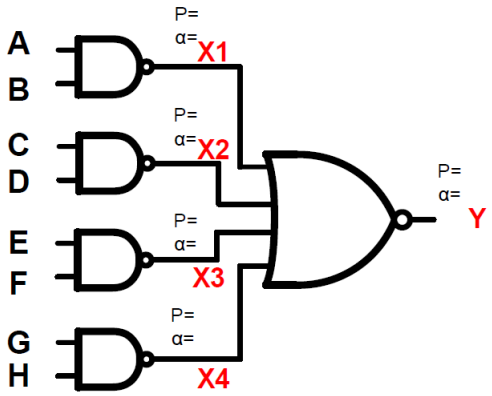


Figure 1. 8-input AND gate

node X1, X2, X3, X4	XAND gate只有在所有輸入都為1時，才會輸出0，因此$P_0 = \frac{1}{2} \cdot \frac{1}{2} = \frac{1}{4}$，$P_1 = 1 - P_0 = 1 - \frac{1}{4} = \frac{3}{4}$，$\alpha = P_0 \cdot P_1 = \frac{3}{16}$。
node Y	XNOR gate 只有在所有輸入都為0時，才會輸出1，因此$P_0 = \left(\frac{1}{4}\right)^4 = \frac{1}{256}$，$P_1 = 1 - P_0 = 1 - \frac{1}{256} = \frac{255}{256}$，$\alpha = P_0 \cdot P_1 = \frac{255}{256} \cdot \frac{1}{256} = \frac{255}{4^8}$。

Define P_i to be the probability that node i is 1

因此 $P_{X1} = P_{X2} = P_{X3} = P_{X4} = \frac{3}{4}$、$\alpha_{X1} = \alpha_{X2} = \alpha_{X3} = \alpha_{X4} = \frac{3}{16}$、$P_Y = \frac{255}{256}$、$\alpha_Y = \frac{255}{4^8}$。

● 1B - activity factor of signal

Consider an input signal as shown in Fig.2. and its rising and falling time are 100ps. The clock rate is 1MHz. Determine the activity factor for the signal.

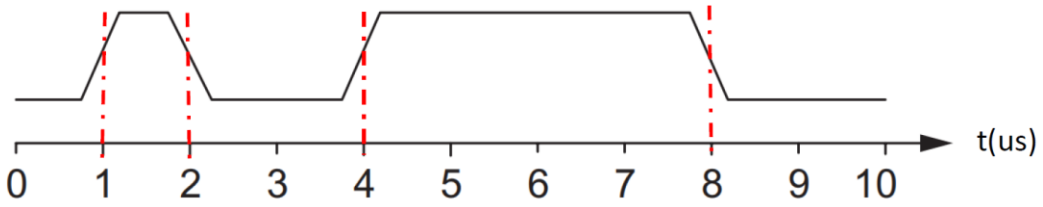


Figure 2. An input signal.

在時間區間$T = 10\mu s = 10 \cdot 10^{-6}$之內"0到1"這個event發生2次，因此$f_{sw} = \frac{2\text{times}}{10 \cdot 10^{-6} s} = 0.2 \cdot 10^6 Hz$，$f_{sw} = \alpha f_{CLK} \Rightarrow \alpha = \frac{f_{sw}}{f_{CLK}} = \frac{0.2 \cdot 10^6}{1 \cdot 10^6} = 0.2$。

- 1C - minimum delay and dynamic power of 2-stage inverter buffer

Consider a 2-stage inverter buffer drives the capacitor, 100Cu , as shown in Fig.3.

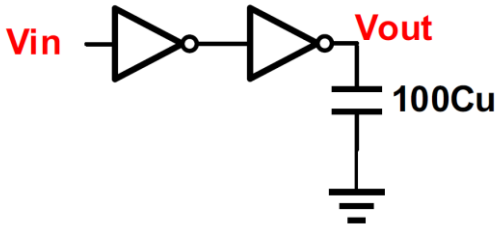


Figure 3. 2-stage inverter diagram.

A. First, design the circuit with the minimum delay and the first inverter input capacitor should be 4Cu. What is the delay you calculate? And what is the size?

根據題意$C_{in} = 4fF, C_{out} = 100fF$。

1. 計算path effort $F = GBH = (1 \cdot 1)(1 \cdot 1) \cdot \frac{100}{4} = 25$。

2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot 25^{\frac{1}{2}} + (1+1) = 12$。

3. 計算各級邏輯閘的effort均為$\hat{f} = F^{\frac{1}{N}} = 25^{\frac{1}{2}} = 5$。

4. 從後往前推，計算每一級的輸入電容值 $\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}$

$$C_{in} = \frac{1 \cdot 100}{5} = 20$$

$$(C_{in})' = \frac{1 \cdot 20}{5} = 4$$

I. 第二級inverter

$C_{in} = 3r + 1r = 4r = 20fF \Rightarrow r = 5$

PMOS : $3r = 15fF \Rightarrow W = \frac{15fF}{\frac{2fF}{\mu m}} = 7.5\mu m$

NMOS : $1r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

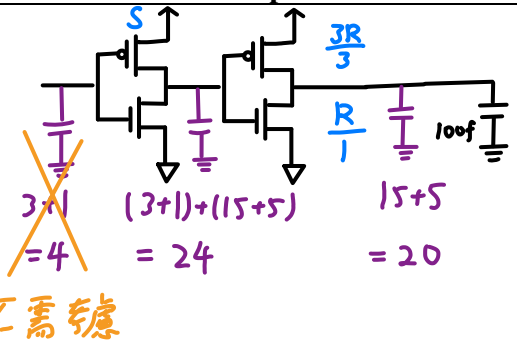
II. 第一級inverter

$C_{in} = 3r + 1r = 4r = 4fF \Rightarrow r = 1$

PMOS : $3r = 3fF \Rightarrow W = \frac{3fF}{\frac{2fF}{\mu m}} = 1.5\mu m$

NMOS : $1r = 1fF \Rightarrow W = \frac{1fF}{\frac{2fF}{\mu m}} = 0.5\mu m$

B. Using Fig.2 as an input signal and using hspice to measure the power of circuit you designed in 1C-a. Additionally, you have to calculate the dynamic power and compare with hspice measurement result to explain the difference.

理論值	 不需要考慮最前面gate電容，那是算在輸入源或是前一級的電路的power，而非這一級的power。

	$P_{dynamic} = \alpha C V_{DD}^2 f = 0.2 \cdot (100 + 44) \cdot 10^{-15} \cdot 1.8^2 \cdot 10^6 = 9.33 \cdot 10^{-8}(W)$
測量值	$P_{measure} = 9.528 \cdot 10^{-8}(W)$
解釋	測量值略大於理論值$P_{measure} = 9.528 \cdot 10^{-8}(W) > P_{dynamic} = 9.33 \cdot 10^{-8}(W)$，推測原因是測量值還包括$P_{short\ circuit}$、$P_{static}$，而理論值只有計算$P_{dynamic} = \alpha C V_{DD}^2 f$而已。

C. Changing the rising and falling time to one-tenth of the clock period and using hspice to mearsure its power again. Is there any difference between 1C-b and 1C-c? If so, please briefly explain it.

	原本	後來
rising and falling time (s)	$100ps = 10^{-10}$	$\frac{1}{10}(1 \cdot 10^{-6})^{-1} = 10^{-7}$
power (W)	$9.528 \cdot 10^{-8}$	$1.433 \cdot 10^{-6}$
推測原因	由於在切換狀態下PMOS和NMOS同時導通會產生短路電流$P_{short\ circuit}$，rising and falling time增加3個order的改變，會讓切換狀態時間變久，而造成短路電流發生的時間增加，因此power會增加。	

- 2A - Presim of ring oscillator with $f_{osc} = 3 \pm 0.1GHz$ and duty cycle $50 \pm 1\ \%$

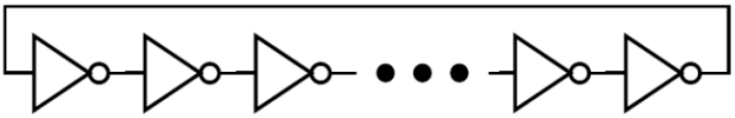


Figure 5. Ring Oscillator Circuit

如上課講義U20-P16觀念，對於ring oscillator中一顆inverter的delay time為$d = gh + p = 1 \cdot 1 + 1 = 2$，再根據講義U20-P6，在.18製程下$3RC = 12\ ps$，，所以$1RC = 4 \cdot 10^{-12}s \Rightarrow 4RC = 12 \cdot 10^{-12}s$。

ring oscillator的震盪頻率是輸入從0到1、1到0算一次，因此要跑兩次，假設有N-stage inverter，ring oscillator的震盪頻率即為

$$f_{osc} = \frac{1}{2 \cdot d \cdot N \cdot \tau} = \frac{1}{4 \cdot N \cdot 12 \cdot 10^{-12}} = 3GHz = 3 \cdot 10^9 Hz$$

$$\Rightarrow N = \frac{1}{4 \cdot 16 \cdot 10^{-12} \cdot 3 \cdot 10^9} = 5.2 \sim 5$$

故使用5級電路實現，由於$\mu_p : \mu_n = 1:3$，為了使上下R充放電一致，$W_p : W_n = 3:1$，經過適當嘗試後，決定$W_p = 3\mu m, W_n = 1\mu m$。

presim模擬數據如下

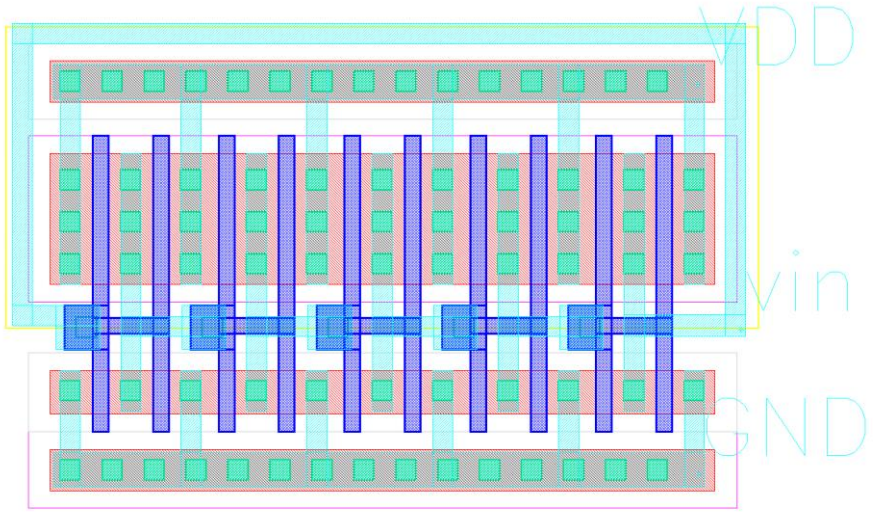
period	frequency	t_on	duty_cycle
3.245e-10	3.082e+09	1.639e-10	0.5050

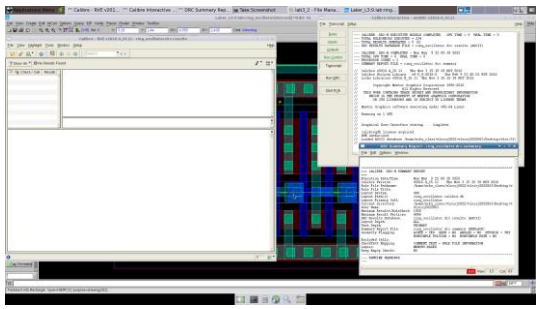
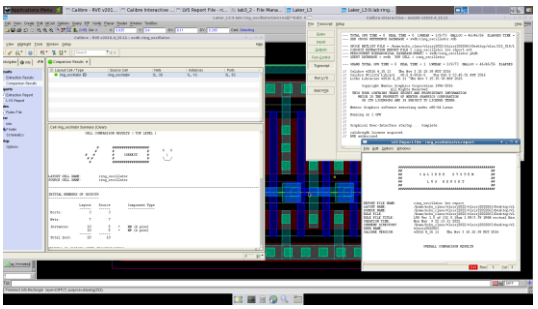
ring oscillator的震盪頻率$f_{osc} = 3.08 \cdot 10^9$介在$f_{osc} = 3 \pm 0.1GHz$之間符合SPEC與duty cycle 50.5 %介在50 ± 1 %之間符合SPEC。

- 2B - Postsim of ring oscillator with $f_{osc} = 3 \pm 0.1GHz$ and duty cycle $50 \pm 1\ \%$

layout技巧是將inverter folding一次，如此VDD和GND會在inverter的外面，兩個inverter之間就可以共用VDD和GND，diffusion就不會中斷，因此diffusion面積變小，代表電晶體的寄生電容電容變小，RC delay就會變小，震盪頻率就能上升。

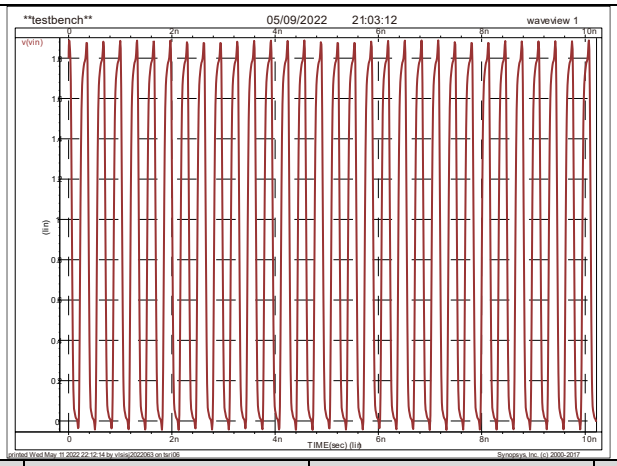
第一次layout我是用metal 2把最右邊和最左邊的電路接在一起，做postsim驗證後發現震盪頻率大於3 ± 0.1GHz，不符合SPEC要求，因此我需要提高寄生電容，這樣震盪頻率才會下降，第二次layout我將metal 2改用metal 1，如下圖從最右邊到最左邊繞了一大圈，如此就可以提高寄生電容，不用metal 2也可以減少光罩次數，使電路製造成本降低。

layout


DRC	LVS
	

postsim模擬數據如下

postsim waveform



period	frequency	t_on	duty_cycle
3.231e-10	3.095e+09	1.618e-10	0.5008

ring oscillator的震盪頻率$f_{osc} = 3.095 \cdot 10^9$介在$f_{osc} = 3 \pm 0.1GHz$之間符合SPEC與duty cycle 50.08 %介在50 ± 1 %之間符合SPEC。

● 2C - Voltage-Controlled ring Oscillator (VCO)

Fig.3 illustrate a Voltage-Controlled ring Oscillator (VCO). The control signals, V_{ctrl} and $\overline{V_{ctrl}}$, are used to control the current source so that the delay can be controlled by the signals. Please derive and design a VCO that the center frequency is 3GHz when $V_{ctrl} = \overline{V_{ctrl}} = 0.9$. Furthermore, the frequency should **cover from** 2.9G to 3.1GHz when $V_{ctrl} = 0.7 - 1.1V$ and $\overline{V_{ctrl}} = 1.8 - V_{ctrl}$. Finally, simulate it with HSpice.

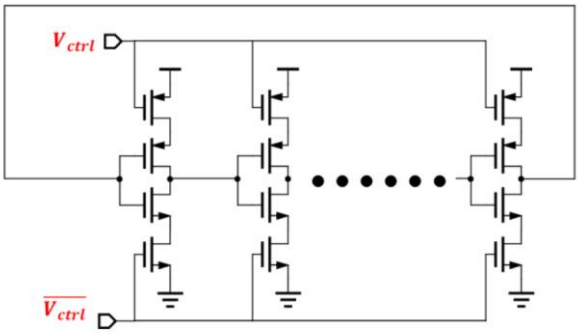


Figure 6. Voltage-Controlled ring Oscillator

計算方式同2A小題，故使用五級電路實現，最上面和最下面的電晶體是current source，調大電晶體的W，current source的電流越大，因此RC delay下降，震盪頻率會上升，而PMOS和NMOS的比例取3:1，使上下電路的電阻相同，如此duty cycle才會趨近於50%。

經過適當嘗試後，決定由上而下電晶體的size依序為6u, 0.45u, 0.25u, 2u。(0.25u的MOS可以用**魚骨頭的layout方式**，中間的diffusion縮減至0.25u，兩旁的diffusion增加直到可以容納一個contact的空間)

presim模擬數據如下

	period	frequency	t_on	duty_cycle
$V_{ctrl} = 0.7V$	7.749e-10	1.291e+09	3.889e-10	0.5019
$V_{ctrl} = 0.9V$	3.313e-10	3.019e+09	1.607e-10	0.4849
$V_{ctrl} = 1.1V$	3.106e-09	3.220e+08	1.557e-09	0.5013

VCO在$V_{ctrl} = 0.9V$時$f_{osc} = 3.019 \cdot 10^9$，介在$f_{osc} = 3 \pm 0.1GHz$之間符合SPEC；

$V_{ctrl} = 0.7V$時$f_{osc} = 1.291 \cdot 10^9$，$V_{ctrl} = 1.1V$時$f_{osc} = 32.2 \cdot 10^9$有包含到(cover from) 2.9G to 3.1GHz符合SPEC。

不太了解電路特性，教授上課也沒有提及這種電路，我只知道最上面和最下面的電晶體是current source而已，花了半個小時才調出符合SPEC的電晶體參數，事後詢問出題助教，助教說這需要修之後進階的PLL類比課程才會比較了解。

- 3A - minimum delay and lowest power between 30τ and 29τ

A. Consider the circuit in Fig.8. How many stages will give the minimum delay, and how should the stages be sized?

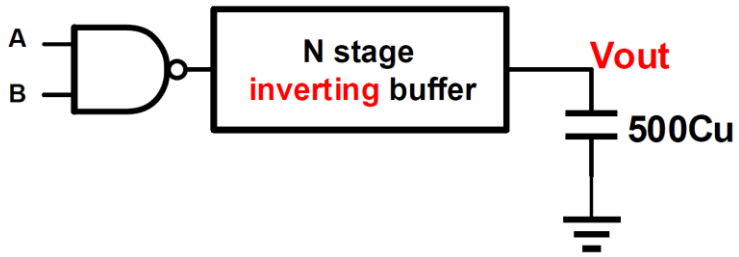
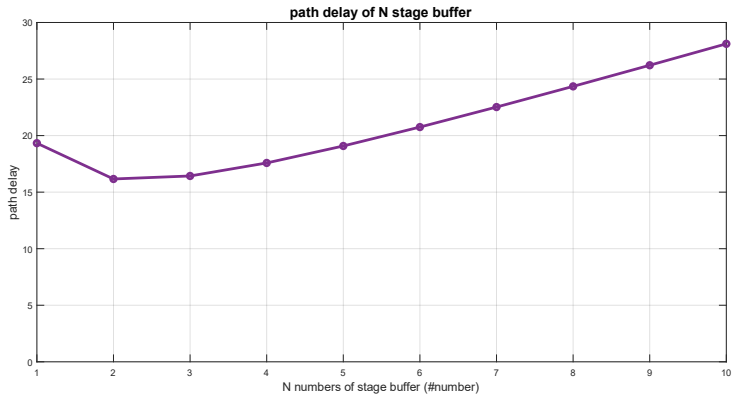


Figure 8. 2-input NAND with N-stage inverting buffer

根據題意$C_{in} = 10fF, C_{out} = 500fF$。

1. 計算path effort $F = GBH = \left(\frac{4}{3} \cdot 1^N\right) \cdot 1 \cdot \frac{500}{10} = \frac{200}{3}$。

2. 計算此path最小delay time是$D = (N+1)F^{\frac{1}{(N+1)}} + P = (N+1)\left(\frac{200}{3}\right)^{\frac{1}{(N+1)}} + (2 + N \cdot 1)$，matlab作圖如下



題目有加條件"N stage inverting buffer"，也就是一定要使用奇數個inverter，因此由上圖可知在此限制條件下$N = 3$時delay會最小。

3. 計算各級邏輯閘的effort均為$\hat{f} = F^{\frac{1}{N+1}} = \left(\frac{200}{3}\right)^{\frac{1}{3+1}} = 2.857$。

4. 從後往前推，計算每一級的輸入電容值 $\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}$

$$C_{in} = \frac{1 \cdot 500}{2.857} = 175$$

$$(C_{in})' = \frac{1 \cdot 175}{2.857} = 61.26$$

$$(C_{in})'' = \frac{1 \cdot 61.26}{2.857} = 21.44$$

$$(C_{in})''' = \frac{1 \cdot 21.44}{2.857} = 10$$

I. 第四級inverter

$C_{in} = 2r + 1r = 3r = 175fF \Rightarrow r = 58.3$

PMOS : $2r = 116.67fF \Rightarrow W = \frac{15fF}{\frac{2fF}{\mu m}} = 58.33\mu m$

NMOS : $1r = 58.33fF \Rightarrow W = \frac{58.33fF}{\frac{2fF}{\mu m}} = 29.15\mu m$

II. 第三級inverter

$C_{in} = 2r + 1r = 3r = 61.26fF \Rightarrow r = 20.42$

PMOS : $2r = 40.84fF \Rightarrow W = \frac{40.84fF}{\frac{2fF}{\mu m}} = 20.42\mu m$

NMOS : $1r = 20.42fF \Rightarrow W = \frac{20.42fF}{\frac{2fF}{\mu m}} = 10.21\mu m$

III. 第二級inverter

$C_{in} = 2r + 1r = 3r = 21.44fF \Rightarrow r = 7.15$

PMOS : $3r = 14.29fF \Rightarrow W = \frac{14.29fF}{\frac{2fF}{\mu m}} = 7.15\mu m$

NMOS : $1r = 7.15fF \Rightarrow W = \frac{7.15fF}{\frac{2fF}{\mu m}} = 3.57\mu m$

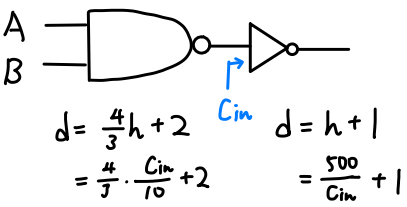
IV. 第一級2-input NAND gate

$C_{in} = 2r + 2r = 4r = 10fF \Rightarrow r = 2.5$

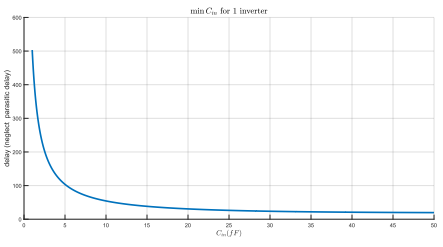
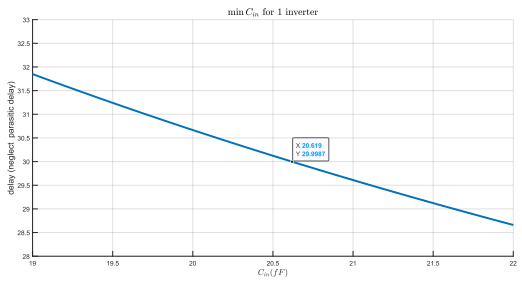
PMOS : $2r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

NMOS : $2r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

B. Furthermore, assume we neglect the diffusion capacitances. If the delay constraint is between 30τ and 29τ, what N should be set to give the lowest power, and how should the stages be sized? How much dynamic power does it consume?



首先決定級數為最小值$N = 1$，因為根據講義U23-8觀念，電路級數越少，power會越小，再來是決定inverter size，delay time計算為$d_{nand\ gate} + d_{inv} = \left(\frac{4}{3} \cdot \frac{C_{in}}{10} + 2\right) + \left(\frac{500}{C_{in}} + 1\right)$，將inverter的輸入電容(gate電容) C_{in}視為變數掃delay在29和30的值，如下圖所示

整體圖	右圖放大
	

由上圖可知極值發生在$C_{in} = 20.62$， 從後往前推，計算每一級的輸入電容值。

I. 第二級inverter

$C_{in} = 2r + 1r = 3r = 20.62fF \Rightarrow r = 6.87$

PMOS : $2r = 13.75fF \Rightarrow W = \frac{13.75fF}{\frac{2fF}{\mu m}} = 6.87\mu m$

NMOS : $1r = 6.87fF \Rightarrow W = \frac{6.87fF}{\frac{2fF}{\mu m}} = 3.44\mu m$

II. 第一級2-input NAND gate

$C_{in} = 2r + 2r = 4r = 10fF \Rightarrow r = 2.5$

PMOS : $2r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

NMOS : $2r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

題目規定計算dynamic power時要忽略diffusion capacitances，因此電容只會有inverter的輸入電容(gate電容) C_{in}和負載電容C_{load}。

$$P_{dynamic} = \alpha C V_{DD}^2 f = \alpha(21f + 500f)V_{DD}^2 f = (521f)\alpha V_{DD}^2 f$$

- 3B - Minimum Power Delay Product estimation

Consider the circuit shown in Fig.9. How should the stages be sized to get the minimum Power Delay Product?

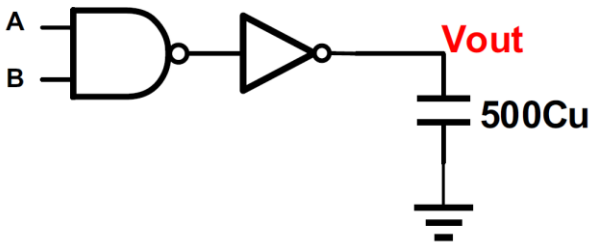


Figure 9. 2-input NAND with 1-stage inverting buffer

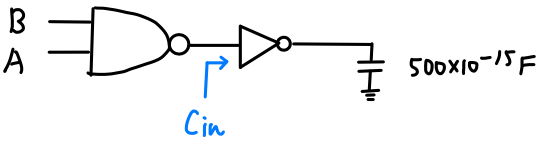
power-delay product(PDP)

$= delay \times power$

$= \left[\left(\frac{4}{3}\cdot\frac{C_{in}}{10} + 2\right) + \left(\frac{500}{C_{in}} + 1\right)\right][\alpha C V_{DD}^2 f]$

在同一α, V_{DD}, f比較基準下

$= \left[\left(\frac{4}{3}\cdot\frac{C_{in}}{10} + 2\right) + \left(\frac{500}{C_{in}} + 1\right)\right] C$



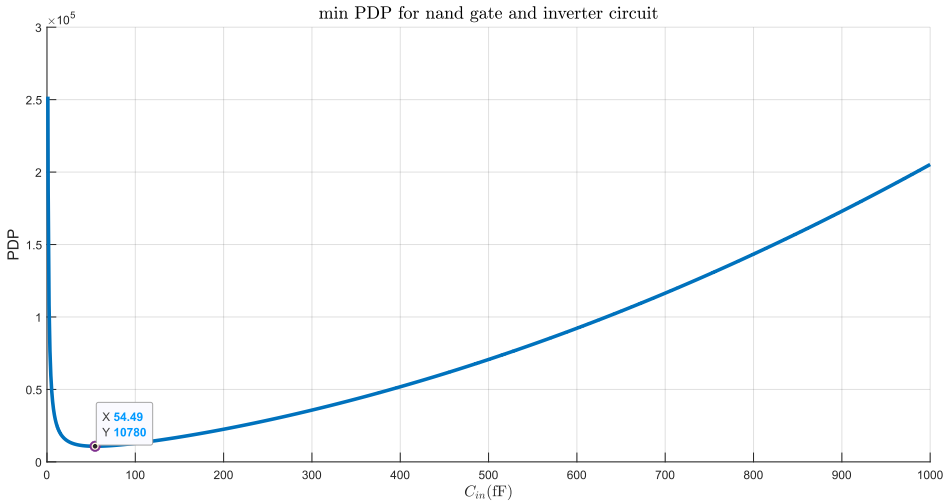
$d = \frac{4}{3}h + 2 = \frac{4}{3}\cdot\frac{C_{in}}{10} + 2$

$d = 1h + 1 = 1\frac{500}{C_{in}} + 1$

計算dynamic power時**選擇**忽略diffusion capacitances，因此電容只會有inverter的輸入電容(gate電容) C_{in}和負載電容C_{load}。

$= \left[\left(\frac{4}{3}\cdot\frac{C_{in}}{10} + 2\right) + \left(\frac{500}{C_{in}} + 1\right)\right](C_{in} + 500)$

將inverter的輸入電容(gate電容) C_{in}視為變數掃PDP，matlab作圖如下



由上圖可知極值發生在$C_{in} = 54.49$， 從後往前推，計算每一級的輸入電容值。

III. 第二級inverter

$C_{in} = 2r + 1r = 3r = 54.49fF \Rightarrow r = 18.16$

PMOS : $2r = 36.33fF \Rightarrow W = \frac{36.33fF}{\frac{2fF}{\mu m}} = 18.16\mu m$

NMOS : $1r = 18.16fF \Rightarrow W = \frac{18.16fF}{\frac{2fF}{\mu m}} = 9.08\mu m$

IV. 第一級2-input NAND gate

$C_{in} = 2r + 2r = 4r = 10fF \Rightarrow r = 2.5$

PMOS : $2r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

NMOS : $2r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

- 3C - Order of input signals and Minimum Power Delay Product simulation

A. Consider the circuit in 3B with the two input signals, A and B, illustrated in Fig.10. However, the input order of 2-input static NAND gate can affect the delay. Please derive the propagation rising delay t_{pdr} and the propagation falling delay t_{pdf} of NAND first to get the correct input order. Clearly present your procedure with explanation and state your assumptions, if any.

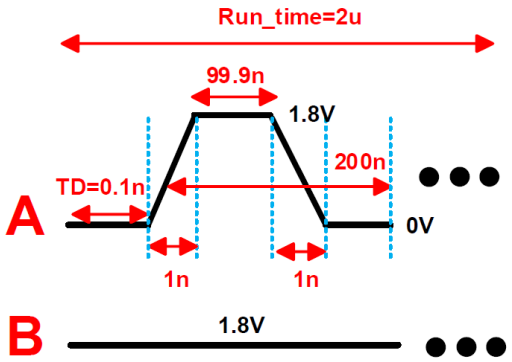
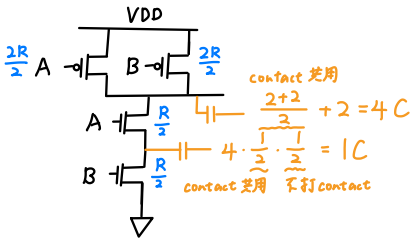
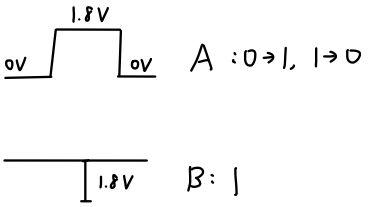


Figure 10. Input signals

寄生電容計算(有考慮layout優化)



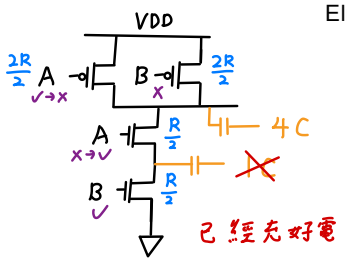


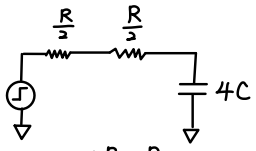
A is inner input，計算結果為 $t_{pdf} = t_{pdr} = 4RC$

case 1-1 A:0→1.8

Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}} C_i$

falling ⇒ source is GND



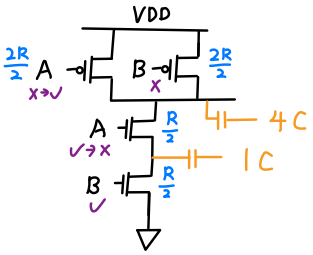


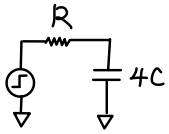
$t_{pdf} = (\frac{R}{2} + \frac{R}{2}) 4C = 4RC$

case 1-2 A: 1.8 →0

Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}} C_i$

rising ⇒ source is VDD





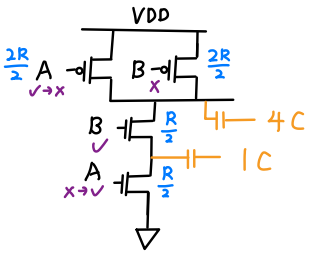
$t_{pdr} = R \cdot 4C = 4RC$

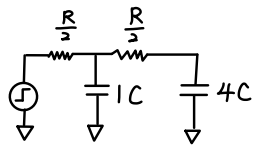
A is outer input，計算結果為 $t_{pdf} = t_{pdr} = \frac{9}{2}RC$

case 2-1 A:0→1.8

Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}} C_i$

falling ⇒ source is GND



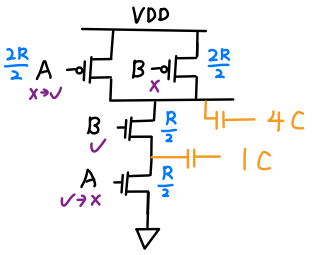


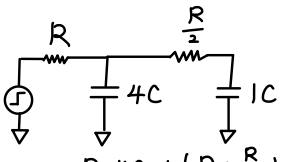
$t_{pdf} = \frac{R}{2} \cdot 1C + (\frac{R}{2} + \frac{R}{2}) 4C = \frac{9}{2} RC$

case 2-2 A: 1.8→0

Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}} C_i$

rising ⇒ source is VDD



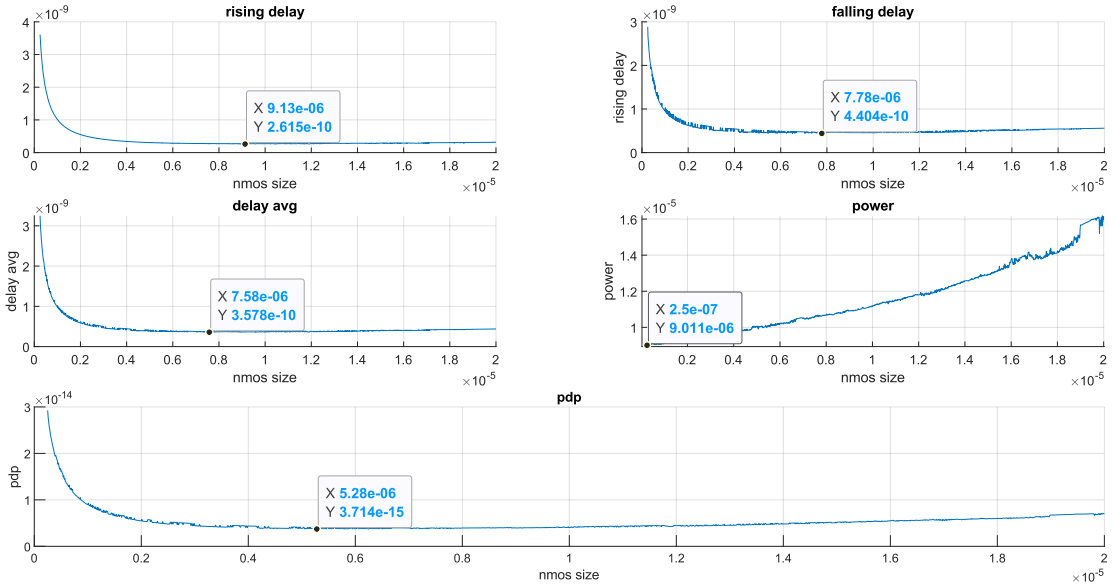


$t_{pdr} = R \cdot 4C + (R + \frac{R}{2}) \cdot 1C = \frac{9}{2} RC$

A是inner input的delay $t_{pdf} = t_{pdr} = 4RC$小於A是outer input的delay $t_{pdf} = t_{pdr} = \frac{9}{2}RC$，因此下一題使用delay小的pattern - A是inner input進行HSPICE模擬。

B. Then, please sweep the sizes of the inverter to get the figure of Power Delay Product, and explain it on the report. According to the figure of Power Delay Product, choose the best one sizes and fill the Table.1.

決定好輸入訊號在NAND gate順序後，接下來跑模擬`.tran 1p 2u sweep size 0.25u 20u 10n`，掃NMOS尺寸`size`(PMOS尺寸為NMOS尺寸的兩倍)，分別測量 t_{pdf}, t_{pdr}, power，因此power delay product即為power $\cdot \frac{t_{pdf}+t_{pdr}}{2}$，匯出文字數據到`*mt0`檔，使用matlab指令`readmatrix`，將文字檔轉為矩陣形式，對matlab來說只要能轉換成矩陣格式之後數據就好處理了，作圖如下



由3C-A小題理論計算rising/falling delay應該保持一致 $t_{pdf} = t_{pdr} = 4RC$，但如上圖實際模擬falling delay是rising delay的1倍到2倍之間。

NMOS size(與PMOS size)很小時，未符合delay time最佳值 - 每一級要推等效4個自己(fanout)，因此inverter推不動負載電容$C_{load} = 500fF$，rising/falling delay很大；NMOS size(與PMOS size)越大時，C_{in}越大，因此$P_{dynamic} = \alpha C V_{DD}^2 f$越大，power會持續上升。由於PDP是delay和power的乘積，size過小rising/falling delay會變很大，size過大power會變很大，因此size對pdp的圖形會是一個兩次微分為正$f''(x) > 0$的上凹圖形。

在power delay product最小值(3.714e-15)下，紀錄此時各量測參數t_{pdf}, t_{pdr}, power如下表所示

NMOS size	5.280e-06
PMOS size	10.560e-06
rising delay	2.976e-10
falling delay	4.457e-10
delay average	3.717e-10
power	-9.993e-06
power delay product	3.714e-15

由3B小題最小PDP理論值應發生在NMOS的size $W = 9.08\mu m$，但實際HSPICE最小PDP模擬值發生在NMOS的size $W = 5.28\mu m$，還是有不小的差距。

● Conclusion

本次作業用到power章節並結合之前speed章節的觀念。

A. 第一大題

1A、1B小題計算不同邏輯閘節點或是單一輸入訊號的activity factor。

1C小題計算dynamic power並與HSPCIE模擬power值做比較，以及探討改變rising/falling time對power的影響。

B. 第二大題

2A、2B小題用到speed章節的ring oscillator觀念，做presim和layout後的postsim驗證確定實際HSPCIE模擬值是否符合題目SPEC要求。

2C小題是vloltage-controlled ring oscillator這部分上課沒提及，不過用目前已知觀念還是可知最上面和最下面的MOS是current source，以此思路去調參數以符合SPEC要求。

C. 第三大題

這大題一開始看不太懂題目，在找出題助教詢問多次後，確認自己解題方向是否正確。

3A小題為在”指定條件”下決定最小delay與最小power下電路的級數和個別電晶體的size。

3B小題決定最小power下電路的級數和個別電晶體的size。

3C小題首先判斷要使用哪種input pattern才能讓delay最小，而再根據最小delay的input pattern，去掃電晶體的size測量rising/falling delay和power，計算pdp，做size對pdp圖，模擬出最小power下個別電晶體的size值，並與3B小題的理論計算值做對照。