VLSI Circuits Design HW#2

Course	Name	Student ID
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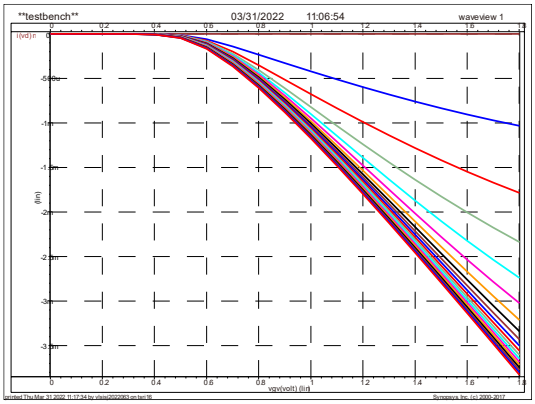
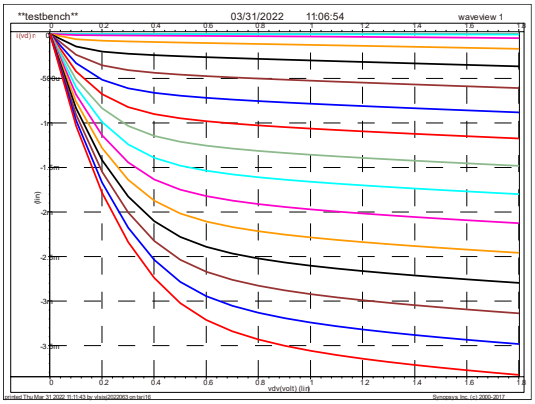
- 1A - NMOS characteristic curve

$i_{DS} - v_{DS}$ with v_{GS}	$i_{DS} - v_{GS}$ with v_{DS}
	
解釋	解釋
在HSPICE測試檔下.PROBE關鍵字，將指定的輸出變數儲存到 HSPICE 的介面圖形資料檔中。 1. $v_{GS} < v_t$時，由於MOS結構是back-to back diode，正常情況下，即使施加多大V_{DS}，電流一樣是0。 2. $v_{GS} > v_t$時，n-channel的電子通道形成，產生電流。 3. 從不同曲線看，當v_{DS}不斷加大，曲線會趨於緊密，代表電流會趨於飽和，v_{DS}再繼續增加對電流影響不大。	1. $v_{DS} = 0$代表MOS兩端無跨壓，自然不會產生電流。 2. 由於v_{DS}非常小，$(v_{GS} - V_t)v_{DS} \gg \frac{1}{2}v_{DS}^2$，則可將二次乘積項消除，因此可視MOSFET為一電阻，電阻值為$r_{DS} = \frac{1}{g_{DS}}$。 3. 當$v_{DS}$不斷加大，靠近drain端的channel深度不斷減少，一直加到$v_{GS} - v_{DS} = v_{GD} = V_t$，此時drain端的channel被"捏到沒有"(等於0)，稱為pinch off，進入飽和(saturation)區。

HSPICE語法

*電源名稱V、電壓VGV跨在G和GND端

```
VG G GND VGV
VD D GND VDV
```

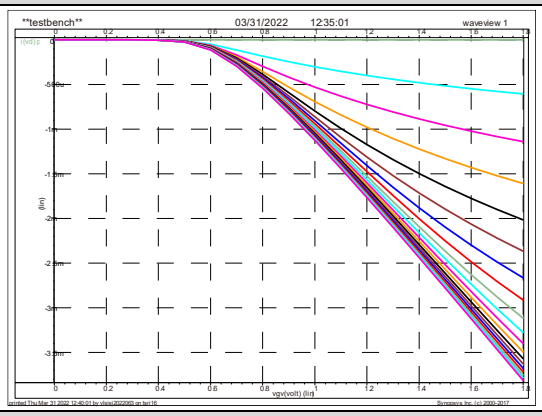
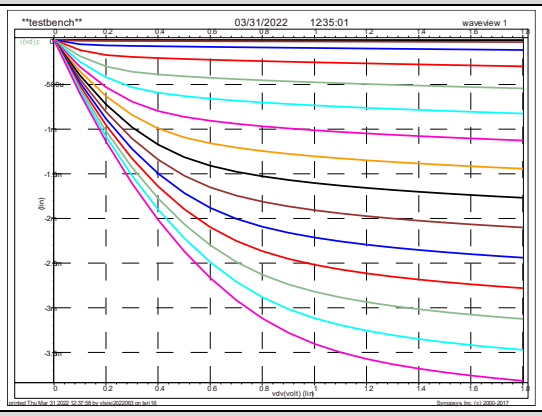
使用DC穩態分析，因此波型檔會輸出至.sw0，固定VGV電壓為0，掃描VDV電壓以0.1間隔從0至1.8，接下來VGV增加至0.2，繼續掃描VDV電壓以0.1間隔從0至1.8，因此最後畫出來的波型y-axis軸會是vgs。

```
.DC VGV 0 1.8 0.1 sweep VDV 0 1.8 0.1
```

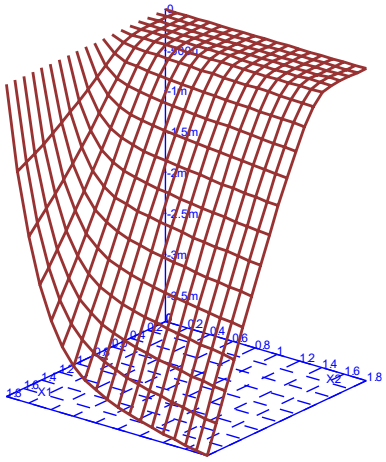
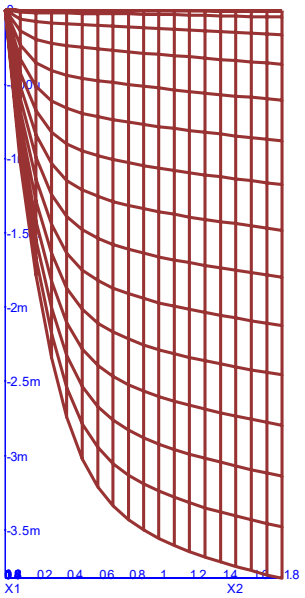
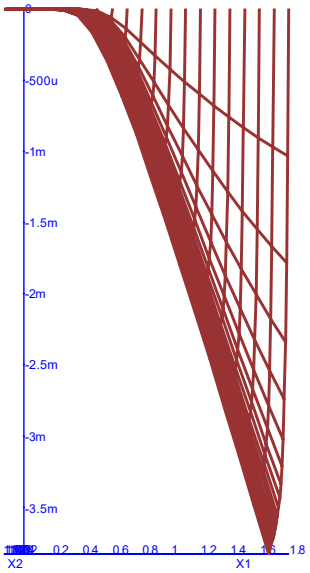
* .PROBE關鍵字將以下指定變數會輸出到波型檔

```
.probe i(MM0) vds(MM0) vgs(MM0)
```

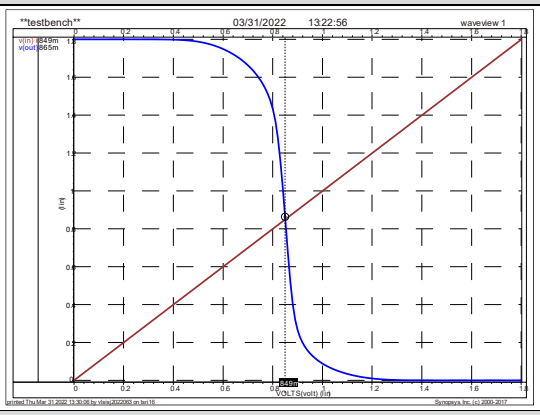
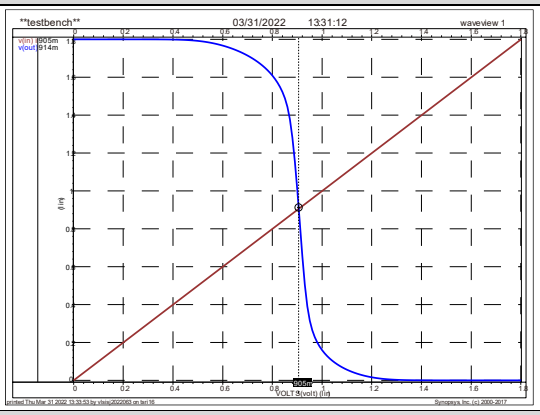
- 1B - PMOS characteristic curve

$i_{DS} - v_{DS}$ with v_{GS}	$i_{DS} - v_{GS}$ with v_{DS}
	
解釋	解釋
同上，PMOS與NMOS的解釋一樣。	同上，PMOS與NMOS的解釋一樣。

- 1C – NMOS characteristic curve in 3D view

$i_{DS} - v_{DS} - v_{GS}$	從v_{DS}面看	從v_{GS}面看
		
解釋		
調整3D圖的位置，分別另外做了從v_{DS}面與v_{GS}面看到的圖，代表意義是對3D圖投影至2D平面，與第一題繪製出的圖形一致，驗證這個答案是沒錯的。		

- 1D – find the proper W of PMOS

$\left(\frac{W}{L}\right)_N = \frac{2\mu m}{0.18\mu m}, \left(\frac{W}{L}\right)_P = \frac{4\mu m}{0.18\mu m}$ $\Rightarrow V_{V_{in}=V_{out}} = 0.849V$	$\left(\frac{W}{L}\right)_N = \frac{2\mu m}{0.18\mu m}, \left(\frac{W}{L}\right)_P = \frac{6\mu m}{0.18\mu m}$ $\Rightarrow V_{V_{in}=V_{out}} = 0.905V$
	

解釋

在HSPICE測試檔下`.meas DC Vth FIND V(out) WHEN V(out) = V(in)`指令，量測DC穩態分析與$V_{in} = V_{out}$下，"out"這個節點名字的電壓值並存入變數`Vth`。根據題目給的數據測出的臨界電壓值過小，未達一半$\frac{V_{DD}}{2} = 0.9V$，在固定NMOS的W下，需要提高PMOS的W，使PMOS電流值加大，更容易導通，這樣臨界電壓才會加大，這部分觀念可以參考U17-8。

- 1E - Linear delay model of inverter

HSPICE語法

* 時間td過後才開始測量，在$V_{in} = 0.9$並且第二次下降與在$V_{out} = 0.9$並且第二次上升的時間差存入變數tdelay_rise

```
.measure tran tdelay_rise trig v(in) val=0.9 td=0 fall=2 targ
v(out) val=0.9 rise=2
.measure tran tdelay_fall trig v(in) val=0.9 td=0 rise=2 targ
v(out) val=0.9 fall=2
```

* propagation delay time為rising propagation delay time與falling propagation delay time的平均值

```
.measure tran tdelay_avg param = '(tdelay_rise + tdelay_fall) /
2'
```

實驗值分析

使用matlab內建函數`polyfit(x,y,1)`，將7筆實驗值做最小平方法找出擬合一階多項式的最佳方程式。

$$\min \text{SSE} = \min \sum_{i=1}^{n} (y_i - \hat{y})^2 = \min \sum_{i=1}^{n} (y_i - a - bx)^2$$

$$\Rightarrow \begin{cases} \frac{\partial}{\partial a}\sum_{i=1}^{n}(y_i - a - bx)^2 = 0 \\ \frac{\partial}{\partial b}\sum_{i=1}^{n}(y_i - a - bx)^2 = 0 \end{cases}$$

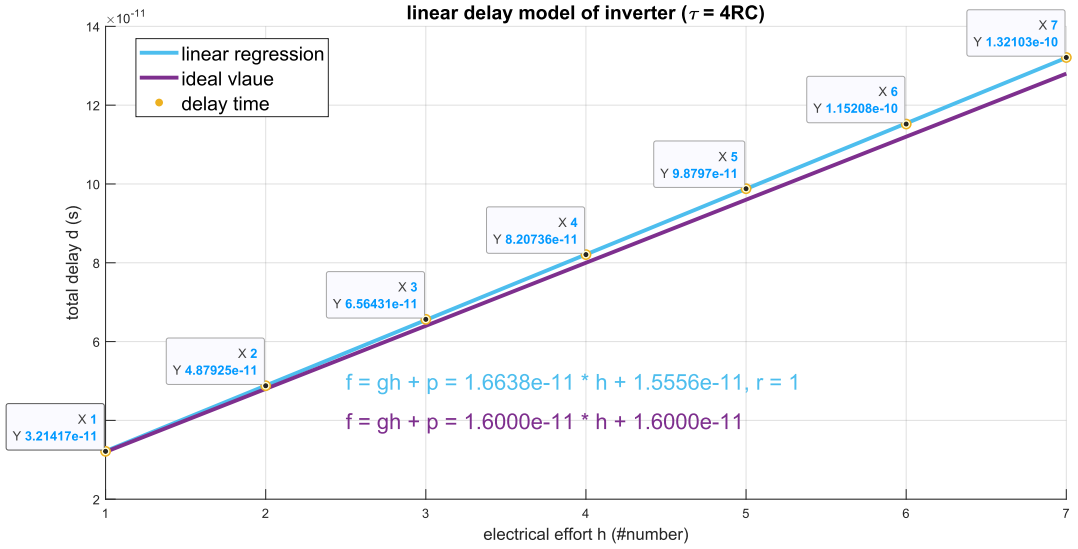
理論值計算

1D小題藉由調整PMOS和NMOS電晶體的W使logic gate switching threshold voltage在$\frac{V_{DD}}{2}$，也就是beta ratio $\frac{\beta_p}{\beta_n} = 1$，此時電晶體的W為$W_{pmos}: W_{nmos} = 3:1 \Rightarrow \mu_p: \mu_n = 1:3$，透過RC delay model將PMOS阻值model為$3R$、將NMOS阻值model為$1R$。

根據講義U20-6使用linear delay model的normalization的準則 - **最小delay的值，也就是一個inverter沒有parasitic delay下delay值**，此題為$1RC + 3RC = 4RC$，再根據講義U20-P6，在.18製程下$3RC = 12\,ps$，，所以$1RC = 4 \cdot 10^{-12}s \Rightarrow 4RC = 16 \cdot 10^{-12}s$，因此一個inverter使用linear delay model分析下的delay time為

$$d = \frac{t_{td}}{\tau} \Rightarrow t_{td} = d \cdot \tau = (1 \cdot h + 1) \cdot 4RC = 1.6 \cdot 10^{-11}h + 1.6 \cdot 10^{-11}(s)$$

linear delay model of inverter ($\tau = 4RC$)



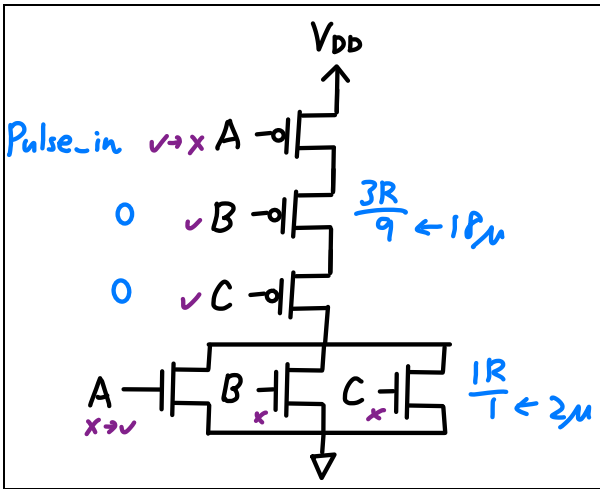
圖表解釋

由前面兩者分析繪圖如上，delay d與electrical effort/fanout h兩變數相關係數 $\gamma \sim 1$，呈現高度相關，且與理論值計算的linear delay model方程式差距非常小。

- 1F - Linear delay model of 3-input NOR gate

理論值計算

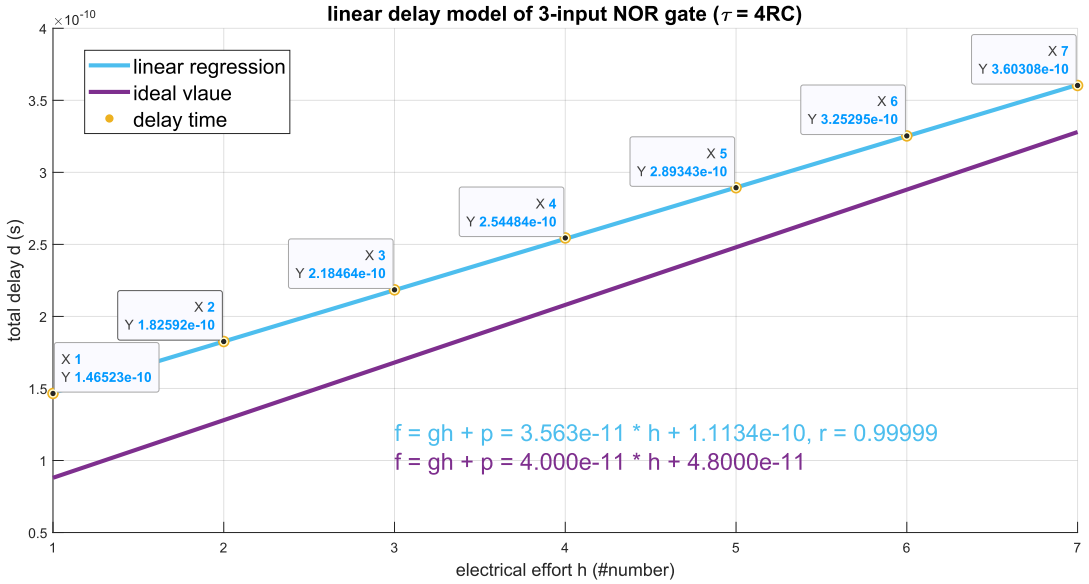
同上題參數$\mu_p: \mu_n = 1:3$，而為了使3-input NOR gate上下迴路RC充放電一致，故決定NMOS的尺寸為1、PMOS的尺寸為9。



由左圖可知，3-input NOR gate的linear delay model即為$d = gh + p = \frac{10RC}{4RC} + \frac{12RC}{4RC} = 2.5h + 3$，delay time即為

$$d = \frac{t_{td}}{\tau}$$
$$\Rightarrow t_{td} = d \cdot \tau$$
$$= (2.5 \cdot h + 3) \cdot 4RC$$
$$= 4 \cdot 10^{-11}h + 4.8 \cdot 10^{-11}(s)$$

linear delay model of 3-input NOR gate ($\tau = 4RC$)



圖表解釋

本題未指定3-input NOR gate輸入端的接法，而我是用worst case去接，電路上面PMOS中B、C端接地是always ON，而A端會隨著輸入訊號pulse_in上下起伏，無論是在(output)rising和falling的階段都會有A端與B端寄生電容18C、B端與C端寄生電容18C影響，這些都是linear delay model所忽略的值，所以上面的圖測量值迴歸線的斜率才會比理論值計算高。

- 1G - Compare 1E and 1F

詳細分析過程如前面所述，整理表格如下

	理論delay time(s)	實際delay time(s)
inverter	$1.6 \cdot 10^{-11}h + 1.6 \cdot 10^{-11}$	$1.7 \cdot 10^{-11}h + 1.6 \cdot 10^{-11}$
3-input NOR gate	$4.0 \cdot 10^{-11}h + 4.8 \cdot 10^{-11}$	$3.6 \cdot 10^{-11}h + 1.1 \cdot 10^{-11}$

- 2A - Path logical delay G and total path effort F

A. 7-input NAND gate and inverter

$$\begin{cases} G = \prod g_i = \frac{8}{3} \cdot 1 = \frac{8}{3} \\ B = 1 \\ \mathrm{H} = \frac{\mathrm{C_{out}}}{\mathrm{C_{in}}} = \frac{1000\mathrm{f}}{10\mathrm{f}} = 100 \end{cases}$$

$$\Rightarrow F = GBH = \frac{8}{3} \cdot 100 = \frac{800}{3}$$

$$P = \sum p = 6 + 1 = 7$$

$$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{800}{3}\right)^{\frac{1}{2}} + 7 = 39.66$$

B. 3-input NAND gate and 2-input NOR gate

$$\begin{cases} G = \prod g_i = \frac{5}{3} \cdot \frac{5}{3} = \frac{25}{9} \\ B = 1 \\ H = \frac{C_{out}}{C_{in}} = \frac{1000f}{10f} = 100 \end{cases}$$

$$\Rightarrow F = GBH = \frac{25}{9} \cdot 100 = \frac{2500}{9}$$

$$P = \sum p = 3 + 2 = 5$$

$$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{2500}{9}\right)^{\frac{1}{2}} + 5 = 38.33$$

C. 2-input NAND gate and 3-input NOR gate

$$\begin{cases} G = \prod g_i = \frac{4}{3} \cdot \frac{7}{3} = \frac{28}{9} \\ B = 1 \\ H = \frac{C_{out}}{C_{in}} = \frac{1000f}{10f} = 100 \end{cases}$$

$$\Rightarrow F = GBH = \frac{20}{9} \cdot 100 = \frac{2800}{9}$$

$$P = \sum p = 2 + 3 = 5$$

$$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{2800}{9}\right)^{\frac{1}{2}} + 5 = 40.28$$

D. 3-input NAND gate, inverter A, 2-input NAND gate, and inverter B

$$\begin{cases} \boldsymbol{G = \prod g_i = \frac{5}{3} \cdot 1 \cdot \frac{4}{3} \cdot 1 = \frac{20}{9}} \\ \boldsymbol{B = 1} \\ \boldsymbol{H = \frac{C_{out}}{C_{in}} = \frac{1000f}{10f} = 100} \end{cases}$$

$$\Rightarrow F = GBH = \frac{20}{9} \cdot 100 = \frac{2000}{9}$$

$$P = \sum p = +3 = 5$$

$$D = NF^{\frac{1}{N}} + P = 4 \cdot \left(\frac{2000}{9}\right)^{\frac{1}{4}} + 7 = 22.44$$

- 2B - Electrical effort h per stage

A. 7-input NAND gate and inverter

$$\hat{f} = F^{\frac{1}{N}} = \left(\frac{800}{3}\right)^{\frac{1}{2}} = \frac{4801}{294}$$

$$\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}$$

$$C_{in} = 1000 \cdot 1 \cdot \frac{4801}{294} = 61.24$$

$$(C_{in})' = 61.24 \cdot \frac{8}{3} \cdot \frac{4801}{294} = 10$$

$$h_{\text{inverter}} = \frac{C_{out}}{(C_{in})'} = \frac{1000}{61.24} = 16.33$$

$$h_{\text{7-input NAND gate}} = \frac{(C_{out})'}{(C_{in})''} = \frac{61.24}{10} = 6.12$$

B. 3-input NAND gate and 2-input NOR gate

$$\hat{f} = F^{\frac{1}{N}} = \left(\frac{2500}{9}\right)^{\frac{1}{2}} = \frac{50}{3}$$

$$\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}$$

$$C_{in} = 1000 \cdot \frac{5}{3} \cdot \frac{3}{50} = 100$$

$$(C_{in})' = 100 \cdot \frac{5}{3} \cdot \frac{4801}{294} = 10$$

$$h_{\text{2-input NOR gate}} = \frac{C_{out}}{(C_{in})'} = \frac{1000}{100} = 10$$

$$h_{\text{3-input NAND gate}} = \frac{(C_{out})'}{(C_{in})''} = \frac{100}{10} = 10$$

C. 2-input NAND gate and 3-input NOR gate

$$\hat{f} = F^{\frac{1}{N}} = \left(\frac{2800}{9}\right)^{\frac{1}{2}} = \frac{8096}{459}$$

$$\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}$$

$$C_{in} = 1000 \cdot \frac{7}{3} \cdot \frac{459}{8096} = 132.94$$

$$(C_{in})' = 132.94 \cdot \frac{4}{3} \cdot \frac{459}{8096} = 10$$

$$h_{\text{3-input NOR gate}} = \frac{C_{out}}{(C_{in})'} = \frac{1000}{132.94} = 7.52$$

$$h_{\text{2-input NAND gate}} = \frac{(C_{out})'}{(C_{in})''} = \frac{132.94}{10} = 13.29$$

D. 3-input NAND gate, inverter A, 2-input NAND gate, and inverter B

$$\hat{f} = F^{\frac{1}{N}} = \left(\frac{2000}{9}\right)^{\frac{1}{4}} = \frac{1583}{410}$$

$$\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}$$

$$C_{in} = 1000 \cdot 1 \cdot \frac{410}{1583} = 259$$

$$(C_{in})' = 259 \cdot \frac{4}{3} \cdot \frac{410}{1583} = 89.44$$

$$(C_{in})'' = 89.44 \cdot 1 \cdot \frac{410}{1583} = 23.17$$

$$(C_{in})''' = 23.17 \cdot \frac{5}{3} \cdot \frac{410}{1583} = 10$$

$$h_{\text{3-input NAND gate}} = \frac{C_{out}}{(C_{in})'} = \frac{1000}{259} = 3.86$$

$$h_{\text{inverter A}} = \frac{(C_{out})'}{(C_{in})''} = \frac{259}{89.44} = 2.90$$

$$h_{\text{2-input NAND gate}} = \frac{(C_{out})''}{(C_{in})'''} = \frac{89.44}{23.17} = 3.86$$

$$h_{\text{inverter B}} = \frac{(C_{out})'''}{(C_{in})''''} = \frac{23.17}{10} = 2.32$$

- 2C - Size the gates

A. 7-input NAND gate and inverter

I. 7-input NAND gate

$C_{in} = 2r + 6r = 8r = 10fF \Rightarrow r = 1.25$

PMOS : $2r = 2.5fF \Rightarrow W = \frac{2.5fF}{\frac{2fF}{\mu m}} = 1.25\mu m$

NMOS : $6r = 7.5fF \Rightarrow W = \frac{7.5fF}{\frac{2fF}{\mu m}} = 3.25\mu m$

II. inverter

$C_{in} = 2r + 1r = 3r = 61.24fF \Rightarrow r = 20.41$

PMOS : $2r = 40.83fF \Rightarrow W = \frac{40.83fF}{\frac{2fF}{\mu m}} = 20.42\mu m$

NMOS : $6r = 20.41fF \Rightarrow W = \frac{20.41fF}{\frac{2fF}{\mu m}} = 10.21\mu m$

B. 3-input NAND gate and 2-input NOR gate

I. 3-input NAND gate

$C_{in} = 2r + 3r = 5r = 10fF \Rightarrow r = 2$

PMOS : $2r = 4fF \Rightarrow W = \frac{4fF}{\frac{2fF}{\mu m}} = 2\mu m$

NMOS : $3r = 6fF \Rightarrow W = \frac{6fF}{\frac{2fF}{\mu m}} = 3\mu m$

II. 2-input NOR gate

$C_{in} = 4r + 1r = 5r = 100fF \Rightarrow r = 20$

PMOS : $4r = 80fF \Rightarrow W = \frac{80fF}{\frac{2fF}{\mu m}} = 40\mu m$

NMOS : $1r = 20fF \Rightarrow W = \frac{20fF}{\frac{2fF}{\mu m}} = 10\mu m$

C. 2-input NAND gate and 3-input NOR gate

I. 2-input NAND gate

$C_{in} = 2r + 2r = 4r = 10fF \Rightarrow r = 2.5$

PMOS : $2r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

NMOS : $2r = 5fF \Rightarrow W = \frac{5fF}{\frac{2fF}{\mu m}} = 2.5\mu m$

II. 3-input NOR gate

$C_{in} = 6r + 1r = 7r = 132.94fF \Rightarrow r = 18.9914$

PMOS : $6r = 113.95fF \Rightarrow W = \frac{113.95fF}{\frac{2fF}{\mu m}} = 56.98\mu m$

NMOS : $1r = 18.99fF \Rightarrow W = \frac{18.99fF}{\frac{2fF}{\mu m}} = 9.50\mu m$

D. 3-input NAND gate, inverter A, 2-input NAND gate, and inverter B

I. 3-input NAND gate

$C_{in} = 2r + 3r = 5r = 10fF \Rightarrow r = 2$

PMOS : $2r = 4fF \Rightarrow W = \frac{4fF}{\frac{2fF}{\mu m}} = 2\mu m$

NMOS : $3r = 6fF \Rightarrow W = \frac{6fF}{\frac{2fF}{\mu m}} = 3\mu m$

II. Inverter A

$C_{in} = 2r + 1r = 3r = 23.17fF \Rightarrow r = 7.723$

PMOS : $2r = 15.447fF \Rightarrow W = \frac{15.447fF}{\frac{2fF}{\mu m}} = 7.72\mu m$

NMOS : $1r = 7.723fF \Rightarrow W = \frac{7.723fF}{\frac{2fF}{\mu m}} = 3.86\mu m$

III. 2-input NAND gate

$C_{in} = 2r + 2r = 4r = 89.44fF \Rightarrow r = 22.36$

PMOS : $2r = 44.72fF \Rightarrow W = \frac{44.72fF}{\frac{2fF}{\mu m}} = 22.36\mu m$

NMOS : $2r = 44.72fF \Rightarrow W = \frac{44.72fF}{\frac{2fF}{\mu m}} = 22.36\mu m$

由於LVS能判讀的最小精度只到小數點第二位，因此folding後的W需要整除至小數點第二位。PMOS需要foding 3次，故取$W = 22.35\ \mu m$；NMOS需要foding 5次，故取$W = 22.35\ \mu m$。

IV. Inverter B

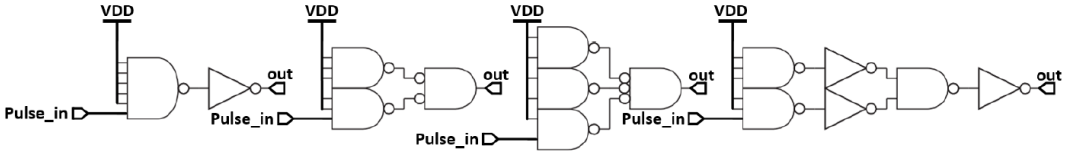
$C_{in} = 2r + 1r = 3r = 259fF \Rightarrow r = 86.3333$

PMOS : $2r = 172.67fF \Rightarrow W = \frac{172.67fF}{\frac{2fF}{\mu m}} = 86.3333\mu m$

NMOS : $1r = 86.33fF \Rightarrow W = \frac{86.33fF}{\frac{2fF}{\mu m}} = 43.1667\mu m$

由於LVS能判讀的最小精度只到小數點第二位，因此folding後的W需要整除至小數點第二位。PMOS需要foding 10次，故取$W = 86.4\ \mu m$；NMOS需要foding 10次，故取$W = 43.2\ \mu m$。

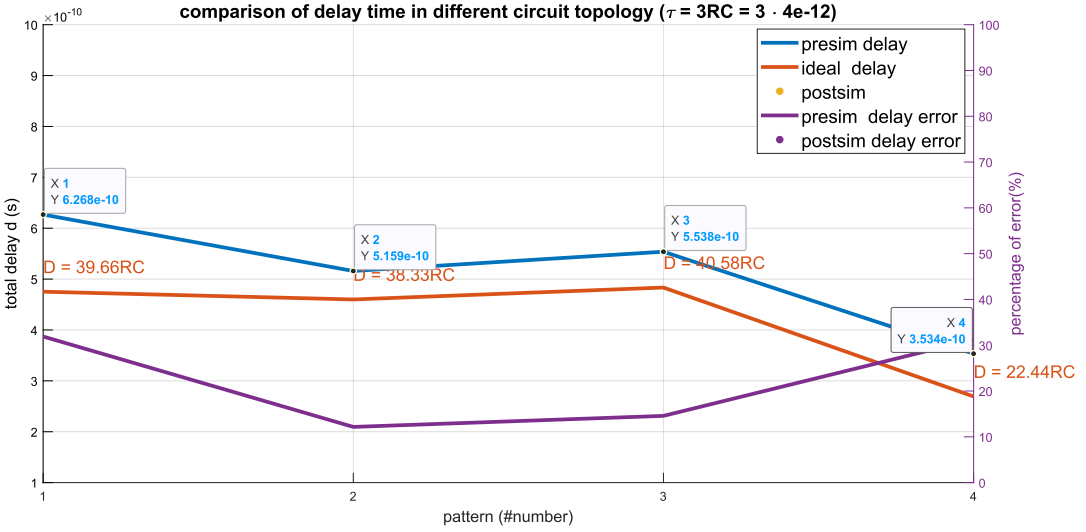
- 2D - Delay time simulation



	tdelay_rise	tdelay_fall	tdelay_fall
7-input NAND gate and inverter	4.387e-10	8.148e-10	6.268e-10
3-input NAND gate and 2-input NOR gate	3.956e-10	6.361e-10	5.159e-10
2-input NAND gate and 3-input NOR gate	4.434e-10	6.642e-10	5.538e-10
3-input NAND gate, inverter A, 2-input NAND gate, and inverter B	2.839e-10	4.229e-10	3.534e-10

- 2E - Compare 2C and 2D

comparison of delay time in different circuit topology ($\tau = 3RC = 3 \cdot 4e-12$)

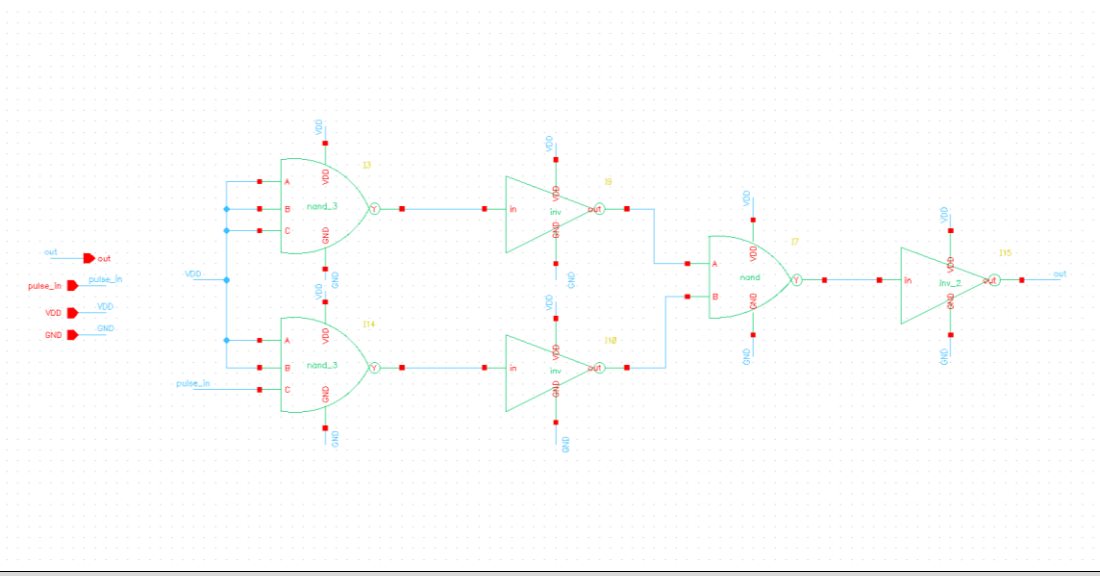


圖表解釋

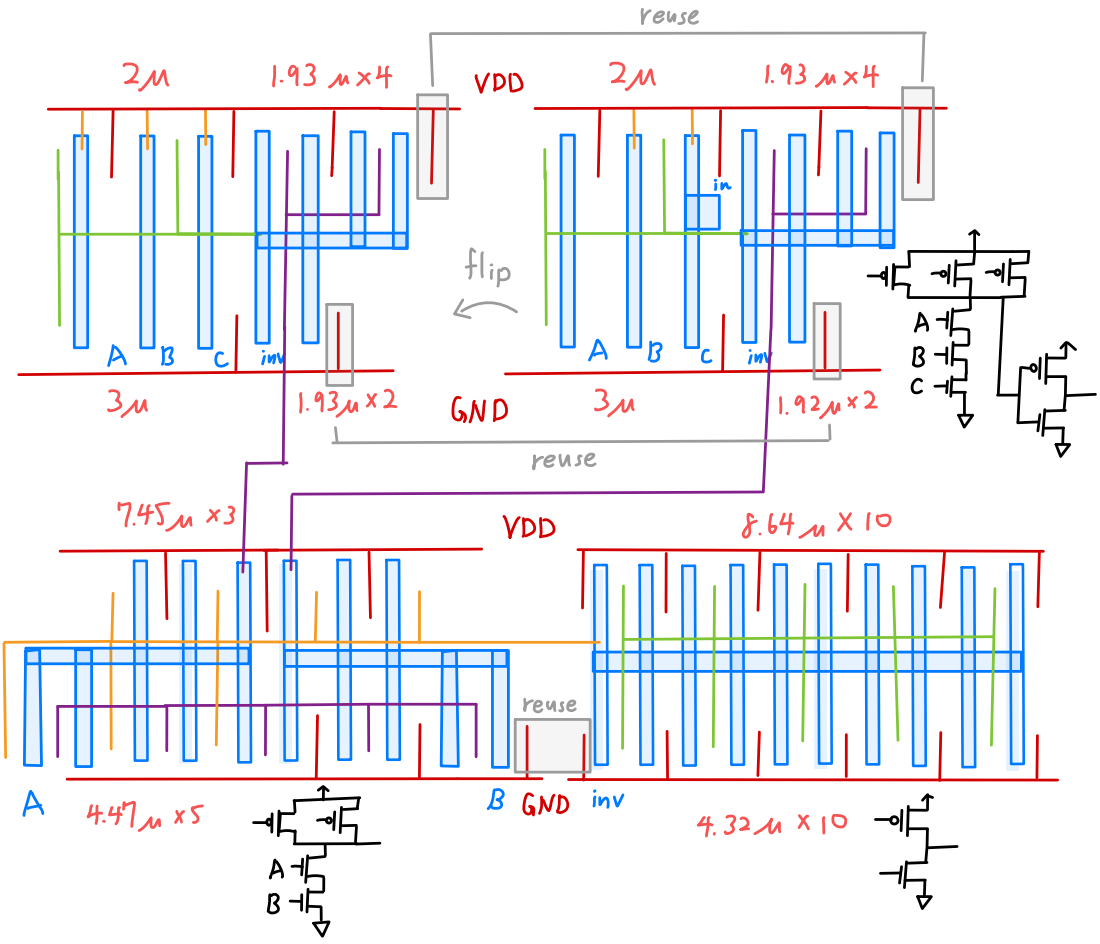
保持在同一種控制變因下去比較測量數據才有意義，因此4種電路接法都是worst case。由2A理論值計算可知第1種電路到第4種電路的delay依序為$39.3RC$, $38.33RC$, $40.58RC$, $22.44RC$，呈上$RC = 4e - 12$即可推出delay time，與測量值做比較，其中第4種電路無論是理論值還是計算值delay time都是最小，整體趨勢大致吻合。

- 2F - Layout of 3-input NAND gate, inverter A, 2-input NAND gate, and inverter B

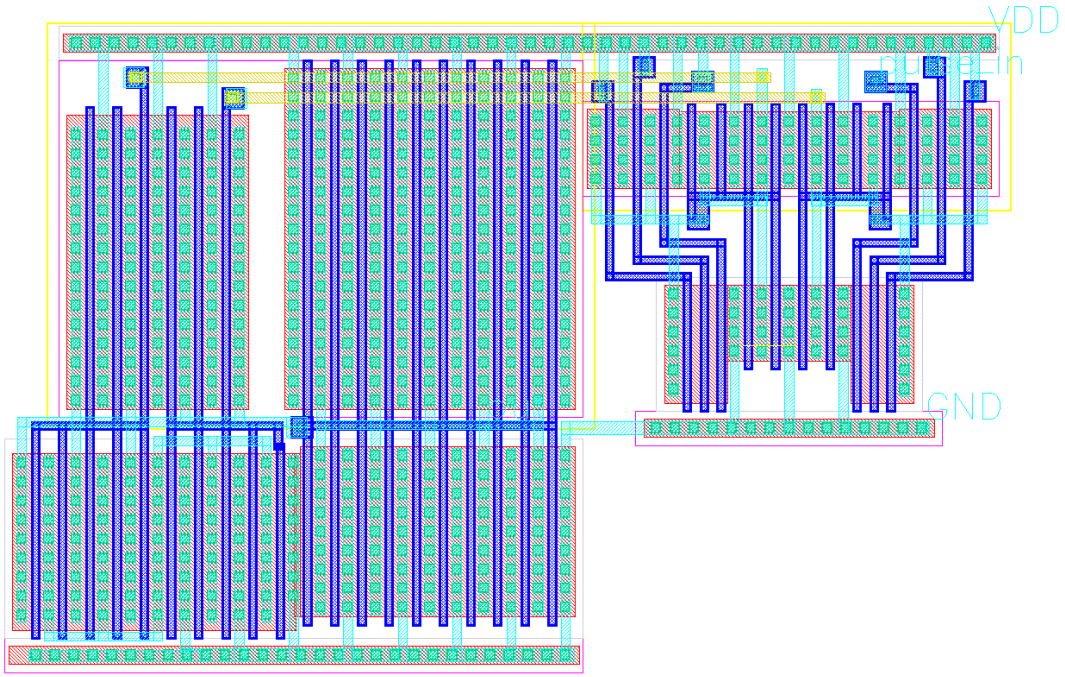
schematic

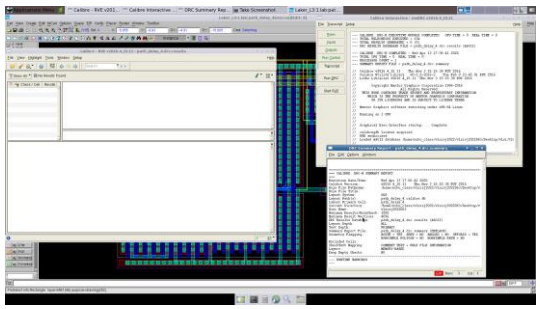
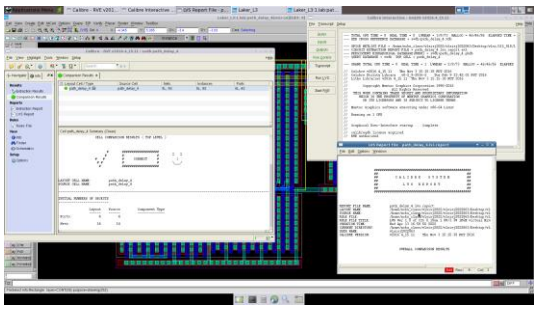


layout scratch

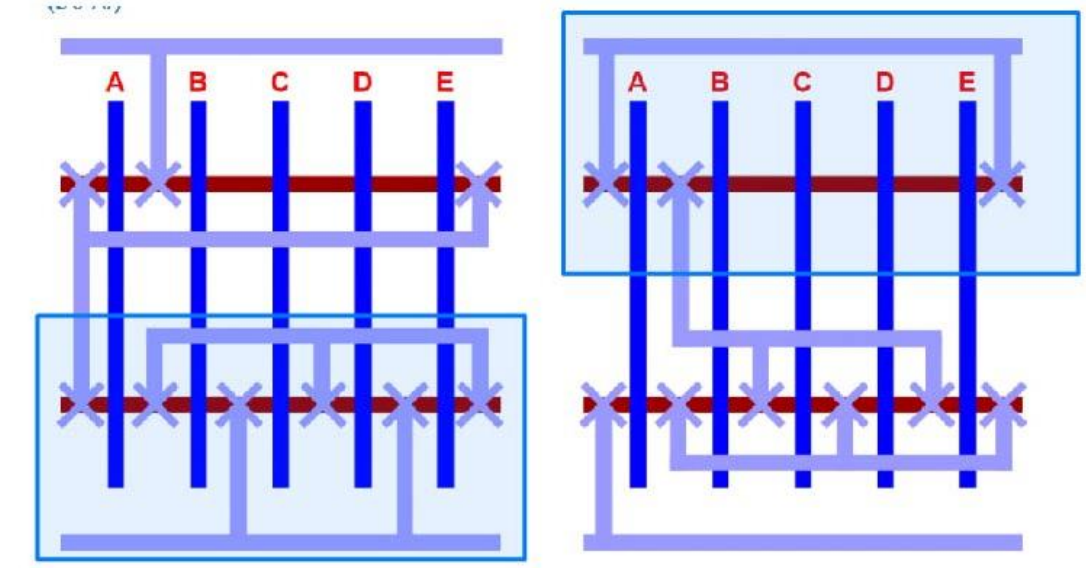


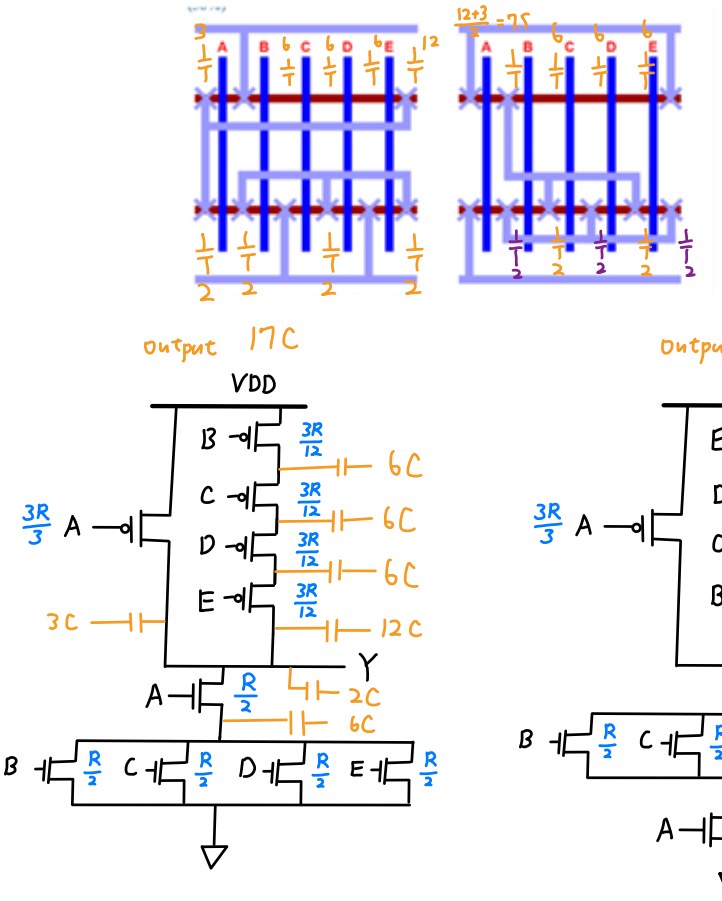
layout



DRC	LVS
	

- 3A - Which one is the better layout

電路圖


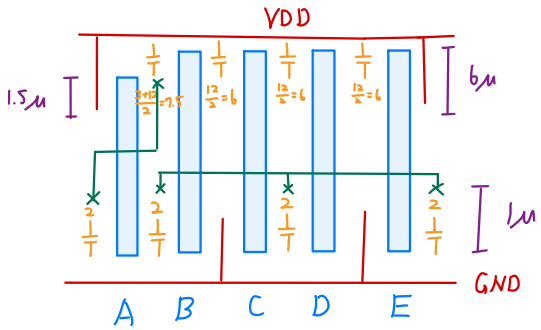
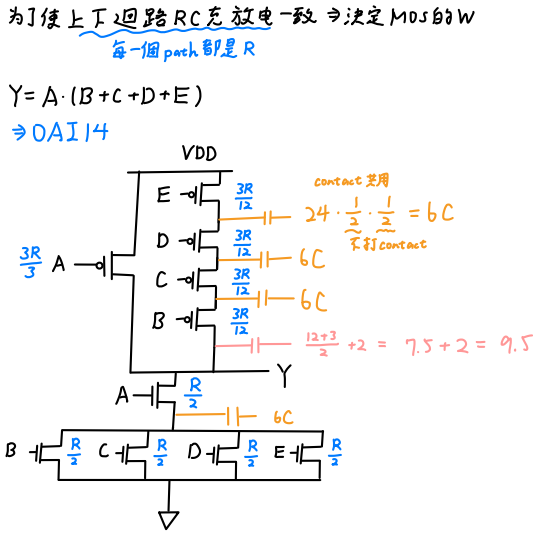


解釋

單從stick diagram看，左邊電路上面壞(輸出沒有共用contact)、下面好(輸出看到NMOS一顆)；右邊電路上面好(輸出有共用contact)、下面壞(輸出看到NMOS兩顆)，因此上下各有不同地方的好壞，無法判斷哪種layout好。(如圖一)

因此考慮上下迴路RC充放電一致，電晶體最佳sizing下，做量化評估分析layout好壞，左邊輸出電容值$C_{output} = 3C + 12C + 2C = 17C$；右邊輸出電容值$C_{output} = \frac{12+3}{2}C + 4C = 11.5C$，因此右邊的layout較好。(如圖二)

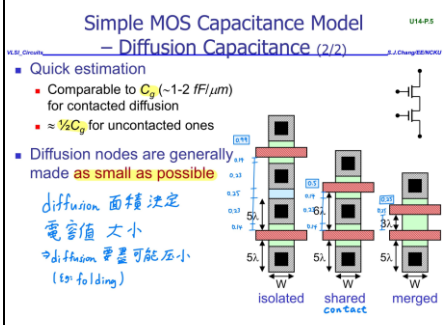
- 3B - Draw a much better one

layout	schematic
	

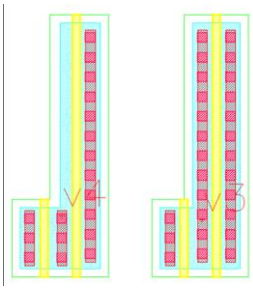
解釋

更好的layout方式就是各取所長 - 取左邊電路的下面與右邊電路的上面。

計算各個節點的寄生電容，結果如圖二所示，根據講義U14-5與助教公告的說明，需要注意兩項觀念。



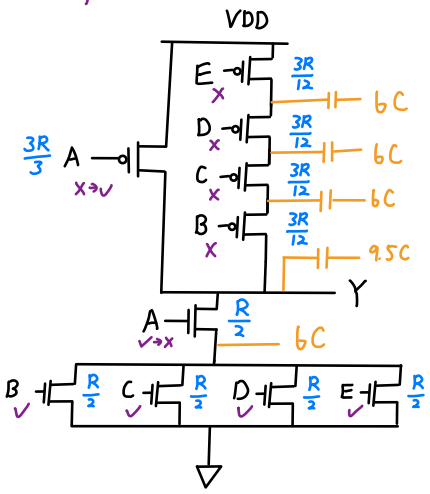
1. **diffusion的面積大小決定電容值大小，兩者成正比**，經過自己實際測試後，數值計算如左圖，兩個contact是0.99 μm、共用contact是0.5 μm、不打contact是0.25 μm，因此大致呈現4:2:1的比例，所以我們才會得到結論 - 當兩個MOS共用contact時，電容取兩個MOS的depletion capacitance的平均 $C_g = \frac{C_{g1}+C_{g2}}{2}$，若沒打contact時，depletion capacitance再砍半$\frac{1}{2}C_g$。



2. 關於不同size的電晶體共用contact的計算方式，如左圖所示，右邊layout的diffusion面積全由右邊電晶體的size所決定，而左邊layout的diffusion面積為左邊與右邊電晶體的size取平均，因此也可知道左邊的layout會比較好，layout很重要的目的就是要**極小化diffusion的面積，因為diffusion的面積與電容值成正比**。

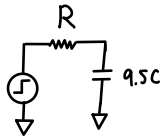
- 3C - estimate the rising or falling delay for 3B circuit

	A	B	C	D	E
pattern 1	1.8→0	1.8	1.8	1.8	1.8



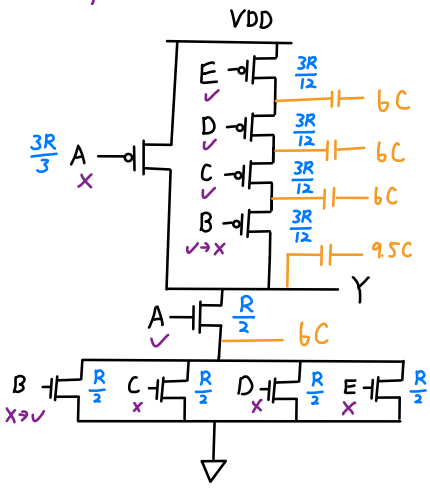
Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}}\, C_i$

rising ⇒ source is VDD



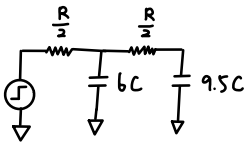
$t_{pdr} = 9.5RC$

	A	B	C	D	E
pattern 2	1.8	0→1.8	0	0	0



Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}}\, C_i$

falling ⇒ source is GND

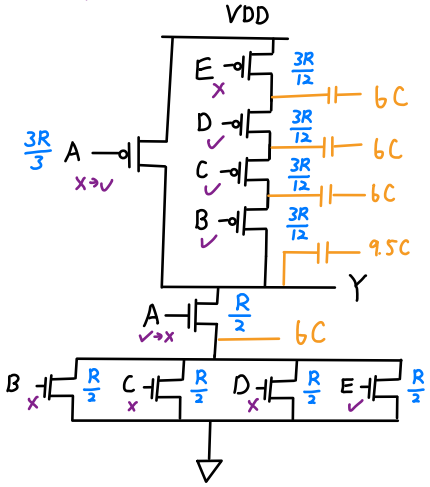


$t_{pdf} = \frac{R}{2}\cdot 6C + (\frac{R}{2}+\frac{R}{2})\cdot 9.5C$

$= 3RC + 9.5RC$

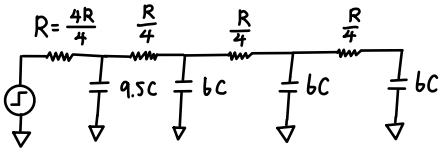
$= 12.5RC$

	A	B	C	D	E
pattern 3	1.8→0	0	0	0	1.8



Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}}\, C_i$

rising ⇒ source is VDD



$t_{pdr} = \frac{1}{4}RC(4\cdot 9.5 + 6\cdot 5 + 6\cdot 6 + 6.7)$

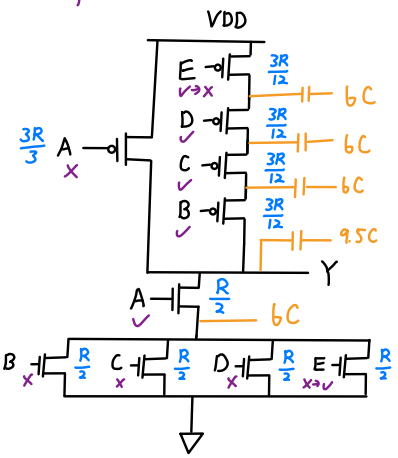
$= \frac{1}{4}RC(38+30+36+42)$

$= \frac{1}{4}RC\cdot 146$

$= 36.5RC$

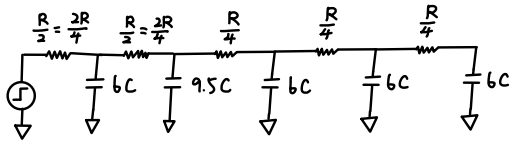
pattern 4

A	B	C	D	E
1.8	0	0	0	0→1.8



Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}} C_i$

falling ⇒ source is GND



$t_{pdf} = \frac{1}{4}RC(6\cdot2 + 9.5\cdot4 + 6\cdot5 + 6\cdot6 + 6\cdot7)$

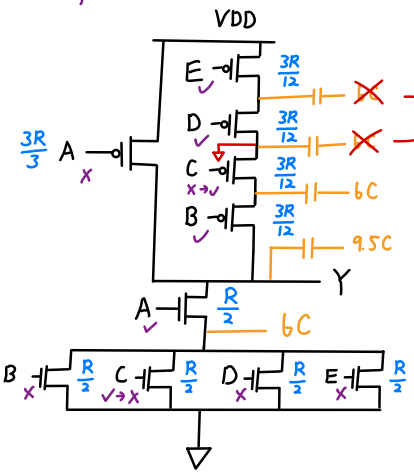
$= \frac{1}{4}RC(12 + 38 + 30 + 36 + 42)$

$= \frac{1}{4}RC \cdot 158$

$= 39.5\,RC$

pattern 5

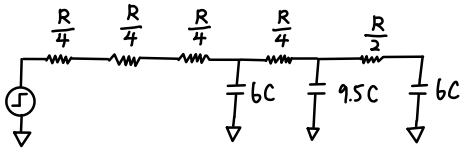
A	B	C	D	E
1.8	0	1.8→0	0	0



Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}} C_i$

D、E 已經充好電

rising ⇒ source is VDD



$t_{pdr} = \frac{1}{4}RC(6\cdot3 + 9.5\cdot4 + 6\cdot6)$

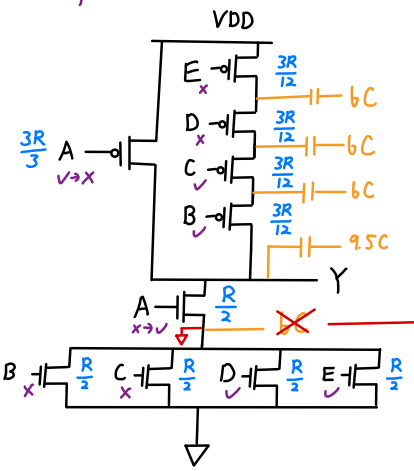
$= \frac{1}{4}RC(18 + 38 + 36)$

$= \frac{1}{4}RC(92)$

$= 23\,RC$

pattern 6

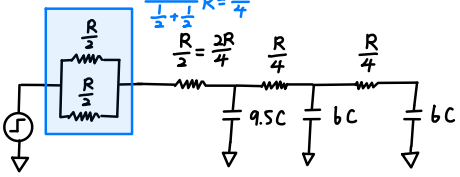
A	B	C	D	E
0→1.8	0	0	1.8	1.8



Elmore Delay Model $t_{pd} = \sum R_{i\text{-to-source}} C_i$

A 已經充好電

falling ⇒ source is GND



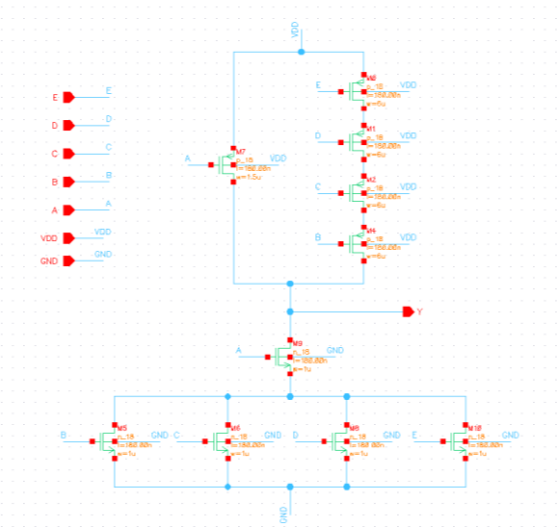
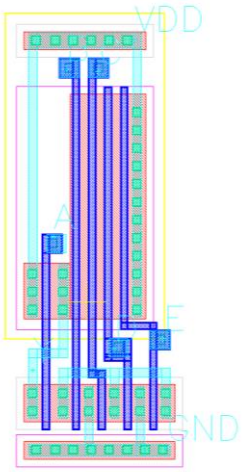
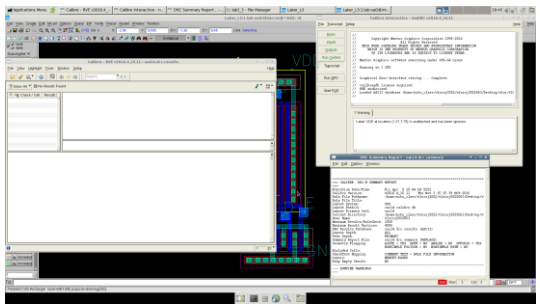
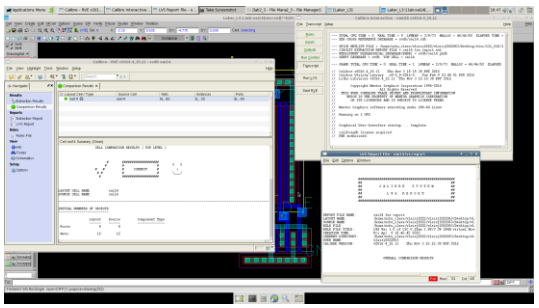
$t_{pdf} = \frac{1}{4}RC(9.5\cdot3 + 6\cdot4 + 6\cdot5)$

$= \frac{1}{4}RC(28.5 + 24 + 30)$

$= \frac{1}{4}RC \cdot 82.5$

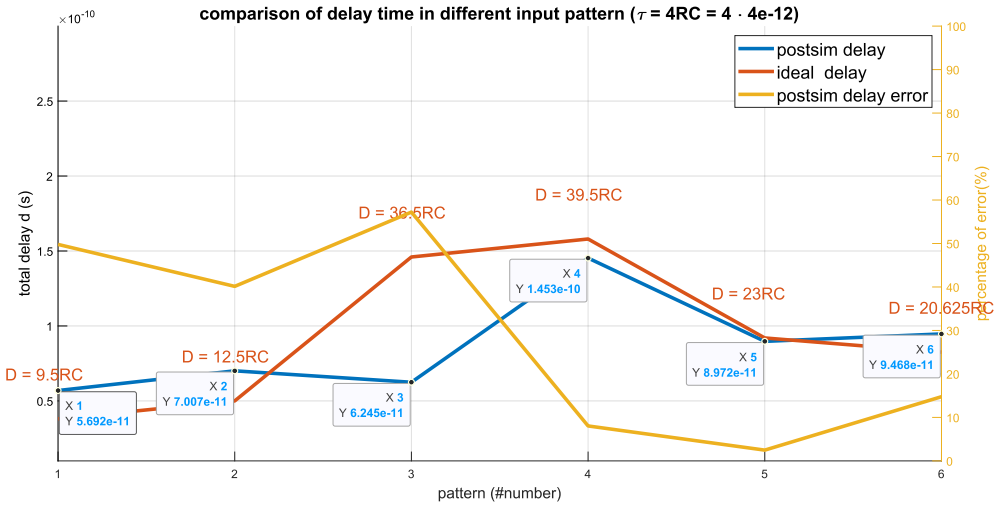
$= 20.625$

- 3D - layout of 3B circuit

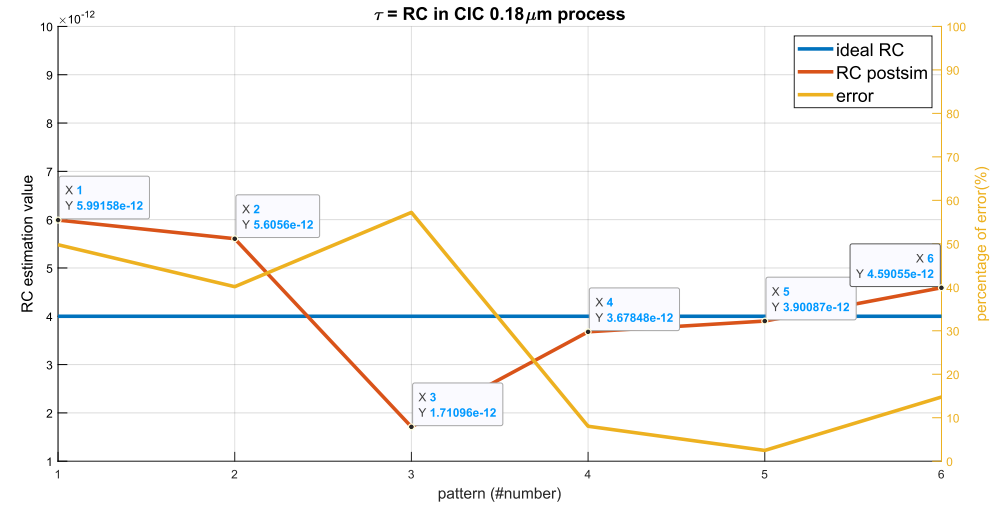
schematic

layout

DRC

LVS


	Estimation delay time t_{pdr} or t_{pdf}	HSPICE postsim simulation
Pattern 1	$9.500RC = 3.80e-11$	$5.692e-11$
Pattern 2	$12.500RC = 5.00e-11$	$7.007e-11$
Pattern 3	$36.500RC = 1.46e-10$	$6.245e-11$

Pattern 4	$39.500RC = 1.58e-10$	$1.453e-10$
Pattern 5	$23.000RC = 9.20e-11$	$8.972e-11$
Pattern 6	$20.625RC = 8.25e-11$	$9.468e-11$

comparison of delay time in different input pattern ($\tau = 4RC = 4 \cdot 4e-12$)

圖表解釋
理論值計算根據講義U20-P6，在.18製程下$3RC = 12\,ps$，，所以$1RC = 4 \cdot 10^{-12}s$，個別帶入3C小題計算每一種pattern的delay值。

- 3E - $\tau = RC$ in CIC 0.18μm process

$\tau = RC$ in CIC 0.18μm process

圖表解釋
理論值計算同上，根據講義U20-P6，在.18製程下$3RC = 12\,ps$，所以$1RC = 4 \cdot 10^{-12}s$。估測值就是把postsim模擬的delay time除以3C小題計算delay值的係數，舉例來說pattern 5的postsim模擬結果是8.972e-11(s)，而計算delay time是23RC，因此可估算$\tau = RC = \frac{8.972 \cdot 10^{-11}}{23}$。

- Conclusion

本次實驗我學到以下5大重點。

A. 熟悉HSPICE語法

尤其是第一大題，1A小題使用.DC關鍵字做穩態分析、sweep關鍵字掃描電壓、.PROBE關鍵字將以下指定變數會輸出到波型檔；1D小題、1E小題使用.MEA關鍵字在特定情況下指定節點與時間資訊輸出數據到文字檔。

B. 建立邏輯閘的linear delay model

1E小題、1F小題藉由計算值匯出至matlab做圖，建立linear delay model並與講義U20-6的理論值做比較。

$$d = \frac{t_{pd}}{\tau} = f + p = \underbrace{g}_{\text{slope}} \cdot h + \underbrace{p}_{\text{y-intercept}}$$

C. 評估不同電路架構的path delay time與最佳化一條path的delay time

第2大題最佳化4種電路架構的delay time並判斷哪種電路架構對於$H = \frac{C_{out}}{C_{in}} = \frac{1000fF}{10fF} = 100$情況下較佳，最佳化一條path的delay time的流程如下

1. 計算path effort $F = GBH$，其中$G = \prod g_i$、$B = \prod b_i$ where $b = \frac{C_{\text{onpath}}+C_{\text{offpath}}}{C_{\text{onpath}}}$、$H = \prod h_i = \frac{C_{out}}{C_{in}^{(1)}} \cdot \frac{C_{out}^{(2)}}{C_{in}^{(2)}} \cdot \ldots \cdot \frac{C_{out}^{(i)}}{C_{\text{in}}} = \frac{C_{\text{out}}}{C_{\text{in}}}$。
2. 決定要用幾級(stage)電路實現，delay time最佳值是每一級要推等效4個自己(fanout)，$F^{\frac{1}{N}} = 4 \Rightarrow N = \log F$。
3. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P$，其中$P = \sum p_i$。
4. 計算各級邏輯閘的effort均為$\hat{f} = F^{\frac{1}{N}}$。
5. 從後往前推，計算每一級的輸入電容值$\hat{f} = g\text{h} = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}$$。
6. 得到各級邏輯閘的C_{in}去決定電晶體的size，假設一個2-input NAND gate計算得$C_{in} = 15$，而計算NMOS和PMOS取size的ratio為4:1，因此NMOS的size取12、PMOS的size取3，輸入源看進去的電容才會是$12 + 3 = 15$。

D. transistor foding的layout技巧

2F小題練習部分。參照這篇文獻裡面的做圖與描述，transistor folding就是並聯2顆W砍半的電晶體，如此等效上還是看到1顆W的電晶體，以降低diffusion面積，使寄生電容降低，從線性區電流公式也可以看出流經迴路的電流還是維持一致。

$$i \propto \frac{W}{L} = \underbrace{\frac{\frac{W}{2}}{L} + \frac{\frac{W}{2}}{L}}_{\text{transistor in parallel}}$$

E. 分析邏輯閘的delay time

第3大題決定電晶體的size、計算layout優化後的寄生電容、計算六種不同輸入pattern下的delay time，分析電路的delay time的步驟如下

1. 為了使上下迴路RC充放電一致，要先決定每一個電晶體的尺寸$\frac{W}{L}$，確保每一條通路的電阻值都相同。
2. 使用RC delay model計算C值，快速方法是從一節點看有i個size是k_i的MOS，電容值即是$\sum_{i=1}^{n} k_i$，至於GND和VDD不需要計算電容值，因為電容兩端電壓固定，所以電容不會充放電。
3. (如果考慮layout優化的問題時)當兩個MOS共用contact時，電容取兩個MOS的

depletion capacitance的平均 $C_g = \frac{C_{g1}+C_{g2}}{2}$，若沒打contact時，depletion capacitance再砍半$\frac{1}{2}C_g$。

4. 決定出RC充放電值最大時的worst case。

5. 分別計算當**輸出上升**時的rising propagation delay time t_{pdr}與當**輸出下降**時的falling propagation delay time t_{pdf}。

6. 使用Elmore delay model，一次只看一個電容充放電行為並相加，計算propagation delay time $t_{pd} = \sum_{\text{nodes } i} R_{\text{i-to-source}} C_i$，代表用一階RC充放電去近似高階RC充放電I-V曲線，注意照理說取時間常數應該是$t_{pd} = R'C \ln 2$，而為求計算方便一般取的R已隱含$R' \ln 2$成分。