National Cheng Kung University
Department of Electrical Engineering

VLSI Circuits Design

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Homework #2

Due Wednesday, April 20, 9am

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※ **If not specifically mentioned in the questions, all simulations are done in CIC 0.18 μ m process, VDD=1.8V, TT Corner.**

Problem 1 – Device and Logical Effort (24%)

1A (3%) Please plot the curve IDS versus VDS for different VGS (With a step of 0.1V in the range of 0 - 1.8V), and IDS versus VGS for different VDS (with a step of 0.1V in the range of 0 - 1.8V), where the NMOS size is $\left(\frac{W}{L}\right) = \frac{6\mu m}{0.18\mu m}$

Hint: You can use the following codes to measure the VDS and VGS.

```
VG VG gnd G
VD VD gnd D
.DC D 0 1.8 0.1 sweep G 0 1.8 0.1
.probe i(MMnmos1) vds(MMnmos1) vgs(MMnmos1)
```

1B (2%) Please plot the curve IDS versus VDS for different VGS (With a step of 0.1V in the range of 0 - 1.8V), and IDS versus VGS for different VDS (with a step of 0.1V in the range of 0 - 1.8V), where the PMOS size is $\left(\frac{W}{L}\right) = \frac{15\mu m}{0.18\mu m}$

1C (2%) Please modify the curves from 1A and merge the I-VDS and I-VGS into a 3-dimension curve in a single plot. You can plot it by Matlab 、Waveview or Hspice.

1D (3%) Please plot the transfer curve of an inverter with $\left(\frac{W}{L}\right)_N = \frac{2\mu m}{0.18\mu m}$、$\left(\frac{W}{L}\right)_P = \frac{4\mu m}{0.18\mu m}$. And find the threshold voltage (Vin = Vout) of the inverter. Will the threshold voltage equal to VDD/2 (0.9V)? If not, fix the NMOS and use HSPICE to find the proper aspect ratio for PMOS which makes the threshold voltage equal to VDD/2.

Hint: You can use the following codes to measure the threshold voltage.

```
Xinv in out vdd gnd inv
Vin in gnd 0
.DC Vin 0 1.8 0.01
.MEAS DC Vth FIND V(out) WHEN V(out)=V(in)
```

In the following questions, you will use HSPICE to measure the logical effort of a few different kinds of gates. According to logical effort:

$$\textbf{Delay} = t_{parasitic} + t_{gate} \times h$$

For each of the following gates, extract the best fit values for $t_{parasitic}$ and t_{gate}.

Note: $t_{avg} = \frac{1}{2}(t_{rising} + t_{falling})$

1E (5%) Plot delay vs. fan-out for a fan-out of 1 to 7 in increments of 1. Find $t_{parasitic}$ and t_{gate} by simulating the inverter chain shown in **Fig. 1a**

Hint: You can use the following codes to measure the delay.

```
.measure tran tdelay_rise trig v(in) val=0.9 td=0 fall=2 targ v(out) val=0.9 rise=2
.measure tran tdelay_fall trig v(in) val=0.9 td=0 rise=2 targ v(out) val=0.9 fall=2

.measure tran tdelay_avg param = '(tdelay_rise+tdelay_fall)/2'
```

Note: $\left(\frac{W}{L}\right)_N = \frac{2\mu m}{0.18\mu m}$ $\left(\frac{W}{L}\right)_P = \frac{6\mu m}{0.18\mu m}$

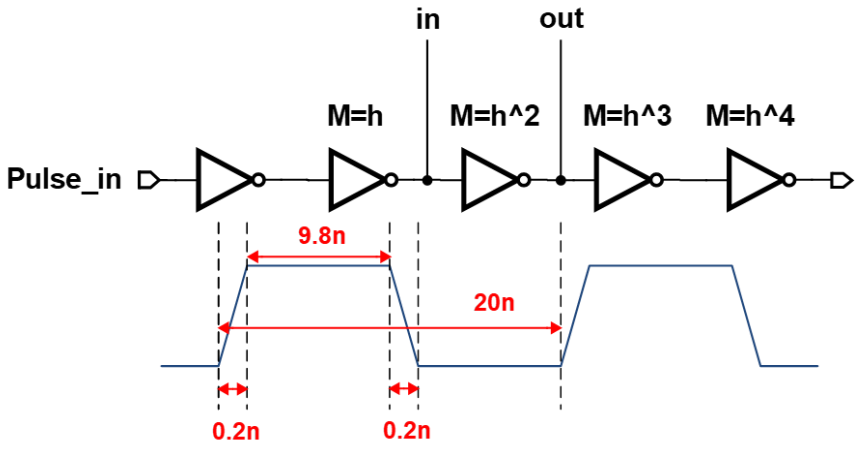


Fig.1a

1F (5%) Plot delay vs. fan-out for a fan-out of 1 to 7 in increments of 1. Find $t_{parasitic}$ and t_{gate} by simulating the NOR chain shown in **Fig. 1b**

Note: $\left(\frac{W}{L}\right)_N = \frac{2\mu m}{0.18\mu m}$ $\left(\frac{W}{L}\right)_P = \frac{18\mu m}{0.18\mu m}$

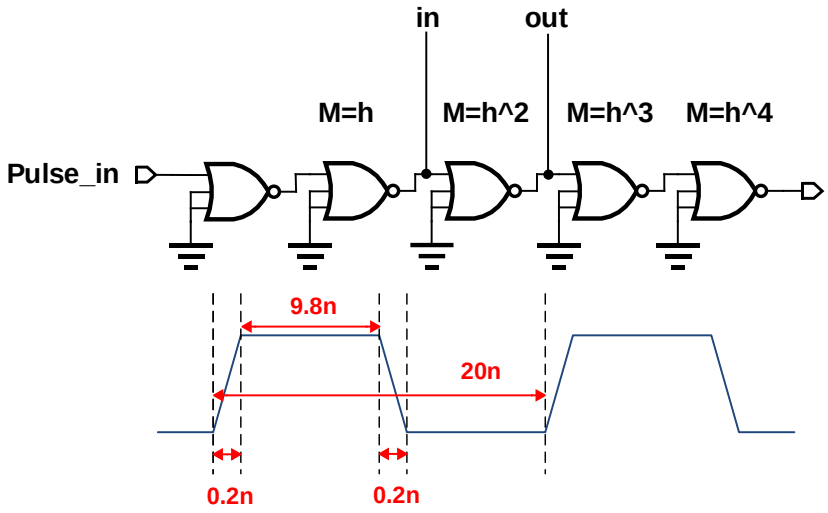


Fig.1b

1G (4%) Please compare the result of the simulation in **1E** and **1F** with the lecture notes (Unit 20) and make some comments on it.

Problem 2 – Delay Estimation and Optimization (40%)

According to the slider of the class, logical effort concept helps us to make decisions like using a simple model of delay, allowing back-of-the envelop calculation and making rapid comparisons between alternatives. **Fig.2a** is four designs of a 6-input AND gate. In this problem you will use the concept learned in class to minimize the path delay of each topology of 6-input AND gate. **(Your calculation answer should be round it to the nearest hundredth)**

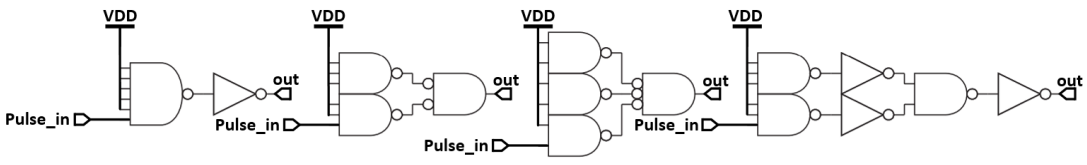


Fig.2a

2A (4%) For the logic path from **Pulse_in** to **out** shown in the **Fig.2a,** please find the **path logical effort**, and the **total path effort** for each topology.

Note:

a. **CG=2fF/μm**
b. **Kn'/Kp' = 2/1**
c. **Assume first stage Cin=10fF**
d. **Assume 1000fF output loading**

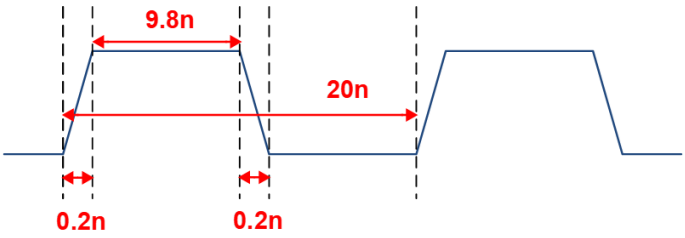
2B (6%) To minimize the path delay, what should **electrical effort** per stage for each topology be?

2C (9%) Size the gates in each topology to minimize the delay from **Pulse_in** to **out. (Notice: You should design first stage Cin=10fF)**

2D (6%) Use your size from **2C**, find the delay from **Pulse_in** to **out** by simulating the circuit shown in **Fig.2a (Notice: 1000fF output loading)**

Note: $t_{avg} = \frac{1}{2}(t_{rising} + t_{falling})$

Input signal:



2E (5%) Make a comparison between your calculation result and simulation result.

2F (10%) Create the layout of the **fastest** (according to the simulation result) circuit in **Fig.2a**. Please show the "No Error Figure" of the DRC and LVS verification, and paste the layout figure.

Note: You must fold the transistor to ensure $W_{max} \leq 10um$

Problem 3 –Elmore Delay Model and Layout Effect on Diffusion Capacitances (36%)

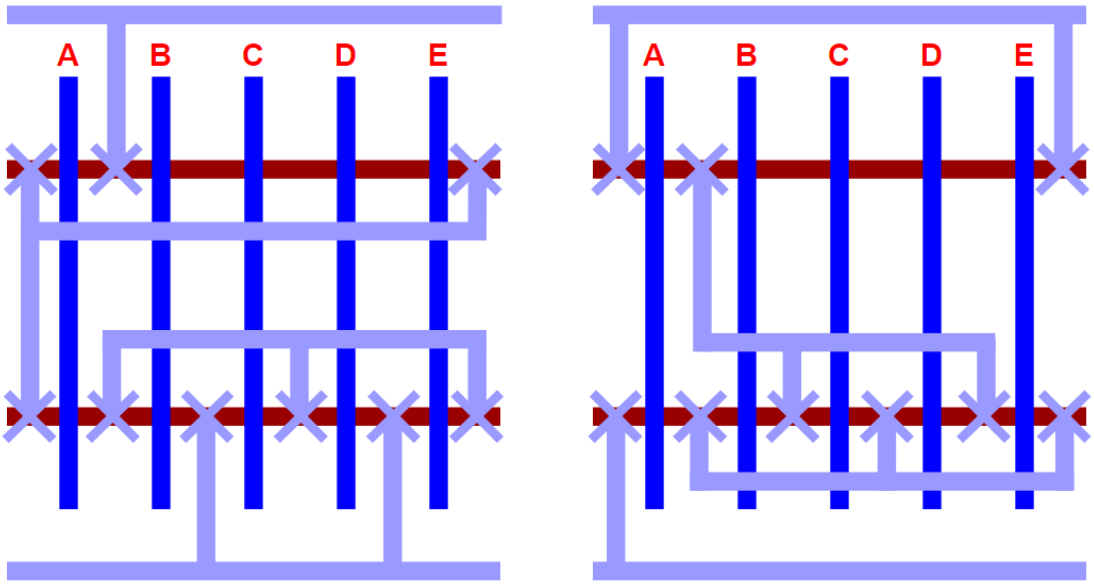


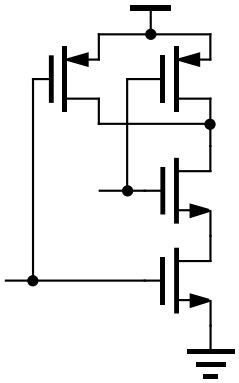
Fig.3 Stick Diagram for Problem 3

3A (3%) Observe the stick diagram in **Fig. 3**, which one is the better layout? Why? Can you draw a much better one? If so, try to draw a stick diagram.

3B (6%) Draw the schematics that corresponds to the two stick diagrams in **Fig. 3**, and find the suitable size of all transistors. Please estimate the diffusion capacitances on the circuit nodes and draw it on the schematic (You must consider layout effect on diffusion capacitances).

(Hint: The size of the NMOS of input A is $\left(\frac{W}{L}\right)_N = \frac{1\mu m}{0.18\mu m}$ and the Kn'/Kp' = 3/1)

(You don't have to draw the schematic by Virtuoso. Just draw a brief schematic like the following picture. Note that this is not the answer of this problem.)



3C (10%) Estimate the rising or falling delays for **the best circuit in 3A**. If the input signals are the patterns in Table 1, please calculate these delays by Elmore delay model and assume that the circuit drives no loading at the output node. **(Hint: The NMOS of input A have R/2 and 2C, and represent your answer with τ =RC. You must consider layout effect on diffusion capacitances)**

	A	B	C	D	E
Pattern1	1.8→0	1.8	1.8	1.8	1.8
Pattern2	1.8	0→1.8	0	0	0
Pattern3	1.8→0	0	0	0	1.8
Pattern4	1.8	0	0	0	0→1.8
Pattern5	1.8	0	1.8→0	0	0
Pattern6	0→1.8	0	0	1.8	1.8

Table.1

3D (15%) Create the layout of the best stick diagram in **3A**, and measure the rising or falling delays from post-layout simulation(R+C+CC) under all conditions in Table.1. Please show the "No Error Figure" of the DRC and LVS verification, and paste the layout figure. Is the result the same as the calculation in **3C**?

3E (2%) According to the result of the simulation, what do you think about the τ =RC value for CIC 0.18μm process?

****Important Notes****

1. 12pt character size in your report.

2. Please invert the color of all your schematics, layouts, and waveforms.

3. Do not copy.

4. No late homework will be accepted. When it is due, it is due.

5. It is needless to print your report. Please prepare the needed files and compress your HW shown as below and upload to