National Cheng Kung University

Department of Electrical Engineering

VLSI Circuits Design

Soon-Jyh Chang **Homework#1**

Due Wednesday, March 30, 9am

TA :鄭愷誠　Mail :brian87128@sscas.ee.ncku.edu.tw

Problem 1 Transmission Gates (40%)

1A

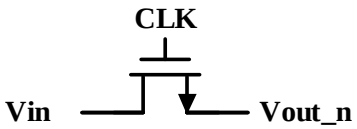

Fig.1-1

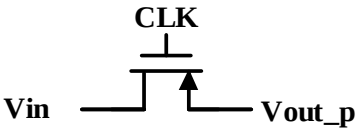

Fig.1-2

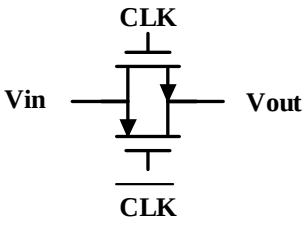

Fig.1-3

$$\left(\frac{W}{L}\right)_p = \left(\frac{1.0um}{0.18um}\right)$$

$$\left(\frac{W}{L}\right)_n = \left(\frac{1.0um}{0.18um}\right)$$

Fig.1-4

Fig.1-1 is a NMOS pass transistor, Fig.1-2 is a PMOS pass transistor and Fig.1-3 is a Transmission gate. Fig.1-4 is the size of the transistors.

(a) Using Cadence virtuoso to draw a transistor level schematic for Fig.1-1, Fig1-2, and Fig.1-3. **Please paste the schematic on the report.**

(b) Simulate the circuit using the given test pattern (Table.1). (Please add the loading as the code in Fig.1-6.)　**Please paste input and output waveforms.**

(c) Compare three output waveforms. **Please explain the reasons why these three outputs are different and why a transmission gate is more widely used**.

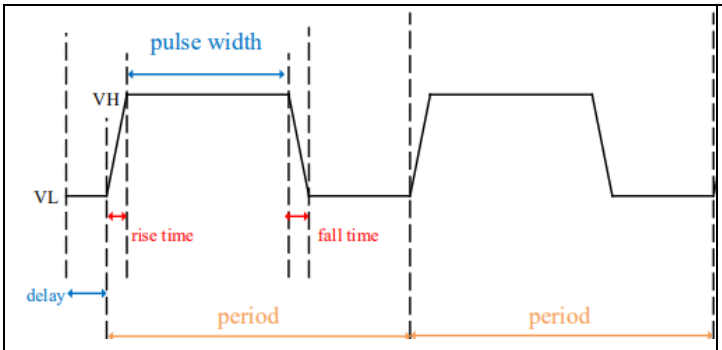

Fig.1-5

```
cload1 vout_n gnd 0.1p
cload2 vout_p gnd 0.1p
cload3 vout   gnd 0.1p
```

Fig.1-6

Table. 1

	delay	Rising time	Falling time	Pulse width	period
Vin	10n	100p	100p	39.8n	80n
CLK	20n	100p	100p	39.8n	80n

*You need to generate $\overline{CLK}$ by inverting circuit. (VL=0V and VH=1.8V)

1B

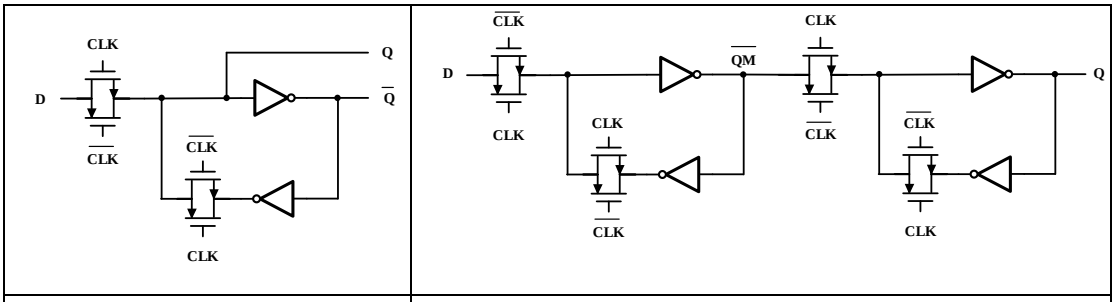

Fig.1-7

Fig.1-8

Fig.1-7 is a D latch. Fig.1-8 is a D flip-flop.

Transmission gate size: $(\frac{W}{L})_p = \frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n = \frac{1\mu m}{0.18\mu m}$

Inverter size: $(\frac{W}{L})_p = \frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n = \frac{0.5\mu m}{0.18\mu m}$

(a) Using Cadence virtuoso to draw a transistor level schematic for Fig.1-7 and Fig.1-8. **Please paste the schematic on the report.**

(b) Simulate the circuit using the given test pattern (Table2). **Please paste input and output waveforms.**

Table. 2

	delay	Rising time	Falling time	Pulse width	period
D	10n	100p	100p	39.8n	80n
CLK	20n	100p	100p	29.8n	60n

*You need to generate $\overline{CLK}$ by inverting circuit. (VL=0V and VH=1.8V)

Inverter size: $(\frac{W}{L})_p = \frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n = \frac{0.5\mu m}{0.18\mu m}$

(c) Create layout for Fig.1-7 and Fig.1-8 and perform verification (DRC and LVS). Please paste your layout and show the no error figures of DRC and LVS.

Problem2 Multiplexers (20%)

2A

Fig.2-1 is a transmission gate multiplexer.

Transmission gate size: $(\frac{W}{L})_p = \frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n = \frac{1\mu m}{0.18\mu m}$

(a) Using Cadence virtuoso to draw a transistor level schematic for Fig.2-1. Please paste the schematic on the report.

(b) Simulate the circuit using the given test pattern (Table. 3). Please paste input and output waveforms.

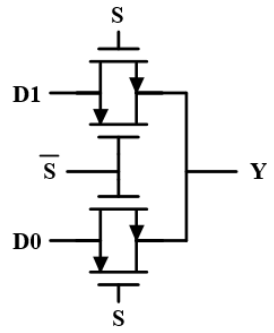

Fig.2-1

Table. 3

	delay	Rising time	Falling time	Pulse width	period
D1	10n	100p	100p	79.8n	160n
D0	10n	100p	100p	39.8n	80n
S	20n	100p	100p	19.8n	40n

*You need to generate $\bar{S}$ by inverting circuit. (VL=0V and VH=1.8V)

2B

(a) Using Cadence virtuoso to draw a transistor level schematic for two different types of multiplexers (compound AOI22 and pair of tristate inverters, etc.). Please paste the schematic on the report.

Transistor size: $(\frac{W}{L})_p = \frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n = \frac{0.5\mu m}{0.18\mu m}$

(b) Simulate the circuit using the given test pattern (Table. 3). Please paste input and output waveforms.

(c) Create layout for Fig.2-1 and two different types of multiplexers (compound AOI22 and pair of tristate inverters, etc.), and perform verification (DRC and LVS). Please paste your layout and show the no error figures of DRC and LVS.

Problem 3 Combinational logic design (40%)

Funtion1: $Y = \overline{ABC + D}$ Funtion2: $Y = \overline{(AB + C) \cdot D}$

Transistor size: $(\frac{W}{L})_p = \frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n = \frac{0.5\mu m}{0.18\mu m}$

3A

(a) Using Cadence virtuoso to draw a transistor level schematic for a compound CMOS logic gate for Funtion1 and Funtion2.

(b) Simulate the circuit of Funtion1 and Funtion2 using the given test pattern (Table. 4). Please paste input and output waveforms.

Table. 4

	delay	Rising time	Falling time	Pulse width	period
A	10n	100p	100p	79.8n	160n
B	10n	100p	100p	39.8n	80n
C	10n	100p	100p	19.8n	40n
D	10n	100p	100p	9.8n	20n

(c) Create layout the circuit of Funtion1 and Funtion2 and perform verification (DRC and LVS). Please paste your layout and show the no error figures of DRC and LVS.

3B

Table. 5

Input				**Output**							
A	**B**	**C**	**D**	**O1**	**O2**	**O3**	**O4**	**O5**	**O6**	**O7**	**O8**
0	**X**	**X**	**X**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
1	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**
1	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**
1	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**
1	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**
1	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
1	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Transistor size: $(\frac{W}{L})_p = \frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n = \frac{0.5\mu m}{0.18\mu m}$

(a) Using Cadence virtuoso to draw the logic circuit diagram for Table. 5

(b) Simulate the circuit using the given test pattern (Table. 6). Please paste input and output waveforms.

(c) Create layout the circuit and perform verification (DRC and LVS). Please paste your layout and show the no error figures of DRC and LVS.

(d) Extract parasitic effect (PEX, C+CC) for your layout and do post-simulation using same test pattern (Table6). Then, paste the input and output waveforms.

Table. 6

	delay	Rising time	Falling time	Pulse width	period
A	10n	100p	100p	79.8n	160n
B	10n	100p	100p	39.8n	80n
C	10n	100p	100p	19.8n	40n
D	10n	100p	100p	9.8n	20n

-----Important Notes-----

1. 12pt character size in your report.
2. Please invert the color of all your schematics, waveforms and layout.
3. **DO NOT COPY**
4. **No late homework will be accepted. When it is due, it is due.**
5. It is needless to print your report. Please compress the needed files and report shown as below. Then upload your compressed file to moodle website.