National Cheng Kung University
Department of Electrical Engineering

VLSI Circuits Design 2022

Soon-Jyh Chang **Homework#5**

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Due on 2022/06/15 ,Wednesday ,9:00

Use 'cic018.l', TT corner, VDD = 1.8V to do every simulation.

Problem 1 - Design 6T SRAM

1A

Please design a 6T-SRAM(as shown in Fig.1) with the clock signal(CLK) and control signals (WE and RE). WE is write enable mode, and RE is read enable mode. You should use pre-charge circuit, read circuit and write circuit to enable 1-bit READ and WRITE function work correctly.

(**Hint** : You can refer to pages 16 of Unit 46 : Memories in lecture notes)

You should simulate the following four patterns to check your design can work correctly:

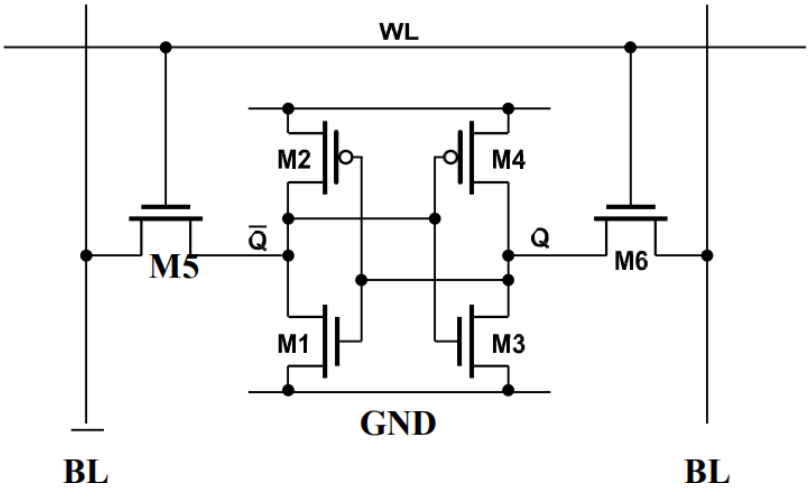


Fig.1 6T SRAM cell

(1) The stored data(Q) is 0, RE is **HIGH**.

(2) The stored data(Q) is 1, RE is **HIGH**.

(3) The stored data(Q) is 0, WE is **HIGH**, write data is 1.

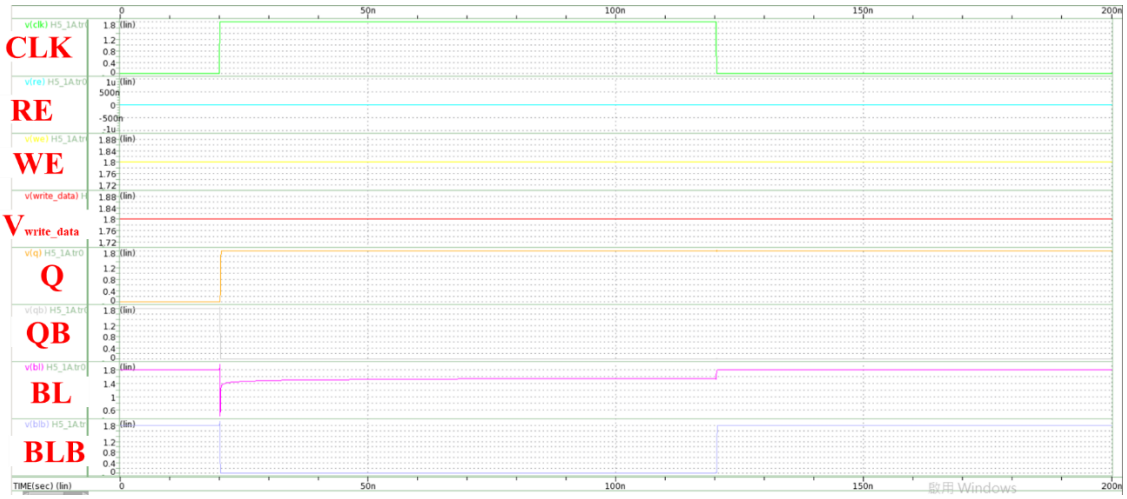
(4) The stored data(Q) is 1, WE is **HIGH**, write data is 0.

Please paste the simulation result in your report with the following signals: CLK, WE,

RE, WL, V_{write_data}, BL, BLB, Q, and QB.

For example, if we want to write 1, the WE will turn on and RE will turn off.

Then, Q will change from 0 to 1.



1B

Please estimate the read static noise margin (SNM) of the SRAM cell you design in **1A**. The method is described as follows:

First, the feedback from the cross-coupled inverters is broken and note that the wordline and bitline are held at VDD during a read, as shown in Fig.2(a).

Next, the VTC(Voltage Transfer Curve) of the "inverter" formed by half of the SRAM cell is found by sweeping V_1 (the inverter's input) from 0 to VDD and measuring V_2 (the inverter's output). This plot is then used to construct the "butterfly plot", which is representative of the two halves of the cell driving each other, as shown in Fig.2(b).

The read SNM is the side length of the maximum possible square that can fit inside of the butterfly plot.

You do not have to calculate the size of this maximum square, but you should submit the butterfly plot (generated by HSPICE or other software) and graphically indicate the SNM. (Note: only simulate the 6T-SRAM without any other control signals.)

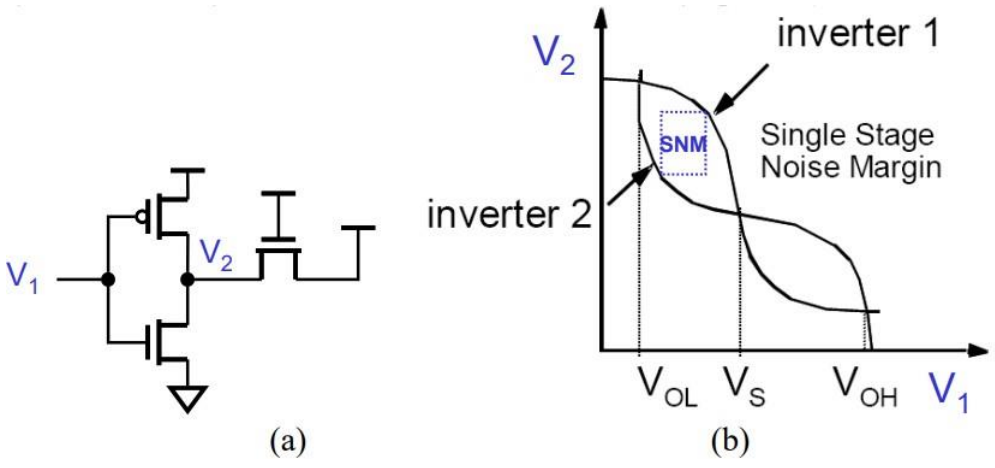


Fig.2 (a)Testing method of the read SNM (b)The butterfly plot used to find SNM

1C

Please estimate the write noise margin (WNM) of the SRAM cell you design in **1A**. The method is described as follows:

During a write, VDD is applied to the wordlines, and the value to be written into the memory cell is driven onto the bitlines. Again, the feedback from the cross-coupled inverters is broken, and the VTC of the "inverters" are measured. Note however that in this case, the VTCs of the two halves of the SRAM are no longer the same (since one of the bitlines is driven to 0V, while the other to VDD), as shown in Fig.3(a). These VTCs are used to create a butterfly plot, and the WNM is the side length of the largest square that can fit inside of the butterfly plot, as shown in Fig.3(b).

You do not have to calculate the WNM, but you should generate the butterfly plot (again by HSPICE or other software) and graphically indicate the WNM. (Note: only simulate the 6T SRAM without any other control signals.)

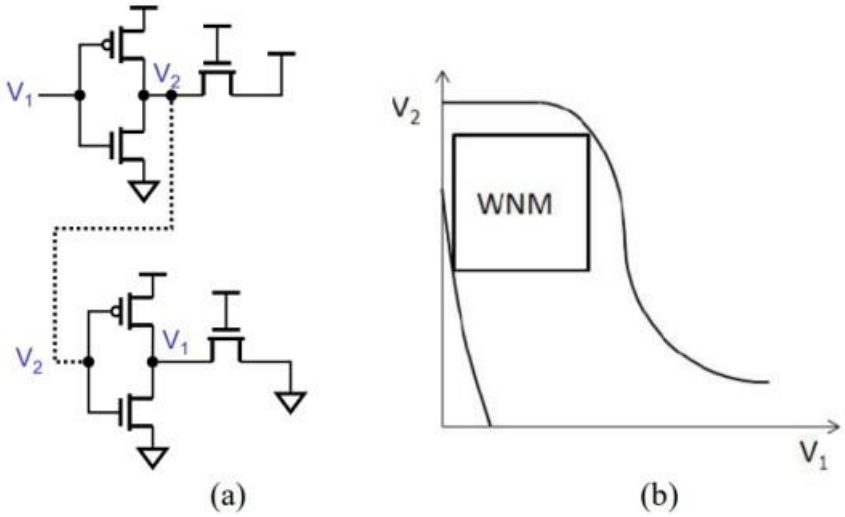


Fig.3 (a)Testing method of the WNM (b)The butterfly plot used to find WNM

Problem 2 – Characterizing Sequencing Element Delay

2A

Fig.4 shows a latch. Assume that the latch is loaded with fan-out of 3.

The size of transmission gate: $(\frac{W}{L})_p=\frac{1.5\mu m}{0.18\mu m}$, $(\frac{W}{L})_n=\frac{1.5\mu m}{0.18\mu m}$

The size of inverter: $(\frac{W}{L})_p=\frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n=\frac{0.5\mu m}{0.18\mu m}$

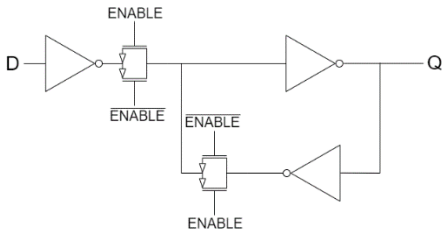


Fig.4 latch

Please use HSPICE to find t_{setup}, t_{ccq} and t_{pdq} of a latch and finish the following sheet.

(t_{pdq} is 5% greater than minimum value of t_{DQ})

You should use ***ENABLE***, $\overline{\textbf{\textit{ENABLE}}}$ and V_{data} with the falling and rising time of 80ps as shown in Fig.5 to simulate.

	t_{setup}	t_{ccq}	t_{pdq}
value			

(Hint: you may use PWL(t_1 v_1 t_2 v_2 t_3 v_3……) or Pulse (v_1 v_2 t_d t_r t_f width period))

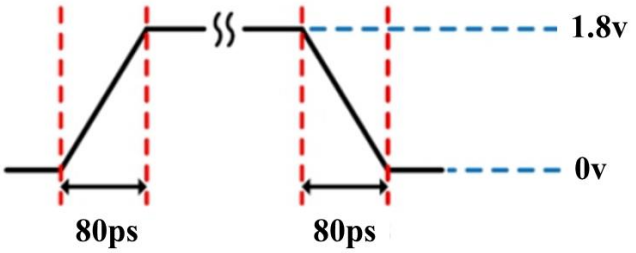


Fig.5 The falling and rising time of ***ENABLE***, $\overline{\textbf{\textit{ENABLE}}}$ and V_{data}

You can refer to the following code to calculate the t_{DCr} , t_{CQ} and t_{DQ}.

```
.measure tran tdcr trig v(D)   val=0.9 rise=1 targ v(clk) val=0.9 rise=1
```

2B

Please use waveview to plot the curve of t_{DCr} vs t_{CQ} and t_{DCr} vs t_{DQ} and merge into one figure.

2C

Fig.6 shows a conventional CMOS flip-flop. Assume that the flip-flop is loaded with fan-out of 4.

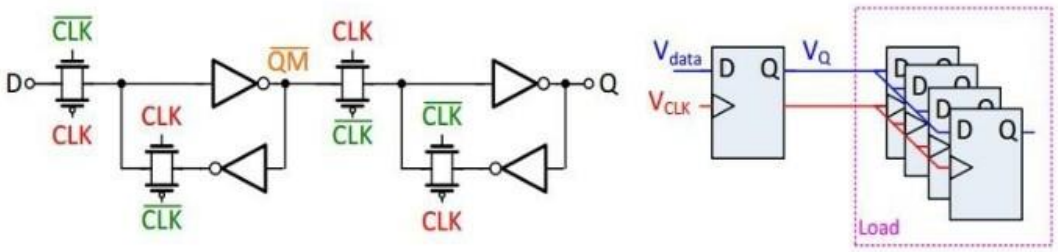


Fig.6 A conventional CMOS flip-flop

The size of transmission gate:$(\frac{W}{L})_p=\frac{1.5\mu m}{0.18\mu m}$, $(\frac{W}{L})_n=\frac{1.5\mu m}{0.18\mu m}$

The size of inverter: $(\frac{W}{L})_p=\frac{1\mu m}{0.18\mu m}$, $(\frac{W}{L})_n=\frac{0.5\mu m}{0.18\mu m}$

Please using HSPICE to find t_{setup0} , t_{pcq0} , t_{ccq0} , $-t_{hold0}$, t_{setup1} , t_{pcq1} , t_{ccq1} , $-t_{hold1}$, t_{ar} and t_{af} of a Conventional CMOS flip-flop and finish the following sheet.

You should use $\boldsymbol{CLK}$,$\overline{\boldsymbol{CLK}}$ and V_{data} with the falling and rising time of 80ps to simulate as shown in Fig.7.

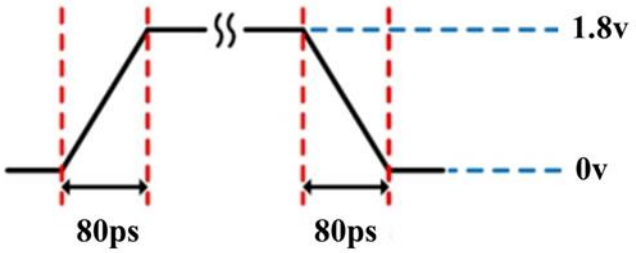


Fig.7 The falling and rising time of $\boldsymbol{CLK}$,$\overline{\boldsymbol{CLK}}$ and V_{data}

(Hint: you may use PWL(t_1 v_1 t_2 v_2 t_3 v_3……) or Pulse (v_1 v_2 t_d t_r t_f width period))

	t_{setup0}	t_{pcq0}	t_{ccq0}	$-t_{hold0}$
value				
	t_{setup1}	t_{pcq1}	t_{ccq1}	$-t_{hold1}$
value				
	t_{ar}	t_{af}		
value				

	explain
t_{setup0}	
t_{pcq0}	
t_{ccq0}	
$-t_{hold0}$	
t_{setup1}	
t_{pcq1}	
t_{ccq1}	

$-t_{hold1}$	
t_{ar}	
t_{af}	

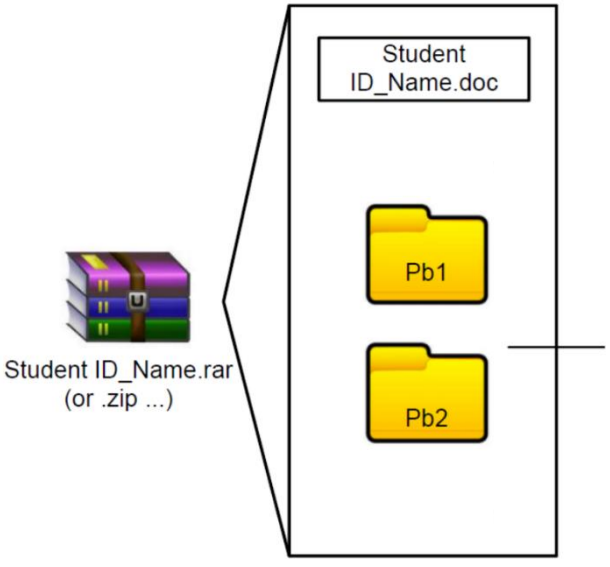
2D

Please use waveview to plot the curve of t_{DC} vs t_{CQ} concluding four cases(D rises Q rises, D rises Q falls, D falls Q rises, D falls Q falls) and merge into one figure.

(Note : You should sweep the same time when you merge four cases t_{CQ} into one figure.)

Note:

1. It is needless to print your report. Please compress the needed files and report shown as below. Then upload your compressed file to moodle website.12pt character size.
2. 12pt character size in your report.
3. Change the background color of all your figures, schematic, and waveforms, to white.
4. **Do not copy**
5. **No late homework will be accepted. When it is due, it is due.**



Problem 1:
Pb1_A.cir,
Pb1_A.sp
Pb1_B.cir,
Pb1_B.sp,
Pb1_C.cir,
Pb1_C.sp

Problem 2:
Pb2_A.cir,
Pb2_A.sp,
Pb2_C.cir
DFQF.sp,
DRQR.sp,
DFQR.sp,
DRQF.sp,