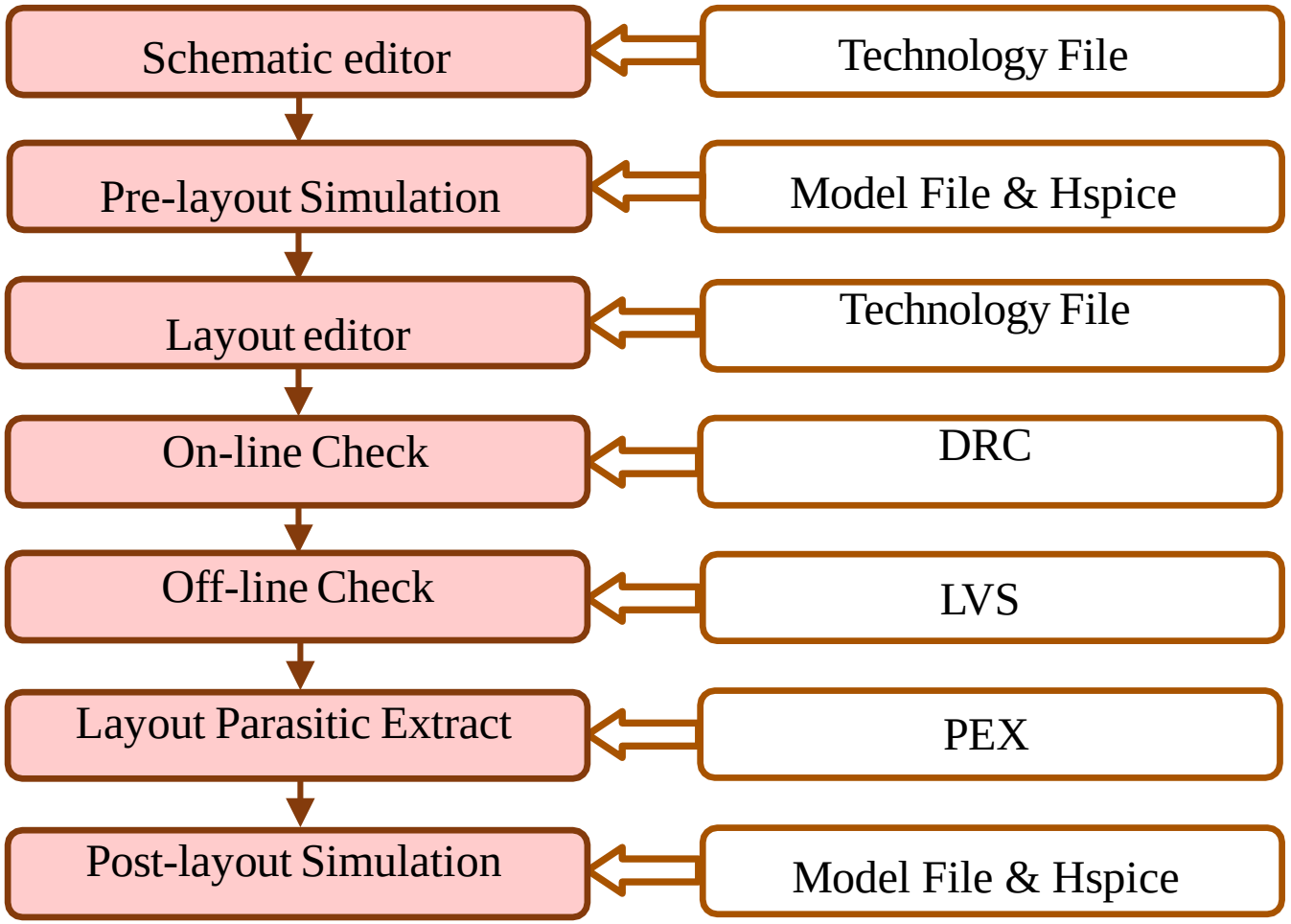
# IC Layout Tools
## Laker & Calibre

**Presenter：許哲維、邱薪育**

# Full-Custom Design Flow



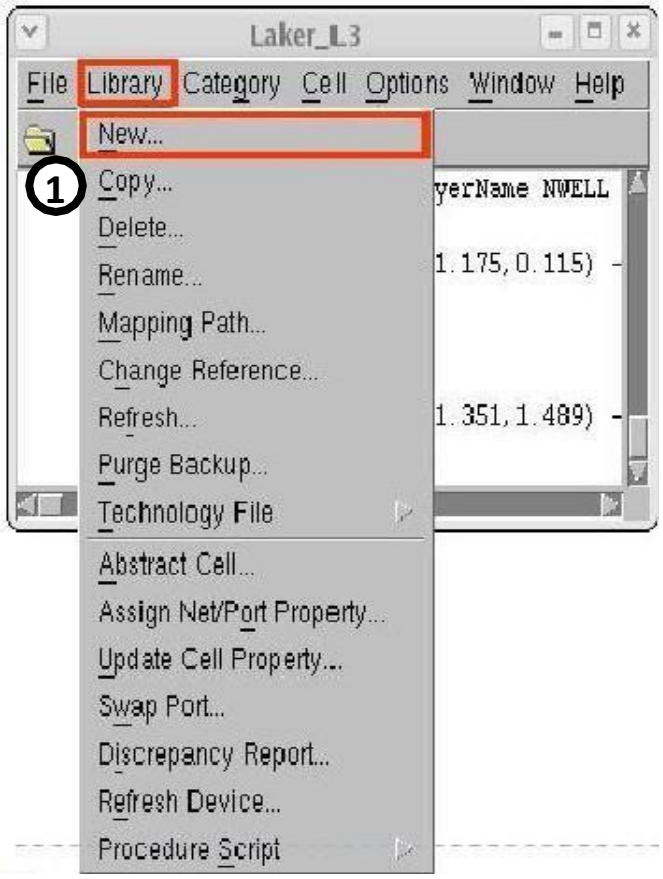
# How to Start Laker?

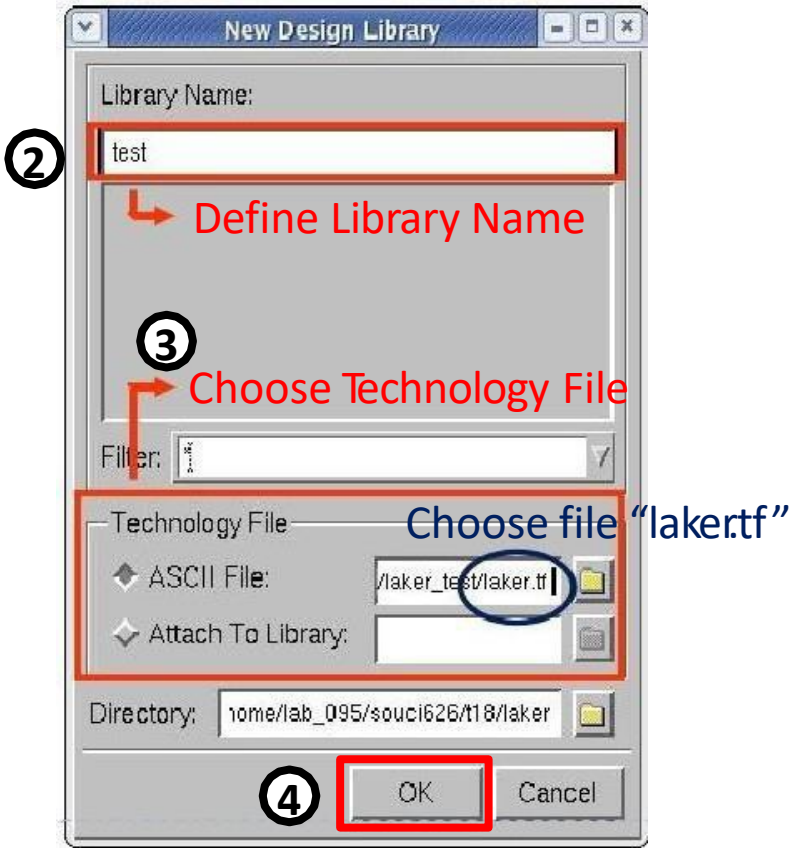
You need these files:

| | |
|---|---|
| laker.tf | Laker technology file |
| rule.drc | **DRC**(*Design Rule Check*) to verify that the layout satisfies design rules. |
| rule.lvs | **LVS** (***Layout Versus Schematic***) to check that circuit in a layout are connected in the same way as in the schematic. |
| rule.rce<br>rule_08KA.rc<br>rule_20KA.rc | **PEX** (***Parasitic Extraction***) to extract the parasitic effects resulted from the interconnection of layout design. |

# Laker – Create New Library

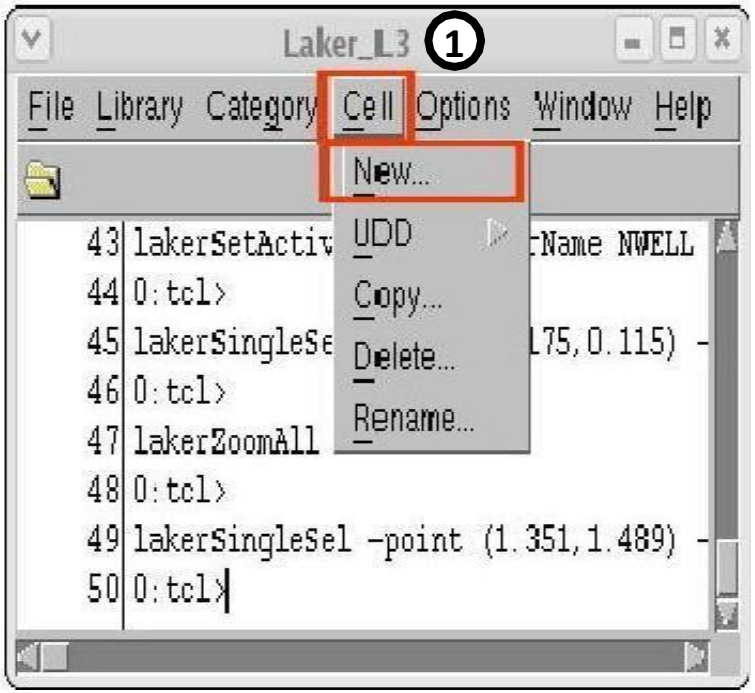
- Terminal enter “laker&”

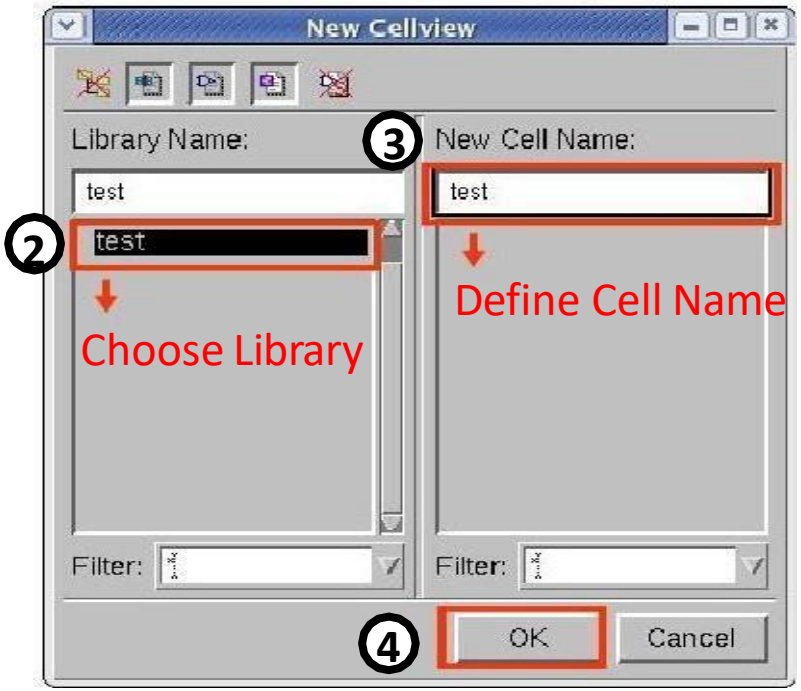


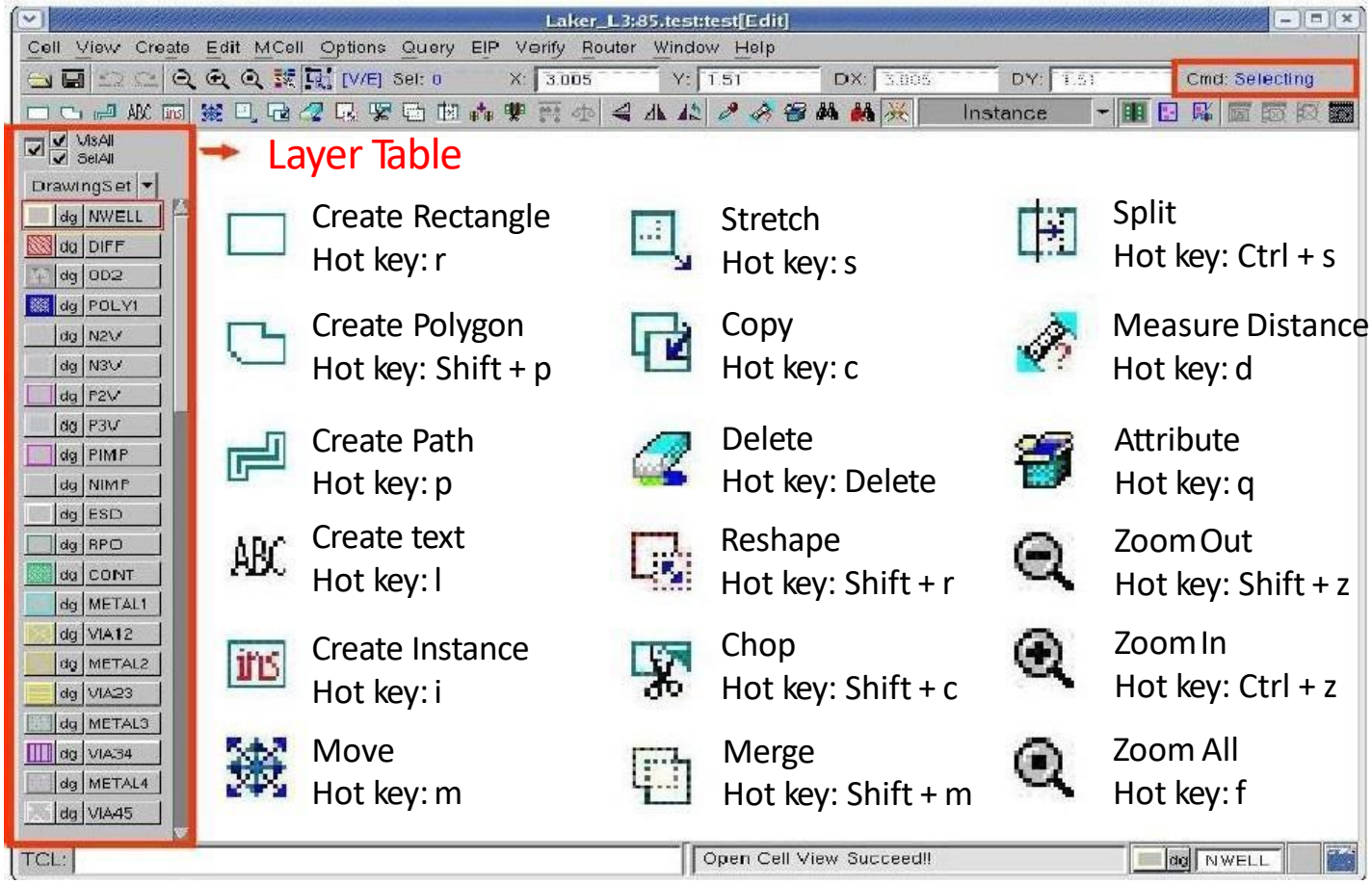

SSCAS

# Laker – Create New Cell



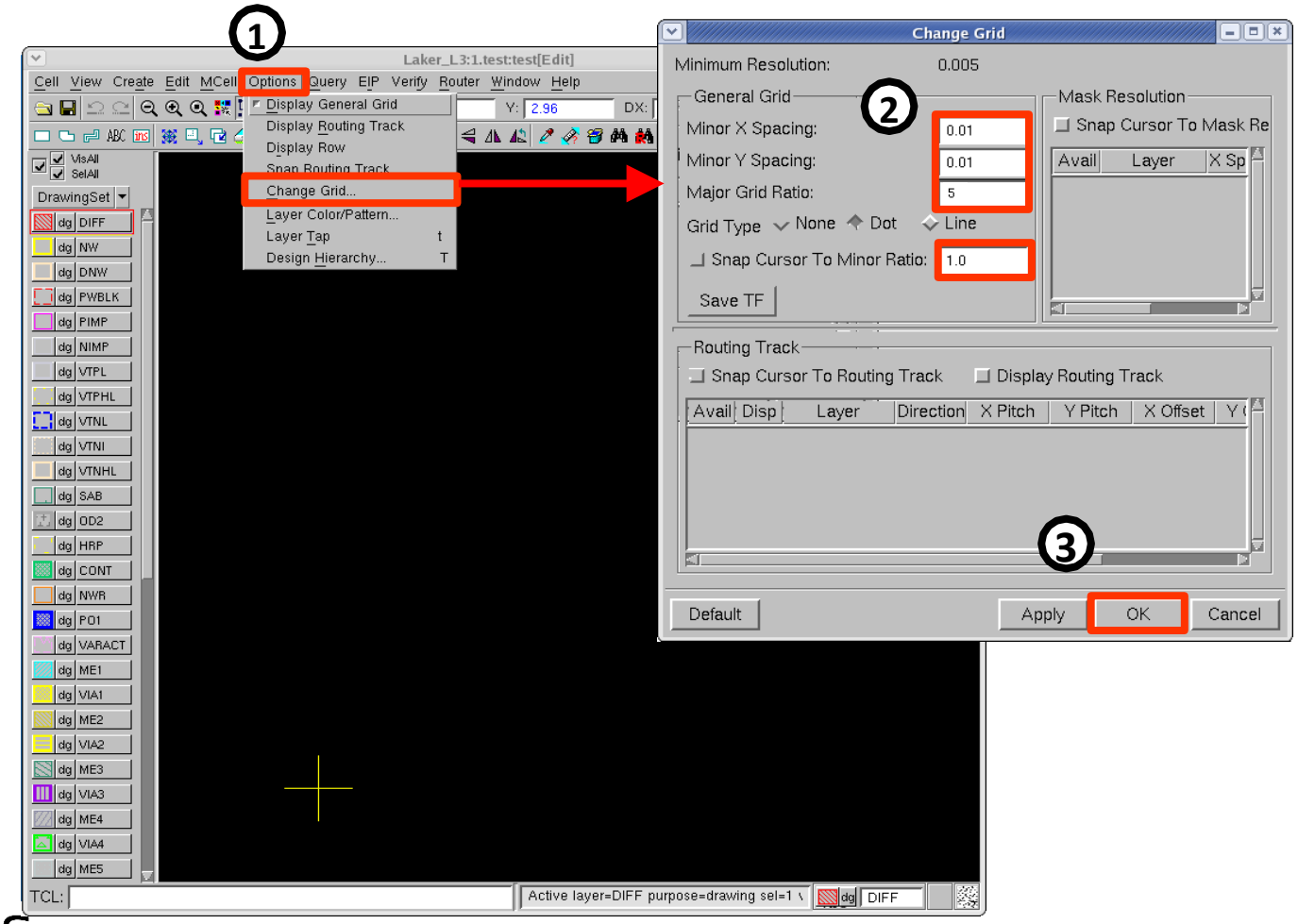
# Laker – Tool Interface



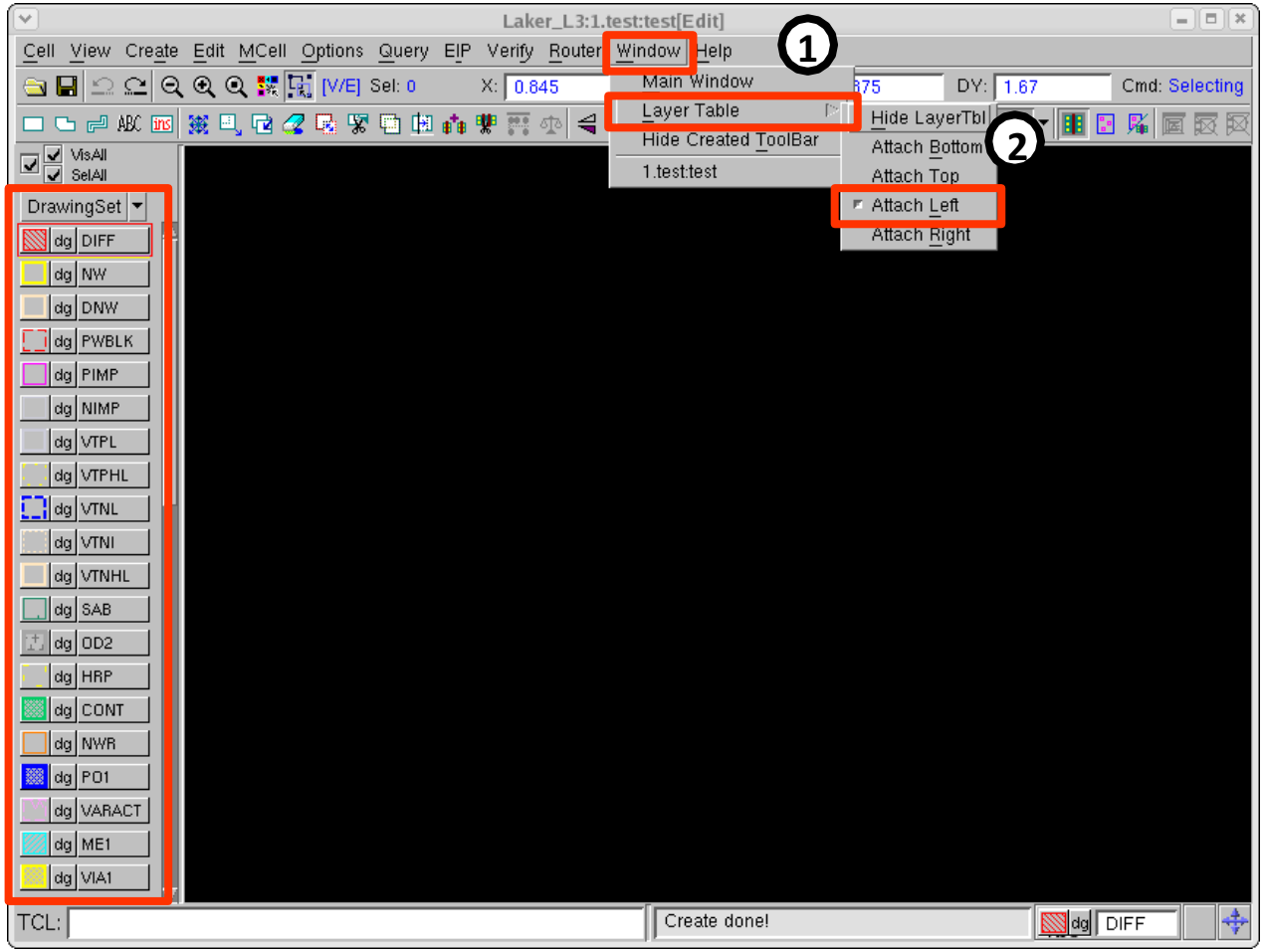
# Laker – Hot Keys

| Hot Key | Function | Hot Key | Function |
|---|---|---|---|
| k | Tag ruler | Ctrl + z | Zoom in |
| Shift + k | Clear ruler | Shift + z | Zoom out |
| r | Create rectangle | Ctrl + a | Select all objects |
| d | Measure distance | Shift + r | Reshape selected object(s) |
| q | Show object attribute | F8 | Clear Highlight |
| s | Stretch selected object(s) | i | Create Instance |
| c | Copy selected object(s) | u | Undo last action |
| m | Move selected object(s) | Shift + u | Redo last action |
| delete | Delete selected object(s) | | |
| a | Align selected objects(s) | | |
| f | Zoom all | | |

# Laker – Basic Setting : Change Grid



# Laker – Basic Setting : Layer Table

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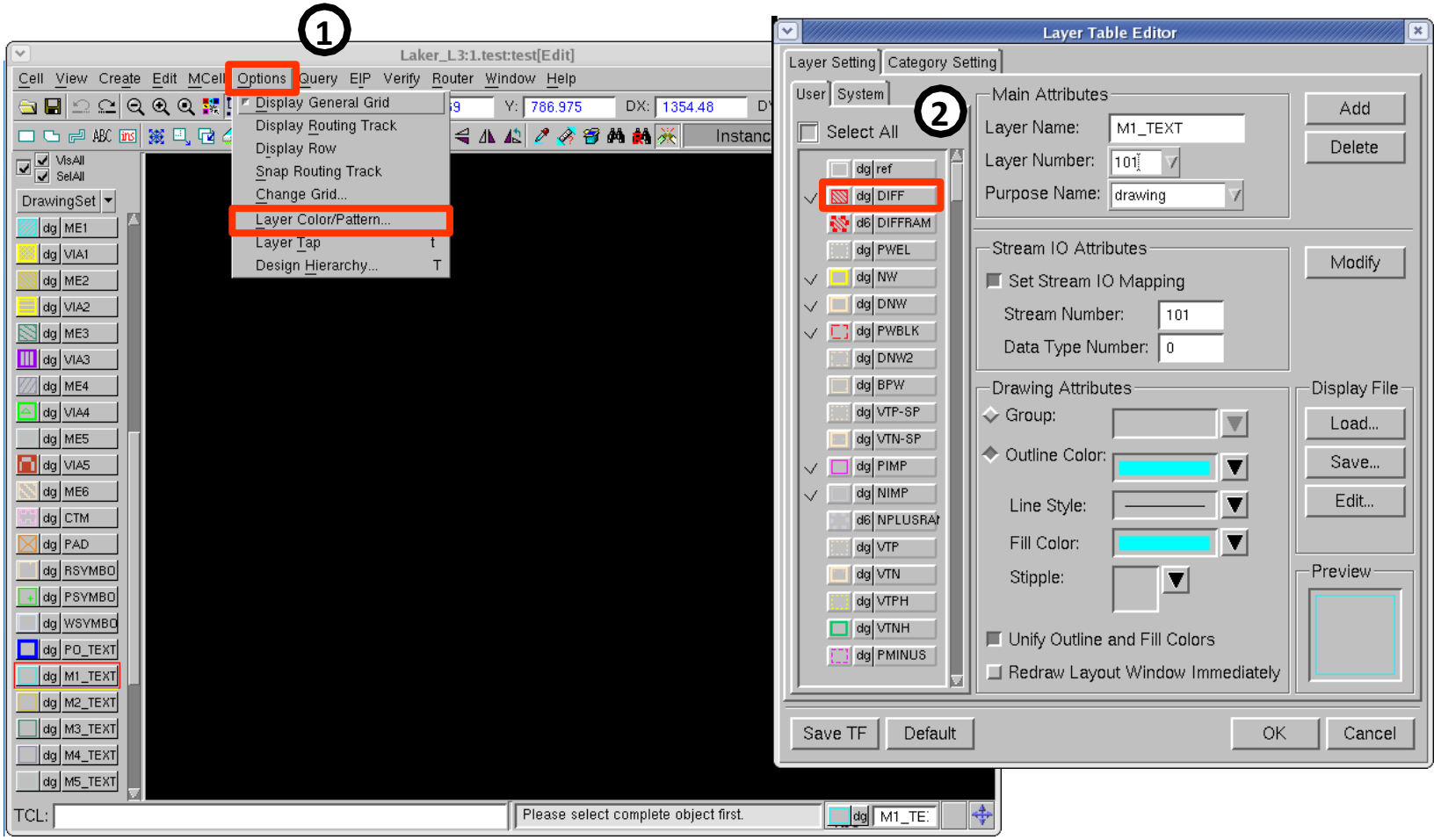
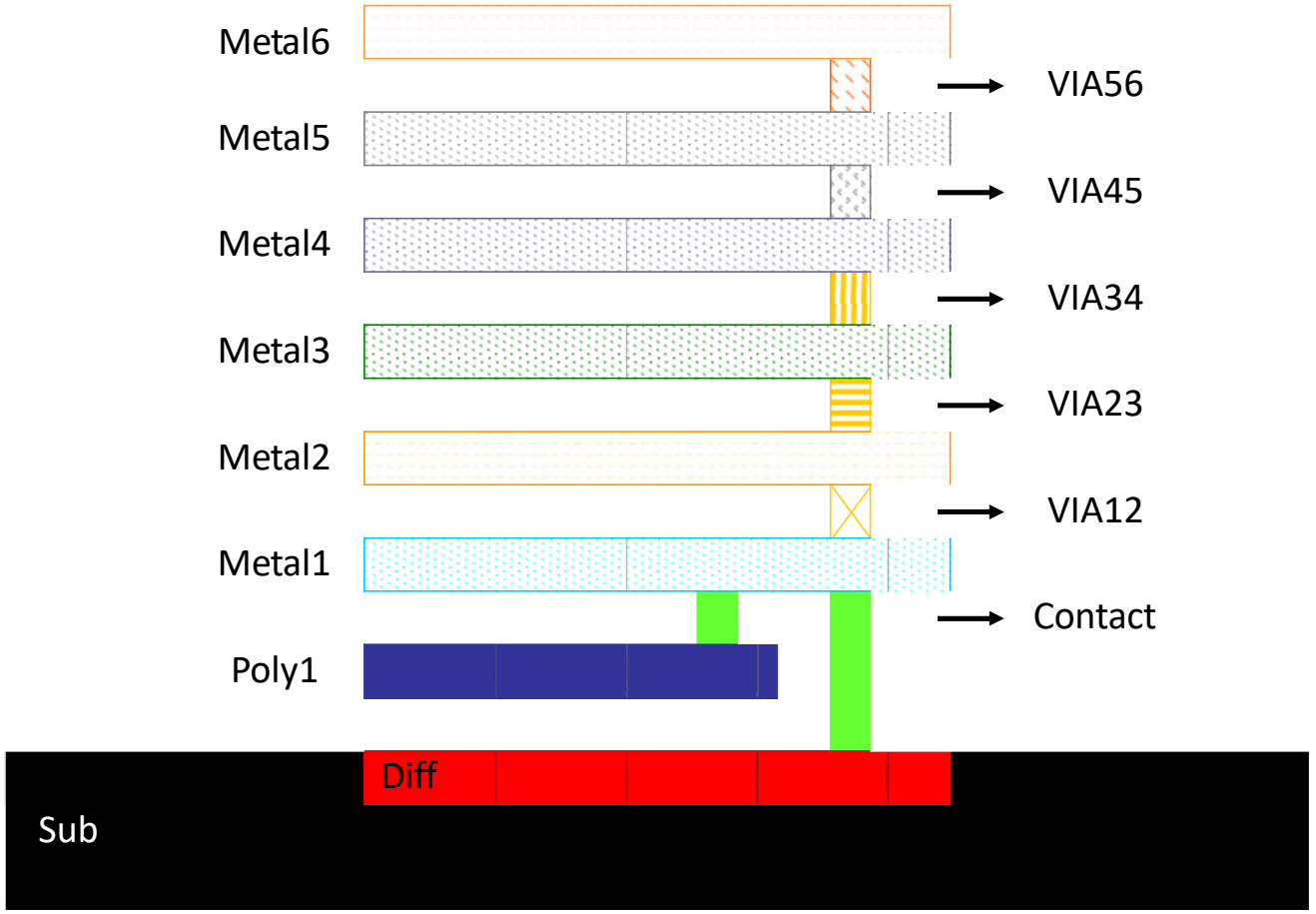
# Laker – Basic Setting : Layer Table Editor

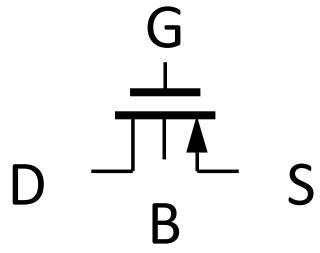


# Laker – Layer Level

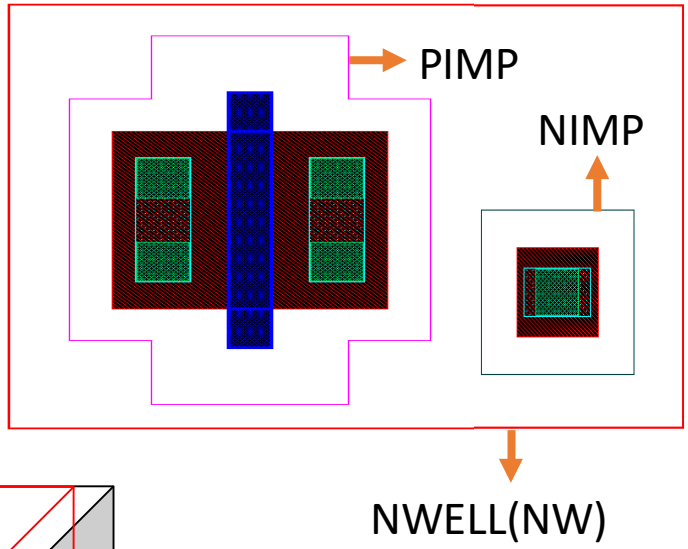


# Laker – Example : PMOS

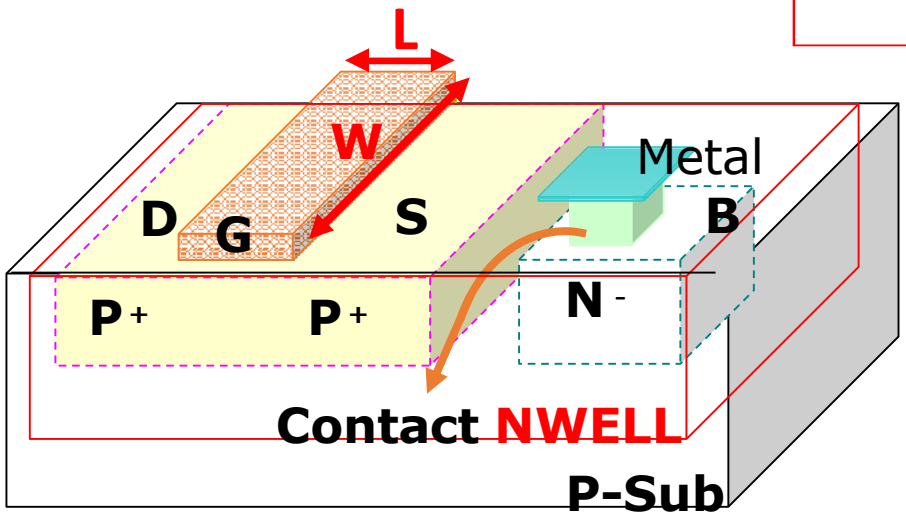
## Symbol




## Layout View




## Process Section

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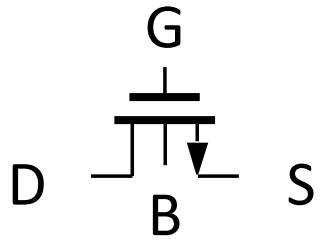
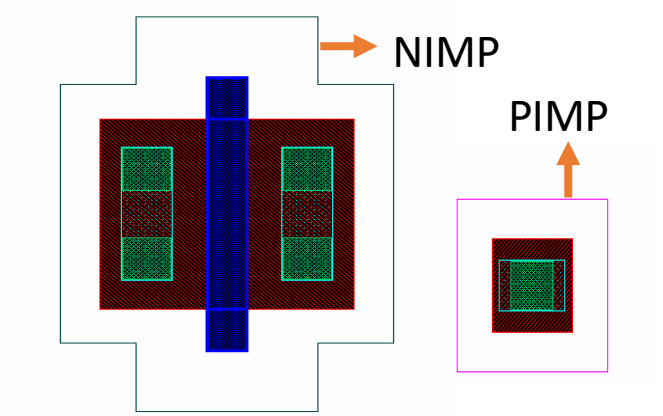
# Laker – Example : NMOS

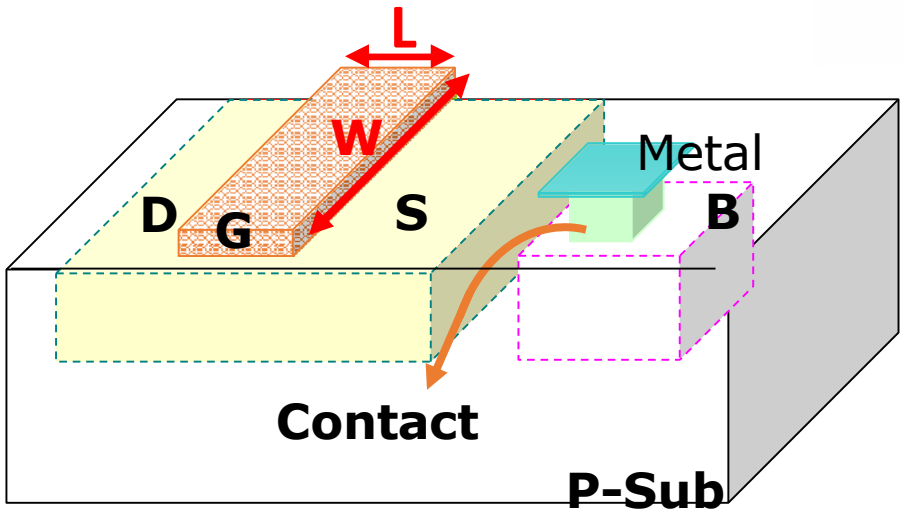
## Symbol




## Layout View




## Process Section

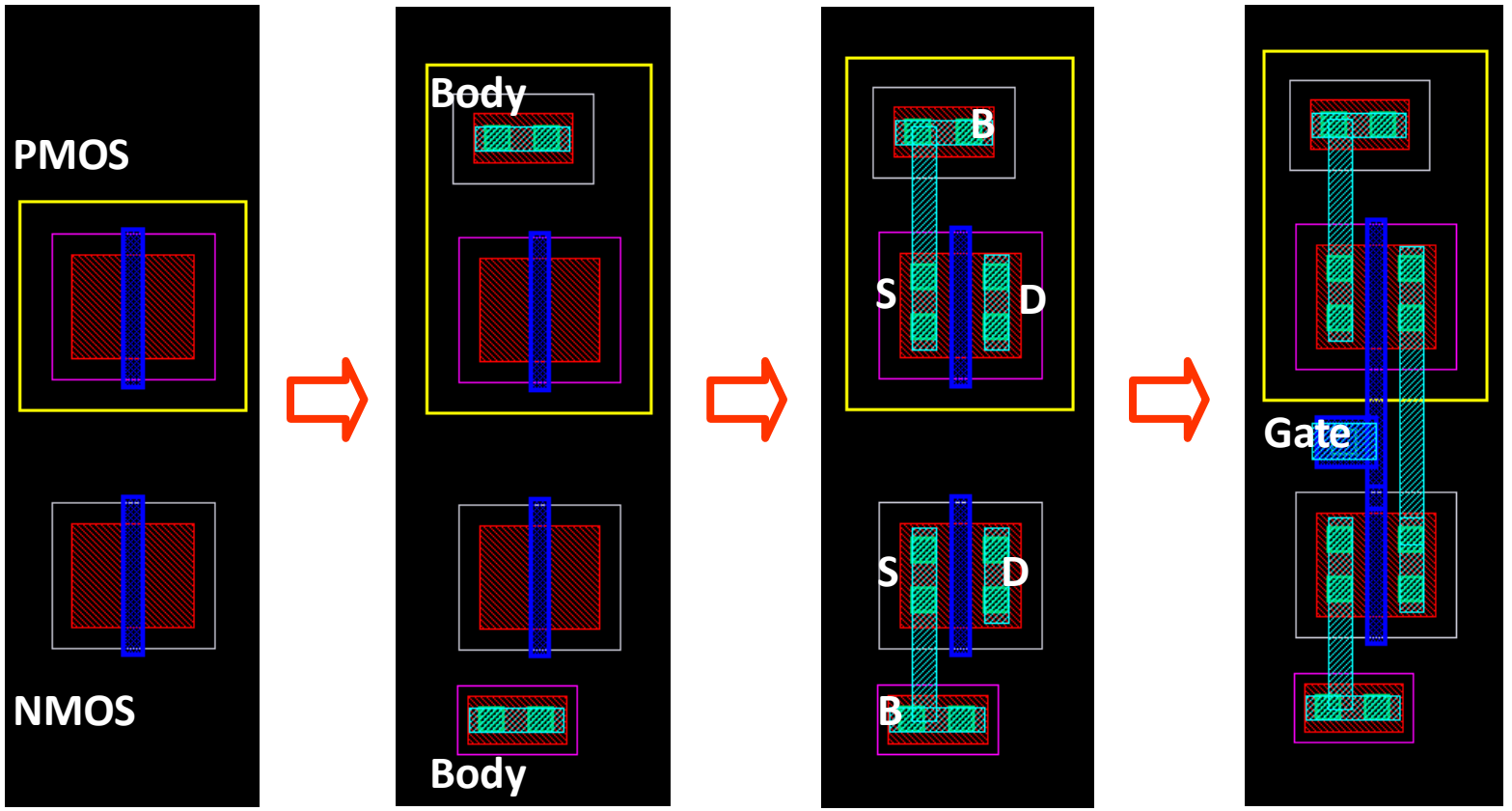


# Laker – Example : Inverter

| Term | Explanation |
|---|---|
| W | Width |
| L | Length |
| DIFF | Diffusion (Drain/Source) |
| PO1 | Poly silicon (Gate) |
| PIMP | P implantation |
| NIMP | N implantation |
| NW | N WELL |

$$\left(\frac{W}{L}\right)_P = \left(\frac{1um}{0.18um}\right), \left(\frac{W}{L}\right)_N = \left(\frac{0.5um}{0.18um}\right)$$

# Laker – Example : Inverter




Create a PMOS & an NMOS

Add Body

Use Metal1 and Contacts to connect source and body

Connect Gate and Drain

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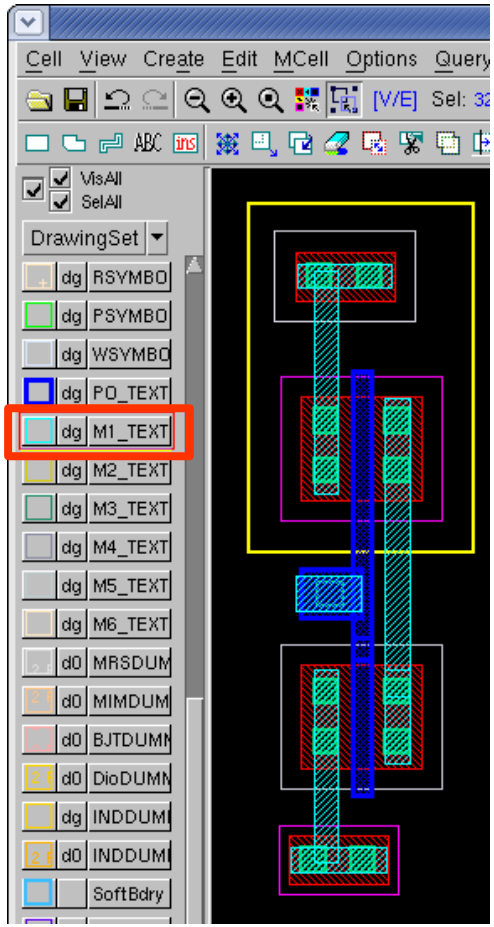
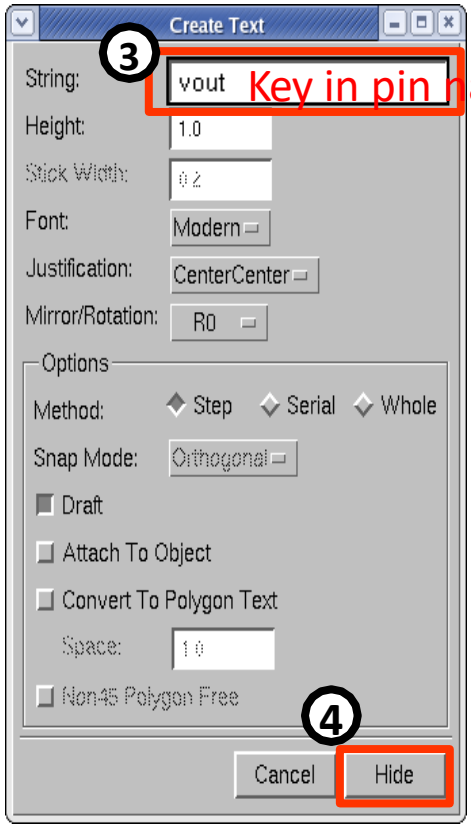
# Laker – Example : Add Pin Name



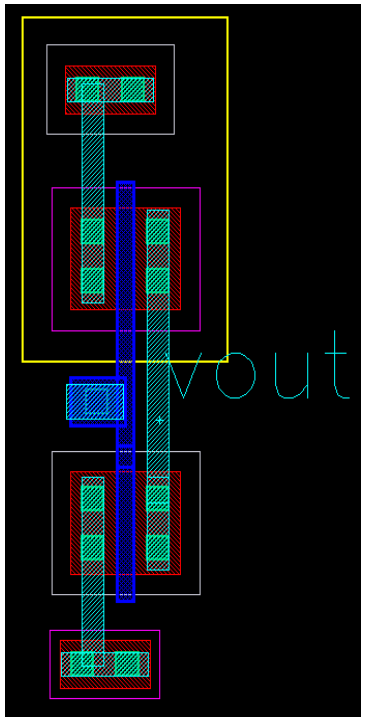

① M1_TEXT

② ABC Create text
Hot key: ℓ




③ Key in pin name

④ Hide

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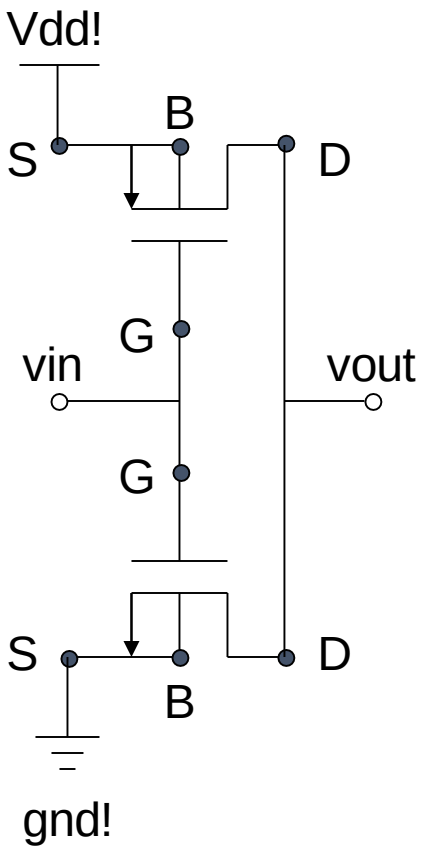
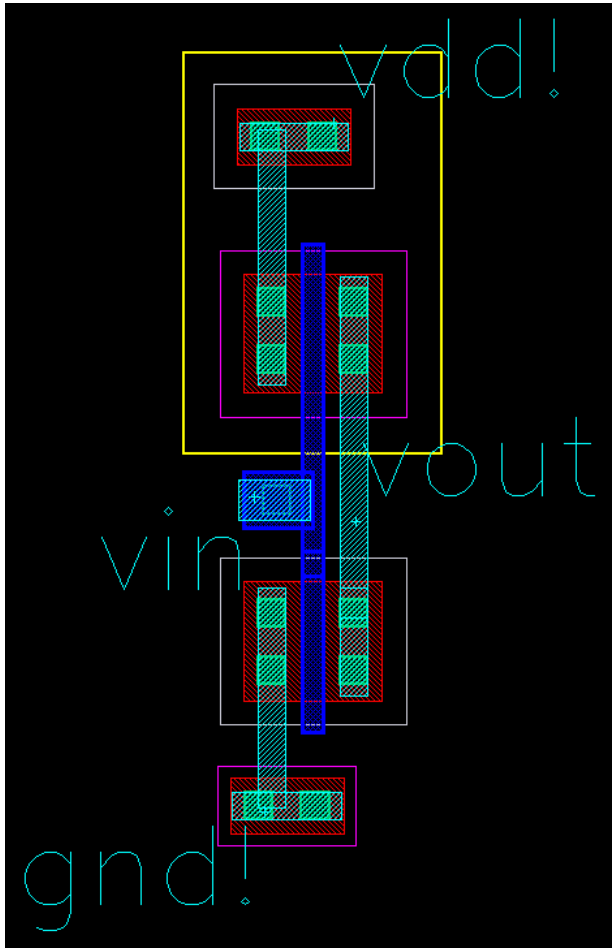
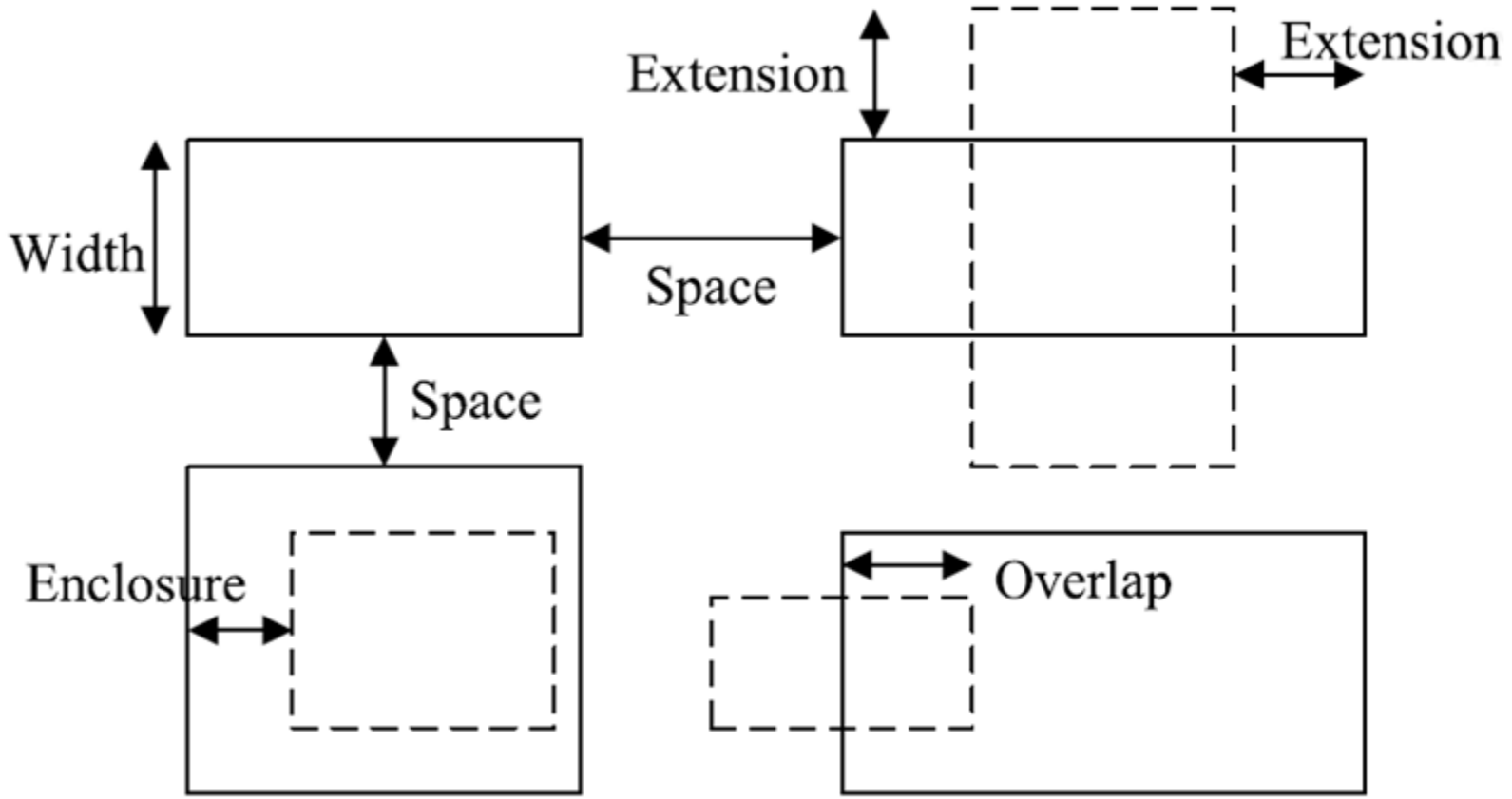
# Laker – Example : Inverter




SSCAS

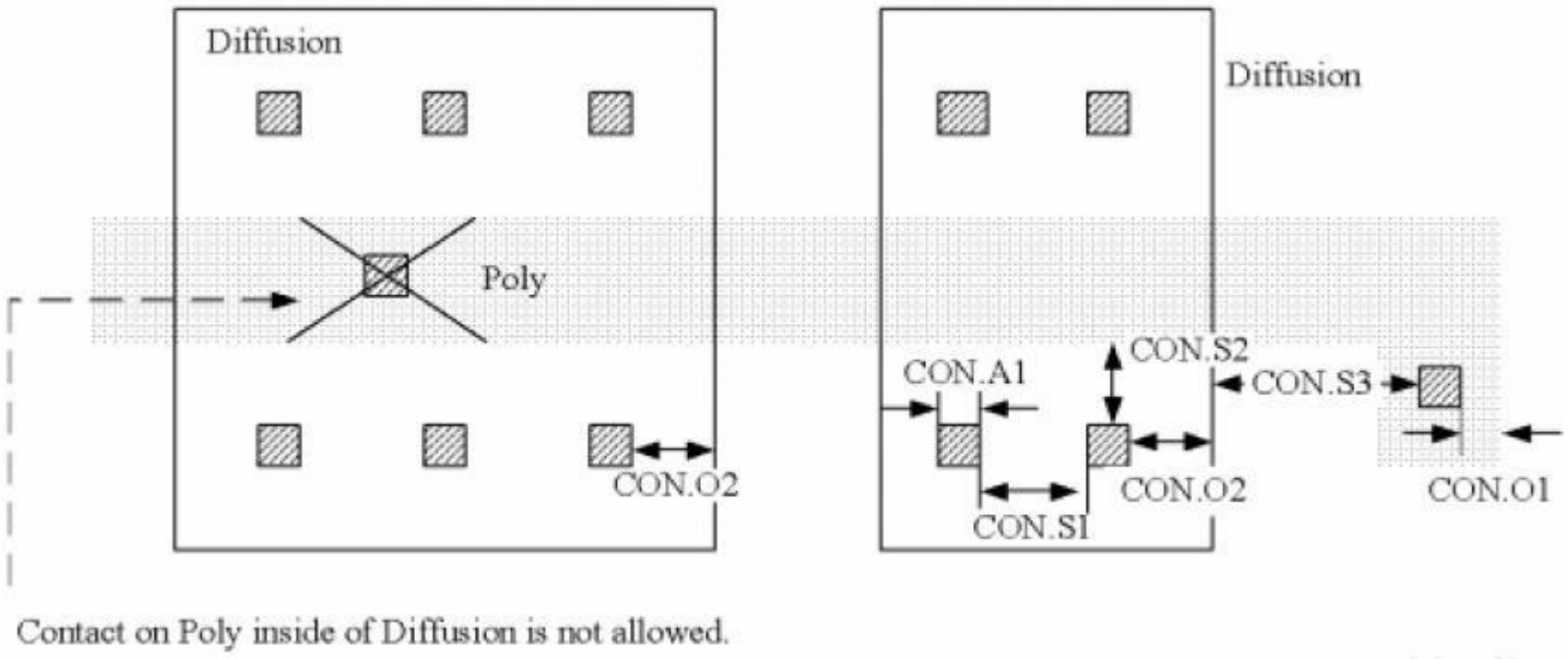
# Design Rule (1/4)



# Design Rule (2/4)

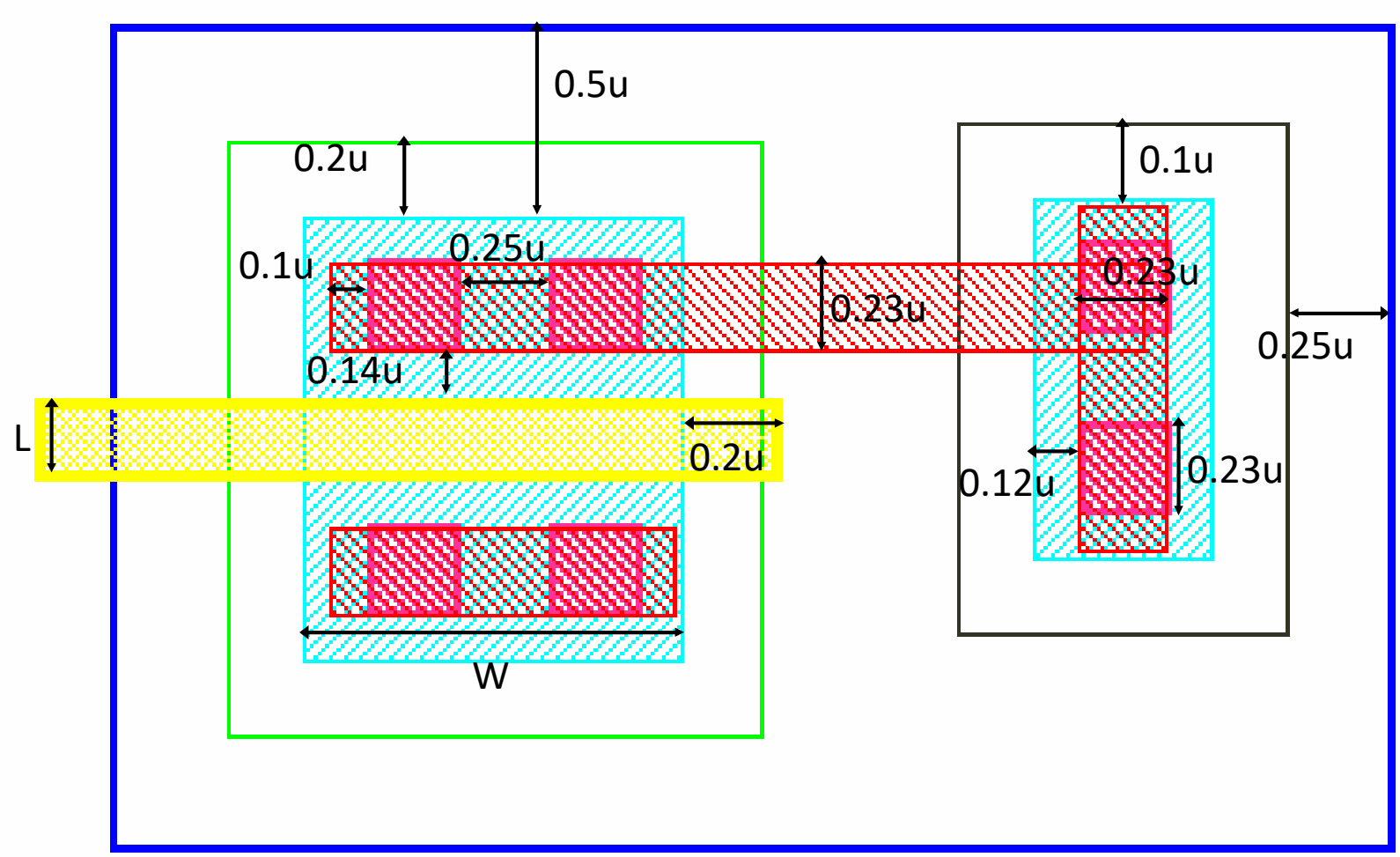
| | | (unit : um) |
|---|---|---|
| CONT.A1 | Maximum and Minimum Contact size | 0.23 *0.23um$^2$ |
| CONT.S1 | Minimum Contact to Contact spacing | 0.25 |
| CONT.S2.18 | Minimum Diffusion Contact to Poly spacing (1.8V device) | 0.14 |
| CONT.S2.33 | Minimum Diffusion Contact to Poly spacing (3.3V device) | 0.28 |
| CONT.S3 | Minimum Poly Contact to Diffusion edge spacing | 0.18 |
| CONT.O1 | Minimum Poly overlap Contact | 0.12 |

# Design Rule (3/4)



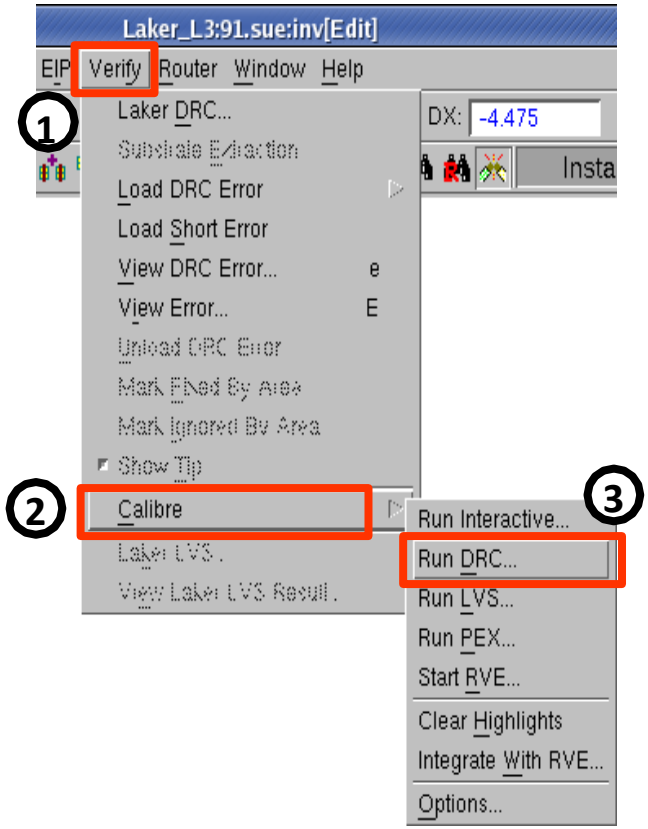

Contact on Poly inside of Diffusion is not allowed.

# Design Rule (4/4): PMOS & NWELL

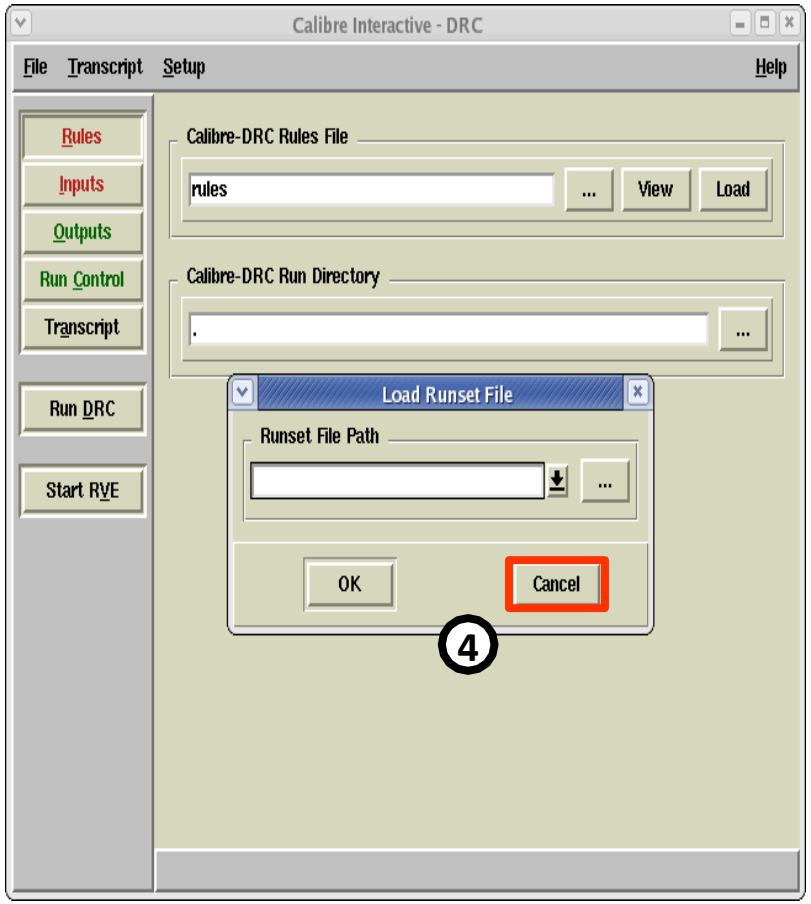


# DRC Check – Open DRC

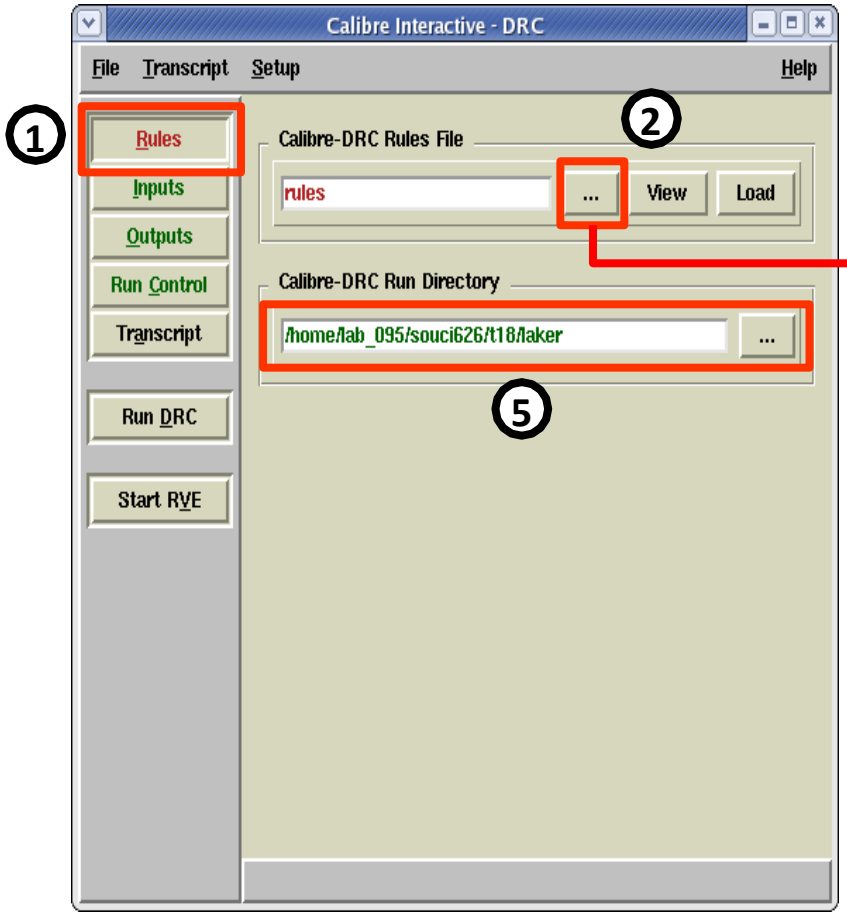
- Check layout layer rule



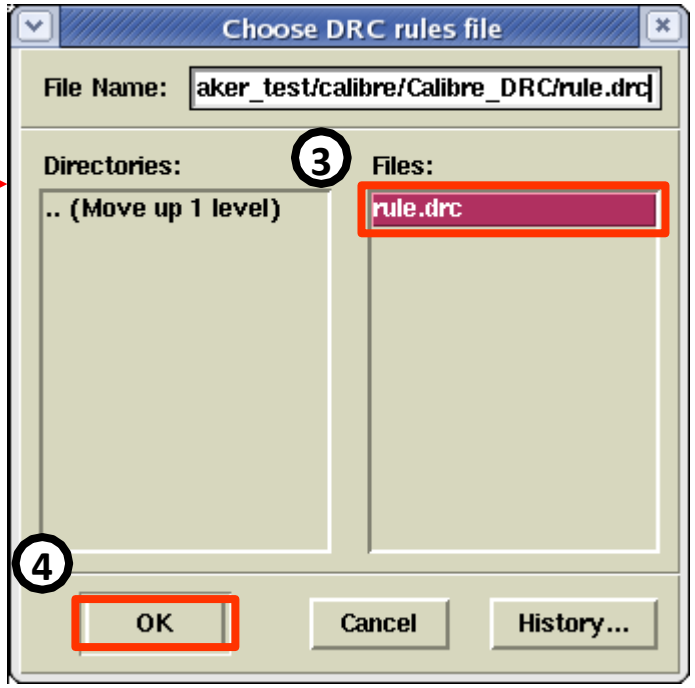


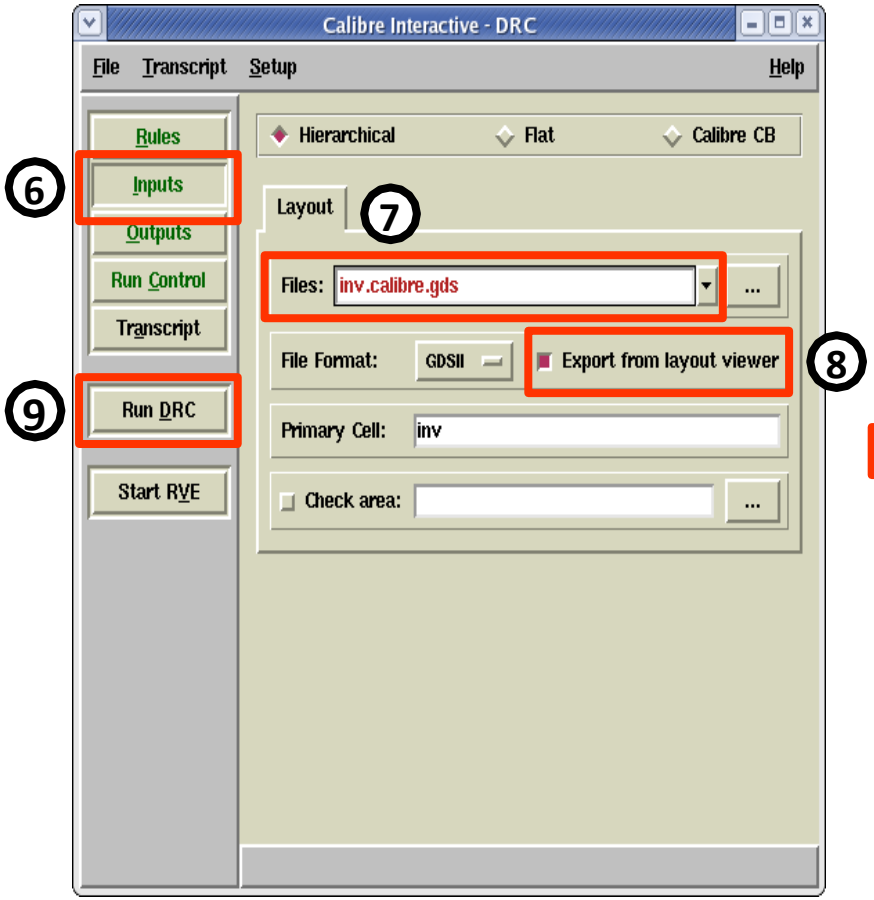
# DRC Check – Define DRC Rule

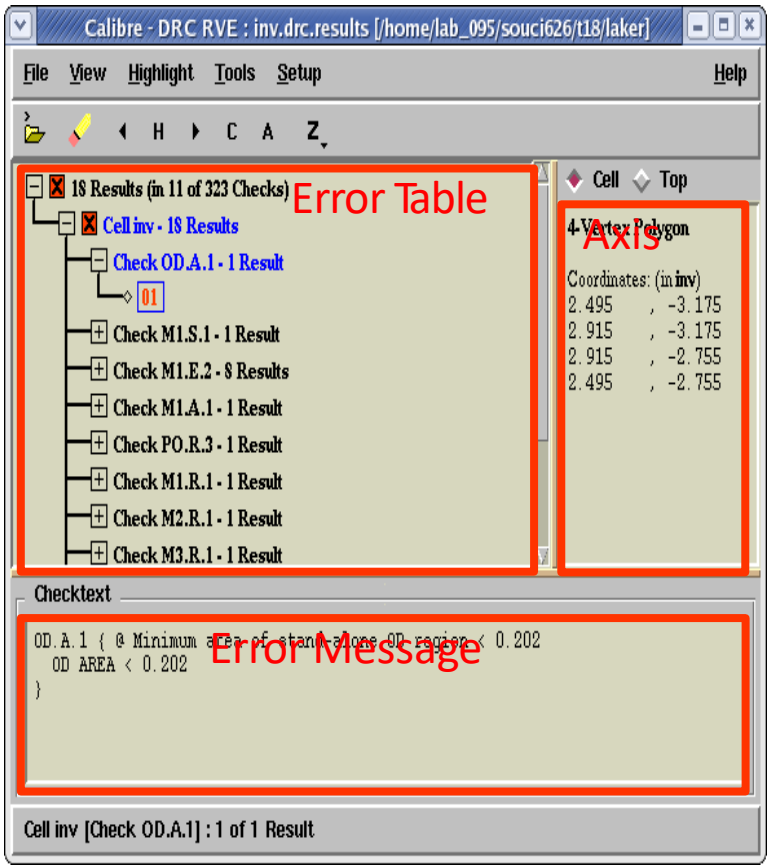



Choose DRC Rule



# DRC Check – Define DRC Rule

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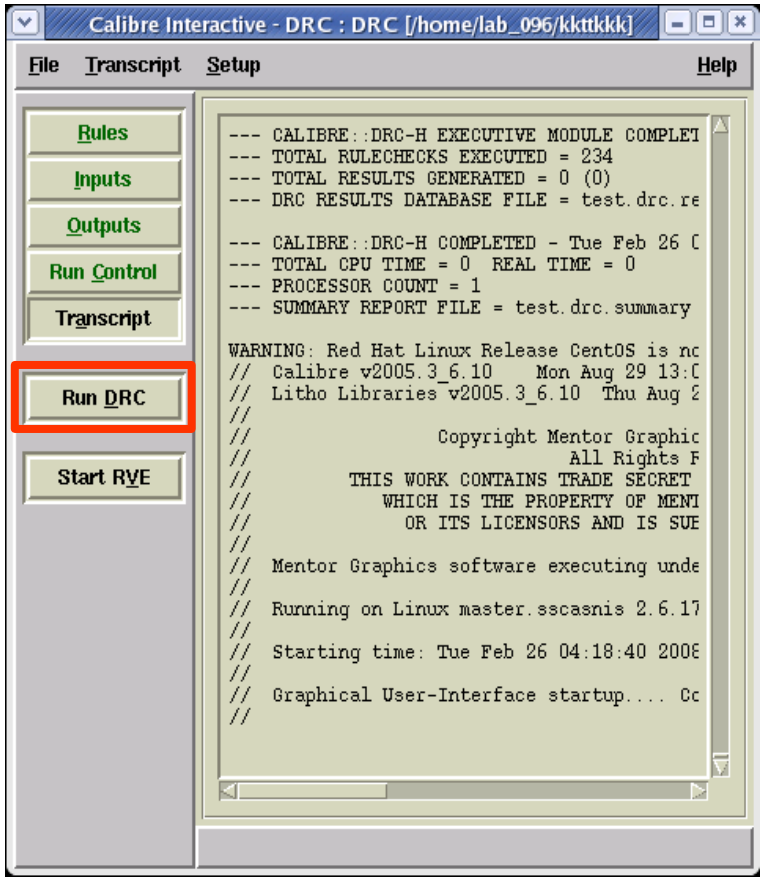
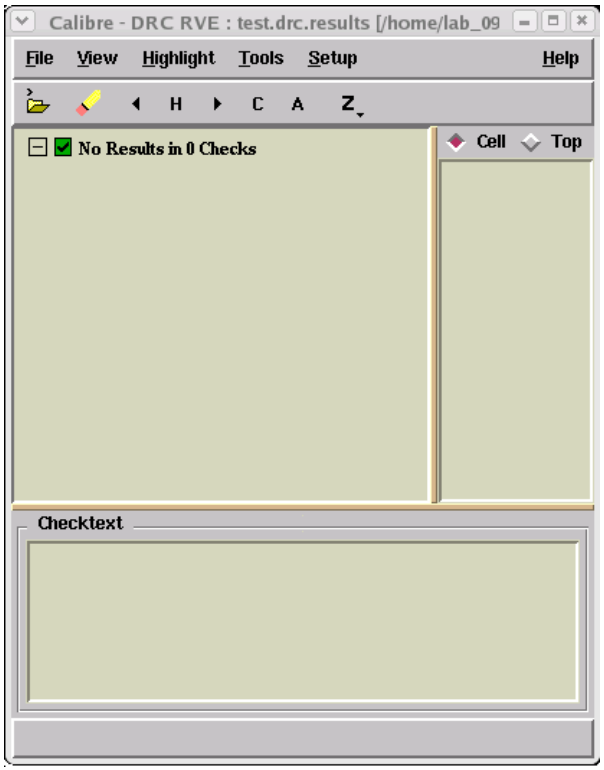
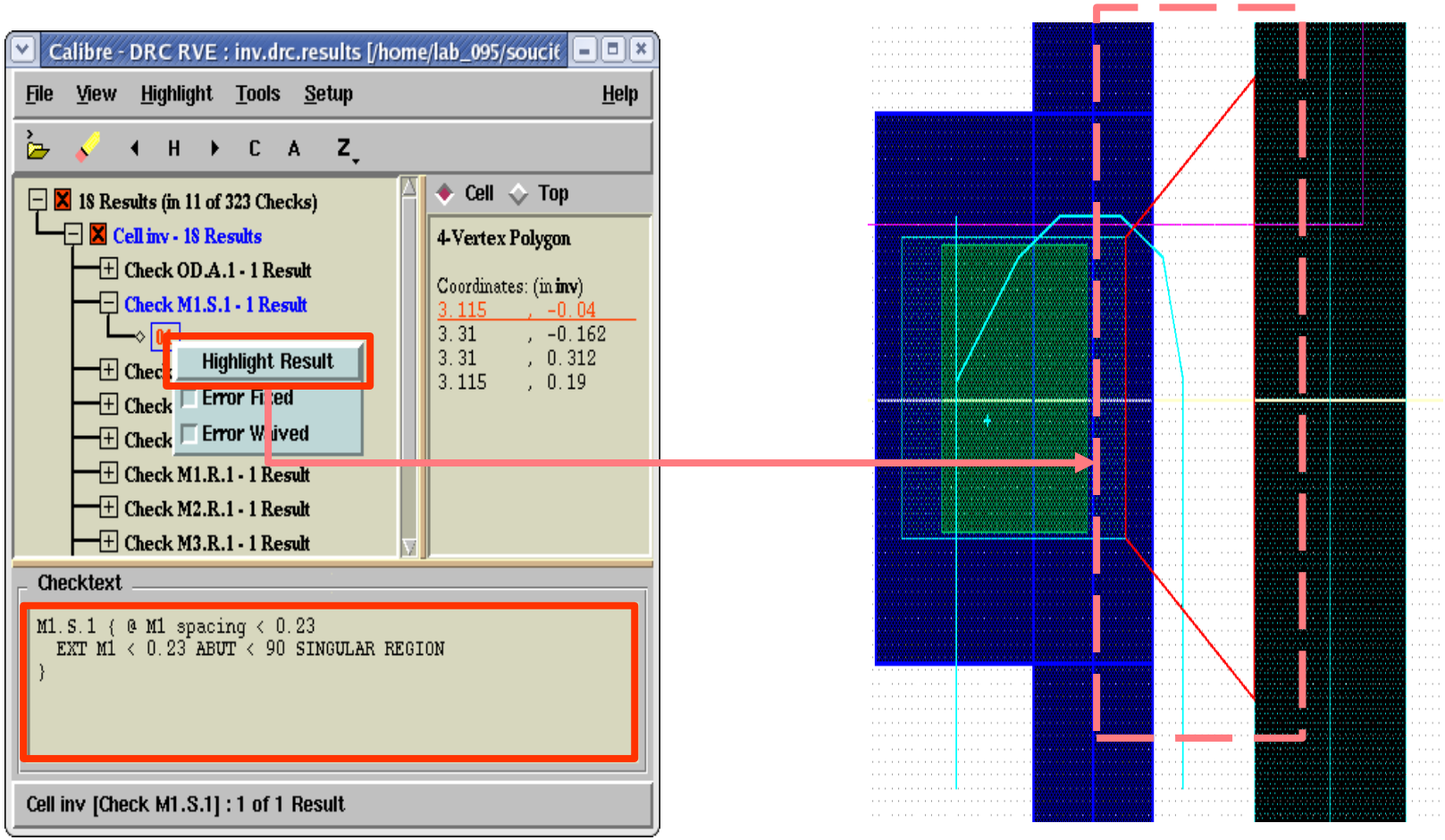
# DRC Check – No Error



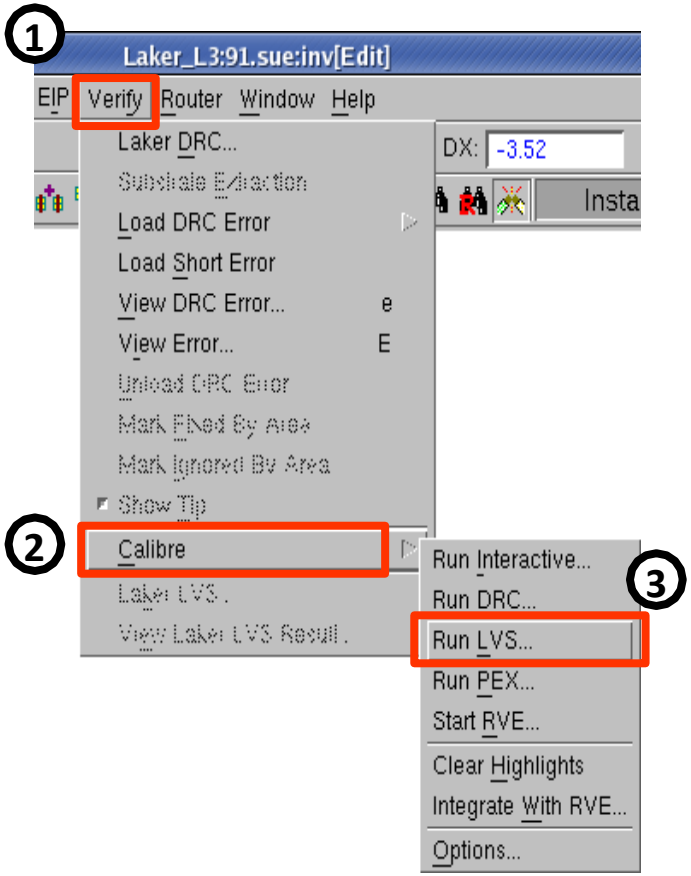

SSCAS

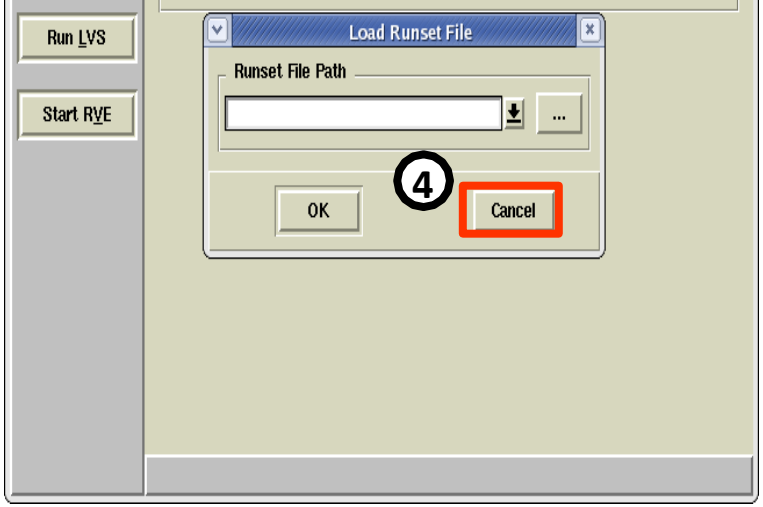
# DRC Check – Highlight Error



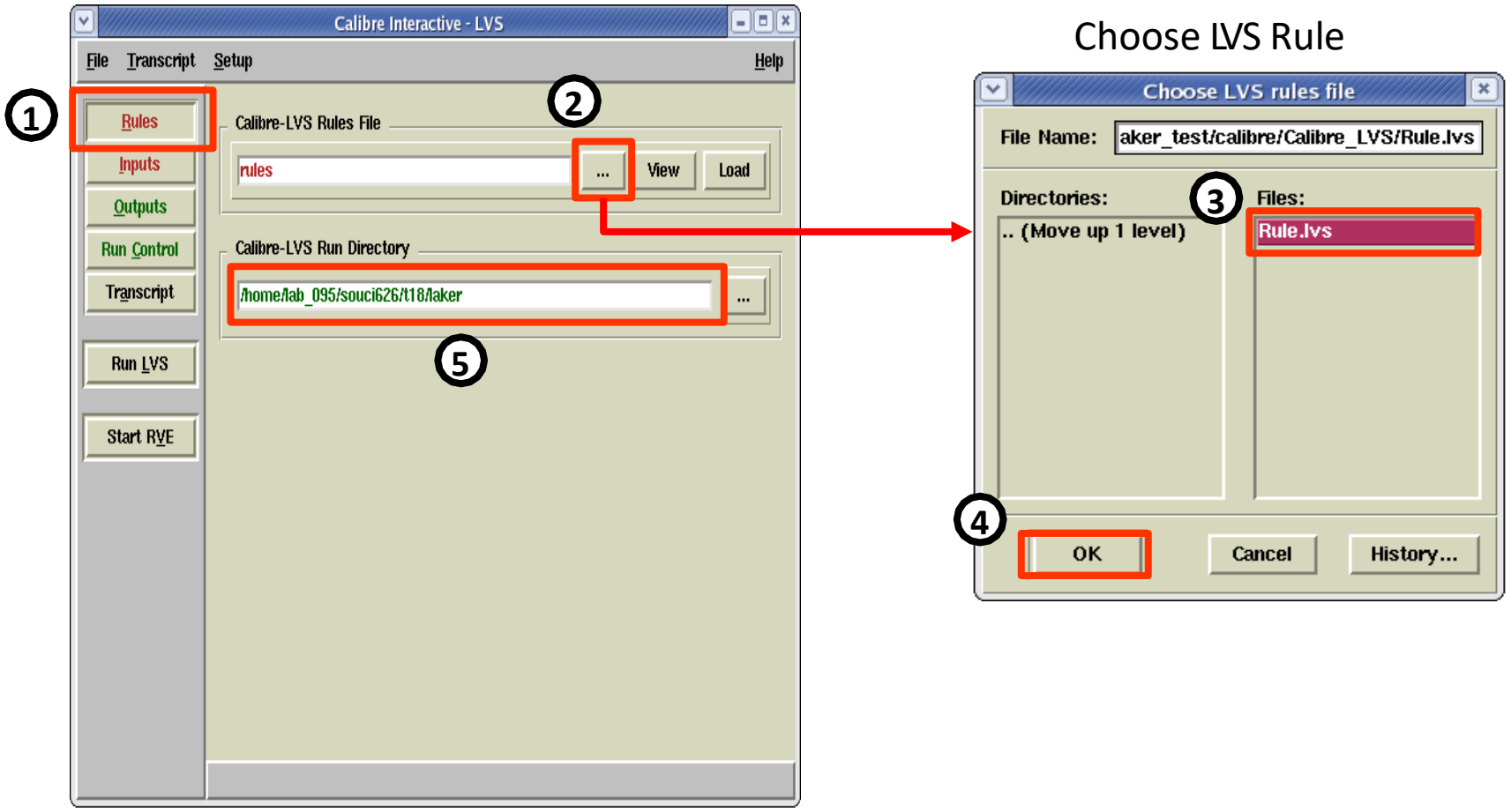

SSCAS

# LVS Check – Open LVS

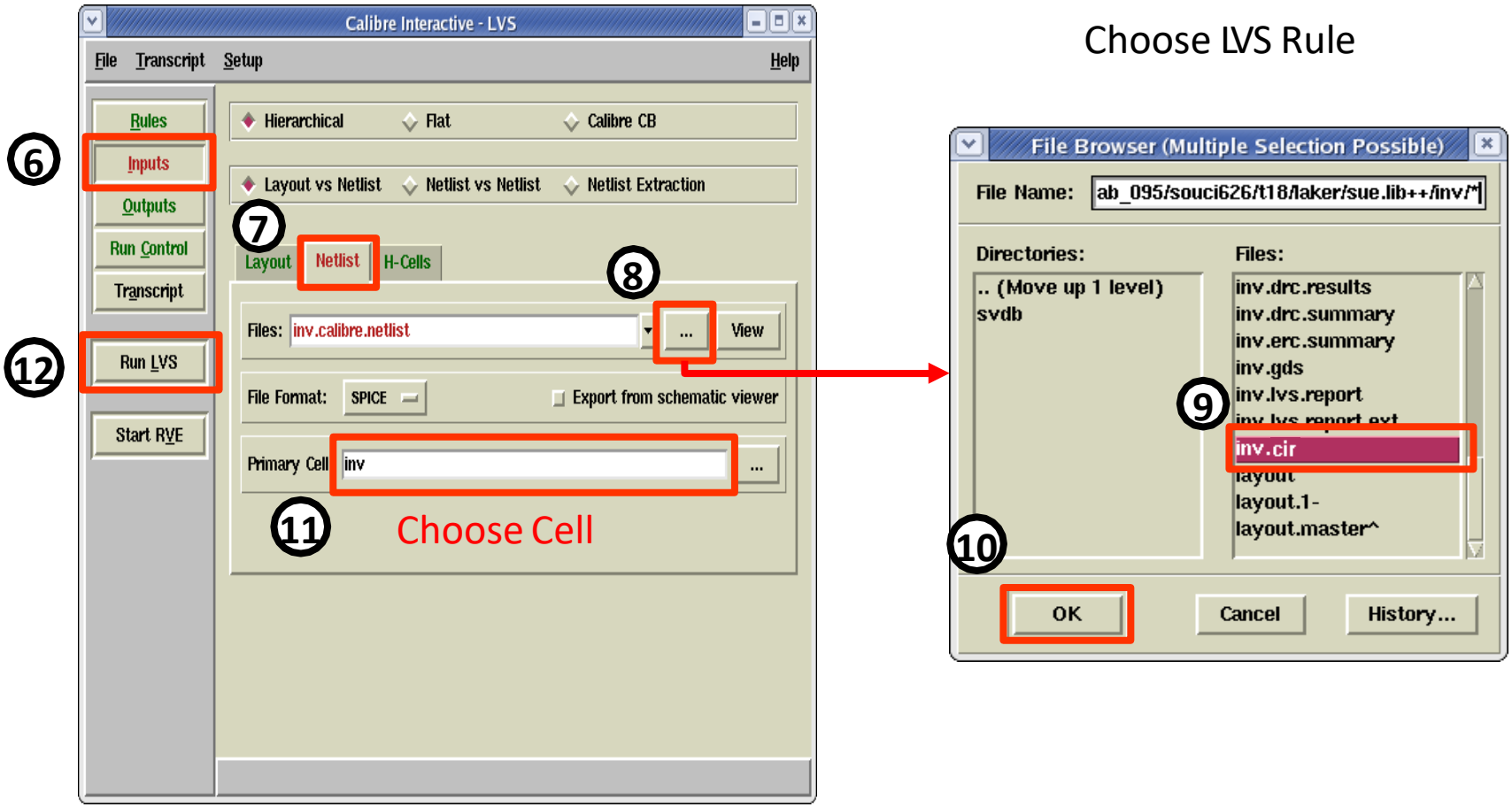


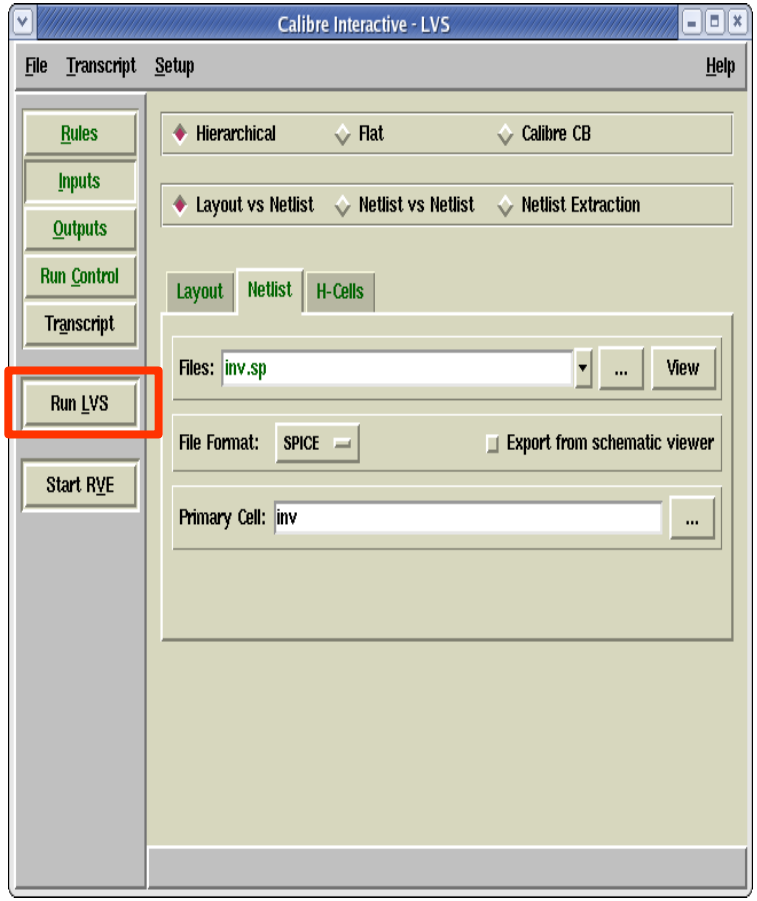
# LVS Check – Define LVS Rule

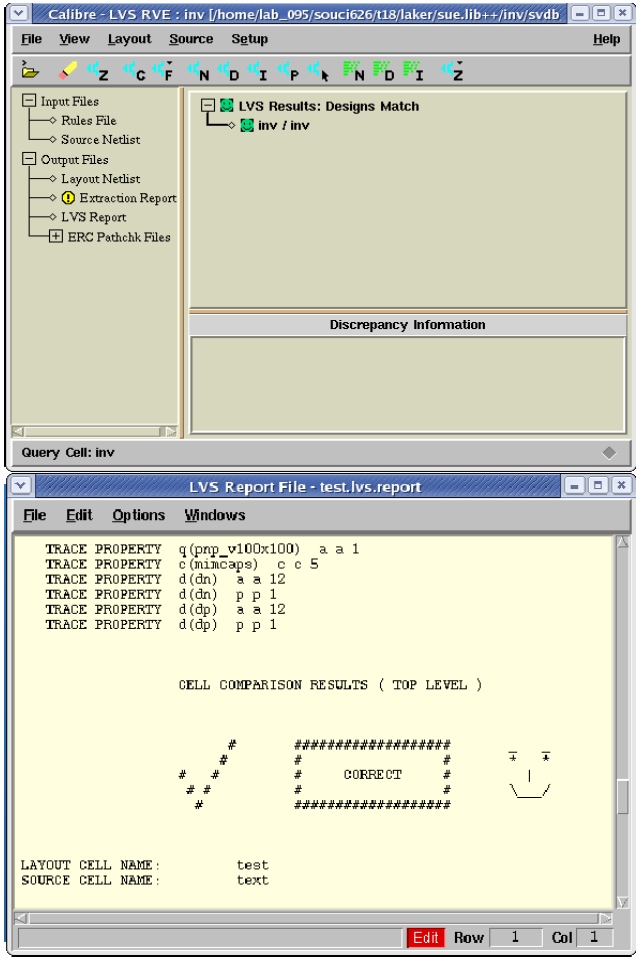


# LVS Check – Define LVS Rule

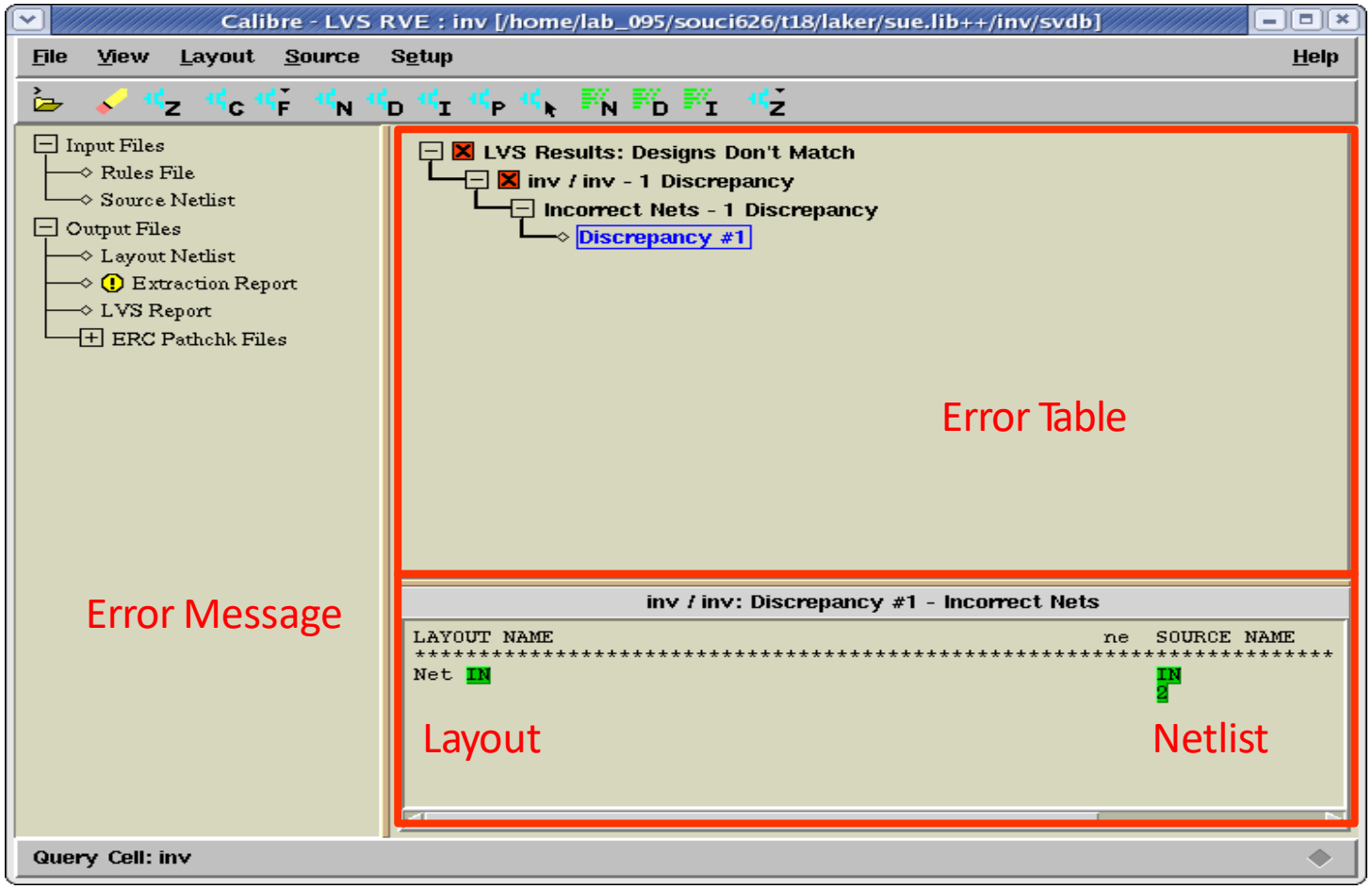


# LVS Check – No Error



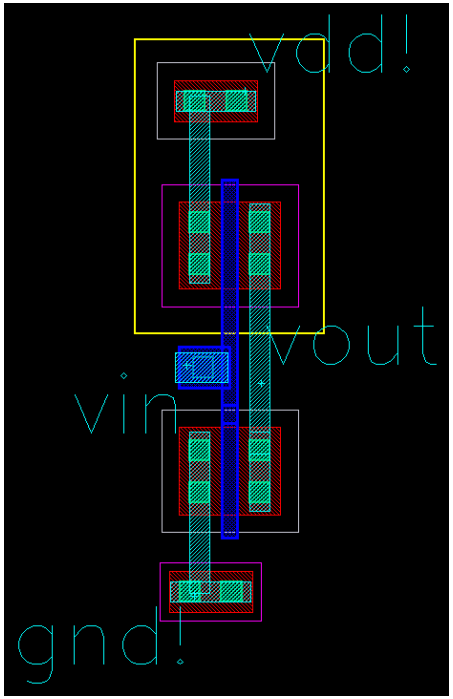



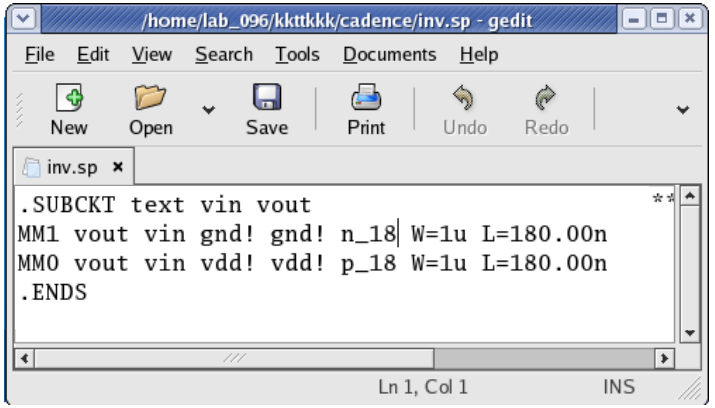
# LVS Check – Error



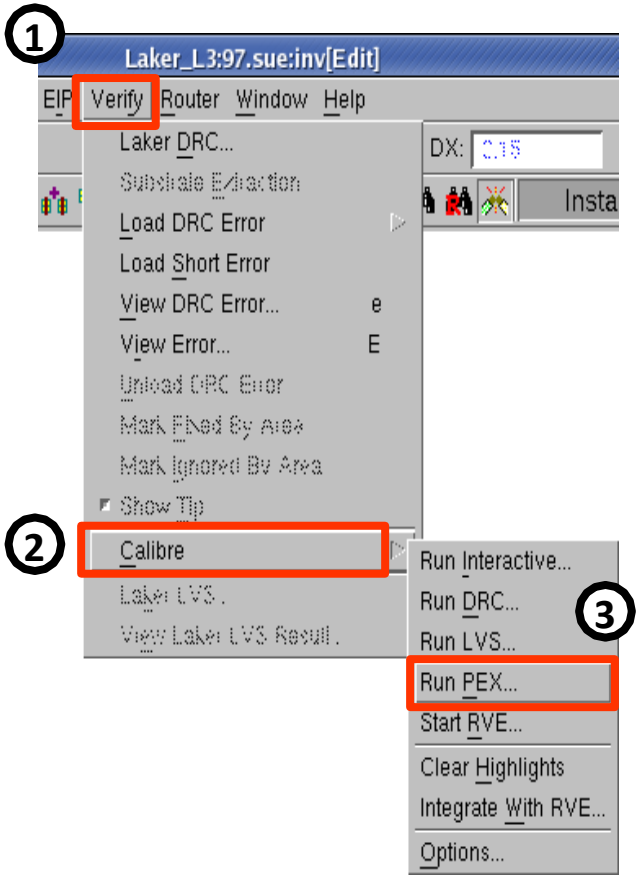
# LVS Check – Be Careful !!

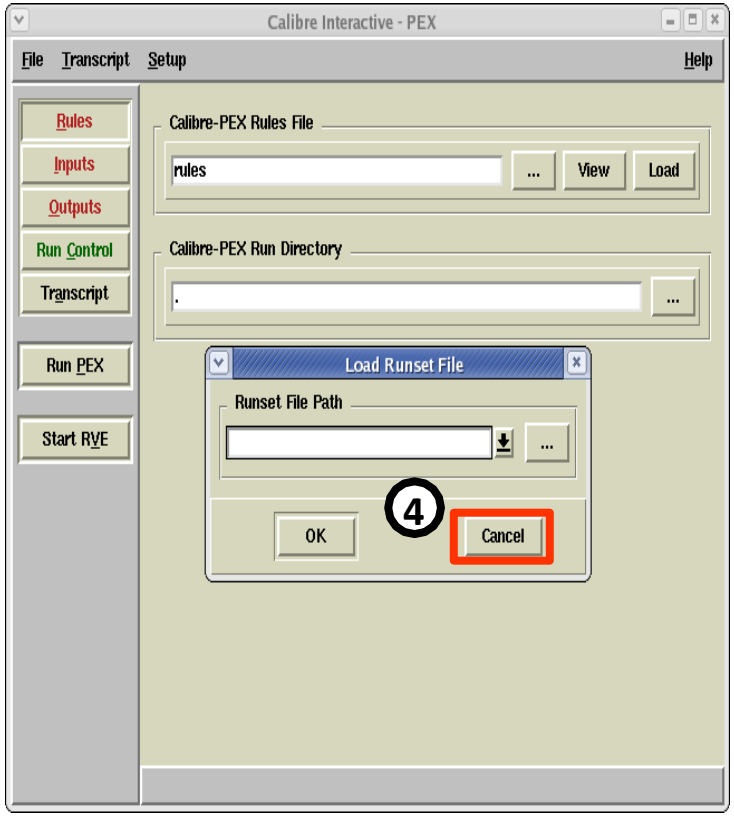
- Layout 中的pin name要和sub-circuit中的pin name相同 (ex: vin, vout, vdd!, gnd!)
- Layout中一定要記得打上 “vdd!”和 “gnd!”



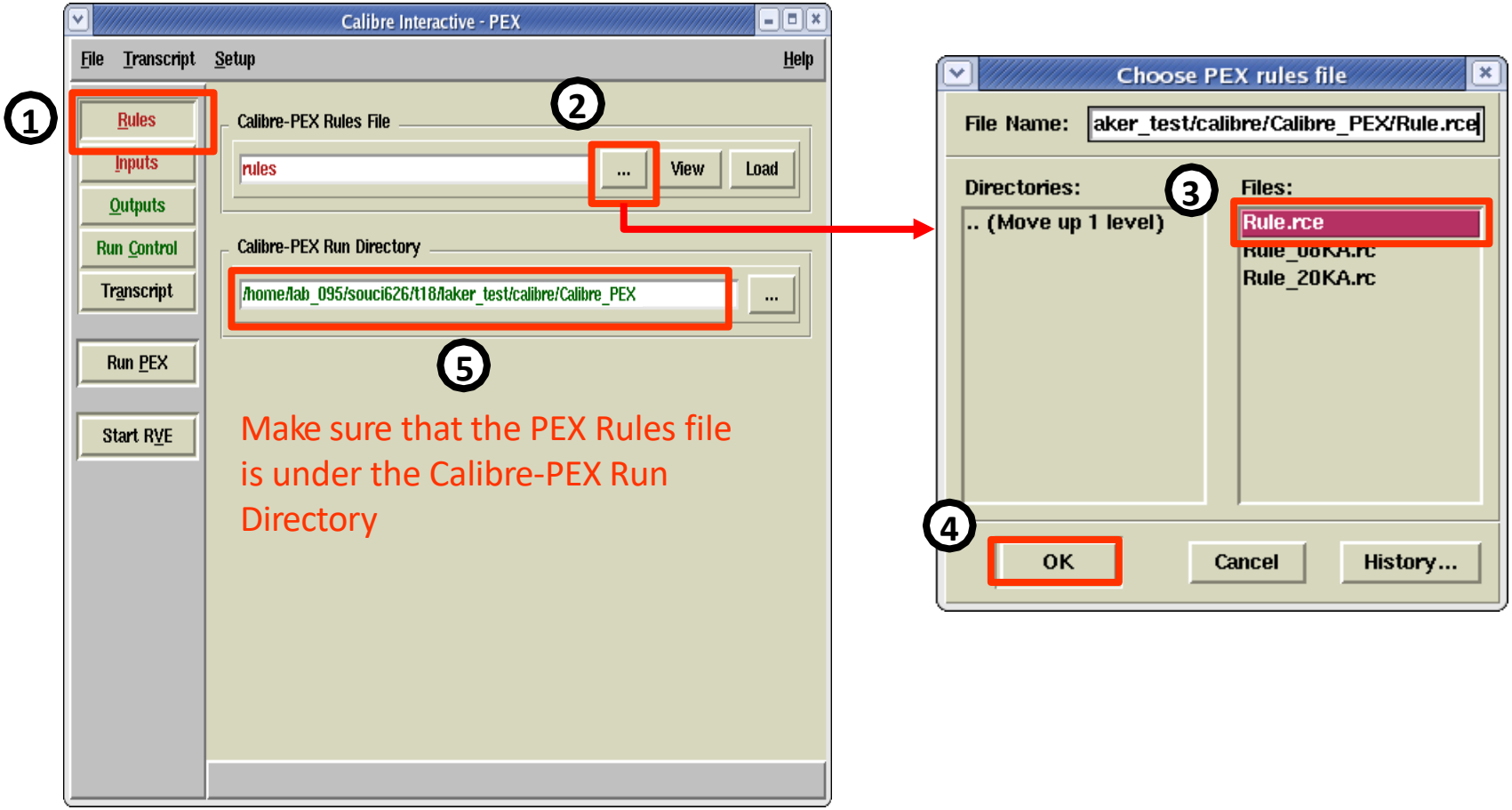



# PEX – Open PEX

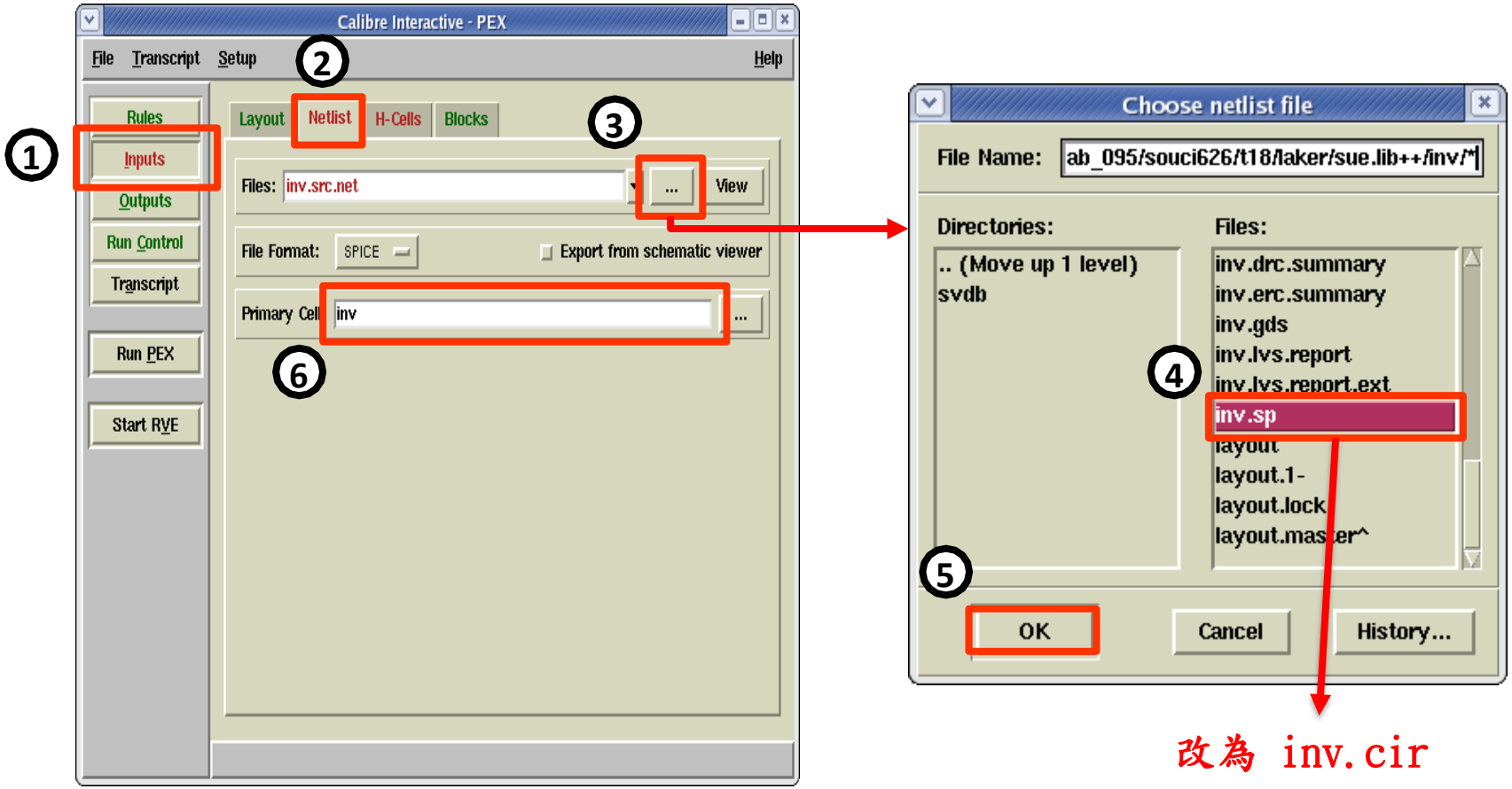

1
Laker_L3:97.sue:inv[Edit]
EIP
Verify
Router
Window
Help
Laker DRC...
Load DRC Error
Load Short Error
View DRC Error...
View Error...
Show Tip
2
Calibre
Run Interactive...
Run DRC...
Run LVS...
Run PEX...
Start RVE...
Clear Highlights
Integrate With RVE...
Options...
3


Calibre Interactive - PEX
File
Transcript
Setup
Help
Rules
Inputs
Outputs
Run Control
Transcript
Run PEX
Start RVE
Calibre-PEX Rules File
rules
View
Load
Calibre-PEX Run Directory
Load Runset File
Runset File Path
OK
Cancel
4

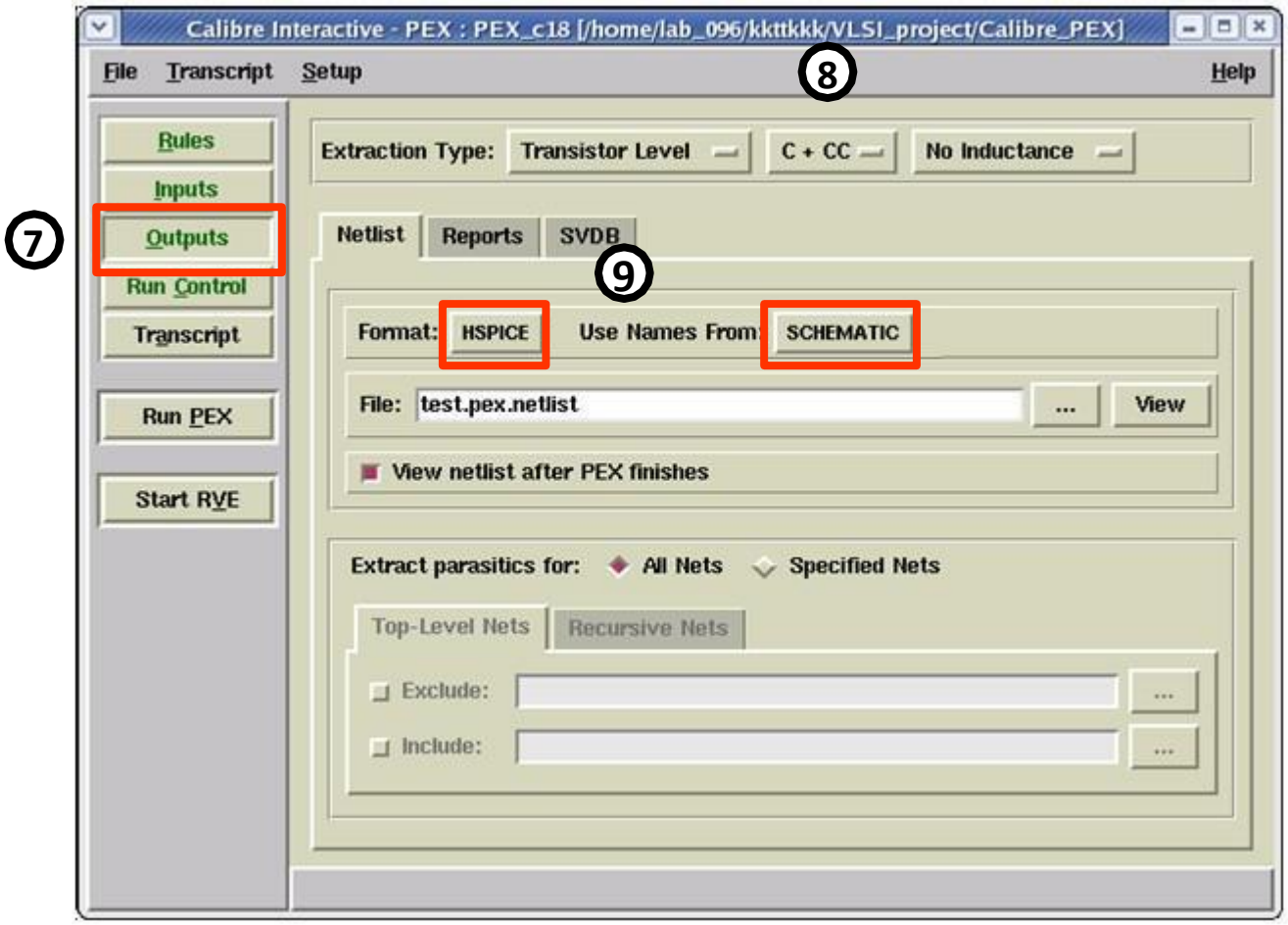
# PEX – Define PEX Rule



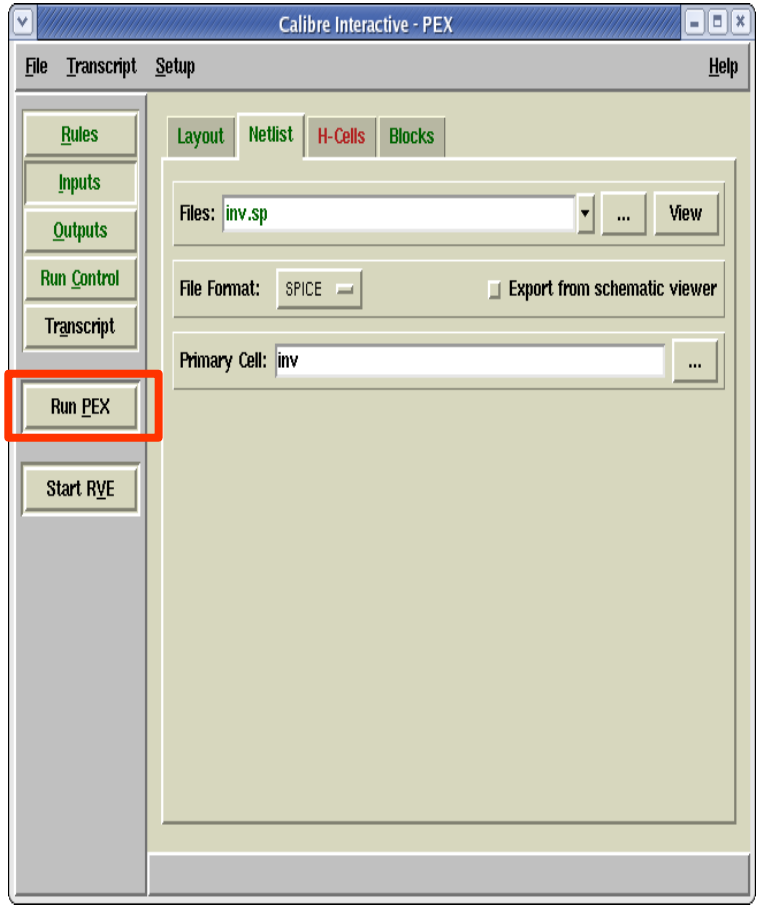
# PEX – Define Netlist File (1/2)

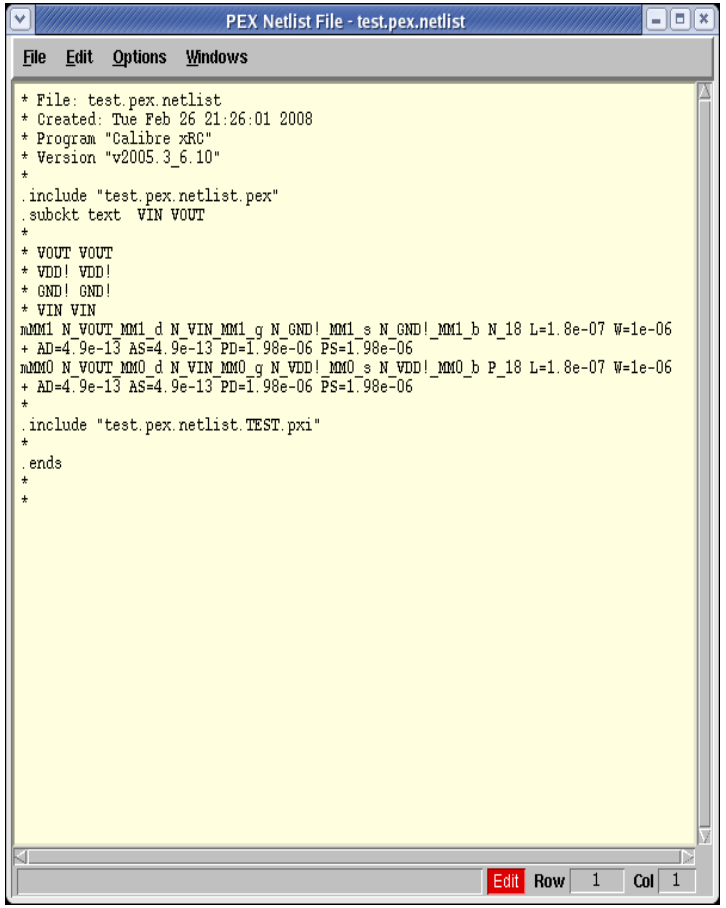


# PEX – Define Netlist File (2/2)



# PEX – PEX Result



# PEX – Netlist File

- Three output files:
  - xxx.pex.netlist
  - xxx.pex.netlist.pex
  - xxx.pex.netlist.xxx.pxi

Top circuit (ex: test.pex.netlist)

sub-circuit (ex: test.pex.netlist.pex)

connection (ex: test.pex.netlist.TEST.pxi)