National Cheng Kung University

Department of Electrical Engineering

VLSI Circuits Design

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Due Wednesday, May 18, 9am

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Problem 1 – Power (30%)

1A : Figure 1 shows an 8-input AND gate built by a tree of gates. If all of the input probabilities are 0.5, please **determine** the activity factors and probabilities at each node in the circuit.

※ **X1,X2,X3,X4 are the names of the nodes.** (10%)

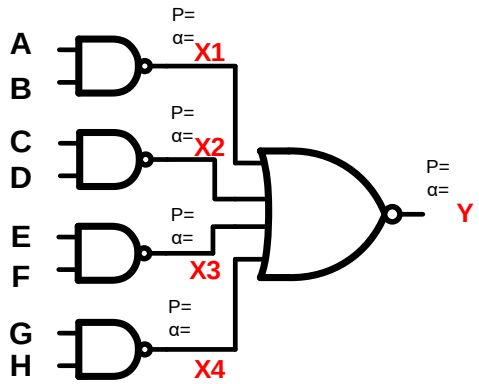

Figure 1. 8-input AND gate

1B : Consider an input signal as shown in Fig.2. and its rising and falling time are 100ps. The clock rate is 1MHz. **Determine** the activity factor for the signal. (5%)

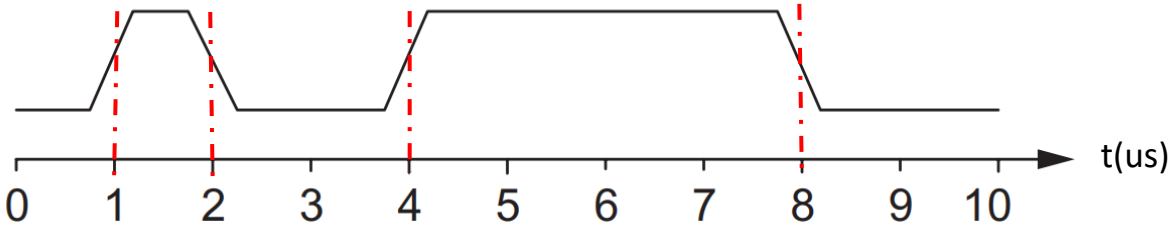

Figure 2. An input signal.

1C : Consider a 2-stage inverter buffer drives the capacitor, $100C_u$, as shown in Fig.3.

1C-a: First, design the circuit with the **minimum delay** and the first inverter input capacitor should be **4Cu**. What is the delay you calculate? And what is the size?

1C-b: Using Fig.2 as an input signal and using hspice to **measure** the power of circuit you designed in 1C-a. Additionally, you have to **calculate** the dynamic power and compare with hspice measurement result to **explain** the difference.

※ **Assume diffusion capacitors are 2fF/um when you calculate the dynamic power.**

1C-c: Changing the rising and falling time to one-tenth of the clock period and using hspice to mearsure its power again. Is there any difference between 1C-b and 1C-c? If so, please briefly explain it. (15%)

Note:

1. **Cu = 1fF.**
2. **Assume CG = 2fF/um .**
3. $Kn'/Kp' = 3/1$
4. **All transistors use minimum length.**

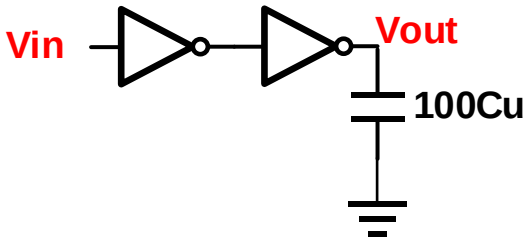

Figure 3. 2-stage inverter diagram.

```
*** clock_rate 1MHz
.param clock_rate = 1Meg
.param clk_period = 1/clock_rate
.param td = 100p
*** vin
vvin vin gnd pwl(
+  0 0v
+ 'clk_period-td/2' 0v
+ 'clk_period+td/2' 1.8v
**********************
*** omission ***
**********************
***
.tran 1p '10*clk_period'
*** meas power
.MEAS       power_avg   AVG   power
```

Figure 4. Reference code.

Problem 2 – Ring Oscillator(40%)

In many applications, we need to generate the clock signal in the chips. Therefore, the ring oscillator would be adopted. Fig.5. shows an N-stage ring oscillator using conventional inverter.

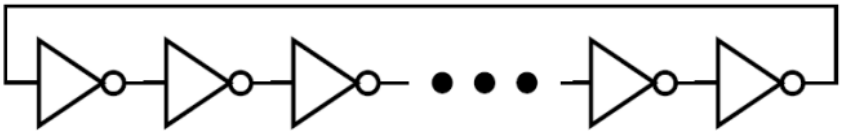

Figure 5. Ring Oscillator Circuit

2A Please derive and design a ring oscillator with **frequency of 3GHz**, and **the duty of the ring oscillator should be 50% ± 1%** . Finally, simulate it with HSpice.
Note: An initial condition at some node in the circuit is required

2B Create the layout of the ring oscillator you design in 2A and run the post-layout simulation(R+C+CC). Make sure the **frequency is 3GHZ and the duty is 50% ± 1%** and paste the result in the report. Please show the "No Error Figure" of the DRC and LVS verification, and paste the layout figure.

2C Fig.3 illustrate a Voltage-Controlled ring Oscillator (VCO). The control signals, V_{ctrl} and $\overline{V_{ctrl}}$, are used to control the current source so that the delay can be controlled by the signals. Please derive and design a VCO that the center frequency is **3GHz** when V_{ctrl} = $\overline{V_{ctrl}}$ = 0.9V. Furthermore, the frequency should **cover from 2.9G to 3.1GHz** when $\boldsymbol{V_{ctrl}}$ **= 0.7~1.1V and** $\overline{\boldsymbol{V_{ctrl}}}$ **= 1.8V -** $\boldsymbol{V_{ctrl}}$. Finally, simulate it with HSpice.
Note: An initial condition at some node in the circuit is required

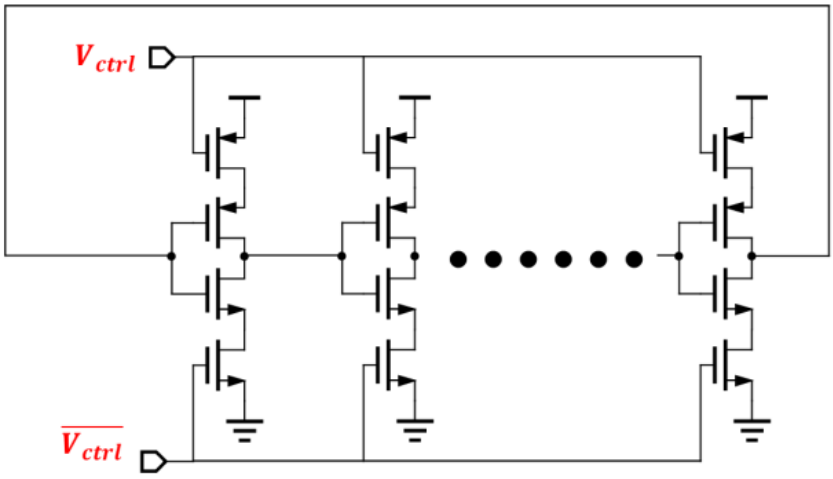

Figure 6. Voltage-Controlled ring Oscillator

```
.meas tran period trig v(vin) val=0.9 fall=10 targ v(vin) val=0.9 fall=11
.meas tran frequency param='1/period'
.meas tran t_on trig v(vin) val=0.9 rise=10 targ v(vin) val=0.9 fall=11
.meas tran duty_cycle param='t_on/period'
```

Figure 7. Reference mearsurement code

Problem 3 - Power Delay Product(30%)

A 2-input static CMOS NAND gate with N-stage **inverting** buffer to drive the capacitor, 500Cu, as shown in Fig.8.

3A : Consider the circuit in Fig.8. How many stages will give the **minimum delay**, and how should the stages be sized? Furthermore, assume we **neglect the diffusion capacitances**. If the delay constraint is **between 30 τ and 29 τ** , what N should be set to give the **lowest** power, and how should the stages be sized? How much dynamic power does it consume?

※Cleary present your procedure with explanation and states your assumptions, if any.

Note:

1. **Each input capacitor of NAND is 10Cu**
2. **Cu = 1fF.**
3. **Assume CG = 2fF/um.**
4. $Kn'/Kp' = 2/1$
5. **All transistors use minimum length.**

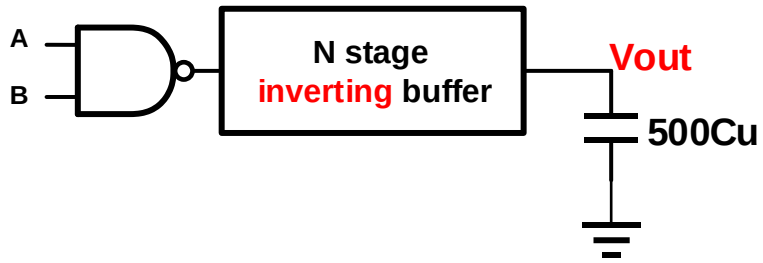

Figure 8. 2-input NAND with N-stage inverting buffer

3B : Consider the circuit shown in Fig.9. How should the stages be sized to get the **minimum Power Delay Product**?

Note:

1. **Cu = 1fF.**
2. **Assume CG = 2fF/um.**
3. $Kn'/Kp' = 2/1$
4. **All transistors use minimum length.**
5. **Each input capacitor of NAND is 10Cu**

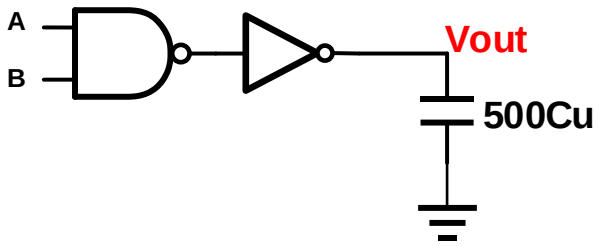

Figure 9. 2-input NAND with 1-stage inverting buffer

3C : Consider the circuit in 3B with the two input signals, A and B, illustrated in Fig.10. However, the input order of 2-input static NAND gate can affect the delay. Please derive the propagation rising delay (t_{pdr}) and the propagation falling delay (t_{pdf}) of NAND first to get the correct input order. **Clearly present your procedure with explanation and state your assumptions, if any**.
※Hint: You should consider the worst case with the input order.

Then, please sweep the sizes of the inverter to get the **figure of Power Delay Product,** and explain it on the report. According to the figure of Power Delay Product, choose the **best one sizes** and fill the Table.1.

Inverter size	t_{pdr}	t_{pdf}	t_{pd}	P_{avg}	$t_{pd} \cdot P_{avg}$
(Pmos_size) (Nmos_size)					

Table.1 the best sizeds chosen from the minimum PDP.

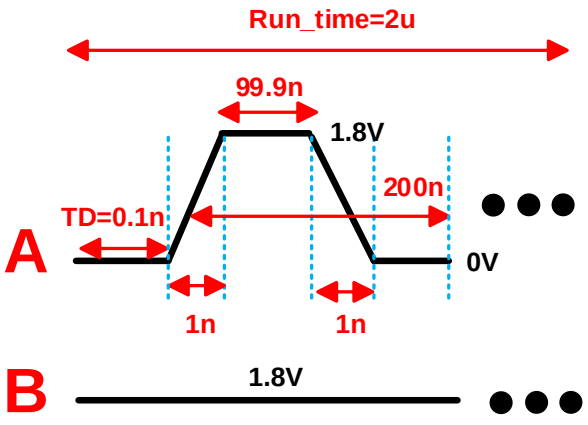

Figure 10. Input signals

```
.meas tran rising_delay
+trig v(vin)    val=0.9 td=td rise=5
+targ v(vout)   val=0.9 td=td rise=5
.meas tran falling_delay
+trig v(vin)    val=0.9 td=td fall=5
+targ v(vout)   val=0.9 td=td fall=5
.meas tran delay_avg
+param = '(rising_delay+falling_delay)/2'
.meas tran power
+avg  p(vdd) from=td to=run_time
.meas tran pdp
+param='abs(delay_avg*power)'
```

Figure 11. Reference measurement code.

-----Important Notes-----

1. 12pt character size in your report.
2. Please invert the color of all your schematics, waveforms and layout.
3. **DO NOT COPY**
4. **No late homework will be accepted. When it is due, it is due.**
5. It is needless to print your report. Please compress the needed files and report shown as below. Then upload your compressed file to moodle website.