VLSI Circuits Design HW#4

Course	Name	Student ID
[3] 2-4	陳旭祺	E24099059

- 1A - charge-sharing noise of dynamic gates

Please Design a 4-input footed dynamic gate which has the function as follow:

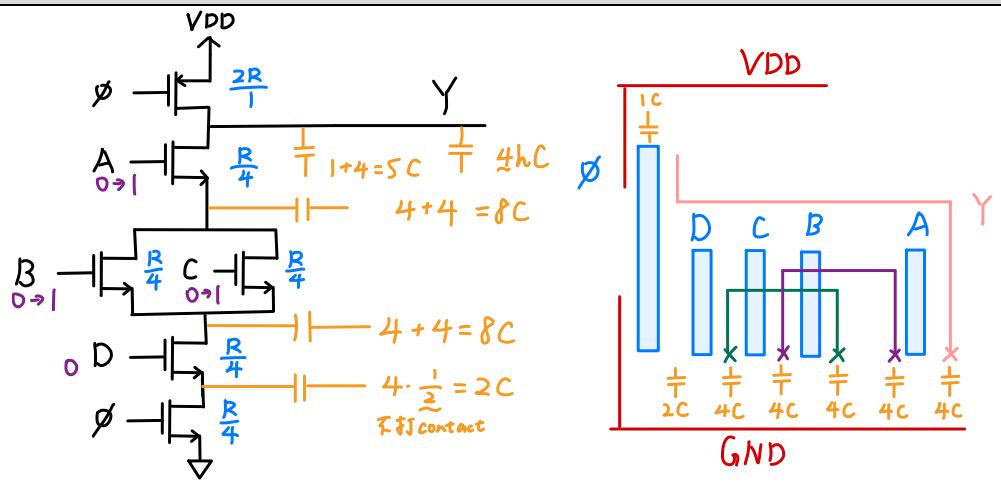
$$Y = \overline{A \cdot (B + C) \cdot D}$$

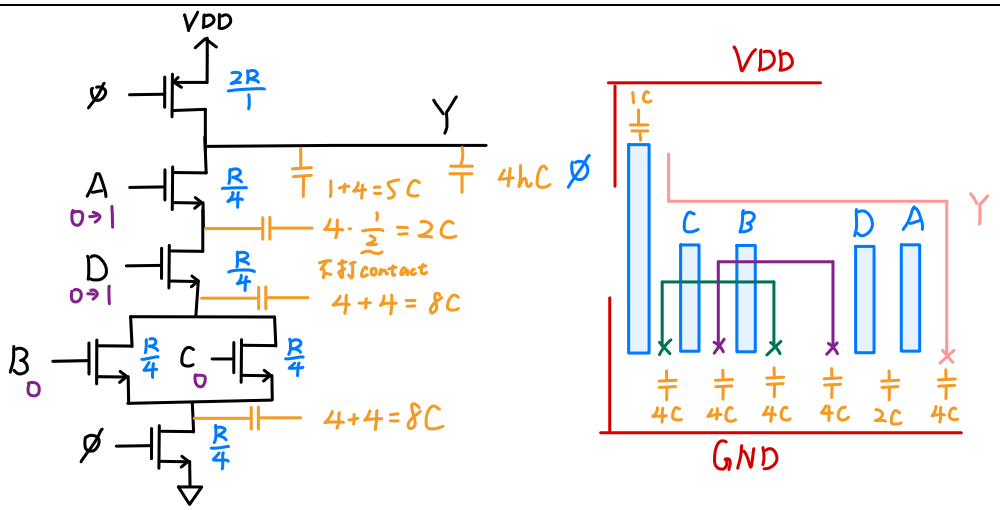
Draw the **schematic** and **stick diagram** you designed (label the I/O port and transistor size), and derive the worst charge-sharing noise as a fraction of V_{DD} and h (electrical effort). Finally, plot the graph of charge-sharing noise versus different electrical effort h from 1 to 7. You can use any tool to plot the graph, such as Excel or Matlab.

Assume that:

1. PMOS/NMOS mobility ratio = 0.5,
2. electrical effort = h,
3. diffusion capacitance on uncontacted nodes is about half of gate capacitance and on contacted nodes it equals gate capacitance.

Hint: You should consider the **input order** of your design. For the different input order, the layout of circuit will different, and the parasitic capacitance of intermediate nodes will also be different. **Choose the best input order** (the smallest charge sharing noise) as your design.

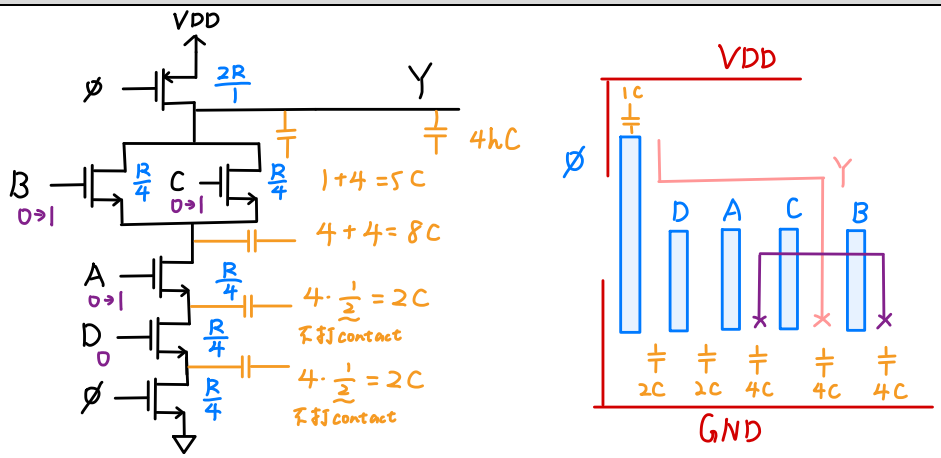
case 1
 $$V_Y = \frac{5C + 4hC}{5C + 4hC + 8C + 8C}$$ $$\Delta V = V_{DD} - V_Y = \left(1 - \frac{4h + 5}{4h + 21}\right) \cdot V_{DD}$$
case 2



$$V_Y = \frac{5C + 4hC}{5C + 4hC + 8C + 2C}$$

$$\Delta V = V_{DD} - V_Y = \left(1 - \frac{4h+5}{4h+15}\right) \cdot V_{DD}$$

case 3



$$V_Y = \frac{5C + 4hC}{5C + 4hC + 8C + 2C}$$

$$\Delta V = V_{DD} - V_Y = \left(1 - \frac{4h+5}{4h+15}\right) \cdot V_{DD}$$

comparison

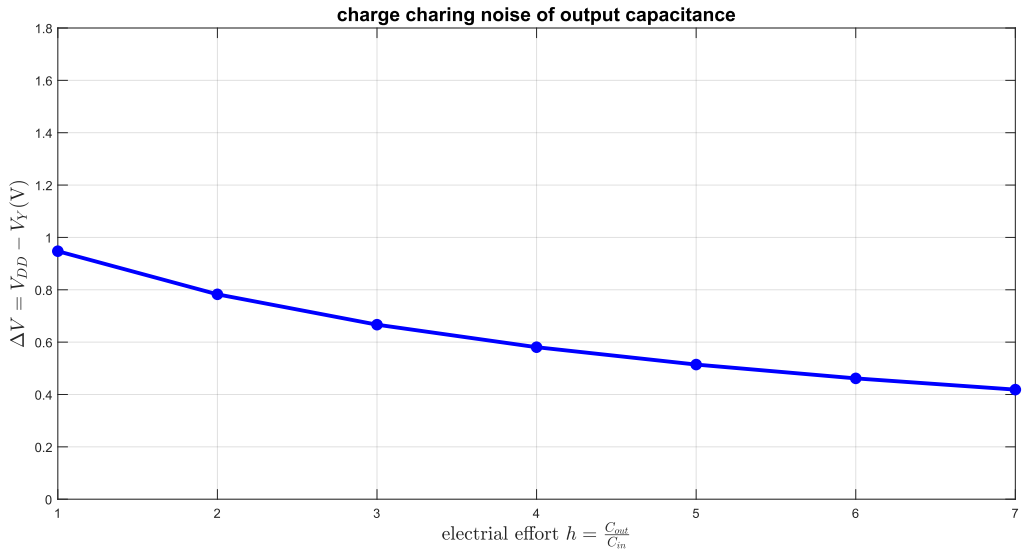
設計4-input footed dynamic gate $Y = \overline{A \cdot (B + C) \cdot D}$，畫出NMOS邏輯電路，由於題目規定是footed電路，上面使用一顆CLK驅動的PMOS和下面一顆CLK驅動的NMOS，由於precharge階段時，不需要在乎速度問題，所以PMOS的size給最低，而下方pull-down通路則選擇電阻R。

再來是決定要用哪種input order，才能最小化"input pattern中最差的charge sharing noise"，分3種不同input order下去討論，畫出stick diagram(layout草稿)計算各個節點的寄生電容，這裡遇到的問題 - 是否要考慮transistor folding，考慮下去就又分很多情況，之後詢問助教是不用考慮，這樣也好，能簡化問題。

如以上3種情況，在不考慮transistor folding的前提下，layout最好的畫法如上圖所示，選擇最小charge sharing noise，即是使輸出電壓ΔV變化幅度小，理論值

計算case 2、case 3相等並比case 1小，而case 3又比case 2更好，因為case 3的diffusion不會中斷，可以減少整體寄生電容。

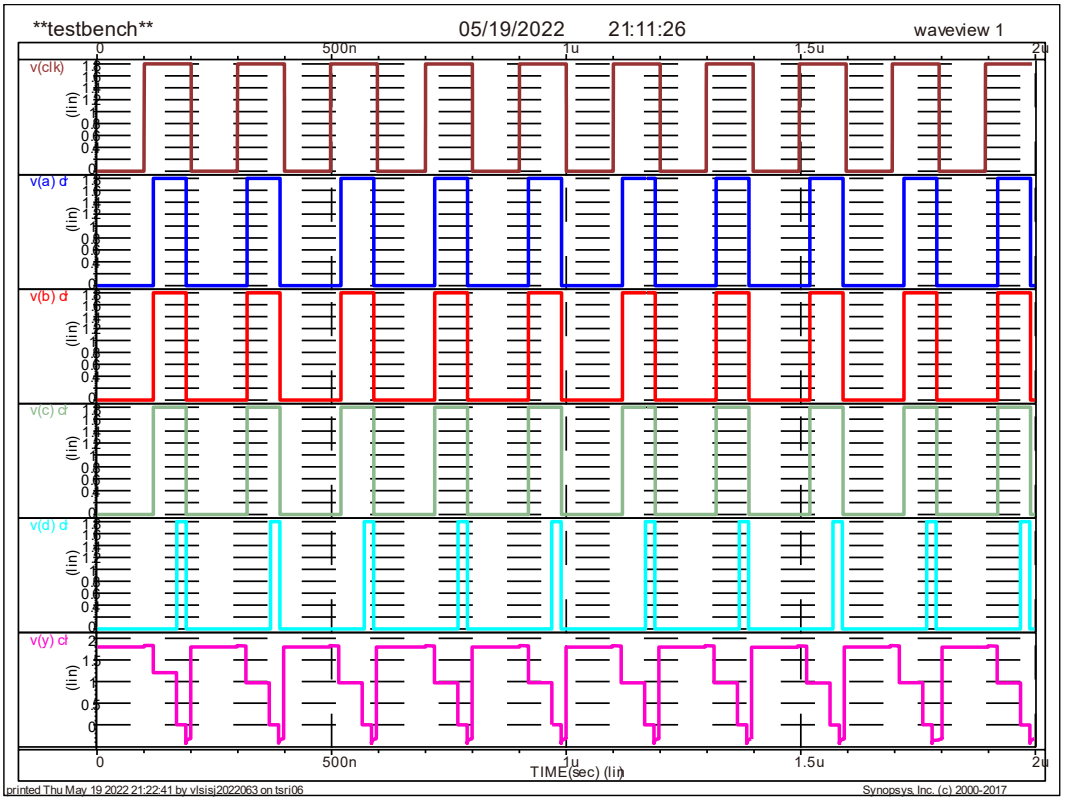
因此使用case 3的input order，charge-sharing noise對electrical effort h的matlab作圖如下



- 1B - presim charge sharing noise

Please simulate the 4-input footed dynamic gate that you have designed in 1A.
You should design the input pattern which causing the worst charge sharing noise at output(Xout). Please write testbench(.sp) by yourself, and Paste the **pre-simulation waveform** and label the amplitude of charge sharing noise.
Assume that:
1. MOS unit size (W/L) = (0.5um/0.18um)
2. Output load a unit-size inverter (inverter output is floating)
3. Input pattern pulses have rising/falling duration = 100ps (from 0 to VDD)
4. The amplitude of charge sharing noise = VDD – VY (Xout = 1)

presim waveform



解釋

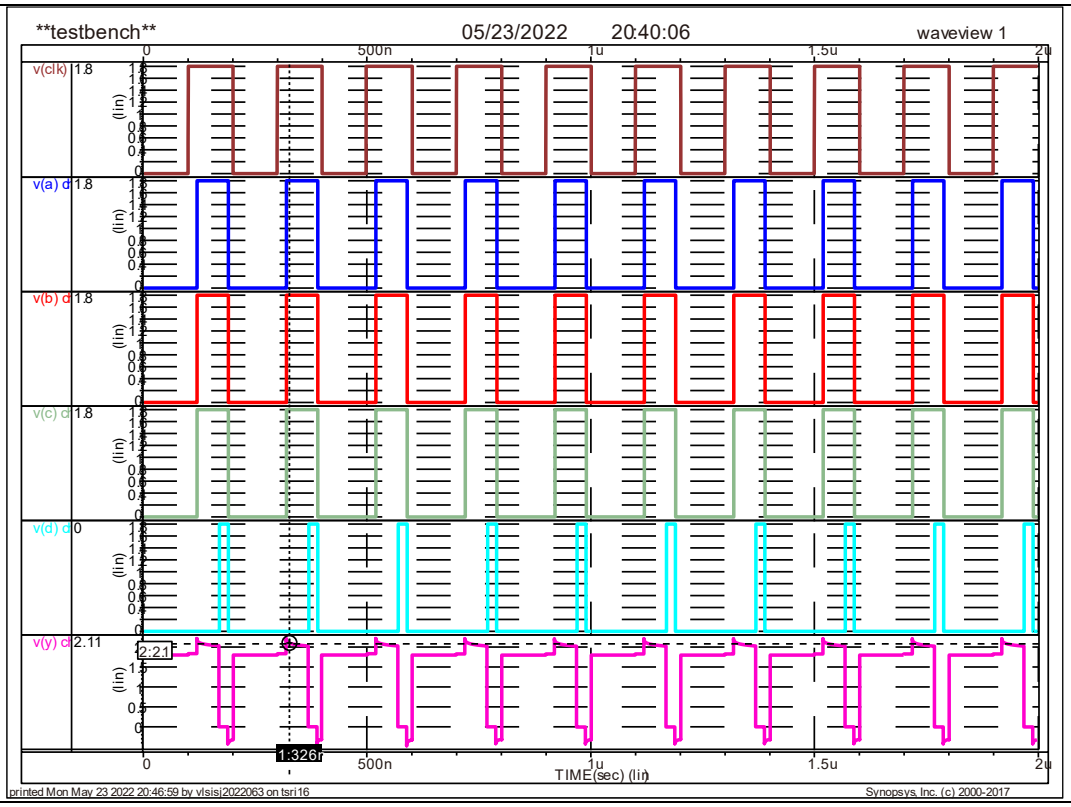
設計的input pattern如1A小題，D關閉，代表輸出應該要是V_{DD}，而A、B、C同時由0變為1，打開後由於輸出端看到內部寄生電容，所以產生charge sharing noise，輸出節點V_Y從原本$V_{DD} = 1.8V$降至$1V$，因此$\Delta V = V_{DD} - V_Y = 1.8 - 1 = 0.8V$，此外input pattern需要注意的是 - 最後要把下面的通路打開，讓所有寄生電容放完電，下一個state才可以繼續觀測到charge sharing noise現象。

● 1C - secondary precharge

From above question 1B, please revise the circuit to deal with the charge sharing issue. Do pre-simulation (the testbench in 1C and 1B should be the same), and plot **waveform** to verify that the output is free from charge sharing noise, and finally explain your approach. In worst case, the amplitude of charge sharing noise should be smaller than 0.1V.

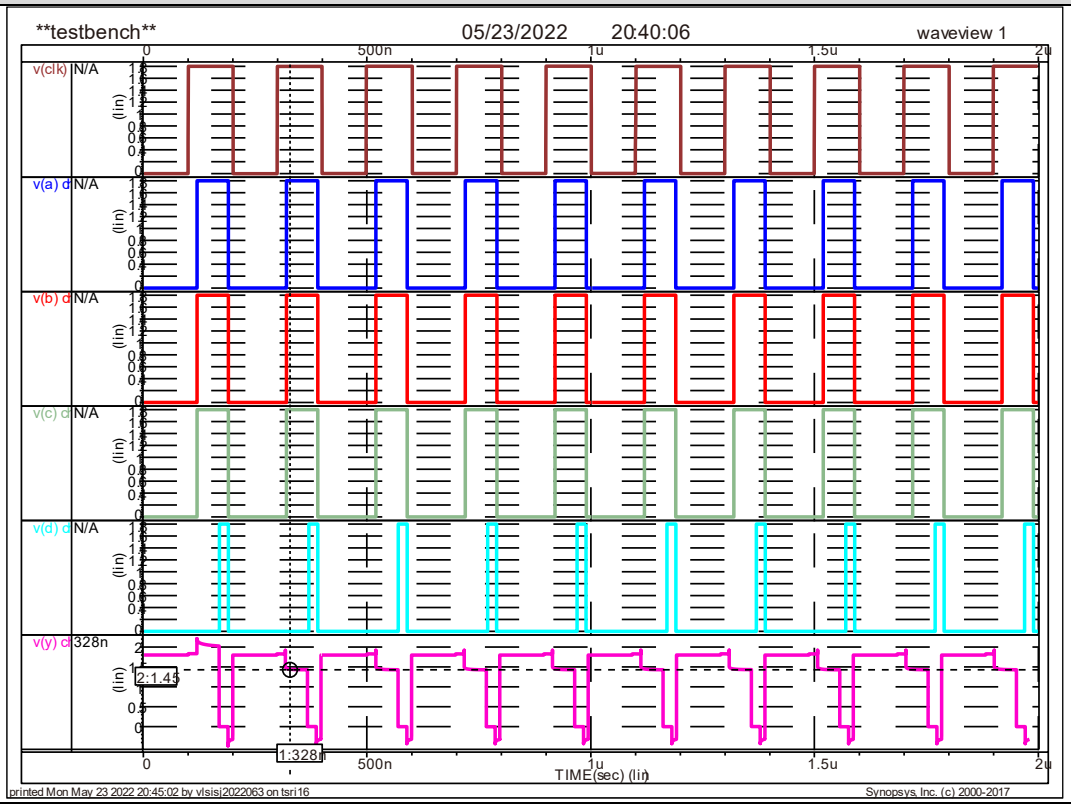
詢問出題助教後，本題SPEC只要求輸出電壓大於$1.8 - 0.1 = 1.7V$即可，從DC transfer characteristics圖觀察，就算輸出電壓高於V_{DD}，對下一級電路來說也是判別為"1"，而低於V_{DD}比較危險，如果低於下一級電路的switching threshold voltage就會出問題。

嘗試1 - secondary precharge在B、C與A之間MOS的節點，修正後$V_Y = 2.21V > 1.7V$，符合SPEC要求。

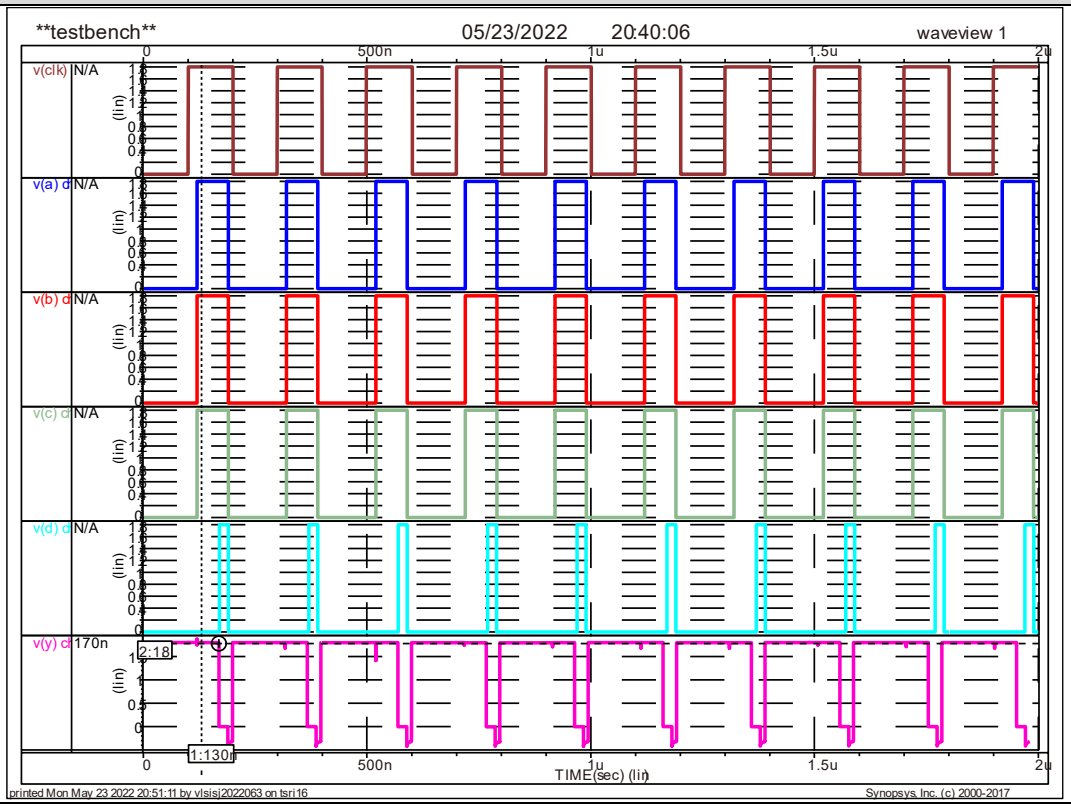


可以使用secondary precharge，此時電壓高於V_{DD}是符合SPEC，發生原因為考慮寄生電容V_{gd}，電容一端為輸出V_{DD}，而另一端為原先的輸入值0，當輸入值從0變為V_{DD}時，為了維持電容兩端跨壓固定，另一端輸出會從V_{DD}衝到$2V_{DD}$，之後才會被下面的電容分壓掉，使電壓下降而停在V_{DD}到$2V_{DD}$之間。

嘗試2(X) - secondary precharge在A與D之間MOS的節點，修正後$V_Y = 1.45V < 1.7V$，不符合SPEC要求。



嘗試3 - 負載inverter後面拉一條線負回授接keeper，修正後$V_Y = 1.8V > 1.7V$，符合SPEC要求。



可以使用keeper，但實務上需要控制不可以讓charge sharing noise影響的輸出電壓低於keeper負回授那顆inverter的switching threshold voltage，如果低於switching threshold voltage，這樣負回授那顆inverter判別為"0"，輸出則為1，PMOS就不開，就無法讓輸出電壓往上修正至V_{DD}。

● 2A - calculation of different gate

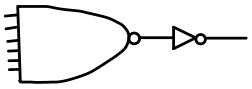
Design a fast 6-input AND gate in each of the following circuit families.
1) Static CMOS
2) Pseudo-nMOS with pMOS transistors 1/4 the strength of the pulldown stack
3) Domino (a **footed dynamic gate** followed by a **HI-skew** static gate), only optimize the delay from rising input to rising output.

Sketch an implementation using two stages of logic (e.g., AND6+INV, NAND3 + NOR2, etc.). Label each gate with the width of the pMOS and nMOS transistors. Each input can drive no more than 30 λ of transistor width. The output must drive a 80λ/40λ inverter (i.e., an inverter with a 80 λ wide pMOS and 40 λ wide nMOS transistor). Use logical effort to choose the topology and size for least average delay. Estimate the delay using logical effort and show the calculation process. When estimating parasitic delays, count only the diffusion capacitance on the output node. (λ=180nm/2=90nm)

$$\min H = \min \frac{C_{out}}{C_{in}} = \min \frac{W_{out}}{W_{in}} = \frac{80\lambda + 40\lambda}{30\lambda} = \frac{120}{3} = 4$$

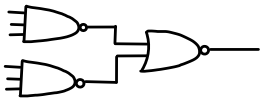
A. Static CMOS

I. NAND6 and INV



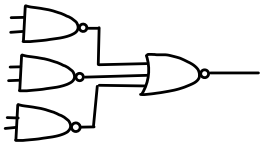
1. 計算path effort $F = GBH = \left(\frac{6+2}{3} \cdot 1\right)(1 \cdot 1) \cdot 4 = \frac{8}{3} \cdot 4$。
2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{8}{3} \cdot 4\right)^{\frac{1}{2}} + (6 + 1) = 13.53$。

II. NAND3 and NOR2



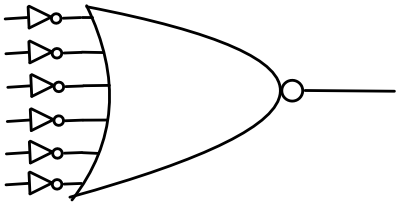
1. 計算path effort $F = GBH = \left(\frac{3+2}{3} \cdot \frac{2 \cdot 2+1}{3}\right)(1 \cdot 1) \cdot 4 = \frac{25}{9} \cdot 4$。
2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{25}{9} \cdot 4\right)^{\frac{1}{2}} + (3 + 2) = 11.67$。

III. NAND2 and NOR3



1. 計算path effort $F = GBH = \left(\frac{2+2}{3} \cdot \frac{2 \cdot 3+1}{3}\right)(1 \cdot 1) \cdot 4 = \frac{28}{9} \cdot 4$。
2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{28}{9} \cdot 4\right)^{\frac{1}{2}} + (2 + 3) = 12.06$。

IV. INV and NOR6



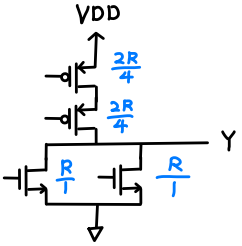
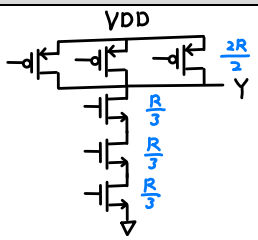
1. 計算path effort $F = GBH = \left(1 \cdot \frac{2 \cdot 6+1}{3}\right)(1 \cdot 1) \cdot 4 = \frac{13}{3} \cdot 4$。
2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{13}{3} \cdot 4\right)^{\frac{1}{2}} + (1 + 6) = 15.33$。

比較1到4的電路，選擇delay time最小(11.67)的第2種電路NAND3 and NOR2，接下來決定各級邏輯閘電晶體的sizing。

1. 計算各級邏輯閘的effort均為$\hat{f} = F^{\frac{1}{N}} = \left(\frac{25}{9} \cdot 4\right)^{\frac{1}{2}} = \frac{10}{3}$。
2. 從後往前推，計算每一級的輸入電容(電晶體W)值 $\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}, C \propto W$。

$$W_{in} = \frac{\frac{5}{3}(120 \cdot 90 \text{ nm})}{\frac{10}{3}} = 5400 \text{ nm}$$

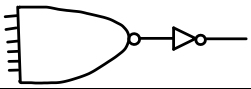
$$(W_{in})' = \frac{\frac{5}{3}(5400\ \text{nm})}{\frac{10}{3}} = 2700\ \text{nm}$$

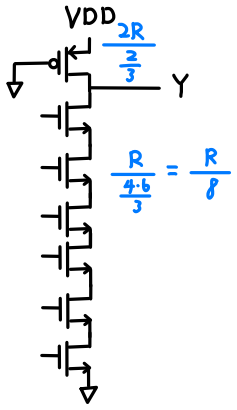
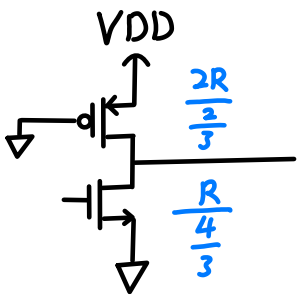
第二級NOR2	
	$\text{PMOS} : W = 5400 \cdot \frac{4}{5} = 4320nm$ $\text{NMOS} : W = 5400 \cdot \frac{1}{5} = 1080nm$
第一級NAND3	
	$\text{PMOS} : W = 2700 \cdot \frac{2}{5} = 1080nm$ $\text{NMOS} : W = 2700 \cdot \frac{3}{5} = 1620nm$

B. Pseudo-nmos

NAND gate用pseudo-nmos反而會比static慢，電路第一級用static，第二級用pseudo-nmos，如此delay會比較小，但現在助教規定每一級通通都要用pseudo-nmos。

I. NAND6 and INV



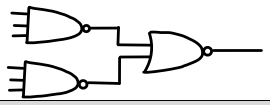
第一級NAND6	
	$g_u = g_d \cdot 3 = \frac{24}{3}$ $g_d = 8 \cdot \frac{1}{3} = \frac{8}{3}$ $g_{avg} = \frac{1}{2}\left(\frac{8}{3} + \frac{24}{3}\right) = \frac{1}{2} \cdot \frac{32}{3} = \frac{16}{3}$ $p_u = p_d \cdot 3 = \frac{78}{9}$ $p_d = \left(\frac{2}{3} + \frac{24}{3}\right) \cdot \frac{1}{3} = \frac{26}{9}$ $p_{avg} = \frac{1}{2}\left(\frac{26}{9} + \frac{78}{9}\right) = \frac{1}{2} \cdot \frac{104}{9} = \frac{52}{9}$
第二級INV	
	$g_u = g_d \cdot 3 = \frac{12}{9}$ $g_d = \frac{4}{3} \cdot \frac{1}{3} = \frac{4}{9}$ $g_{avg} = \frac{1}{2}\left(\frac{12}{9} + \frac{4}{9}\right) = \frac{1}{2} \cdot \frac{4 \cdot 4}{9} = \frac{8}{9}$ $p_u = p_d \cdot 3 = 2$ $p_d = \left(\frac{2}{3} + \frac{4}{3}\right) \cdot \frac{1}{3} = \frac{2}{3}$

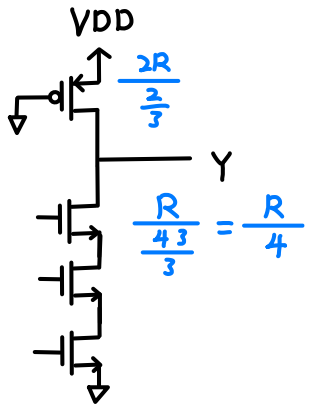
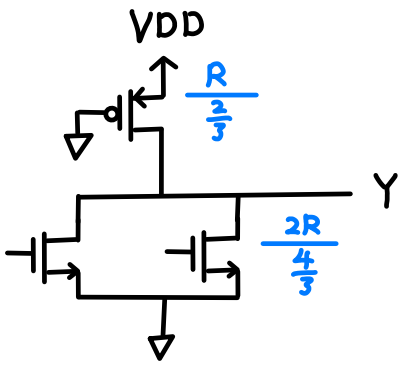
	$p_{avg}=\frac{1}{2}\left(\frac{6}{3}+\frac{2}{3}\right)=\frac{1}{2}\cdot\frac{8}{3}=\frac{4}{3}$

1. 計算path effort $F=GBH=\left(\frac{16}{3}\cdot\frac{8}{9}\right)(1\cdot 1)\cdot 4=\frac{128}{27}\cdot 4$。

2. 計算此path最小delay time是$D=NF^{\frac{1}{N}}+P=2\cdot\left(\frac{128}{27}\cdot 4\right)^{\frac{1}{2}}+\left(\frac{52}{9}+\frac{4}{3}\right)=15.82$。

II. NAND3 and NOR2

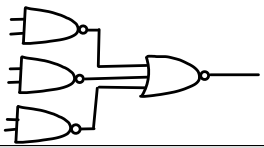


第一級NAND3	
	$g_u=g_d\cdot 3=\frac{12}{3}$ $g_d=4\cdot\frac{1}{3}=\frac{4}{3}$ $g_{avg}=\frac{1}{2}\left(\frac{4}{3}+\frac{12}{3}\right)=\frac{1}{2}\cdot\frac{16}{3}=\frac{8}{3}$ $p_u=p_d\cdot 3=\frac{41}{9}$ $p_d=\frac{14}{3}\cdot\frac{1}{3}=\frac{14}{9}$ $p_{avg}=\frac{1}{2}\left(\frac{14}{9}+\frac{41}{9}\right)=\frac{1}{2}\cdot\frac{55}{9}=\frac{55}{18}$
第二級NOR2	
	$g_u=g_d\cdot 3=\frac{12}{9}$ $g_d=\frac{4}{3}\cdot\frac{1}{3}=\frac{4}{9}$ $g_{avg}=\frac{1}{2}\left(\frac{12}{9}+\frac{4}{9}\right)=\frac{1}{2}\cdot\frac{16}{9}=\frac{8}{9}$ $p_u=p_d\cdot 3=\frac{30}{9}$ $p_d=\frac{10}{3}\cdot\frac{1}{3}=\frac{10}{9}$ $p_{avg}=\frac{1}{2}\left(\frac{30}{9}+\frac{10}{9}\right)=\frac{1}{2}\cdot\frac{40}{9}=\frac{20}{9}$

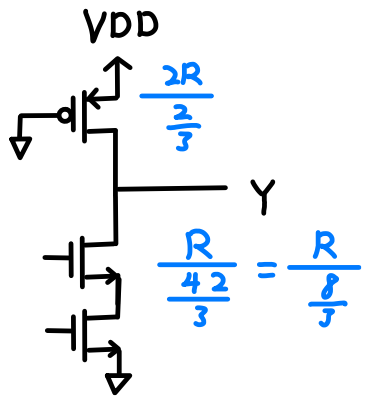
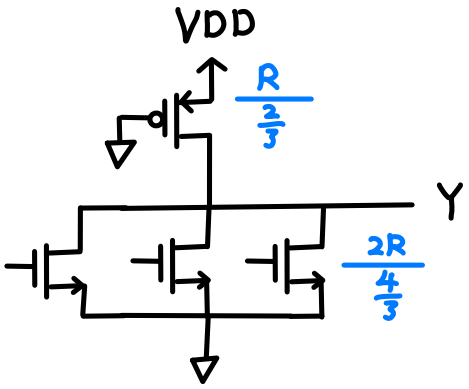
1. 計算path effort $F=GBH=\left(\frac{8}{3}\cdot\frac{8}{9}\right)(1\cdot 1)\cdot 4=\frac{64}{27}\cdot 4$。

2. 計算此path最小delay time是$D=NF^{\frac{1}{N}}+P=2\cdot\left(\frac{64}{27}\cdot 4\right)^{\frac{1}{2}}+\left(\frac{55}{18}+\frac{20}{9}\right)=11.45$。

III. NAND2 and NOR3



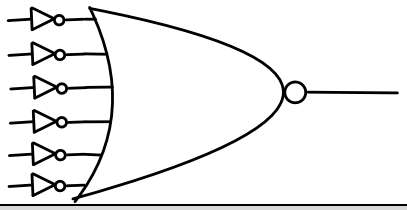
第一級NAND2

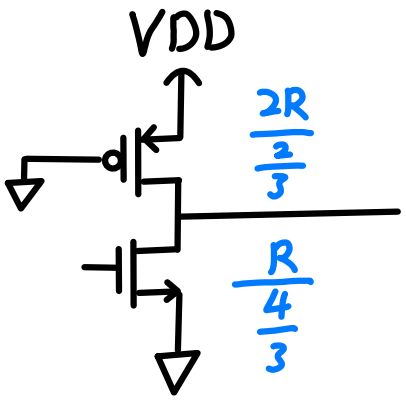
	$g_u = g_d \cdot 3 = \frac{24}{9}$ $g_d = \frac{8}{3} \cdot \frac{1}{3} = \frac{8}{9}$ $g_{avg} = \frac{1}{2}\left(\frac{24}{9} + \frac{8}{9}\right) = \frac{1}{2} \cdot \frac{32}{9} = \frac{16}{9}$ $p_u = p_d \cdot 3 = \frac{30}{9}$ $p_d = \frac{10}{3} \cdot \frac{1}{3} = \frac{10}{9}$ $p_{avg} = \frac{1}{2}\left(\frac{30}{9} + \frac{10}{9}\right) = \frac{1}{2} \cdot \frac{40}{9} = \frac{20}{9}$
第二級NOR3	
	$g_u = g_d \cdot 3 = \frac{12}{9}$ $g_d = \frac{4}{3} \cdot \frac{1}{3} = \frac{4}{9}$ $g_{avg} = \frac{1}{2}\left(\frac{12}{9} + \frac{4}{9}\right) = \frac{1}{2} \cdot \frac{16}{9} = \frac{8}{9}$ $p_u = p_d \cdot 3 = \frac{42}{9}$ $p_d = \frac{14}{3} \cdot \frac{1}{3} = \frac{14}{9}$ $p_{avg} = \frac{1}{2}\left(\frac{42}{9} + \frac{14}{9}\right) = \frac{1}{2} \cdot \frac{56}{9} = \frac{28}{9}$

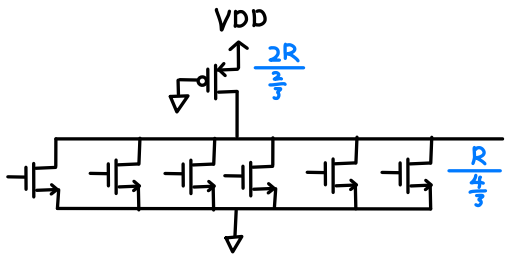
1. 計算path effort $F = GBH = \left(\frac{16}{9} \cdot \frac{8}{9}\right)(1 \cdot 1) \cdot 4 = \frac{128}{81} \cdot 4$。

2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{128}{81} \cdot 4\right)^{\frac{1}{2}} + \left(\frac{8}{9} + \frac{28}{9}\right) = 10.36$。

IV. INV and NOR6



第一級INV	
	$g_u = g_d \cdot 3 = \frac{12}{9}$ $g_d = \frac{4}{3} \cdot \frac{1}{3} = \frac{4}{9}$ $g_{avg} = \frac{1}{2}\left(\frac{12}{9} + \frac{4}{9}\right) = \frac{1}{2} \cdot \frac{16}{9} = \frac{8}{9}$ $p_u = p_d \cdot 3 = \frac{6}{3}$ $p_d = \left(\frac{2}{3} + \frac{4}{3}\right) \cdot \frac{1}{3} = \frac{2}{3}$ $p_{avg} = \frac{1}{2}\left(\frac{6}{3} + \frac{2}{3}\right) = \frac{1}{2} \cdot \frac{8}{3} = \frac{4}{3}$

第二級NOR6	
	$g_u = g_d \cdot 3 = \frac{12}{9}$ $g_d = \frac{4}{3} \cdot \frac{1}{3} = \frac{4}{9}$ $g_{avg} = \frac{1}{2}\left(\frac{12}{9} + \frac{4}{9}\right) = \frac{1}{2} \cdot \frac{16}{9} = \frac{8}{9}$ $p_u = p_d \cdot 3 = \frac{78}{9}$ $p_d = \frac{26}{3} \cdot \frac{1}{3} = \frac{26}{9}$ $p_{avg} = \frac{1}{2}\left(\frac{78}{9} + \frac{26}{9}\right) = \frac{1}{2} \cdot \frac{104}{9} = \frac{52}{9}$

1. 計算path effort $F = GBH = \left(\frac{8}{9} \cdot \frac{8}{9}\right)(1 \cdot 1) \cdot 4 = \frac{64}{81} \cdot 4$。

2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{64}{81} \cdot 4\right)^{\frac{1}{2}} + \left(\frac{8}{9} + \frac{52}{9}\right) = 10.67$。

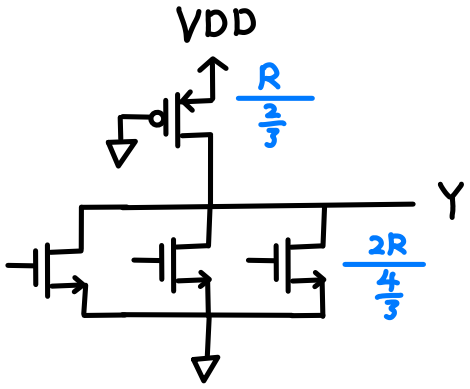
比較1到4的電路，選擇delay time最小(10.36)的第3種電路NAND2 and NOR3，接下來決定各級邏輯閘電晶體的sizing。

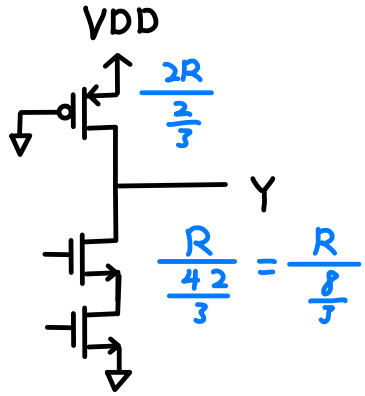
1. 計算各級邏輯閘的effort均為$\hat{f} = F^{\frac{1}{N}} = \left(\frac{128}{81} \cdot 4\right)^{\frac{1}{2}} = 2.514$。

2. 從後往前推，計算每一級的輸入電容(電晶體W)值 $\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}, C \propto W$。

$$W_{in} = \frac{\frac{8}{9}(120 \cdot 90\ \text{nm})}{2.514} = 3818\ \text{nm}$$

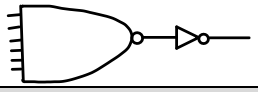
$$(W_{in})' = \frac{\frac{16}{9}(3818\ \text{nm})}{2.514} = 2700\ \text{nm}$$

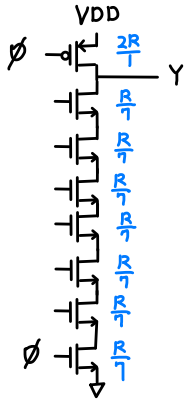
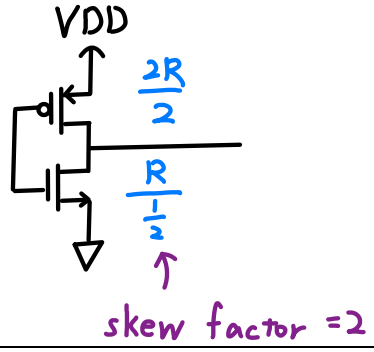
第二級NOR3	
	PMOS : $W = 3818 \cdot \frac{4}{5} = 1909 \approx 1910nm$ NMOS : $W = 3818 \approx 3820nm$ (pseudo-nmos的C_{in}全給NMOS)
第一級NAND2	

	PMOS : $W = 2700 \cdot \frac{1}{4} = 675 \approx 680nm$ NMOS : $W = 2700nm$ (pseudo-nmos的C_{in}全給NMOS)

C. Domino(footed dynamic + HI-skew)

I. NAND6 and INV

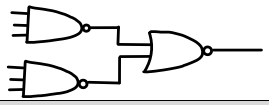


第一級NAND6	
	$g_d = \frac{7}{3}$ $p_u = \frac{8}{3}$
第二級INV	
	$g_u = \frac{2.5}{3} = \frac{5}{6}$ $(g_d = \frac{2.5}{1.5} = \frac{5}{3})$ $p_u = \frac{2.5}{3} = \frac{5}{6}$

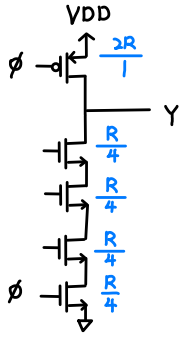
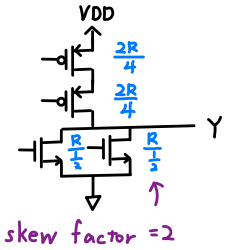
1. 計算path effort $F = GBH = \left(\frac{7}{3} \cdot \frac{5}{6}\right)(1 \cdot 1) \cdot 4 = \frac{35}{18} \cdot 4$。

2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{35}{18} \cdot 4\right)^{\frac{1}{2}} + \left(\frac{8}{3} + \frac{5}{6}\right) = 9.08$。

II. NAND3 and NOR2

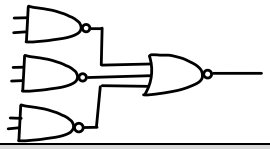


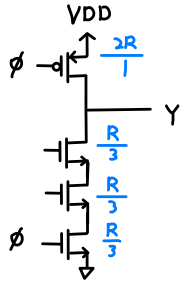
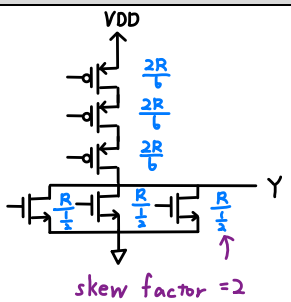
第一級NAND3

	$g_d = \frac{4}{3}$ $p_u = \frac{5}{3}$
第二級NOR2	
	$g_u = \frac{4.5}{3} = \frac{9}{6}$ $(g_d = \frac{4.5}{1.5} = \frac{9}{3})$ $p_u = \frac{5}{3}$

1. 計算path effort $F = GBH = \left(\frac{4}{3} \cdot \frac{9}{6}\right)(1 \cdot 1) \cdot 4 = 2 \cdot 4$。
2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot (2 \cdot 4)^{\frac{1}{2}} + \left(\frac{5}{3} + \frac{5}{3}\right) = 8.99$。

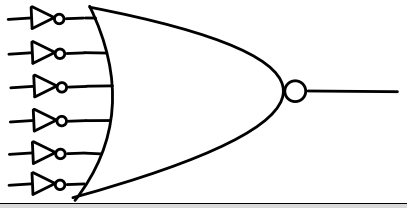
III. NAND2 and NOR3

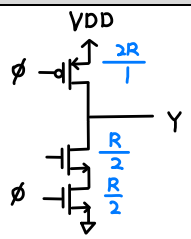
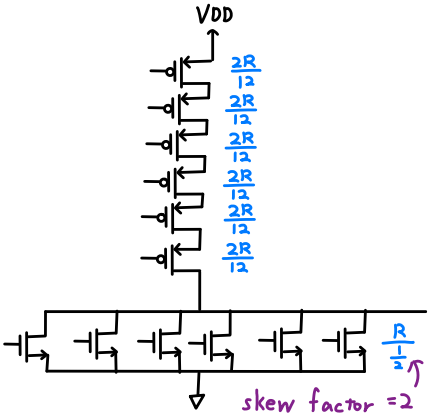


第一級NAND2	
	$g_d = \frac{3}{3} = 1$ $p_u = \frac{4}{3}$
第二級NOR3	
	$g_u = \frac{6.5}{3} = \frac{13}{6}$ $(g_d = \frac{6.5}{1.5} = \frac{13}{3})$ $p_u = \frac{7.5}{3} = \frac{15}{6}$

1. 計算path effort $F = GBH = \left(1 \cdot \frac{13}{6}\right)(1 \cdot 1) \cdot 4 = \frac{13}{6} \cdot 4$。
2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{13}{6} \cdot 4\right)^{\frac{1}{2}} + \left(\frac{4}{3} + \frac{15}{6}\right) = 9.72$。

IV. INV and NOR6



第一級INV	
	$g_d = \frac{2}{3}$ $p_u = \frac{3}{3}$
第二級NOR6	
	$g_u = \frac{12.5}{3} = \frac{25}{6}$ $(g_d = \frac{12.5}{1.5} = \frac{25}{3})$ $p_u = \frac{15}{3}$

1. 計算path effort $F = GBH = \left(\frac{2}{3} \cdot \frac{25}{6}\right)(1 \cdot 1) \cdot 4 = \frac{50}{18} \cdot 4$。

2. 計算此path最小delay time是$D = NF^{\frac{1}{N}} + P = 2 \cdot \left(\frac{50}{18} \cdot 4\right)^{\frac{1}{2}} + \left(\frac{3}{3} + \frac{15}{3}\right) = 12.67$。

比較1到4的電路，選擇delay time最小(8.99)的第2種電路NAND3 and NOR2，接下來決定各級邏輯閘電晶體的sizing。

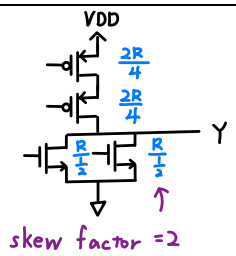
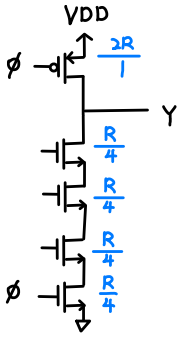
1. 計算各級邏輯閘的effort均為$\hat{f} = F^{\frac{1}{N}} = (2 \cdot 4)^{\frac{1}{2}} = 2.828$。

2. 從後往前推，計算每一級的輸入電容(電晶體W)值 $\hat{f} = gh = g\frac{C_{\text{out}}}{C_{\text{in}}} \Rightarrow (C_{\text{in}})_i = \frac{g_i(C_{\text{out}})_i}{\hat{f}}, C \propto W$。

$$W_{in} = \frac{\frac{3}{2}(120 \cdot 90\ \text{nm})}{2.828} = 5728\ \text{nm}$$

$$(W_{in})' = \frac{\frac{16}{9}(3818\ \text{nm})}{2.828} = 2700\ \text{nm}$$

第二級NOR2

	PMOS : $W = 5728 \cdot \frac{8}{9} = 5092 \approx 5090nm$ NMOS : $W = 5728 \cdot \frac{1}{9} = 636 \approx 640nm$
第一級NAND3	
	PMOS : $W = 2700 \cdot \frac{1}{4} = 675 \approx 680nm$ NMOS : $W = 2700nm$ (dynamic gate的C_{in}全給NMOS)

- 2B - simulation of different gate

Simulate each gate you designed in Exercise 2A. The output loading in your simulation should place a 80λ/40λ inverter. And the output of the output inverter should place another 240λ/120λ inverter which output is a floating node. The reason of placing two consecutive inverter (load and load of load) is to simulate the real scenario in a VLSI circuit by taking Miller's effect and loading into account. Design your input pattern to get the **average delay** for static CMOS and pseudo-NMOS family and the **rising delay** for the domino family. Logical effort is only an approximation. **Tweak the transistor sizes** to **improve the delay**. How much improvement can you obtain? Paste your input and output waveforms and show the delays. The rising/falling duration of each input signal is 100ps as Figure. 6.

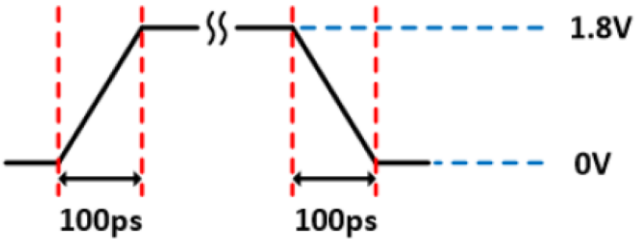
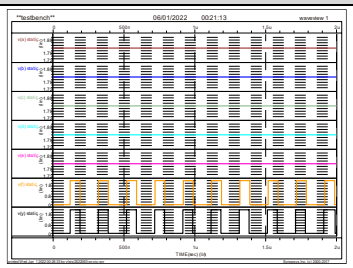
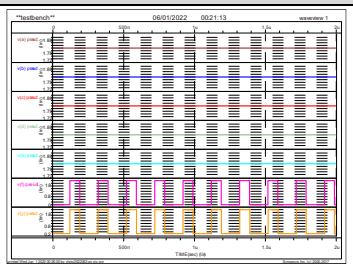
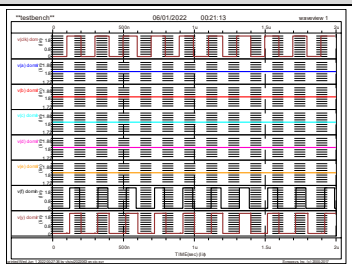
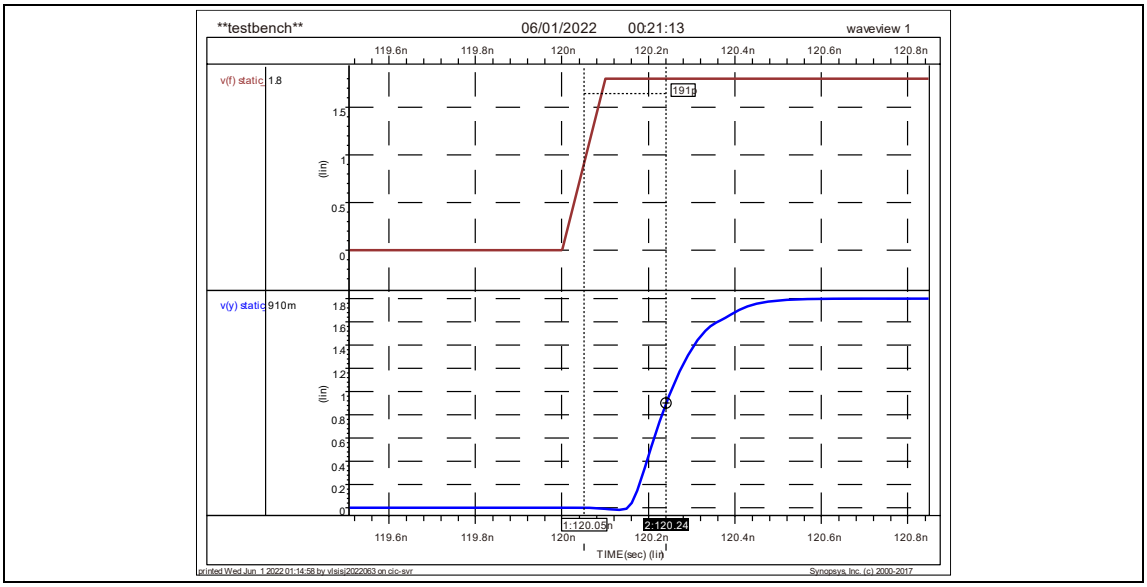


Fig. 1 input signal waveform

A.波型

static CMOS	pseudo-nmos	domino
		
static CMOS量測輸入0.9V到輸出0.9V的時間差 $t_{\text{rising delay}}$示意圖，實際量測還是使用.MEAS語法直接將量測數據輸出至.mt0檔，比起cursor量的還準確。		



B. 模擬結果

circuit family	tweak	delay average / rising delay for domino
static CMOS	before	1.867e-10
	after	1.634e-10
pseudo NMOS	before	1.360e-10
	after	1.341e-10
domino	before	1.114e-10
	after	1.069e-10

在電晶體調整前HSPICE模擬出的delay time結果有符合2A小題計算趨勢 - delay time : static CMOS(11.67) > pseudo-nmos(10.36) > domino(8.99)。

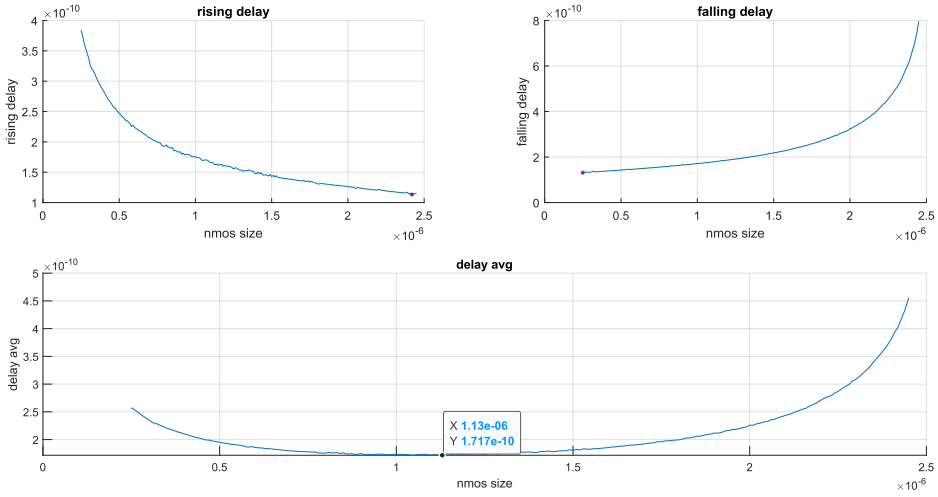
circuit family	transistor	before	after
static CMOS	stage1 PMOS	1080n	1570n
	stage1 NMOS	1620n	1130n
	stage2 PMOS	4320n	3530n
	stage2 NMOS	1080n	1650n
pseudo NMOS	stage1 PMOS	680n	680n
	stage1 NMOS	2700n	2700n
	stage2 PMOS	1910n	2170n
	stage2 NMOS	3820n	4320n
domino	stage1 PMOS	680n	680n
	stage1 NMOS	2700n	2700n
	stage2 PMOS	5090n	8000n
	stage2 NMOS	640n	1000n

C. 個人的優化方式

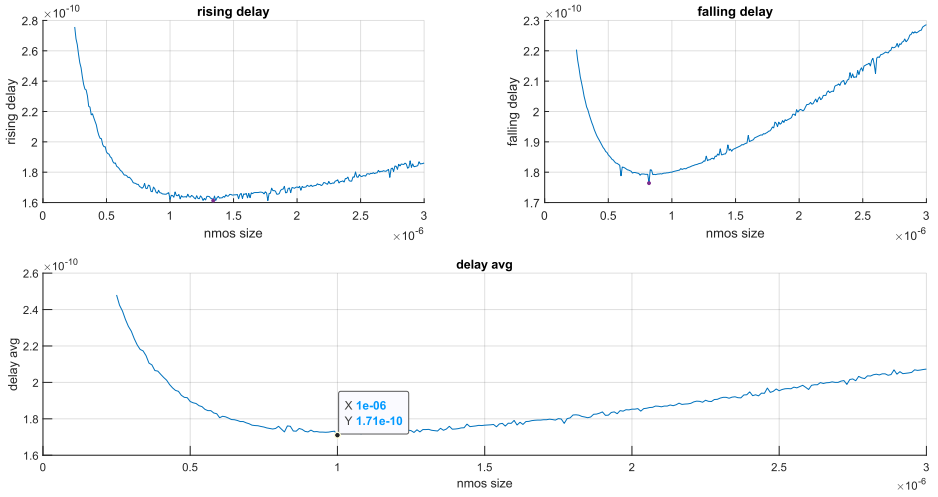
題目要求要調整電晶體改善delay time，但也沒有具體的SPEC，詢問出題助教後，助教表示本題也沒有一個標準答案，只需要注意有"第一級輸入電容在30λ以下"這個限制，附上一個優化前和優化後的表格，delay有比原本的小即可，有解釋一下自己是優化的方法會更好。

1. static CMOS我採取的優化方式

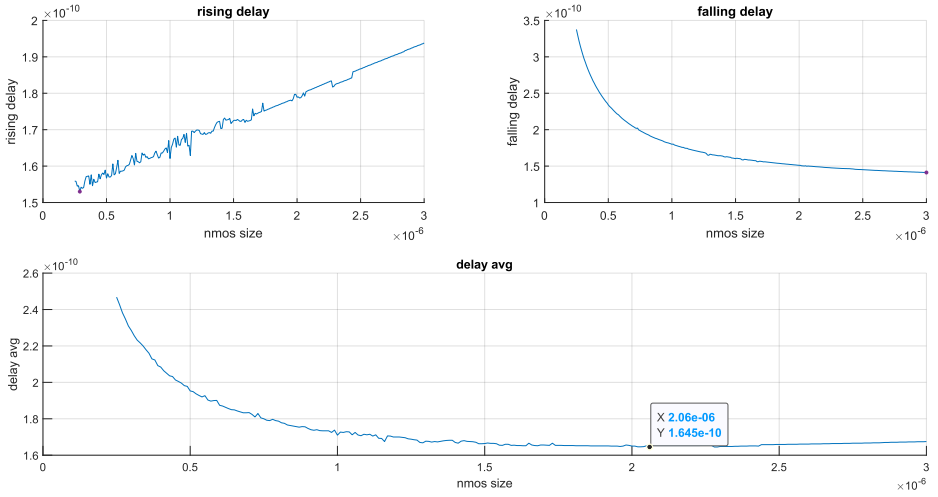
1. 由於題目要求第一級輸入電容最多是30λ，也就是PMOS加上NMOS固定在2700nm，所以掃NMOS `size`、PMOS `2700n - size`，得極值。



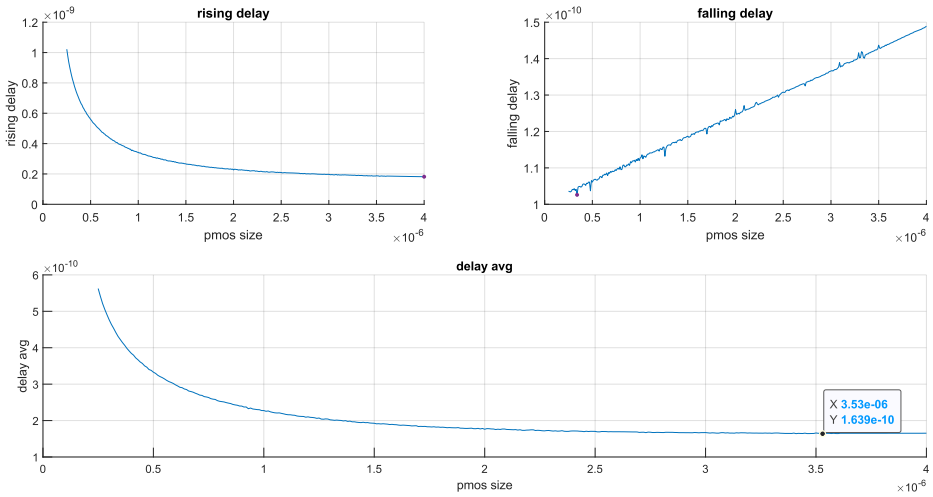
2. 第二級固定PN比例 掃NMOS `size`，PMOS `4*size`，得極值。



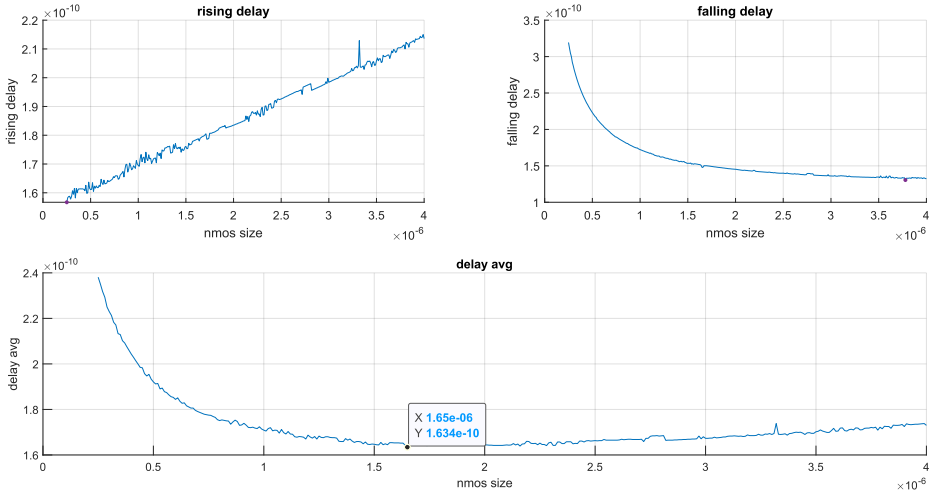
3. 第二級固定P，掃NMOS `size`，得N的極值。



4. 第二級固定N，掃PMOS `size`，得P的極值。

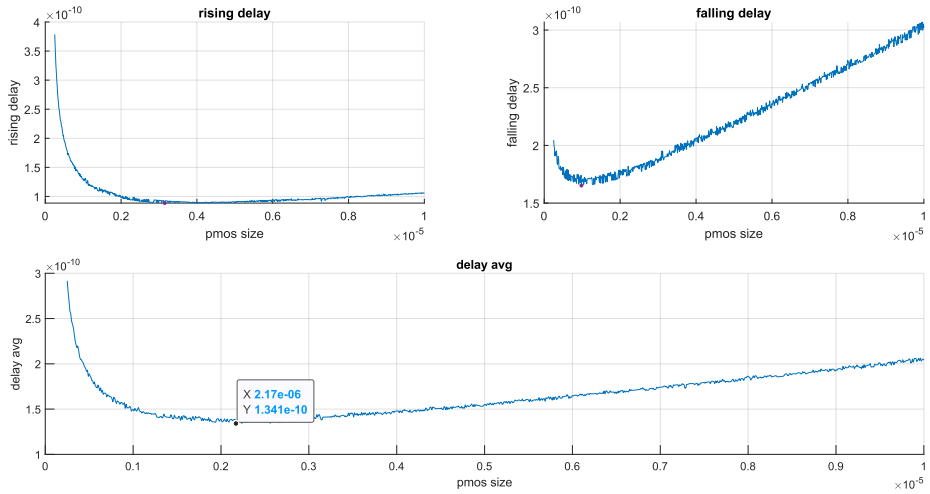


5. 第二級固定P，掃NMOS `size`，得N的極值。



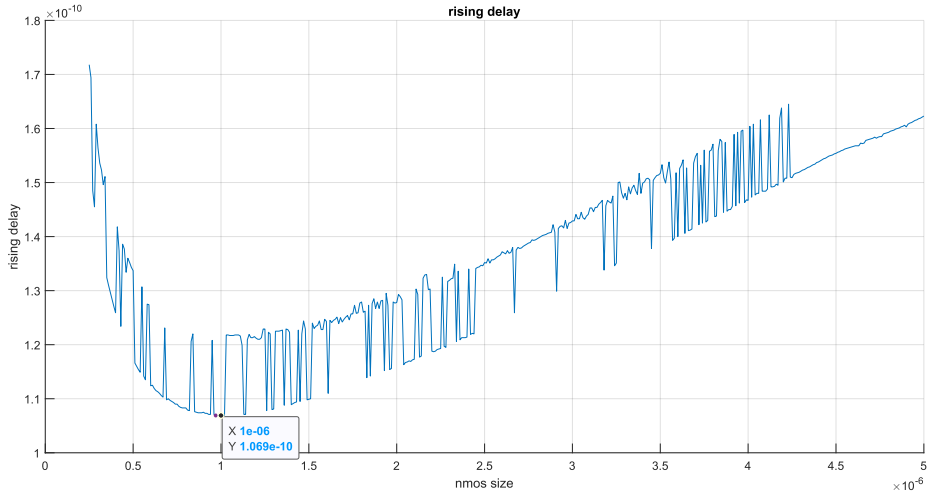
2. pseudo-nmos我採取的優化方式

如果只有第一級輸入電容在30λ以下"這個限制，**不固定PN比例，則找不到delay time(delay average)最小的極值，會是遞增或是遞減函數**，因此加上題目有限制"PMOS is $\frac{1}{4}$ strength of the pulldown stack"，但這是就個別每一個邏輯閘而言，因此真的要完成這個SPEC，要個別測量每一級邏輯閘的輸入與輸出節點數值，保持在 $\text{falling delay} = 3 \cdot \text{rising delay}$，實際實踐起來太麻煩，搞很久卻搞不出結果，也沒有任何實質上的意義，所以我改固定第二級的PN比例得極值。



3. domino我採取的優化方式

同前一題pseudo-nmos的優化方式，固定第二級的PN比例得極值。

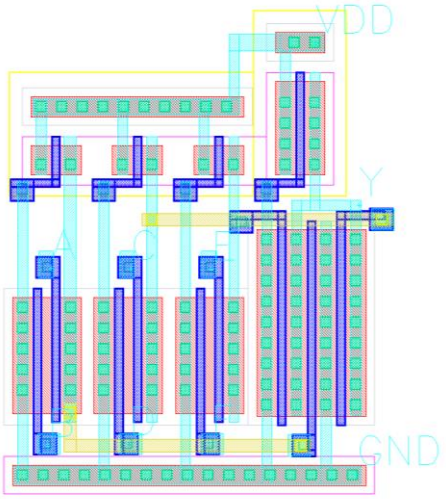


題目要求"improve the delay"，我覺得"最小化delay time"未必是最好的電路，就HI-skewed而言，可以把NMOS最小化使rising delay time提高，但缺點有2個，一是falling delay time變差、二是由於switching threshold voltage往右移，會讓noise margin變差，所以我們才會定一個skew factor為2。

- 2C - layout of pseudo-nmos logic

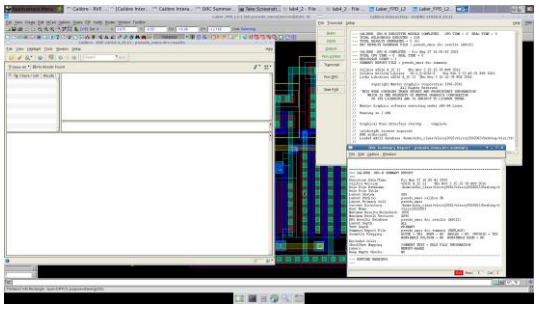
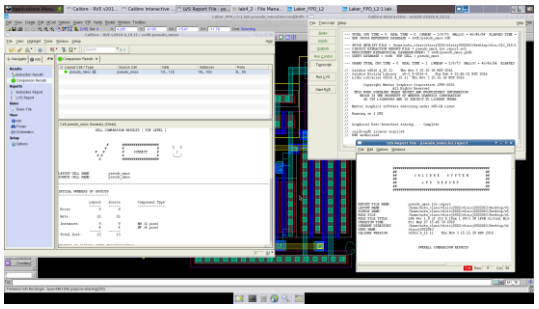
Create layout for **Pseudo-nmos logic (Student ID is odd)** or Domino logic (Student ID is even) with the sizes you tweaked in Exercise 2B. Paste layout pictures and show the “No Error Figure” of DRC/LVS verification. Compare the simulation result of post-layout to that of pre-layout.

layout



layout說明

不同於前三次作業static CMOS其中PMOS與NMOS具有對稱性，比較好layout，這次作業中pseudo-NMOS的PMOS只有一個並且是接到GND，因此我把PMOS的gate(ploy)拉出來接GND，再來**把A、C、E外接腳位，壓在GND、輸出節點兩個metal之間**，因此就可以極小化NAND gate之間的距離為0.3μm，即為diffusion之間的最小間距。

DRC	LVS
	

	rising delay	falling delay	delay average
presim	9.485e-11	1.734e-10	1.341e-10
postsim	9.591e-11	1.735e-10	1.347e-10

如上表rising delay與falling delay在presim與postsim模擬的差距微小。

● Conclusion

本次作業用到gate章節並結合之前speed章節的觀念。

A. 第一大題

觀念：

charge sharing noise起因是充飽電輸出電容會與未充飽電內部寄生電容"共享電荷"，導致輸入電壓下降，解決方法是讓輸入電容加大，或是使用secondary precharge，在一開始也把內部寄生電容也先precharge好。

解題:

1A小題不同input order情況下charge sharing noise理論計算。

1B小題charge sharing noise的HSPICE模擬。

1C小題解決charge sharing noise的方法 - 使用secondary precharge或是keeper。

B. 第二大題

觀念：

static CMOS的計算方式前一次作業已經熟悉，這次要會pseudo-NMOS、footed dynamic gate、HI skew static gate這3種方式的計算流程。

1. pseudo-NMOS

1. 電晶體size決定

- 為了使 ratioed circuit 能與 static CMOS 比較基準一致，設定 PMOS 製造$\frac{I}{3}$電流、NMOS 製造$\frac{4I}{3}$電流，對於 falling 時的淨(net)電流是$\frac{4I}{3}-\frac{I}{3}=I$，由於$I\cdot R=V_{DD}=$ const.，要使 NMOS 製造$\frac{4I}{3}$電流，NMOS 的 size 勢必要增大使電阻值降低，因此 size $k=\frac{4}{3}$。
- PMOS 的 size 要除以 4 倍，但由於 PMOS 的 mobility 比較低($\mu_n:\mu_p=2:1$)，所以再乘以 2 倍，因此 size $k=\frac{2}{3}$。

2. logic effort計算

- 看進去的輸入電容只有 NMOS 的$\frac{4}{3}$，由於前面假設 falling 時的淨(net)電流是$\frac{4I}{3}-\frac{I}{3}=I$，所以$\frac{4}{3}$只需要除以 unit inverter 的輸入電容作 normalize，得 falling(down)的 logic effort$g_d=\frac{4}{3}\cdot\frac{1}{3}=\frac{4}{9}$。
- 由於 rising 的電流是$\frac{I}{3}$比 falling 的電流I少 3 倍，因此上升的速度會慢 3 倍，logic effort 會變大 3 倍，得 rising(up)的 logic effort $g_u=g_d\cdot 3=\frac{4}{3}$。

2. footed dynamic gate

1. 電晶體size決定

由於CLK是對所有電路同時precharge，不需要在乎速度問題，所以為了降低寄生電容，PMOS電晶體的sizing會給最小；而pull-down電晶體的sizing則依照static CMOS的方式，使下方路徑維持在一個R。

2. logic effort計算

只需要計算falling時的logic effort g_d，因為precharge階段把會先把輸出充至V_{DD}，而evaluate階段輸出電壓只有下降(falling)或是不下降兩種可能而已。

3. HI skew static gate

1. 電晶體size決定

選擇要favor rising變成HI-skew或是favor falling變成LO-skew，根據skew factor，一般設定為2倍，將不favor的path中電晶體的size縮小2倍，如此從輸入和輸出看進去的電容都會變小，對favor的路徑速度變快，但同時對不favor的path，由於電晶體的size縮小等效電阻增加，所以對不favor的路徑速度變慢。

2. logic effort計算

在rising(up)的logic effort g_u維持**等效電路上相同的rise電阻**，調整inverter的電晶體至unskewed狀態，計算兩者比例$g_u=\frac{g_{\text{HI-skew}}}{g_{\text{unskewed inverter}}}$；在falling(down)的logic effort g_d維持**等效電路上相同的falling電阻**，調整inverter的電晶體至unskewed狀態，計算兩者比例$g_u=\frac{g_{\text{HI-skew}}}{g_{\text{unskewed inverter}}}$。

解題:

2A小題計算static CMOS, pseudo-nmos, domino不同電路種類與NAND6 and INV, NAND3 and NOR2, NAND3 and NOR2, INV and NOR6不同邏輯閘之間，最佳path

delay與決定電晶體size。
2B小題模擬2A小題電路，並透過不同策略去優化delay time。
2C小題完成pseudo-nmos NAND3 and NOR2的layout，萃取出寄生電容(R+C+CC)，並做HSPICE的postsim模擬。