National Cheng Kung University

Department of Electrical Engineering

VLSI Circuits Design

Soon-Jyh Chang **Homework #4**

Due Wednesday, June 1, 9 am

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In this homework, please use 'cic018.l', TT corner, VDD = 1.8V to do every simulation.

Problem 1 - Dynamic gate

1A Please Design a 4-input footed dynamic gate which has the function as follow:

$$X_{out} = \overline{A \cdot (B + C) \cdot D}$$

Draw the schematic and stick diagram you designed (label the I/O port and transistor size), and Derive the worst charge-sharing noise as a fraction of VDD and **h** (electrical effort). Finally, plot the graph of charge-sharing noise versus different electrical effort **h** from 1 to **7**. You can use any tool to plot the graph, such as Excel or Matlab.

Assume that:

1. PMOS/NMOS mobility ratio = 0.5,
2. electrical effort = h,
3. diffusion capacitance on uncontacted nodes is about half of gate capacitance and on contacted nodes it equals gate capacitance.

Hint: You should consider the **Input Order** of your design. For the different input order, the **layout of circuit will different**, and the **parasitic capacitance of intermediate nodes will also be different**. Choose the **best** input order (the smallest charge sharing noise) as your design.

1B Please Simulate the 4-input footed dynamic gate that you have designed in 1A. You should design the input pattern which causing the worst charge sharing noise at output(Xout). Please write testbench(.sp) by yourself, and Paste the pre-simulation waveform and label the amplitude of charge sharing noise.

- MOS unit size (W/L) = (0.5um/0.18um),
- Output load a **unit-size** inverter (inverter output is floating),
- Input pattern pulses have rising/falling duration = **100ps** (from 0 to VDD),
- The amplitude of charge sharing noise = VDD – V_Y (Xout = 1)

1C From above question 1B, please revise the circuit to deal with the charge sharing issue. Do pre-simulation (the testbench in 1C and 1B should be the same), and plot waveform to verify that the output is free from charge sharing noise, and finally explain your approach.

- In worst case, the amplitude of charge sharing noise should be smaller than 0.1V.

Problem 2 – Gate Comparison

Design a fast 6-input AND gate in each of the following circuit families.

1) Static CMOS
2) Pseudo-nMOS with pMOS transistors **1/4** the strength of the pulldown stack
3) Domino (a footed dynamic gate followed by a **HI-skew** static gate);
   only optimize the delay from rising input to rising output.

2A **Sketch** an implementation using two stages of logic (e.g., AND6+INV, NAND3 + NOR2, etc.). **Label** each gate with the width of the pMOS and nMOS transistors. Each input can drive no more than 30 λ of transistor width. The output must drive a 80λ/40λ inverter (i.e., an inverter with a 80 λ wide pMOS and 40 λ wide nMOS transistor). Use logical effort to choose the topology and size for least average delay. Estimate the delay using logical effort and show the calculation process. When estimating parasitic delays, count only the diffusion capacitance on the output node. (λ=180nm/2=90nm)

2B **Simulate** each gate you designed in Exercise 2A. The output loading in your simulation should place a 80λ/40λ inverter. And the output of the output inverter should place another 240λ/120λ inverter which output is a floating node. The reason of placing two consecutive inverter (load and load of load) is to simulate the real scenario in a VLSI circuit by taking Miller's effect and loading into account. **Design your input pattern** to **get the average delay** for static CMOS and pseudo-NMOS family and the **rising delay** for the domino family. Logical effort is only an approximation. **Tweak the transistor sizes** to improve the delay. How much improvement can you obtain? Paste your input and output waveforms and show the delays.

- The **rising/falling** duration of each input signal is **100ps** as Figure. 6.

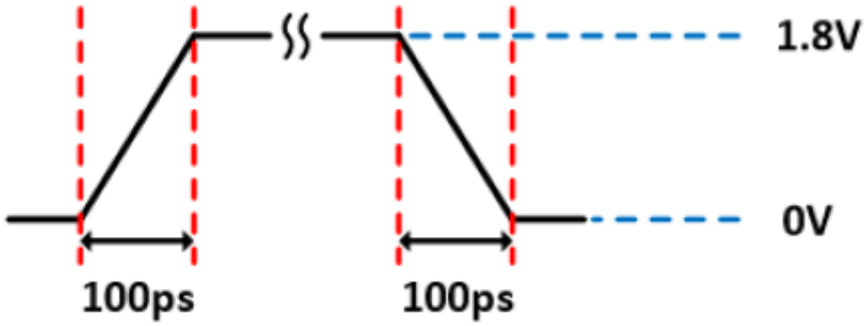


Fig. 1 input signal waveform

2C Create layout for **Pseudo-nmos logic (Student ID is odd) or Domino logic (Student ID is even)** with the sizes you **tweaked** in Exercise 2B. Paste **layout pictures** and show the "No Error Figure" of **DRC/LVS** verification. Compare the simulation result of post-layout to that of pre-layout.

The files you should upload in Problem 2 are :

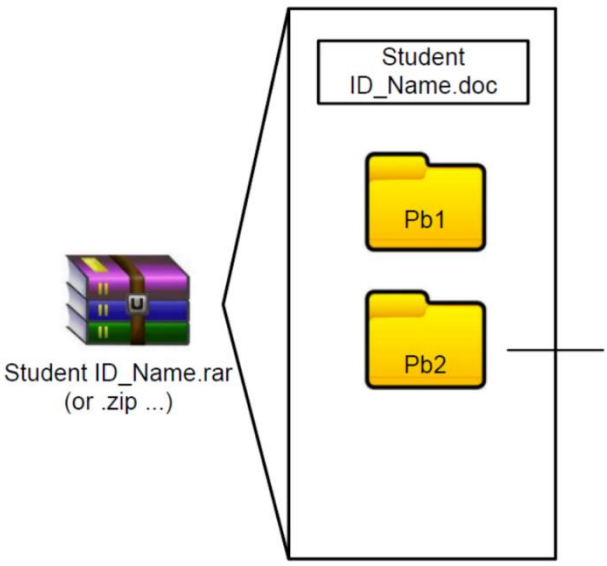
(a) AND6_static.cir, AND6_static.sp,

(b) AND6_pseudo.cir, AND6__pseudo.sp, AND6_pseudo.gds (odd),

(c) AND6_domino.cir, AND6_domino.sp, AND6_domino.gds (even).

Important Note

1. It is needless to print your report. Please compress the needed files and report shown as below. Then upload your compressed file to moodle website.
2. 12pt character size in your report.
3. **Change the background color of all your figures, schematic, layout, and waveforms, to write.**
4. **DO NOT COPY**
5. No late homework will be accepted. When it is due, it is due.



Problem 1:
Pb1_B.cir,
Pb1_C.cir,
Pb1.sp

Problem 2:
AND6_static.cir,
AND6_static.sp,
AND6_pseudo.cir,
AND6_pseudo.sp,
AND6_ pseudo.gds (odd),
AND6_domino.cir,
AND6_domino.sp,
AND6_domino.gds (even).
__.drc.summary
__.lvs.report
__.pex.netlist
__.pex.netlist.__.pxi
__.pex.netlist.pex