

IC Layout Tools

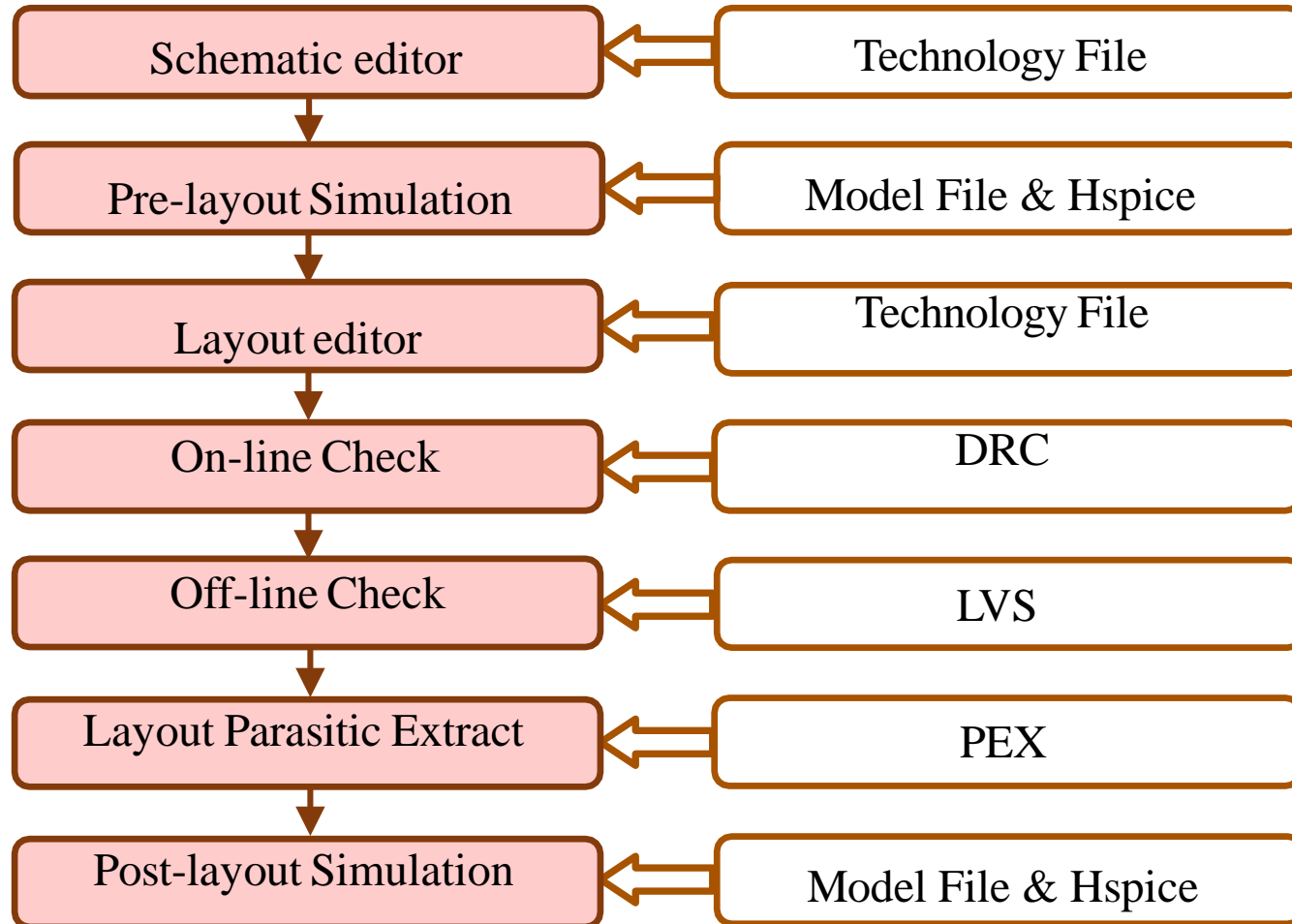
Laker & Calibre



Presenter：許哲維、邱薪育



Full-Custom Design Flow



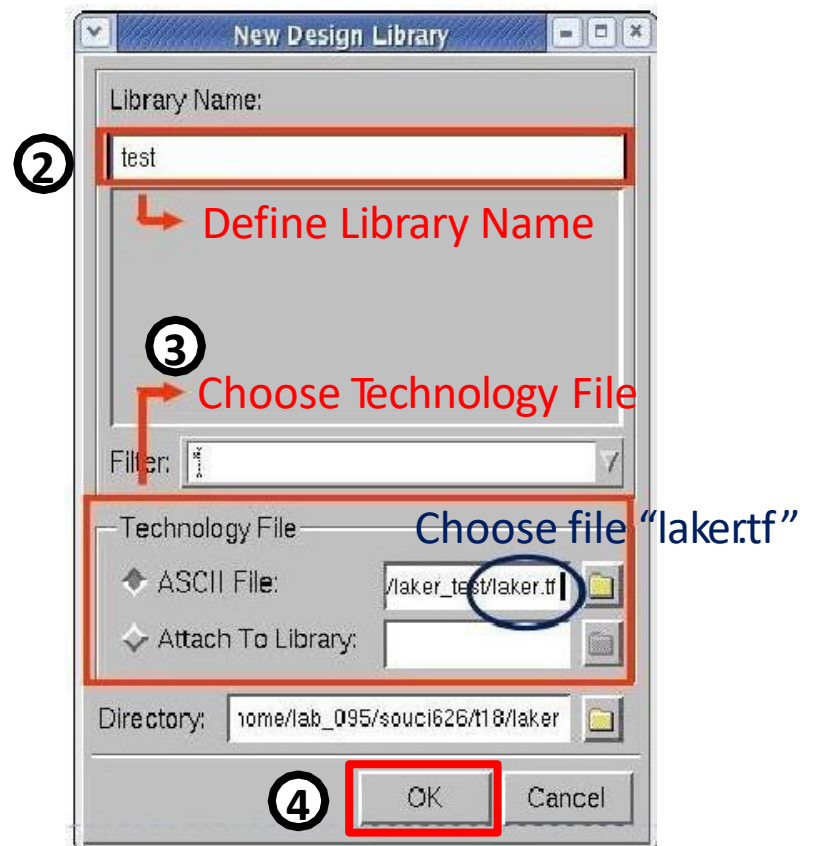
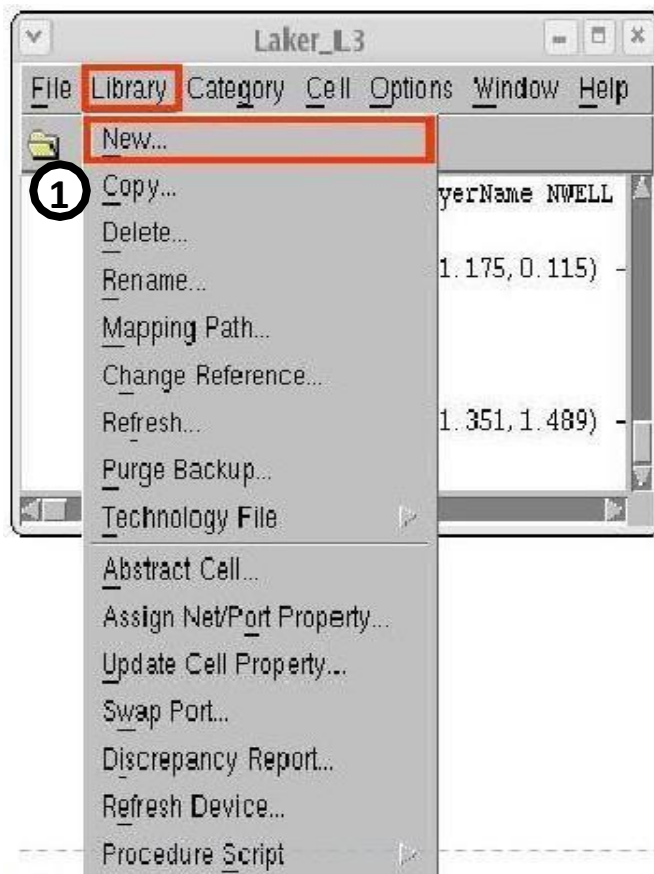
How to Start Laker?

You need these files:

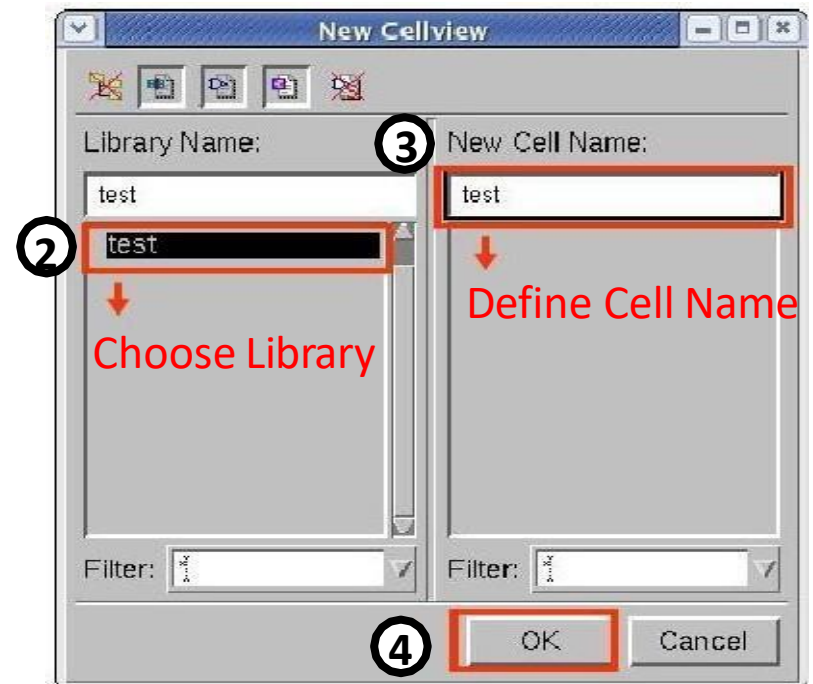
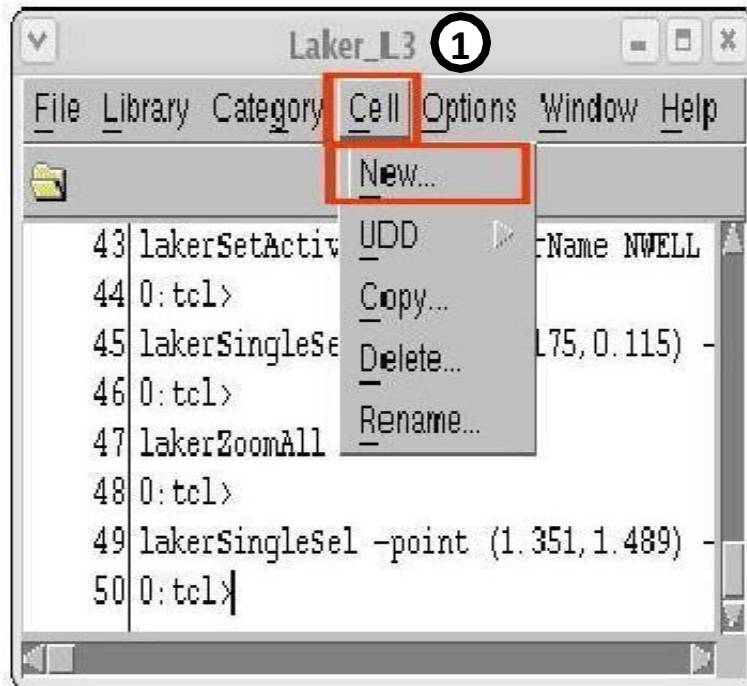
laker.tf	Laker technology file
rule.drc	DRC (<i>Design Rule Check</i>) to verify that the layout satisfies design rules.
rule.lvs	LVS (<i>Layout Versus Schematic</i>) to check that circuit in a layout are connected in the same way as in the schematic.
rule.rce rule_08KA.rc rule_20KA.rc	PEX (<i>Parasitic Extraction</i>) to extract the parasitic effects resulted from the interconnection of layout design.

Laker – Create New Library

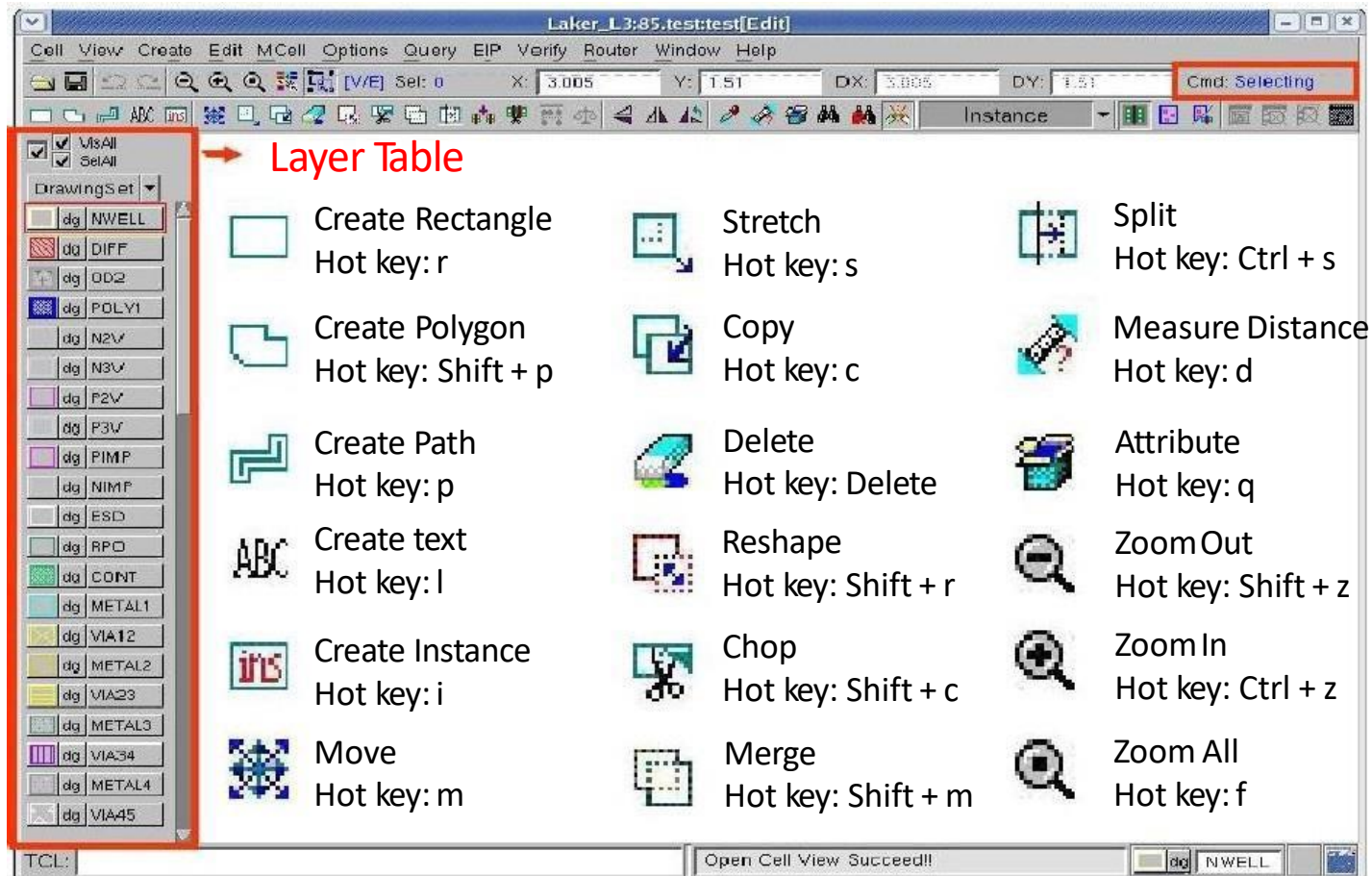
- Terminal enter “laker&”



Laker – Create New Cell



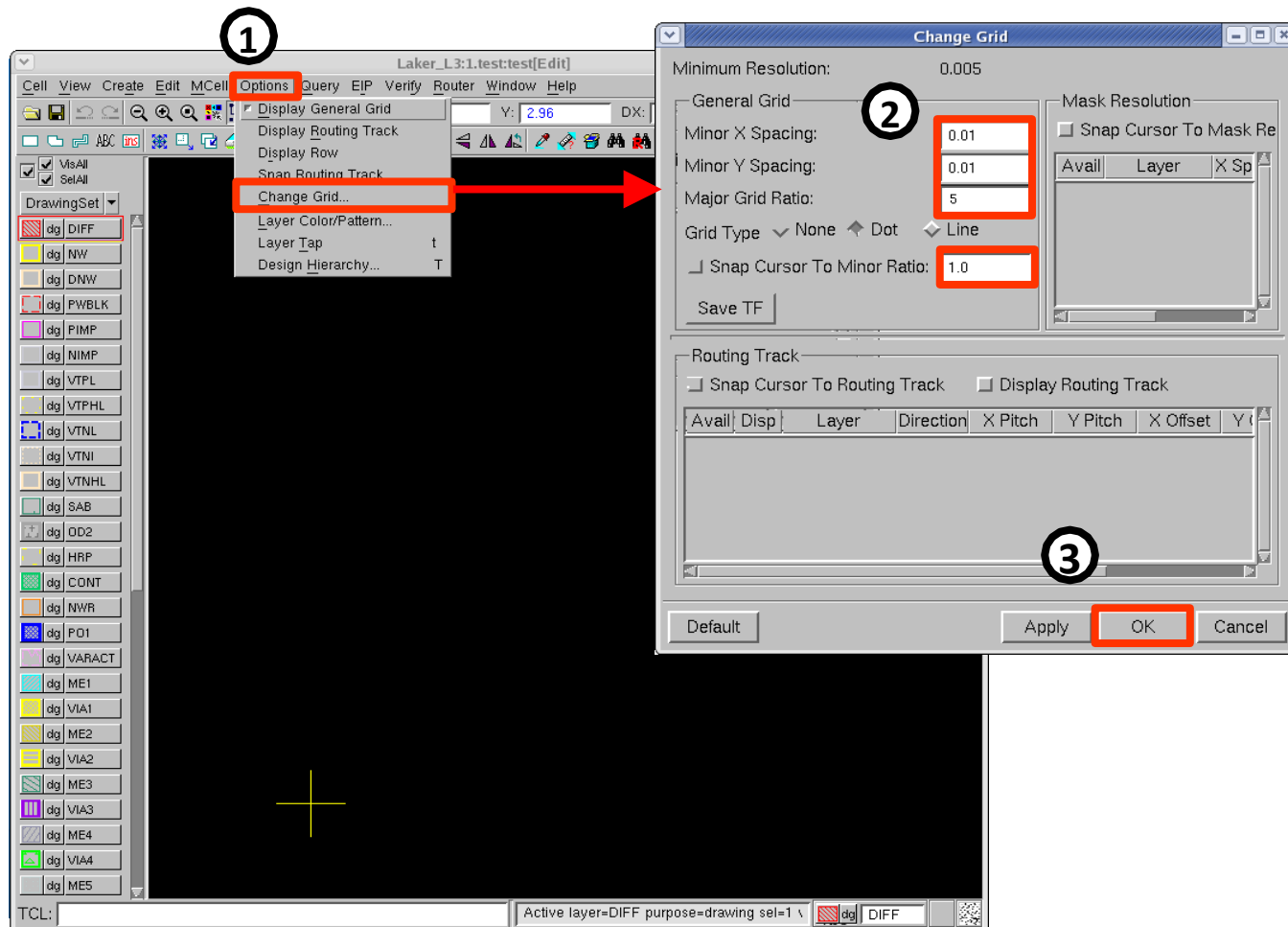
Laker – Tool Interface



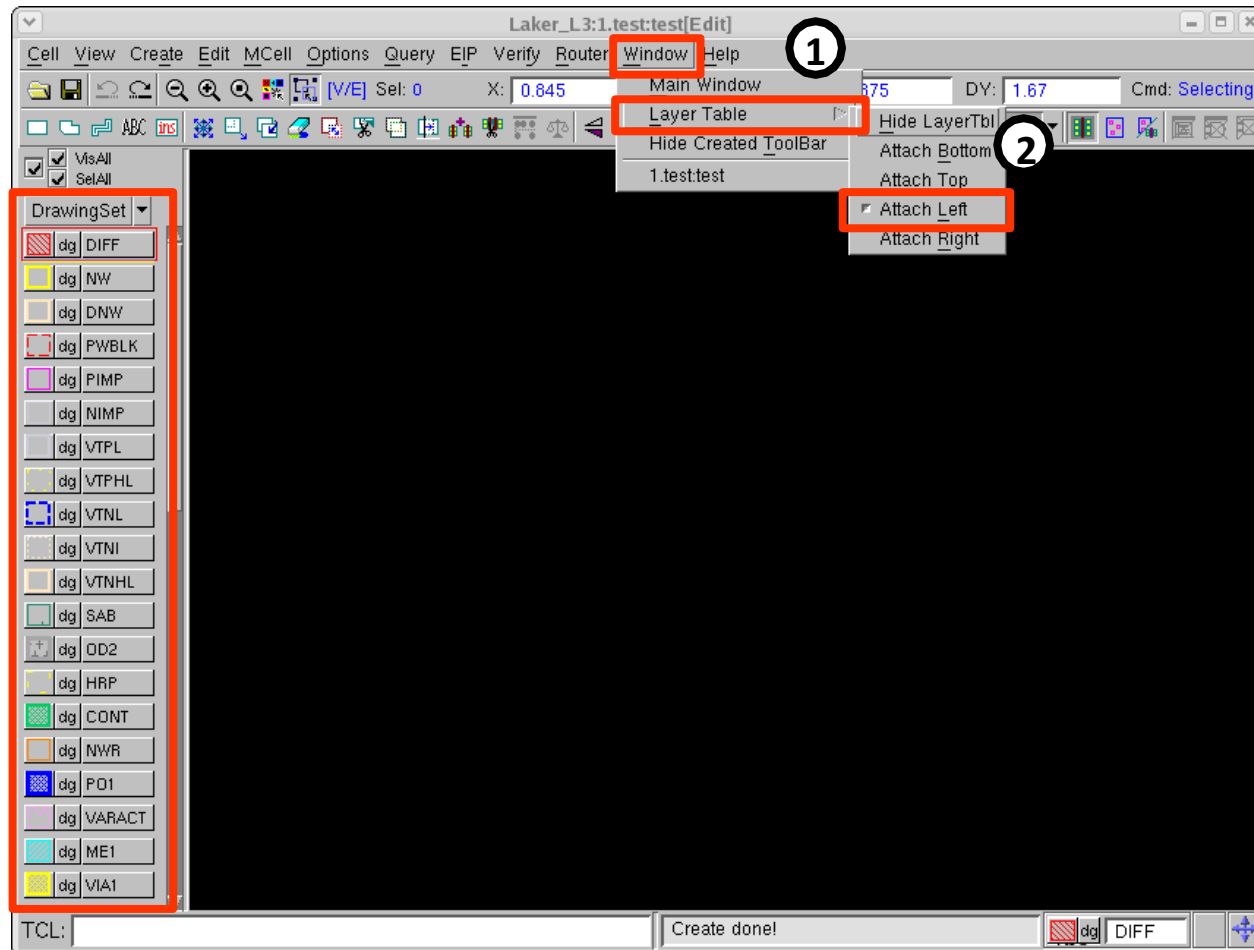
Laker – Hot Keys

Hot Key	Function	Hot Key	Function
k	Tag ruler	Ctrl + z	Zoom in
Shift + k	Clear ruler	Shift + z	Zoom out
r	Create rectangle	Ctrl + a	Select all objects
d	Measure distance	Shift + r	Reshape selected object(s)
q	Show object attribute	F8	Clear Highlight
s	Stretch selected object(s)	i	Create Instance
c	Copy selected object(s)	u	Undo last action
m	Move selected object(s)	Shift + u	Redo last action
delete	Delete selected object(s)		
a	Align selected objects(s)		
f	Zoom all		

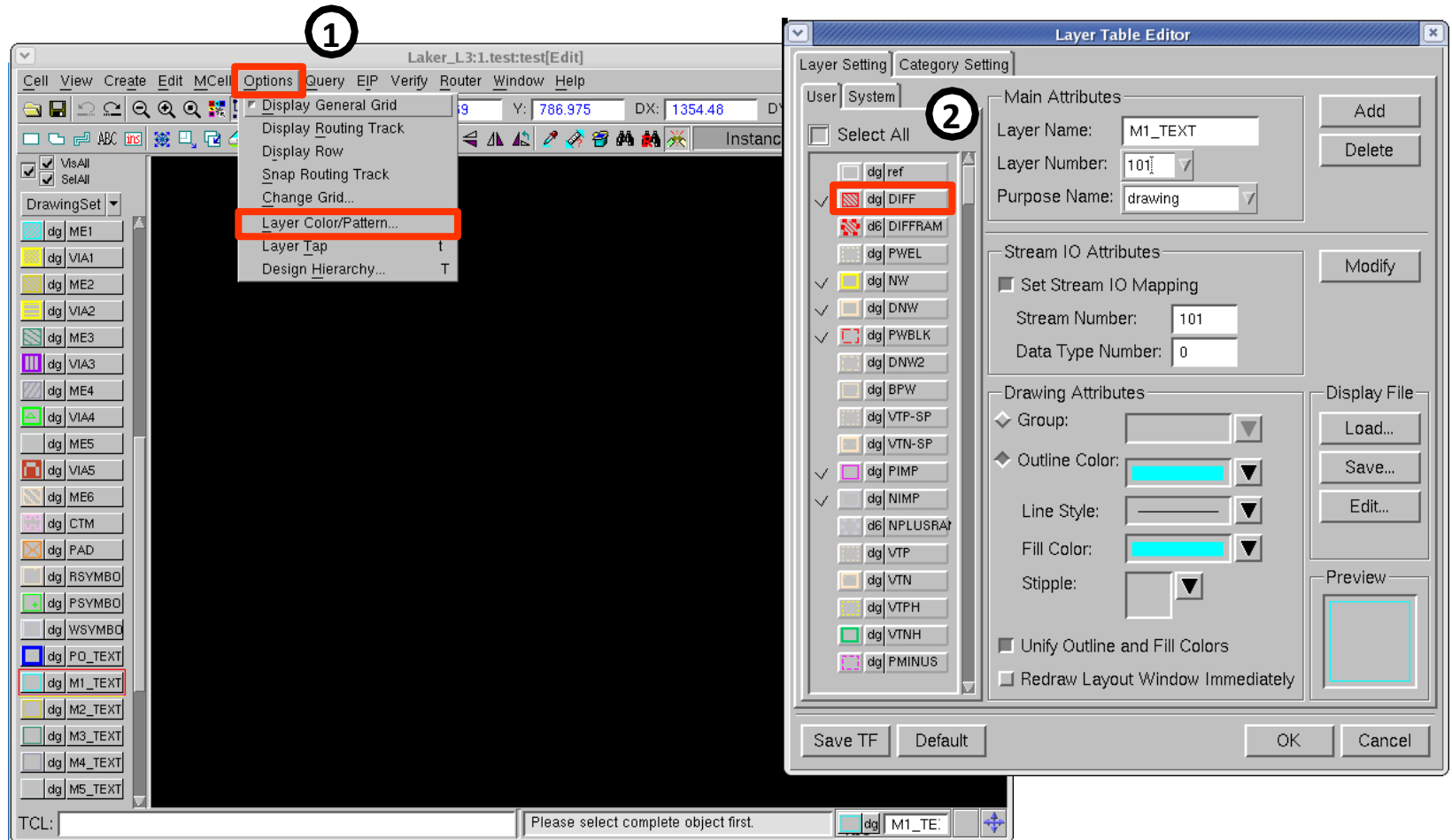
Laker – Basic Setting : Change Grid



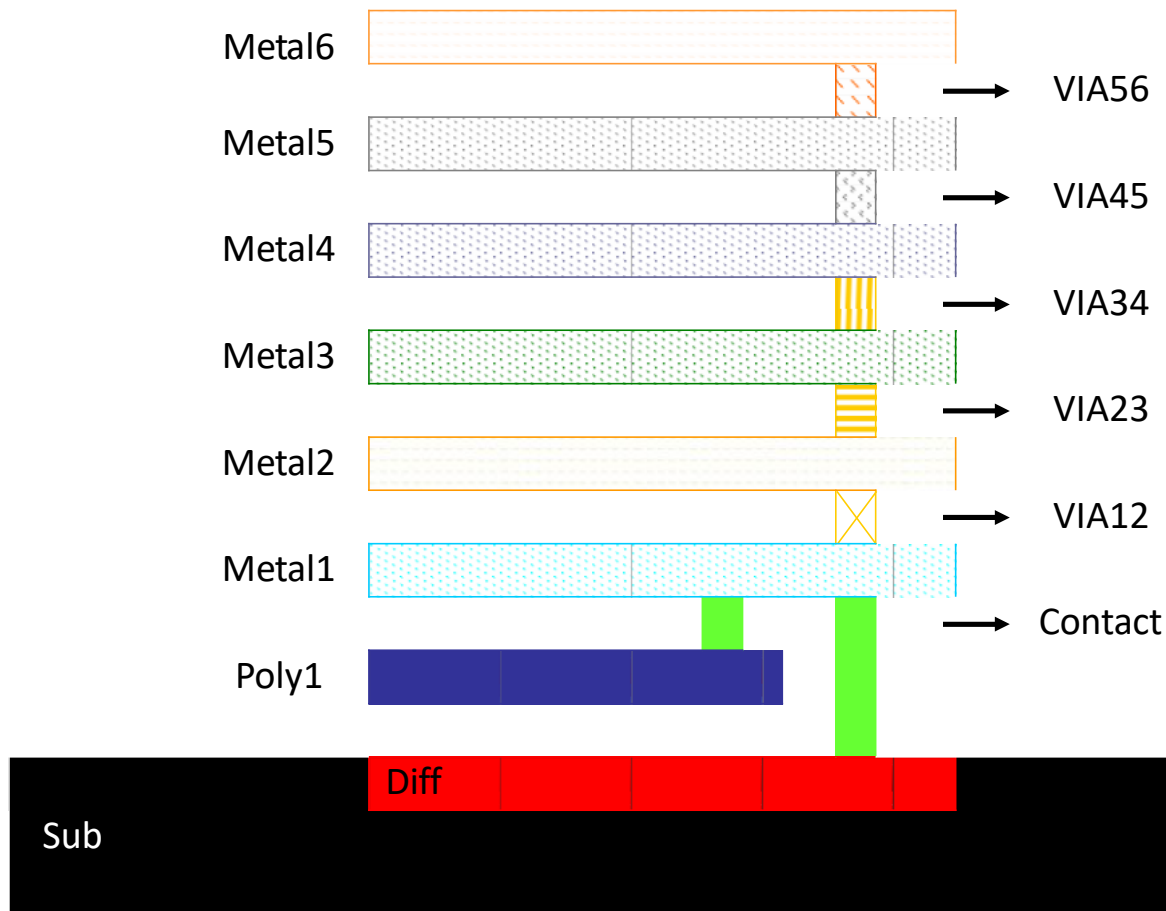
Laker – Basic Setting : Layer Table



Laker – Basic Setting : Layer Table Editor

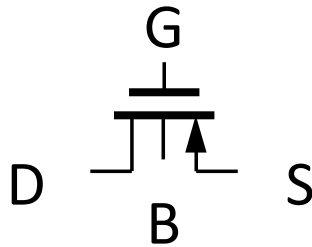


Laker – Layer Level

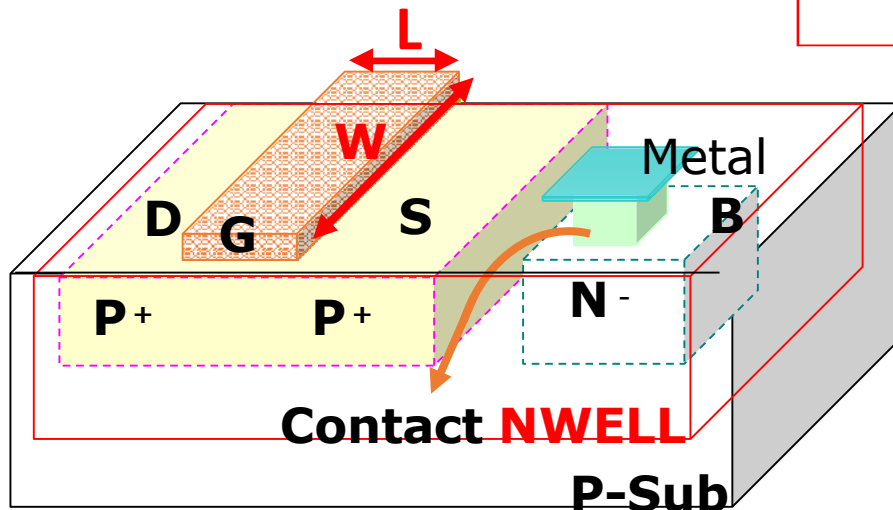


Laker – Example : PMOS

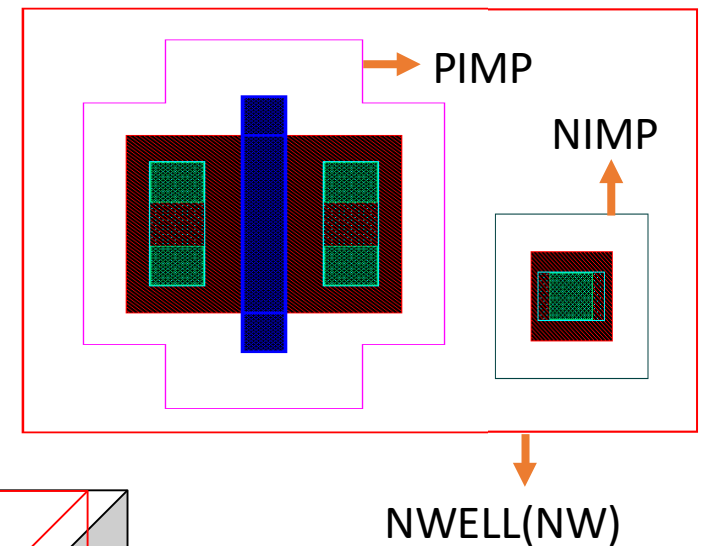
Symbol



Process Section

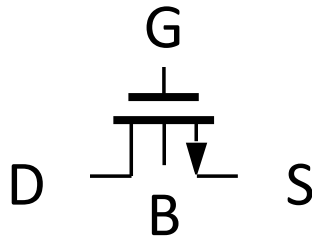


Layout View

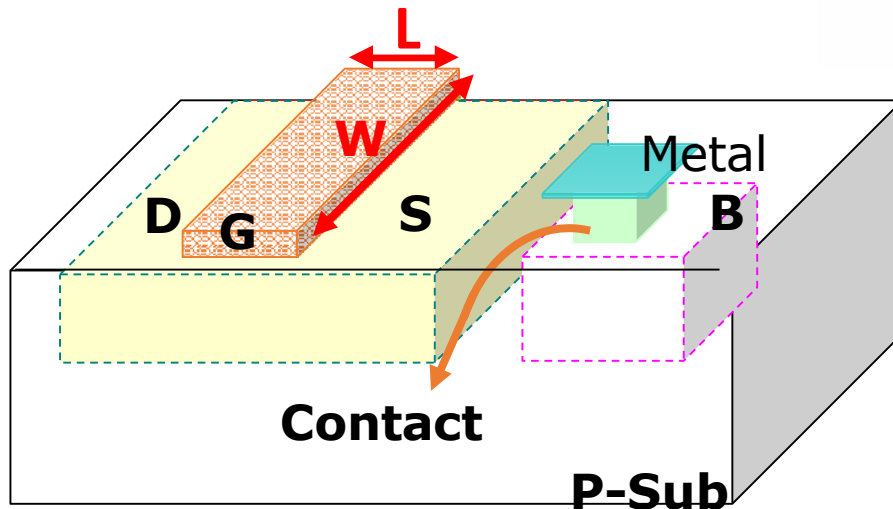


Laker – Example : NMOS

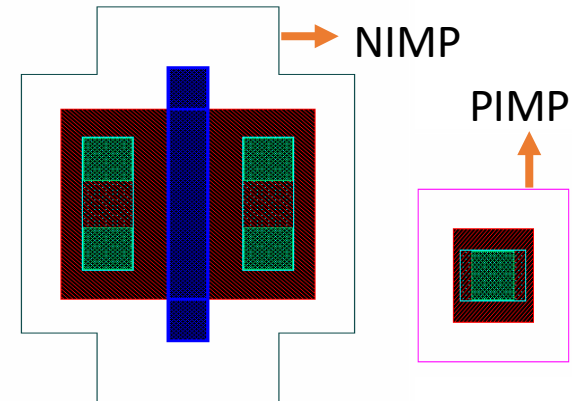
Symbol



Process Section



Layout View

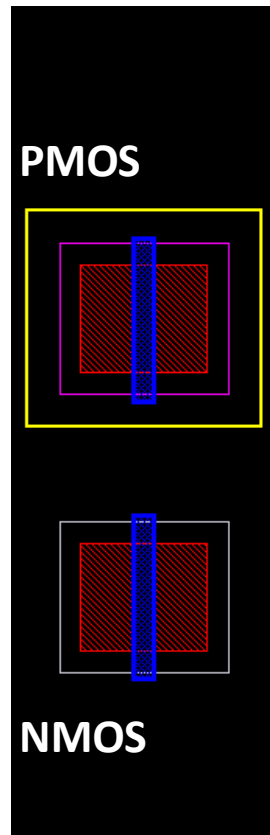


Laker – Example : Inverter

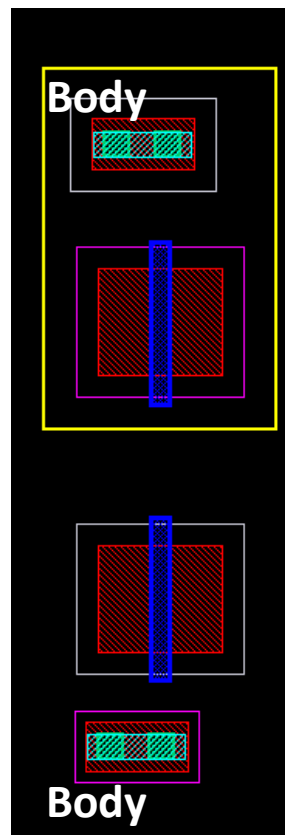
Term	Explanation
W	Width
L	Length
DIFF	Diffusion (Drain/Source)
PO1	Poly silicon (Gate)
PIMP	P implantation
NIMP	N implantation
NW	N WELL

$$\left(\frac{W}{L}\right)_P = \left(\frac{1\mu m}{0.18\mu m}\right), \left(\frac{W}{L}\right)_N = \left(\frac{0.5\mu m}{0.18\mu m}\right)$$

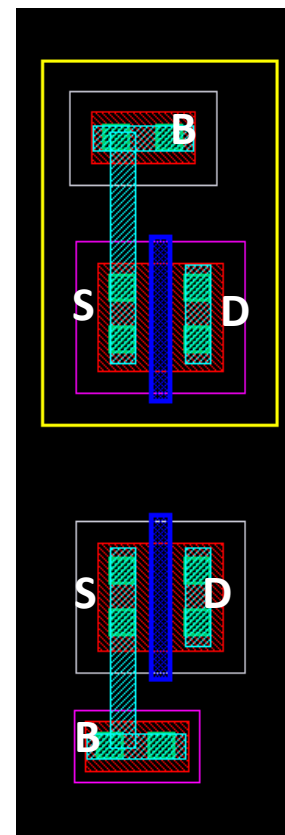
Laker – Example : Inverter



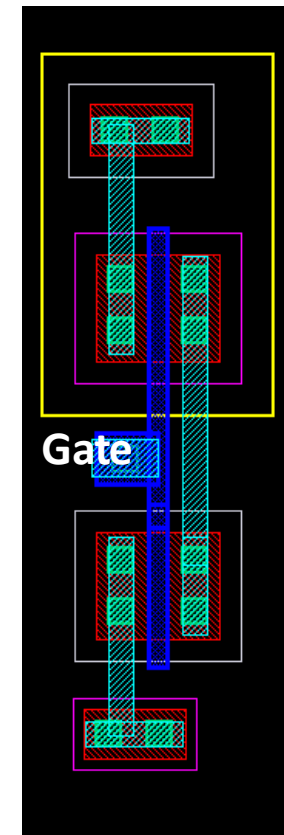
Create a PMOS
& an NMOS



Add Body



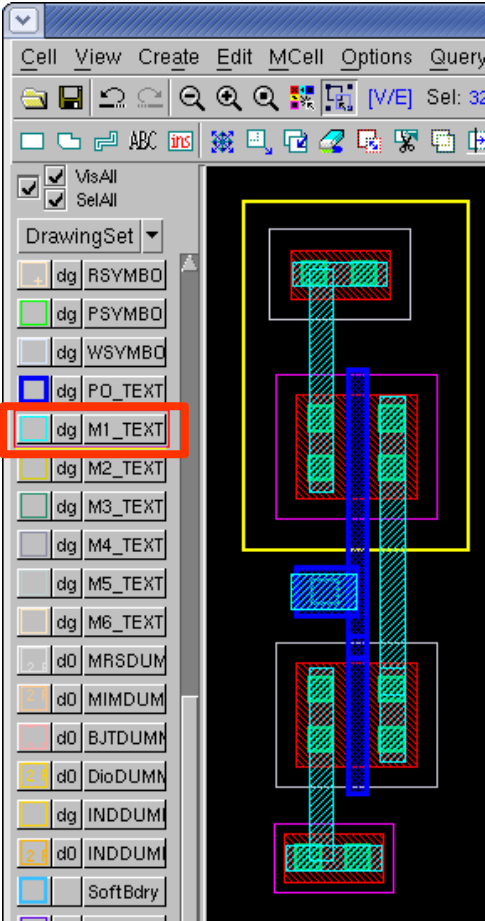
Use Metal1 and
Contacts to
connect source
and body



Connect Gate
and Drain

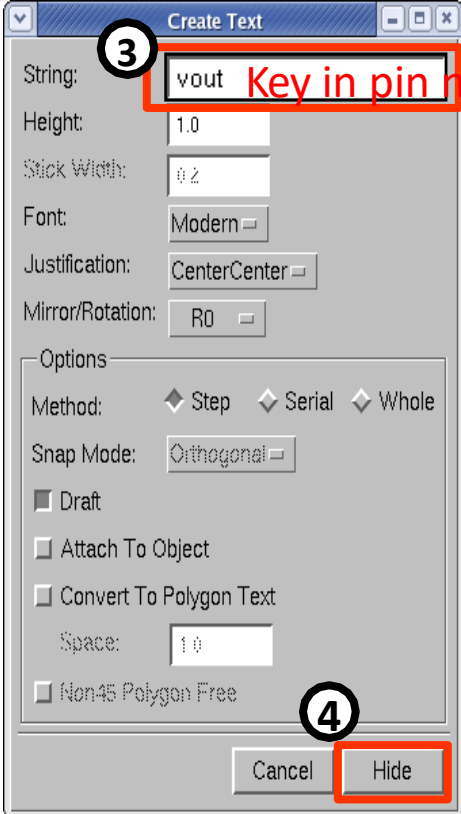
Laker – Example : Add Pin Name

①

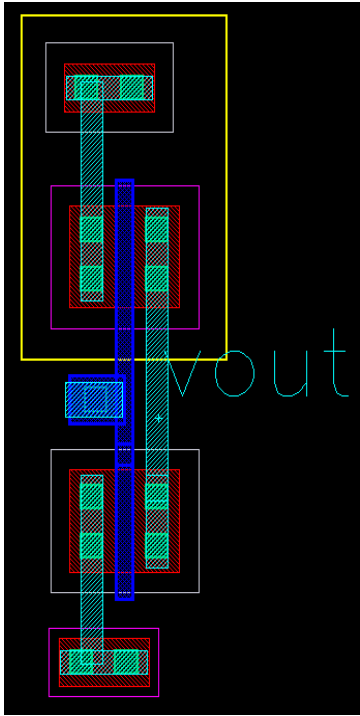


② ABC Create text
Hot key: *ℓ*

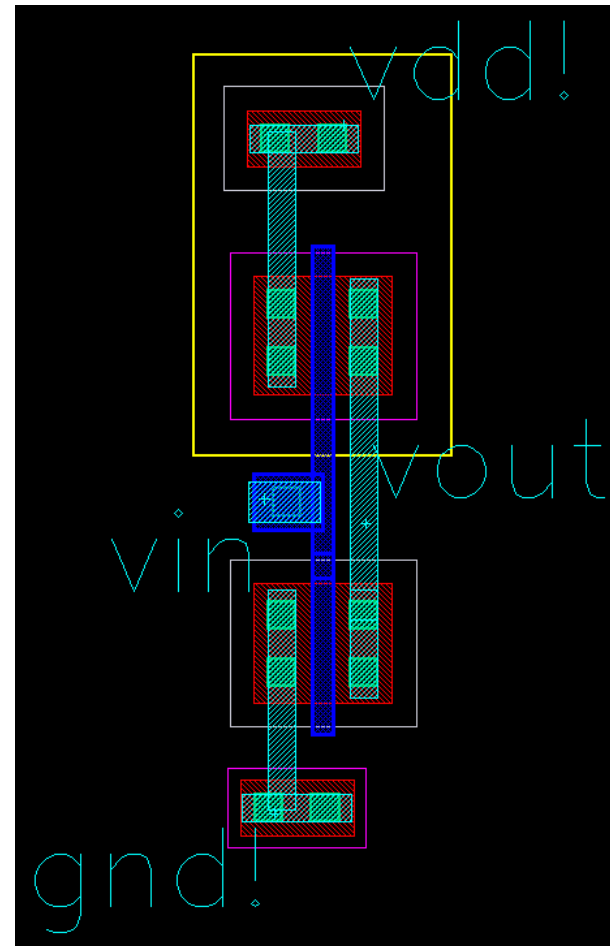
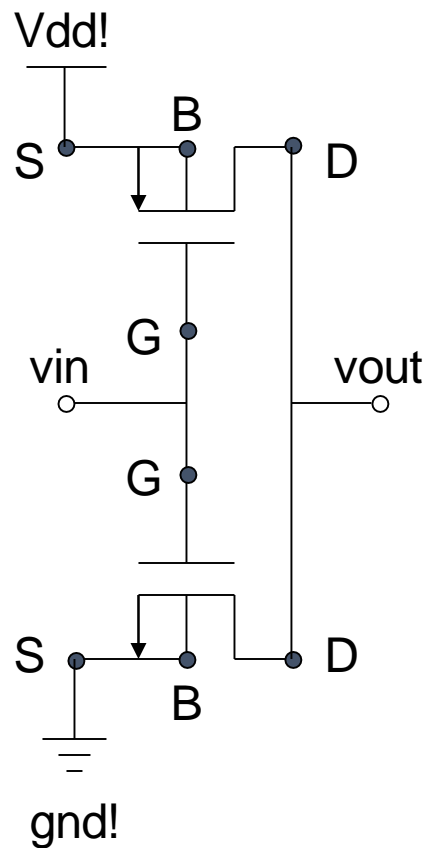
③ vout Key in pin name



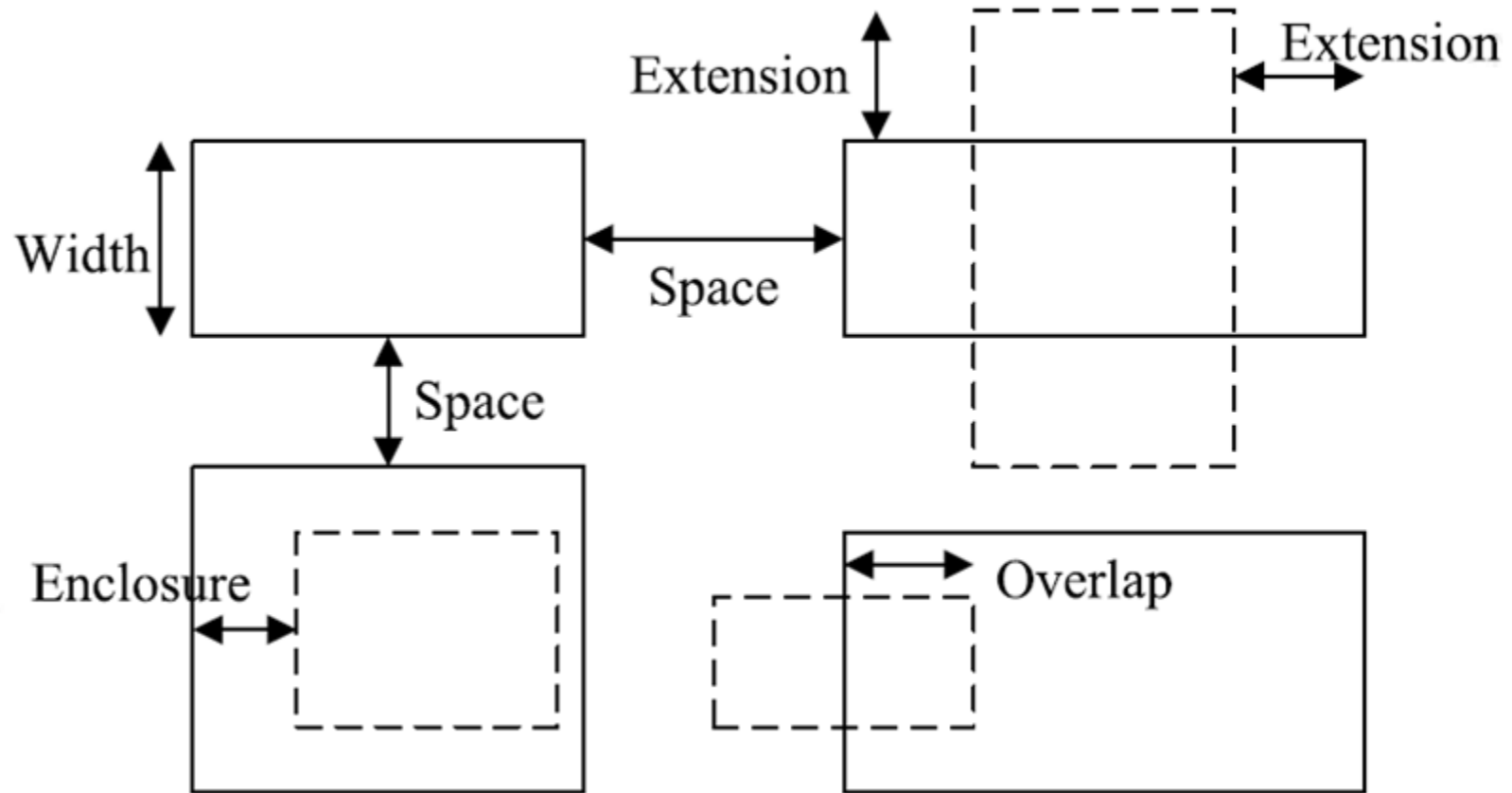
④



Laker – Example : Inverter



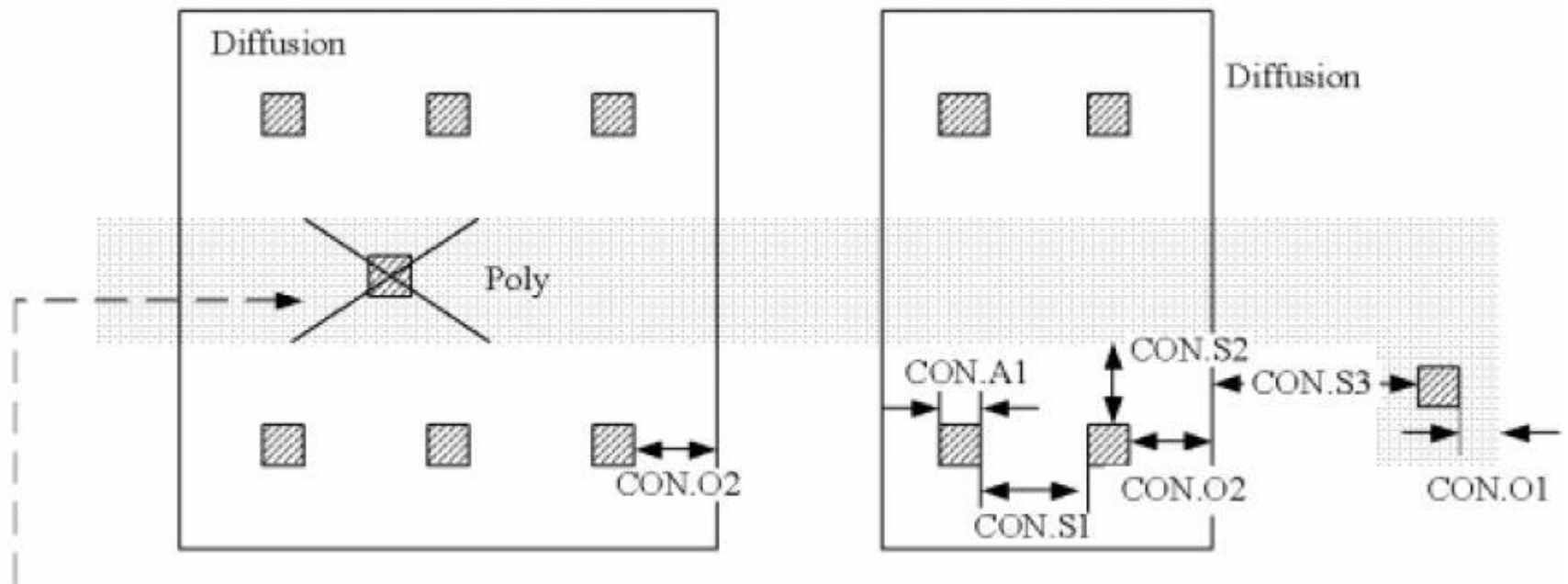
Design Rule (1/4)



Design Rule (2/4)

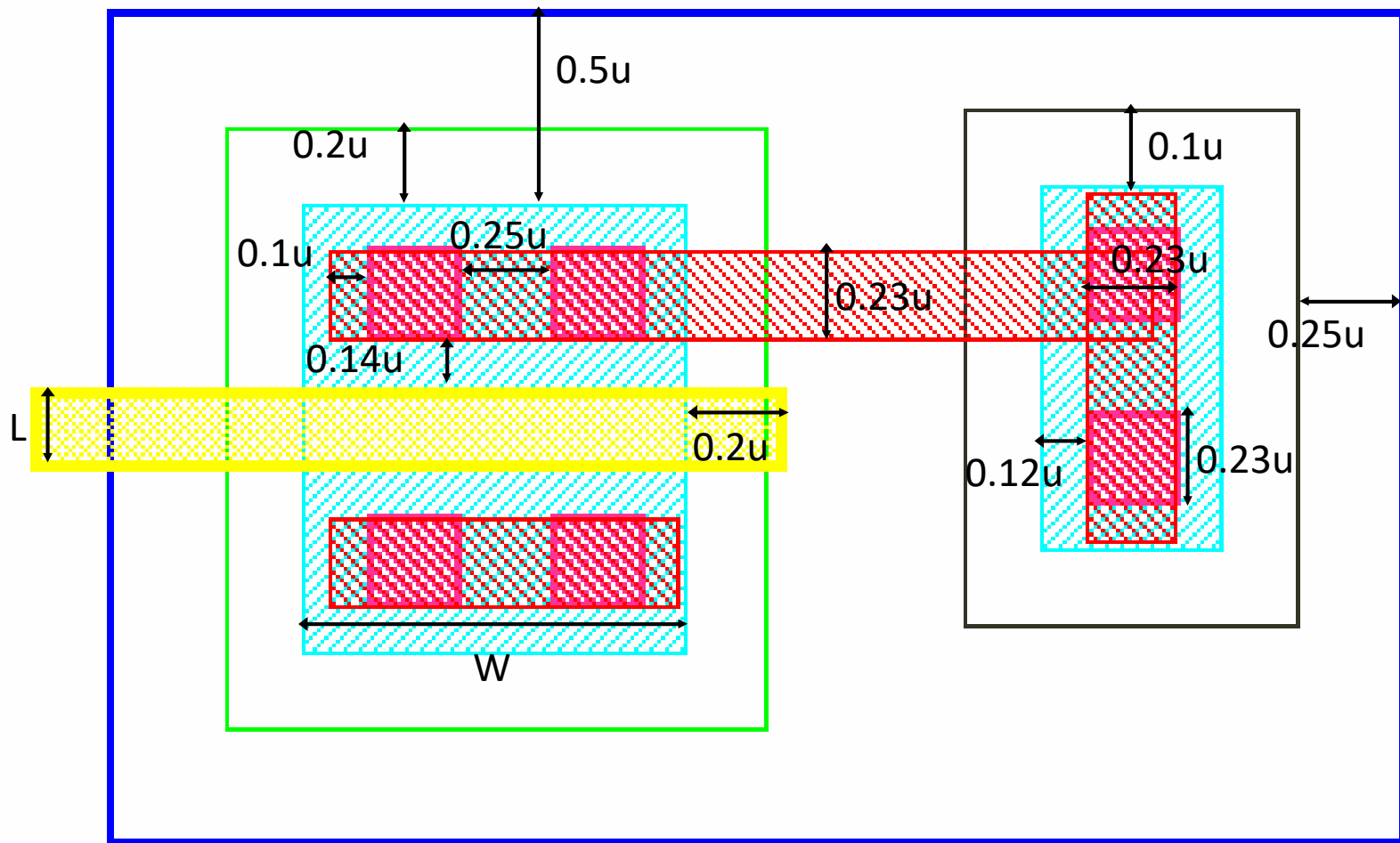
		(unit : um)
CONT.A1	Maximum and Minimum Contact size	0.23 *0.23um ²
CONT.S1	Minimum Contact to Contact spacing	0.25
CONT.S2.18	Minimum Diffusion Contact to Poly spacing (1.8V device)	0.14
CONT.S2.33	Minimum Diffusion Contact to Poly spacing (3.3V device)	0.28
CONT.S3	Minimum Poly Contact to Diffusion edge spacing	0.18
CONT.O1	Minimum Poly overlap Contact	0.12

Design Rule (3/4)



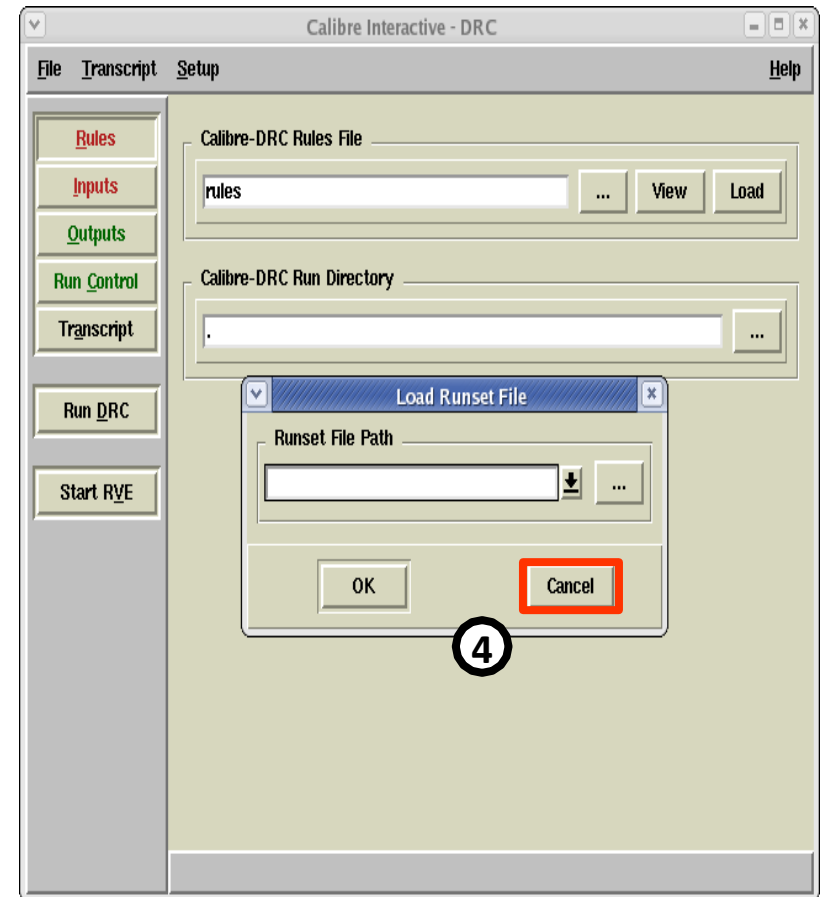
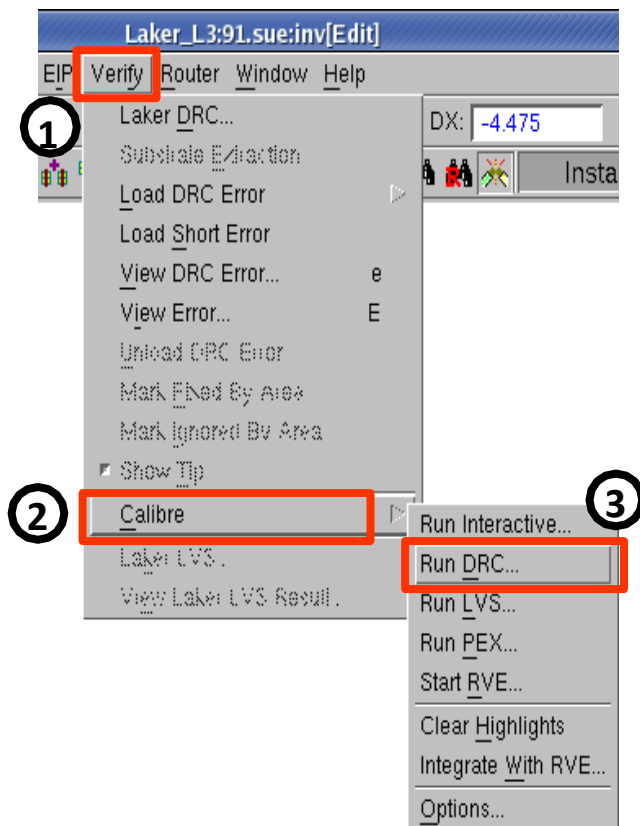
Contact on Poly inside of Diffusion is not allowed.

Design Rule (4/4): PMOS & NWELL

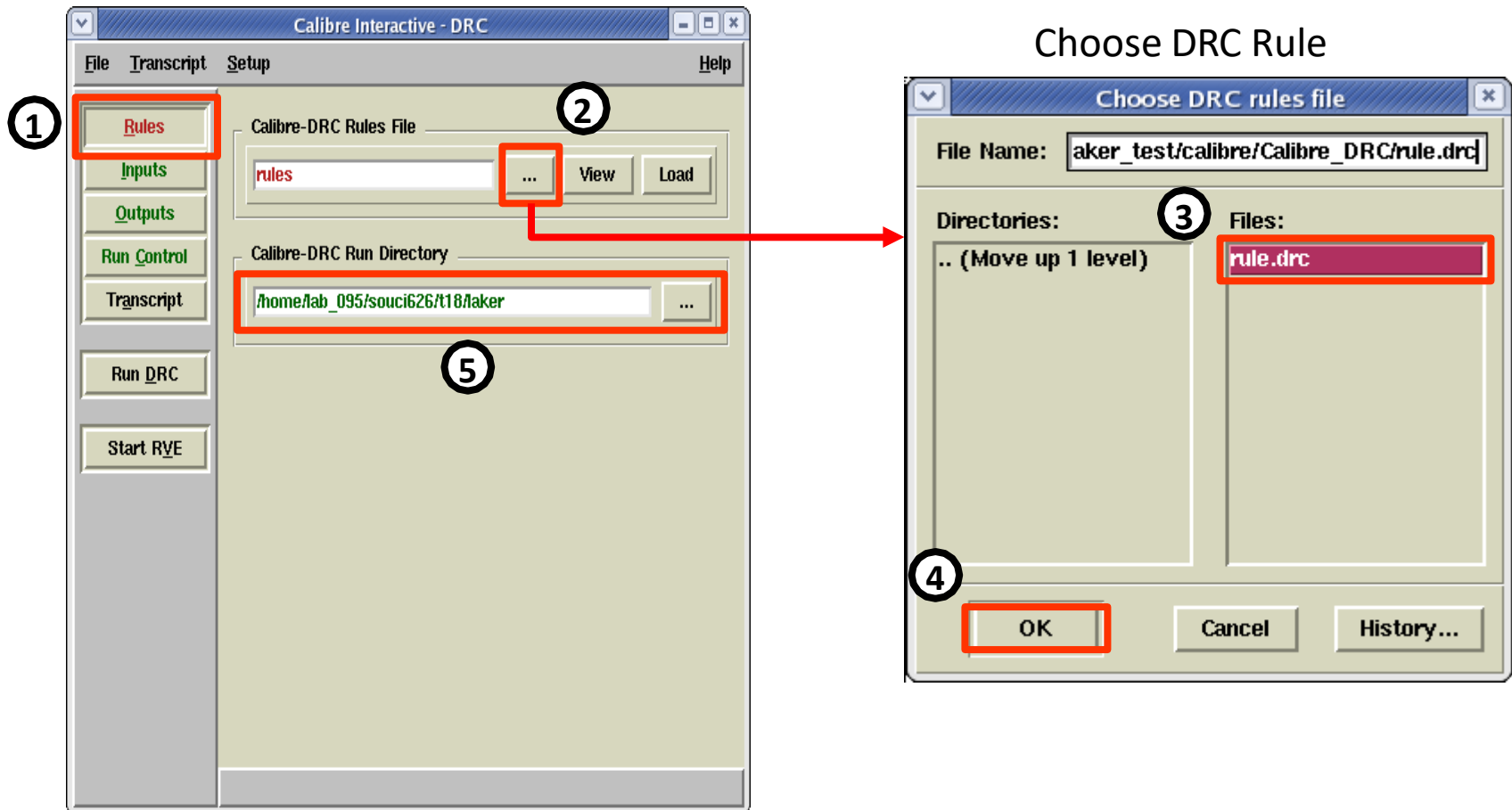


DRC Check – Open DRC

- Check layout layer rule



DRC Check – Define DRC Rule



DRC Check – Define DRC Rule

The image shows two screenshots of the Calibre DRC interface. The left screenshot is the 'Calibre Interactive - DRC' window. It has a menu bar with 'File', 'Transcript', 'Setup', and 'Help'. On the left is a sidebar with buttons: 'Rules', 'Inputs', 'Outputs', 'Run Control', 'Transcript', 'Run DRC', and 'Start RVE'. The 'Run DRC' button is circled with a red box and labeled with a circled '9'. The main area has tabs for 'Hierarchical', 'Flat', and 'Calibre CB'. The 'Layout' tab is selected and labeled with a circled '7'. Below the tabs, there's a 'Files' field containing 'inv.calibre.gds', a 'File Format' dropdown set to 'GDSII', and an 'Export from layout viewer' checkbox which is checked and labeled with a circled '8'. The 'Primary Cell' field is set to 'inv'. The right screenshot is the 'Calibre - DRC RVE : inv.drc.results' window. It has a menu bar with 'File', 'View', 'Highlight', 'Tools', 'Setup', and 'Help'. The main area shows a tree view of results. The 'Error Table' section is highlighted with a red box and contains the following data:

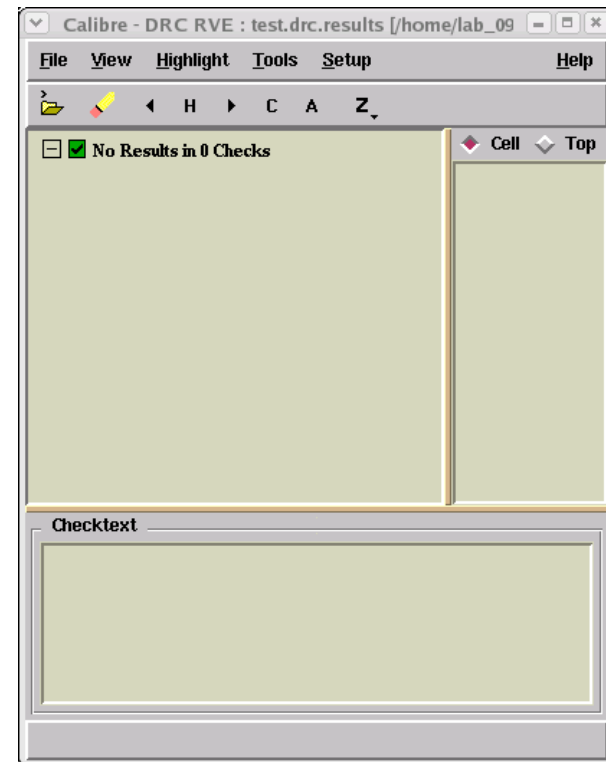
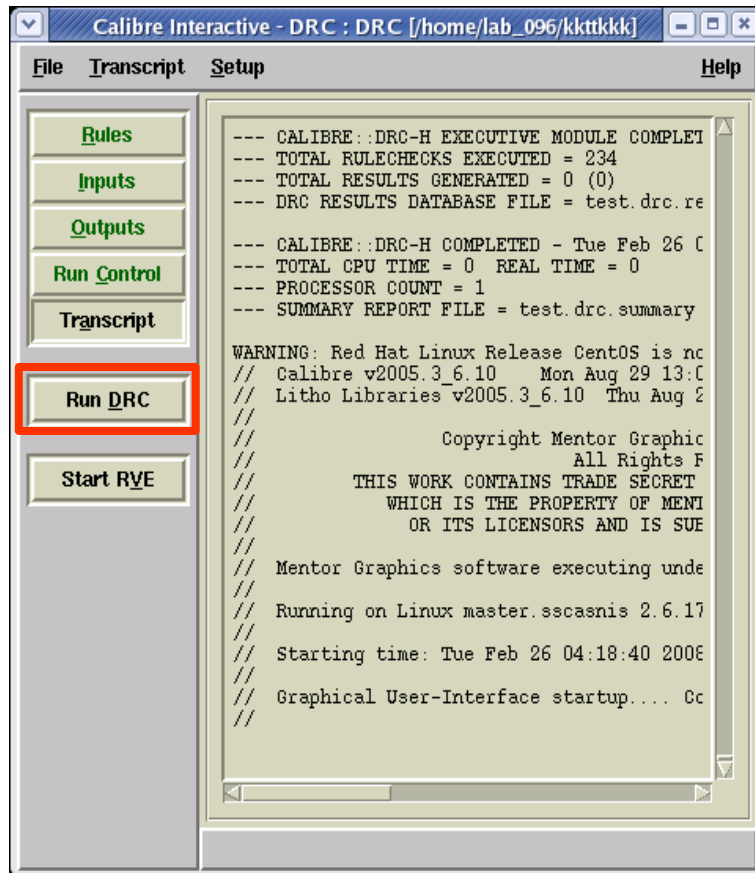
Cell	Top
4-Vertex Polygon	
Coordinates: (in inv)	
2.495	-3.175
2.915	-3.175
2.915	-2.755
2.495	-2.755

The 'Error Message' section is also highlighted with a red box and contains the following text:

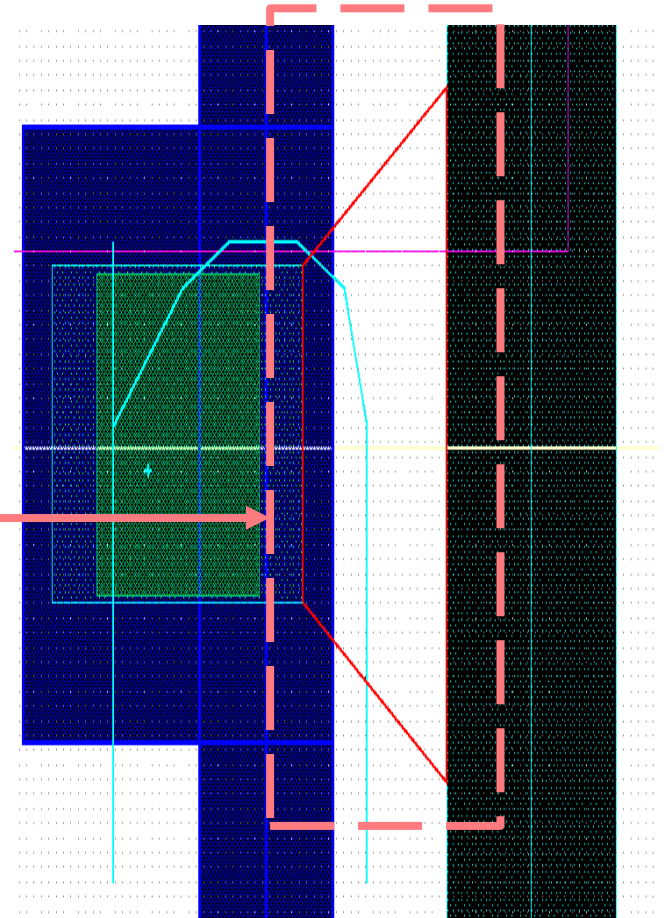
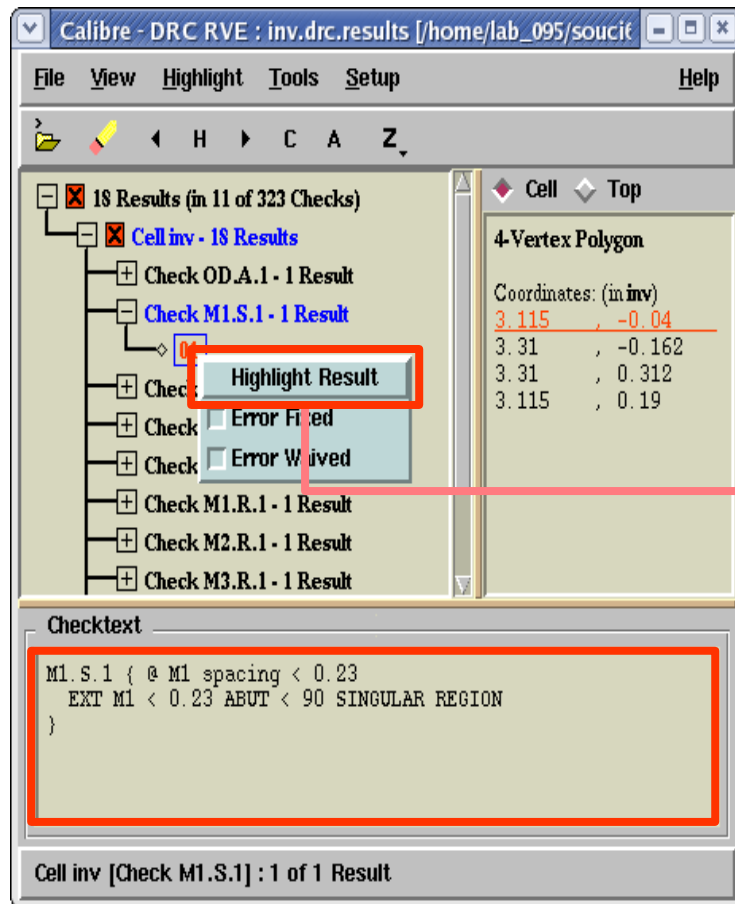
```
OD.A.1 { @ Minimum area of standard OT region < 0.202
OD AREA < 0.202
}
```

An orange arrow points from the 'Run DRC' button in the left window to the 'Error Table' in the right window.

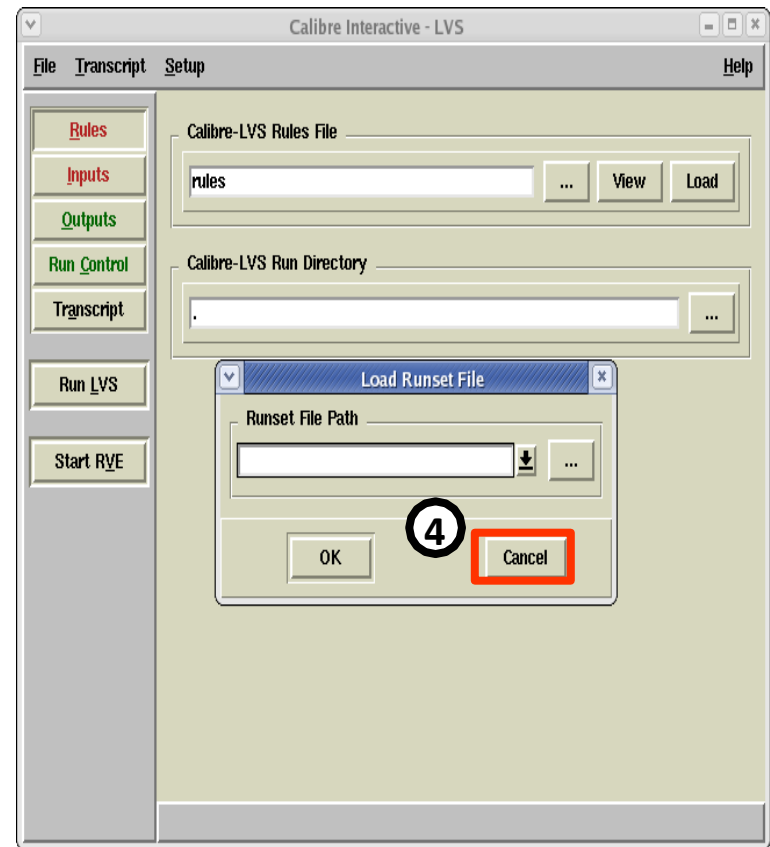
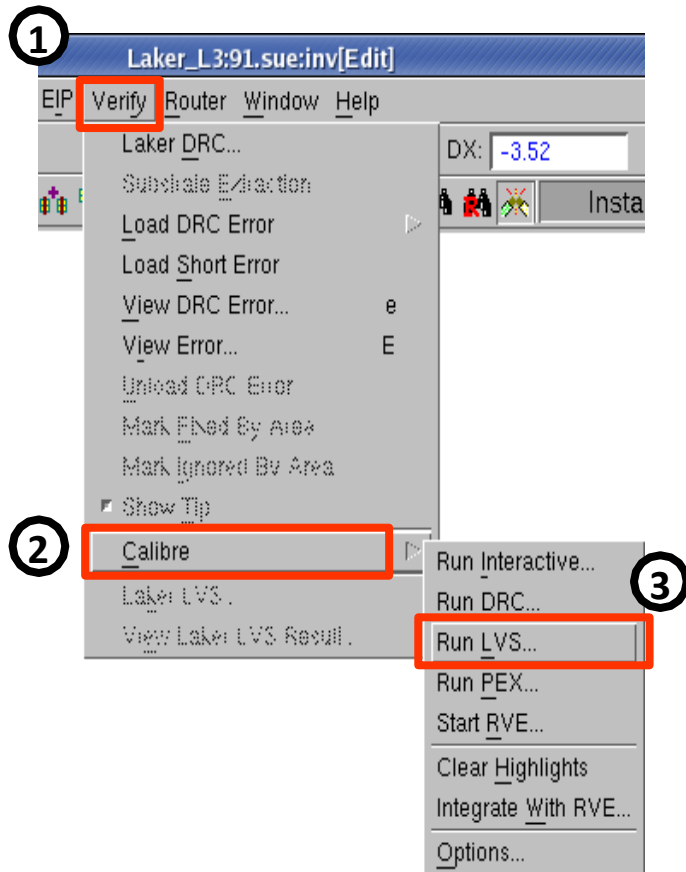
DRC Check – No Error



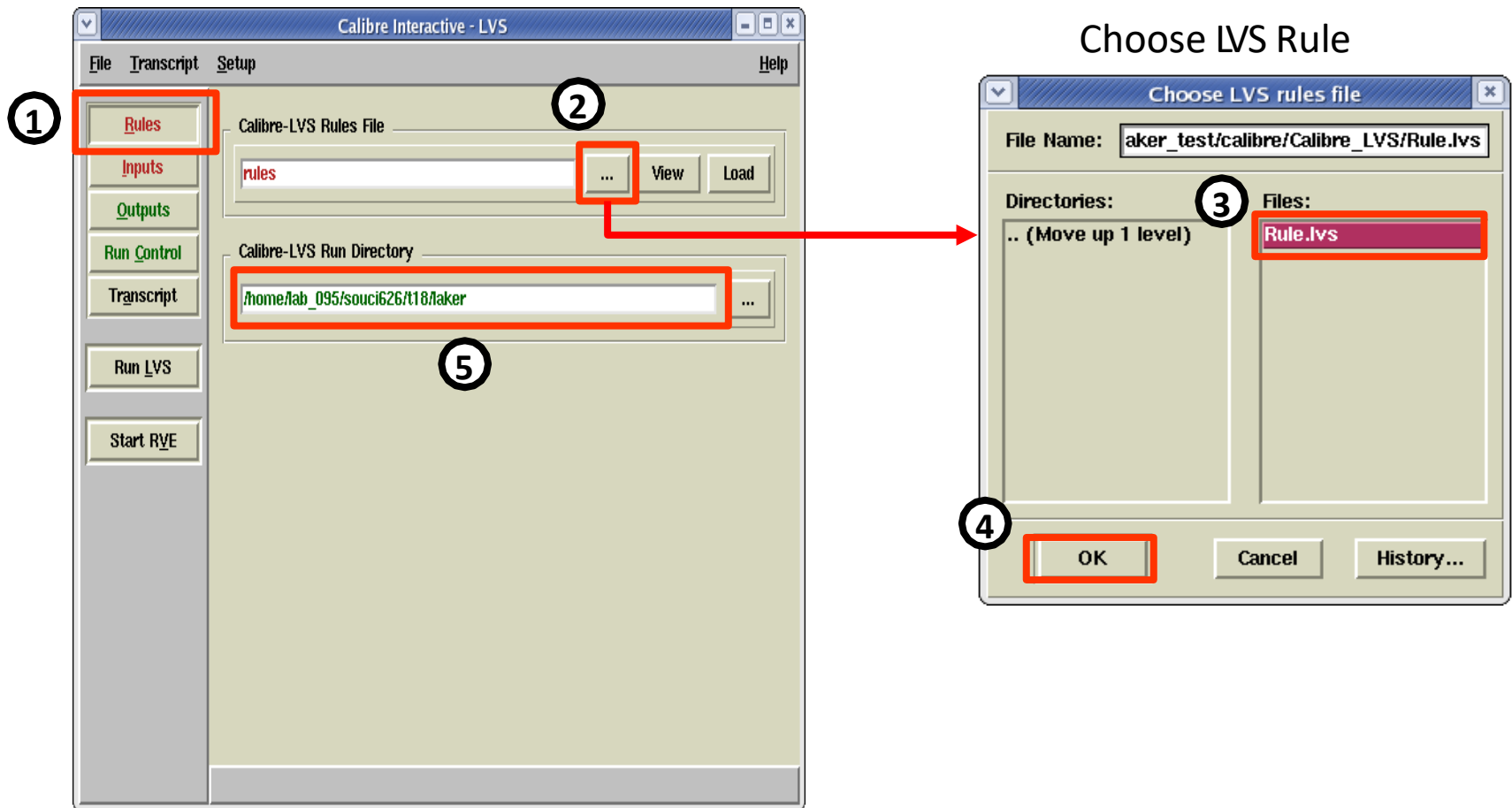
DRC Check – Highlight Error



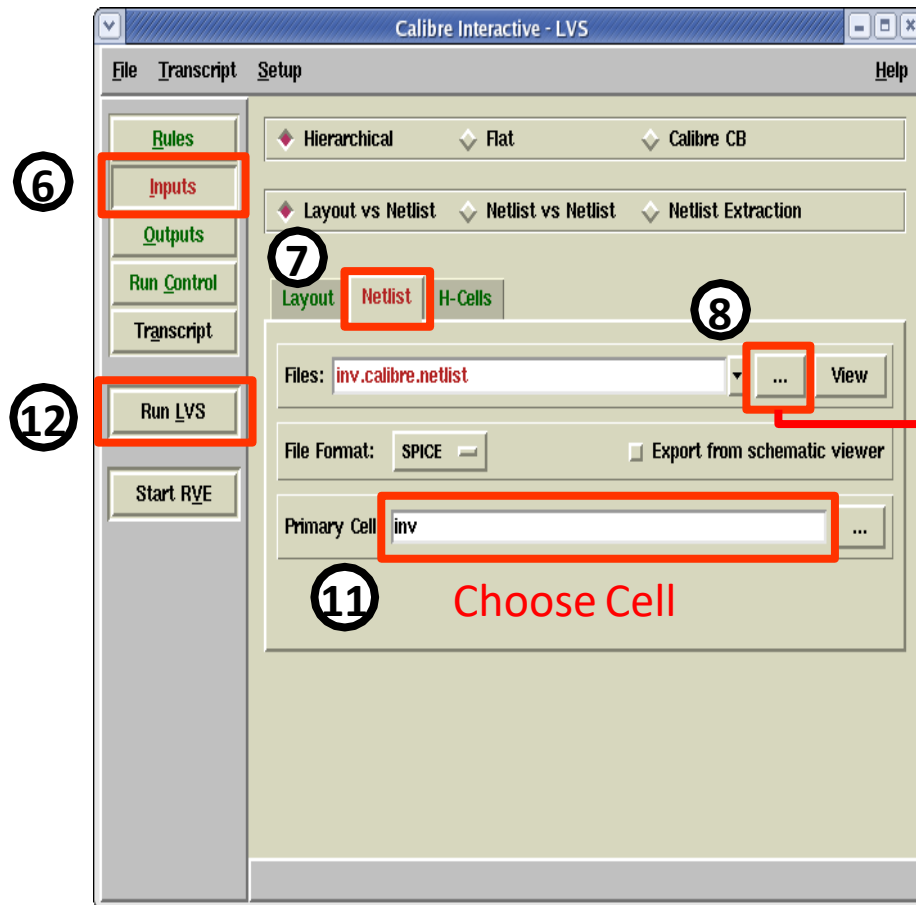
LVS Check – Open LVS



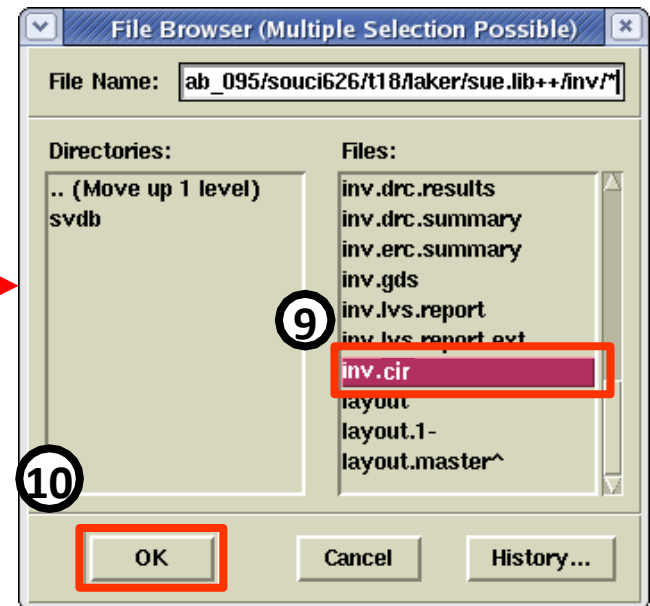
LVS Check – Define LVS Rule



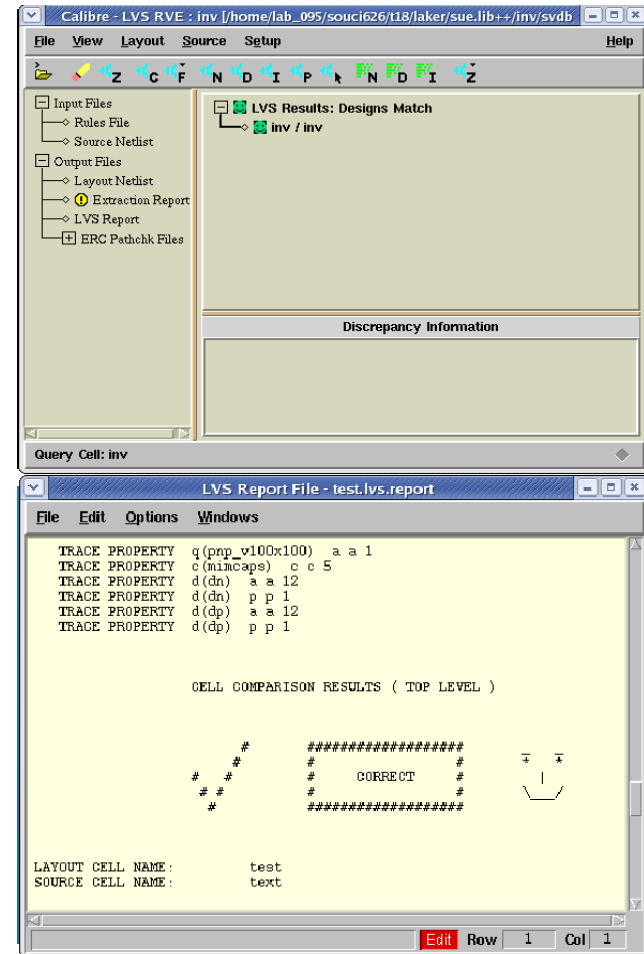
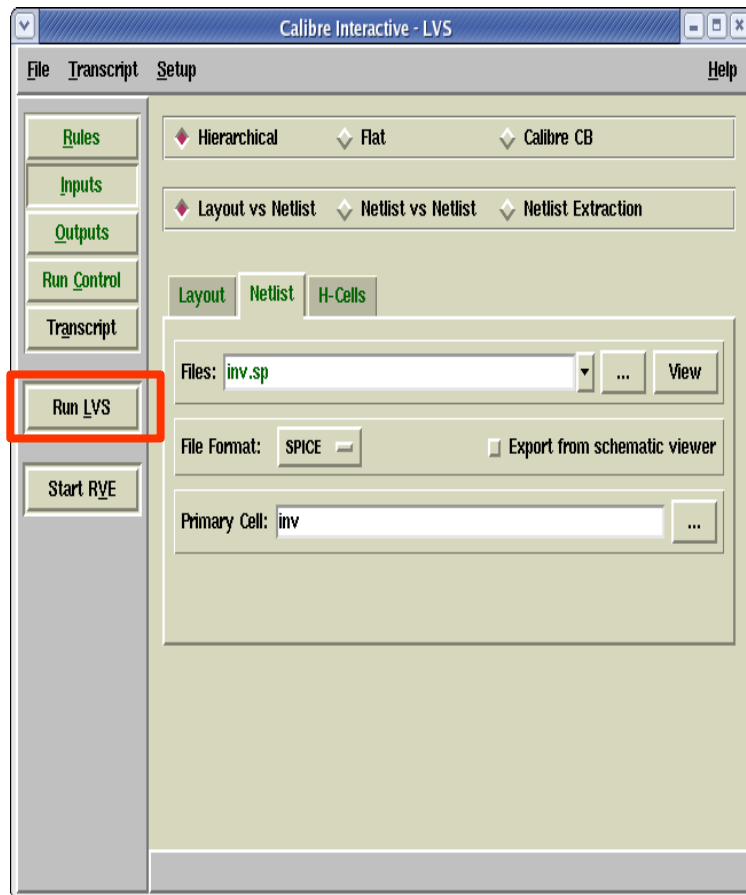
LVS Check – Define LVS Rule



Choose LVS Rule



LVS Check – No Error



LVS Check – Error

Calibre - LVS RVE : inv [/home/lab_095/souci626/t18/laker/sue.lib++/inv/svdb]

File View Layout Source Setup Help

Input Files
Rules File
Source Netlist
Output Files
Layout Netlist
Extraction Report
LVS Report
ERC Pathchk Files

LVS Results: Designs Don't Match
inv / inv - 1 Discrepancy
Incorrect Nets - 1 Discrepancy
Discrepancy #1

Error Message

Error Table

inv / inv: Discrepancy #1 - Incorrect Nets

LAYOUT NAME	ne	SOURCE NAME
Net IN		IN

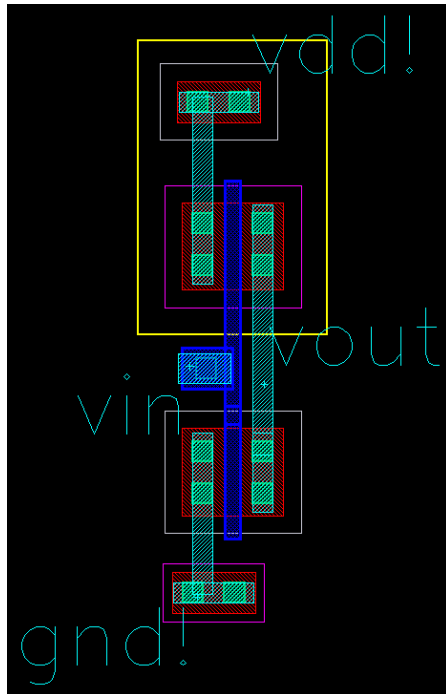
Layout

Netlist

Query Cell: inv

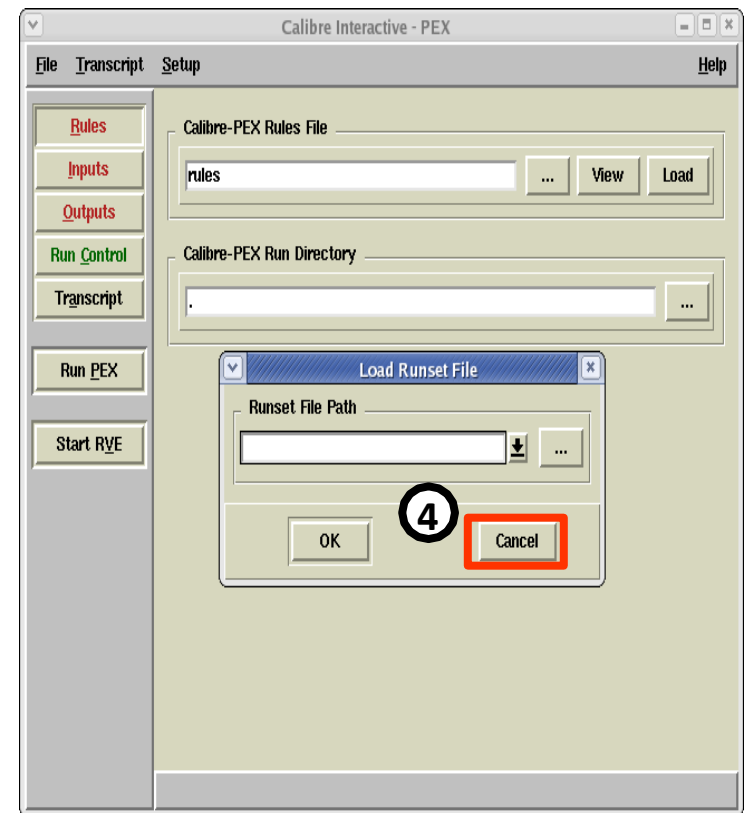
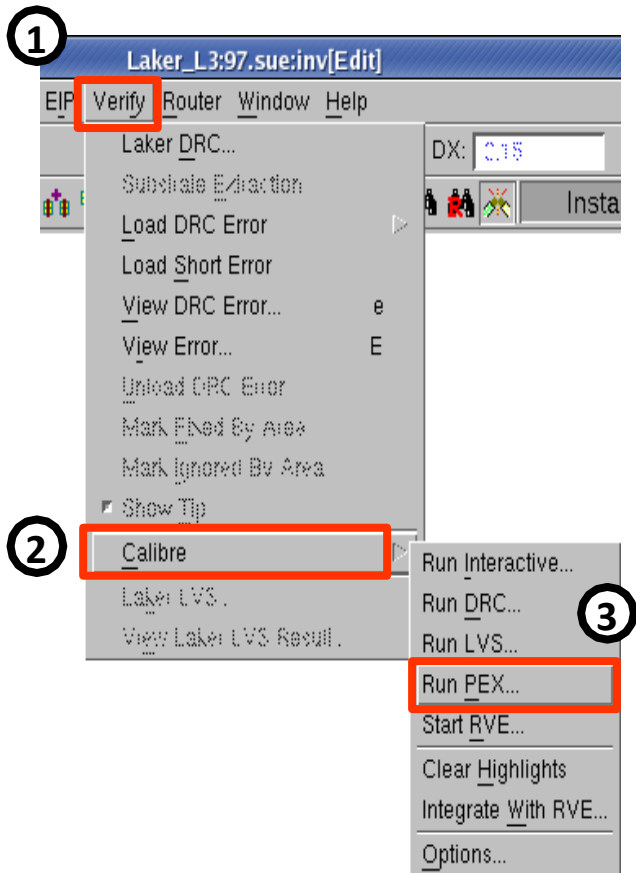
LVS Check – Be Careful !!

- Layout 中的pin name要和sub-circuit中的pin name相同 (ex: vin, vout, vdd!, gnd!)
- Layout中一定要記得打上 “vdd!”和 “gnd!”

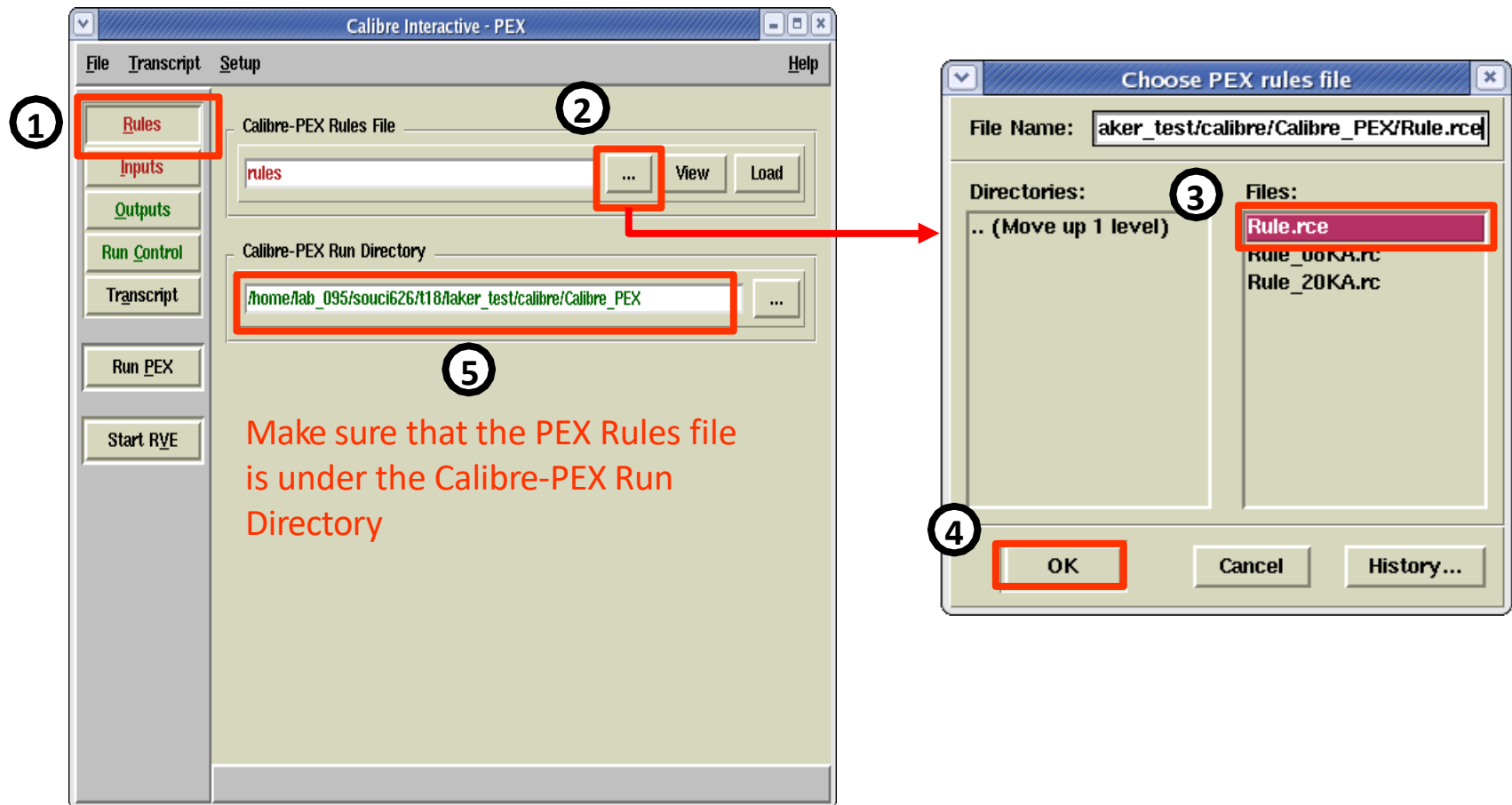


```
.SUBCKT text vin vout
MM1 vout vin gnd! gnd! n_18 W=1u L=180.00n
MM0 vout vin vdd! vdd! p_18 W=1u L=180.00n
.ENDS
```

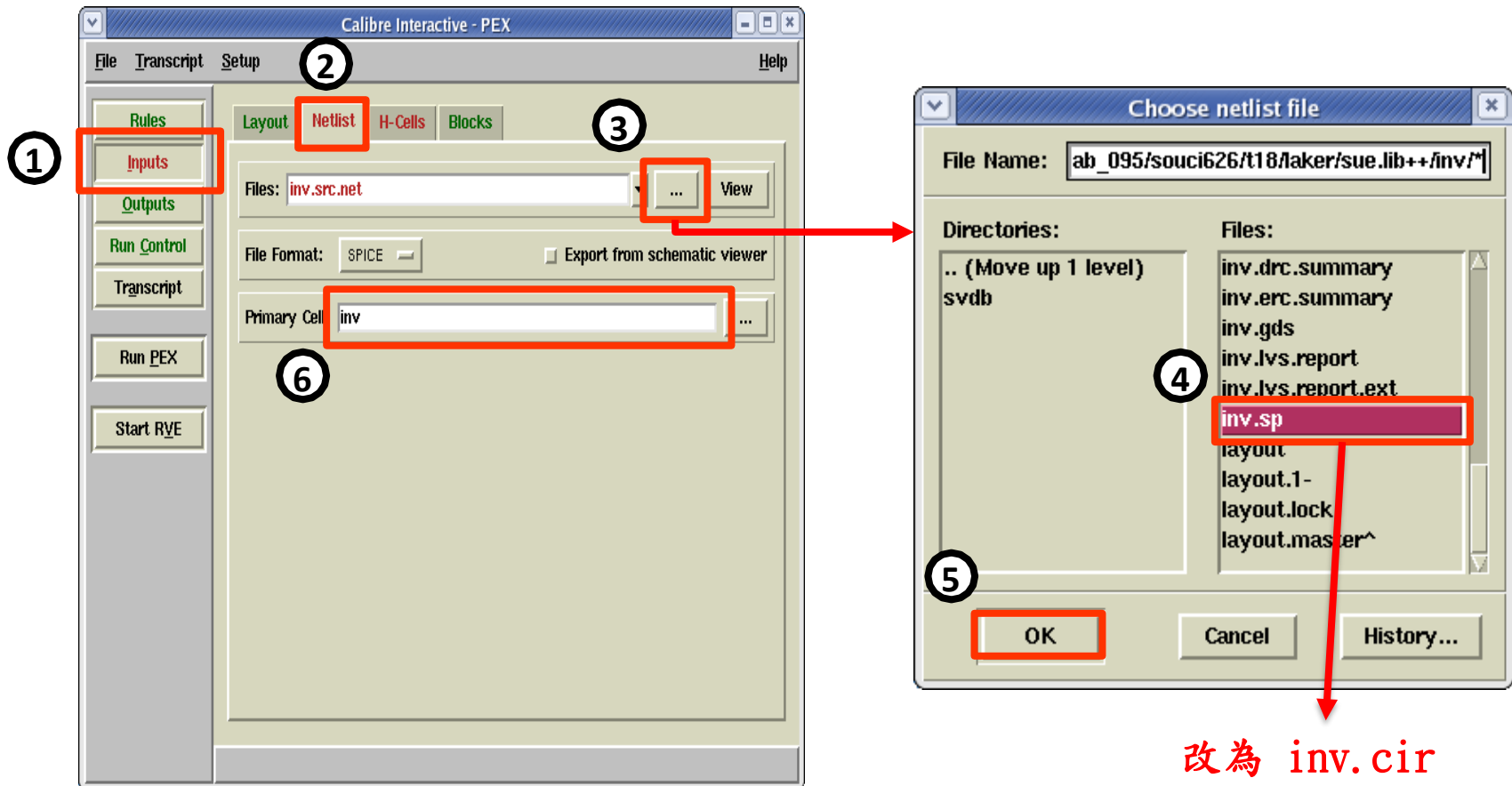

PEX – Open PEX



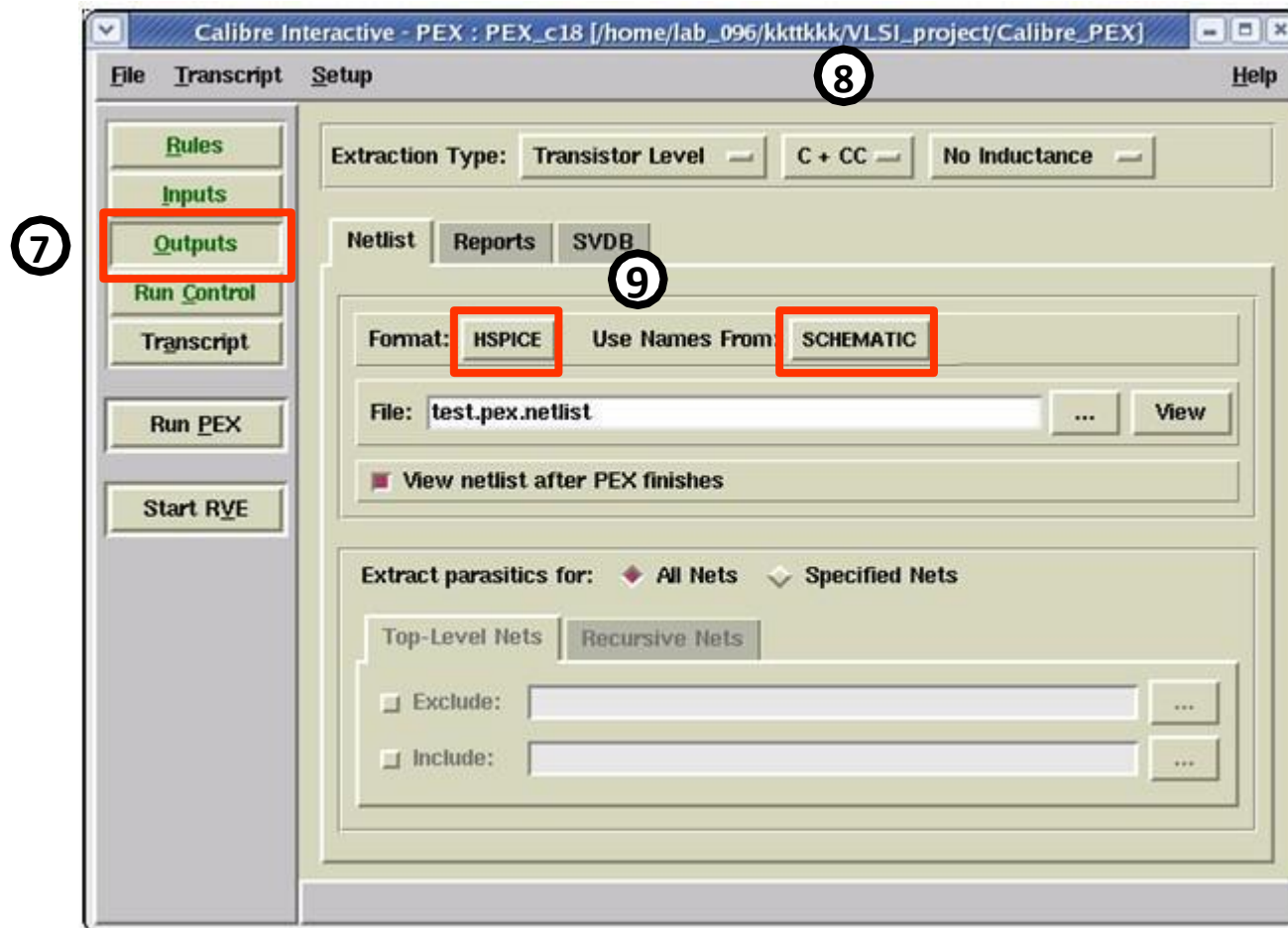
PEX – Define PEX Rule



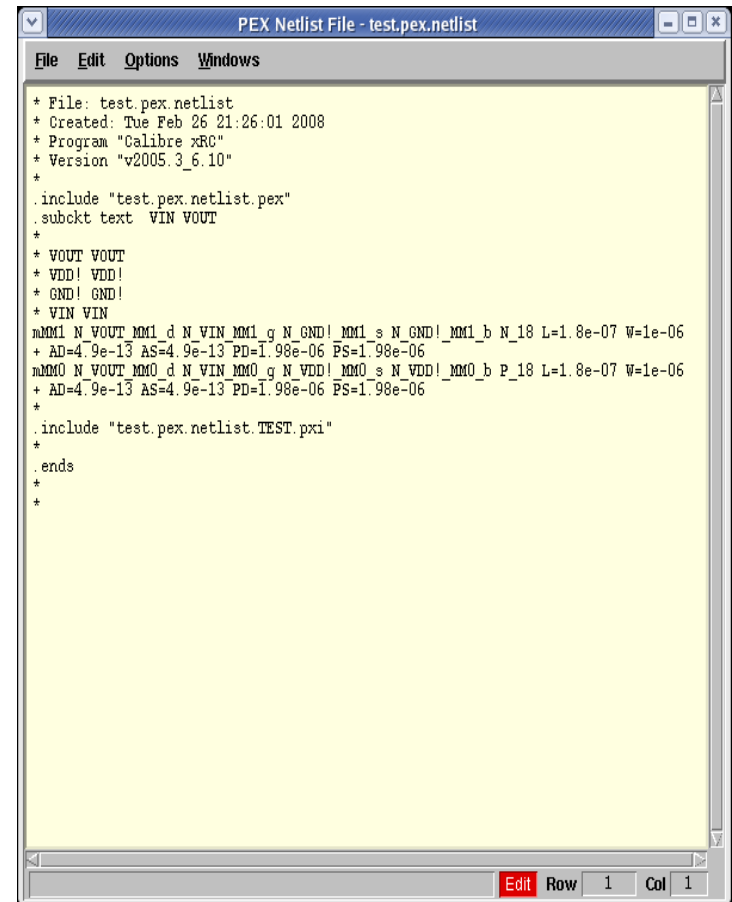
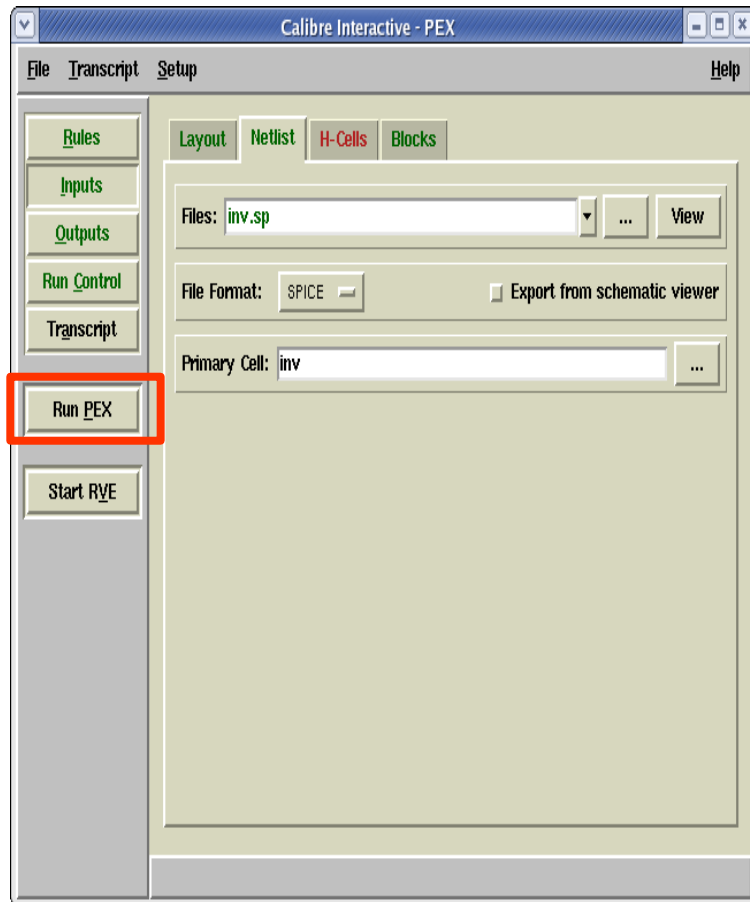
PEX – Define Netlist File (1/2)



PEX – Define Netlist File (2/2)



PEX – PEX Result



PEX – Netlist File

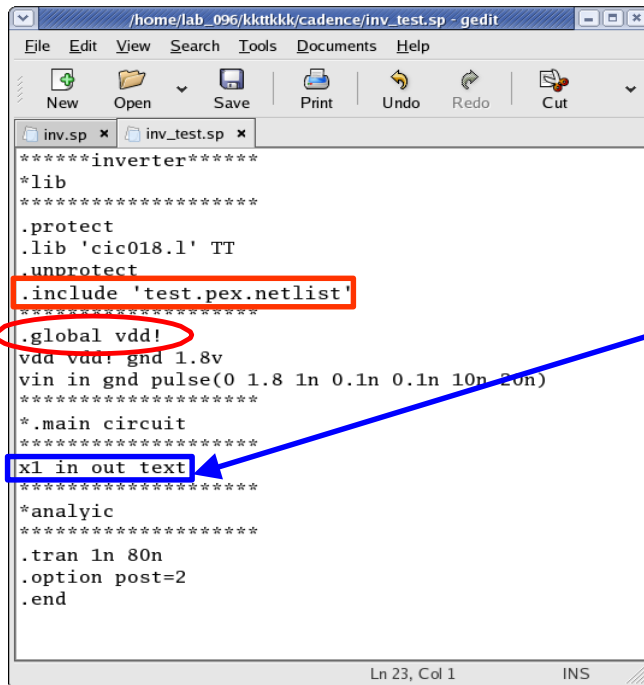
- Three output files:

- xxx.pex.netlist
- xxx.pex.netlist.pex
- xxx.pex.netlist.xxx.pxi

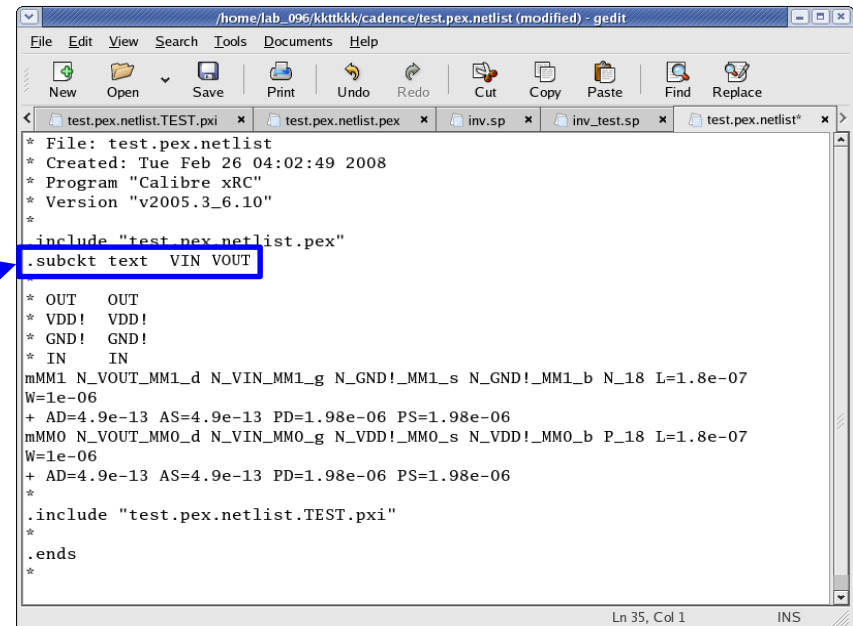
Top circuit (ex: test.pex.netlist)

sub-circuit (ex: test.pex.netlist.pex)

connection (ex: test.pex.netlist.TEST.pxi)



```
****inverter****
*lib
*****
.protect
.lib 'cic018.1' TT
.unprotect
.include 'test.pex.netlist'
*****
.global vdd!
vdd vdd! gnd 1.8v
vin in gnd pulse(0 1.8 1n 0.1n 0.1n 10n 20n)
*****
*.main circuit
*****
x1 in out text
*****
*analyic
*****
.tran 1n 80n
.option post=2
.end
```



```
* File: test.pex.netlist
* Created: Tue Feb 26 04:02:49 2008
* Program "Calibre xRC"
* Version "v2005.3_6.10"

.include "test.pex.netlist.pex"
.subckt text VIN VOUT

* OUT OUT
* VDD! VDD!
* GND! GND!
* IN IN
mMM1 N_VOUT_MM1_d N_VIN_MM1_g N_GND!_MM1_s N_GND!_MM1_b N_18 L=1.8e-07
W=1e-06
+ AD=4.9e-13 AS=4.9e-13 PD=1.98e-06 PS=1.98e-06
mMM0 N_VOUT_MM0_d N_VIN_MM0_g N_VDD!_MM0_s N_VDD!_MM0_b P_18 L=1.8e-07
W=1e-06
+ AD=4.9e-13 AS=4.9e-13 PD=1.98e-06 PS=1.98e-06
*
.include "test.pex.netlist.TEST.pxi"
*
.ends
*
```