



CADENCE VIRTUOSO

SCHEMATIC EDITOR

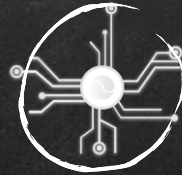


PRESENTER: PO-HAN, LIN (林柏翰)

ADVISOR: SOON-JYH CHANG (張順志)



Introduction to Cadence Virtuoso Schematic Editor



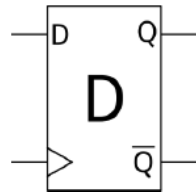
INTRODUCTION

X Cadence Virtuoso Schematic Editor

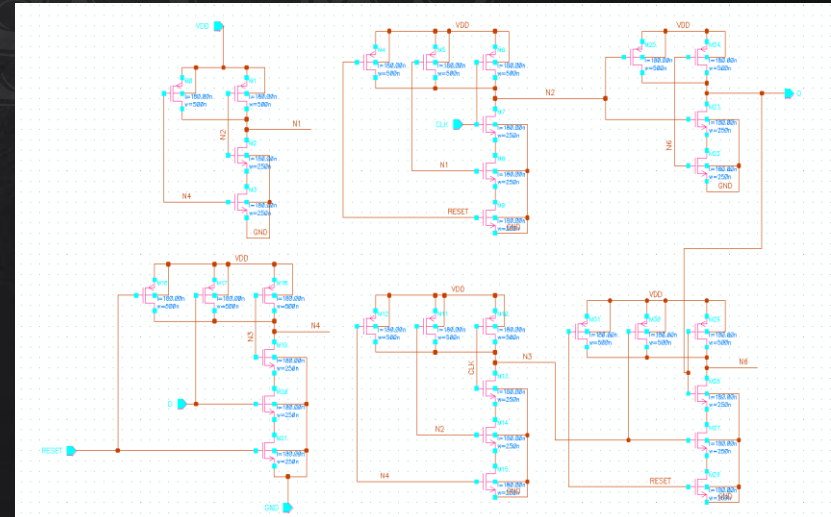
Cadence's Product

Create and edit a schematic

Simulate circuit



D Flip-Flop



cadence

Custom IC Design Tools

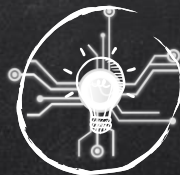
Virtuoso® Front to Back Design Environment

Copyright © 1992-2009 Cadence Design Systems, Inc. All rights reserved. Cadence and the Cadence logo are registered trademarks. All others are properties of their respective holders.



Start Virtuoso



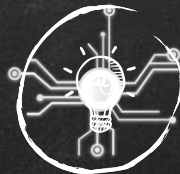


Start Virtuoso(1/2)

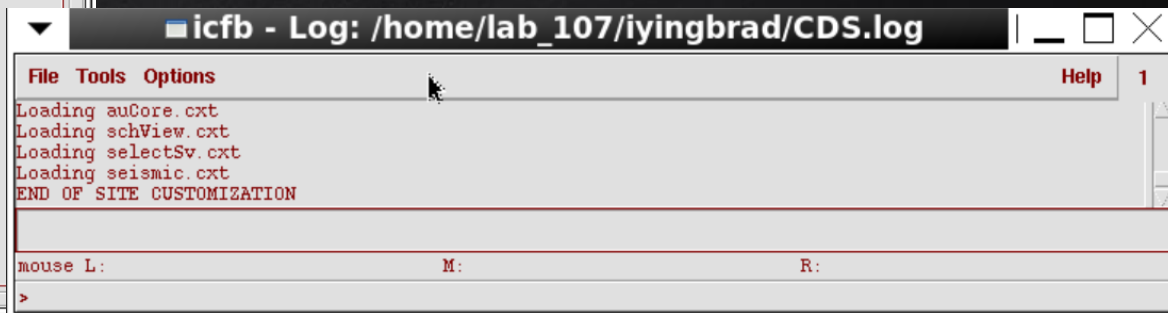
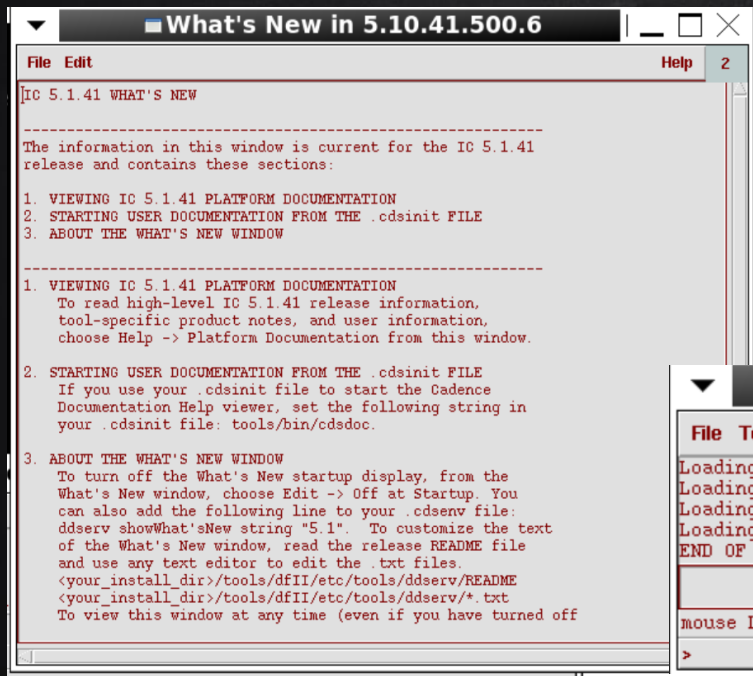
- X Open terminal in the folder you want to save the schematic
Type command: icfb &
The '&' is optional

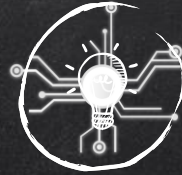
```
iyingbrad@goat:~/schematic_
File Edit View Search Terminal Help
[iyingbrad@goat ~/schematic_folder]$ icfb &
[1] 28609
[iyingbrad@goat ~/schematic_folder]$
```

Folder in which you
want to save schematic



Start Virtuoso(2/2)





Library Manager

icfb - Log: /home/lab_107/iyingbrad/CDS.log

1

Tools

2

Library Manager...

Library Path Editor...

PCD

Verilog Integration

VHDL Tool Box...

Synopsys Integration...

Router

Constraint Manager...

Mixed Signal Environment

Analog Environment

VSHE

Technology File Manager...

Display Resource Manager...

CDF

AMS

Camera

SKILL Development...

Library Manager: Directory ...107/iyingbrad/schematic folder

File Edit View Design Manager Help

Show Categories Show Files

Library	Cell	View
US_8ths ahdLib analogLib basic cdsDefTechLib functional rfExamples rfLib		

Library

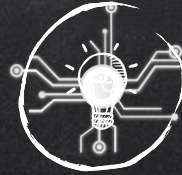
CELL:
Inverter
And...

View:
Schematic
symbol ...

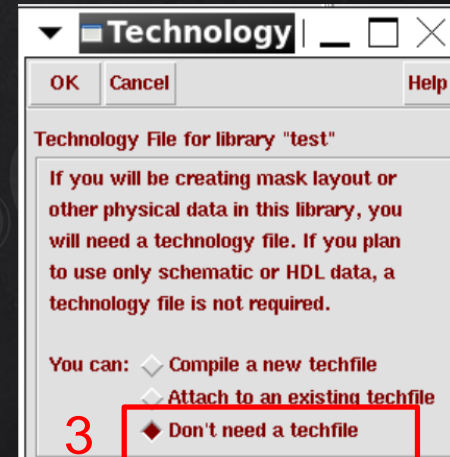
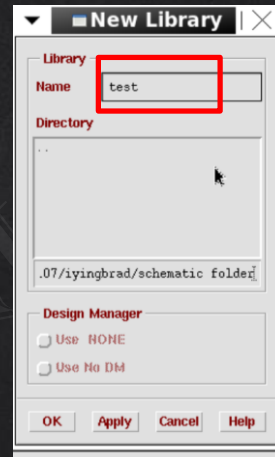
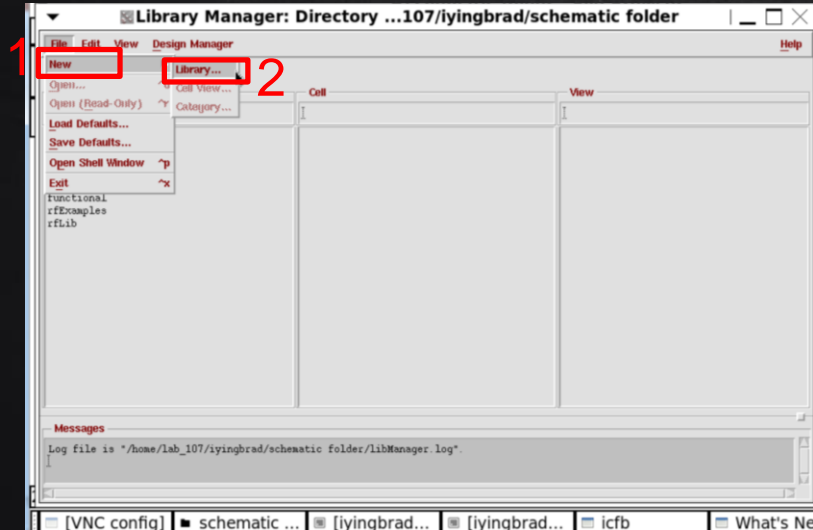
Messages

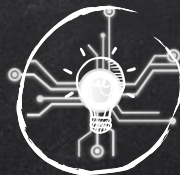
Log file is "/home/lab_107/iyingbrad/schematic folder/libManager.log".

AIWAN

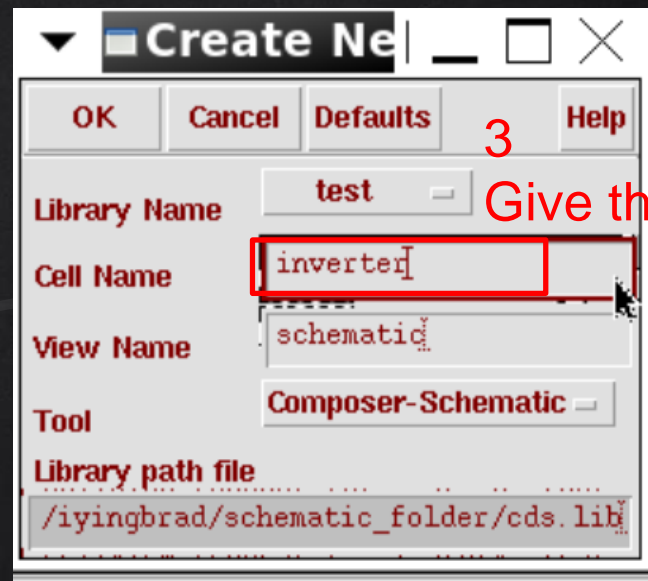
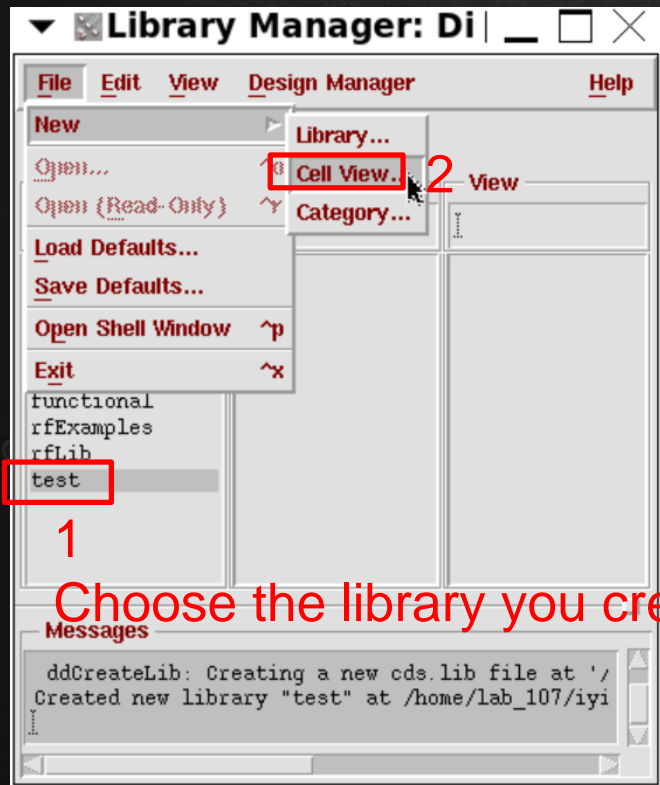


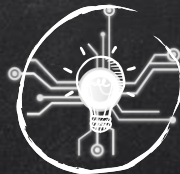
Create New Library



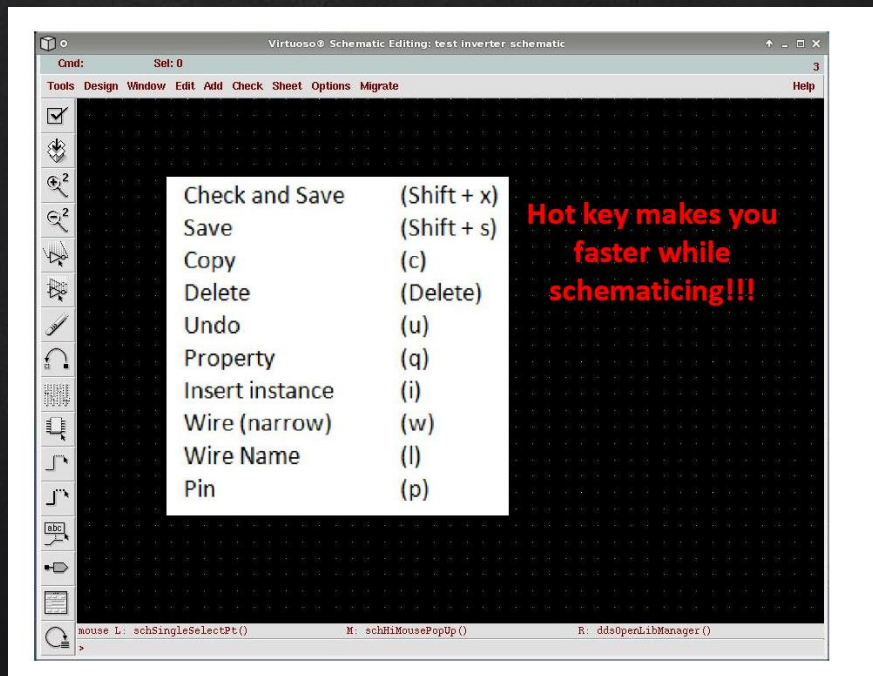


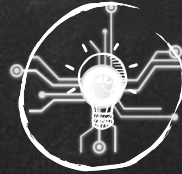
Create New Cell



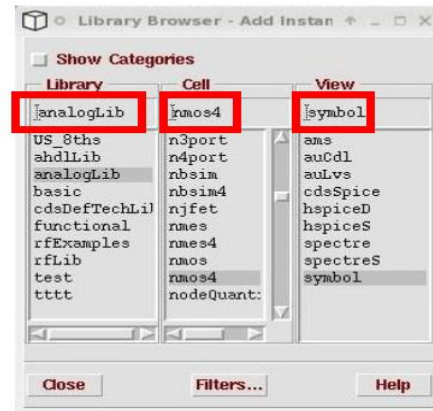
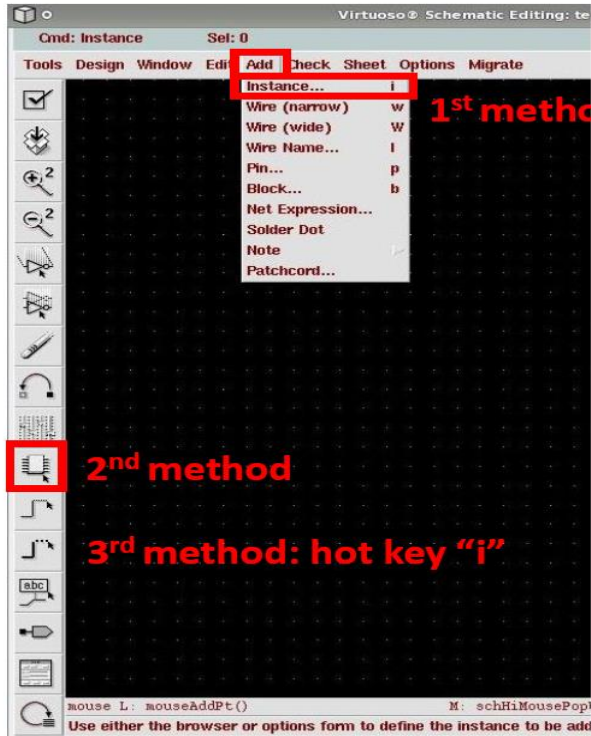


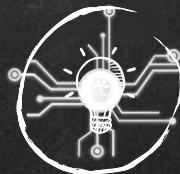
Hot key for schematic





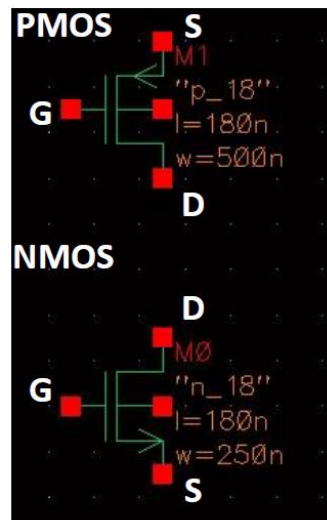
Add instance





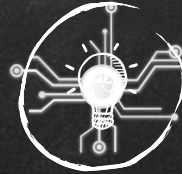
Add instance

Library: analogLib
Cell: nmos4
View: symbol
Names:
Array: Rows: 1, Columns: 1
Rotate, Sideways, Upside Down
Model name: n_18
Multiplier:
Width: 250n M
Length: 180n M
Drain diffusion area:
Source diffusion area:
Drain diffusion periphery:



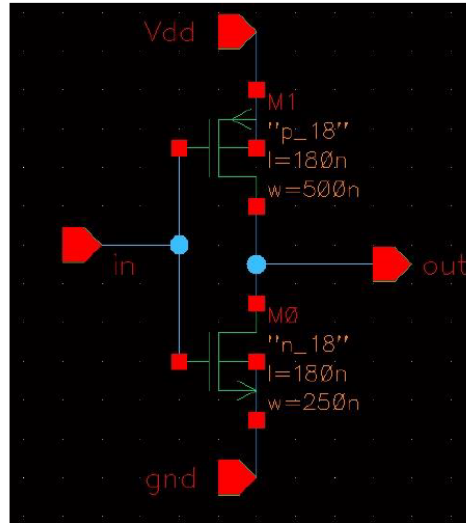
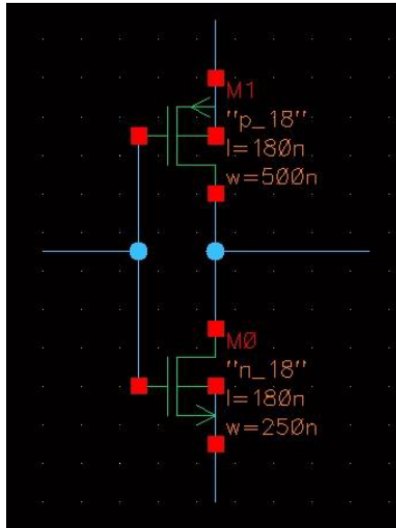
Model Name:

1. n_18 (for NMOS)
2. p_18 (for PMOS)



Inverter – wiring and pins

Wire: hot key “w” Pin: hot key “p”



Wire body to vdd (for PMOS)
gnd (for NMOS)

3. Hide



1. Give pin name

Set pin direction



Inverter -tips

Virtuoso® Schematic Editing: test inverter schematic

Cmd: Wire Name Sel: 0 8

Tools Design Window Edit Add Check Sheet Options Migrate Help

Wire name need to be the same as pin name! (except for inter node)

in Vdd M1 "p_18" l=180n w=500n in out M0 "n_" l=180n w=200n gnd

mouse L: mouseAddPt() M: schHiMousePopUp()
Point at location for the wire name.

Add Wire Name

Hide Cancel Defaults Help

Wire Name Net Expression

Names net

Font Height 0.0625

Font Style stick

Justification lowerCenter

Entry Style fixed offset

Bus Expansion off on

Placement single multiple

Purpose label alias

Bundle Display horizontal vertical

Show Offset Defaults

Rotate



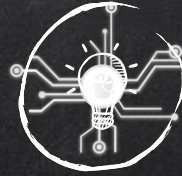
Inverter -Check and save

The screenshot displays the Cadence Virtuoso Schematic Editor interface. The main window shows a schematic of an inverter with an input terminal 'IN', an output terminal 'OUT', and power connections to 'VDD' and 'GND'. The inverter is implemented with two MOSFETs: a PMOS transistor (labeled 'p_18') and an NMOS transistor (labeled 'n_18'). The PMOS parameters are 'l=180n' and 'w=1u'. The NMOS parameters are 'l=180n' and 'w=500n'. The left toolbar contains various design tools, with the 'Check and Save' icon (a checkmark) highlighted by a red box.

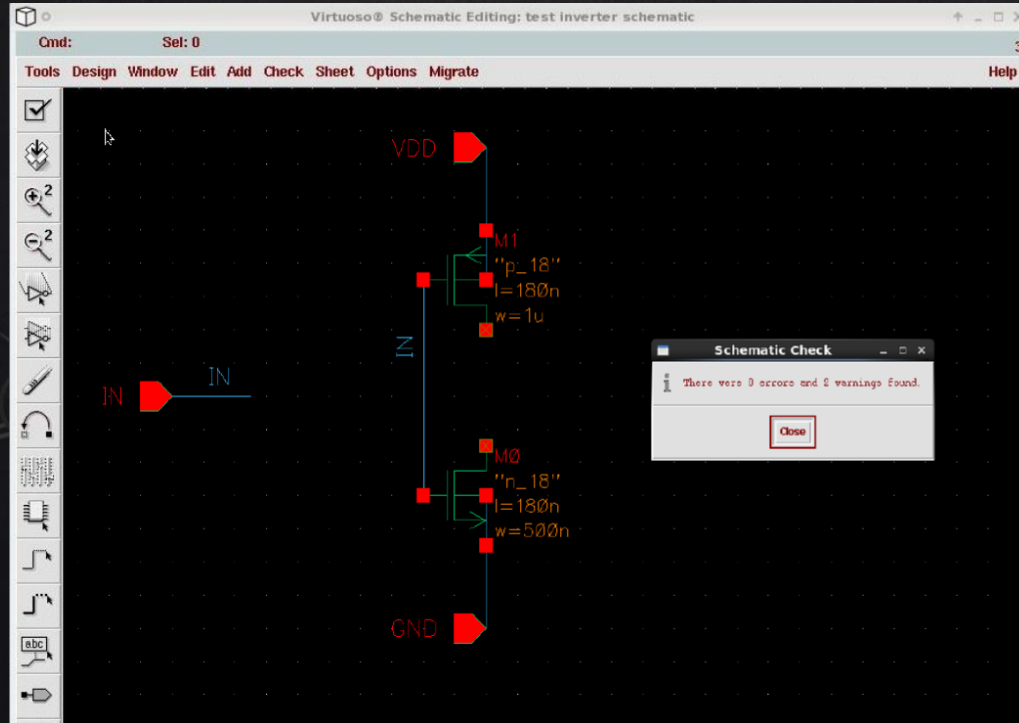
Overlaid on the right is a command window titled 'icfb - Log: /home/ncu_class/vlsi2016/vlsi201698/CDS.log'. It shows the following log entries:

```
File Tools Options
Loading cdf.cxt
Loading layers.cxt
Extracting "inverter.schematic"
"test inverter schematic" saved
Loading schView.cxt
mouse L: mouseAddPt() M: schHiMousePopUp() R: Rotate 90
Use the options form to supply terminal names for the pins.
```

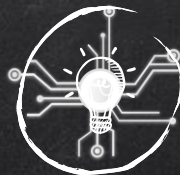
A red box highlights the line '"test inverter schematic" saved', and a large red text overlay 'Succeed!' is positioned next to it.



Inverter- Error



Please make sure there is no error before you go to the next step!



Inverter – create cellview(1/2)

The image shows the Virtuoso Schematic Editing interface for creating a cellview for an inverter. The main schematic shows an inverter symbol with pins labeled IN, OUT, VDD, and GND. A red box highlights the 'Design' menu, and another red box highlights the 'Create Cellview' option. A third red box highlights the 'From Cellview...' option. A red arrow points from the 'From Cellview...' option to the 'Cellview From Cellview' dialog box. Another red arrow points from the 'Cellview From Cellview' dialog box to the 'Symbol Generation Options' dialog box.

Cellview From Cellview

OK Cancel Defaults Apply Help

Library Name test Browse

Cell Name inverted

From View Name schematic To View Name symbol

Tool / Data Type Composer-Symbol

Display Cellview ☐

Edit Options ☐

Symbol Generation Options

OK Cancel Apply Help

Library Name test Cell Name inverted View Name symbol

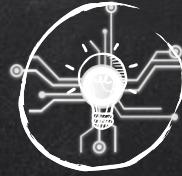
Pin Specifications

Pin Specification	Value	Attributes
Left Pins	Vdd gnd in	List
Right Pins	out	List
Top Pins		List
Bottom Pins		List

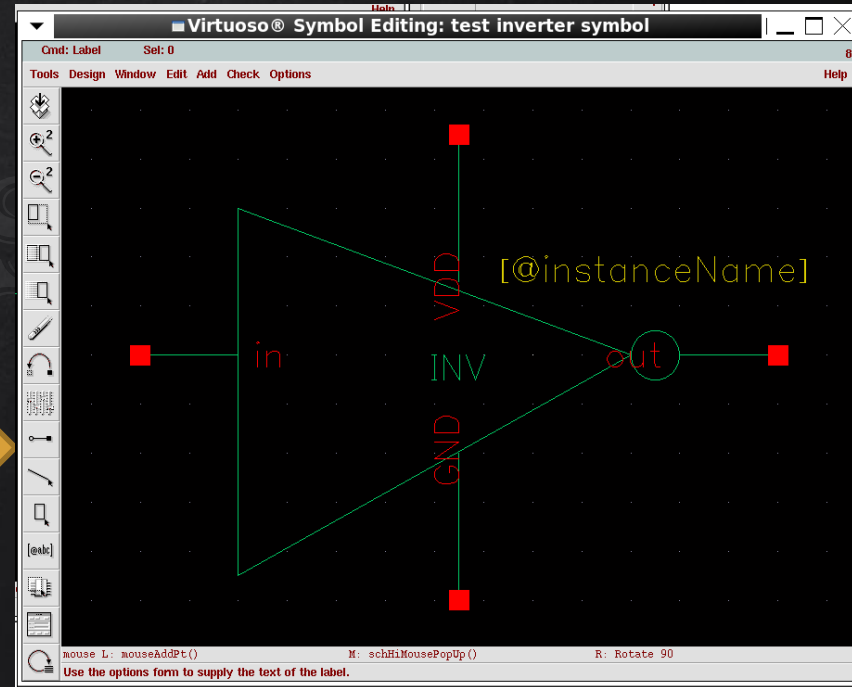
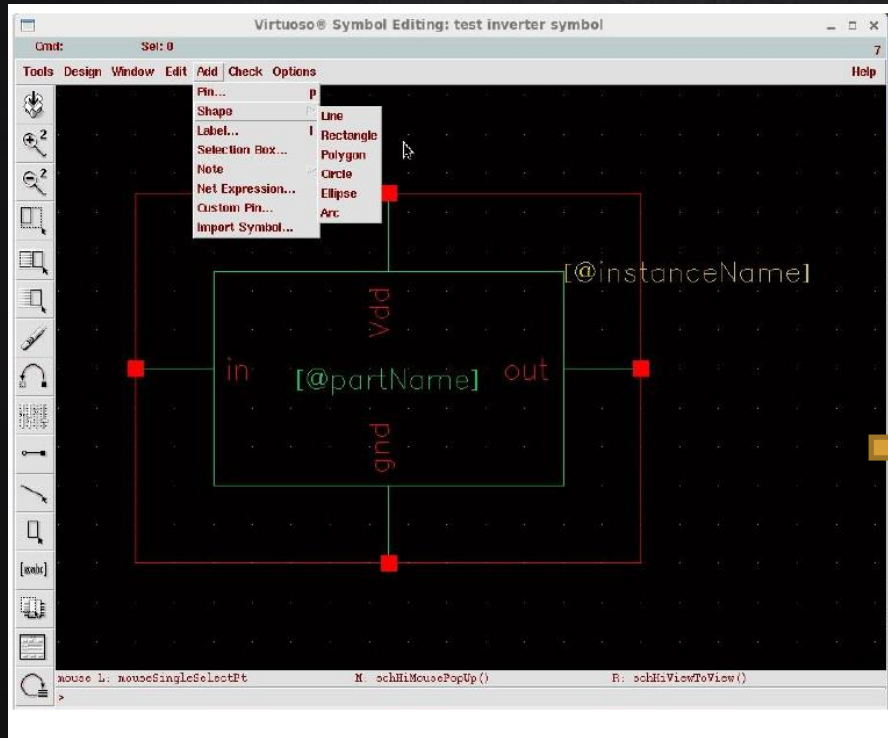
Exclude Inherited Connection Pins:

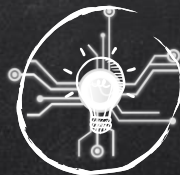
☒ None ☐ All ☐ Only these:

Load/Save ☐ Edit Attributes ☐ Edit Labels ☐ Edit Properties ☐



Inverter – create cellview(2/2)





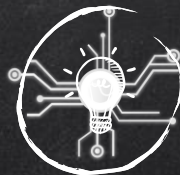
Inverter – use symbol on other cell(1/2)

On new cell (NAND NOR ...), you can hierarchically create the circuit with add instance

The screenshot displays the Virtuoso Schematic Editing environment. The main window, titled "Virtuoso® Schematic Editing: test buffer schematic", shows a schematic diagram of an inverter (a triangle with a circle at the output) on a grid. The status bar at the bottom indicates the mouse is at location (1, 1) and the instance is at (1, 1). The status bar also shows the command "M: schHiMousePopUp ()" and "R: Rotate 90".

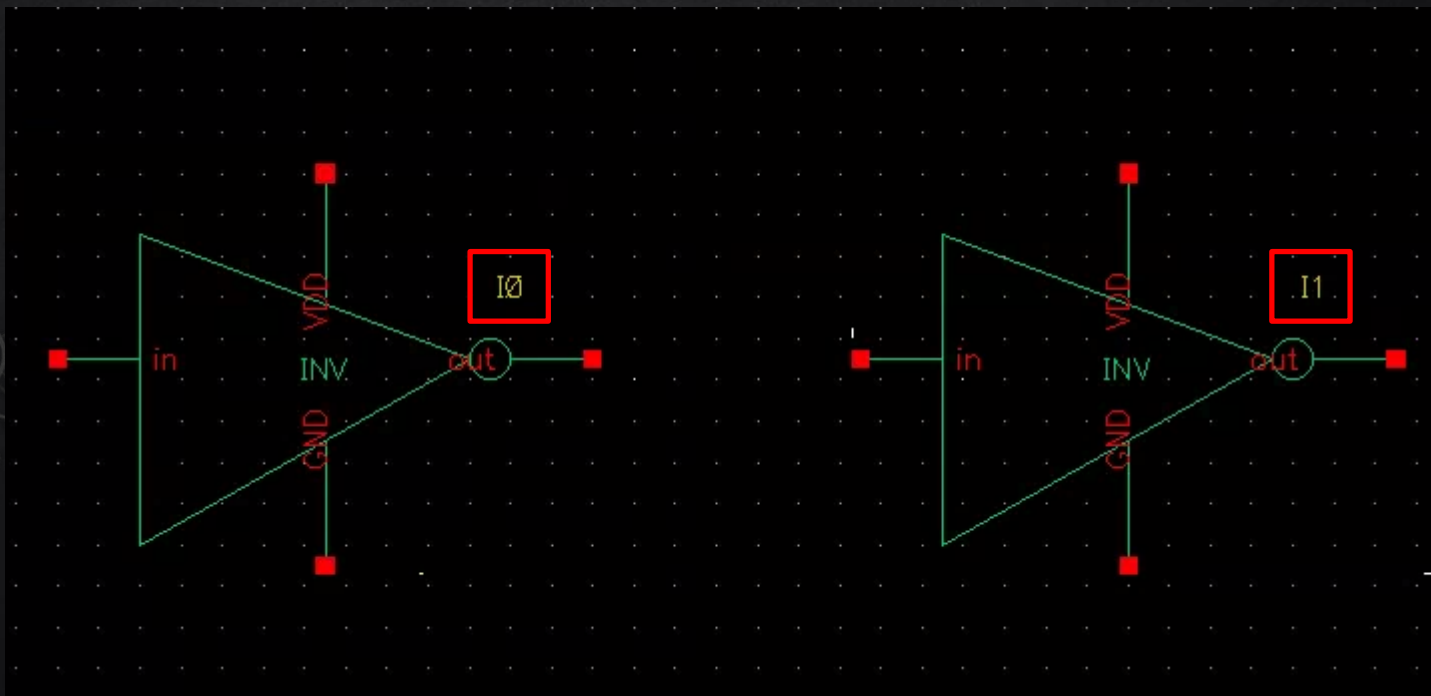
Two dialog boxes are open:

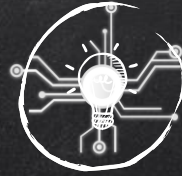
- Add Instance**: This dialog box is used to add a new instance to the schematic. It has tabs for "Hide", "Cancel", "Defaults", and "Help". The "Library" field is set to "test", the "Cell" field is set to "inverter", and the "View" field is set to "symbol". The "Names" field is empty. The "Array" section shows "Rows" and "Columns" both set to 1. The "Rotate" button is highlighted.
- Library Browser - Add Instance**: This dialog box is used to browse the library for a cell. It has tabs for "Show Categories", "Library", "Cell", and "View". The "Library" list shows "test" selected. The "Cell" list shows "inverter" selected. The "View" list shows "symbol" selected. The "Close" button is highlighted.



Inverter– use symbol on other cell(2/2)

Instance name will automatically be created





Inverter- CDL out

Output spice file according to schematic

1 **File** 2 **Export** 3 **CDL...**

icfb - Log: /home/lab_107/iyingbrad/CDS.log

Library Browser - Virtuoso®

Library	Cell	View
test	inverter	schematic
US_8ths	buffer	symbol
ahdlLib	inverter	
analogLib		
basic		
cdsDefTechLib		
functional		
rfExamples		
rfLib		
test		

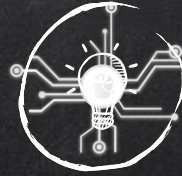
4 **Library Browser**

5 **Virtuoso® CDL Out**

6 **inv.cir**

Change file name (filename.rar)

21



Inverter- CDL out

Output spice file according to schematic

icfb - Log: /home/lab_107/iyingbrad/CDS.log

File Tools Options Help 1

- New cellview request for library "test".
- Open... saved.
- Import saved.
- Export saved.

Library Browser - Virtuoso®

Show Categories

Analysis Job Succeeded

Job '/home/lab_107/iyingbrad/schematic_folder/' that was started at 'Feb 23 02:16:04 2019' has succeeded

8

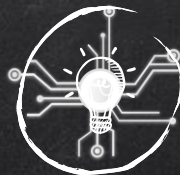
OK Cancel Help

Library Browser

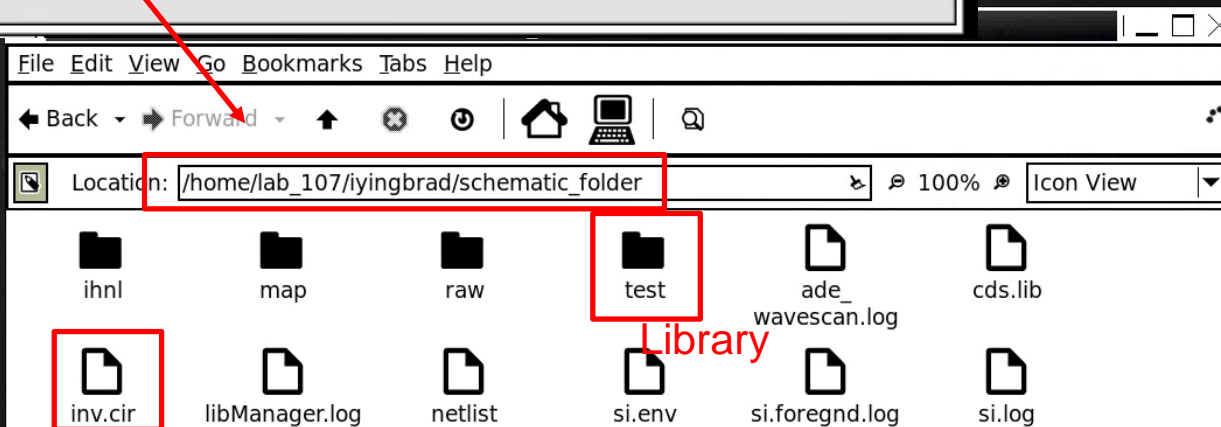
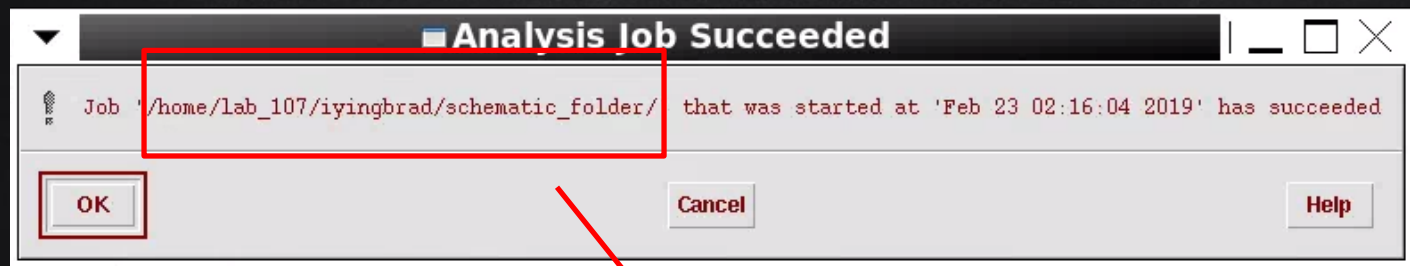
Top Cell Name	inverted
View Name	schematic
Library Name	test
Output File	inv.cir

22

Close Filters... Help



Inverter- CDL out



Schematic



THANKS!

