Overview

The IObundle CACHE is ....

Features

- feature1
- feature2

Benefits

- Compact and easy to integrate hardware and software implementation
- Can fit many instances in low cost FPGAs and ASICs
- Low power consumption

Deliverables

- ASIC or FPGA synthesized netlist or Verilog source code, and respective synthesis and implementation scripts
- ASIC or FPGA verification environment by simulation and emulation
- Bare-metal software driver and example user software
- User documentation for easy system integration
- Example integration in IOb-SoC (optional)

Resource	Used
LUTs	2168
Registers	1227
DSPs	0
BRAM	0

Resource	Used
ALM	826
FF	610
DSP	0
BRAM blocks	68
BRAM bits	72,768

Table 1: FPGA results for Kintex Ultrascale (left) and Cyclone V GT (right).
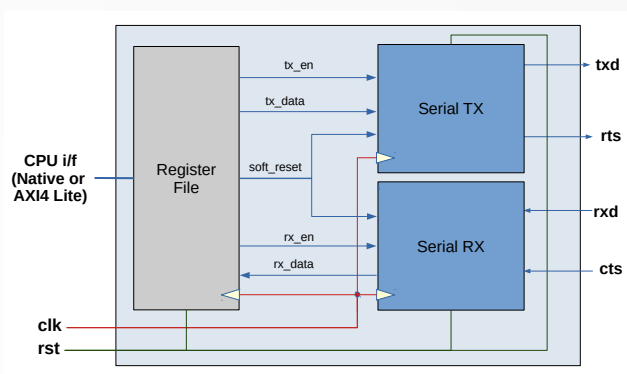
Block Diagram

Figure 1: High-level block diagram.

Implementation Results

The following are FPGA implementation results for two FPGA families. The following are FPGA implementation results for two FPGA families.