Overview

IOb-SoC is a RISC-V-based System-on-Chip Platform written in Verilog, which users can download for free, modify, simulate and implement in FPGA or ASIC. It supports stand-alone and boot loading modes, and can use an internal RAM or an external DDR controller via an L1/L2 cache system. The IP is currently supported in ASICs and FPGAs. Licensable commercial versions are available.

Features

- 32-bit RISC-V control CPU
- Support for Integer (I), atomic (A) and multiply/divide extensions (M)
- Instruction and data caches
- RS232 interfaces for viewing runtime messages
- Optional timer peripheral
- Optional Ethernet peripheral
- Frequency of operation at 167MHz on FPGA
- Needs external DDR4 memory controller IP

Benefits

- Compact and easy to integrate hardware and software implementation
- Can fit many instances in low cost FPGAs and ASICs
- Low power consumption

Deliverables

- ASIC or FPGA synthesized netlist or Verilog source code, and respective synthesis and implementation scripts
- ASIC or FPGA verification environment by simulation and emulation
- Bare-metal software driver and example user software
- User documentation for easy system integration
- Example integration in IOb-SoC (optional)

Block Diagram

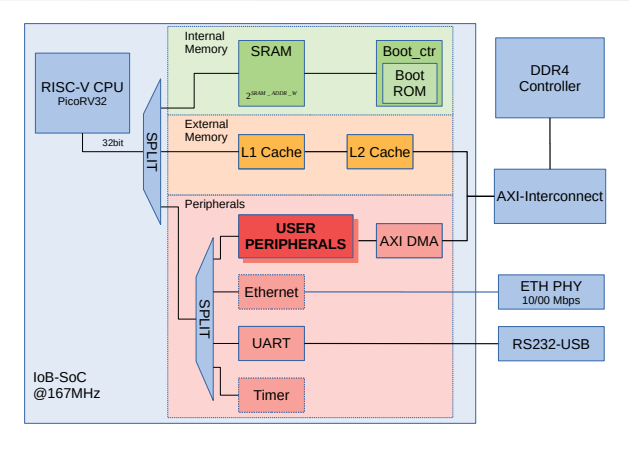

Figure 1: High-level block diagram

FPGA Resources

Resource	Used
LUTs	19893
Registers	22957
DSPs	7
BRAM	34.5

Resource	Used
ALM	1,541
FF	1230
DSP	3
BRAM blocks	38
BRAM bits	296,960
PIN	6

Table 1: FPGA results for Kintex Ultrascale (left) and Cyclone V GT (right)

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