CO 224 Lab 05 Bonus

Group 19

This documentation is regarding Logical Shift, Logical Right Shift operation working under this CPU model

OP-CODE (bits 31-24)	RD / IMM (bits 23-16)	RT (bits 15-8)	RS / IMM (bits7-0)

Bits (31-24) : OPCODE

Bits (23-16) : The register to be written

Bits (15-8) : The register to be read from the register file.

Bits (7-0) : Immediate value

The basic element in this circuit is the shifter comprising two AND gates and an OR gate. The SHIFT control signal here is designated by S. There are two inputs.

Fig 01: Logic Gate implementation

But here, CPU is getting an 8-bit input.so eight elements are required.

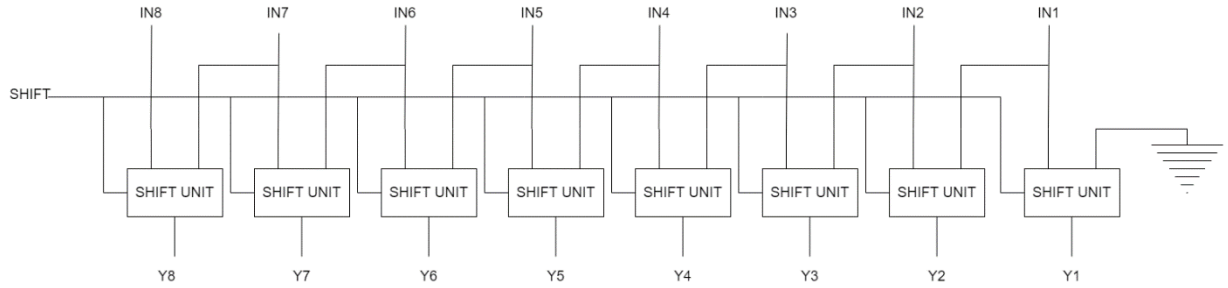
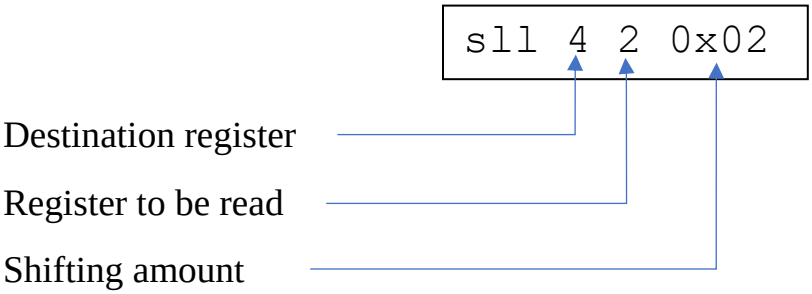


Fig 02: Left Shifting by one unit

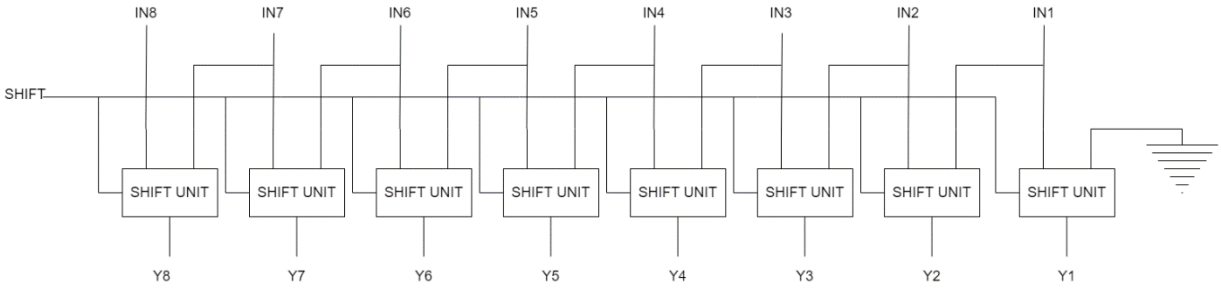
The above module is for shifting by one unit.to be shifted by multiple units, the CPU needs such above 8 modules.

The shift is implemented in four stages. the first stage shifting by either **0** or **1**, and the second stage shifting by either **0** or **2**. At the third stage shifting by either **0** or **4**. At the fourth stage shifting by either **0** or **8**. Shifts can be by any count up to **15** but shifts by more than the size of the register leave it all **0's**. shifting **up to 8** will get useful outputs.

Logical Left Shift

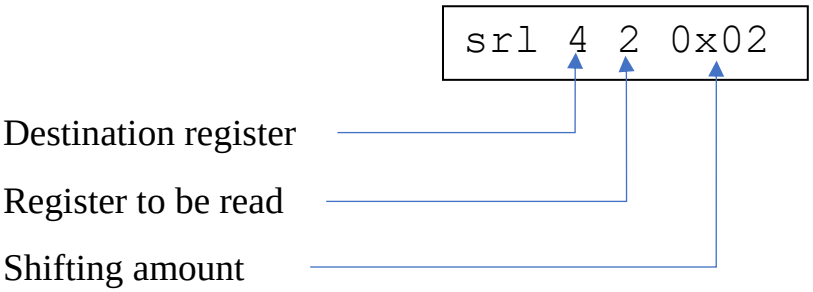


OPCODE regarding the Logical left shifting will be **0000_1000**.ALUOP will be **100**.shifting amount will be given as a **hexadecimal** value.



To be shifted by multiple units eight such modules are used.

Logical Right Shift



OPCODE regarding the Logical left shifting will be **0000_1001**.ALUOP will be **100**.shifting amount will be given as a **hexadecimal** value.

To get the logical right shift the mirror-image of the logical left shifter can be used.

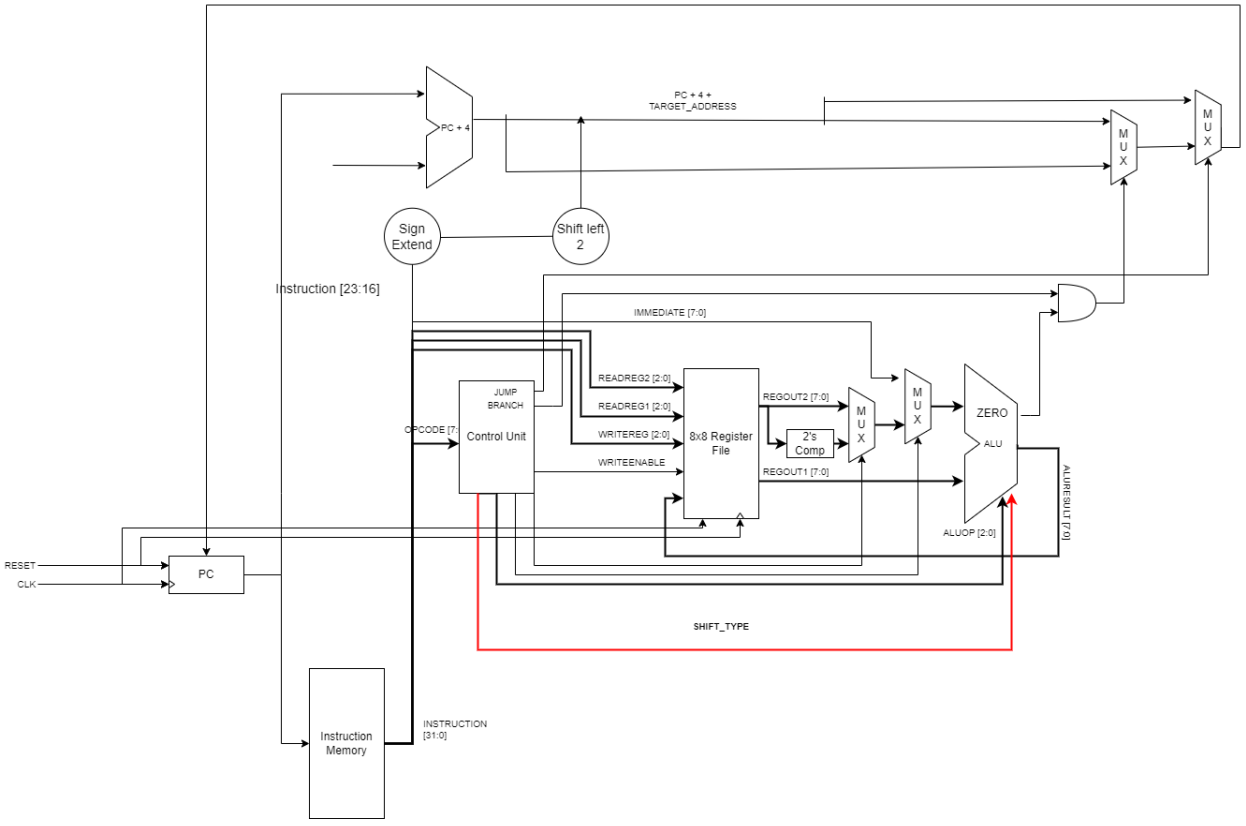


Fig 03: Datapath Diagram

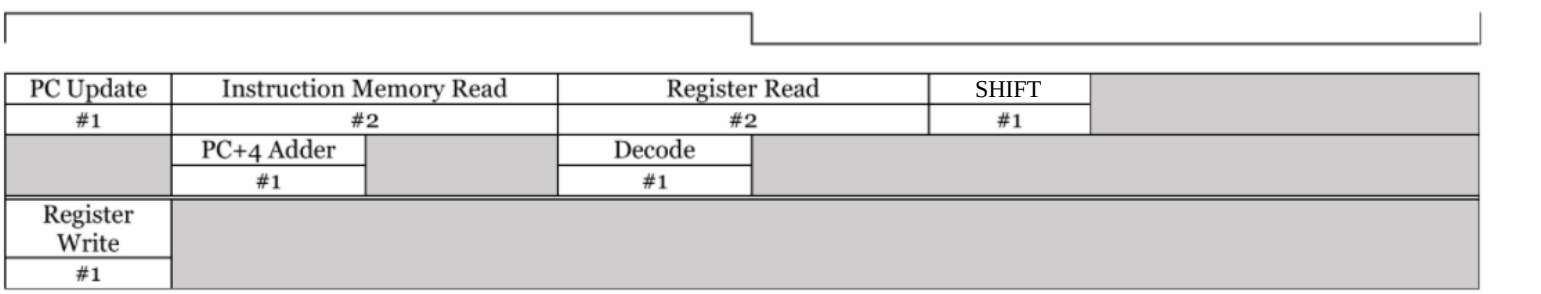


Fig 04: Timing Diagram