CO 224 Lab 06 Part 02

Comparison Report

Group 19

Read/write hit

For a read/write hit it will take 40 clock cycles to do the operation having only a data memory, but it will take only a single clock cycle to do the operation having a data memory with cache memory.

Read/write miss (dirty bit = 0)

With a data memory only, it will take only 5 clock cycles but with data memory and cache memory, it will take 21 clock cycles.

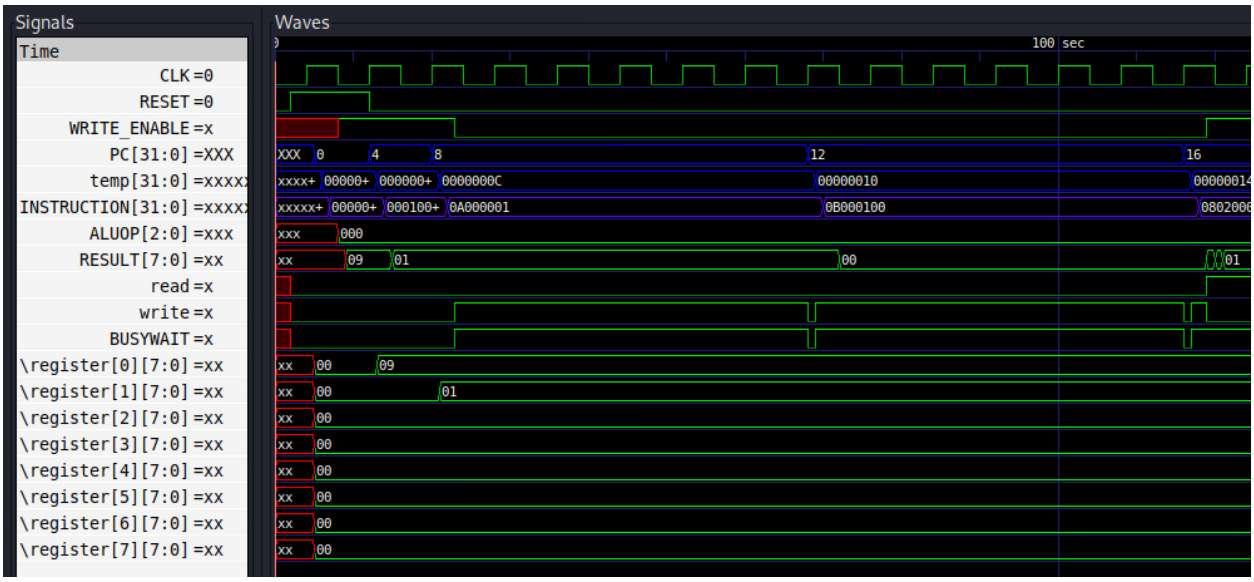
Read/write miss (dirty bit = 1)

With a data memory only, it will take only 5 clock cycles but with data memory and cache memory, it will take 42 clock cycles.

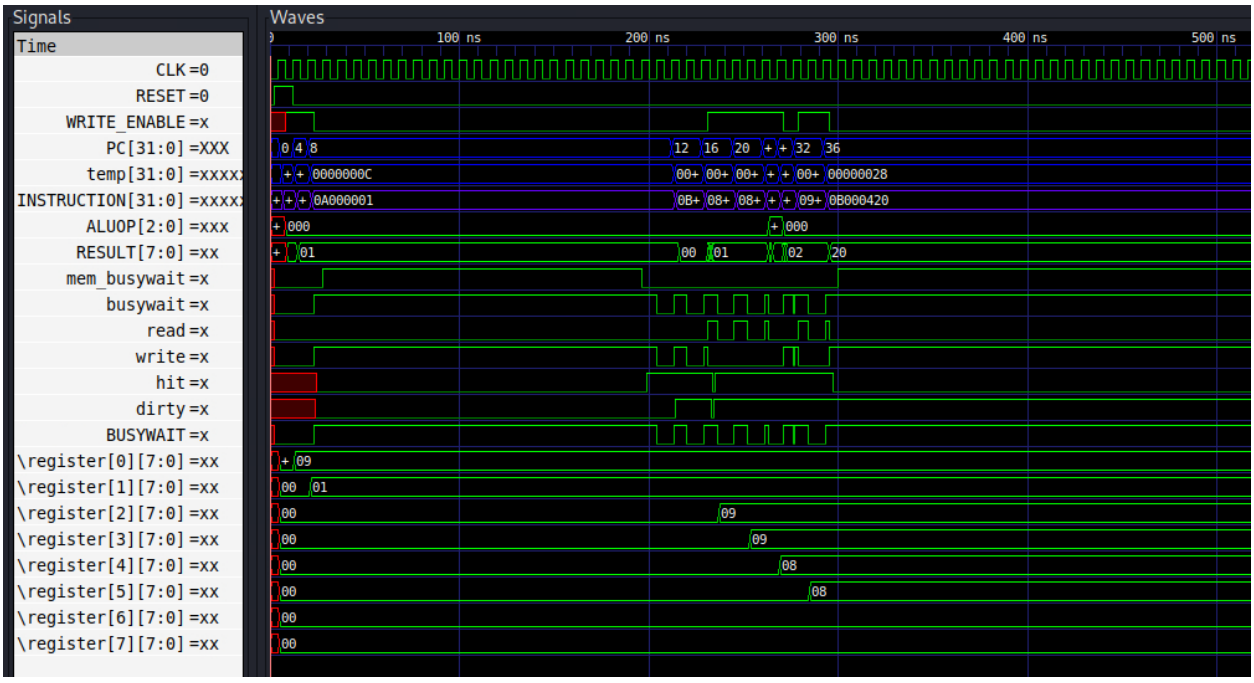
Conclusion

- CPU with cache memory will have better performance when the operation is read/write hit.
- When the operation is read/write miss, then the CPU without cache spend less clock cycles to complete operation than CPU with cache memory.

CPU timing diagram without the cache memory



CPU timing diagram with the cache memory



Instruction set used

```
loadi 0 0x09
loadi 1 0x01
swd 0 1
swi 1 0x00
lwd 2 1
lwd 3 1
sub 4 0 1
swi 4 0x07
lwi 5 0x07
lwi 6 0x20
swi 4 0x20
```

Time consumed for CPU without the cache memory – 365 units

Time consumed for CPU with the cache memory – 661 units